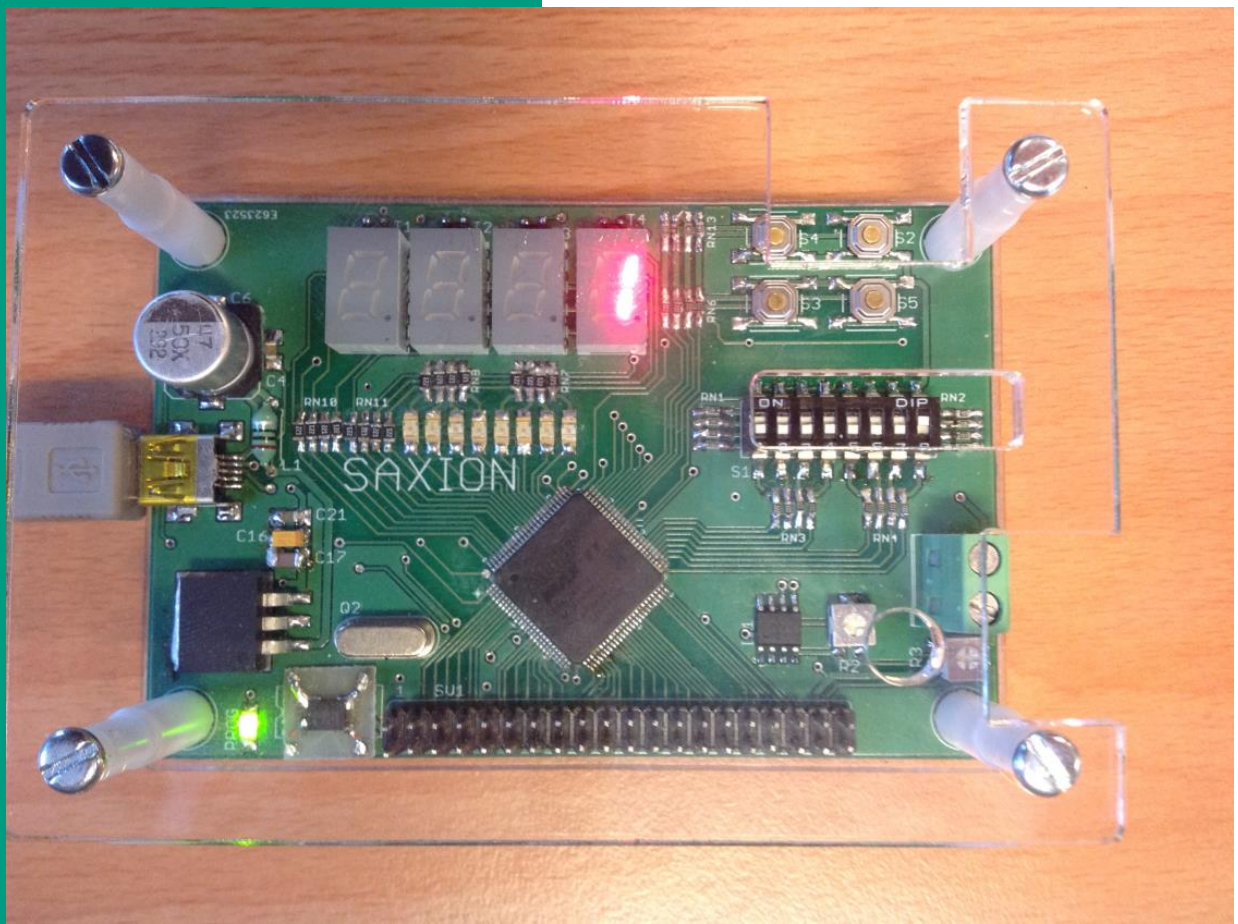
Very High Speed Integrated Circuits Hardware Description Language

Lesson 4
VHDL
Counters



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Lesson 4 outline

- Inferred latches(Chapter 9)
- Counters (Chapter 10)
- Simulating with Quartus simulator
- FPGA MAX II technology
- LUT
- I/O

Accidental Synthesis of inferred latch

```
ARCHITECTURE behavior OF ilatch IS
BEGIN
    PROCESS (A, B)
    BEGIN
        IF A = '0' THEN
            Output1 <= '0';
            Output2 <= '0';
        ELSE
            IF B = '1' THEN
                Output1 <= '1';
                Output2 <= '1';
            ELSE
                Output1 <= '0'; --latch inferred since
-- value is assigned to output 2 in the else clause
            END IF;
        END IF;
    END PROCESS;
```

Counters

```
USE  IEEE.STD_LOGIC_ARITH.all;
USE  IEEE.STD_LOGIC_UNSIGNED.all
```

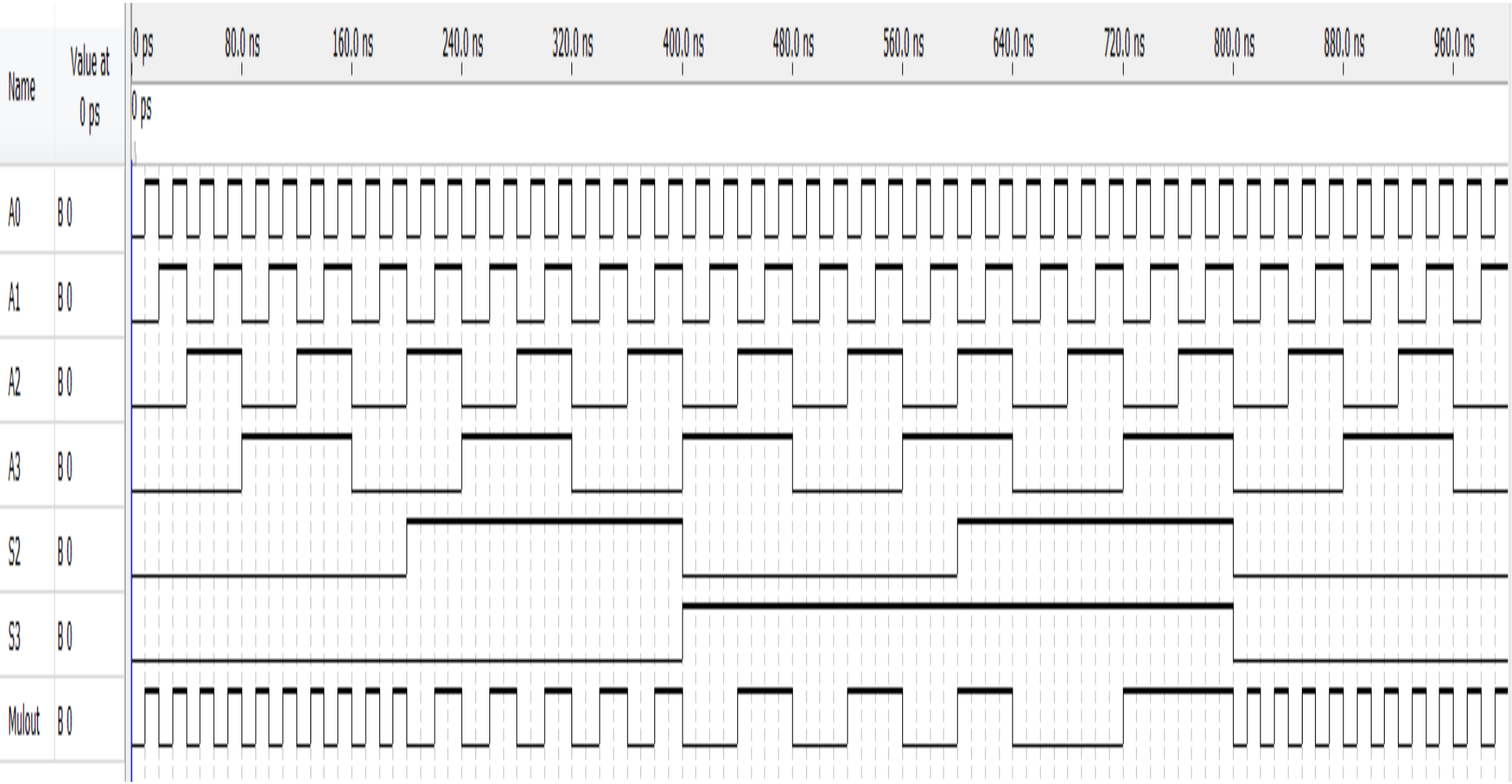
```
internal_count <= internal_count +1
```

Counters

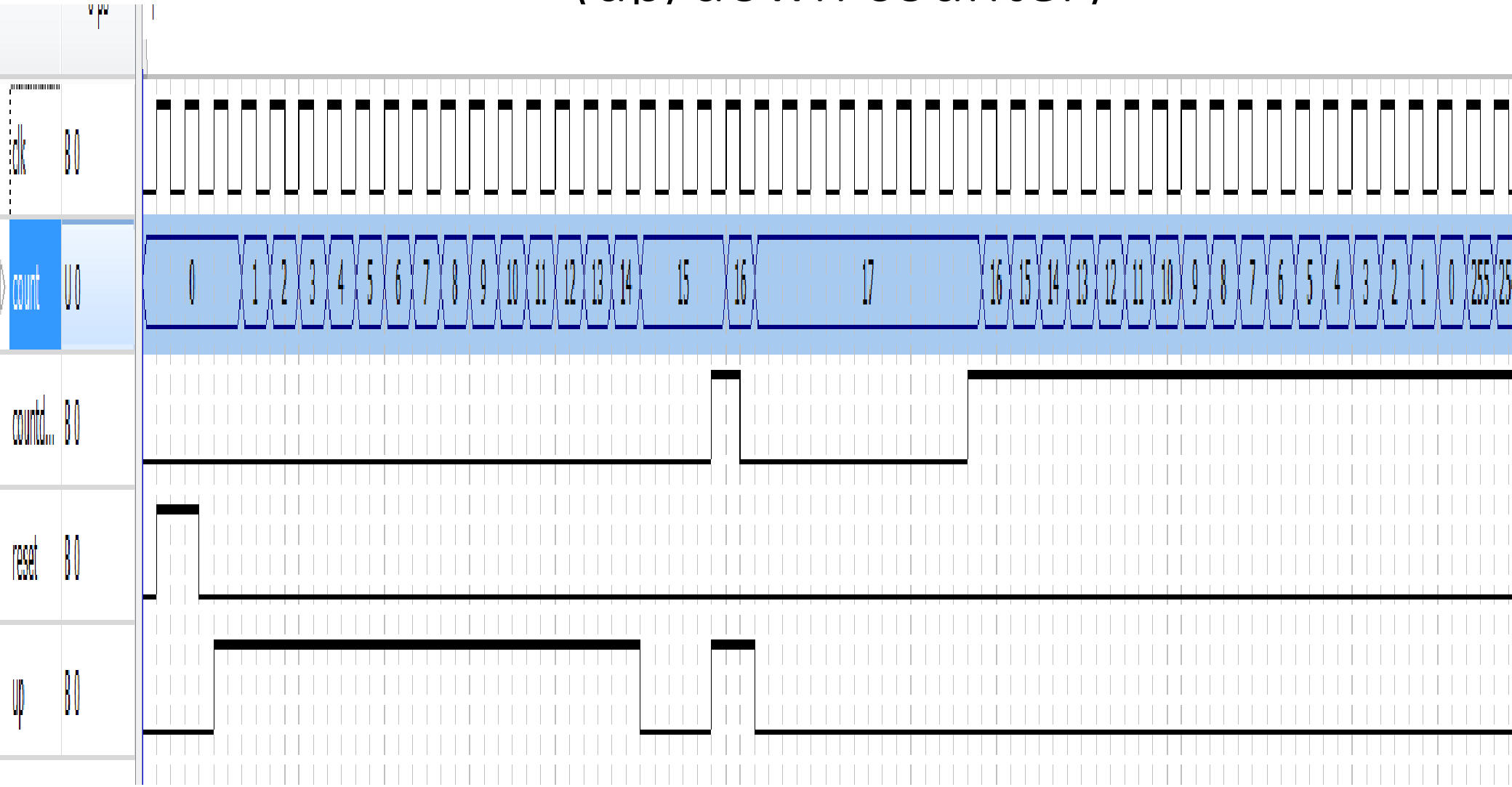
```
use IEEE.STD_LOGIC_1164.ALL;
 use IEEE.STD_LOGIC_ARITH.ALL;
 use IEEE.STD_LOGIC_UNSIGNED.ALL;


 entity Counter2_VHDL is
 port( Clock_enable_B: in std_logic;
 Clock: in std_logic;
 Reset: in std_logic;
 Output: out std_logic_vector(0 to 3));
end Counter2_VHDL;
```

```
architecture Behavioral of Counter2_VHDL is signal
temp: std_logic_vector(0 to 3);
 begin
 process(Clock,Reset)
            begin
           if Reset='1‘
                then temp <= "0000";
           elsif(Clock'event and Clock='1')
                 then if Clock_enable_B='0'
                 then if temp="1111"
                 then temp<="0000";
                    else temp <= temp + 1;
                end if;
               end if;
              end if;
   end process;
 Output <= temp;
end Behavioral;
```

Simulating with Quarter simulator (1) 4 to 1

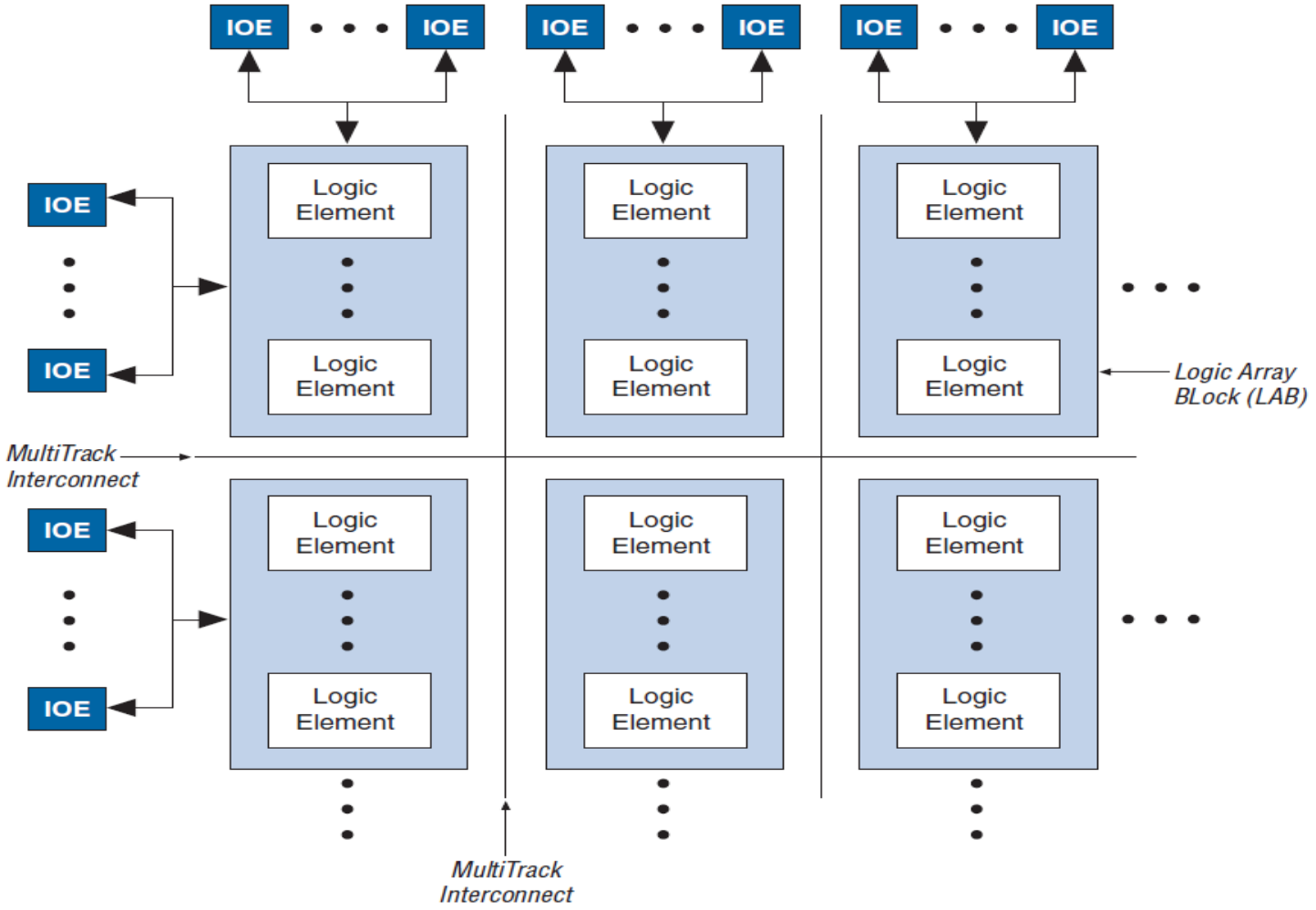


Simulating with Quarter simulator (up/down counter)



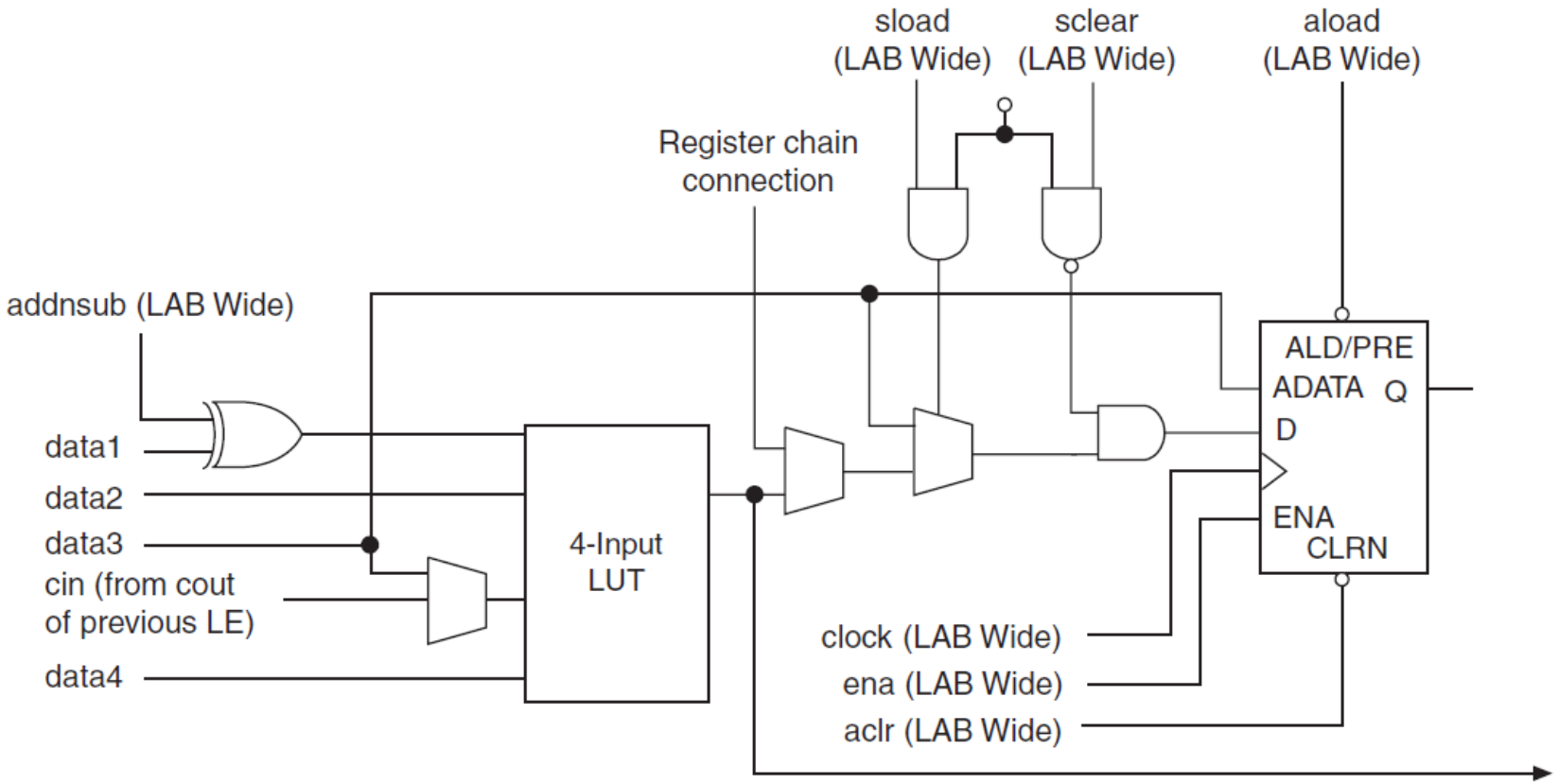
FPGA MAX II technology (1)

Figure 2–1. MAX II Device Block Diagram



FPGA MAX II technology (2)

Figure 3. MAX II LE with a 4-Input LUT



Look Up Table (LUT)

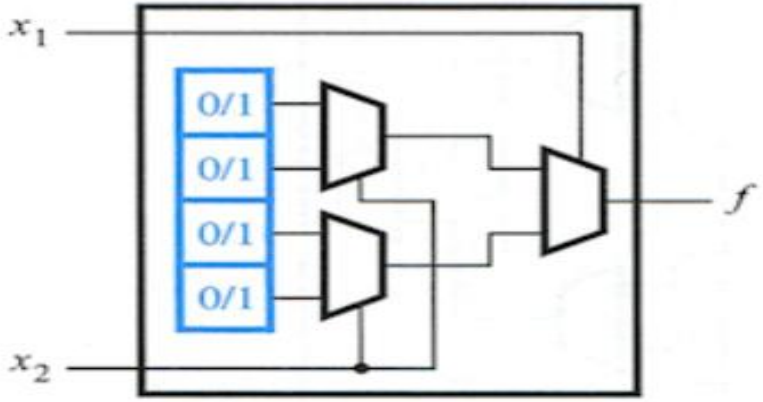
A LUT can be programmed so that it can contain any type of logic function.

Each logic block can only store small functions of several variables.

A LUT may be used as:

- A random combinatorial circuit with up to 4 inputs
- 16-bit memory

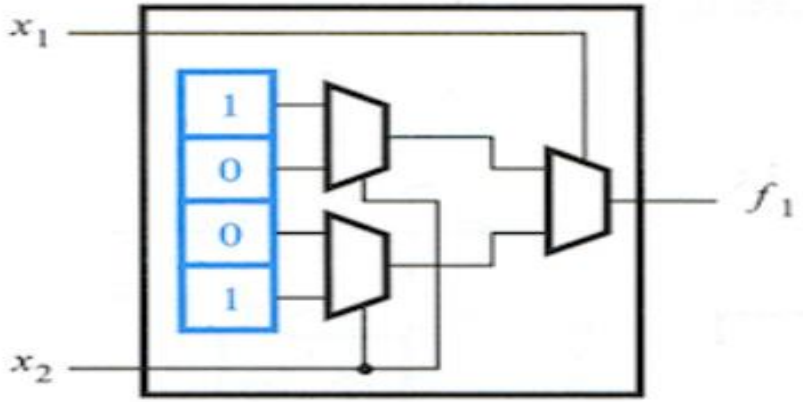
Look Up Table (LUT)



Circuit for a two-input LUT

x_1	x_2	f_1
0	0	1
0	1	0
1	0	0
1	1	1

$$f_1 = \bar{x}_1\bar{x}_2 + x_1x_2$$



Storage cell contents in the LUT

A two-input lookup table (LUT)

Table 1–1 shows the MAX II family features.

Table 1–1. MAX II Family Features

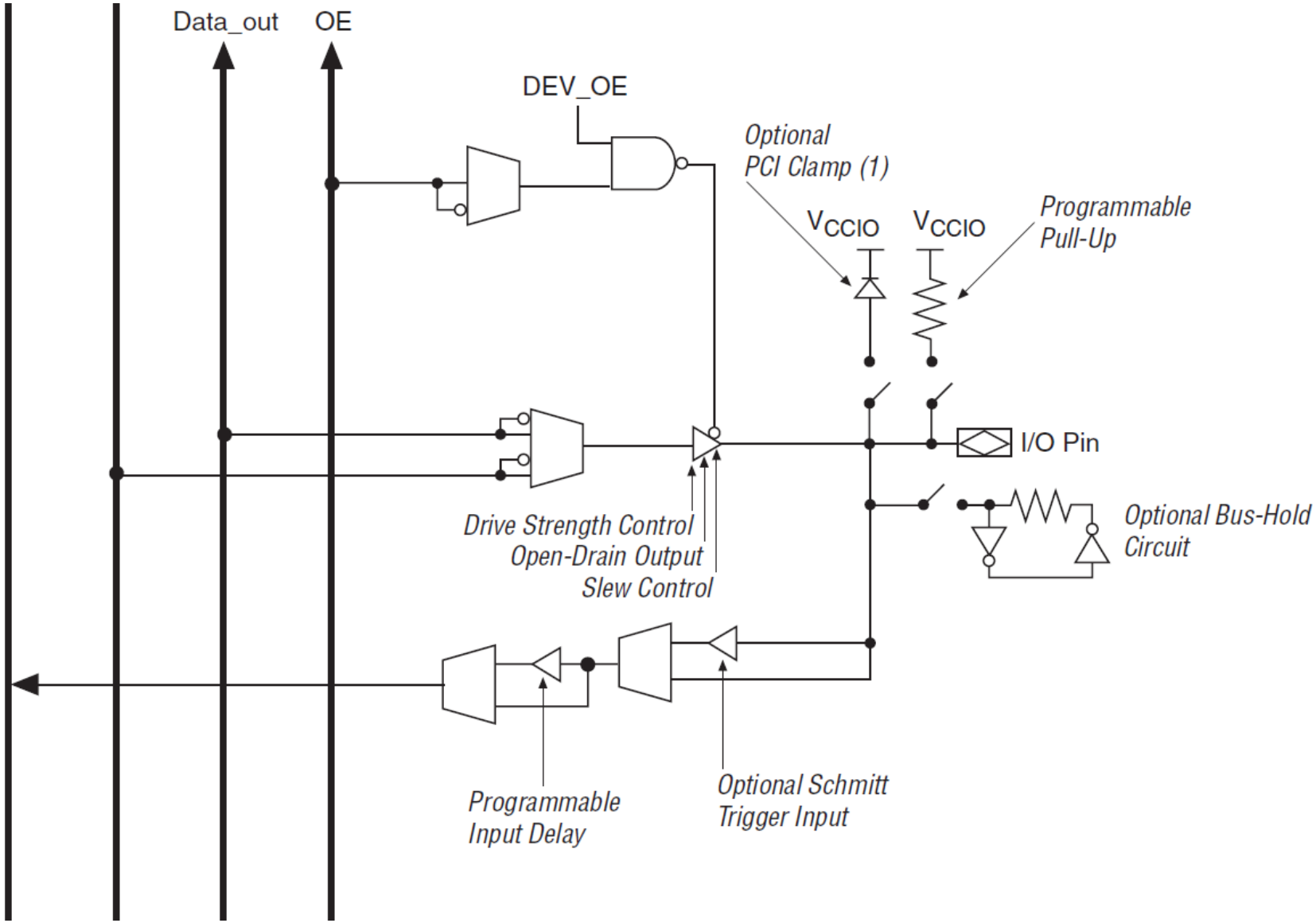
Feature	EPM240 EPM240G	EPM570 EPM570G	EPM1270 EPM1270G	EPM2210 EPM2210G	EPM240Z	EPM570Z
LEs	240	570	1,270	2,210	240	570
Typical Equivalent Macrocells	192	440	980	1,700	192	440
Equivalent Macrocell Range	128 to 240	240 to 570	570 to 1,270	1,270 to 2,210	128 to 240	240 to 570
UFM Size (bits)	8,192	8,192	8,192	8,192	8,192	8,192
Maximum User I/O pins	80	160	212	272	80	160
t_{PD1} (ns) *(1)*	4.7	5.4	6.2	7.0	7.5	9.0
f_{CNT} (MHz) *(2)*	304	304	304	304	152	152
t_{SU} (ns)	1.7	1.2	1.2	1.2	2.3	2.2
t_{CO} (ns)	4.3	4.5	4.6	4.6	6.5	6.7

I/O FEATURES

IOEs support many features, including:

- LVTTL and LVCMOS I/O standards
- 3.3-V, 32-bit, 66-MHz PCI compliance
- Weak pull-up resistors during power-up and in system programming
- Slew-rate control
- Tri-state buffers with individual output enable control
- Programmable pull-up resistors in user mode
- Unique output enable per pin
- Open-drain outputs
- Schmitt trigger inputs
- Programmable Drive Strength

I/O


Data_out
OE
DEV_OE
Optional
PCI Clamp (1)
VCCIO
VCCIO
Programmable
Pull-Up
I/O Pin
Drive Strength Control
Open-Drain Output
Slew Control
Optional Bus-Hold
Circuit
Programmable
Input Delay
Optional Schmitt
Trigger Input

Assignment week 4

- Do self test chapter 9 ,10
- Do the exercises chapter