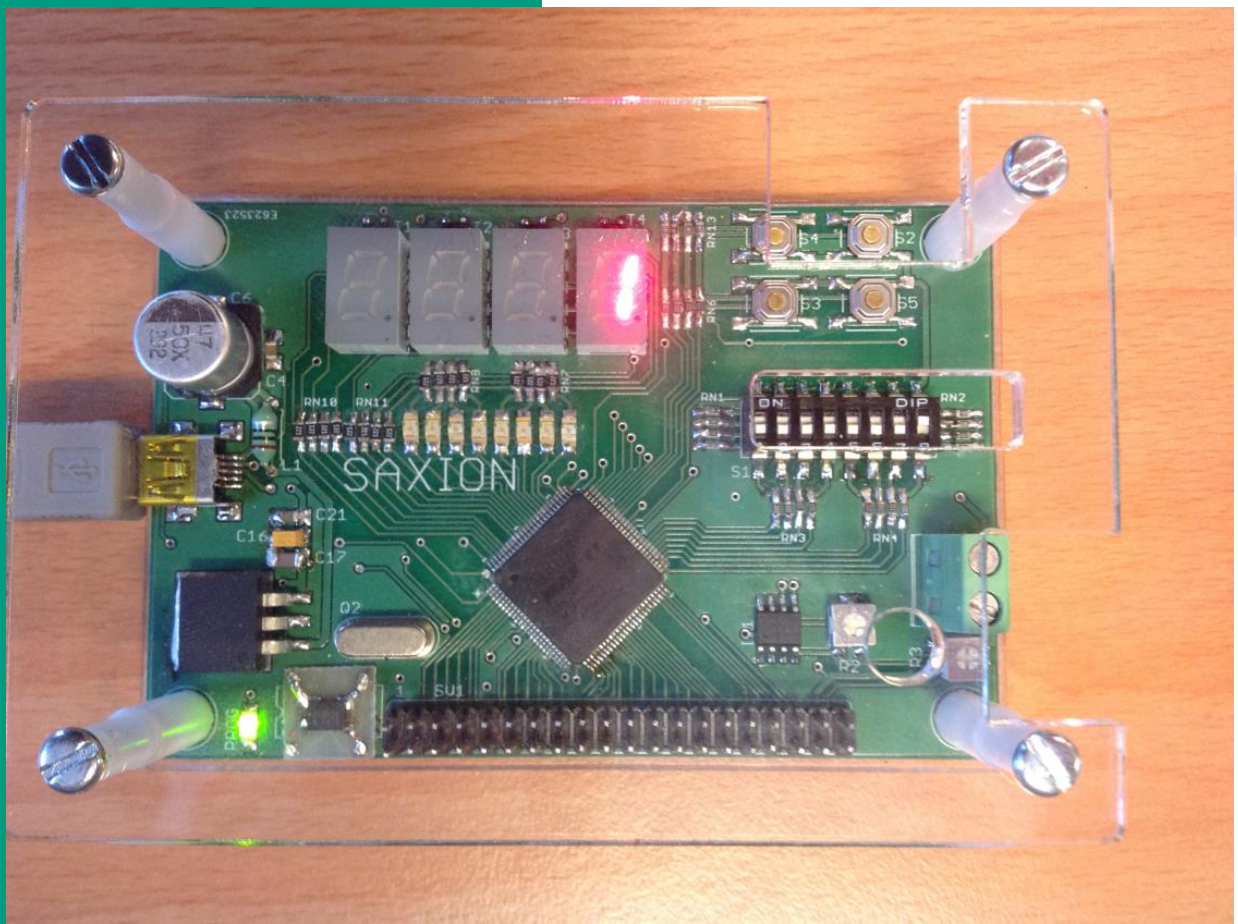
Very High Speed Integrated Circuits Hardware Description Language

Lesson 6
VHDL Hierarchy



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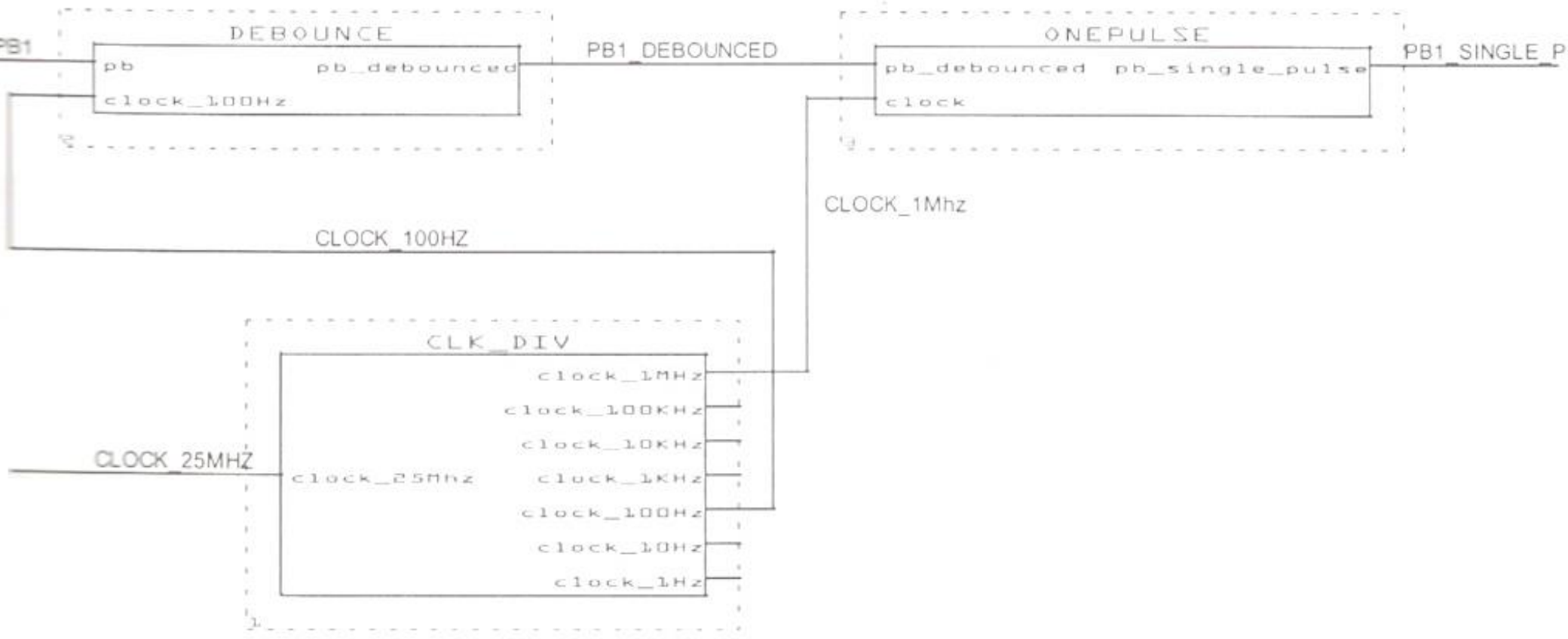
Lesson 6 outline

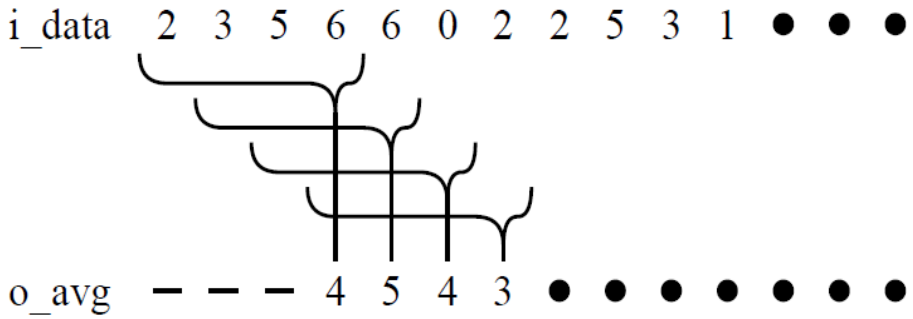
- Hierarchy
- Testbenches
- Final Assignments

15 Hierarchy in VHDL Synthesis models



Final assignment: Moving average filter

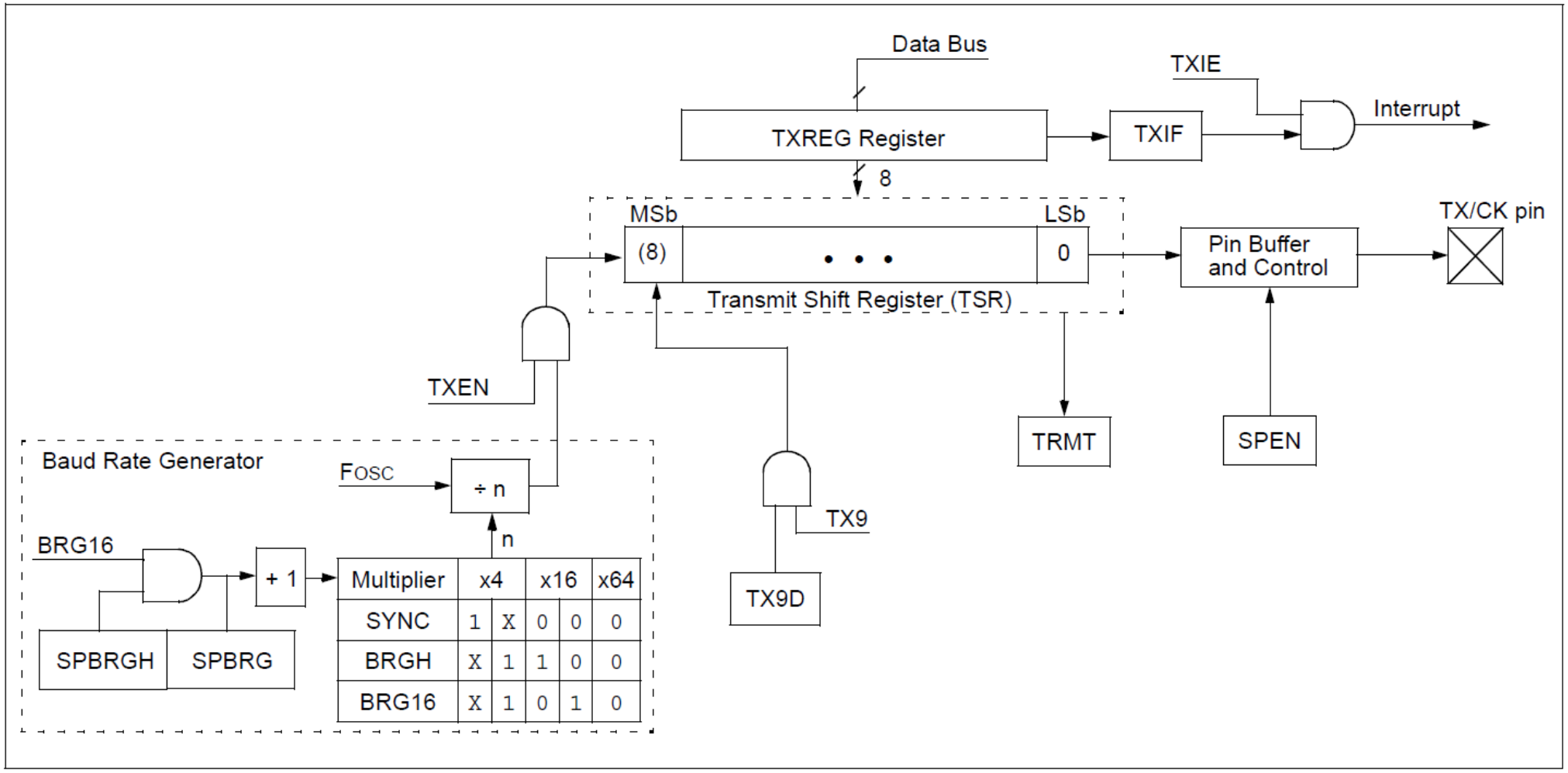
data. When each new data item is received, the output is the average of the four most recently received data.



$$avg_t = \left(x_{t-3} + x_{t-2} + x_{t-1} + x_t\right)/4$$

Final assignment: Serial send (9600 baud)

FIGURE 12-1: EUSART TRANSMIT BLOCK DIAGRAM



17 Conclusion

- Just an introduction of VHDL basics
- Many templates and examples IEEE
- Many online examples