单周期CPU

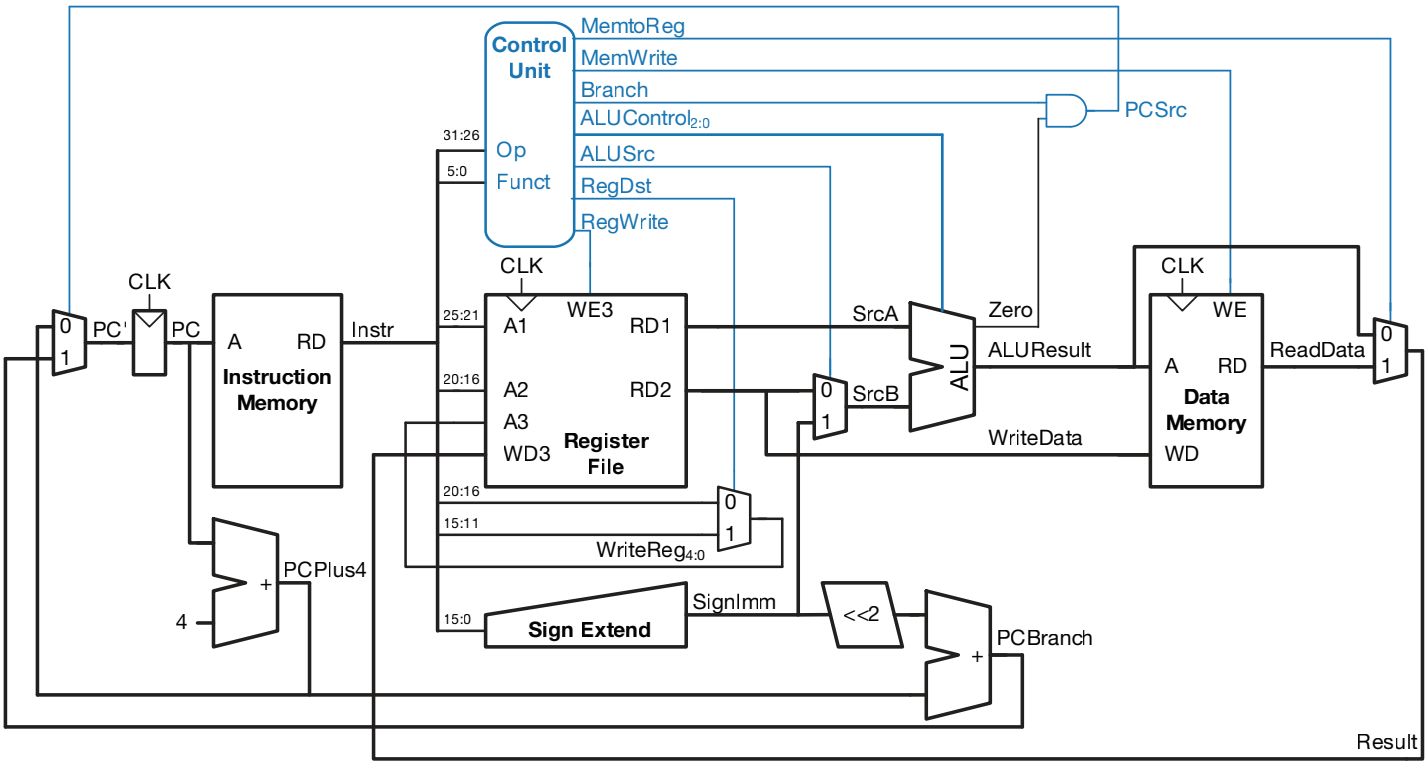


Figure 7.11 Complete single-cycle MIPS processor

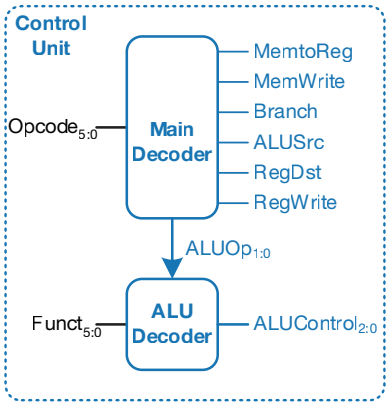


Figure 7.12 Control unit internal structure

Table 7.3 Main decoder truth table

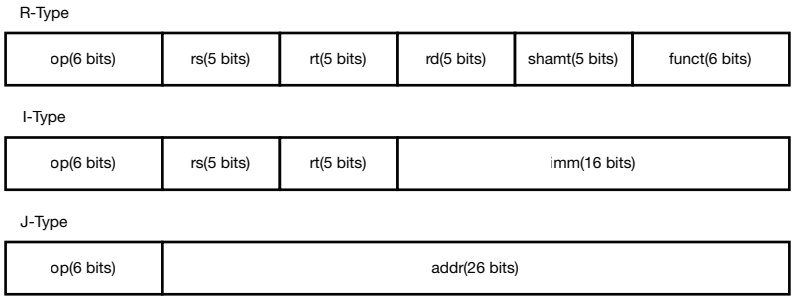
Instruction	Opcode	RegWrite	RegDst	ALUSrc	Branch	MemWrite	MemtoReg	ALUOp
R-type	000000	1	1	0	0	0	0	10
lw	100011	1	0	1	0	0	1	00
sw	101011	0	X	1	0	1	X	00
beq	000100	0	X	0	1	0	X	01

Table 7.1 ALUOp encoding

ALUOp	Meaning
00	add
01	subtract
10	look at funct field
11	n/a

Table 7.2 ALU decoder truth table

ALUOp	Funct	ALUControl
00	X	010 (add)
X1	X	110 (subtract)
1X	100000 (add)	010 (add)
1X	100010 (sub)	110 (subtract)
1X	100100 (and)	000 (and)
1X	100101 (or)	001 (or)
1X	101010 (slt)	111 (set less than)



R-type		
funct		
100000	add	[rd]=[rs]+[rt]
100010	sub	[rd]=[rs]-[rt]
100100	and	[rd]=[rs]&[rt]
100101	or	[rd]=[rs]|[rt]
101010	slt	[rs]<[rt]?[rd]=1:[rd]=0
Memory		
opcode		
100011	lw	[rt]=[Address]
101011	sw	[Address]=[rt]
Branches		
opcode		
000100	beq	if([rs]==[rt]) PC=BTA