

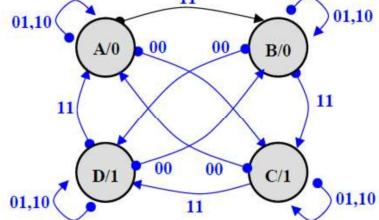
# Lab 5

Monday, December 7, 2020 4:54 PM

Name:

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- 5) [20] At right is the state diagram for a Moore sequential circuit which monitors two inputs  $X_1X_0$ . When the two inputs  $X_1X_0$  are 00, the output Z toggles at every clock. When the two inputs  $X_1X_0$  are 11, the output Z toggles at every other clock. When the two inputs  $X_1X_0$  are different, the output Z holds its state and does not change until the inputs are equal again.



Use the following table with the gray code assigned (easier to fill in the K-Map if use gray code)

Present State (Q)		Input (X)	Output (Z)	Next State (Q+)		Flip Flop Transition	
State Name	Q <sub>1</sub> Q <sub>0</sub>	X <sub>1</sub> X <sub>0</sub>	Z	State Name	Q <sub>1</sub> <sup>+</sup> Q <sub>0</sub> <sup>+</sup>	J <sub>1</sub> K <sub>1</sub>	J <sub>0</sub> K <sub>0</sub>
A	0 0	0 0	0	C	1 0 0 0	1 X	1 X
	0 1	0 1	0	A	0 0 0 1	0 X	0 X
	1 1	1 1	1	B	0 1 1 0	0 X	1 X
	1 0	1 0	0	A	0 0 1 0	0 X	0 X
B	0 1	0 0	0	D	1 1 0 0	1 X	1 X
	0 1	0 1	0	B	1 0 1 0	0 X	0 X
	1 1	1 1	1	B	1 0 0 1	0 X	1 X
	1 0	1 0	0	B	1 0 1 1	0 X	0 X
C	1 1	0 0	1	A	0 0 0 0	X X	X X
	0 1	0 1	0	C	0 1 1 1	0 0	0 0
	1 1	1 1	0	C	0 1 0 0	X X	X X
	1 0	1 0	1	C	0 1 1 0	0 0	0 0
D	1 0	0 0	0	B	0 0 1 0	X X	1 X
	0 1	0 1	0	D	0 1 0 0	1 0	1 X
	1 1	1 1	1	A	0 1 1 0	X X	0 0
	1 0	1 0	0	D	0 1 0 1	1 0	X X

5.a) [TA-4] Fill in the **output** and the **next state** columns of the table

5.b) [TA-4] Fill in the the next state columns of the table

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Flip Flop Transition indicates what is the input needed for J and K to cause the change from the present state to the next state. Before we can fill the Flip Flop Transition columns of the table, complete the JK truth table. Note: Action can be the following H = Hold (don't change), S=Set, R=Reset, T=Toggle (change).

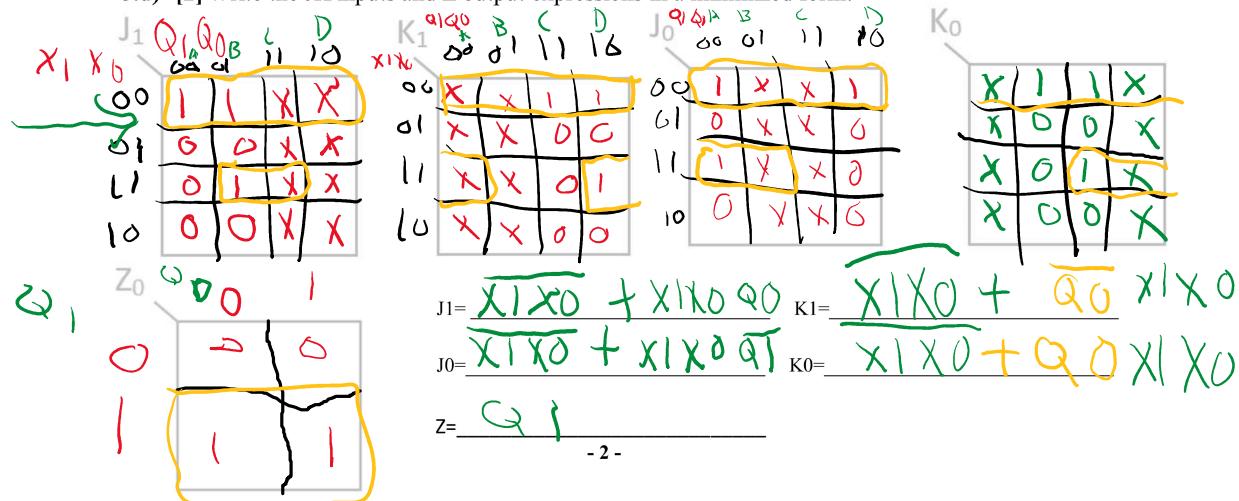
Then complete the **JK Excitation Table** that permits the Flip Flop to change from  $Q$  to  $Q^+$

J	K	Q	Action	$Q^+$	<b><math>Q \rightarrow Q^+ \text{ Action } JK</math></b>
0	0	0	Hold	0	$0 \rightarrow 0 \quad H \ 0 \ 0 \quad 0 \ X$
		1		1	$R \ 0 \ 1$
0	1	0	Reset	0	$0 \rightarrow 1 \quad T \ 1 \ 1 \quad 1 \ X$
		1		0	$S \ 1 \ 0$
1	0	0	Set	1	$1 \rightarrow 0 \quad T \ 1 \ 1 \quad X \ 1$
		1		0	$R \ 0 \ 1$
1	1	0	Toggle	1	$1 \rightarrow 1 \quad T \ 0 \ 0 \quad X \ Y$
		1		0	$T \ 1 \ 0$

In the table on the first page highlight the values of  $Q_1$ ,  $Q_1^+$  and area under  $J_1 \ K_1$  in one color, use a different highlight for  $Q_0$ ,  $Q_0^+$  and  $J_0 \ K_0$ . Using the Excitation table compare the same color  $Q \rightarrow Q^+$  to fill the value under corresponding  $J \ K$  to complete the JK Transition table

5.e) [2] Fill the JK input maps for each of the two flip-flops. Note how easy it is to fill in from the table because we are using the gray code for numbering.

5.d) [2] Write the JK inputs and Z output expressions in a minimized form:



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$Z = \bar{Q}_1$

$J_1 = X_1 \bar{X}_0 + \bar{X}_1 X_0$

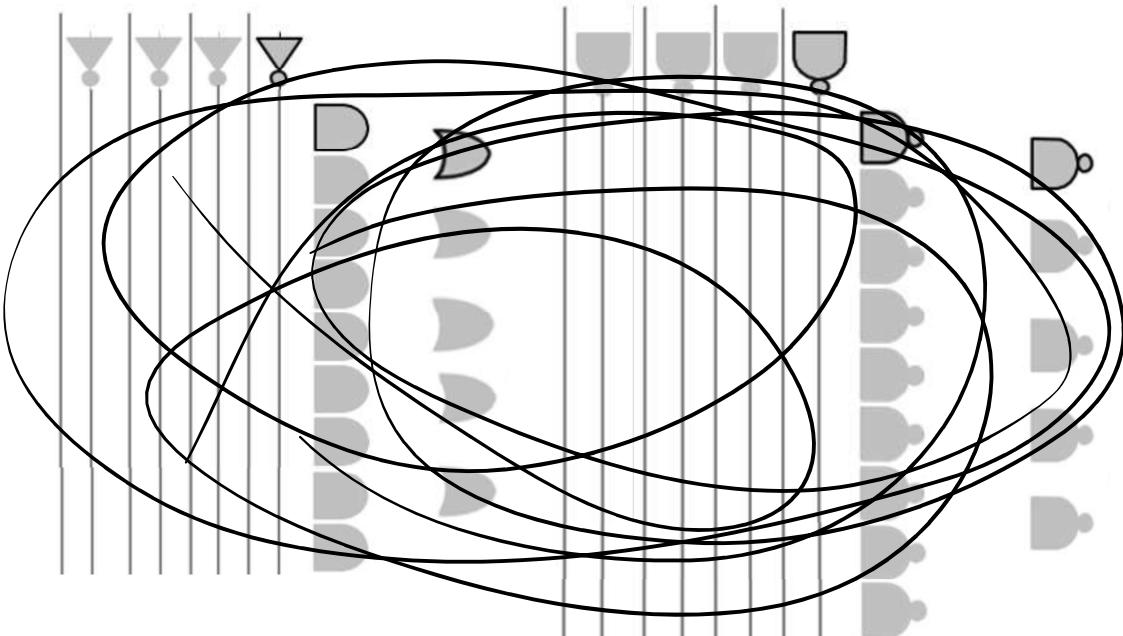
$K_1 = \bar{X}_1 \bar{X}_0 + \bar{Q}_0 \bar{X}_0$

$J_0 = \bar{X}_1 \bar{X}_0 + \bar{X}_1 X_0$

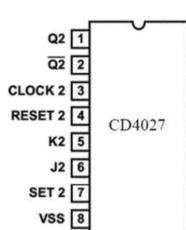
$K_0 = \bar{X}_1 \bar{X}_0 + \bar{Q}_0 \bar{X}_0$

Design the simplest circuit with NOT-AND-ORs, no limit on inputs

Design the simplest All NAND circuits, no limits on # of inputs



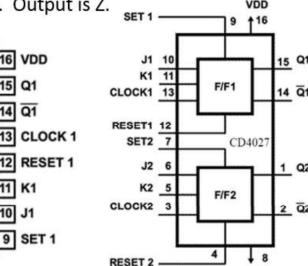
- 5.e [Petrie - 80] Design the circuit above using the **CD4027BE** dual JK flip-flop in your kit and as many 2, 3, or 4 input NAND gates as needed. Inputs are  $X_1$  and  $X_2$ , Clock and Reset. Reset should reset both Flip Flops so the system starts in State A = 00. Output is Z.



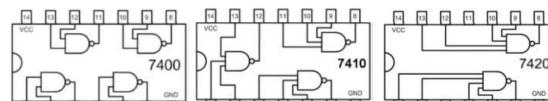
(a) Pinout

(b) Functional Diagram

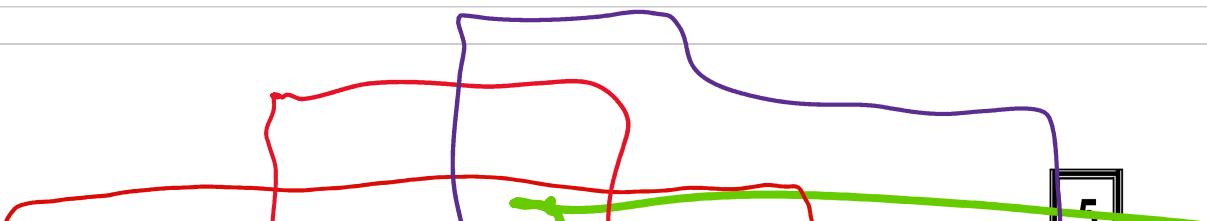
CD4027BE dual JK flip-flop



Note for the CD4027: the clocks are activated on the rising edge (going from 0 to 1 – when pushing down the pulse switch to turn on). If the pulse switch does not work well as the clock, use a toggle switch, sometimes the switches “bounce”. Note that the CD4027 has a SET and a RESET. These are used to clear to 0 or set the values to the first state of the state diagram. Note both SET and RESET are active high. If you assigned State A as 00 then to start we need to RESET both Flip Flops, so link them together and connect to one of the switches. So you will have the two ~~sw~~ and the RESET for the circuit linked to the Switches. You will not be using SET, so tie it to ground so it won't be activated, note it is active high. VDD is equivalent to VCC and VSS is equivalent to GND



Determine how many NAND Chips you need



• CDA3201 • Intro to Logic Design •

Lab Assignment

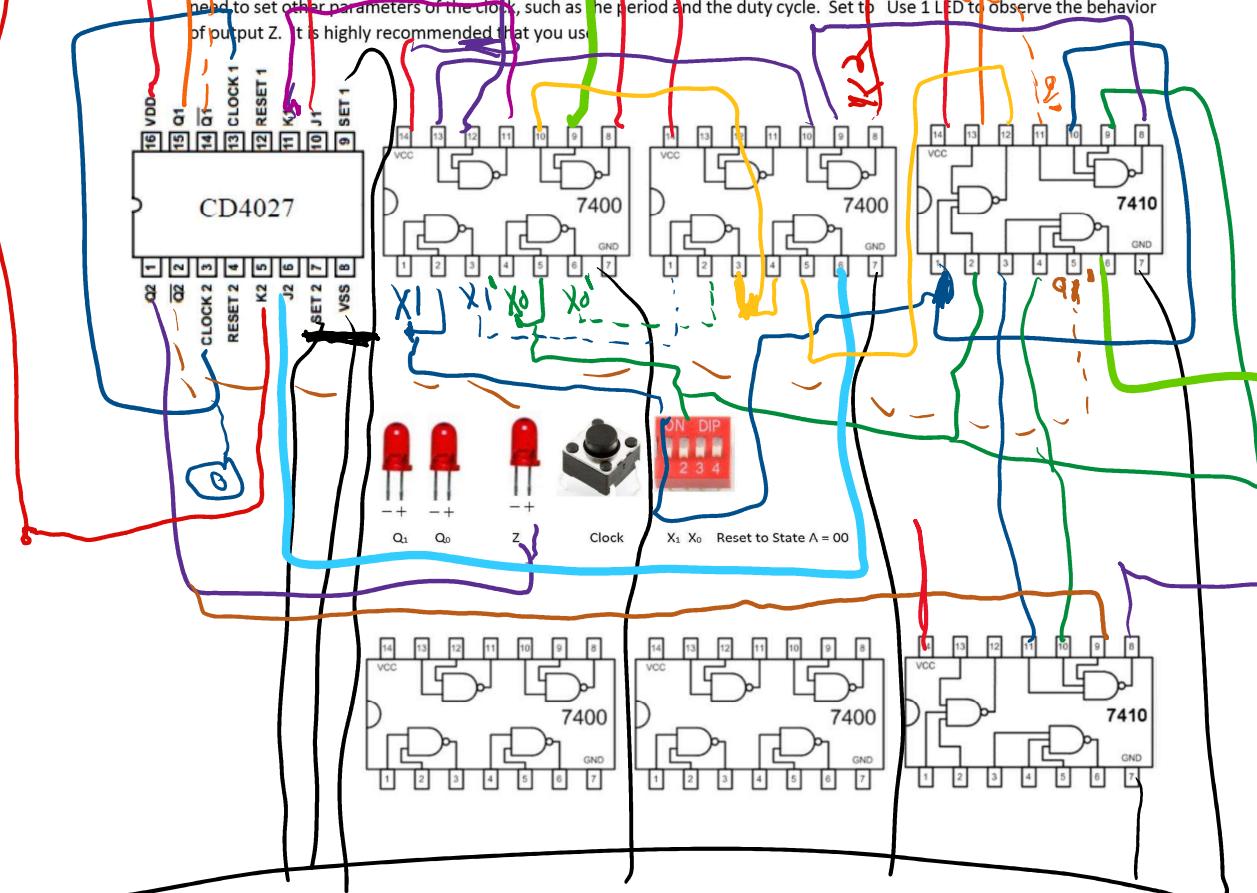
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YOU DO NOT NEED TO DO QUARTUS FOR LAB 5

5.f) [4] Verify the circuit design/behavior by implementing the circuit using Quartus. In Quartus you can group inputs X1 and X2 to count, the Clock is set using the same interface as you select to produce binary count but select Clock instead. You will need to set other parameters of the clock, such as the period and the duty cycle. Set to Use 1 LED to observe the behavior of output Z. It is highly recommended that you use



- 5.e) [8] Build the above circuit using the CD4027 dual JK flip-flop and as many 2, 3 or 4 input NAND gates as needed on your breadboard and then connect it to your test platform to test it. Use 2 logic switches for inputs X1 and X2 and 1 pulse switch for the Clock. Use 1 LED to observe the behavior of output Z.

Take a picture and create a portfolio. Upload into Canvas after it is graded.