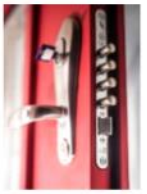
Lab1a-SimplifyingCircuitSimulations-PETRIE.v2

Wednesday, October 7, 2020 12:05 PM

• CDA3201 • Introduction to Logic Design • Dr. Maria Larrondo Petrie **Lab Assignment** **1***

Name: Dov Cattan **ID#:** **Grade:** /15

** This lab assignment is based on, but greatly expands Lab 1 in the FAU Logic Design Lab Manual by Dr. Bassem Alhalabi.*



The Problem: A security firm contracts you to build circuits that will let the guard know whether to open a door to a secure room. The engineer gives you the equation below, based on the value of 4 conditions: if it is a person (C=1), if it has badge (B=1), if it is a service animal or robot (A=1), if fingerprint is on file (D=1). The door will open (X=1), only if:

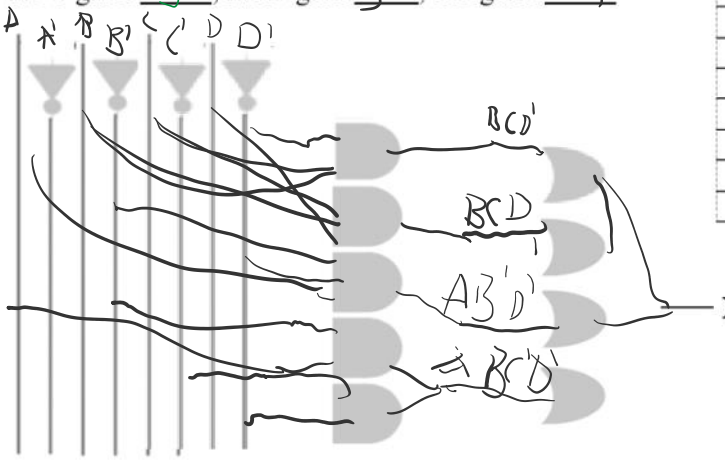
$$X = B C \overline{D} + B C D + A \overline{B} \overline{D} + A B \overline{C} \overline{D}$$

1.1 Construct the Truth Table (at right)

ABCD	BCD'	BCD	AB'D'	ABC'D'	X
0000					
0001					
0010					
0011					
0100					
0101					
0110					
0111					
1000					
1001					
1010					
1011					
1100					
1101					
1110					
1111					

1.2 Plan the circuit: Plan the circuit in pencil using the template below. Outline and number only the gates needed, draw however many inputs are needed for each gate to implement X exactly as specified. Number each gate used 1, 2, 3 ... How many gates do you need for this circuit?

NOT gates 3, AND gates 5, OR gates 4



$$X = B C \overline{D} + B C D + A \overline{B} \overline{D} + A B \overline{C} \overline{D}$$

Look at the 7400 Series Family of Integrated Circuit in 1.4 on the next page. There are 2-input, 3-input and 4-input AND chips, but no 4-input ORs, so make the necessary changes to 1.2 in pencil to use only 2-input ORs.

1.3 Simulate the circuit: Create a project in Quartus called **lab1-PETRIE-yourlastname** following Dr. Petrie's step by step videos and guide. Create a new Block Diagram/Schematic (.bdf file) using the exact same name as the project. Construct the design you did in 1.2. Note there are no 4-input OR gate available. Save the schematic. Now follow the step by step to compile and correct any errors by correcting the .bdf file (don't worry about warnings). Save and compile again until no more errors. Generate a Timing Diagram (called Vector Waveform file, .vwf file), save with the exact same name as the project. Group the input variables and use the counter to set the values. Simulate. Make sure to save the project, the .bdf and .vwf files often. Check the .vwf to verify it produces same results as Truth Table 1.1. If it does not match the Truth Table, then determine if error is in the Truth Table or your design, or your Quartus Schematic. Save and keep the project and files to expand the Block Diagram with the rest of Lab 1. Take a picture or snip of the bdf and vwf windows including their file names for inclusion in the portfolio.

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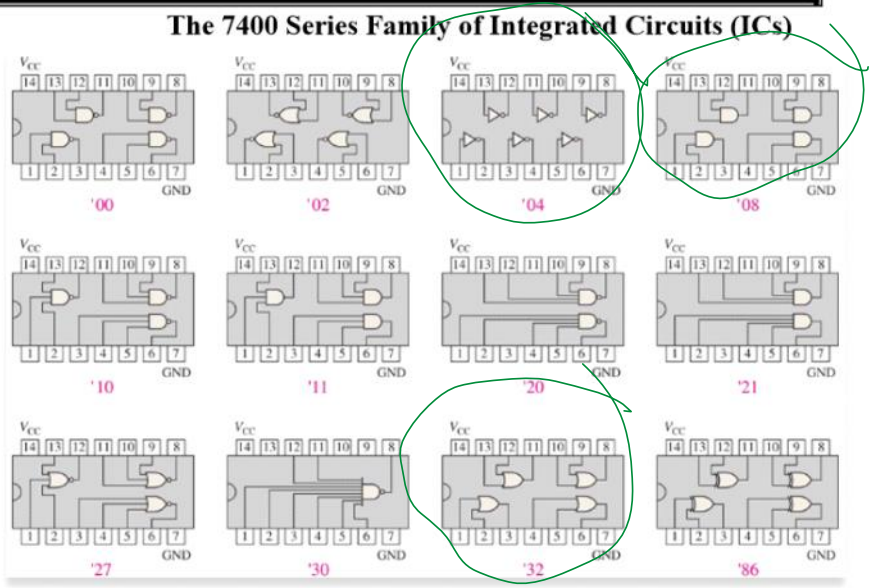
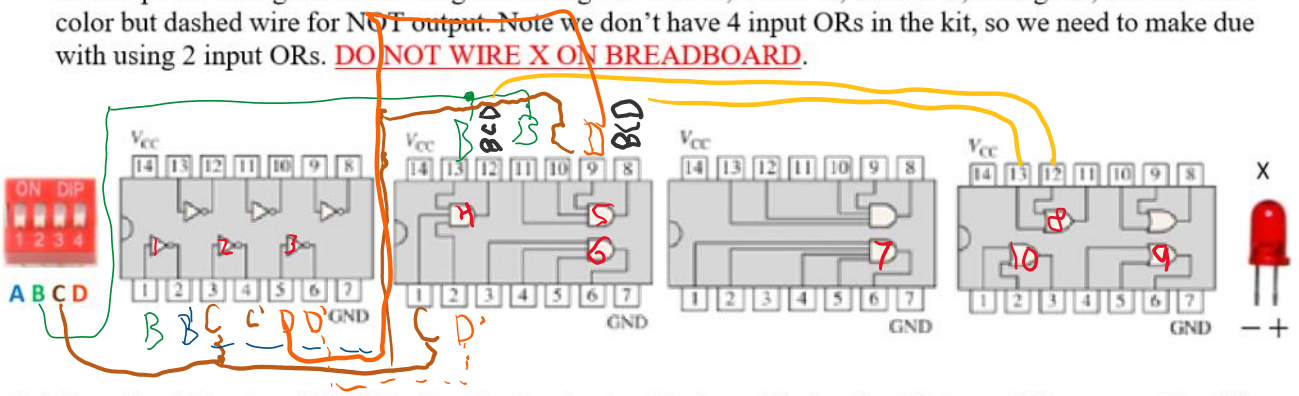
The 7400 Series Family of Integrated Circuits (ICs)



1.4 Plan the wiring: Gates are packaged in ICs. Determine which and how many ICs from the 7400 Series family at right you will need to implement the circuit as you specified in 1.3 (Note there are no 4 input ORs in your kit so use 2-input OR ICs instead:

Quantity needed?	7400 Series IC #
3	

Plan out the layout by numbering the gates used with the same number in your 1.2 plan. Labeling inputs and outputs of the gates or drawing the wiring use blue-A, Green-B, Brown-C, Orange-D, use the same color but dashed wire for NOT output. Note we don't have 4 input ORs in the kit, so we need to make due with using 2 input ORs. DO NOT WIRE X ON BREADBOARD.



1.6 Can circuit be simplified? Look at the handout on Boolean Algebra Postulates and Theorems. Identify by either writing the name or the equation of the postulate(s) or theorem(s) used to simplify.

$$X = B\,C\,\overline{D} + B\,C\,D + A\,\overline{B}\,\overline{D} + A\,B\,\overline{C}\,\overline{D}$$

Distributive

$$= B\,C\,(\overline{D} + D) + (\overline{B} + B\,\overline{C})\,A\,\overline{D}$$

Absorption

$$= B\,C\,(1) + (\overline{B} + \overline{C})\,A\,\overline{D} = B\,C + A\,\overline{B}\,\overline{D} + A\,\overline{C}\,\overline{D}$$

Factor

Additive compl.

Identity

Or

Demorgans

$$= BC + \overline{(BC)}\,A\,\overline{D} = B\,C + A\,\overline{D}$$

Distributive

absorbstion

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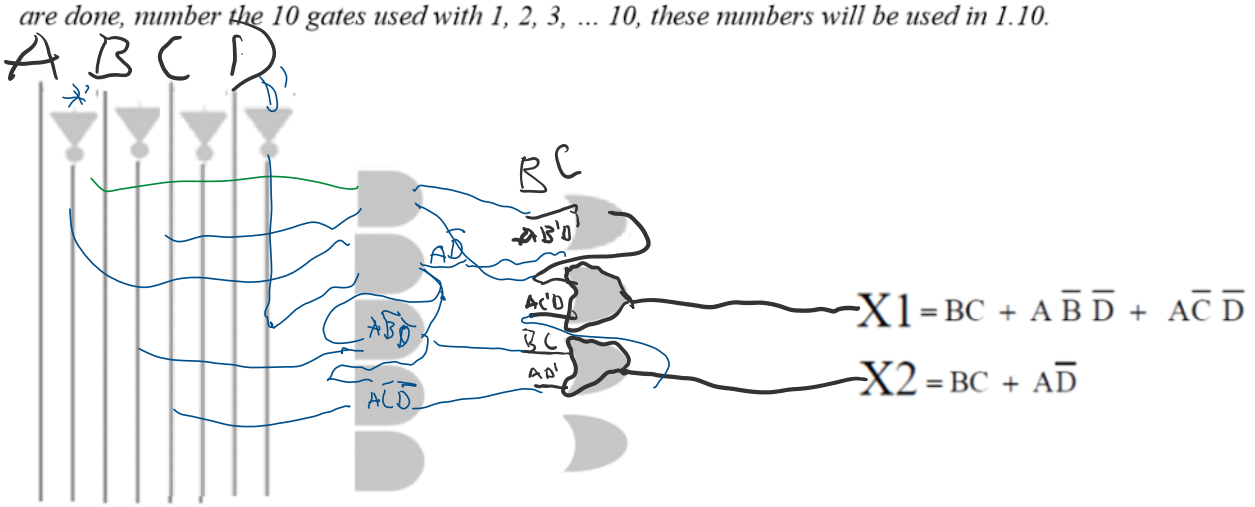
As you verified in 1.a.6, the following Boolean function algebraically reduced to two different forms denoted below as X1 and X2 as follows.

$$X = B\,C\,\overline{D} + B\,C\,D + A\,\overline{B}\,\overline{D} + A\,B\,\overline{C}\,\overline{D}$$
$$= BC\,(\overline{D} + D) + (\overline{B} + B\overline{C})\,A\overline{D}$$
$$= BC + (\overline{B} + \overline{C})\,A\overline{D} = \underline{BC + A\,\overline{B}\,\overline{D} + A\overline{C}\,\overline{D}} = X1$$
$$\text{or} = BC + \overline{(BC)}\,A\overline{D} = \underline{BC + A\overline{D}} = X2$$

ABCD	BC	AB'D'	AC'D'	AD'	X1	X2
0000	0	0	0	0	0	
0001	0	0	0	0		
0010						
0011						
0100						
0101						
0110	1				1	1
0111	1				1	1
1000	1	1	1	1	1	1
1001	1	1	1	0		
1010	1	1	1	0	1	1
1011	1	1	1	0		
1100	1	0	1	1	1	1
1101						
1110	1				1	1
1111	1				1	1

1.7 Construct the Truth Table: Verify the equivalence of X1 and X2 using the following truth table, note there are only 4 different subterms, 2 are the same, so list them only once in Truth Table. Compare it to the Truth Tale for X in 1.1 and verify they outputs are the same.

1.8 Plan the circuit with constraints: Design the circuit <u>in pencil</u> for the above two reduced functions, X1 and X2. However, there are constraints that you must abide by. <u>Constraints:</u> use exactly 3 NOT gates, 4 2-input AND gates, 3 2-input OR gates. *Note: Look for things both equations have in common. After you are done, number the 10 gates used with 1, 2, 3, … 10, these numbers will be used in 1.10.*



1.9 Simulate: Verify the circuit design/behavior by simulating the circuit using Quartus before you actually build the circuit on the breadboard. Open the Quartus project you build in 1.3 and add the X1 and X2 circuits to the X circuit Block Diagram / Schematic by drawing them below the circuit for X. Save. Compile. Debug if needed. Generate the Vector Waveform file adding the X1 and X2 outputs so it will display X, X1 and X2. Simulate. Check if all their waveforms are equivalent, X = X1 = X2. Save. Take a picture of the new .bdf and .vwf files making sure to include the file name that is in the window in the picture or snip to include in the portfolio. The TA may ask you for these pictures at grading. If they do not, don't worry, I will add the Quartus points when I grade your portfolio.

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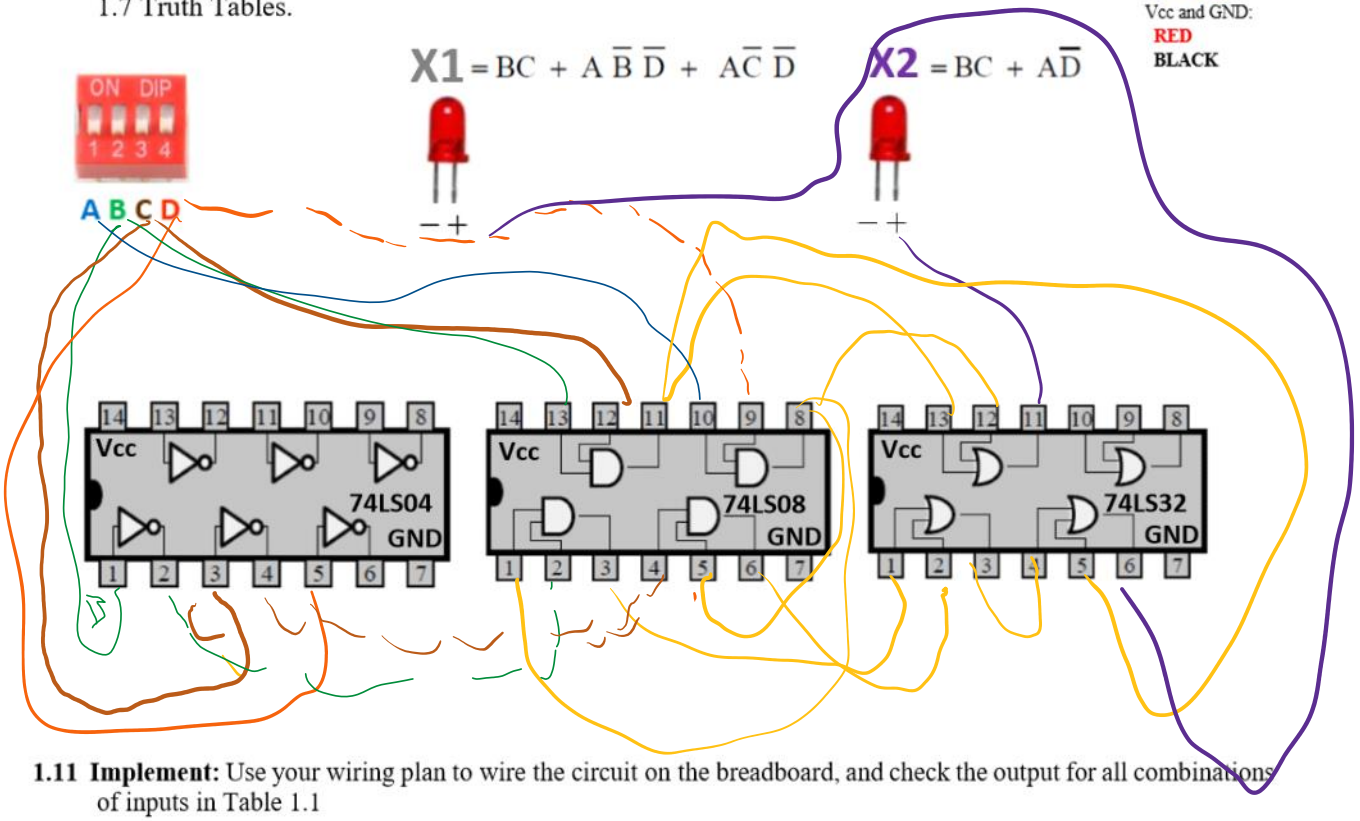
1.10. Plan your wiring of just X1 and X2: Use the following chip pin-out to conveniently plan your wiring X1 and X2 (not X, you do not wire X) on your breadboard with **constraint:** using exactly 1/2 7404 (3 NOT gates in the 74LS04), 1 7408 (4 AND gates in the 74LS08), and 3/4 7432 (3 OR gates in the 74LS32) chips on your breadboard. Number the gates used with the corresponding number of the gates in 1.8. Connect inputs ABCD to 4 DIP switches using the colors designated. Use white wire to connect the ANDs and ORs to output X1. Use yellow to connect the ANDs and ORs to output X2. This is done to make tracing and debugging easier. Test all the 16 different input combinations and observe the two outputs to be equivalent and matching the 1.1 and 1.7 Truth Tables.

Suggested color code
Inputs:
BLUE
GREEN
BROWN
ORANGE
In-Between:
WHITE
YELLOW
Outputs:
GREY
PURPLE
Vcc and GND:
RED
BLACK



1.11 Implement: Use your wiring plan to wire the circuit on the breadboard, and check the output for all combinations of inputs in Table 1.1

1.12 Deploy: If you received extra parts in your kit to connect your circuit to your computer via USB. Follow the directions provided in the extra kit, go to the link provided, and create an account with your fau.edu email, select LACCEI Gallery, select FAU, select Logic Design, select Lab 0. It will guide you through a series of steps to test the circuit for each input, if you succeed, then you will see on your computer, a guard and someone or something asking entrance to the security door, you will control with your circuit if the guard lets them in or not. You will now remove the wires to your input switches and press Submit on the screen. You will see if your circuit functions in the real world

1.13 Get it graded: Take a picture of the breadboard with your name showing, together with your ID and the ID of the TA grades it to submit as part of Lab 1 portfolio. After it is graded, you will be asked to pull the wires from your lab circuit. Do NOT pull the test platform wires just the ones in the upper breadboard. Leave the three ICs plugged into your board with power and ground connected. **KEEP THE WIRES TO REUSE FOR NEXT LAB.**

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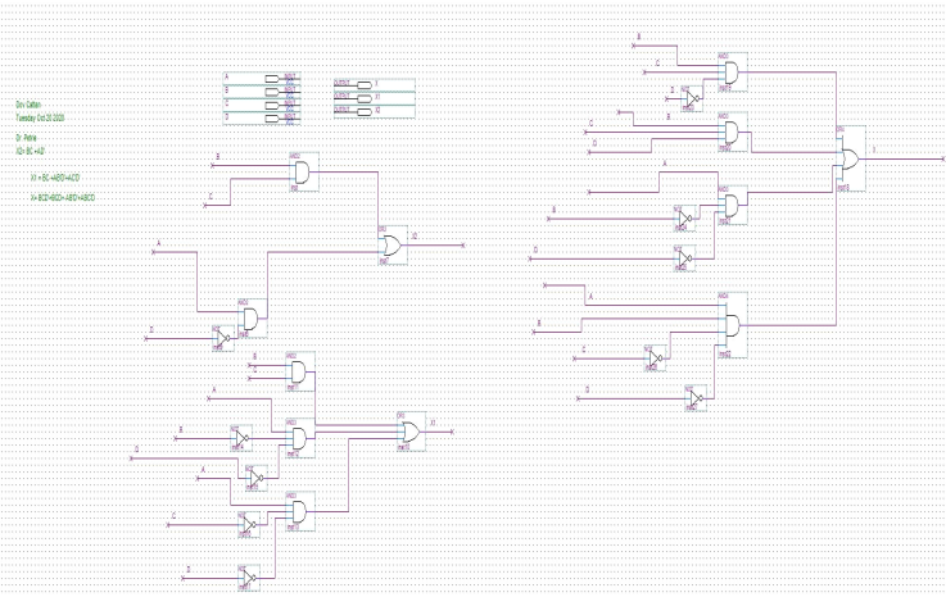
1.14 Reflect on Impact: Examine the equations the engineer gave you for programming the lock mechanism, is it correct or can you think of a better equation? Why go through the trouble of simplifying a switching function? Engineering design projects can have very serious impacts. Consider the following areas, circle the ones your circuit could potentially impact. For the ones you circled, briefly discuss the impact you considered:

- **Public Health:**
- **Safety:**
- **Global:**
- **Cultural:**
- **Social:**
- **Environmental:**
- **Economic:**



1.15 Submit your portfolio to Canvas: To get all your lab points, you need to get your lab graded by the Teaching Assistant (TA), and submit under Canvas > Assignment > Lab 1 a **portfolio** (report) consisting of one pdf file that includes:

- Header: Cover page or header with your name, my name, number, Logic Design class and class section
- Handwork: copy of planning work you did by hand (take picture of this worksheet or annotate this pdf electronically)
- Simulation: a copy of the work you did in Altera Quartus
  - Schematic do all 3 circuits in one schematic window, must include comment with your name and Z#, the file name must include your name as part of the file name so it appears on the schematic screen window. You can take a picture of the screen or use Snipping Tool under Start menu to capture the pertinent part of the screen containing the Block Diagram window with the file name containing your name.
  - Vector Waveform simulation (simulated timing diagram) a picture or screen shot that include output for all 3 circuits in the Vector Waveform window with the file name containing your name.
- Wiring: a picture of your breadboard with the wired circuit and your FAU OWL Card (if you got it graded in the lab also include with TA OWL card and make sure the name and Z# written on your board are showing).
- Link to Video demo required only for online students who cannot come to campus to get labs graded by TA in EE-203. Enter this video link also under Lab 1 Online Grading assignment.