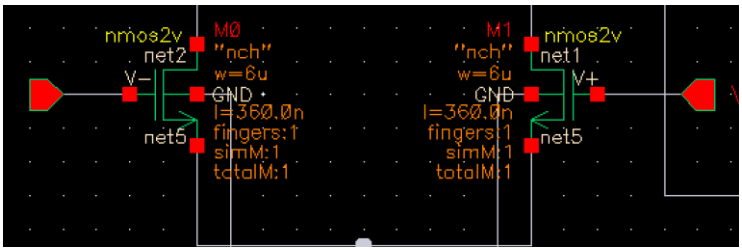
Low Dropout Regulator

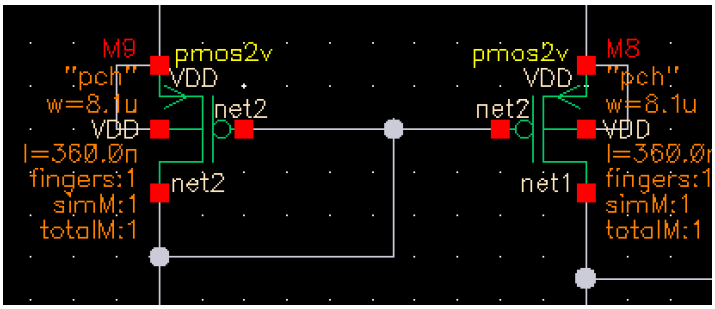
Design Specifications

1. OpAmp Specifications
    a. Input Common Mode range:- 1.23 V
    b. Two stage Amplifier
    c. Open Loop Gain – 60dB
    d. Unity Gain Bandwidth – 75MHz
    e. Load Capacitor = 5pF
    f. ICMR+ = 1.53
    g. ICMR- = 0.93
2. OpAmp Transistor specifications.
    a. Differential Pair



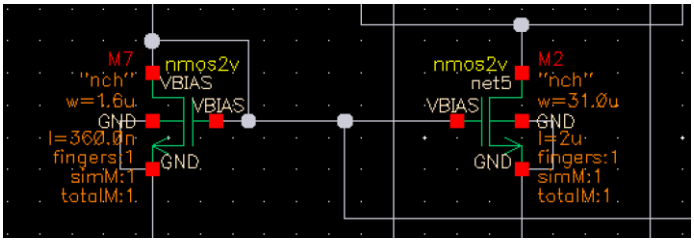
M0 = 6u/360n
M1 = 6u/360n

    b. PMOS Current Mirror



M9 = 8.1u/360n
M8 = 8.1u/360n

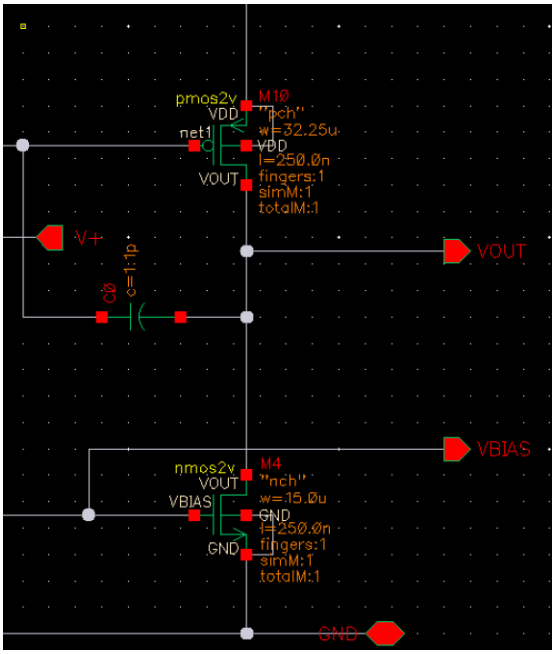
c. NMOS Current Mirror



M7 = 4.44u/1u

M2 = 15.5u/1u

d. Second Stage + Capacitance

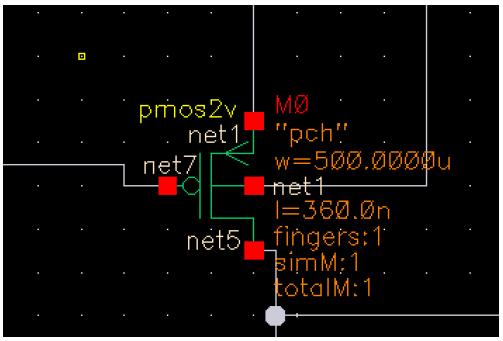


M10 = 32.35u/250n

M4 = 15u/250n

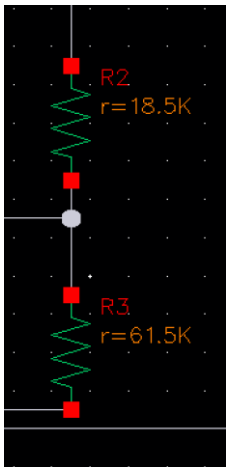
C_c = 1.1p

3. LDO Pass Transistor



M0 = 500u/560n

4. Resistor

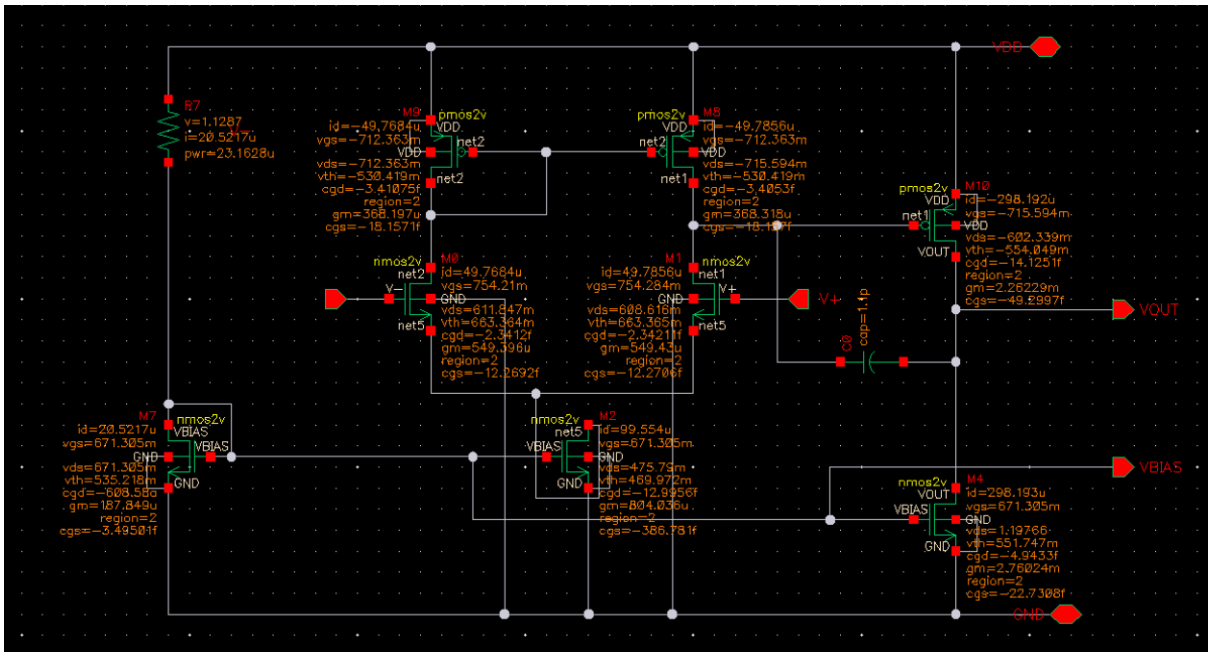


R1 = 18.5kOhm

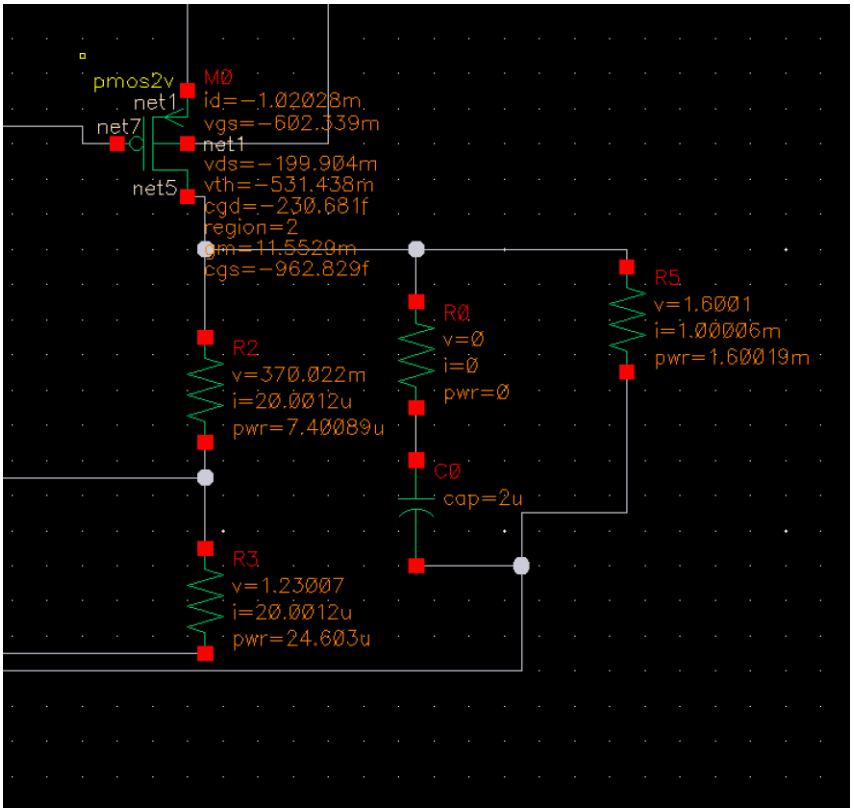
R2 = 61.5kOhm

Simulations.

1. DC analysis of the different transistors.

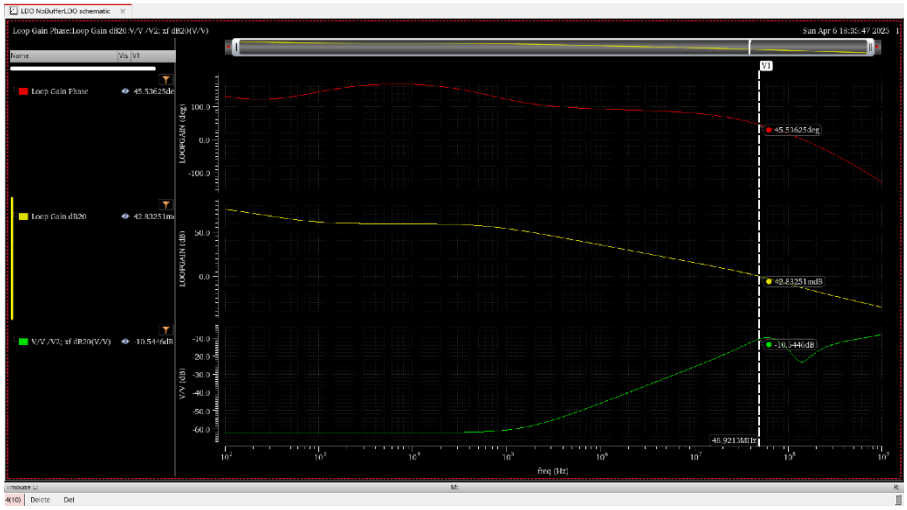


Transistor and overdrive voltages of different transistors in OpAmp



Output Voltage and current through Pass Transistors

2. Stability Analysis



The Loop is stable with a Phase Margin of 45 degrees and gain of 75dB.

PSRR of the Loop is 61dB for a 3dB bandwidth of 100kHz

Load Capacitor = 2uF and the ESR = 100Ohm

Load current = 1mA

Design Procedure:

a. Design of the OpAmp:
   First We started with the Differential Pair Transistors. We decided a current of 100uA to flow through the two transistors together. This makes 50uA flow through each individual transistor. The input common mode voltage was 1.23V.

   We started with the Bandwidth required for the OpAmp. This requires gm of the NMOS differential pair to be 0.64mS for a bandwidth of 100MHz.

   We needed to run a load of 5pF , so the Cc was chosen to be 1.1pF .

   Now using the gm Value we sized the differential Pair. When we calculated the overdrive for this transistor it turned out to be 77mV. And we got a gm of 0.58mS.

   Now using ICMR- of the OpAmp we designed the current Mirror current which has to flow 100uA of current. The W/L of this transistor was obtained this way.

   Then we come to the design of the PMOS current mirror of 1st stage. Using the ICMR+ we found out the Vgs of the PMOS transistor and we know the current passing through each of them is 50uA. Using this we calculated the W/L of thie two PMOS current mirro transistors.

   Now coming the the second stage. We need the determine the size of the PMOS of the inverter amplifier. We first calculated the gm of this transistor from the UGB specifications of the OpAmp. Now considering this UGB, we assumed an overdrive of 150mV and calculated the W/L of these transistor. Now we calculated the current passing through this transistor and this turned out to be around 310uA.

   Now using this current we designed the W/L of the NMOS current mirror in inverter amplifier. We knew the overdrive of the NMOS transistor as it is set from the NMOS current mirror structure. Now we adjust the ratio of these two transistors in such a way that 310uA of current flows into this.

b. Design of the Pass Transistor.
   Now we decided the amount current that has to be flown into the pass transistor to be 1mA. And the external capacitance = 5pF. But because of large capacitor and unwanted feedback poles, the output capacitance was increased from 5pF to 2uF.

Now we have to decide on the voltage dropout. We decided on the voltage dropout to be 200mV. So we decided the overdrive of the PMOS transistor to be 100mV. Assuming 100mV, we sized the transistor of the PMOS current source.

Now when we checked the stability criteria, there were two poles and the phase margin was -20degrees. So we tried identifying the pole location and cancelled the pole by adding a zero with the help of ESR of capacitor. And ESR of 100Ohms was chosen which yielded a good result of 45 degrees of Phase Margin.

Now we tried checking the load regulation of the LDO. And we found that a resistor of 3kOhms gives the best phase margin and the worst phase margin was obtained when a resistor of 500Ohms was connected to the output of the LDO. The variation in phase margin was from 60 degrees to 40 degrees.