

Yanling Zhi

A Software Engineer and Researcher

5F, Building A, 391 Wen'er Road
Hangzhou, Zhejiang, China

✉ i@dr-zhi.com

🌐 www.dr-zhi.com

🎧 Dr-Zhi

📌 DrYanlingZhi



*Some birds aren't meant to be caged. Their feathers are just too bright.
—"The Shawshank Redemption"*

Education

- Sep. 2007 – **Ph.D.**, *State-Key Lab. of ASIC & System, Fudan University*, Shanghai, GPA 3.78/4.
June 2012
 - Thesis: Efficient Algorithms for Critical Problems in Clock Skew Scheduling;
 - Supervisors: Prof. Hai Zhou (Northwestern University) and Wai-Shing Luk (Fudan University).
- Sep. 2003 – **B.E.**, *Electrical Engineering, Wuhan University*, Wuhan, GPA 3.63/4.
June 2007
 - Graduated with Rank 1st out of 77, and thereafter joined State-Key Lab. of ASIC & System with recommendation.

Experience

Vocational

- July 2012 – **Senior Software Engineer**, *MicroStrategy*, Hangzhou.
Present
 - Worked on MicroStrategy Mobile for iPad/iPhone (<http://www.microstrategy.com/mobile>).
 - Participated in the entire lifecycle of new feature development.
 - Focused on building prototypes, integrating with the product, testing and fixing issues.
 - Effectively communicated and collaborated with managers, architects and cross-team engineers in both China and US.
 - Featured work includes navigation document (tab bar), panel caching, resetting to first panel, etc.
 - Grew to be a mature programmer on Objective-C/iOS in three months (from a green hand).
- Jan 2011 – **R&D Engineer Intern (Part-time)**, *Verigy*, Shanghai.
Dec. 2011
 - Worked on algorithms design for Memory Redundancy Repair product
 - Formally formulate the memory redundancy repair problem, and proposed new algorithms based on perfect matching in bipartite graphs;
 - Implemented a prototype to validate the efficiency of the algorithms;
 - Worked closely with engineers in both China and Germany.
- Aug. 2009 – **R&D Engineer Intern**, *Verigy*, Shanghai.
May 2010
 - Worked on parallel computing for the product MTL.
 - Designed multithreading algorithms and implemented prototypes based on C++ Library Threading Building Blocks;
 - Remarkable speedup was achieved on industrial benchmarks;
 - The work was integrated into the products of next generation;
 - Won the 2010 Brilliance of Innovation Honorable Mention award in Verigy.

Academic

Dec. 2009 – **Researched on clock skew optimization algorithms.**

- Mar. 2012
- Proposed novel efficient algorithms based on network flow algorithms for multi-domain clock skew scheduling and yield-driven clock skew scheduling;
 - Programmed extensively using C/C++ in building prototypes to validate the efficiency of algorithms;
 - Acquired solid skills in **algorithms research and development**, and paper writing;
 - Publications as first author on world-class conferences/journals in Electronic Design Automation field (<http://scholar.google.com/citations?user=w-DiTg4AAAAAJ>):
 1. **Yanling Zhi**, Wai-Shing Luk, Hai Zhou and Xuan Zeng, Smipref: An efficient method for multi-domain clock skew scheduling. *Integration, the VLSI Journal*, 2012.
 2. **Yanling Zhi**, Wai-Shing, Luk, Yi Wang, Changhao Yan and Xuan Zeng, Yield-driven clock skew scheduling for arbitrary distributions of critical path delays. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, 95(12):2172–2181, 2012.
 3. **Yanling Zhi**, Wai-Shing Luk, Hai Zhou, Changhao Yan, Hengliang Zhu and Xuan Zeng, An efficient algorithm for multi-domain clock skew scheduling. In *IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE) 2011*, pages 1–6, France, 2011.
 4. **Yanling Zhi**, Hai Zhou and Xuan Zeng. A practical method for multi-domain clock skew optimization. In *16th IEEE Asia and South Pacific Design Automation Conference (ASP-DAC)*, pages 521–526. Japan, 2011.

July 2008 – **Researched on formal verification algorithms.**

- Nov. 2009
- Worked on sequential equivalence checking problems;
 - Proposed a new algorithm based on bounded model checking using covering relations among signals in sequential circuits;
 - Built prototypes to verify the efficiency of the algorithm.

Sep. 2007 – **Developed PhysicalCMP simulation tools.**

- July 2008
- Worked as one of the core programers in the entire development process;
 - Designed and implemented graphical user interface (using Qt Library) and chip layout information extraction algorithms in C++;
 - The work was later integrated into National Major Science & Technology Project in the Eleventh Five-Year period;

Professional Skills

- Proficient in C/C++ programming (5+ years experience);
- Experienced in object-oriented programming, parallel computing on multithreading platforms;
- Experienced in Objective-C, iOS programming (0.8 year experience);
- Skilled in algorithms design;
- Familiar with Matlab programming and shell;
- Interested in design patterns.

Languages

English Fluent in both spoken and written English. CET-6: 93/100, TOEFL: 617/677.

Chinese Native.

Awards and Honors

- 2011 Won the Intel Fellowship Winner award.
- 2010 Won the Brilliance of Innovation Honorable Mention award in Verigy.
- 2008-2010 Won Academic Scholarship in Fudan University every year.
- 2007 Joined State-Key Lab. of ASIC & System without taking post-graduate entrance examination, and also won the Entrance Scholarship in Fudan University.
- 2003-2007 Won first class People Scholarship and "Merit Student" title in Wuhan University every year; won LG Electronics Scholarship in 2005.

Community and Contacts

Home page: <http://Dr-Zhi.com> (personal blog)
GitHub: <https://github.com/Dr-Zhi>
LinkedIn: <http://www.linkedin.com/in/DrYanlingZhi>
Email: i@dr-zhi.com

Self Evaluation

A software developer and researcher, who is always willing and eager to learn new technologies, and strives for perfection in working naturally.