CMPS 3240 **Name (Print):** _____
Fall 2017
Midterm II
11/7/2017
Time Limit: 150 minutes Instructor A. Cruz

This exam contains 6 pages (including this cover page) and 7 problems. Check to see if any pages are missing. Enter all requested information on the top of this page, and put your initials on the top of every page, in case the pages become separated.

You may *not* use your books, notes, or any computer/cell phone/tablet/etc. on this exam.

You are required to show your work on each problem on this exam (except multiple choice). The following rules apply:

- **You are allowed to have one cheat sheet**. You may write on both sides. The paper must be 8.5x11 inches. You must turn in your cheat sheet at the end of the test. It must have your name on it.
- **An ID is required**. You will not be able to turn in the test unless you show a photo ID.
- **Mysterious or unsupported answers will not receive full credit**. A correct answer, unsupported by calculations, explanation, or algebraic work will receive no credit; an incorrect answer supported by substantially correct calculations and explanations might still receive partial credit.
- If you need more space, use the back of the pages; clearly indicate when you have done this.

Do not write in the table to the right.

Problem	Points	Score
1	10	
2	9	
3	15	
4	15	
5	10	
6	10	
7	10	
Total:	79	

Please circle your major (if applicable). This is for ABET accreditation purposes only and will not affect your grade in any way.

1. Computer Engineering
2. Computer Science
3. Computer Information Systems
4. Information Security
5. Electrical Engineering

1. (10 points) The following questions are fill in the blank.
   1. In MIPS, on _____, the program counter is set to 0x80000180.
   2. A _____ hazard happens when two processes use the same component at the same time.
   3. In MIPS, the EPC register contains the _____.
   4. The _____ is a segment of instruction memory that handles an exception.
   5. A _____ hazard happens when IF does not know what instruction to fetch because of branching.
   6. The _____ stage detects if an overflow or underflow occurs.
   7. Long length wires in a bus must be _____.
   8. If ID fetches the register value in the _____ half of the ID cycle, it can peek at a value that is not yet written back.
   9. A _____ hazard happens when ID needs a value that has not yet been written back.
   10. If a MIPS instruction has the register _____ as a target, nothing will happen.
2. The following question pertains to latches and flip-flops.
   (a) (2 points) Give the design of an SR latch.

   (b) (4 points) Complete the truth table for an SR latch.

S	R	Q	Not Q
0	0		
0	1		
1	0		
1	1		

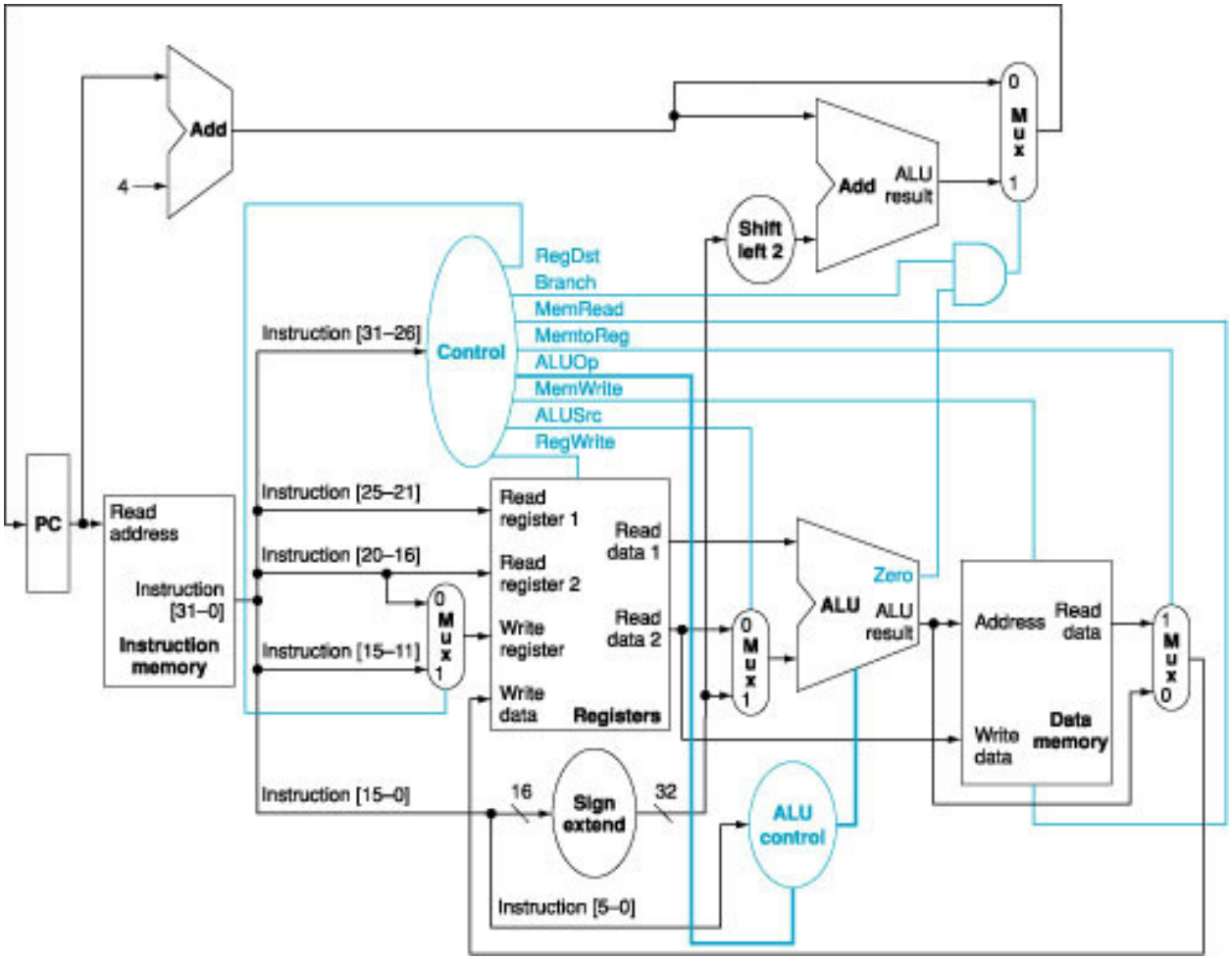
   (c) (3 points) Give the design of a D flip-flop that is triggered on the falling edge.

3. (15 points) Consider a simple, single datapath for a MIPS microprocessor. Give values for the following lines. Show your work if necessary.

```
add $t0, $v0, $t1
```

Give the numeric value for the following lines (not English). Indicate N/A if it is not applicable for this instruction.

Line	Value	Line	Value
RegDst		Rs	
Branch		Rt	
MemRead		Rd	
MemtoReg		Opcode	
ALUOp		Func	
ALU Control		Shamt	
MemWrite		Branch	
ALUSrc		Immidiate	



4. (15 points) Repeat the previous question for the following instruction:

```
lw $t3, 0($s2)
```

Give the numeric value for the following lines (not English). Indicate N/A if it is not applicable for this instruction.

Line	Value	Line	Value
RegDst		Rs	
Branch		Rt	
MemRead		Rd	
MemtoReg		Opcode	
ALUOp		Func	
ALU Control		Shamt	
MemWrite		Branch	
ALUSrc		Immidiate	

5. Consider a pipelined MIPS architecture that does not use any forwarding, and given the following code.

```
add $t1, $t2, $t3
lw $t4, 0($t5)
add $t2, $t3, $t4
add $t6, $t1, $t2
```

(a) (6 points) Assuming that there is no forwarding, give a timeline from start to wind-down for the code.

(b) (2 points) If forwarding is enabled, how would this change the timeline?

(c) (2 points) As a follow up to the previous question, we happen to know that the delay following a load instruction cannot be totally removed with forwarding. Why is this the case?

6. Refer to the pipeline given in Question 3. Given the following instruction:

```
00100100010001111111111111111111111111111111111111
```

Register	0	1	2	3	4	5	6	7	8	9
Value	12	10	21	2	3	1	100	8	12	13

(a) (2 points) What type of instruction is this, and what instruction is this?

(b) (2 points) What is the value after the "sign extend" resource?

(c) (2 points) Is there an exception? If so, what type of exception has occurred?

(d) (4 points) What are all values of inputs for the register file (if applicable)?

7. Refer to the pipeline given in Question 3. Given the following instruction:

   `10001100101000010000000000000000`

   Use the register values from the previous page.

   (a) (2 points) What type of instruction is thiss, and what instruction is this?

   (b) (2 points) What is the value of ALU result?

   (c) (2 points) Is there an exception? If so, what type of exception has occurred?

   (d) (4 points) What are all values of inputs for the register file (if applicable)?