

Full Can Clock Oscillator (1 – 20MHz) optional.  
Do not connect the output of both oscillators at the same time!

The frequency of the clock is given by:  
 $f = 0.8 / (RC)$   
E.g.  $R = 68k\Omega$  and  $C = 22\mu F$ ,  $f = 1.5Hz$

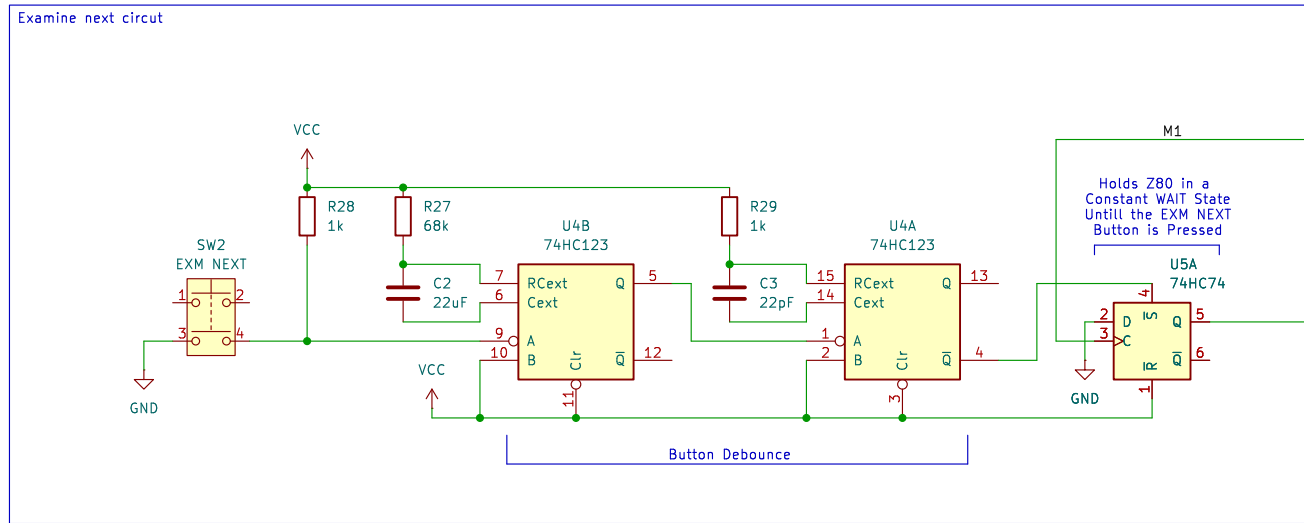
Notes:

The Z80 and 62256 SRAM would be a lot happier if you used a 74HC245 (or an actual LED driver) to buffer the address bus and data bus.

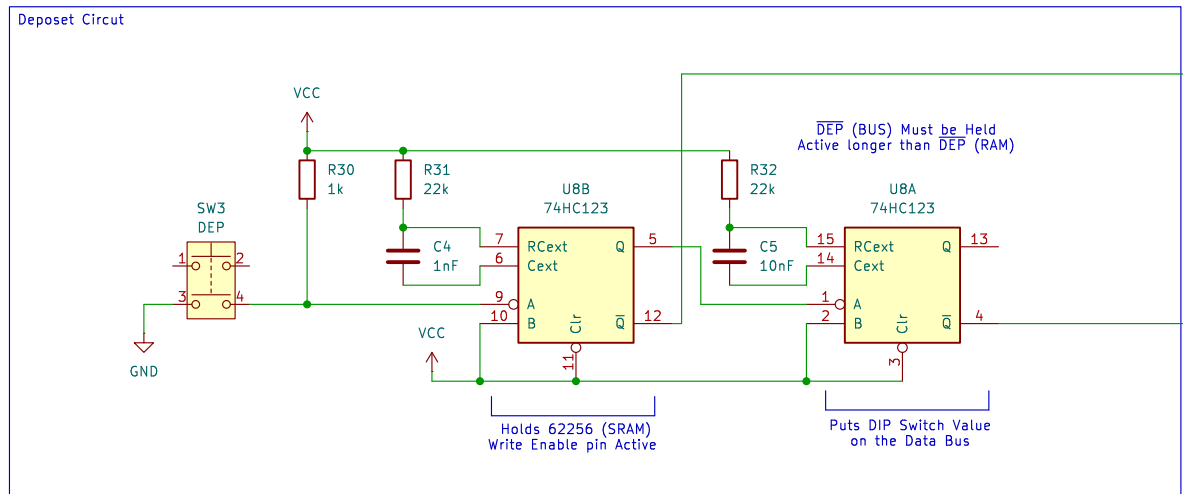
Decoupling capacitors (~0.1uF) on the power rails probably wouldn't be a bad idea.

There will be a few us of bus contention at the begining of the deposit operation. See Write cycle (2) in HM62256B Series datasheet for details. This could be cured by using another monostable multivibrator to give a delay between the DEP (RAM) and -(DEP (BUS) signals. But this is just a play computer so I'm just ignore it :p

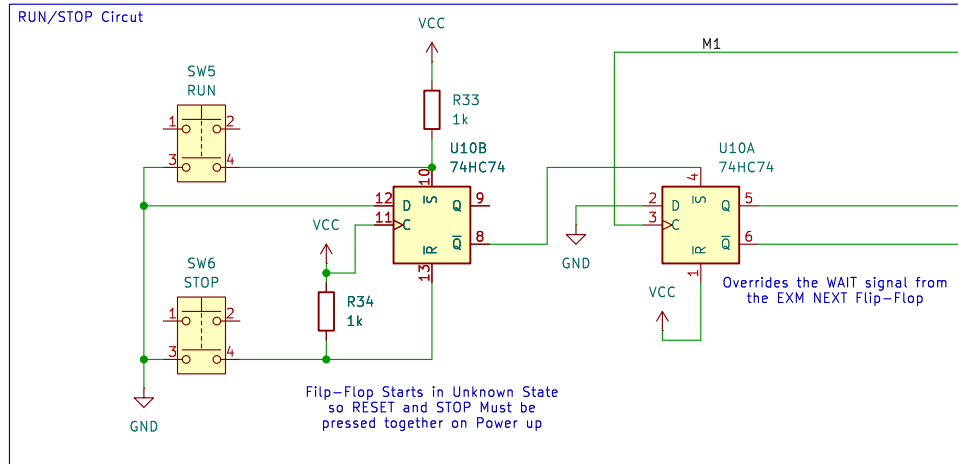
Examine next circuit



Deposet Circuit



RUN/STOP Circuit



Data Bus Pull Down Resistors

