

- Low Supply Voltage Range, 1.8 V to 3.6 V
- Ultra-Low Power Consumption:
 - Active Mode: 365 μ A at 1 MHz, 2.2 V
 - Standby Mode (VLO): 0.5 μ A
 - Off Mode (RAM Retention): 0.1 μ A
- Wake-Up From Standby Mode in Less Than 1 μ s
- 16-Bit RISC Architecture, 62.5-ns Instruction Cycle Time
- Three-Channel Internal DMA
- 12-Bit Analog-to-Digital (A/D) Converter With Internal Reference, Sample-and-Hold, and Autoscan Feature
- Dual 12-Bit Digital-to-Analog (D/A) Converters With Synchronization
- 16-Bit Timer_A With Three Capture/Compare Registers
- 16-Bit Timer_B With Seven Capture/Compare-With-Shadow Registers
- On-Chip Comparator
- Four Universal Serial Communication Interfaces (USCI)
 - USCI_A0 and USCI_A1
 - Enhanced UART Supporting Auto-Baudrate Detection
 - IrDA Encoder and Decoder
 - Synchronous SPI
 - USCI_B0 and USCI_B1
 - I²C™
 - Synchronous SPI
- Supply Voltage Supervisor/Monitor With Programmable Level Detection
- Brownout Detector
- Bootstrap Loader
- Serial Onboard Programming, No External Programming Voltage Needed Programmable Code Protection by Security Fuse
- Family Members[†] Include:
 - MSP430F2416 92KB+256B Flash Memory, 4KB RAM
 - MSP430F2417 92KB+256B Flash Memory, 8KB RAM
 - MSP430F2418 116KB+256B Flash Memory, 8KB RAM
 - MSP430F2419 120KB+256B Flash Memory, 4KB RAM
 - MSP430F2616 92KB+256B Flash Memory, 4KB RAM
 - MSP430F2617 92KB+256B Flash Memory, 8KB RAM
 - MSP430F2618 116KB+256B Flash Memory, 8KB RAM
 - MSP430F2619 120KB+256B Flash Memory, 4KB RAM
- Available in 80-Pin Quad Flat Pack (QFP), 64-Pin QFP, and 113-Pin Ball Grid Array (BGA) (See Available Options)
- For Complete Module Descriptions, See the *MSP430x2xx Family User's Guide*, Literature Number SLAU144

[†] The MSP430F241x devices are identical to the MSP430F261x devices, with the exception that the DAC12 modules and the DMA controller are not implemented.

description

The Texas Instruments MSP430 family of ultralow-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The calibrated digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1 μ s.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications. These devices have limited built-in ESD protection.



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MSP430F241x, MSP430F261x MIXED SIGNAL MICROCONTROLLER

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description (continued)

The MSP430F261x/241x series are microcontroller configurations with two built-in 16-bit timers, a fast 12-bit A/D converter, a comparator, dual 12-bit D/A converters, four universal serial communication interface (USCI) modules, DMA, and up to 64 I/O pins. The MSP430F241x devices are identical to the MSP430F261x devices, with the exception that the DAC12 and the DMA modules are not implemented.

Typical applications include sensor systems, industrial control applications, hand-held meters, etc.

AVAILABLE OPTIONS

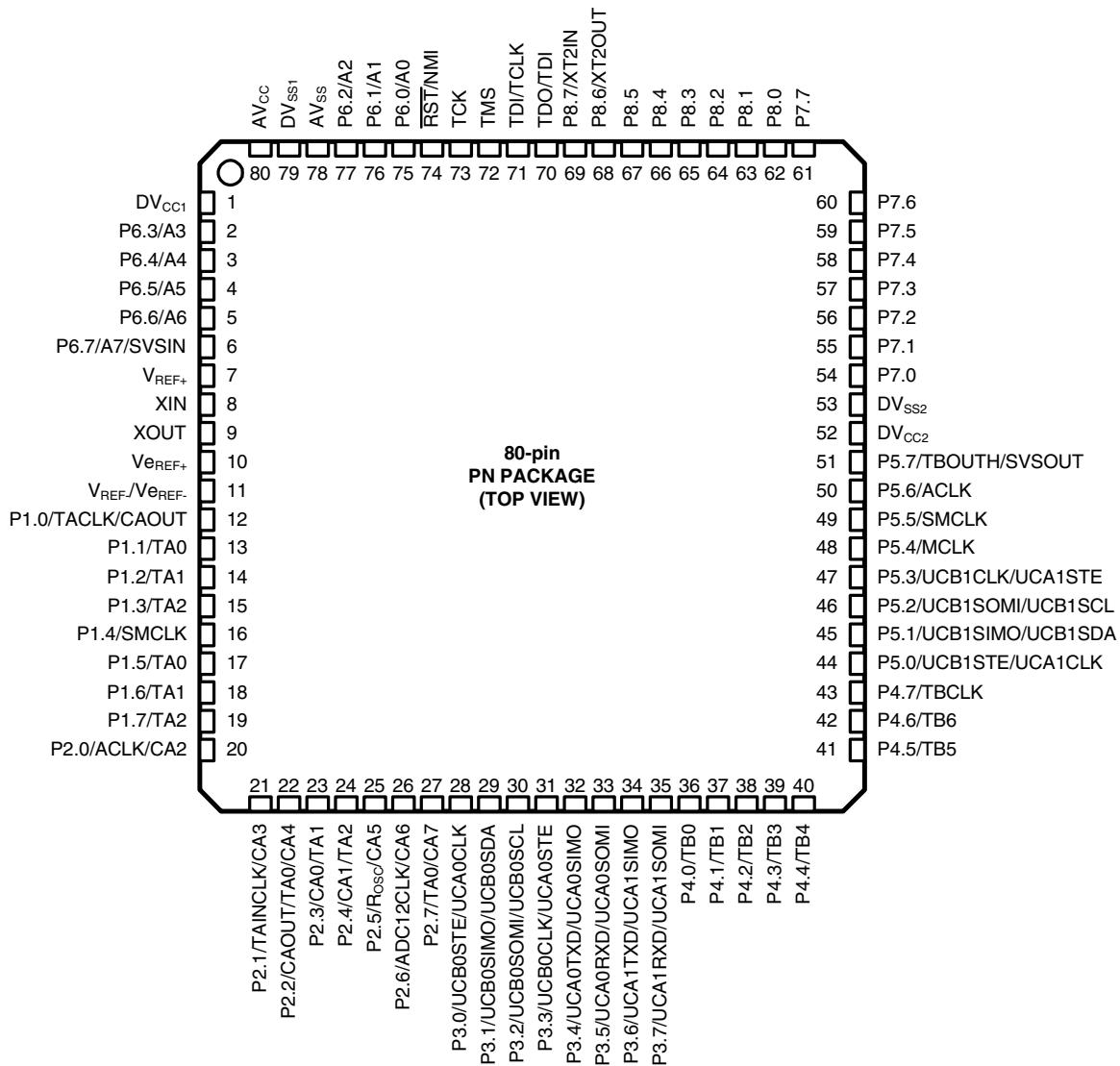
T _A	PACKAGED DEVICES		
	PLASTIC 113-PIN BGA (ZQW)	PLASTIC 80-PIN LQFP (PN)	PLASTIC 64-PIN LQFP (PM)
-40°C to 105°C	MSP430F2416TZQW MSP430F2417TZQW MSP430F2418TZQW MSP430F2419TZQW MSP430F2616TZQW MSP430F2617TZQW MSP430F2618TZQW MSP430F2619TZQW	MSP430F2416TPN MSP430F2417TPN MSP430F2418TPN MSP430F2419TPN MSP430F2616TPN MSP430F2617TPN MSP430F2618TPN MSP430F2619TPN	MSP430F2416TPM MSP430F2417TPM MSP430F2418TPM MSP430F2419TPM MSP430F2616TPM MSP430F2617TPM MSP430F2618TPM MSP430F2619TPM

DEVELOPMENT TOOL SUPPORT

All MSP430 microcontrollers include an Embedded Emulation Module (EEM) allowing advanced debugging and programming through easy-to-use development tools. Recommended hardware options include:

- Debugging and Programming Interface
 - MSP-FET430UIF (USB)
 - MSP-FET430PIF (Parallel Port)
- Debugging and Programming Interface with Target Board
 - MSP-FET430U64
 - MSP-FET430U80
- Standalone Target Board
 - MSP-TS430PM64
- Production Programmer
 - MSP-GANG430

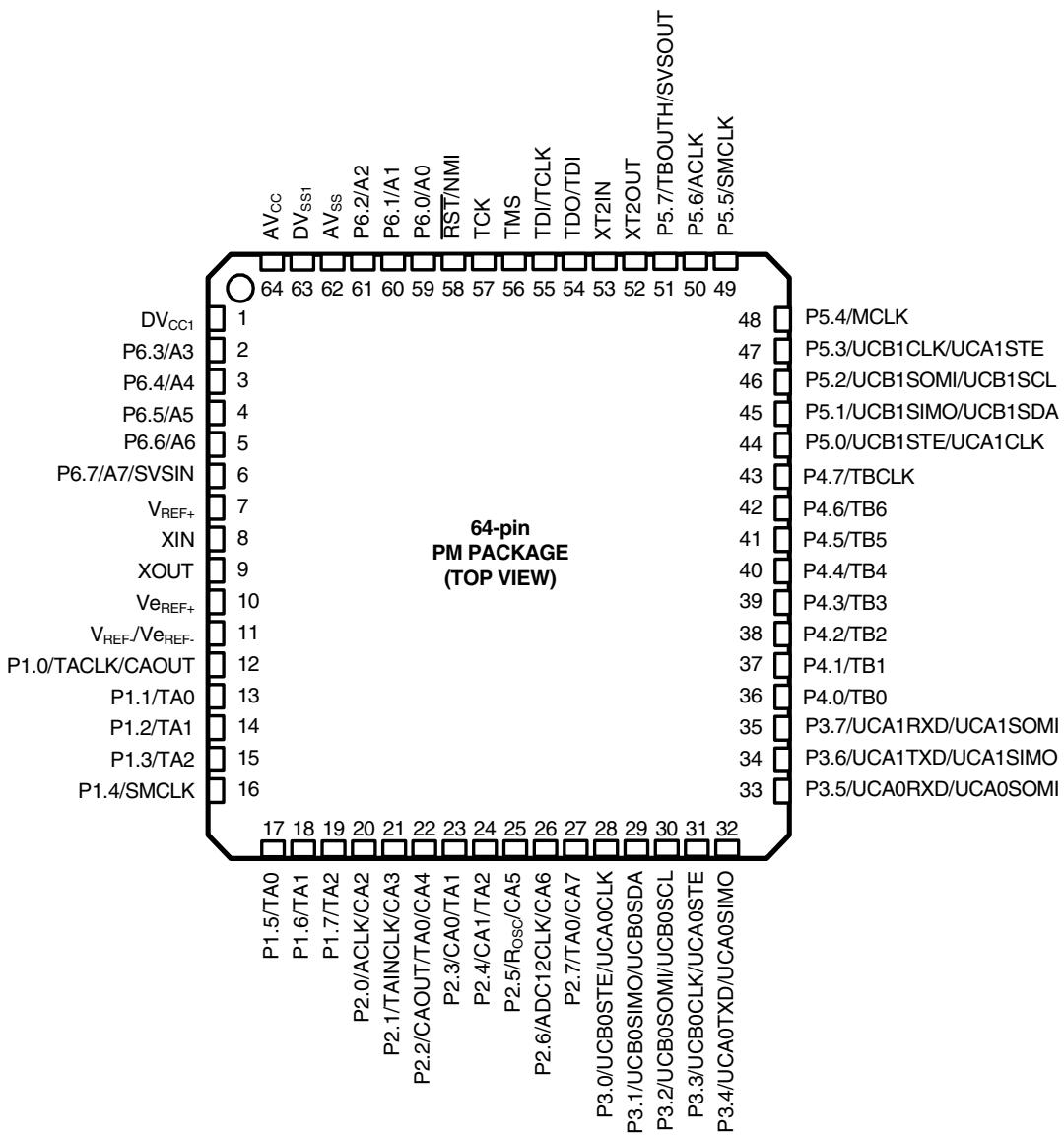
pin designation, MSP430F241x, 80-pin PN package



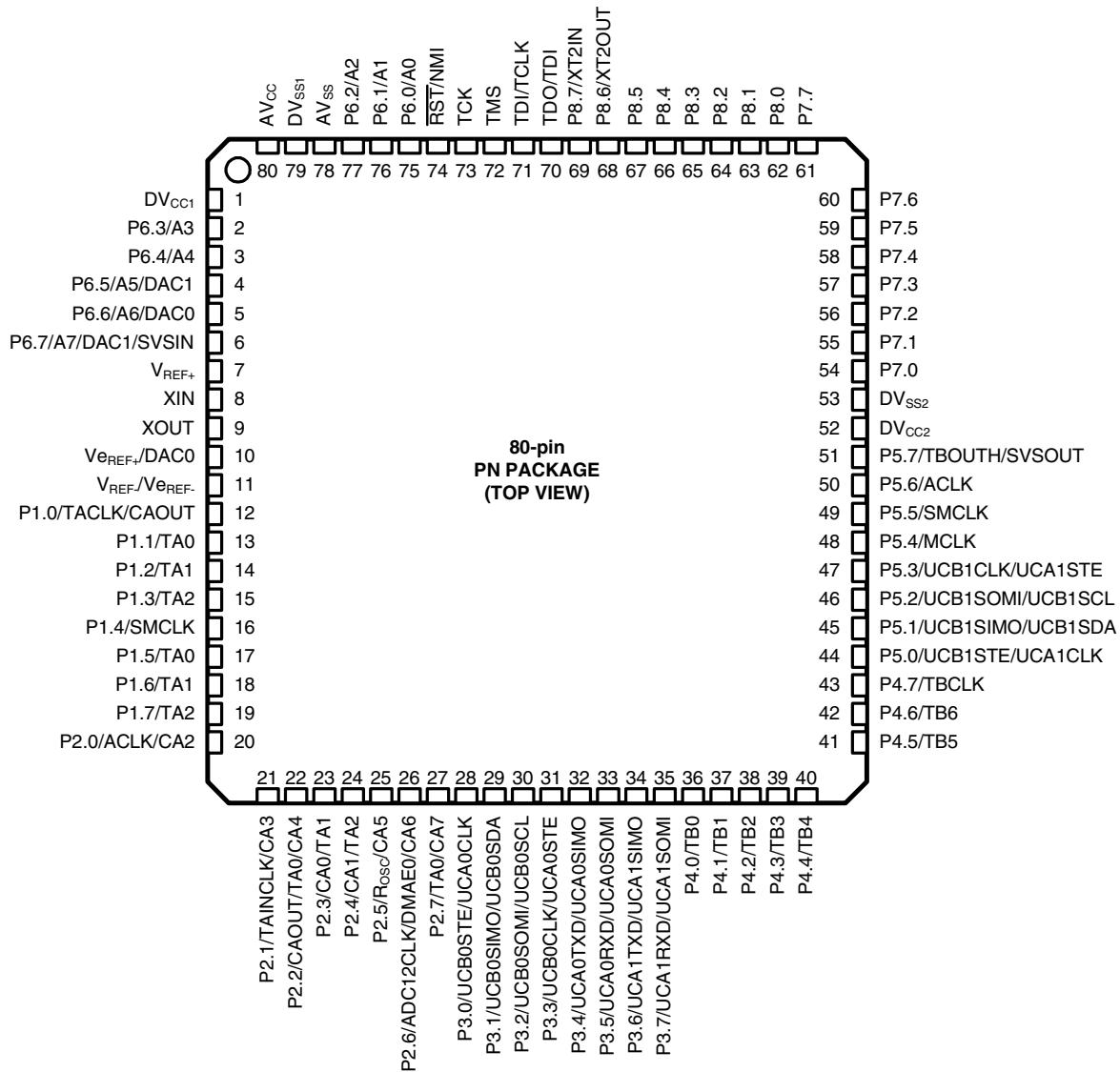
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pin designation, MSP430F241x, 64-pin PM package



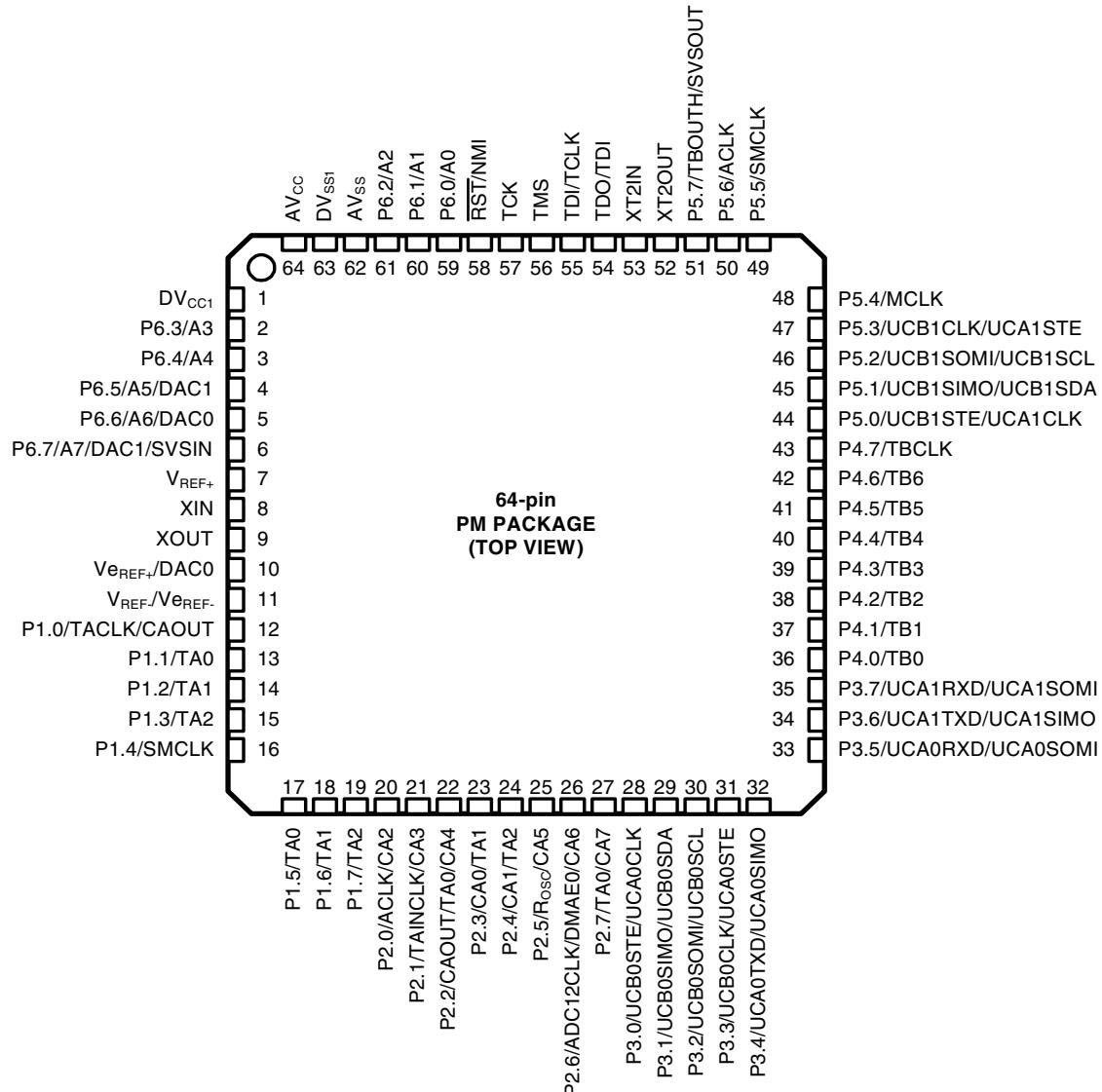
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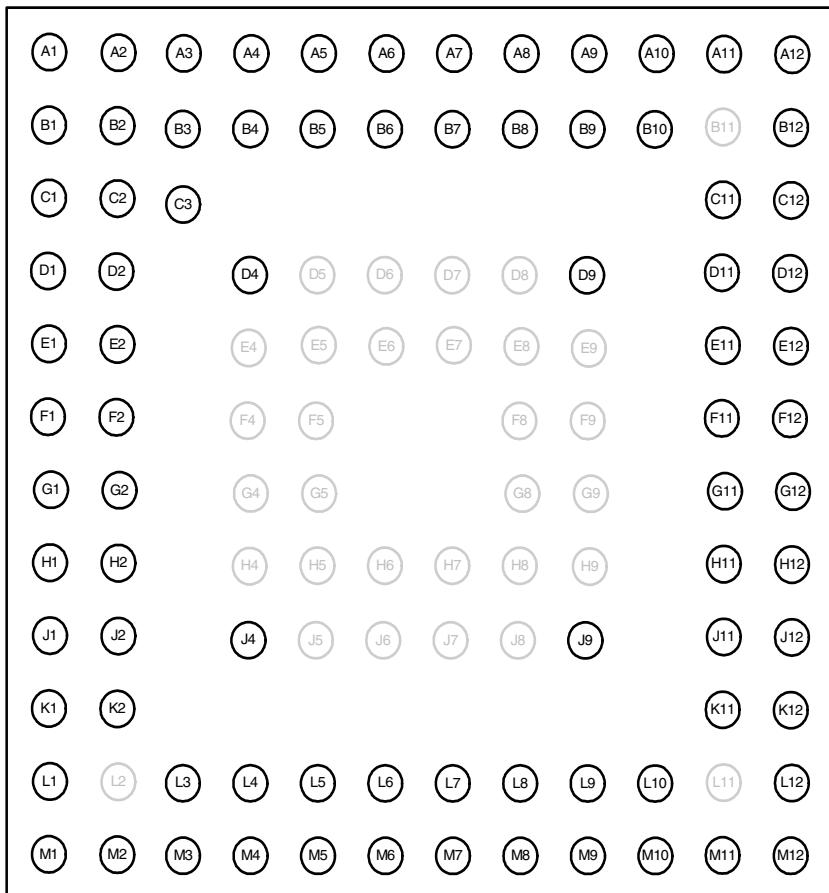
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pin designation, MSP430F261x, 64-pin PM package



pin designation, 113-pin ZQW package

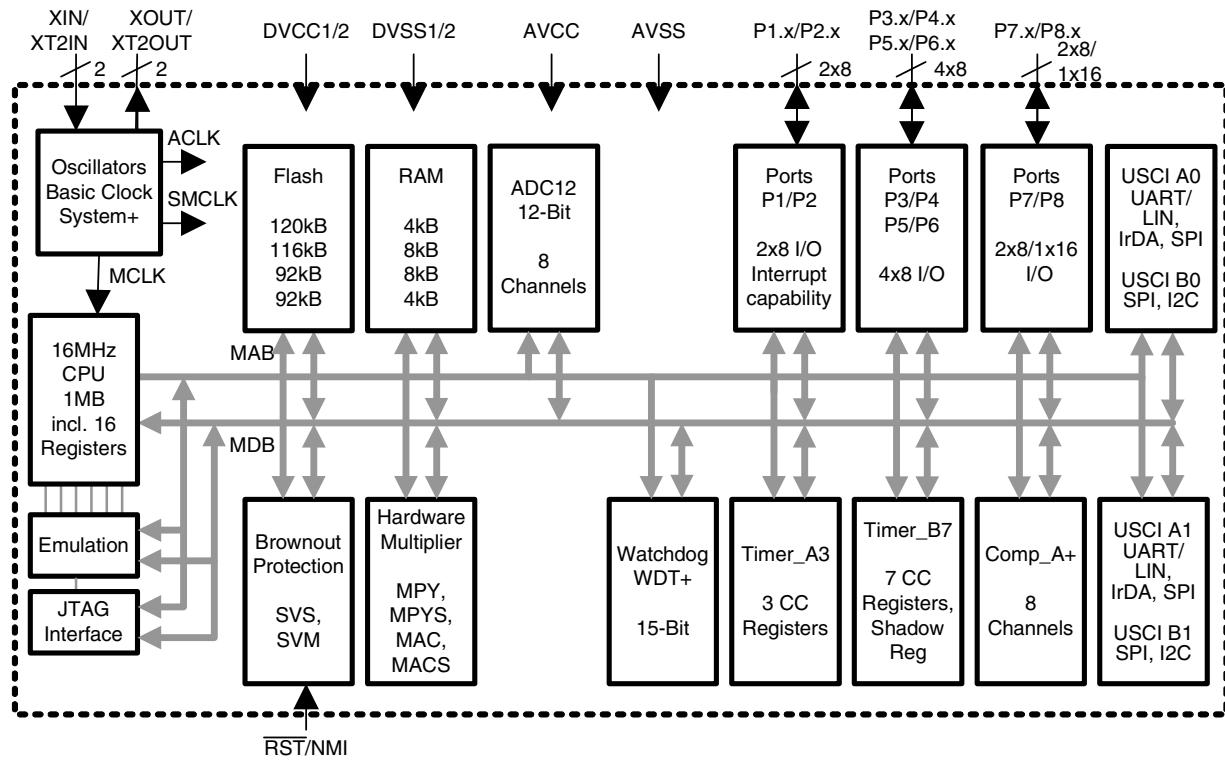


Note: For terminal assignments, see the *MSP430F261x Terminal Functions* table.

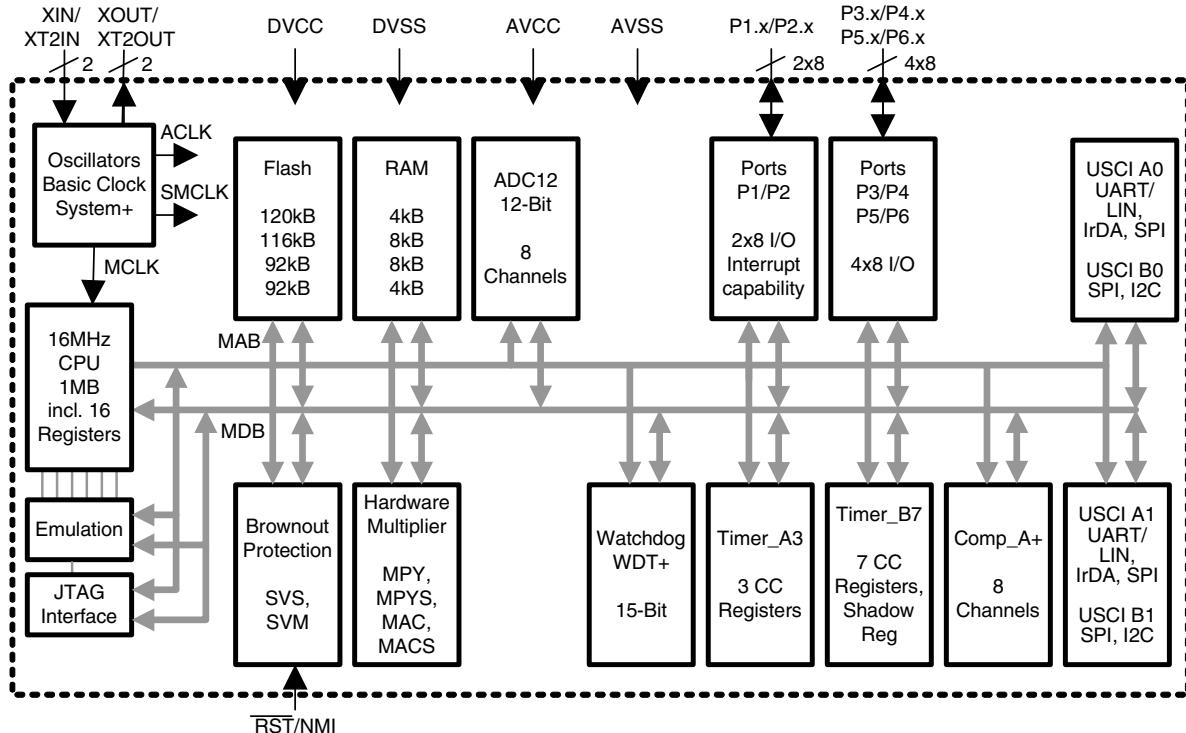
MSP430F241x, MSP430F261x MIXED SIGNAL MICROCONTROLLER

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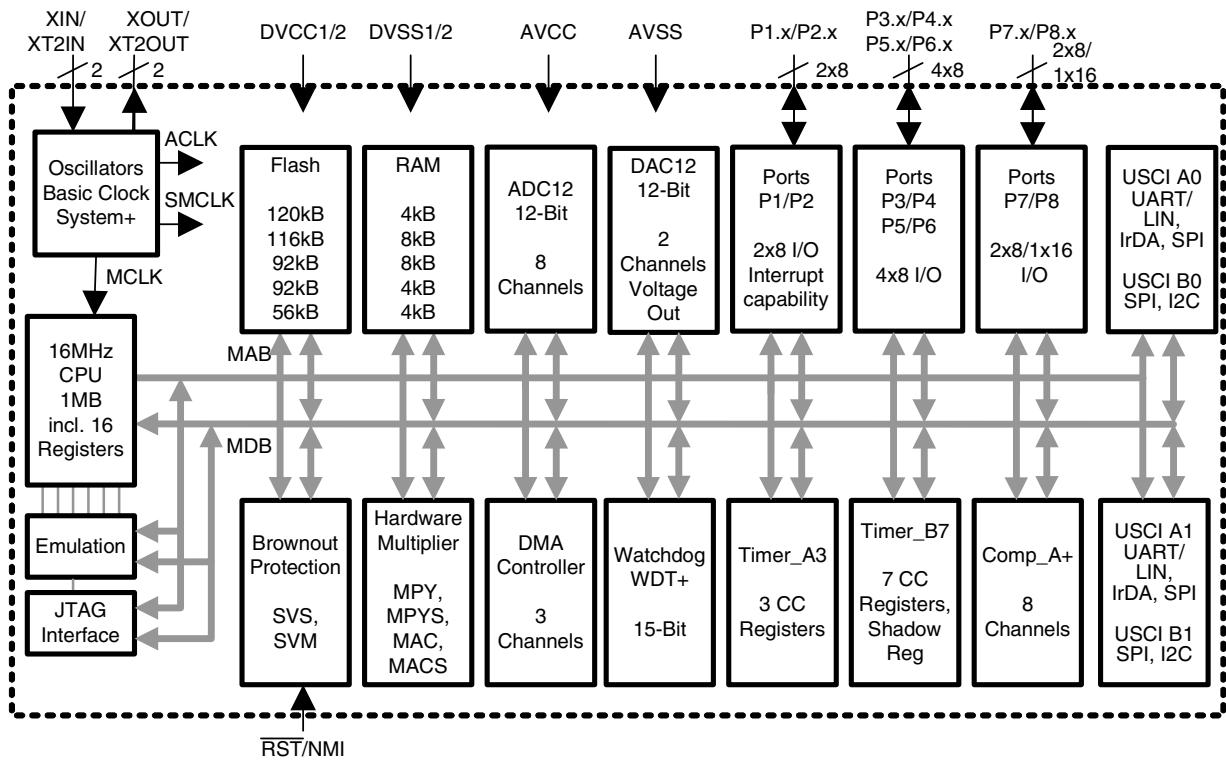
functional block diagram, MSP430F241x, 80-pin PN package



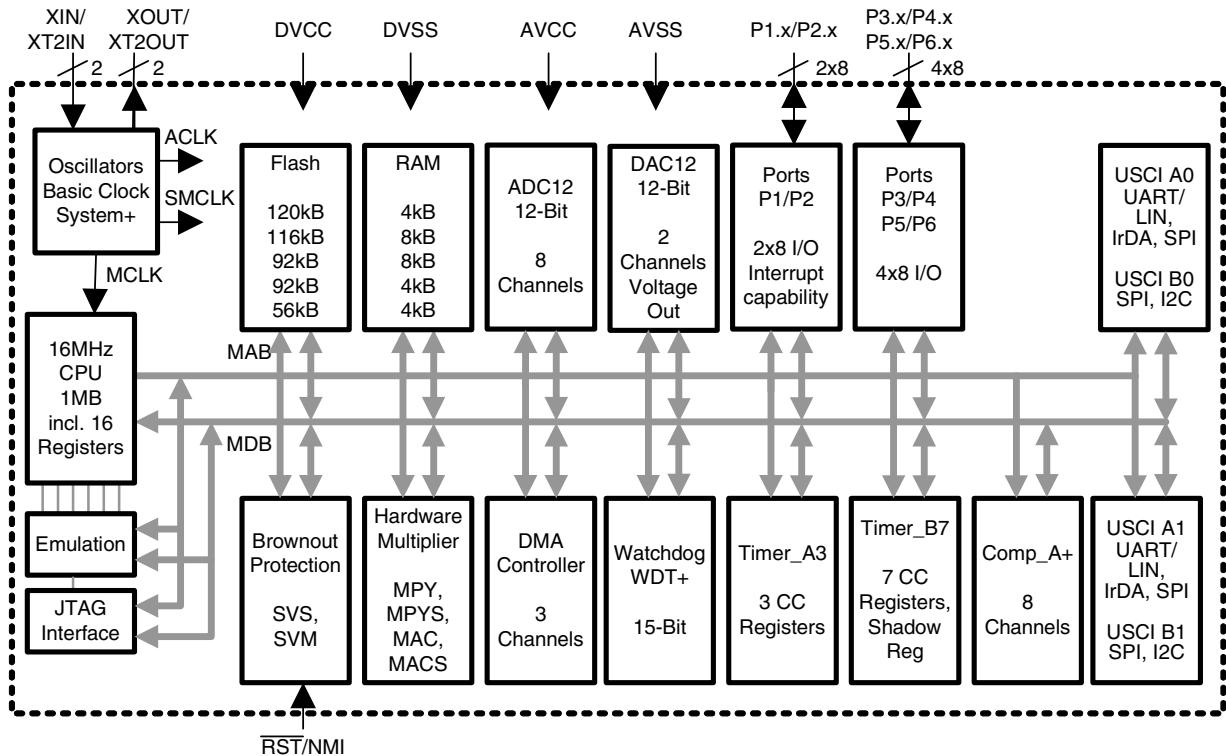
functional block diagram, MSP430F241x, 64-pin PM package



functional block diagram, MSP430F261x, 80-pin PN package



functional block diagram, MSP430F261x, 64-pin PM package



MSP430F241x, MSP430F261x MIXED SIGNAL MICROCONTROLLER

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Terminal Functions

TERMINAL				I/O	DESCRIPTION		
NAME	NO.						
	64 PIN	80 PIN	113 PIN				
AV _{CC}	64	80	A2		Analog supply voltage, positive terminal. Supplies only the analog portion of ADC12 and DAC12.		
AV _{SS}	62	78	B2, B3		Analog supply voltage, negative terminal. Supplies only the analog portion of ADC12 and DAC12.		
DV _{CC1}	1	1	A1		Digital supply voltage, positive terminal. Supplies all digital parts.		
DV _{SS1}	63	79	A3		Digital supply voltage, negative terminal. Supplies all digital parts.		
DV _{CC2}		52	F12		Digital supply voltage, positive terminal. Supplies all digital parts.		
DV _{SS2}		53	E12		Digital supply voltage, negative terminal. Supplies all digital parts.		
P1.0/TACLK/CAOUT	12	12	G2	I/O	General-purpose digital I/O pin/Timer_A, clock signal TACLK input/Comparator_A output		
P1.1/TA0	13	13	H1	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI0A input, compare: Out0 output/BSL transmit		
P1.2/TA1	14	14	H2	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI1A input, compare: Out1 output		
P1.3/TA2	15	15	J1	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI2A input, compare: Out2 output		
P1.4/SMCLK	16	16	J2	I/O	General-purpose digital I/O pin/SMCLK signal output		
P1.5/TA0	17	17	K1	I/O	General-purpose digital I/O pin/Timer_A, compare: Out0 output		
P1.6/TA1	18	18	K2	I/O	General-purpose digital I/O pin/Timer_A, compare: Out1 output		
P1.7/TA2	19	19	L1	I/O	General-purpose digital I/O pin/Timer_A, compare: Out2 output		
P2.0/ACLK/CA2	20	20	M1	I/O	General-purpose digital I/O pin/ACLK output/Comparator_A input		
P2.1/TA1/NCLK/CA3	21	21	M2	I/O	General-purpose digital I/O pin/Timer_A, clock signal at NCLK		
P2.2/CAOUT/TA0/CA4	22	22	M3	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI0B input/Comparator_A output/BSL receive/Comparator_A input		
P2.3/CA0/TA1	23	23	L3	I/O	General-purpose digital I/O pin/Timer_A, compare: Out1 output/Comparator_A input		
P2.4/CA1/TA2	24	24	L4	I/O	General-purpose digital I/O pin/Timer_A, compare: Out2 output/Comparator_A input		
P2.5/Rosc/CA5	25	25	M4	I/O	General-purpose digital I/O pin/input for external resistor defining the DCO nominal frequency/Comparator_A input		
P2.6/ADC12CLK/DMAE0†/CA6	26	26	J4	I/O	General-purpose digital I/O pin/conversion clock – 12-bit ADC/DMA channel 0 external trigger/Comparator_A input		
P2.7/TA0/CA7	27	27	L5	I/O	General-purpose digital I/O pin/Timer_A, compare: Out0 output/Comparator_A input		
P3.0/UCB0STE/UCA0CLK	28	28	M5	I/O	General-purpose digital I/O pin/USCI B0 slave transmit enable/USCI A0 clock input/output		
P3.1/UCB0SIMO/UCB0SDA	29	29	L6	I/O	General-purpose digital I/O pin/USCI B0 slave in/master out in SPI mode, SDA I ² C data in I ² C mode		
P3.2/UCB0SOMI/UCB0SCL	30	30	M6	I/O	General-purpose digital I/O pin/USCI B0 slave out/master in in SPI mode, SCL I ² C clock in I ² C mode		
P3.3/UCB0CLK/UCA0STE	31	31	L7	I/O	General-purpose digital I/O/USCI B0 clock input/output, USCI A0 slave transmit enable		
P3.4/UCA0TXD/UCA0SIMO	32	32	M7	I/O	General-purpose digital I/O pin/USCI A transmit data output in UART mode, slave data in/master out in SPI mode		
P3.5/UCA0RXD/UCA0SOMI	33	33	L8	I/O	General-purpose digital I/O pin/USCI A0 receive data input in UART mode, slave data out/master in in SPI mode		

[†] MSP430F261x devices only



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Terminal Functions (Continued)

TERMINAL				I/O	DESCRIPTION		
NAME	NO.						
	64 PIN	80 PIN	113 PIN				
P3.6/UCA1TXD/ UCA1SIMO	34	34	M8	I/O	General-purpose digital I/O pin/USCI A1 transmit data output in UART mode, slave data in/master out in SPI mode		
P3.7/UCA1RXD/ UCA1SOMI	35	35	L9	I/O	General-purpose digital I/O pin/USCI A1 receive data input in UART mode, slave data out/master in in SPI mode		
P4.0/TB0	36	36	M9	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI0A/B input, compare: Out0 output		
P4.1/TB1	37	37	J9	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI1A/B input, compare: Out1 output		
P4.2/TB2	38	38	M10	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI2A/B input, compare: Out2 output		
P4.3/TB3	39	39	L10	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI3A/B input, compare: Out3 output		
P4.4/TB4	40	40	M11	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI4A/B input, compare: Out4 output		
P4.5/TB5	41	41	M12	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI5A/B input, compare: Out5 output		
P4.6/TB6	42	42	L12	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI6A input, compare: Out6 output		
P4.7/TBCLK	43	43	K11	I/O	General-purpose digital I/O pin/Timer_B, clock signal TBCLK input		
P5.0/UCB1STE/ UCA1CLK	44	44	K12	I/O	General-purpose digital I/O pin/USCI B1 slave transmit enable/USCI A1 clock input/output		
P5.1/UCB1SIMO/ UCB1SDA	45	45	J11	I/O	General-purpose digital I/O pin/USCI B1 slave in/master out in SPI mode, SDA I ² C data in I ² C mode		
P5.2/UCB1SOMI/ UCB1SCL	46	46	J12	I/O	General-purpose digital I/O pin/USCI B1 slave out/master in in SPI mode, SCL I ² C clock in I ² C mode		
P5.3/UCB1CLK/ UCA1STE	47	47	H11	I/O	General-purpose digital I/O/USCI B1 clock input/output, USCI A1 slave transmit enable		
P5.4/MCLK	48	48	H12	I/O	General-purpose digital I/O pin/main system clock MCLK output		
P5.5/SMCLK	49	49	G11	I/O	General-purpose digital I/O pin/submain system clock SMCLK output		
P5.6/ACLK	50	50	G12	I/O	General-purpose digital I/O pin/auxiliary clock ACLK output		
P5.7/TBOUTH/ SVSOUT	51	51	F11	I/O	General-purpose digital I/O pin/switch all PWM digital output ports to high impedance - Timer_B TB0 to TB6/SVS comparator output		
P6.0/A0	59	75	D4	I/O	General-purpose digital I/O pin/analog input A0 – 12-bit ADC		
P6.1/A1	60	76	A4	I/O	General-purpose digital I/O pin/analog input A1 – 12-bit ADC		
P6.2/A2	61	77	B4	I/O	General-purpose digital I/O pin/analog input A2 – 12-bit ADC		
P6.3/A3	2	2	B1	I/O	General-purpose digital I/O pin/analog input A3 – 12-bit ADC		
P6.4/A4	3	3	C1	I/O	General-purpose digital I/O pin/analog input A4 – 12-bit ADC		
P6.5/A5/DAC1 [†]	4	4	C2 C3	I/O	General-purpose digital I/O pin/analog input A5 – 12-bit ADC/DAC12.1 output		
P6.6/A6/DAC0 [†]	5	5	D1	I/O	General-purpose digital I/O pin/analog input A6 – 12-bit ADC/DAC12.0 output		
P6.7/A7/DAC1 [†] / SVSIN	6	6	D2	I/O	General-purpose digital I/O pin/analog input a7 – 12-bit ADC/DAC12.1 output/SVS input		
P7.0		54	E11	I/O	General-purpose digital I/O pin		
P7.1		55	D12	I/O	General-purpose digital I/O pin		
P7.2		56	D11	I/O	General-purpose digital I/O pin		
P7.3		57	C12	I/O	General-purpose digital I/O pin		
P7.4		58	C11	I/O	General-purpose digital I/O pin		
P7.5		59	B12	I/O	General-purpose digital I/O pin		
P7.6		60	A12	I/O	General-purpose digital I/O pin		
P7.7		61	A11	I/O	General-purpose digital I/O pin		

[†] MSP430F261x devices only

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Terminal Functions (Continued)

TERMINAL			I/O	DESCRIPTION		
NAME	NO.					
	64 PIN	80 PIN				
P8.0		62	B10	I/O General-purpose digital I/O pin		
P8.1		63	A10	I/O General-purpose digital I/O pin		
P8.2		64	D9	I/O General-purpose digital I/O pin		
P8.3		65	A9	I/O General-purpose digital I/O pin		
P8.4		66	B9	I/O General-purpose digital I/O pin		
P8.5		67	B8	I/O General-purpose digital I/O pin		
P8.6/XT2OUT		68	A8	O General-purpose digital I/O pin/Output terminal of crystal oscillator XT2		
P8.7/XT2IN		69	A7	I General-purpose digital I/O pin/Input port for crystal oscillator XT2. Only standard crystals can be connected.		
XT2OUT	52		O	Output terminal of crystal oscillator XT2		
XT2IN	53		I	Input port for crystal oscillator XT2		
RST/NMI	58	74	B5	I Reset input, nonmaskable interrupt input port, or bootstrap loader start (in flash devices).		
TCK	57	73	A5	I Test clock (JTAG). TCK is the clock input port for device programming test and bootstrap loader start.		
TDI/TCLK	55	71	A6	I Test data input or test clock input. The device protection fuse is connected to TDI/TCLK.		
TDO/TDI	54	70	B7	I/O Test data output port. TDO/TDI data output or programming data input terminal.		
TMS	56	72	B6	I Test mode select. TMS is used as an input port for device programming and test.		
V _{eREF+} /DAC0 [†]	10	10	F2	I Input for an external reference voltage/DAC12.0 output		
V _{REF+}	7	7	E2	O Output of positive terminal of the reference voltage in the ADC12		
V _{REF-/-V_{eREF-}}	11	11	G1	I Negative terminal for the reference voltage for both sources, the internal reference voltage, or an external applied reference voltage		
XIN	8	8	E1	I Input port for crystal oscillator XT1. Standard or watch crystals can be connected.		
XOUT	9	9	F1	O Output port for crystal oscillator XT1. Standard or watch crystals can be connected.		
Reserved	-	-	L2, E4 F4, G4 H4, D5 E5, F5 G5, H5 J5, D6 E6, H6 J6, D7 E7, H7 J7, D8 E8, F8 G8, H8 J8, E9 F9, G9 H9, B11 L11	NA Reserved pins. Connection to D/A/V _{SS} recommended.		

[†] MSP430F261x devices only

short-form description

CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats; the address modes are listed in Table 2.

Program Counter	PC/R0
Stack Pointer	SP/R1
Status Register	SR/CG1/R2
Constant Generator	CG2/R3
General-Purpose Register	R4
General-Purpose Register	R5
General-Purpose Register	R6
General-Purpose Register	R7
General-Purpose Register	R8
General-Purpose Register	R9
General-Purpose Register	R10
General-Purpose Register	R11
General-Purpose Register	R12
General-Purpose Register	R13
General-Purpose Register	R14
General-Purpose Register	R15

Table 1. Instruction Word Formats

Dual operands, source-destination	e.g., ADD R4,R5	R4 + R5 ---> R5
Single operands, destination only	e.g., CALL R8	PC --->(TOS), R8---> PC
Relative jump, un/conditional	e.g., JNE	Jump-on-equal bit = 0

Table 2. Address Mode Descriptions

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	●	●	MOV Rs,Rd	MOV R10,R11	R10 ---> R11
Indexed	●	●	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5) ---> M(6+R6)
Symbolic (PC relative)	●	●	MOV EDE,TONI		M(EDE) ---> M(TONI)
Absolute	●	●	MOV &MEM,&TC DAT		M(MEM) ---> M(TCDAT)
Indirect	●		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) ---> M(Tab+R6)
Indirect autoincrement	●		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) ---> R11 R10 + 2 ---> R10
Immediate	●		MOV #X,TONI	MOV #45,TONI	#45 ---> M(TONI)

NOTE: S = source D = destination

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operating modes

The MSP430 has one active mode and five software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
 - All clocks are active.
- Low-power mode 0 (LPM0)
 - CPU is disabled.
 - ACLK and SMCLK remain active. MCLK is disabled.
- Low-power mode 1 (LPM1)
 - CPU is disabled.
 - ACLK and SMCLK remain active. MCLK is disabled.
 - DCO's dc generator is disabled if DCO not used in active mode.
- Low-power mode 2 (LPM2)
 - CPU is disabled.
 - MCLK and SMCLK are disabled.
 - DCO's dc generator remains enabled.
 - ACLK remains active.
- Low-power mode 3 (LPM3)
 - CPU is disabled.
 - MCLK and SMCLK are disabled.
 - DCO's dc generator is disabled.
 - ACLK remains active.
- Low-power mode 4 (LPM4)
 - CPU is disabled.
 - ACLK is disabled.
 - MCLK and SMCLK are disabled.
 - DCO's dc generator is disabled.
 - Crystal oscillator is stopped.



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interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the address range 0xFFFF to 0xFFC0. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence. If the reset vector (0xFFFFE) contains 0xFFFF (e.g., flash is not programmed), the CPU enters LPM4 after power-up.

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-up External Reset Watchdog Flash Key Violation PC out of range (see Note 1)	PORIFG WDTIFG RSTIFG KEYV (see Note 2)	Reset	0xFFFFE	31, highest
NMI Oscillator Fault Flash memory access violation	NMIIFG OFIFG ACCVIFG (see Notes 2 and 6)	(Non)maskable (Non)maskable (Non)maskable	0x0FFFC	30
Timer_B7	TBCCR0 CCIFG (see Note 3)	Maskable	0x0FFFA	29
Timer_B7	TBCCR1 to TBCCR6 CCIFGs, TBIFG (see Notes 2 and 3)	Maskable	0x0FFF8	28
Comparator_A+	CAIFG	Maskable	0x0FFF6	27
Watchdog timer+	WDTIFG	Maskable	0x0FFF4	26
Timer_A3	TACCR0 CCIFG (see Note 3)	Maskable	0x0FFF2	25
Timer_A3	TACCR1 CCIFG TACCR2 CCIFG TAIFG (see Notes 2 and 3)	Maskable	0x0FFF0	24
USCI_A0/USCI_B0 receive USCI_B0 I2C status	UCA0RXIFG, UCB0RXIFG (see Notes 2 and 4)	Maskable	0x0FFEE	23
USCI_A0/USCI_B0 transmit USCI_B0 I2C receive/transmit	UCA0TXIFG, UCB0TXIFG (see Note 2 and 5)	Maskable	0x0FFEC	22
ADC12	ADC12IFG (see Notes 2 and 3)	Maskable	0x0FFEA	21
			0x0FFE8	20
I/O port P2 (eight flags)	P2IFG.0 to P2IFG.7 (see Notes 2 and 3)	Maskable	0x0FFE6	19
I/O port P1 (eight flags)	P1IFG.0 to P1IFG.7 (see Notes 2 and 3)	Maskable	0x0FFE4	18
USCI_A0/USCI_B1 receive USCI_B1 I2C status	UCA1RXIFG, UCB1RXIFG (see Notes 2 and 4)	Maskable	0x0FFE2	17
USCI_A1/USCI_B1 transmit USCI_B1 I2C receive/transmit	UCA1TXIFG, UCB1TXIFG (see Notes 2 and 5)	Maskable	0x0FFE0	16
DMA	DMA0IFG, DMA1IFG, DMA2IFG (see Notes 2 and 3)	Maskable	0x0FFDE	15
DAC12	DAC12_0IFG, DAC12_1IFG (see Notes 2 and 3)	Maskable	0x0FFDC	14
Reserved (see Notes 7 and 8)	Reserved		0x0FFDA to 0x0FFC0	13 to 0, lowest

- NOTES:
- A reset is executed if the CPU tries to fetch instructions from within the module register memory address range (0x00000 to 0x001FF) or from within unused address ranges.
 - Multiple source flags.
 - Interrupt flags are located in the module.
 - In SPI mode: UCB0RXIFG. In I2C mode: UCALIFG, UCNACKIFG, ICSTTIIFG, UCSTPIFG.
 - In UART/SPI mode: UCB0TXIFG. In I2C mode: UCB0RXIFG, UCB0TXIFG.
 - (Non)maskable: The individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot.
 - The address 0xFFBE is used as bootstrap loader security key (BSLSKEY). A 0xAA55 at this location disables the BSL completely.
 - A zero disables the erasure of the flash if an invalid password is supplied.
 - The interrupt vectors at addresses 0xFFDA to 0xFFC0 are not used in this device and can be used for regular program code if necessary.

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special function registers

Most interrupt enable bits are collected in the lowest address space. Special-function register bits not allocated to a functional purpose are not physically present in the device. This arrangement provides simple software access.

interrupt enable 1 and 2

Address	7	6	5	4	3	2	1	0
00h			ACCVIE	NMIIE			OFIE	WDTIE

Interrupt Enable Register 1

- WDTIE Watchdog timer interrupt enable. Inactive if watchdog mode is selected.
Active if watchdog timer is configured as general-purpose timer.
- OFIE Oscillator fault interrupt enable
- NMIIE Nonmaskable interrupt enable
- ACCVIE Flash memory access violation interrupt enable

Address	7	6	5	4	3	2	1	0
01h					UCB0TXIE	UCB0RXIE	UCA0TXIE	UCA0RXIE

Interrupt Enable Register 2

- UCA0RXIE USCI_A0 receive interrupt enable
- UCA0TXIE USCI_A0 transmit interrupt enable
- UCB0RXIE USCI_B0 receive interrupt enable
- UCB0TXIE USCI_B0 transmit interrupt enable

interrupt flag register 1 and 2

Address	7	6	5	4	3	2	1	0
02h				NMIIFG	RSTIFG	PORIFG	OFIFG	WDTIFG

rw-0 rw-(0) rw-(1) rw-1 rw-(0)

Interrupt Flag Register 1

- WDTIFG** Set on watchdog timer overflow or security key violation
 Reset on V_{CC} power-on or a reset condition at the RST/NMI pin in reset mode.
OFIFG Flag set on oscillator fault7
PORIFG Power-on interrupt flag. Set on V_{CC} power up.
RSTIFG External reset interrupt flag. Set on a reset condition at RST/NMI pin in reset mode. Reset on V_{CC} power up.
NMIIFG Set via RST/NMI pin

Address	7	6	5	4	3	2	1	0
03h					UCB0TX IFG	UCB0RX IFG	UCA0TX IFG	UCA0RX IFG

rw-1 rw-0 rw-1 rw-0

Interrupt Flag Register 2

- UCA0RXIFG** USCI_A0 receive interrupt flag
UCA0TXIFG USCI_A0 transmit interrupt flag
UCB0RXIFG USCI_B0 receive interrupt flag
UCB0TXIFG USCI_B0 transmit interrupt flag

Legend

rw:	Bit can be read and written.
rw-0,1:	Bit can be read and written. It is Reset or Set by PUC.
rw-(0,1)	Bit can be read and written. It is Reset or Set by POR. SFR bit is not present in device.

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memory organization

		MSP430F2416 MSP430F2616	MSP430F2417 MSP430F2617
Memory	Size	92KB	92KB
Main: interrupt vector	Flash	0x0FFFF - 0x0FFC0	0x0FFFF - 0x0FFC0
Main: code memory	Flash	0x18FFF - 0x02100	0x19FFF - 0x03100
RAM (total)	Size	4kB	8kB
Extended	Size	0x020FF - 0x01100	0x030FF - 0x01100
Mirrored	Size	2kB	6kB
		0x020FF - 0x01900	0x030FF - 0x01900
		2kB	2kB
		0x018FF - 0x01100	0x018FF - 0x01100
Information memory	Size	256 Byte	256 Byte
	Flash	0x010FF - 0x01000	0x010FF - 0x01000
Boot memory	Size	1KB	1KB
	ROM	0x00FFF - 0x00C00	0x00FFF - 0x00C00
RAM (mirrored at 0x18FF to 0x01100)	Size	2KB	2KB
		0x009FF - 0x00200	0x009FF - 0x00200
Peripherals	16-bit	0x001FF - 0x00100	0x001FF - 0x00100
	8-bit	0x000FF - 0x00010	0x000FF - 0x00010
	8-bit SFR	0x0000F - 0x00000	0x0000F - 0x00000

		MSP430F2618 MSP430F2418	MSP430F2619 MSP430F2419
Memory	Size	116KB	120KB
Main: interrupt vector	Flash	0x0FFFF - 0x0FFC0	0x0FFFF - 0x0FFC0
Main: code memory	Flash	0x1FFFF - 0x03100	0x1FFFF - 0x02100
RAM (total)	Size	8kB	4kB
Extended	Size	0x030FF - 0x01100	0x020FF - 0x01100
Mirrored	Size	6kB	2kB
		0x030FF - 0x01900	0x020FF - 0x01900
		2kB	2kB
		0x018FF - 0x01100	0x018FF - 0x01100
Information memory	Size	256 Byte	256 Byte
	Flash	0x010FF - 0x01000	0x010FF - 0x01000
Boot memory	Size	1KB	1KB
	ROM	0x00FFF - 0x00C00	0x00FFF - 0x00C00
RAM (mirrored at 0x18FF to 0x01100)	Size	2KB	2KB
		0x009FF - 0x00200	0x009FF - 0x00200
Peripherals	16-bit	0x001FF - 0x00100	0x001FF - 0x00100
	8-bit	0x000FF - 0x00010	0x000FF - 0x00010
	8-bit SFR	0x0000F - 0x00000	0x0000F - 0x00000

bootstrap loader (BSL)

The MSP430 BSL enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by a user-defined password. For complete description of the features of the BSL and its implementation, see the application report *Features of the MSP430 Bootstrap Loader*, literature number SLAA089.

BSL FUNCTION	PM, PN PACKAGE PINS	ZQW PACKAGE PINS
Data Transmit	13 - P1.1	H1 - P1.1
Data Receive	22 - P2.2	M3 - P2.2

flash memory

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n. Segments A to D are also called *information memory*.
- Segment A contains calibration data. After reset, segment A is protected against programming or erasing. It can be unlocked, but care should be taken not to erase this segment if the calibration data is required.
- Flash content integrity check with marginal read modes

peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x2xx Family User's Guide*, literature number SLAU144.

DMA controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC12 conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode without having to awaken to move data to or from a peripheral.

oscillator and system clock

The clock system in the MSP430x241x and MSP430x261x family of devices is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal very low-power low-frequency oscillator, an internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator. The basic clock module is designed to meet the requirements of both low system cost and low power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 1 μ s. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal, a high-frequency crystal, or a very low-power LF oscillator
- Main clock (MCLK), the system clock used by the CPU
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules

The DCO settings to calibrate the DCO output frequency are stored in the information memory segment A.

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calibration data stored in information memory segment A

Calibration data is stored for the DCO and for the ADC12. It is organized in a tag-length-value (TLV) structure.

TAGS USED BY THE TLV STRUCTURE			
NAME	ADDRESS	VALUE	DESCRIPTION
TAG_DCO_30	0x10F6	0x01	DCO frequency calibration at VCC = 3 V and TA = 25°C at calibration
TAG_ADC12_1	0x10DA	0x08	ADC12_1 calibration tag
TAG_EMPTY	-	0xFE	Identifier for empty memory areas

LABELS USED BY THE ADC CALIBRATION STRUCTURE			
LABEL	CONDITION AT CALIBRATION / DESCRIPTION	SIZE	ADDRESS OFFSET
CAL_ADC_25T85	INCHx = 0x1010; REF2_5 = 1, TA = 85°C	word	0x000E
CAL_ADC_25T30	INCHx = 0x1010; REF2_5 = 1, TA = 30°C	word	0x000C
CAL_ADC_25VREF_FACTOR	REF2_5 = 1, TA = 30°C	word	0x000A
CAL_ADC_15T85	INCHx = 0x1010; REF2_5 = 0, TA = 85°C	word	0x0008
CAL_ADC_15T30	INCHx = 0x1010; REF2_5 = 0, TA = 30°C	word	0x0006
CAL_ADC_15VREF_FACTOR	REF2_5 = 0, TA = 30°C	word	0x0004
CAL_ADC_OFFSET	External V _{REF} = 1.5 V, f _{ADC12CLK} = 5 MHz	word	0x0002
CAL_ADC_GAIN_FACTOR	External V _{REF} = 1.5 V, f _{ADC12CLK} = 5 MHz	word	0x0000
CAL_BC1_1MHZ	-	byte	0x0007
CAL_DCO_1MHZ	-	byte	0x0006
CAL_BC1_8MHZ	-	byte	0x0005
CAL_DCO_8MHZ	-	byte	0x0004
CAL_BC1_12MHZ	-	byte	0x0003
CAL_DCO_12MHZ	-	byte	0x0002
CAL_BC1_16MHZ	-	byte	0x0001
CAL_DCO_16MHZ	-	byte	0x0000

brownout, supply voltage supervisor (SVS)

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off. The SVS circuitry detects if the supply voltage drops below a user selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (SVM) (the device is not automatically reset).

The CPU begins code execution after the brownout circuit releases the device reset. However, V_{CC} may not have ramped to V_{CC(min)} at that time. The user must ensure that the default DCO settings are not changed until V_{CC} reaches V_{CC(min)}. If desired, the SVS circuit can be used to determine when V_{CC} reaches V_{CC(min)}.

digital I/O

There are up to eight 8-bit I/O ports implemented—ports P1 through P8:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all eight bits of ports P1 and P2.
- Read/write access to port-control registers is supported by all instructions.
- Each I/O has an individually programmable pullup/pulldown resistor.
- Ports P7/P8 can be accessed word-wise.



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watchdog timer+ (WDT+)

The primary function of the WDT+ module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

hardware multiplier

The multiplication operation is supported by a dedicated peripheral module. The module performs 16×16 , 16×8 , 8×16 , and 8×8 bit operations. The module is capable of supporting signed and unsigned multiplication as well as signed and unsigned multiply and accumulate operations. The result of an operation can be accessed immediately after the operands have been loaded into the peripheral registers. No additional clock cycles are required.

universal serial communication interface (USCI)

The USCI modules are used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3 pin or 4 pin) or I²C, and asynchronous combination protocols such as UART, enhanced UART with automatic baudrate detection (LIN), and IrDA.

The USCI A module provides support for SPI (3 pin or 4 pin), UART, enhanced UART, and IrDA.

The USCI B module provides support for SPI (3 pin or 4 pin) and I²C.

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Timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/comparisons, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

TIMER_A3 SIGNAL CONNECTIONS							
INPUT PIN NUMBER (ZQW)	INPUT PIN NUMBER (PM, PN)	DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER (PM, PN)	OUTPUT PIN NUMBER (ZQW)
G2 - P1.0	12 - P1.0	TACLK	TACLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
M2 - P2.1	21 - P2.1	TAINCLK	INCLK				
H1 - P1.1	13 - P1.1	TA0	CC10A	CCR0	TA0	13 - P1.1	H1 - P1.1
M3 - P2.2	22 - P2.2	TA0	CC10B			17 - P1.5	K1 - P1.5
		DV _{SS}	GND			27 - P2.7	L5 - P2.7
		DV _{CC}	V _{CC}				
H2 - P1.2	14 - P1.2	TA1	CC11A	CCR1	TA1	14 - P1.2	H2 - P1.2
		CAOUT (internal)	CC11B			18 - P1.6	K2 - P1.6
		DV _{SS}	GND			23 - P2.3	L3 - P2.3
		DV _{CC}	V _{CC}			ADC12 (internal)	
J1 - P1.3	15 - P1.3	TA2	CC12A	CCR2	TA2	15 - P1.3	J1 - P1.3
		ACLK (internal)	CC12B			19 - P1.7	L1 - P1.7
		DV _{SS}	GND			24 - P2.4	L4 - P2.4
		DV _{CC}	V _{CC}				

Timer_B7

Timer_B7 is a 16-bit timer/counter with seven capture/compare registers. Timer_B7 can support multiple capture/comparisons, PWM outputs, and interval timing. Timer_B7 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

TIMER_B3/B7 SIGNAL CONNECTIONS [†]							
INPUT PIN NUMBER (ZQW)	INPUT PIN NUMBER (PM, PN)	DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER (PM, PN)	OUTPUT PIN NUMBER (ZQW)
K11 - P4.7	43 - P4.7	TBCLK	TBCLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
K11 - P4.7	43 - P4.7	TBCLK	INCLK				
M9 - P4.0	36 - P4.0	TB0	CC10A	CCR0	TBO	36 - P4.0	M9 - P4.0
M9 - P4.0	36 - P4.0	TB0	CC10B			ADC12 (internal)	
		DV _{SS}	GND				
		DV _{CC}	V _{CC}				
J9 - P4.1	37 - P4.1	TB1	CC11A	CCR1	TB1	37 - P4.1	J9 - P4.1
J9 - P4.1	37 - P4.1	TB1	CC11B			ADC12 (internal)	
		DV _{SS}	GND				
		DV _{CC}	V _{CC}				
M10 - P4.2	38 - P4.2	TB2	CC12A	CCR2	TB2	38 - P4.2	M10 - P4.2
M10 - P4.2	38 - P4.2	TB2	CC12B			DAC_0(internal)	
		DV _{SS}	GND			DAC_1(internal)	
		DV _{CC}	V _{CC}				
L10 - P4.3	39 - P4.3	TB3	CC13A	CCR3	TB3	39 - P4.3	L10 - P4.3
L10 - P4.3	39 - P4.3	TB3	CC13B				
		DV _{SS}	GND				
		DV _{CC}	V _{CC}				
M11 - P4.4	40 - P4.4	TB4	CC14A	CCR4	TB4	40 - P4.4	M11 - P4.4
M11 - P4.4	40 - P4.4	TB4	CC14B				
		DV _{SS}	GND				
		DV _{CC}	V _{CC}				
M12 - P4.5	41 - P4.5	TB5	CC15A	CCR5	TB5	41 - P4.5	M12 - P4.5
M12 - P4.5	41 - P4.5	TB5	CC15B				
		DV _{SS}	GND				
		DV _{CC}	V _{CC}				
L12 - P4.6	42 - P4.6	TB6	CC16A	CCR6	TB6	42 - P4.6	L12 - P4.6
		ACLK (internal)	CC16B				
		DV _{SS}	GND				
		DV _{CC}	V _{CC}				

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Comparator_A+

The primary function of the comparator_A+ module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

ADC12

The ADC12 module supports fast 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, reference generator, and a 16-word conversion-and-control buffer. The conversion-and-control buffer allows up to 16 independent ADC samples to be converted and stored without any CPU intervention.

DAC12

The DAC12 module is a 12-bit, R-ladder, voltage-output digital-to-analog converter (DAC). The DAC12 may be used in 8-bit or 12-bit mode and may be used in conjunction with the DMA controller. When multiple DAC12 modules are present, they may be grouped together for synchronous operation.



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peripheral file map

PERIPHERAL FILE MAP			
DMA [†]	DMA channel 2 transfer size DMA channel 2 destination address DMA channel 2 source address DMA channel 2 control DMA channel 1 transfer size DMA channel 1 destination address DMA channel 1 source address DMA channel 1 control DMA channel 0 transfer size DMA channel 0 destination address DMA channel 0 source address DMA channel 0 control DMA module interrupt vector word DMA module control 1 DMA module control 0	DMA2SZ DMA2DA DMA2SA DMA2CTL DMA1SZ DMA1DA DMA1SA DMA1CTL DMA0SZ DMA0DA DMA0SA DMA0CTL DMAIV DMACTL1 DMACTL0	0x01F2 0x01EE 0x01EA 0x01E8 0x01E6 0x01E2 0x01DE 0x01DC 0x01DA 0x01D6 0x01D2 0x01D0 0x0126 0x0124 0x0122
DAC12 [†]	DAC12_1 data DAC12_1 control DAC12_0 data DAC12_0 control	DAC12_1DAT DAC12_1CTL DAC12_0DAT DAC12_0CTL	0x01CA 0x01C2 0x01C8 0x01C0
ADC12	Interrupt-vector-word register Inerrupt-enable register Inerrupt-flag register Control register 1 Control register 0 Conversion memory 15 Conversion memory 14 Conversion memory 13 Conversion memory 12 Conversion memory 11 Conversion memory 10 Conversion memory 9 Conversion memory 8 Conversion memory 7 Conversion memory 6 Conversion memory 5 Conversion memory 4 Conversion memory 3 Conversion memory 2 Conversion memory 1 Conversion memory 0	ADC12IV ADC12IE ADC12IFG ADC12CTL1 ADC12CTL0 ADC12MEM15 ADC12MEM14 ADC12MEM13 ADC12MEM12 ADC12MEM11 ADC12MEM10 ADC12MEM9 ADC12MEM8 ADC12MEM7 ADC12MEM6 ADC12MEM5 ADC12MEM4 ADC12MEM3 ADC12MEM2 ADC12MEM1 ADC12MEM0	0x01A8 0x01A6 0x01A4 0x01A2 0x01A0 0x015E 0x015C 0x015A 0x0158 0x0156 0x0154 0x0152 0x0150 0x014E 0x014C 0x014A 0x0148 0x0146 0x0144 0x0142 0x0140

[†] MSP430F261x devices only

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PERIPHERAL FILE MAP (CONTINUED)			
ADC12 (continued)	ADC memory-control register15 ADC memory-control register14 ADC memory-control register13 ADC memory-control register12 ADC memory-control register11 ADC memory-control register10 ADC memory-control register9 ADC memory-control register8 ADC memory-control register7 ADC memory-control register6 ADC memory-control register5 ADC memory-control register4 ADC memory-control register3 ADC memory-control register2 ADC memory-control register1 ADC memory-control register0	ADC12MCTL15 ADC12MCTL14 ADC12MCTL13 ADC12MCTL12 ADC12MCTL11 ADC12MCTL10 ADC12MCTL9 ADC12MCTL8 ADC12MCTL7 ADC12MCTL6 ADC12MCTL5 ADC12MCTL4 ADC12MCTL3 ADC12MCTL2 ADC12MCTL1 ADC12MCTL0	0x008F 0x008E 0x008D 0x008C 0x008B 0x008A 0x0089 0x0088 0x0087 0x0086 0x0085 0x0084 0x0083 0x0082 0x0081 0x0080
Timer_B7	Capture/compare register 6 Capture/compare register 5 Capture/compare register 4 Capture/compare register 3 Capture/compare register 2 Capture/compare register 1 Capture/compare register 0 Timer_B register Capture/compare control 6 Capture/compare control 5 Capture/compare control 4 Capture/compare control 3 Capture/compare control 2 Capture/compare control 1 Capture/compare control 0 Timer_B control Timer_B interrupt vector	TBCCR6 TBCCR5 TBCCR4 TBCCR3 TBCCR2 TBCCR1 TBCCR0 TBR TBCCTL6 TBCCTL5 TBCCTL4 TBCCTL3 TBCCTL2 TBCCTL1 TBCCTL0 TBCTL TBIV	0x019E 0x019C 0x019A 0x0198 0x0196 0x0194 0x0192 0x0190 0x018E 0x018C 0x018A 0x0188 0x0186 0x0184 0x0182 0x0180 0x011E
Timer_A3	Capture/compare register 2 Capture/compare register 1 Capture/compare register 0 Timer_A register Reserved Reserved Reserved Reserved Capture/compare control 2 Capture/compare control 1 Capture/compare control 0 Timer_A control Timer_A interrupt vector	TACCR2 TACCR1 TACCR0 TAR TACCTL2 TACCTL1 TACCTL0 TACTL TAIV	0x0176 0x0174 0x0172 0x0170 0x016E 0x016C 0x016A 0x0168 0x0166 0x0164 0x0162 0x0160 0x012E

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PERIPHERAL FILE MAP (CONTINUED)			
Hardware Multiplier	Sum extend Result high word Result low word Second operand Multiply signed +accumulate/operand1 Multiply+accumulate/operand1 Multiply signed/operand1 Multiply unsigned/operand1	SUMEXT RESHI RESLO OP2 MACS MAC MPYS MPY	0x013E 0x013C 0x013A 0x0138 0x0136 0x0134 0x0132 0x0130
Flash	Flash control 4 Flash control 3 Flash control 2 Flash control 1	FCTL4 FCTL3 FCTL2 FCTL1	0x01BE 0x012C 0x012A 0x0128
Watchdog	Watchdog Timer control	WDTCTL	0x0120
USCI A0/B0	USCI A0 auto baud rate control USCI A0 transmit buffer USCI A0 receive buffer USCI A0 status USCI A0 modulation control USCI A0 baud rate control 1 USCI A0 baud rate control 0 USCI A0 control 1 USCI A0 control 0 USCI A0 IrDA receive control USCI A0 IrDA transmit control USCI B0 transmit buffer USCI B0 receive buffer USCI B0 status USCI B0 I2C interrupt enable USCI B0 baud rate control 1 USCI B0 baud rate control 0 USCI B0 control 1 USCI B0 control 0 USCI B0 I2C slave address USCI B0 I2C own address	UCA0ABCTL UCA0TXBUF UCA0RXBUF UCA0STAT UCA0MCTL UCA0BR1 UCA0BR0 UCA0CTL1 UCA0CTL0 UCA0IRRCTL UCA0IRCLT UCB0TXBUF UCB0RXBUF UCB0STAT UCB0CIE UCB0BR1 UCB0BR0 UCB0CTL1 UCB0CTL0 UCB0SA UCB0OA	0x005D 0x0067 0x0066 0x0065 0x0064 0x0063 0x0062 0x0061 0x0060 0x005F 0x005E 0x006F 0x006E 0x006D 0x006C 0x006B 0x006A 0x0069 0x0068 0x011A 0x0118
USCI A1/B1	USCI A1 auto baud rate control USCI A1 transmit buffer USCI A1 receive buffer USCI A1 status USCI A1 modulation control USCI A1 baud rate control 1 USCI A1 baud rate control 0 USCI A1 control 1 USCI A1 control 0 USCI A1 IrDA receive control USCI A1 IrDA transmit control	UCA1ABCTL UCA1TXBUF UCA1RXBUF UCA1STAT UCA1MCTL UCA1BR1 UCA1BR0 UCA1CTL1 UCA1CTL0 UCA1IRRCTL UCA1IRCLT	0x00CD 0x00D7 0x00D6 0x00D5 0x00D4 0x00D3 0x00D2 0x00D1 0x00D0 0x00CF 0x00CE

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PERIPHERAL FILE MAP (CONTINUED)			
USCI A1/B1 (continued)	USCI B1 transmit buffer USCI B1 receive buffer USCI B1 status USCI B1 I2C interrupt enable USCI B1 baud rate control 1 USCI B1 baud rate control 0 USCI B1 control 1 USCI B1 control 0 USCI B1 I2C slave address USCI B1 I2C own address USCI A1/B1 interrupt enable USCI A1/B1 interrupt flag	UCB1TXBUF UCB1RXBUF UCB1STAT UCB1CIE UCB1BR1 UCB1BR0 UCB1CTL1 UCB1CTL0 UCB1SA UCB1OA UC1IE UC1IFG	0x00DF 0x00DE 0x00DD 0x00DC 0x00DB 0x00DA 0x00D9 0x00D8 0x017E 0x017C 0x0006 0x0007
Comparator_A+	Comparator_A port disable Comparator_A control2 Comparator_A control1	CAPD CACTL2 CACTL1	0x005B 0x005A 0x0059
Basic Clock	Basic clock system control3 Basic clock system control2 Basic clock system control1 DCO clock frequency control	BCSCTL3 BCSCTL2 BCSCTL1 DCOCTL	0x0053 0x0058 0x0057 0x0056
Brownout, SVS	SVS control register (reset by brownout signal)	SVSCTL	0x0055
Port PA[†]	Port PA resistor enable Port PA selection Port PA direction Port PA output Port PA input	PAREN PASEL PADIR PAOUT PAIN	0x0014 0x003E 0x003C 0x003A 0x0038
Port P8[†]	Port P8 resistor enable Port P8 selection Port P8 direction Port P8 output Port P8 input	P8REN P8SEL P8DIR P8OUT P8IN	0x0015 0x003F 0x003D 0x003B 0x0039
Port P7[†]	Port P7 resistor enable Port P7 selection Port P7 direction Port P7 output Port P7 input	P7REN P7SEL P7DIR P7OUT P7IN	0x0014 0x003E 0x003C 0x003A 0x0038
Port P6	Port P6 resistor enable Port P6 selection Port P6 direction Port P6 output Port P6 input	P6REN P6SEL P6DIR P6OUT P6IN	0x0013 0x0037 0x0036 0x0035 0x0034
Port P5	Port P5 resistor enable Port P5 selection Port P5 direction Port P5 output Port P5 input	P5REN P5SEL P5DIR P5OUT P5IN	0x0012 0x0033 0x0032 0x0031 0x0030

[†] 80-pin PN and 113-pin ZQW devices only

PERIPHERAL FILE MAP (CONTINUED)			
Port P4	Port P4 selection	P4SEL	0x001F
	Port P4 resistor enable	P4REN	0x0011
	Port P4 direction	P4DIR	0x001E
	Port P4 output	P4OUT	0x001D
	Port P4 input	P4IN	0x001C
Port P3	Port P3 resistor enable	P3REN	0x0010
	Port P3 selection	P3SEL	0x001B
	Port P3 direction	P3DIR	0x001A
	Port P3 output	P3OUT	0x0019
	Port P3 input	P3IN	0x0018
Port P2	Port P2 resistor enable	P2REN	0x002F
	Port P2 selection	P2SEL	0x002E
	Port P2 interrupt enable	P2IE	0x002D
	Port P2 interrupt-edge select	P2IES	0x002C
	Port P2 interrupt flag	P2IFG	0x002B
	Port P2 direction	P2DIR	0x002A
	Port P2 output	P2OUT	0x0029
	Port P2 input	P2IN	0x0028
Port P1	Port P1 resistor enable	P1REN	0x0027
	Port P1 selection	P1SEL	0x0026
	Port P1 interrupt enable	P1IE	0x0025
	Port P1 interrupt-edge select	P1IES	0x0024
	Port P1 interrupt flag	P1IFG	0x0023
	Port P1 direction	P1DIR	0x0022
	Port P1 output	P1OUT	0x0021
	Port P1 input	P1IN	0x0020
Special Functions	SFR interrupt flag2	IFG2	0x0003
	SFR interrupt flag1	IFG1	0x0002
	SFR interrupt enable2	IE2	0x0001
	SFR interrupt enable1	IE1	0x0000

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absolute maximum ratings (see Note 1)

Voltage applied at V _{CC} to V _{SS}	-0.3 V to 4.1 V
Voltage applied to any pin (see Note 2)	-0.3 V to V _{CC} + 0.3 V
Diode current at any device terminal	±2 mA
Storage temperature: Unprogrammed device (see Note 3)	-55°C to 150°C
Programmed device (see Note 3)	-40°C to 105°C

NOTES: 1. Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2. All voltages referenced to V_{SS}. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TDI/TCLK pin when blowing the JTAG fuse.
3. Higher temperature may be applied during board soldering process according to the current JEDEC J-STD-020 specification, with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

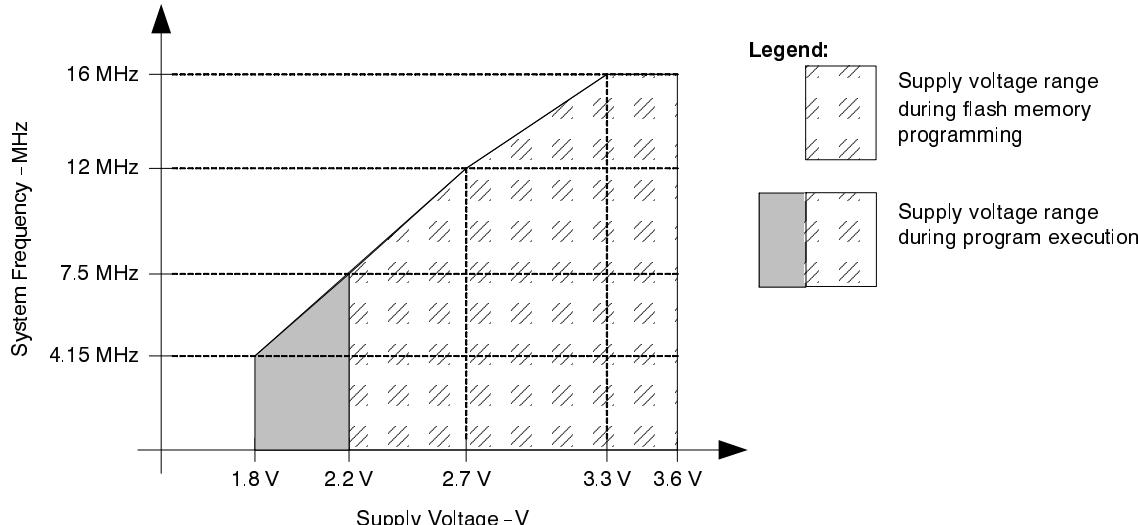
recommended operating conditions

PARAMETER		MIN	MAX	UNIT
Supply voltage during program execution, V _{CC}	A _{VCC} = D _{VCC} = V _{CC} (see Note 1)	1.8	3.6	V
Supply voltage during flash memory programming, V _{CC}	A _{VCC} = D _{VCC} = V _{CC} (see Note 1)	2.2	3.6	V
Supply voltage, V _{SS}	A _{VSS} = D _{VSS} = V _{SS}	0.0	0.0	V
Operating free-air temperature, T _A	I version	-40	85	°C
	T version	-40	105	
Processor frequency f _{SYSYTEM} (maximum MCLK frequency) (see Notes 2 and 3 and Figure 1)	V _{CC} = 1.8 V, Duty cycle = 50% ± 10%	dc	4.15	MHz
	V _{CC} = 2.7 V, Duty cycle = 50% ± 10%	dc	12	
	V _{CC} ≥ 3.3 V, Duty cycle = 50% ± 10%	dc	16	

NOTES: 1. It is recommended to power A_{VCC} and D_{VCC} from the same source. A maximum difference of 0.3 V between A_{VCC} and D_{VCC} can be tolerated during power-up.

2. The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.

3. Modules might have a different maximum input clock specification. See the specification of the respective module in this data sheet.



NOTE: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.2 V.

Figure 1. Operating Area

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

active mode supply current into V_{CC} excluding external current (see Notes 1 and 2)

PARAMETER	TEST CONDITIONS	T _A	V _{CC}	MIN	TYP	MAX	UNIT
I _{AM, 1MHz}	Active mode (AM) current (1 MHz) f _{DCO} = f _{MCLK} = f _{SMCLK} = 1 MHz, f _{ACLK} = 32768 Hz, Program executes from flash, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	-40°C to 85°C	2.2 V		365	395	μA
		105°C			375	420	
		-40°C to 85°C	3 V		515	560	
		105°C			525	595	
I _{AM, 1MHz}	Active mode (AM) current (1 MHz) f _{DCO} = f _{MCLK} = f _{SMCLK} = 1 MHz, f _{ACLK} = 32768 Hz, Program executes in RAM, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	-40°C to 85°C	2.2 V		330	370	μA
		105°C			340	390	
		-40°C to 85°C	3 V		460	495	
		105°C			470	520	
I _{AM, 4kHz}	Active mode (AM) current (4 kHz) f _{MCLK} = f _{SMCLK} = f _{ACLK} = 32768 Hz/8 = 4096 Hz, f _{DCO} = 0 Hz, Program executes in flash, SELMx = 11, SELS = 1, DIVMx = DIVSx = DIVAx = 11, CPUOFF = 0, SCG0 = 1, SCG1 = 0, OSCOFF = 0	-40°C to 85°C	2.2 V		2.1	9	μA
		105°C			15	31	
		-40°C to 85°C	3 V		3	11	
		105°C			19	32	
I _{AM, 100kHz}	Active mode (AM) current (100 kHz) f _{MCLK} = f _{SMCLK} = f _{DCO(0, 0)} ≈ 100 kHz, f _{ACLK} = 0 Hz, Program executes in flash, RSELx = 0, DCOx = 0, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 1	-40°C to 85°C	2.2 V		67	86	μA
		105°C			80	99	
		-40°C to 85°C	3 V		84	107	
		105°C			99	128	

- NOTES: 1. All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current.
 2. The currents are characterized with a micro crystal CC4V-T1ASMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

typical characteristics - active mode supply current (into DV_{CC} + AV_{CC})

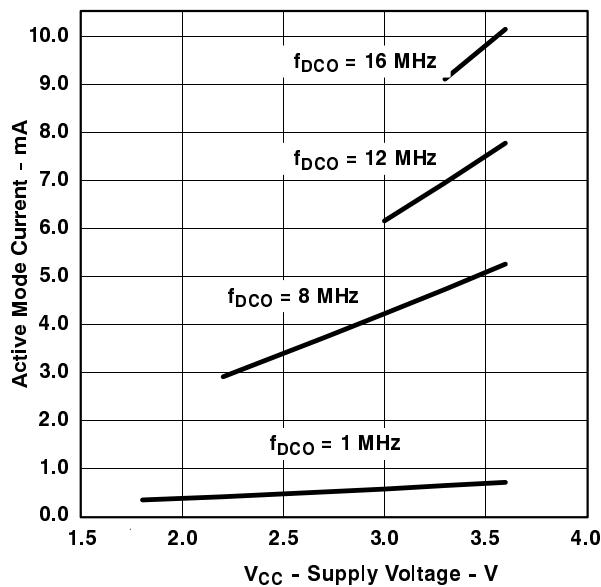


Figure 2. Active Mode Current vs V_{CC}, T_A = 25°C

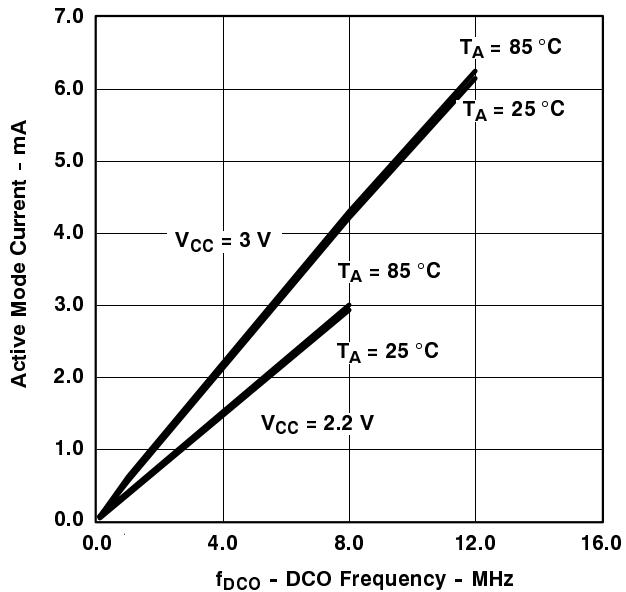


Figure 3. Active Mode Current vs DCO Frequency

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

low-power mode supply current into V_{CC} excluding external current (see Notes 1 and 2)

PARAMETER	TEST CONDITIONS	T _A	V _{CC}	MIN	TYP	MAX	UNIT
I _{LPM0, 1MHz} Low-power mode 0 (LPM0) current, see Note 3	f _{MCLK} = 0 MHz, f _{SMCLK} = f _{DCO} = 1 MHz, f _{ACLK} = 32768 Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0	-40°C to 85°C	2.2 V	68	83	83	μA
		105°C		83	98	98	
		-40°C to 85°C	3 V	87	105	105	
		105°C		100	125	125	
I _{LPM0, 100kHz} Low-power mode 0 (LPM0) current, see Note 3	f _{MCLK} = 0MHz, f _{SMCLK} = f _{DCO(0,0)} ≈ 100 kHz, f _{ACLK} = 0 Hz, RSELX = 0, DCOx = 0, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 1	-40°C to 85°C	2.2 V	37	49	49	μA
		105°C		50	62	62	
		-40°C to 85°C	3 V	40	55	55	
		105°C		57	73	73	
I _{LPM2} Low-power mode 2 (LPM2) current, see Note 4	f _{MCLK} = f _{SMCLK} = 0 MHz, f _{DCO} = 1 MHz, f _{ACLK} = 32768 Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0	-40°C to 85°C	2.2 V	23	33	33	μA
		105°C		35	46	46	
		-40°C to 85°C	3 V	25	36	36	
		105°C		40	55	55	
I _{LPM3,LFXT1} Low-power mode 3 (LPM3) current, see Note 4	f _{DCO} = f _{MCLK} = f _{SMCLK} = 0 MHz, f _{ACLK} = 32768 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	-40°C	2.2 V	0.8	1.2	1.2	μA
		25°C		1	1.3	1.3	
		85°C		4.6	7	7	
		105°C		14	24	24	
		-40°C	3 V	0.9	1.3	1.3	
		25°C		1.1	1.5	1.5	
		85°C		5.5	8	8	
		105°C		17	30	30	
I _{LPM3,VLO} Low-power mode 3 (LPM3) current, see Note 4	f _{DCO} = f _{MCLK} = f _{SMCLK} = 0 MHz, f _{ACLK} from internal LF oscillator (VLO), CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	-40°C	2.2 V	0.4	1.0	1.0	μA
		25°C		0.5	1.0	1.0	
		85°C		4.3	6.5	6.5	
		105°C		14	24	24	
		-40°C	3 V	0.6	1.2	1.2	
		25°C		0.6	1.2	1.2	
		85°C		5	7.5	7.5	
		105°C		16.5	29.5	29.5	

- NOTES:
1. All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current.
 2. The currents are characterized with a micro crystal CC4V-T1ASMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.
 3. Current for Brownout and WDT+ is included. The WDT+ is clocked by SMCLK.
 4. Current for Brownout and WDT+ is included. The WDT+ is clocked by ACLK.

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

low-power mode supply current into V_{CC} excluding external current (see Notes 1 and 2) (continued)

PARAMETER	TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
I_{LPM4} Low-power mode 4 (LPM4) current, see Note 3	$f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$ MHz, $f_{ACLK} = 0$ Hz, $CPUOFF = 1$, $SCG0 = 1$, $SCG1 = 1$, $OSCOFF = 1$	-40°C	2.2 V		0.1	0.5	μA
		25°C			0.1	0.5	
		85°C			4	6	
		105°C			13	23	
I_{LPM4} Low-power mode 4 (LPM4) current, see Note 3	$f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$ MHz, $f_{ACLK} = 0$ Hz, $CPUOFF = 1$, $SCG0 = 1$, $SCG1 = 1$, $OSCOFF = 1$	-40°C	3 V		0.2	0.5	μA
		25°C			0.2	0.5	
		85°C			4.7	7	
		105°C			14	24	

NOTES: 1. All inputs are tied to 0 V or V_{CC} . Outputs do not source or sink any current.

2. The currents are characterized with a micro crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.

3. Current for Brownout included.

typical characteristics - LPM4 current

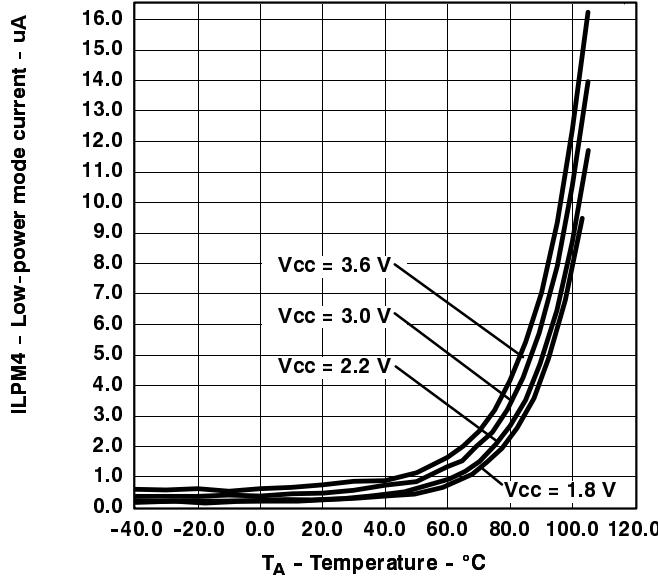


Figure 4. I_{LPM4} - LPM4 Current vs Temperature

Schmitt-trigger inputs - ports P1 through P8, RST/NMI, JTAG, XIN, and XT2IN (see Note 1)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{IT+} Positive-going input threshold voltage			0.45 V _{CC}	0.75 V _{CC}		V
		2.2 V	1.0	1.65		
		3 V	1.35	2.25		
V _{IT-} Negative-going input threshold voltage			0.25 V _{CC}	0.55 V _{CC}		V
		2.2 V	0.55	1.2		
		3 V	0.75	1.65		
V _{hys} Input voltage hysteresis (V _{IT+} - V _{IT-})		2.2 V	0.2	1.0		V
		3 V	0.3	1.0		
R _{Pull} Pullup/pulldown resistor	Pullup: V _{IN} = V _{SS} , Pulldown: V _{IN} = V _{CC}		20	35	50	kΩ
C _i Input capacitance	V _{IN} = V _{SS} or V _{CC}			5		pF

NOTE 1: XIN and XT2IN in bypass mode only.

inputs - ports P1 and P2

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	MAX	UNIT
t _{int} External interrupt timing	Port P1, P2: P1.x to P2.x, external trigger pulse width to set the interrupt flag (see Note 1)	2.2 V/3 V	20		ns

NOTE 1: The external signal sets the interrupt flag every time the minimum t_(int) parameters are met. It may be set with trigger signals shorter than t_(int).

leakage current - ports P1 through P8 (see Note 1 and 2)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	MAX	UNIT
I _{lk} _g (P _{x,x}) High-impedance leakage current	see Notes 1 and 2	2.2 V/3 V	±50		nA

NOTES: 1. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
2. The leakage of digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

standard inputs - \overline{RST}/NMI

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{IL} Low-level input voltage		2.2 V/3 V	V_{SS}	$V_{SS}+0.6$	V
V_{IH} High-level input voltage		2.2 V/3 V	$0.8 \times V_{CC}$	V_{CC}	V

outputs - ports P1 through P8

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH} High-level output voltage	$I_{OH(max)} = -1.5 \text{ mA}$ (see Note 1)	2.2 V	$V_{CC}-0.25$	V_{CC}	V
	$I_{OH(max)} = -6 \text{ mA}$ (see Note 2)		$V_{CC}-0.6$	V_{CC}	
	$I_{OH(max)} = -1.5 \text{ mA}$ (see Note 1)	3 V	$V_{CC}-0.25$	V_{CC}	
	$I_{OH(max)} = -6 \text{ mA}$ (see Note 2)		$V_{CC}-0.6$	V_{CC}	
V_{OL} Low-level output voltage	$I_{OL(max)} = 1.5 \text{ mA}$ (see Note 1)	2.2 V	V_{SS}	$V_{SS}+0.25$	V
	$I_{OL(max)} = 6 \text{ mA}$ (see Note 2)		V_{SS}	$V_{SS}+0.6$	
	$I_{OL(max)} = 1.5 \text{ mA}$ (see Note 1)	3 V	V_{SS}	$V_{SS}+0.25$	
	$I_{OL(max)} = 6 \text{ mA}$ (see Note 2)		V_{SS}	$V_{SS}+0.6$	

- NOTES: 1. The maximum total current, $|I_{OH(max)}$ and $|I_{OL(max)}$, for all outputs combined, should not exceed $\pm 12 \text{ mA}$ to satisfy the maximum voltage drop specified.
 2. The maximum total current, $|I_{OH(max)}$ and $|I_{OL(max)}$, for all outputs combined, should not exceed $\pm 48 \text{ mA}$ to satisfy the maximum voltage drop specified.

output frequency - ports P1 through P8

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{Px,y}$ Port output frequency with load	P1.4/SMCLK, $C_L = 20 \text{ pF}$, $R_L = 1 \text{ k}\Omega$ (see Notes 1 and 2)	2.2 V	DC		10	MHz
		3.0 V	DC		12	
f_{Port_CLK} Clock output frequency	P2.0/ACLK/CA2, P1.4/SMCLK, $C_L = 20 \text{ pF}$ (see Note 2)	2.2 V	DC		12	MHz
		3.3 V	DC		16	
$t_{(Xdc)}$ Duty cycle of output frequency	P5.6/ACLK, $C_L = 20 \text{ pF}$, LF mode		30	50	70	%
	P5.6/ACLK, $C_L = 20 \text{ pF}$, XT1 mode		40	50	60	
	P5.4/MCLK, $C_L = 20 \text{ pF}$, XT1 mode		40		60	%
	P5.4/MCLK, $C_L = 20 \text{ pF}$, DCO	50% - 15 ns	50	50% + 15 ns		
	P1.4/SMCLK, $C_L = 20 \text{ pF}$, XT2 mode		40		60	%
	P1.4/SMCLK, $C_L = 20 \text{ pF}$, DCO	50% - 15 ns		50% + 15 ns		

- NOTES: 1. A resistive divider with 2 times $0.5 \text{ k}\Omega$ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
 2. The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics - outputs

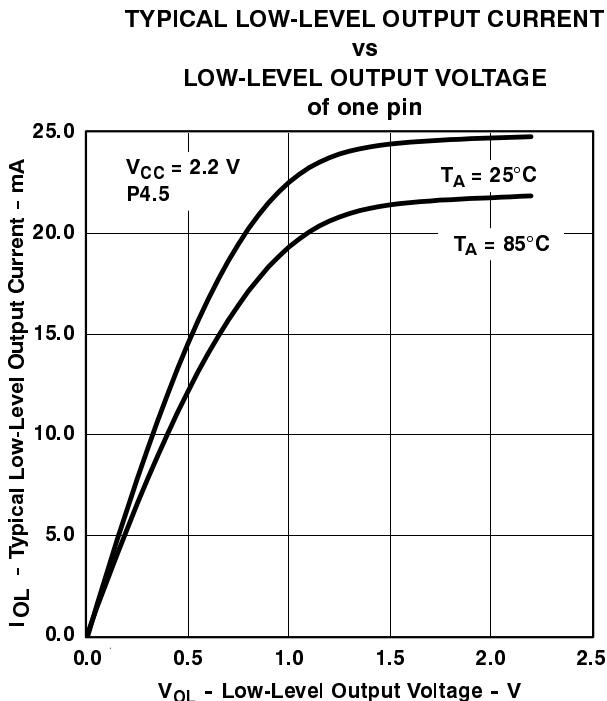


Figure 5

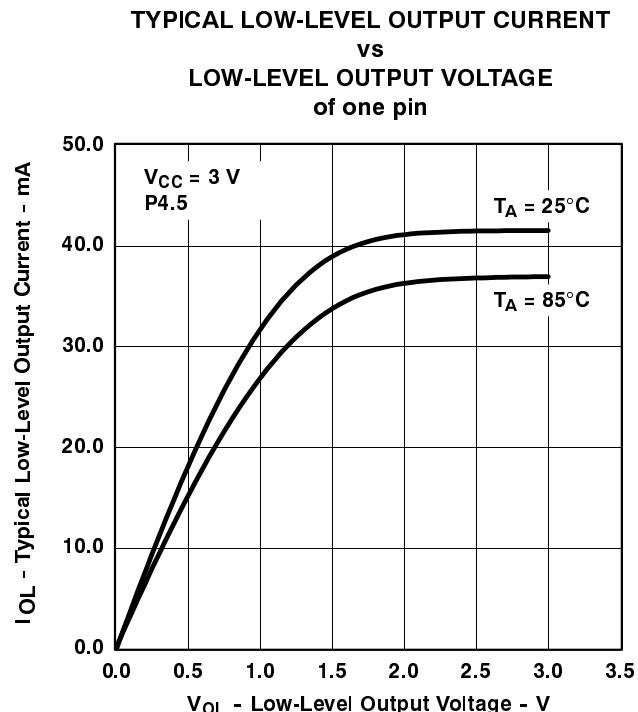


Figure 6

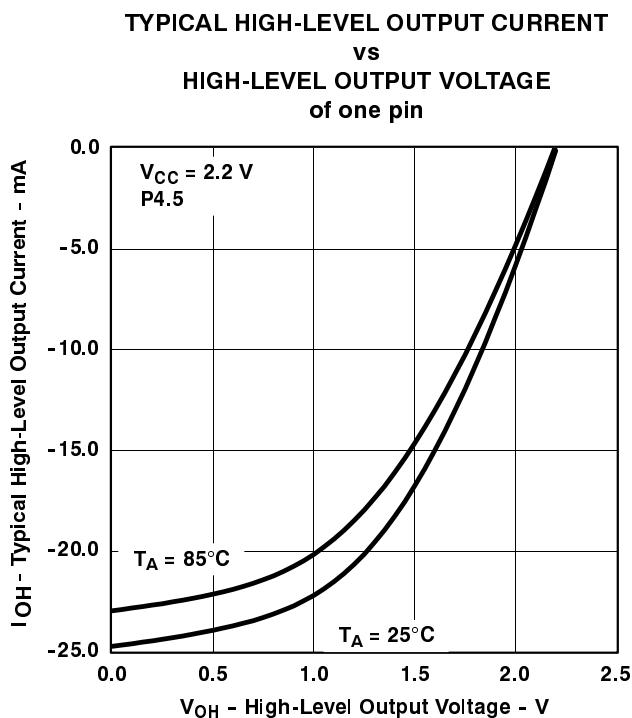


Figure 7

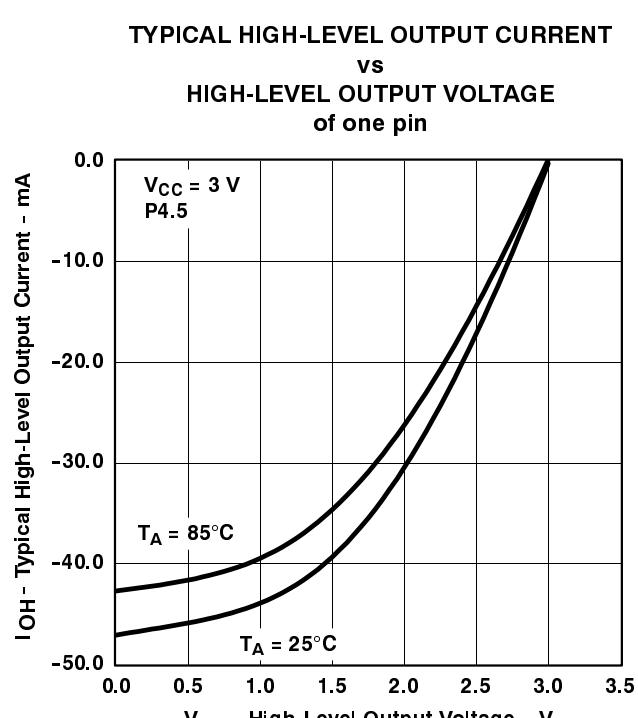


Figure 8

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

POR/brownout reset (BOR) (see Notes 1 and 2)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{CC(start)} Operating voltage	dV _{CC} /dt \leq 3 V/s		0.7 \times V _(B_IT-)			V
V _(B_IT-) Negative going V _{CC} reset threshold voltage	dV _{CC} /dt \leq 3 V/s			1.71		V
V _{hys(B_IT-)} V _{CC} reset threshold hysteresis	dV _{CC} /dt \leq 3 V/s		70	130	210	mV
t _{d(BOR)} BOR reset release delay time					2000	μ s
t _{reset} Pulse length at RST/NMI pin to accept a reset		2.2 V / 3 V	2			μ s

- NOTES: 1. The current consumption of the brownout module is included in the I_{CC} current consumption data. The voltage level V_(B_IT-) + V_{hys(B_IT-)} is \leq 1.8 V.
 2. During power up, the CPU begins code execution following a period of t_{d(BOR)} after V_{CC} = V_(B_IT-) + V_{hys(B_IT-)}. The default DCO settings must not be changed until V_{CC} \geq V_{CC(MIN)}, where V_{CC(min)} is the minimum supply voltage for the desired operating frequency.

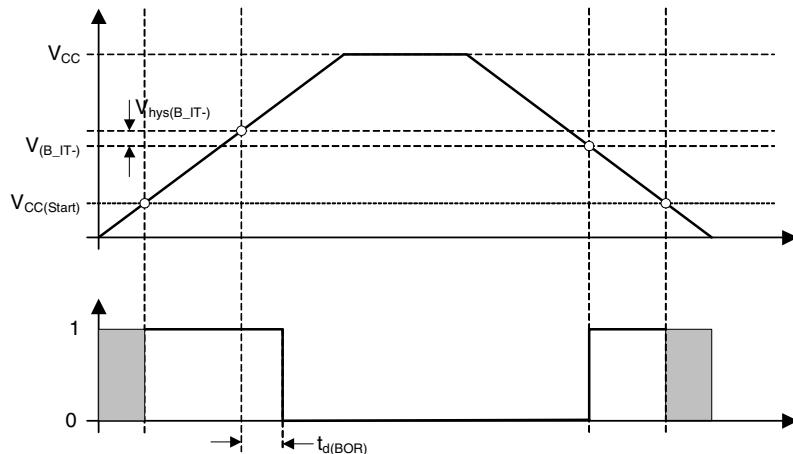


Figure 9. POR/Brownout Reset (BOR) vs Supply Voltage

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics - POR/brownout reset (BOR)

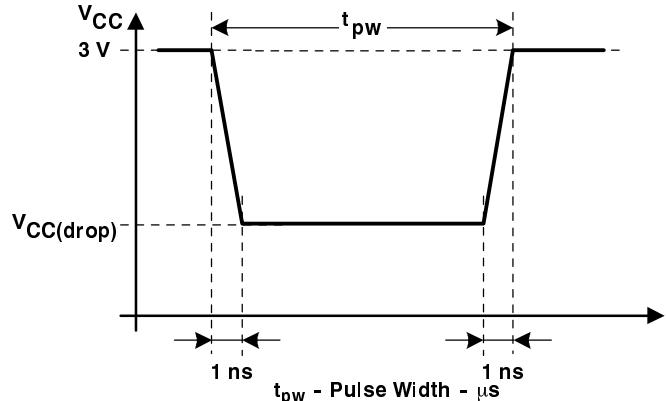
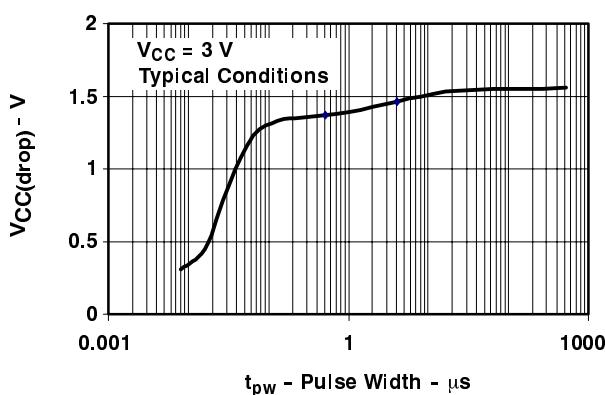


Figure 10. $V_{CC(drop)}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal

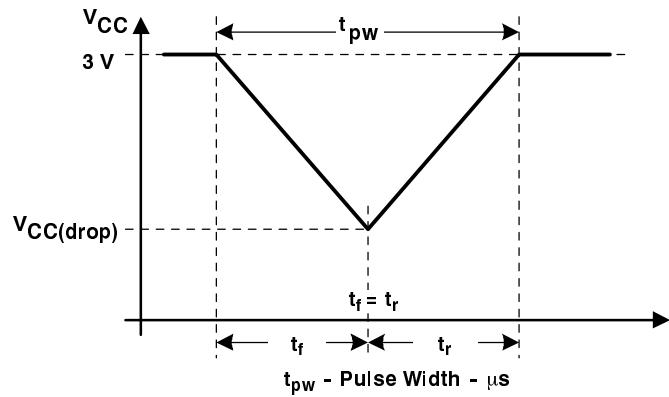
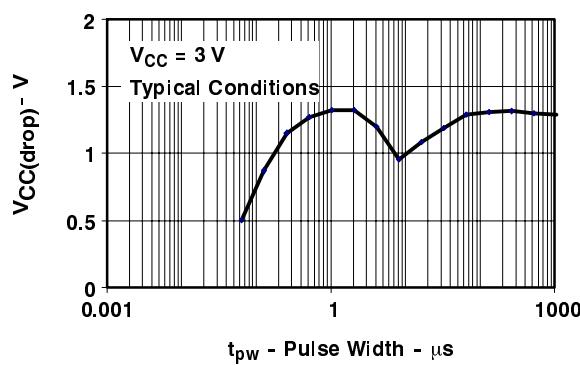


Figure 11. $V_{CC(drop)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

SVS (supply voltage supervisor/monitor)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(SVSR)}$	$dV_{CC}/dt > 30 \text{ V/ms}$ (see Figure 12)	5	150		μs
	$dV_{CC}/dt \leq 30 \text{ V/ms}$		2000		
$t_d(SVS_{on})$	SVSON, switch from VLD = 0 to VLD ≠ 0, $V_{CC} = 3 \text{ V}$	20	150		μs
t_{settle}	$VLD \neq 0^\ddagger$		12		μs
$V_{(SVS_{start})}$	$VLD \neq 0, V_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 12)		1.55	1.7	V
$V_{hys(SVS_IT-)}$	$V_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 12)	VLD = 1	70	120	210
		VLD = 2 to 14	$V_{(SVS_IT-)} \times 0.004$	$V_{(SVS_IT-)} \times 0.016$	V
	$V_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 12), External voltage applied on A7	VLD = 15	4.4	20	mV
$V_{(SVS_IT-)}$	$V_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 12 and Figure 13)	VLD = 1	1.8	1.9	2.05
		VLD = 2	1.94	2.1	2.25
		VLD = 3	2.05	2.2	2.37
		VLD = 4	2.14	2.3	2.48
		VLD = 5	2.24	2.4	2.6
		VLD = 6	2.33	2.5	2.71
		VLD = 7	2.46	2.65	2.86
		VLD = 8	2.58	2.8	3
		VLD = 9	2.69	2.9	3.13
		VLD = 10	2.83	3.05	3.29
		VLD = 11	2.94	3.2	3.42
		VLD = 12	3.11	3.35	3.61 [†]
		VLD = 13	3.24	3.5	3.76 [†]
		VLD = 14	3.43	3.7 [†]	3.99 [†]
	$V_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 12 and Figure 13), External voltage applied on A7	VLD = 15	1.1	1.2	1.3
$I_{CC(SVS)}$ (see Note 1)				10	15
					μA

[†] The recommended operating voltage range is limited to 3.6 V.

[‡] t_{settle} is the settling time that the comparator o/p needs to have a stable level after VLD is switched VLD ≠ 0 to a different VLD value between 2 and 15. The overdrive is assumed to be > 50 mV.

NOTE 1: The current consumption of the SVS module is not included in the I_{CC} current consumption data.

typical characteristics

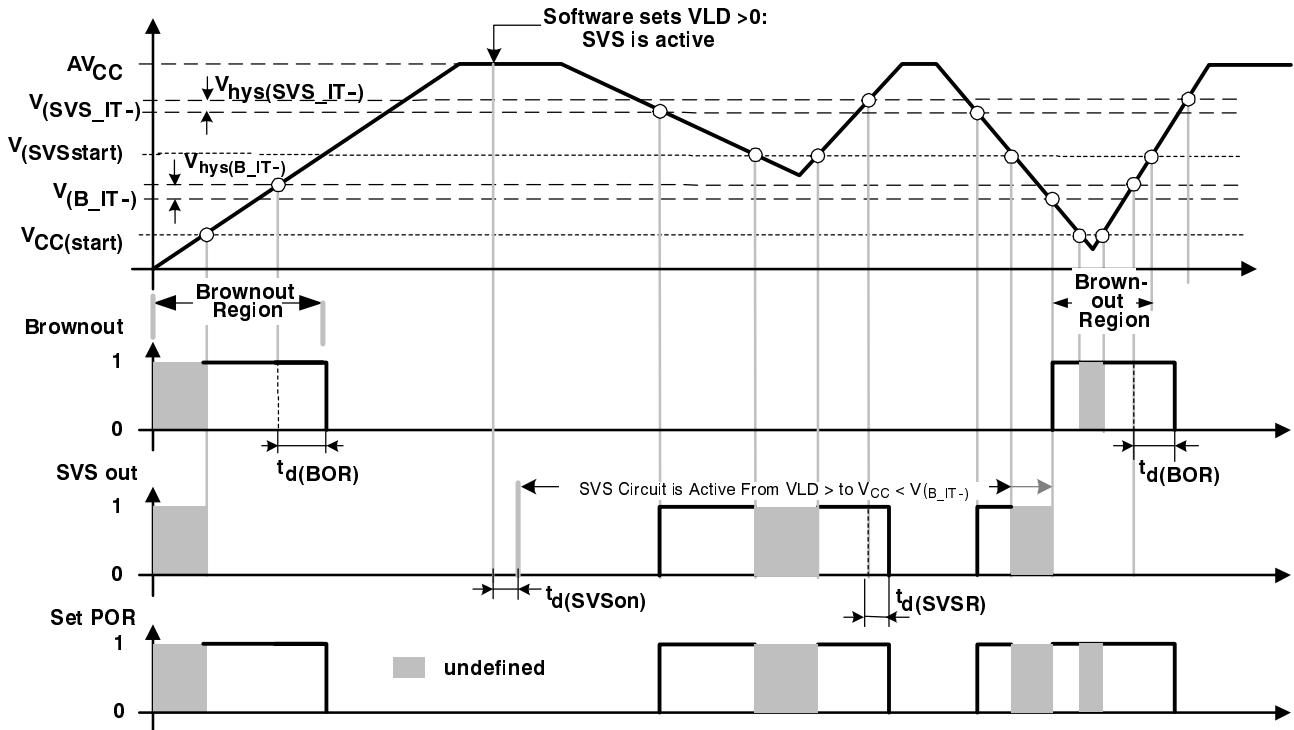


Figure 12. SVS Reset (SVSR) vs Supply Voltage

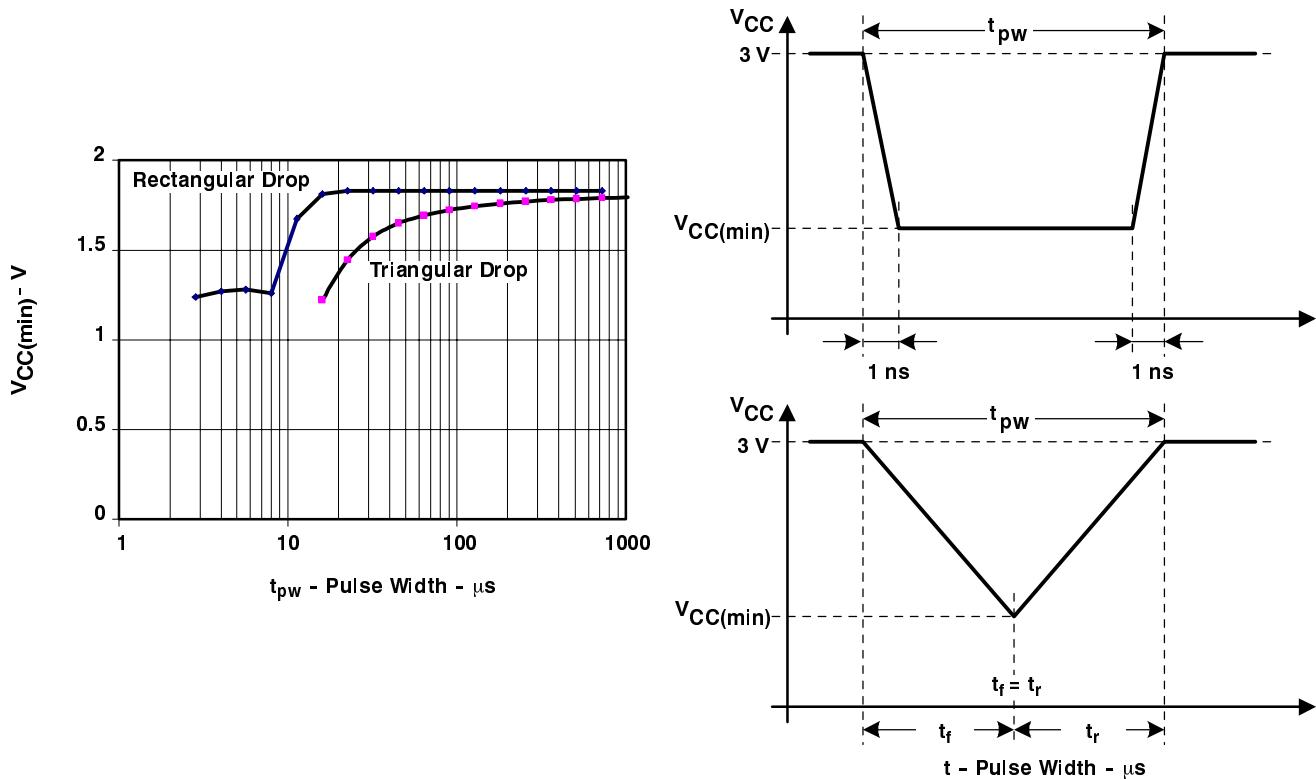


Figure 13. $V_{CC(\min)}$: Square Voltage Drop and Triangle Voltage Drop to Generate an SVS Signal ($VLD = 1$)

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

main DCO characteristics

- All ranges selected by RSELx overlap with RSELx + 1: RSELx = 0 overlaps RSELx = 1, ... RSELx = 14 overlaps RSELx = 15.
- DCO control bits DCOx have a step size as defined by parameter S_{DCO} .
- Modulation control bits MODx select how often $f_{DCO(RSEL,DCO+1)}$ is used within the period of 32 DCOCLK cycles. The frequency $f_{DCO(RSEL,DCO)}$ is used for the remaining cycles. The frequency is an average equal to:

$$f_{\text{average}} = \frac{32 \times f_{DCO(RSEL,DCO)} \times f_{DCO(RSEL,DCO+1)}}{MOD \times f_{DCO(RSEL,DCO)} + (32 - MOD) \times f_{DCO(RSEL,DCO+1)}}$$

DCO frequency

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{CC} Supply voltage	RSELx < 14		1.8	3.6		V
	RSELx = 14		2.2	3.6		
	RSELx = 15		3.0	3.6		
$f_{DCO(0,0)}$	DCO frequency (0, 0)	RSELx = 0, DCOx = 0, MODx = 0	2.2 V/3 V	0.06	0.14	MHz
$f_{DCO(0,3)}$	DCO frequency (0, 3)	RSELx = 0, DCOx = 3, MODx = 0	2.2 V/3 V	0.07	0.17	MHz
$f_{DCO(1,3)}$	DCO frequency (1, 3)	RSELx = 1, DCOx = 3, MODx = 0	2.2 V/3 V	0.10	0.20	MHz
$f_{DCO(2,3)}$	DCO frequency (2, 3)	RSELx = 2, DCOx = 3, MODx = 0	2.2 V/3 V	0.14	0.28	MHz
$f_{DCO(3,3)}$	DCO frequency (3, 3)	RSELx = 3, DCOx = 3, MODx = 0	2.2 V/3 V	0.20	0.40	MHz
$f_{DCO(4,3)}$	DCO frequency (4, 3)	RSELx = 4, DCOx = 3, MODx = 0	2.2 V/3 V	0.28	0.54	MHz
$f_{DCO(5,3)}$	DCO frequency (5, 3)	RSELx = 5, DCOx = 3, MODx = 0	2.2 V/3 V	0.39	0.77	MHz
$f_{DCO(6,3)}$	DCO frequency (6, 3)	RSELx = 6, DCOx = 3, MODx = 0	2.2 V/3 V	0.54	1.06	MHz
$f_{DCO(7,3)}$	DCO frequency (7, 3)	RSELx = 7, DCOx = 3, MODx = 0	2.2 V/3 V	0.80	1.50	MHz
$f_{DCO(8,3)}$	DCO frequency (8, 3)	RSELx = 8, DCOx = 3, MODx = 0	2.2 V/3 V	1.10	2.10	MHz
$f_{DCO(9,3)}$	DCO frequency (9, 3)	RSELx = 9, DCOx = 3, MODx = 0	2.2 V/3 V	1.60	3.00	MHz
$f_{DCO(10,3)}$	DCO frequency (10, 3)	RSELx = 10, DCOx = 3, MODx = 0	2.2 V/3 V	2.50	4.30	MHz
$f_{DCO(11,3)}$	DCO frequency (11, 3)	RSELx = 11, DCOx = 3, MODx = 0	2.2 V/3 V	3.00	5.50	MHz
$f_{DCO(12,3)}$	DCO frequency (12, 3)	RSELx = 12, DCOx = 3, MODx = 0	2.2 V/3 V	4.30	7.30	MHz
$f_{DCO(13,3)}$	DCO frequency (13, 3)	RSELx = 13, DCOx = 3, MODx = 0	2.2 V/3 V	6.00	9.60	MHz
$f_{DCO(14,3)}$	DCO frequency (14, 3)	RSELx = 14, DCOx = 3, MODx = 0	2.2 V/3 V	8.60	13.9	MHz
$f_{DCO(15,3)}$	DCO frequency (15, 3)	RSELx = 15, DCOx = 3, MODx = 0	3 V	12.0	18.5	MHz
$f_{DCO(15,7)}$	DCO frequency (15, 7)	RSELx = 15, DCOx = 7, MODx = 0	3 V	16.0	26.0	MHz
S_{RSEL}	Frequency step between range RSEL and RSEL+1	$S_{RSEL} = f_{DCO(RSEL+1,DCO)} / f_{DCO(RSEL,DCO)}$	2.2 V/3 V		1.55	ratio
S_{DCO}	Frequency step between tap DCO and DCO+1	$S_{DCO} = f_{DCO(RSEL,DCO+1)} / f_{DCO(RSEL,DCO)}$	2.2 V/3 V	1.05	1.08	1.12
Duty cycle	Measured at P1.4/SMCLK	2.2 V/3 V	40	50	60	%

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

calibrated DCO frequencies - tolerance at calibration

PARAMETER	TEST CONDITIONS	T _A	V _{CC}	MIN	TYP	MAX	UNIT
Frequency tolerance at calibration		25°C	3 V	-1	±0.2	+1	%
f _{CAL(1MHz)} 1-MHz calibration value	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	25°C	3 V	0.990	1	1.010	MHz
f _{CAL(8MHz)} 8-MHz calibration value	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	25°C	3 V	7.920	8	8.080	MHz
f _{CAL(12MHz)} 12-MHz calibration value	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	25°C	3 V	11.88	12	12.12	MHz
f _{CAL(16MHz)} 16-MHz calibration value	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	25°C	3 V	15.84	16	16.16	MHz

calibrated DCO frequencies - tolerance over temperature 0°C to 85°C

PARAMETER	TEST CONDITIONS	T _A	V _{CC}	MIN	TYP	MAX	UNIT
1-MHz tolerance over temperature		0°C to 85°C	3 V	-2.5	±0.5	+2.5	%
8-MHz tolerance over temperature		0°C to 85°C	3 V	-2.5	±1.0	+2.5	%
12-MHz tolerance over temperature		0°C to 85°C	3 V	-2.5	±1.0	+2.5	%
16-MHz tolerance over temperature		0°C to 85°C	3 V	-3.0	±2.0	+3.0	%
f _{CAL(1MHz)} 1-MHz calibration value	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	0°C to 85°C	2.2 V	0.970	1	1.030	MHz
			3 V	0.975	1	1.025	
			3.6 V	0.970	1	1.030	
f _{CAL(8MHz)} 8-MHz calibration value	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	0°C to 85°C	2.2 V	7.760	8	8.400	MHz
			3 V	7.800	8	8.200	
			3.6 V	7.600	8	8.240	
f _{CAL(12MHz)} 12-MHz calibration value	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	0°C to 85°C	2.2 V	11.64	12	12.36	MHz
			3 V	11.64	12	12.36	
			3.6 V	11.64	12	12.36	
f _{CAL(16MHz)} 16-MHz calibration value	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	0°C to 85°C	3 V	15.52	16	16.48	MHz
			3.6 V	15.00	16	16.48	

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

calibrated DCO frequencies - tolerance over supply voltage V_{CC}

PARAMETER	TEST CONDITIONS	T _A	V _{CC}	MIN	TYP	MAX	UNIT
1-MHz tolerance over V _{CC}		25°C	1.8 V to 3.6 V	-3	±2	+3	%
8-MHz tolerance over V _{CC}		25°C	1.8 V to 3.6 V	-3	±2	+3	%
12-MHz tolerance over V _{CC}		25°C	2.2 V to 3.6 V	-3	±2	+3	%
16-MHz tolerance over V _{CC}		25°C	3.0 V to 3.6 V	-6	±2	+3	%
f _{CAL(1MHz)} 1-MHz calibration value	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	25°C	1.8 V to 3.6 V	0.970	1	1.030	MHz
f _{CAL(8MHz)} 8-MHz calibration value	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	25°C	1.8 V to 3.6 V	7.760	8	8.240	MHz
f _{CAL(12MHz)} 12-MHz calibration value	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	25°C	2.2 V to 3.6 V	11.64	12	12.36	MHz
f _{CAL(16MHz)} 16-MHz calibration value	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	25°C	3.0 V to 3.6 V	15.00	16	16.48	MHz

calibrated DCO frequencies - overall tolerance

PARAMETER	TEST CONDITIONS	T _A	V _{CC}	MIN	TYP	MAX	UNIT
1-MHz tolerance overall		-40°C to 105°C	1.8 V to 3.6 V	-5	±2	+5	%
8-MHz tolerance overall		-40°C to 105°C	1.8 V to 3.6 V	-5	±2	+5	%
12-MHz tolerance overall		-40°C to 105°C	2.2 V to 3.6 V	-5	±2	+5	%
16-MHz tolerance overall		-40°C to 105°C	3 V to 3.6 V	-6	±3	+6	%
f _{CAL(1MHz)} 1-MHz calibration value	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	-40°C to 105°C	1.8 V to 3.6 V	0.950	1	1.050	MHz
f _{CAL(8MHz)} 8-MHz calibration value	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	-40°C to 105°C	1.8 V to 3.6 V	7.600	8	8.400	MHz
f _{CAL(12MHz)} 12-MHz calibration value	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	-40°C to 105°C	2.2 V to 3.6 V	11.40	12	12.60	MHz
f _{CAL(16MHz)} 16-MHz calibration value	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	-40°C to 105°C	3 V to 3.6 V	15.00	16	17.00	MHz

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics - calibrated 1-MHz DCO frequency

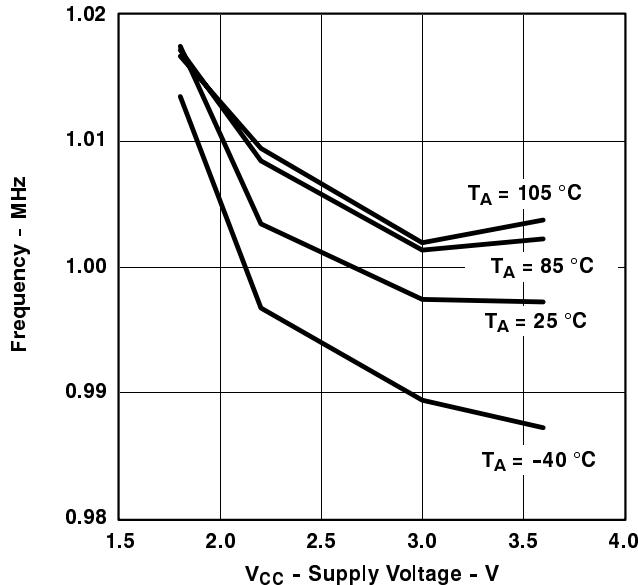


Figure 14. Calibrated 1-MHz Frequency vs V_{CC}

typical characteristics - calibrated 8-MHz DCO frequency

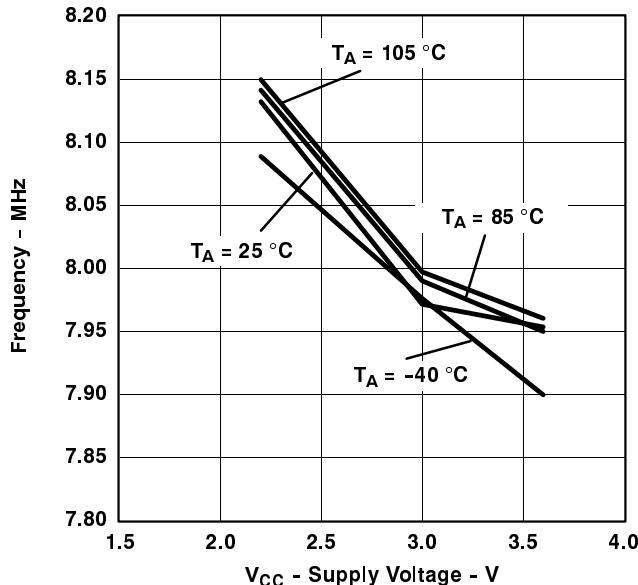


Figure 15. Calibrated 8-MHz Frequency vs V_{CC}

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics - calibrated 12-MHz DCO frequency

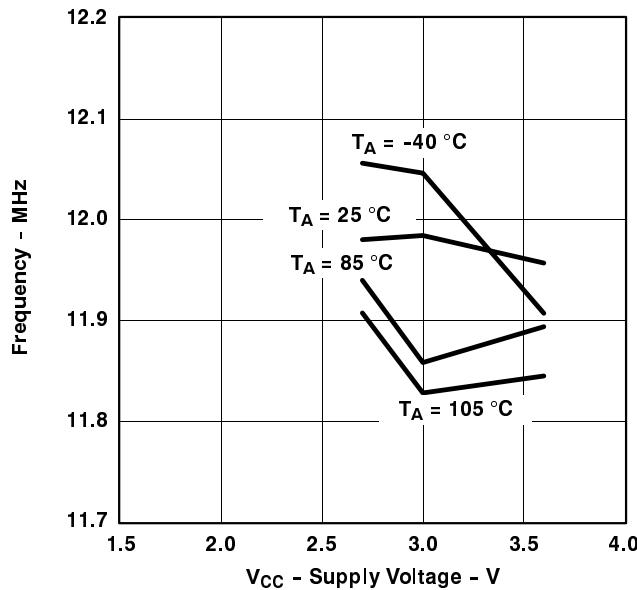


Figure 16. Calibrated 12-MHz Frequency vs V_{CC}

typical characteristics - calibrated 16-MHz DCO frequency

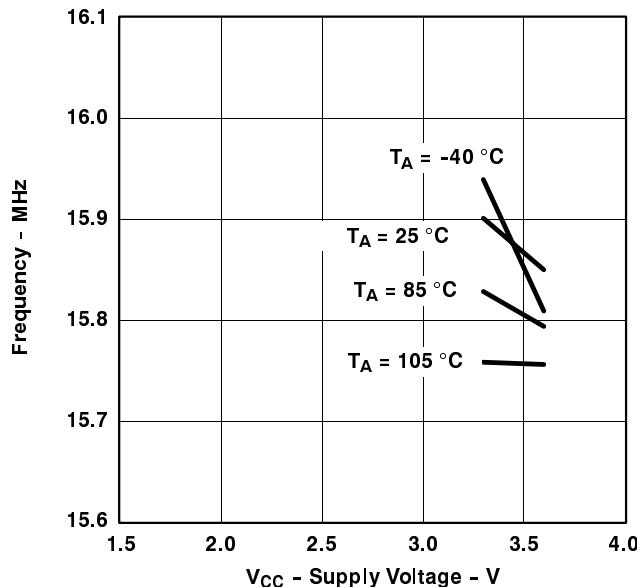


Figure 17. Calibrated 16-MHz Frequency vs V_{CC}

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

wake-up from low-power modes (LPM3/LPM4)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
t _{DCO,LPM3/4} DCO clock wake-up time from LPM3/4 (see Note 1)	BCSCTL1= CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ	2.2 V/3 V		2		μs
	BCSCTL1= CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ	2.2 V/3 V		1.5		
	BCSCTL1= CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ	2.2 V/3 V		1		
	BCSCTL1= CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ	3 V		1		
t _{CPU,LPM3/4} CPU wake-up time from LPM3/4 (see Note 2)				1/f _{MCLK} + t _{Clock,LPM3/4}		

NOTES: 1. The DCO clock wake-up time is measured from the edge of an external wake-up signal (e.g., port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).
 2. Parameter applicable only if DCOCLK is used for MCLK.

typical characteristics - DCO clock wake-up time from LPM3/4

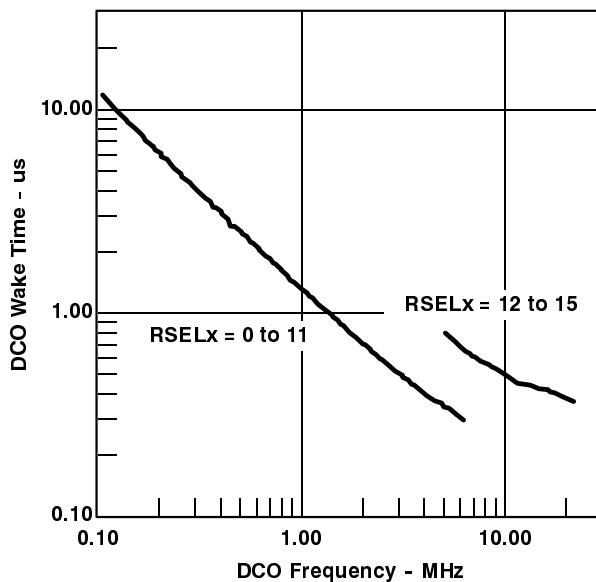


Figure 18. Clock Wake-Up Time From LPM3 vs DCO Frequency

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

DCO with external resistor R_{OSC} (see Note 1)

PARAMETER	TEST CONDITIONS	V _{CC}	TYP	UNIT
$f_{DCO,ROSC}$	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0, $T_A = 25^\circ C$	2.2 V	1.8	MHz
		3 V	1.95	
D_t	Temperature drift	2.2 V/3 V	± 0.1	%/ $^\circ C$
D_V	Drift with V_{CC}	2.2 V/3 V	10	%/V

NOTE 1: $R_{OSC} = 100 \text{ k}\Omega$. Metal film resistor, type 0257. 0.6 watt with 1% tolerance and $T_K = \pm 50 \text{ ppm}/^\circ C$.

typical characteristics - DCO with external resistor R_{OSC}

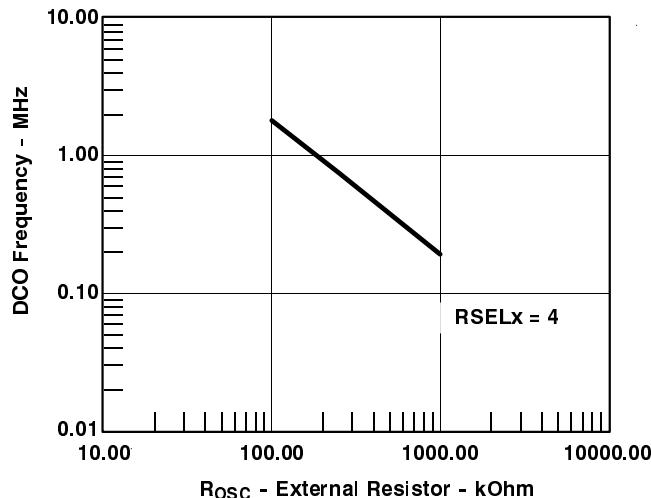


Figure 19. DCO Frequency vs R_{OSC} ,
 $V_{CC} = 2.2 \text{ V}$, $T_A = 25^\circ C$

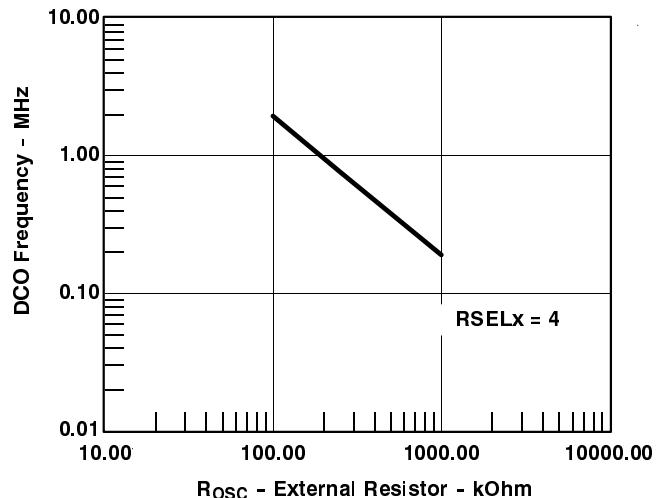


Figure 20. DCO Frequency vs R_{OSC} ,
 $V_{CC} = 3.0 \text{ V}$, $T_A = 25^\circ C$

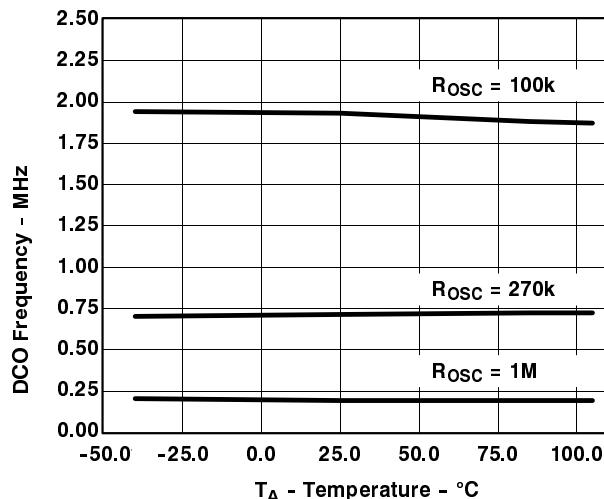


Figure 21. DCO Frequency vs Temperature,
 $V_{CC} = 3.0 \text{ V}$

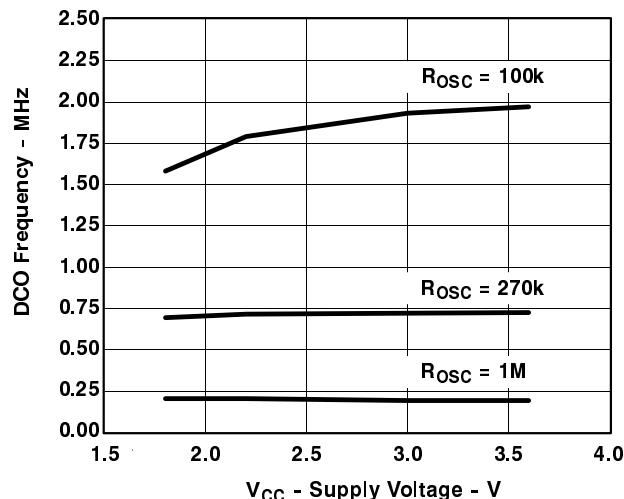


Figure 22. DCO Frequency vs V_{CC} ,
 $T_A = 25^\circ C$

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

crystal oscillator, LFXT1, low frequency modes (see Note 4)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT	
f _{LFXT1,LF}	LFXT1 oscillator crystal frequency, LF mode 0/1	XTS = 0, LFXT1Sx = 0 or 1	1.8 V to 3.6 V		32768	Hz	
f _{LFXT1,LF,logic}	LFXT1 oscillator logic level square wave input frequency, LF mode	XTS = 0, LFXT1Sx = 3, XCAPx = 0	1.8 V to 3.6 V	10000	32768	50000	Hz
OA _{LF}	Oscillation allowance for LF crystals	XTS = 0, LFXT1Sx = 0, f _{LFXT1,LF} = 32768 kHz, C _{L,eff} = 6 pF		500	200	kΩ	
		XTS = 0, LFXT1Sx = 0; f _{LFXT1,LF} = 32768 kHz, C _{L,eff} = 12 pF					
C _{L,eff}	Integrated effective load capacitance, LF mode (see Note 1)	XTS = 0, XCAPx = 0		1	5.5	pF	
		XTS = 0, XCAPx = 1					
		XTS = 0, XCAPx = 2					
		XTS = 0, XCAPx = 3					
Duty cycle	LF mode	XTS = 0, Measured at P1.4/ACLK, f _{LFXT1,LF} = 32768 Hz	2.2 V/3 V	30	50	70	%
f _{Fault,LF}	Oscillator fault frequency, LF mode (see Note 3)	XTS = 0, LFXT1Sx = 3, XCAPx = 0 (see Note 2)	2.2 V/3 V	10	10000	Hz	

NOTES: 1. Includes parasitic bond and package capacitance (approximately 2 pF per pin).

Since the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.

2. Measured with logic level input frequency but also applies to operation with crystals.
3. Frequencies below the MIN specification set the fault flag, frequencies above the MAX specification do not set the fault flag, and frequencies in between might set the flag.
4. To improve EMI on the LFXT1 oscillator the following guidelines should be observed.
 - Keep the trace between the device and the crystal as short as possible.
 - Design a good ground plane around the oscillator pins.
 - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
 - Avoid running PCB traces under or adjacent to the XIN and XOUT pins.
 - Use assembly materials and practices to avoid any parasitic load on the oscillator XIN and XOUT pins.
 - If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
 - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.
5. Applies only if using an external logic-level clock source. Not applicable when using a crystal or resonator.

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

internal very low power, low frequency oscillator (VLO)

PARAMETER	TEST CONDITIONS	T _A	V _{CC}	MIN	TYP	MAX	UNIT
f _{VLO}	VLO frequency	-40°C to 85°C	2.2 V/3 V	4	12	20	kHz
		105°C				22	
d _{f_{VLO}} /dT	VLO frequency temperature drift	See Note 1	2.2 V/3 V		0.5		%/°C
d _{f_{VLO}} /dV _{CC}	VLO frequency supply voltage drift	See Note 2	25°C	1.8V – 3.6V		4	%/V

NOTES:

- Calculated using the box method:
I version: $(\text{MAX}(-40^\circ\text{C} \text{ to } 85^\circ\text{C}) - \text{MIN}(-40^\circ\text{C} \text{ to } 85^\circ\text{C})) / \text{MIN}(-40^\circ\text{C} \text{ to } 85^\circ\text{C}) / (85^\circ\text{C} - (-40^\circ\text{C}))$
T version: $(\text{MAX}(-40^\circ\text{C} \text{ to } 105^\circ\text{C}) - \text{MIN}(-40^\circ\text{C} \text{ to } 105^\circ\text{C})) / \text{MIN}(-40^\circ\text{C} \text{ to } 105^\circ\text{C}) / (105^\circ\text{C} - (-40^\circ\text{C}))$
- Calculated using the box method: $(\text{MAX}(1.8 \text{ V} \text{ to } 3.6\text{V}) - \text{MIN}(1.8 \text{ V} \text{ to } 3.6\text{V})) / \text{MIN}(1.8 \text{ V} \text{ to } 3.6\text{V}) / (3.6 \text{ V} - 1.8 \text{ V})$

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

crystal oscillator, LFXT1, high frequency modes (see Note 5)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{LFXT1,HF0}	LFXT1 oscillator crystal frequency, HF mode 0	XTS = 1, LFXT1Sx = 0, XCAPx = 0	1.8 V to 3.6 V	0.4	1	MHz
f _{LFXT1,HF1}	LFXT1 oscillator crystal frequency, HF mode 1	XTS = 1, LFXT1Sx = 1, XCAPx = 0	1.8 V to 3.6 V	1	4	MHz
f _{LFXT1,HF2}	LFXT1 oscillator crystal frequency, HF mode 2	XTS = 1, LFXT1Sx = 2, XCAPx = 0	1.8 V to 3.6 V	2	10	MHz
			2.2 V to 3.6 V	2	12	
			3 V to 3.6 V	2	16	
f _{LFXT1,HF,logic}	LFXT1 oscillator logic level square-wave input frequency, HF mode	XTS = 1, LFXT1Sx = 3, XCAPx = 0	1.8 V to 3.6 V	0.4	10	MHz
			2.2 V to 3.6 V	0.4	12	
			3 V to 3.6 V	0.4	16	
OA _{HF}	Oscillation allowance for HF crystals (see Figure 23 and Figure 24)	XTS = 1, XCAPx = 0, LFXT1Sx = 0, f _{LFXT1,HF} = 1 MHz, C _{L,eff} = 15 pF		2700	800	Ω
		XTS = 1, XCAPx = 0, LFXT1Sx = 1, f _{LFXT1,HF} = 4 MHz, C _{L,eff} = 15 pF				
		XTS = 1, XCAPx = 0, LFXT1Sx = 2, f _{LFXT1,HF} = 16 MHz, C _{L,eff} = 15 pF				
C _{L,eff}	Integrated effective load capacitance, HF mode (see Note 1)	XTS = 1, XCAPx = 0 (see Note 2)			1	pF
Duty cycle	HF mode	XTS = 1, XCAPx = 0, Measured at P1.4/ACLK, f _{LFXT1,HF} = 10 MHz	2.2 V/3 V	40	50	60
		XTS = 1, XCAPx = 0, Measured at P1.4/ACLK, f _{LFXT1,HF} = 16 MHz	2.2 V/3 V	40	50	60
f _{Fault,HF}	Oscillator fault frequency, HF mode (see Note 4)	XTS = 1, LFXT1Sx = 3, XCAPx = 0 (see Note 3)	2.2 V/3 V	30	300	kHz

- NOTES:
- Includes parasitic bond and package capacitance (approximately 2 pF per pin). Since the PCB adds additional capacitance it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup the effective load capacitance should always match the specification of the used crystal.
 - Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
 - Measured with logic level input frequency but also applies to operation with crystals.
 - Frequencies below the MIN specification set the fault flag, frequencies above the MAX specification do not set the fault flag, and frequencies in between might set the flag.
 - To improve EMI on the LFXT1 oscillator the following guidelines should be observed.
 - Keep the trace between the device and the crystal as short as possible.
 - Design a good ground plane around the oscillator pins.
 - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
 - Avoid running PCB traces under or adjacent to the XIN and XOUT pins.
 - Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
 - If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
 - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics - LFXT1 oscillator in HF mode (XTS = 1)

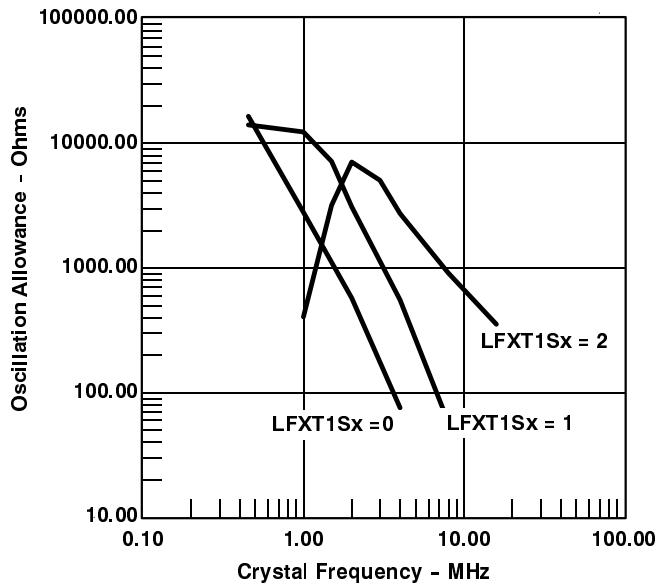


Figure 23. Oscillation Allowance vs Crystal Frequency, $C_{L,\text{eff}} = 15 \text{ pF}$, $T_A = 25^\circ\text{C}$

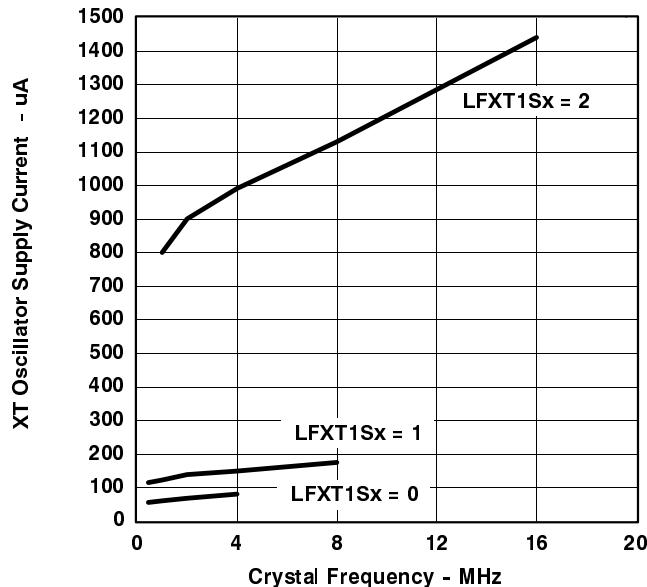


Figure 24. XT Oscillator Supply Current vs Crystal Frequency, $C_{L,\text{eff}} = 15 \text{ pF}$, $T_A = 25^\circ\text{C}$

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

crystal oscillator, XT2 (see Note 5)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{XT2}	XT2 oscillator crystal frequency, mode 0	XT2Sx = 0	1.8 V to 3.6 V	0.4	1	MHz
f _{XT2}	XT2 oscillator crystal frequency, mode 1	XT2Sx = 1	1.8 V to 3.6 V	1	4	MHz
f _{XT2}	XT2 oscillator crystal frequency, mode 2	XT2Sx = 2	1.8 V to 3.6 V	2	10	MHz
			2.2 V to 3.6 V	2	12	
			3 V to 3.6 V	2	16	
f _{XT2}	XT2 oscillator logic level square-wave input frequency	XT2Sx = 3	1.8 V to 3.6 V	0.4	10	MHz
			2.2 V to 3.6 V	0.4	12	
			3 V to 3.6 V	0.4	16	
OA	Oscillation allowance (see Figure 23 and Figure 24)	XT2Sx = 0, f _{XT2} = 1 MHz, C _{L,eff} = 15 pF			2700	Ω
					800	
					300	
C _{L,eff}	Integrated effective load capacitance, HF mode (see Note 1)	See Note 2			1	pF
Duty cycle		Measured at P1.4/SMCLK, f _{XT2} = 10 MHz	2.2 V/3 V	40	50	60
		Measured at P1.4/SMCLK, f _{XT2} = 16 MHz		40	50	60
f _{Fault}	Oscillator fault frequency, HF mode (see Note 4)	XT2Sx = 3, (see Note 3)	2.2 V/3 V	30	300	kHz

NOTES: 1. Includes parasitic bond and package capacitance (approximately 2 pF per pin).

Since the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.

2. Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
3. Measured with logic level input frequency but also applies to operation with crystals.
4. Frequencies below the MIN specification set the fault flag, frequencies above the MAX specification do not set the fault flag, and frequencies in between might set the flag.
5. To improve EMI on the LFXT1 oscillator the following guidelines should be observed.
 - Keep the trace between the device and the crystal as short as possible.
 - Design a good ground plane around the oscillator pins.
 - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
 - Avoid running PCB traces under or adjacent to the XIN and XOUT pins.
 - Use assembly materials and practices to avoid any parasitic load on the oscillator XIN and XOUT pins.
 - If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
 - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics - XT2 oscillator

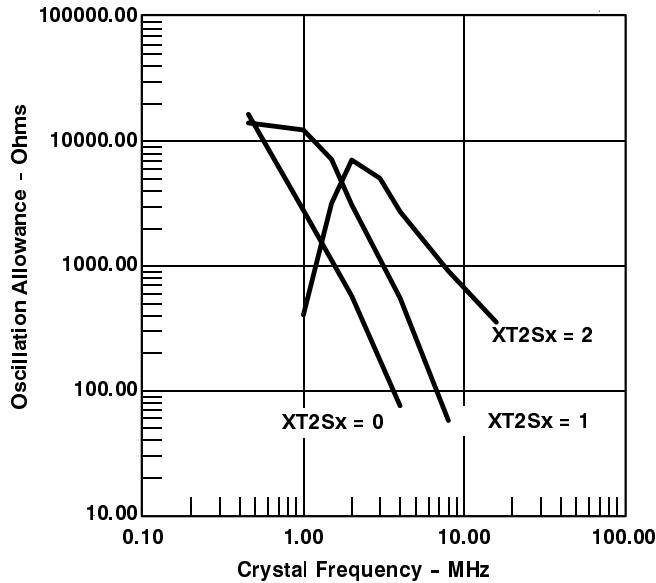


Figure 25. Oscillation Allowance vs Crystal Frequency, $C_{L,\text{eff}} = 15 \text{ pF}$, $T_A = 25^\circ\text{C}$

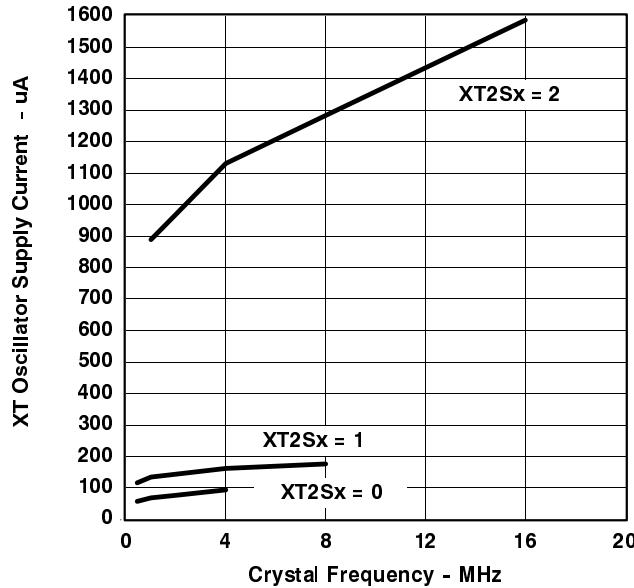


Figure 26. XT2 Oscillator Supply Current vs Crystal Frequency, $C_{L,\text{eff}} = 15 \text{ pF}$, $T_A = 25^\circ\text{C}$

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

Timer_A

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	MAX	UNIT
f _{TA} Timer_A clock frequency	Internal: SMCLK, ACLK, External: TACLK, INCLK, Duty cycle = 50% ±10%	2.2 V		10	MHz
		3.3 V		16	
t _{TA,cap} Timer_A, capture timing	TA0, TA1, TA2	2.2 V/3 V	20		ns

Timer_B

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	MAX	UNIT
f _{TB} Timer_B clock frequency	Internal: SMCLK, ACLK, External: TBCLK, Duty cycle = 50% ±10%	2.2 V		10	MHz
		3.3 V		16	
t _{TB,cap} Timer_B, capture timing	TB0, TB1, TB2	2.2 V/3 V	20		ns

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

USCI (UART mode)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{USCI}	USCI input clock frequency Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10%				f _{SYSTEM}	MHz
f _{BITCLK}	BITCLK clock frequency (equals baud rate in MBaud)	2.2 V / 3 V			1	MHz
t _r	UART receive deglitch time (see Note 1)		2.2 V	50	150	600
			3 V	50	100	600
					ns	

NOTE 1: Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized their width should exceed the maximum specification of the deglitch time.

USCI (SPI master mode) (see Figure 27 and Figure 28)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	MAX	UNIT
f _{USCI}	USCI input clock frequency SMCLK, ACLK Duty cycle = 50% ± 10%			f _{SYSTEM}	MHz
t _{SU,MI}	SOMI input data setup time		2.2 V	110	ns
			3 V	75	
t _{HD,MI}	SOMI input data hold time		2.2 V	0	ns
			3 V	0	
t _{VALID,MO}	SIMO output data valid time UCLK edge to SIMO valid; C _L = 20 pF		2.2 V	30	ns
			3 V	20	

NOTE 1: f_{UCxCLK} = $\frac{1}{2t_{LO/HI}}$ with t_{LO/HI} ≥ max(t_{VALID,MO(USCI)} + t_{SU,SI(Slave)}, t_{SU,MI(USCI)} + t_{VALID,SO(Slave)}).

For the slave parameters t_{SU,SI(Slave)} and t_{VALID,SO(Slave)}, see the SPI parameters of the attached slave.

USCI (SPI slave mode) (see Figure 29 and Figure 30)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
t _{STE,LEAD}	STE lead time, STE low to clock	2.2 V/3 V		50		ns
t _{STE,LAG}	STE lag time, Last clock to STE high	2.2 V/3 V		10		ns
t _{STE,ACC}	STE access time, STE low to SOMI data out	2.2 V/3 V		50		ns
t _{STE,DIS}	STE disable time, STE high to SOMI high impedance	2.2 V/3 V		50		ns
t _{SU,SI}	SIMO input data setup time		2.2 V	20	ns	
			3 V	15		
t _{HD,SI}	SIMO input data hold time		2.2 V	10	ns	
			3 V	10		
t _{VALID,SO}	SOMI output data valid time UCLK edge to SOMI valid; C _L = 20 pF		2.2 V	75	110	ns
			3 V	50	75	

NOTE 1: f_{UCxCLK} = $\frac{1}{2t_{LO/HI}}$ with t_{LO/HI} ≥ max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)})

For the master parameters t_{SU,MI(Master)} and t_{VALID,MO(Master)}, see the SPI parameters of the attached master.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

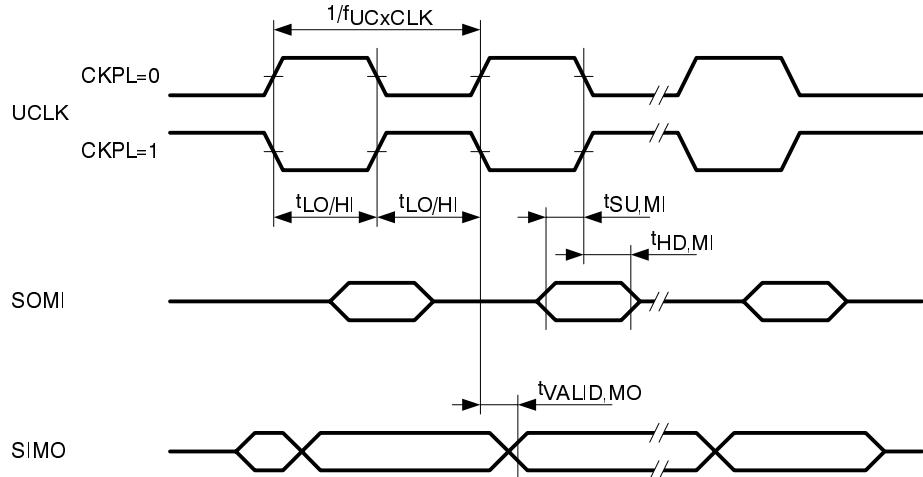


Figure 27. SPI Master Mode, $\text{CKPH} = 0$

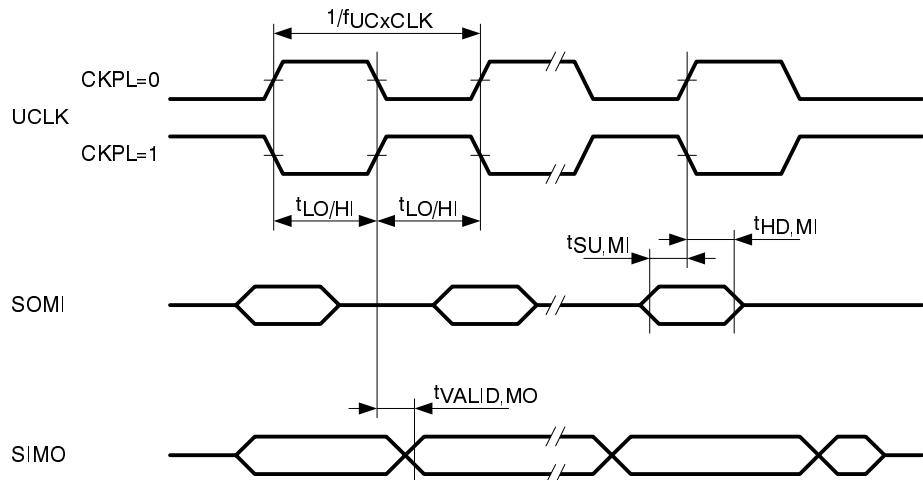


Figure 28. SPI Master Mode, $\text{CKPH} = 1$

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

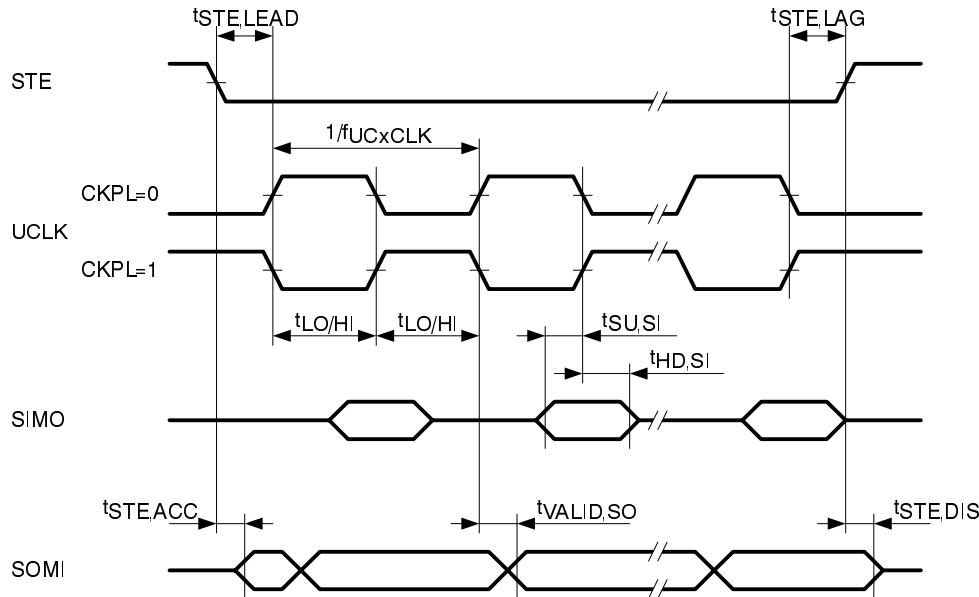


Figure 29. SPI Slave Mode, CKPH = 0

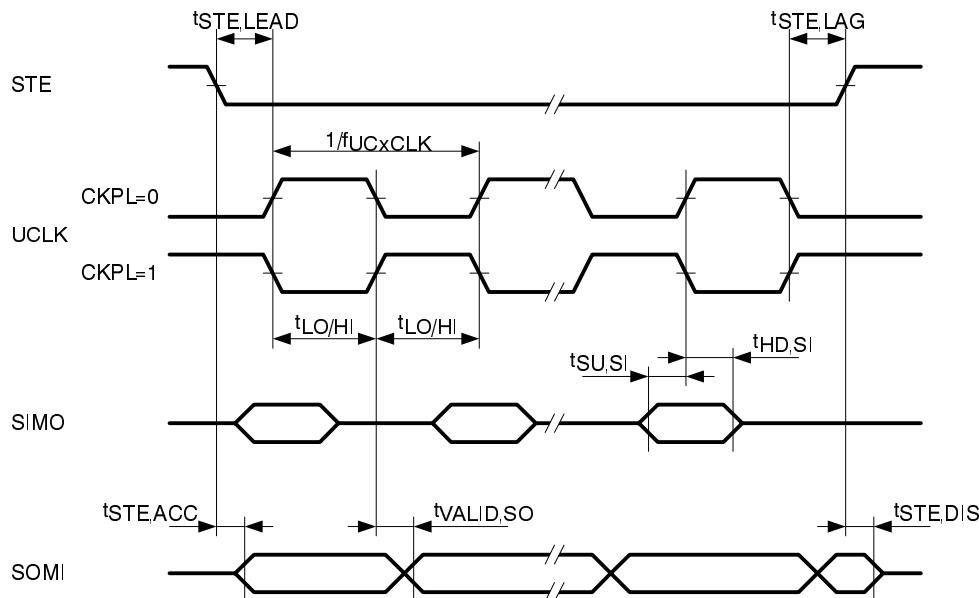


Figure 30. SPI Slave Mode, CKPH = 1

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

USCI (I²C mode) (see Figure 31)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{USCI} USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10%				f _{SYSTEM}	MHz
f _{SCL} SCL clock frequency		2.2 V/3 V	0	400	kHz	
t _{HD,STA} Hold time (repeated) Start	f _{SCL} ≤ 100 kHz	2.2 V/3 V	4.0			μs
	f _{SCL} > 100 kHz		0.6			
t _{SU,STA} Setup time for a repeated Start	f _{SCL} ≤ 100 kHz	2.2 V/3 V	4.7			μs
	f _{SCL} > 100 kHz		0.6			
t _{HD,DAT} Data hold time		2.2 V/3 V	0			ns
t _{SU,DAT} Data setup time		2.2 V/3 V	250			ns
t _{SU,STO} Setup time for Stop		2.2 V/3 V	4.0			μs
t _{SP} Pulse width of spikes suppressed by input filter		2.2 V	50	150	600	ns
		3 V	50	100	600	

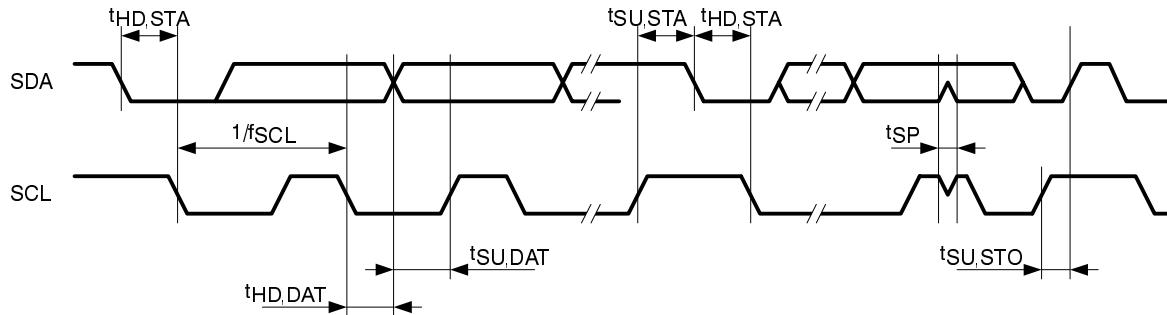


Figure 31. I²C Mode Timing

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

Comparator_A+ (see Note 1)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT	
I _(DD)	CAON = 1, CARSEL = 0, CAREF = 0	2.2 V	25	40		μA	
		3 V	45	60			
I _(Refadder/Refdiode)	CAON = 1, CARSEL = 0, CAREF = 1/2/3, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2	2.2 V	30	50		μA	
		3 V	45	71			
V _(IC)	Common-mode input voltage	CAON = 1	2.2 V/3 V	0	V _{CC} -1	V	
V _(Ref025)	Voltage at 0.25 V _{CC} node V _{CC}	PCA0 = 1, CARSEL = 1, CAREF = 1, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2	2.2 V/3 V	0.23	0.24	0.25	
V _(Ref050)	Voltage at 0.5V _{CC} node V _{CC}	PCA0 = 1, CARSEL = 1, CAREF = 2, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2	2.2 V/3 V	0.47	0.48	0.5	
V _(RefVT)	See Figure 35 and Figure 36	PCA0 = 1, CARSEL = 1, CAREF = 3, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2, T _A = 85°C	2.2 V	390	480	540	mV
			3 V	400	490	550	
V _(offset)	Offset voltage	See Note 2	2.2 V/3 V	-30	30	mV	
V _{hys}	Input hysteresis	CAON=1	2.2 V/3 V	0	0.7	1.4	mV
t _(response)	Response time, low-to-high and high-to-low (see Note 3)	T _A = 25°C, Overdrive 10 mV, Without filter: CAF = 0	2.2 V	80	165	300	ns
			3 V	70	120	240	
	T _A = 25°C, Overdrive 10 mV, With filter: CAF = 1	2.2 V	1.4	1.9	2.8	μs	
			3 V	0.9	1.5	2.2	

- NOTES:
1. The leakage current for the Comparator_A+ terminals is identical to I_{lkg(Px,x)} specification.
 2. The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A+ inputs on successive measurements. The two successive measurements are then summed together.
 3. The response time is measured at P2.2/CAOUT/TA0/CA4 with an input voltage step, with Comparator_A+ already enabled (CAON = 1). If CAON is set at the same time, a settling time of up to 300 ns is added to the response time.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

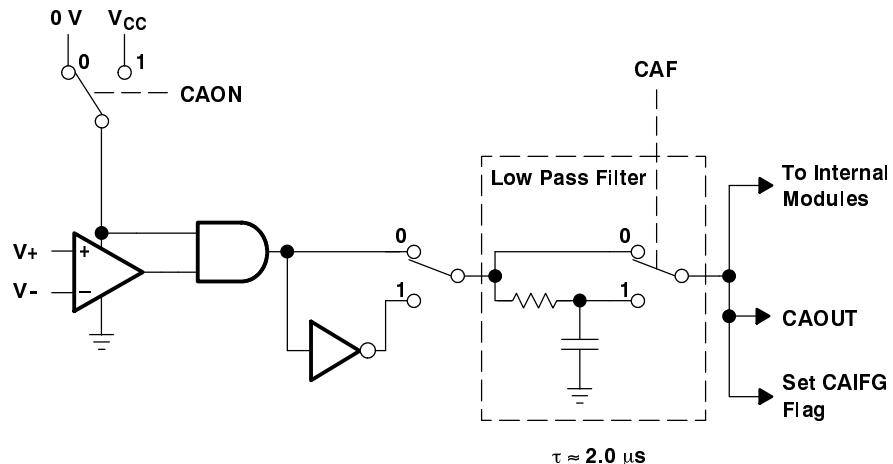


Figure 32. Block Diagram of Comparator_A Module

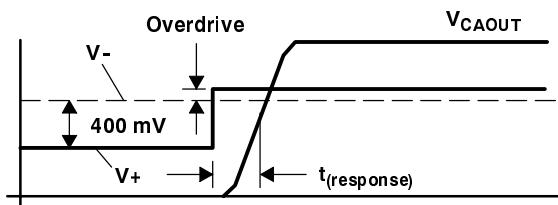


Figure 33. Overdrive Definition

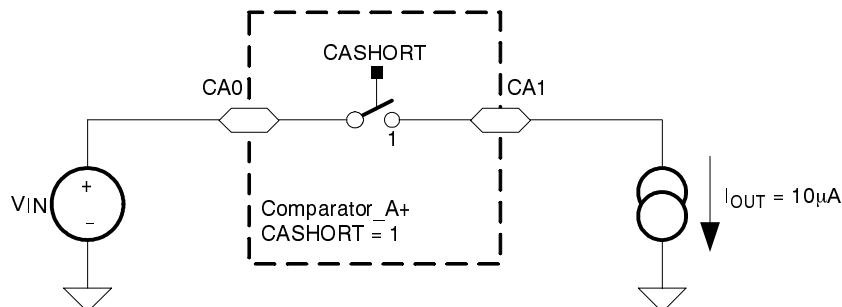


Figure 34. Comparator_A+ Short Resistance Test Condition

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics - Comparator A+

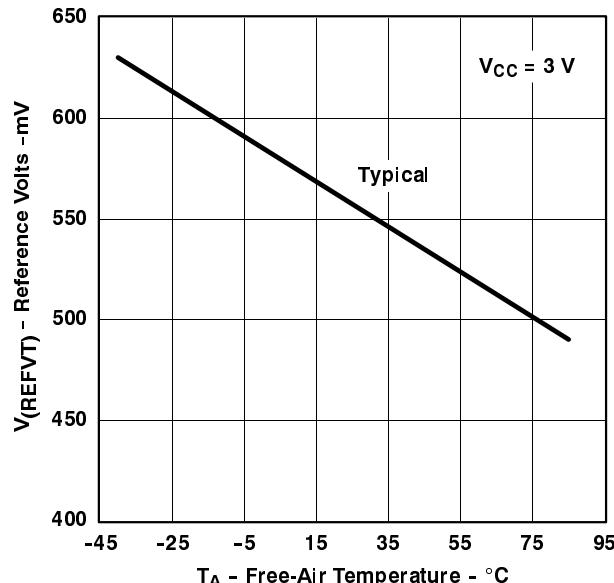


Figure 35. $V_{(REFVT)}$ vs Temperature, $V_{CC} = 3\text{ V}$

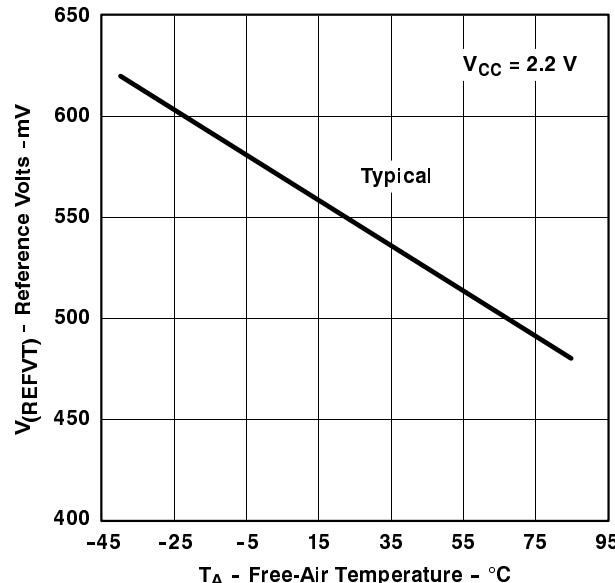


Figure 36. $V_{(REFVT)}$ vs Temperature, $V_{CC} = 2.2\text{ V}$

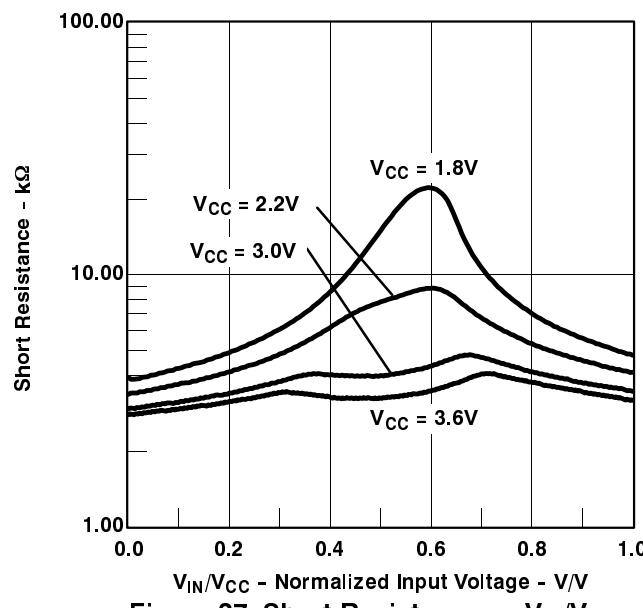


Figure 37. Short Resistance vs V_{IN}/V_{CC}

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC power supply and input range conditions (see Note 1)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
A _{V_{CC}}	Analog supply voltage A _{V_{CC}} and D _{V_{CC}} are connected together, A _{V_{SS}} and D _{V_{SS}} are connected together, V _(AVSS) = V _(DVSS) = 0 V		2.2		3.6	V
V _(P6.x/Ax)	Analog input voltage (see Note 2) All P6.0/A0 to P6.7/A7 terminals. Analog inputs selected in ADC12MCTLx register and P6Sel.x = 1, 0 ≤ x ≤ 7, V _(AVSS) ≤ V _{P6.x/Ax} ≤ V _(AVCC)		0		V _{AVCC}	V
I _{ADC12}	Operating supply current into A _{V_{CC}} terminal (see Note 3)	f _{ADC12CLK} = 5 MHz, ADC12ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC12DIV = 0	2.2 V	0.65	0.8	mA
			3 V	0.8	1.0	
I _{REF+}	Operating supply current into A _{V_{CC}} terminal (see Note 4)	f _{ADC12CLK} = 5 MHz, ADC12ON = 0, REFON = 1, REF2_5V = 1	3 V	0.5	0.7	mA
		f _{ADC12CLK} = 5 MHz, ADC12ON = 0, REFON = 1, REF2_5V = 0	2.2 V	0.5	0.7	
			3 V	0.5	0.7	
C _i †	Input capacitance Only one terminal can be selected at one time, P6.x/Ax	2.2 V			40	pF
R _i †	Input MUX ON resistance 0 V ≤ V _{Ax} ≤ V _{AVCC}	3 V			2000	Ω

† Limits verified by design

- NOTES: 1. The leakage current is defined in the leakage current table with P6.x/Ax parameter.
 2. The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
 3. The internal reference supply current is not included in current consumption parameter I_{|ADC12}.
 4. The internal reference current is supplied via terminal A_{V_{CC}}. Consumption is independent of the ADC12ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion.

12-bit ADC external reference (see Note 1)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	MAX	UNIT
V _{eREF+}	Positive external reference voltage input V _{eREF+} > V _{REF-/eREF-} (see Note 2)		1.4	V _{AVCC}	V
V _{REF-/eREF-}	Negative external reference voltage input V _{eREF+} > V _{REF-/eREF-} (see Note 3)		0	1.2	V
(V _{eREF+} - V _{REF-/eREF-})	Differential external reference voltage input V _{eREF+} > V _{REF-/eREF-} (see Note 4)		1.4	V _{AVCC}	V
I _{eREF+}	Static input current 0 V ≤ V _{eREF+} ≤ V _{AVCC}	2.2 V/3 V		±1	µA
I _{REF-/eREF-}	Static input current 0 V ≤ V _{eREF-} ≤ V _{AVCC}	2.2 V/3 V		±1	µA

- NOTES: 1. The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C_i, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.
 2. The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
 3. The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
 4. The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC built-in reference

PARAMETER	TEST CONDITIONS	V _{CC}	TA	MIN	TYP	MAX	UNIT
V _{REF+} Positive built-in reference voltage output	REF2_5V = 1 (2.5 V) V _{REF+} max ≤ V _{REF+} ≤ V _{REF+} min	3 V	-40°C to 85°C	2.4	2.5	2.6	V
	REF2_5V = 0 (1.5 V) V _{REF+} max ≤ V _{REF+} ≤ V _{REF+} min		105°C	2.37	2.5	2.64	
AV _{CC(min)} AV _{CC} minimum voltage, positive built-in reference active	REF2_5V = 0, V _{REF+} max ≤ V _{REF+} ≤ V _{REF+} min	2.2 V/3 V 2.2 V/3 V	-40°C to 85°C	1.44	1.5	1.56	V
	REF2_5V = 1, -0.5mA ≤ V _{REF+} max ≤ V _{REF+} min		105°C	1.42	1.5	1.57	
	REF2_5V = 1, -1mA ≤ V _{REF+} max ≤ V _{REF+} min						
V _{REF+} Load current out of V _{REF+} terminal		2.2 V		0.01	-0.5	mA	
		3 V		0.01	-1		
I _{L(VREF+)} [†] Load-current regulation, V _{REF+} terminal	V _{REF+} = 500 μA +/- 100 μA Analog input voltage ~0.75 V, REF2_5V = 0	2.2 V				±2	LSB
	V _{REF+} = 500 μA ± 100 μA Analog input voltage ~1.25 V, REF2_5V = 1	3 V				±2	
		3 V				±2	
I _{DL(VREF+)} [‡] Load current regulation V _{REF+} terminal	V _{REF+} = 100 μA → 900 μA, C _{VREF+} = 5 μF, at ~0.5 V _{REF+} , Error of conversion result ≤ 1 LSB	3 V				20	ns
C _{VREF+}	Capacitance at pin V _{REF+} (see Note 1)	REFON = 1, 0 mA ≤ V _{REF+} ≤ V _{REF+} max	2.2 V/3 V		5	10	μF
T _{REF+} [†]	Temperature coefficient of built-in reference	V _{REF+} is a constant in the range of 0 mA ≤ V _{REF+} ≤ 1 mA	2.2 V/3 V			±100	ppm/°C
t _{REFON} [†]	Settle time of internal reference voltage (see Figure 38 and Note 2)	V _{REF+} = 0.5 mA, C _{VREF+} = 10 μF, V _{REF+} = 1.5 V, V _{AVCC} = 2.2 V				17	ms

[†] Limits characterized

[‡] Limits verified by design

- NOTES:
- The internal buffer operational amplifier and the accuracy specifications require an external capacitor. All INL and DNL tests use two capacitors between pins V_{REF+} and AV_{SS} and V_{REF-}/V_{eREF-} and AV_{SS}: 10 μF tantalum and 100 nF ceramic.
 - The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB. The settling time depends on the external capacitive load.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics - ADC12

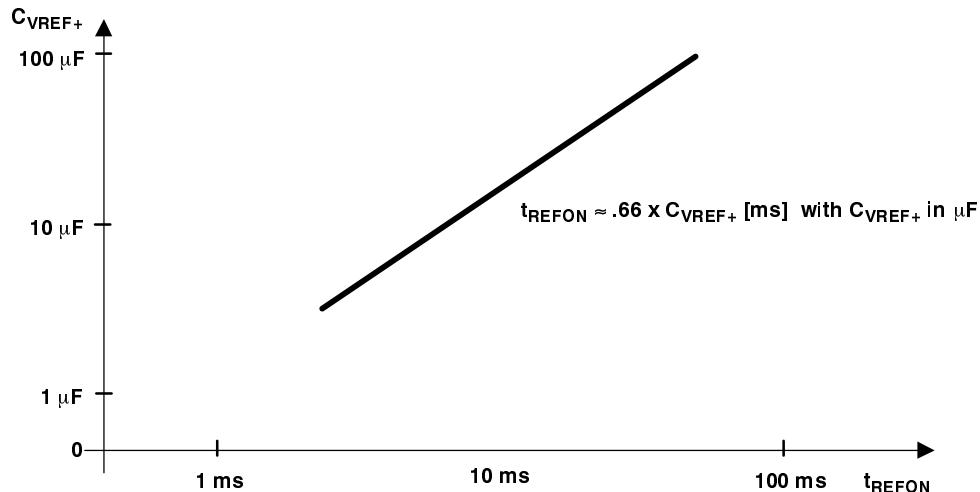


Figure 38. Typical Settling Time of Internal Reference t_{REFON} vs External Capacitor on V_{REF+}

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

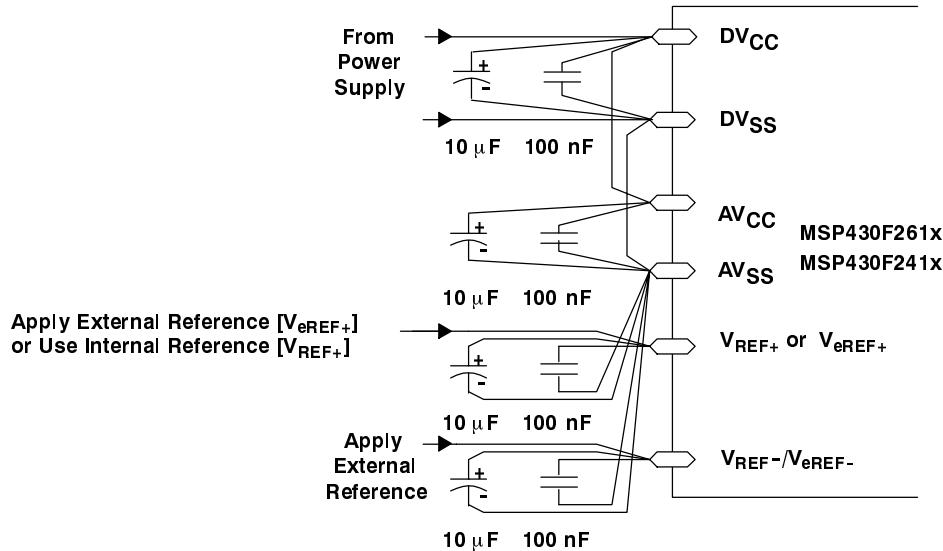


Figure 39. Supply Voltage and Reference Voltage Design V_{REF-}/V_{eREF-} External Supply

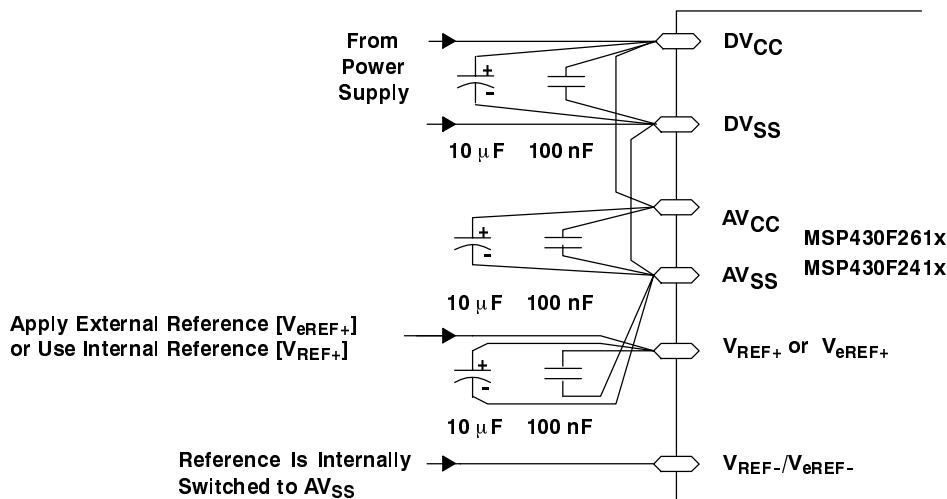


Figure 40. Supply Voltage and Reference Voltage Design $V_{REF-}/V_{eREF-} = AV_{SS}$, Internally Connected

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC timing parameters

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT	
f _{ADC12CLK}	For specified performance of ADC12 linearity parameters	2.2V/3 V	0.45	5	6.3	MHz	
f _{ADC12OSC}	Internal ADC12 oscillator	ADC12DIV = 0, f _{ADC12CLK} = f _{ADC12OSC}	2.2 V / 3 V	3.7	5	6.3	MHz
t _{CONVERT}	Conversion time	C _{VREF+} ≥ 5 μF, Internal oscillator, f _{ADC12OSC} = 3.7 MHz to 6.3 MHz	2.2 V / 3 V	2.06	3.51	μs	
		External f _{ADC12CLK} from ACLK, MCLK or SMCLK, ADC12SSEL ≠ 0		13 × ADC12DIV × 1/f _{ADC12CLK}			
t _{ADC12ON} [†]	Turn-on settling time of the ADC	See Note 1			100	ns	
t _{Sample} [‡]	Sampling time	R _S = 400 Ω, R _I = 1000 Ω, C _I = 30 pF, τ = [R _S + R _I] × C _I ; (see Note 2)	3 V	1220		ns	
			2.2 V	1400			

[†] Limits characterized

[‡] Limits verified by design

- NOTES: 1. The condition is that the error in a conversion started after t_{ADC12ON} is less than ±0.5 LSB. The reference and input signal are already settled.
2. Approximately ten Tau (τ) are needed to get an error of less than ±0.5 LSB:
 $t_{\text{sample}} = \ln(2^{n+1}) \times (R_S + R_I) \times C_I + 800 \text{ ns}$ where n = ADC resolution = 12, R_S = external source resistance.

12-bit ADC linearity parameters

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
E _I	1.4 V ≤ (V _{eREF+} - V _{REF-} /V _{eREF-}) min ≤ 1.6 V	2.2 V/3 V		±2		LSB
	1.6 V < (V _{eREF+} - V _{REF-} /V _{eREF-}) min ≤ V _{AVCC}			±1.7		
E _D	(V _{eREF+} - V _{REF-} /V _{eREF-}) _{min} ≤ (V _{eREF+} - V _{REF-} /V _{eREF-}), C _{VREF+} = 10 μF (tantalum) and 100 nF (ceramic)	2.2 V/3 V		±1		LSB
E _O	(V _{eREF+} - V _{REF-} /V _{eREF-}) _{min} ≤ (V _{eREF+} - V _{REF-} /V _{eREF-}), Internal impedance of source R _S < 100 Ω, C _{VREF+} = 10 μF (tantalum) and 100 nF (ceramic)	2.2 V/3 V		±2	±4	LSB
E _G	(V _{eREF+} - V _{REF-} /V _{eREF-}) _{min} ≤ (V _{eREF+} - V _{REF-} /V _{eREF-}), C _{VREF+} = 10 μF (tantalum) and 100 nF (ceramic)	2.2 V/3 V		±1.1	±2	LSB
E _T	(V _{eREF+} - V _{REF-} /V _{eREF-}) _{min} ≤ (V _{eREF+} - V _{REF-} /V _{eREF-}), C _{VREF+} = 10 μF (tantalum) and 100 nF (ceramic)	2.2 V/3 V		±2	±5	LSB

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC temperature sensor and built-in V_{MID}

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
I _{SENSOR}	Operating supply current into AV _{CC} terminal (see Note 1)	REFON = 0, INCH = 0Ah, ADC12ON = 1, T _A = 25°C	2.2 V	40	120	μA
		3 V	60	160		
V _{SENSOR} [†]	See Note 2	ADC12ON = 1, INCH = 0Ah, T _A = 0°C	2.2 V	986		mV
		3 V	986			
T _C _{SENSOR} [†]		ADC12ON = 1, INCH = 0Ah	2.2 V	3.55		mV/°C
		3 V	3.55			
t _{SENSOR(sample)} [†]	Sample time required if channel 10 is selected (see Note 3)	ADC12ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB	2.2 V	30		μs
		3 V	30			
I _V _{MID}	Current into divider at channel 11 (see Note 4)	ADC12ON = 1, INCH = 0Bh	2.2 V		NA	μA
		3 V			NA	
V _{MID}	AV _{CC} divider at channel 11	ADC12ON = 1, INCH = 0Bh, V _{MID} is ~0.5 × V _{AVCC}	2.2 V	1.1	1.1 ± 0.04	V
		3 V	1.5	1.50 ± 0.04		
t _V _{MID} (sample)	Sample time required if channel 11 is selected (see Note 5)	ADC12ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB	2.2 V	1400		ns
		3 V	1220			

[†] Limits characterized

- NOTES:
- The sensor current I_{SENSOR} is consumed if (ADC12ON = 1 and REFON = 1) or if (ADC12ON = 1, INCH = 0Ah and sample signal is high). When REFON = 1, I_{SENSOR} is already included in I_{REF+}.
 - The temperature sensor offset can be as much as ±20°C. A single-point calibration is recommended to minimize the offset error of the built-in temperature sensor.
 - The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time t_{SENSOR(on)}.
 - No additional current is needed. The V_{MID} is used during sampling.
 - The on time t_V_{MID}(on) is included in the sampling time t_V_{MID}(sample); no additional on time is needed.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

12-bit DAC supply specifications

PARAMETER	TEST CONDITIONS	V _{CC}	T _A	MIN	TYP	MAX	UNIT
AV _{CC} Analog supply voltage	AV _{CC} = DV _{CC} , AV _{SS} = DV _{SS} = 0 V			2.20	3.60		V
I _{DD} Supply current, single DAC channel (see Notes 1 and 2)	DAC12AMPx = 2, DAC12IR = 0, DAC12_xDAT = 0x0800	2.2V/3V	-40°C to 85°C	50	110		μA
	DAC12AMPx = 2, DAC12IR = 1, DAC12_xDAT = x00800, V _{eREF+} = V _{REF+} = AV _{CC}		105°C	69	150		
	DAC12AMPx = 5, DAC12IR = 1, DAC12_xDAT = 0x0800, V _{eREF+} = V _{REF+} = AV _{CC}	2.2V/3V		50	130		
	DAC12AMPx = 7, DAC12IR = 1, DAC12_xDAT = 0x0800, V _{eREF+} = V _{REF+} = AV _{CC}	2.2V/3V		200	440		
PSRR Power-supply rejection ratio (see Notes 3 and 4)	DAC12_xDAT = 800h, V _{REF} = 1.5 V, ΔAV _{CC} = 100mV	2.2V		70			dB
	DAC12_xDAT = 800h, V _{REF} = 1.5 V or 2.5 V, ΔAV _{CC} = 100mV	3V					

- NOTES: 1. No load at the output pin, DAC12_0 or DAC12_1, assuming that the control bits for the shared pins are set properly.
 2. Current into reference terminals not included. If DAC12IR = 1 current flows through the input divider; see Reference Input specifications.
 3. PSRR = $20 \times \log \{\Delta V_{CC}/\Delta V_{DAC12_XOUT}\}$
 4. V_{REF} is applied externally. The internal reference is not used.

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit DAC linearity specifications (see Figure 41)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT		
Resolution		12-bit monotonic		12			bits		
INL	Integral nonlinearity (see Note 1)	V _{REF} = 1.5 V DAC12AMPx = 7, DAC12 R = 1	2.2 V		±2.0	±8.0	LSB		
		V _{REF} = 2.5 V DAC12AMPx = 7, DAC12 R = 1	3 V						
DNL	Differential nonlinearity (see Note 1)	V _{REF} = 1.5 V DAC12AMPx = 7, DAC12 R = 1	2.2 V		±0.4	±1.0	LSB		
		V _{REF} = 2.5 V DAC12AMPx = 7, DAC12 R = 1	3 V						
E _O	Offset voltage without calibration (see Notes 1 and 2)	V _{REF} = 1.5 V DAC12AMPx = 7, DAC12 R = 1	2.2 V		±21	mV	mV		
		V _{REF} = 2.5 V DAC12AMPx = 7, DAC12 R = 1	3 V						
	Offset voltage with calibration (see Notes 1 and 2)	V _{REF} = 1.5 V DAC12AMPx = 7, DAC12 R = 1	2.2 V		±2.5				
		V _{REF} = 2.5 V DAC12AMPx = 7, DAC12 R = 1	3 V						
d _{E(O)} /d _T	Offset error temperature coefficient (see Note 1)		2.2 V/3 V	30			µV/C		
E _G	Gain error (see Note 1)	V _{REF} = 1.5 V	2.2 V		±3.50	% FSR			
		V _{REF} = 2.5 V	3 V						
d _{E(G)} /d _T	Gain temperature coefficient (see Note 1)		2.2 V/3 V	10			ppm of FSR/°C		
t _{Offset_Cal}	Time for offset calibration (see Note 3)	DAC12AMPx = 2		100		ms	ms		
		DAC12AMPx = 3, 5	2.2 V/3 V	32					
		DAC12AMPx = 4, 6, 7		6					

- NOTES:
1. Parameters calculated from the best-fit curve from 0x0A to 0xFFFF. The best-fit curve method is used to deliver coefficients "a" and "b" of the first-order equation: $y = a + b \times x$. $V_{DAC12_xOUT} = E_O + (1 + E_G) \times (V_{eREF+}/4095) \times DAC12_xDAT$, DAC12|R = 1.
 2. The offset calibration works on the output operational amplifier. Offset calibration is triggered setting bit DAC12CALON.
 3. The offset calibration can be done if DAC12AMPx = {2, 3, 4, 5, 6, 7}. The output operational amplifier is switched off with DAC12AMPx = {0, 1}. The DAC12 module should be configured prior to initiating calibration. Port activity during calibration may affect accuracy and is not recommended.

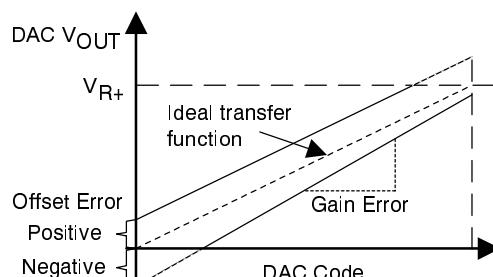
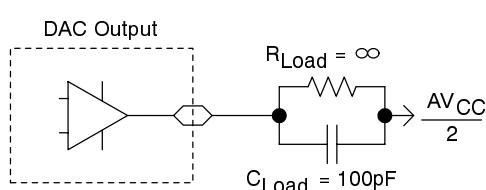
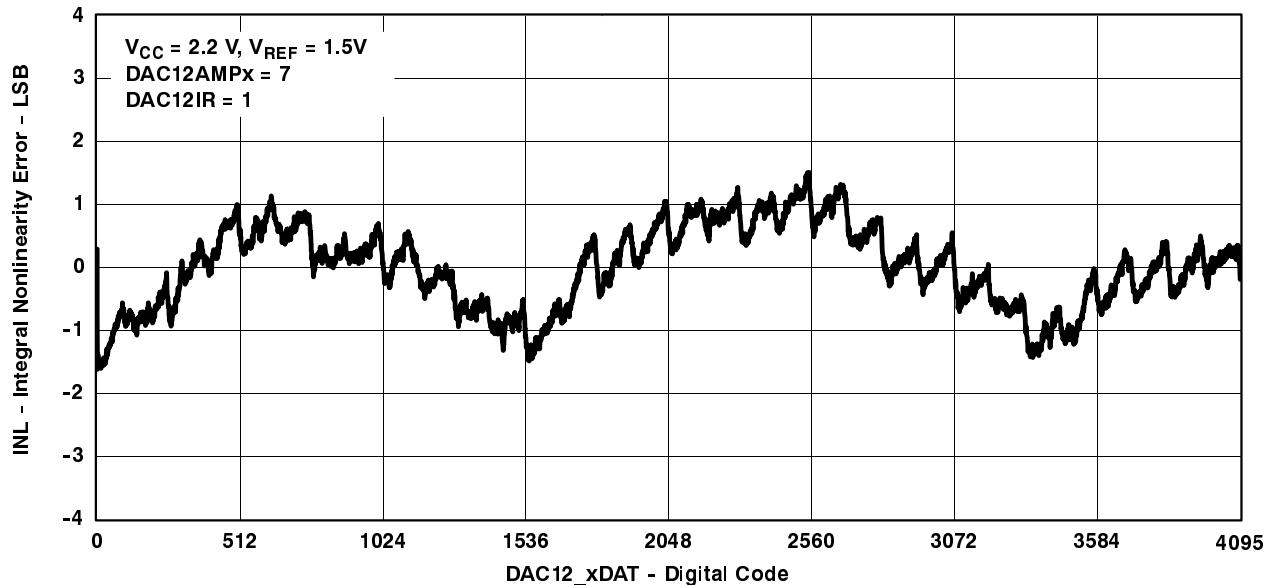


Figure 41. Linearity Test Load Conditions and Gain/Offset Definition

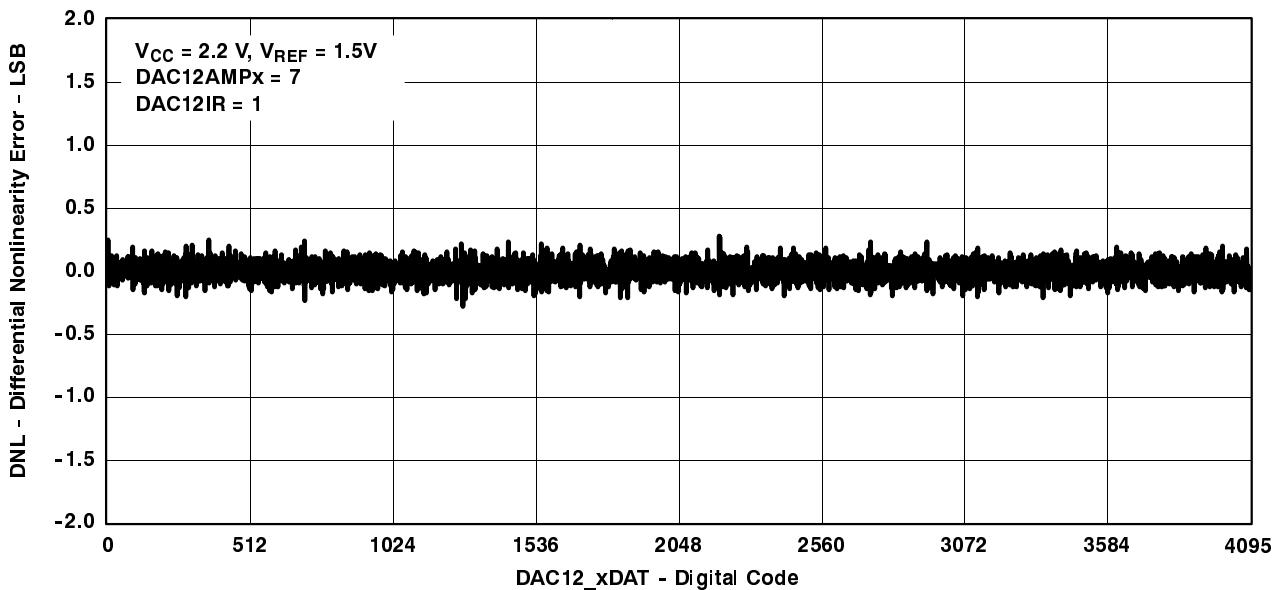
electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

typical characteristics - 12-bit DAC, linearity specifications

TYPICAL INL ERROR
vs
DIGITAL INPUT DATA



TYPICAL DNL ERROR
vs
DIGITAL INPUT DATA



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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit DAC output specifications

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _O Output voltage range (see Note 1 and Figure 44)	No Load, V _{eREF+} = AV _{CC} , DAC12_xDAT = 0h, DAC12 R = 1, DAC12AMPx = 7	2.2 V/3 V	0	0.005		V
	No Load, V _{eREF+} = AV _{CC} , DAC12_xDAT = 0FFFh, DAC12 R = 1, DAC12AMPx = 7		AV _{CC} -0.05		AV _{CC}	
	R _{Load} = 3 kΩ, V _{eREF+} = AV _{CC} , DAC12_xDAT = 0h, DAC12 R = 1, DAC12AMPx = 7		0	0.1		
	R _{Load} = 3 kΩ, V _{eREF+} = AV _{CC} , DAC12_xDAT = 0FFFh, DAC12 R = 1, DAC12AMPx = 7		AV _{CC} -0.13		AV _{CC}	
C _{L(DAC12)} Max DAC12 load capacitance		2.2 V/3 V		100		pF
I _{L(DAC12)} Max DAC12 load current		2.2V	-0.5	+0.5		mA
		3V	-1.0	+1.0		
R _{O/P(DAC12)} Output resistance (see Figure 44)	R _{Load} = 3 kΩ, V _{O/P(DAC12)} = 0 V, DAC12AMPx = 7, DAC12_xDAT = 0h	2.2 V/3 V	150	250		Ω
	R _{Load} = 3 kΩ, V _{O/P(DAC12)} = AV _{CC} , DAC12AMPx = 7, DAC12_xDAT = 0FFFh		150	250		
	R _{Load} = 3 kΩ, 0.3 V < V _{O/P(DAC12)} ≤ AV _{CC} - 0.3 V, DAC12AMPx = 7		1	4		

NOTE 1: Data is valid after the offset calibration of the output amplifier.

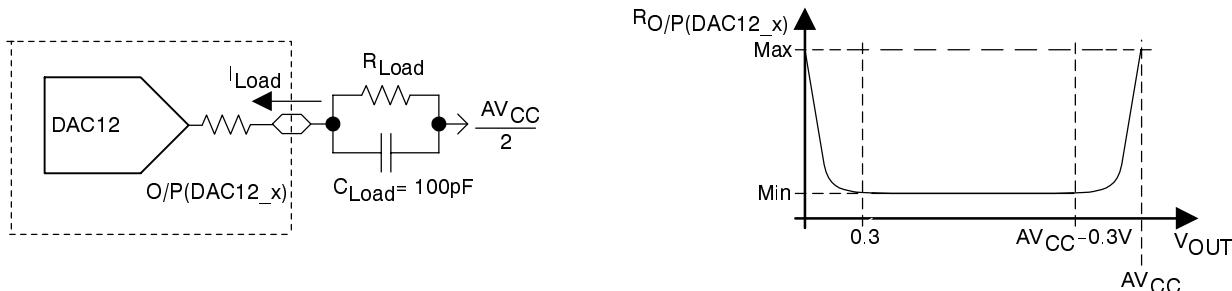


Figure 44. DAC12_x Output Resistance Tests

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit DAC reference input specifications

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{eREF+}	Reference input voltage range	DAC12IR = 0, (see Notes 1 and 2)	2.2 V/3 V	AV _{CC} /3		AV _{CC} +0.2	V
		DAC12IR = 1, (see Notes 3 and 4)		AV _{CC}		AV _{CC} +0.2	
R _i (V _{REF+}), R _i (V _{eREF+})	Reference input resistance	DAC12_0 IR = DAC12_1 IR = 0	2.2 V/3 V	20		MΩ	
		DAC12_0 IR = 1, DAC12_1 IR = 0		40		48	56
		DAC12_0 IR = 0, DAC12_1 IR = 1		20		24	28
		DAC12_0 IR = DAC12_1 IR = 1	2.2 V/3 V	kΩ			
		DAC12_0 SREFx = DAC12_1 SREFx (see Note 5)					

- NOTES:
1. For a full-scale output, the reference input voltage can be as high as 1/3 of the maximum output voltage swing (AV_{CC}).

$$V_{eREF+} = [AV_{CC} - V_{E(O)}] / [3*(1 + E_G)]$$
 2. The maximum voltage applied at reference input voltage terminal V_{eREF+} = [AV_{CC} - V_{E(O)}] / (1 + E_G).
 3. For a full-scale output, the reference input voltage can be as high as the maximum output voltage swing (AV_{CC}).

$$V_{eREF+} = [AV_{CC} - V_{E(O)}] / (1 + E_G)$$
 4. When DAC12IR = 1 and DAC12SREFx = 0 or 1 for both channels, the reference input resistive dividers for each DAC are in parallel reducing the reference input resistance.

12-bit DAC dynamic specifications, V_{ref} = V_{CC}, DAC12IR = 1 (see Figure 45 and Figure 46)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT	
t _{ON}	DAC12 on-time	DAC12_xDAT = 800h, Error _{V(O)} < ±0.5 LSB (see Note 1 and Figure 45)	2.2 V/3 V	60		120	μs	
		DAC12AMPx = 0 → {2, 3, 4}		15		30		
		DAC12AMPx = 0 → {5, 6}		6		12		
t _{S(FS)}	Settling time, full scale	DAC12_xDAT = 80h → F7Fh → 80h	2.2 V/3 V	100		200	μs	
		DAC12AMPx = 2		40		80		
		DAC12AMPx = 4, 6, 7		15		30		
t _{S(C-C)}	Settling time, code to code	DAC12_xDAT = 3F8h → 408h → 3F8h	2.2 V/3 V	5		μs		
		BF8h → C08h → BF8h		2				
		DAC12AMPx = 4, 6, 7		1				
SR	Slew rate	DAC12_xDAT = 80h → F7Fh → 80h	2.2 V/3 V	0.05	0.12	V/μs		
		DAC12AMPx = 3, 5		0.35	0.7			
		DAC12AMPx = 4, 6, 7		1.5	2.7			
Glitch energy, full scale	Glitch energy, full scale	DAC12_xDAT = 80h → F7Fh → 80h	2.2 V/3 V	600		nV-s		
		DAC12AMPx = 3, 5		150				
		DAC12AMPx = 4, 6, 7		30				

- NOTES:
1. R_{Load} and C_{Load} are connected to AV_{SS} (not AV_{CC}/2) in Figure 45.
 2. Slew rate applies to output voltage steps ≥ 200 mV.

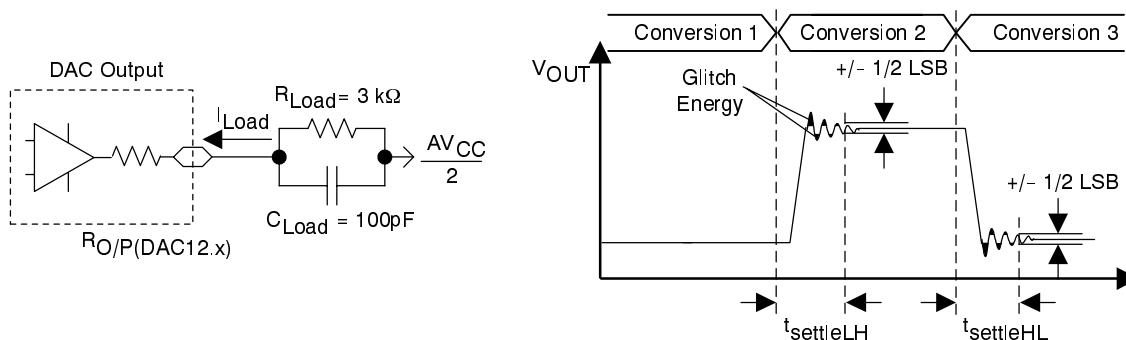


Figure 45. Settling Time and Glitch Energy Testing

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

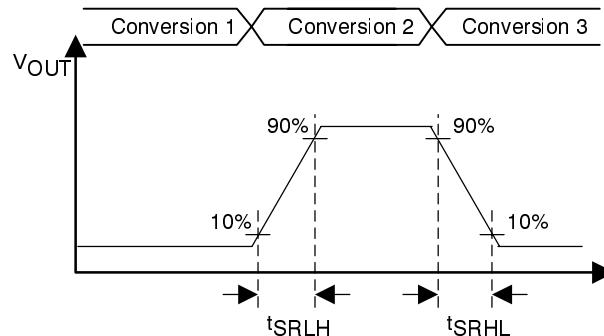


Figure 46. Slew Rate Testing

12-bit DAC, dynamic specifications (continued) ($T_A = 25^\circ\text{C}$, unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
BW _{-3dB} 3-dB bandwidth, V _{DC} = 1.5 V, V _{AC} = 0.1 V _{PP} (see Figure 47)	DAC12AMPx = {2, 3, 4}, DAC12SREFx = 2, DAC12 R = 1, DAC12_xDAT = 800h	2.2 V/3 V	40	180	550	kHz
	DAC12AMPx = {5, 6}, DAC12SREFx = 2, DAC12 R = 1, DAC12_xDAT = 800h					
	DAC12AMPx = 7, DAC12SREFx = 2, DAC12 R = 1, DAC12_xDAT = 800h					
Channel-to-channel crosstalk (see Note 1 and Figure 48)	DAC12_0DAT = 800h, No load, DAC12_1DAT = 80h->F7Fh, R _{Load} = 3 kΩ, f _{DAC12_1OUT} = 10 kHz, Duty cycle = 50%	2.2 V/3 V	-80	-80	dB	
	DAC12_0DAT = 80h->F7Fh, R _{Load} = 3 kΩ, DAC12_1DAT = 800h, No load, f _{DAC12_0OUT} = 10 kHz, Duty cycle = 50%					

NOTE 1: R_{LOAD} = 3 kΩ, C_{LOAD} = 100 pF

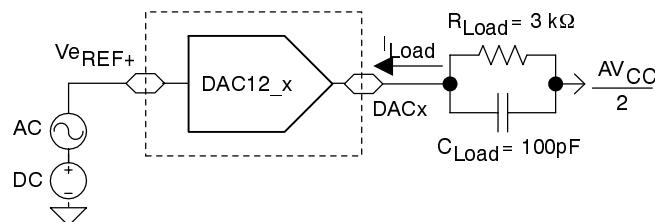


Figure 47. Test Conditions for 3-dB Bandwidth Specification

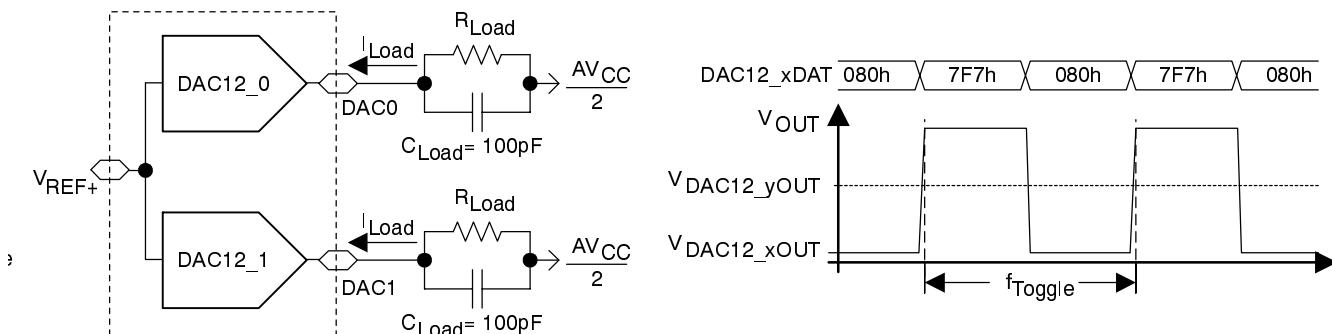


Figure 48. Crosstalk Test Conditions

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

flash memory

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{CC(PGM/ERASE)} Program and erase supply voltage			2.2	3.6	3.6	V
f _{FTG} Flash Timing Generator frequency			257	476	476	KHz
I _{PGM} Supply current from DV _{CC} during program		2.2 V/ 3.6 V	3	5	5	mA
I _{ERASE} Supply current from DV _{CC} during erase		2.2 V/ 3.6 V	3	7	7	mA
t _{CPT} Cumulative program time	See Note 1	2.2 V/ 3.6 V			10	ms
t _{CMErase} Cumulative mass erase time		2.2 V/ 3.6 V	20			ms
Program/Erase endurance			10 ⁴	10 ⁵		cycles
t _{Retention} Data retention duration	T _J = 25°C		100			years
t _{Word} Word or byte program time	See Note 2			35		t _{FTG}
t _{Block, 0} Block program time for first byte or word	See Note 2			30		t _{FTG}
t _{Block, 1-63} Block program time for each additional byte or word	See Note 2			21		t _{FTG}
t _{Block, End} Block program end-sequence wait time	See Note 2			6		t _{FTG}
t _{Mass Erase} Mass erase time	See Note 2			10593		t _{FTG}
t _{Seg Erase} Segment erase time	See Note 2			4819		t _{FTG}

NOTES: 1. The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
 2. These values are hardwired into the Flash Controller's state machine ($t_{FTG} = 1/f_{FTG}$).

RAM

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
VRAMh See Note 1	CPU halted	1.6		V

NOTE 1: This parameter defines the minimum supply voltage when the data in program memory RAM remain unchanged. No program execution should take place during this supply voltage condition.

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

JTAG interface

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
f _{TCK} TCK input frequency	See Note 1	2.2 V	0	5		MHz
		3 V	0	10		
R _{Internal} Internal pullup resistance on TMS, TCK, TDI/TCLK	See Note 2	2.2 V/ 3 V	25	60	90	kΩ

NOTES: 1. f_{TCK} may be restricted to meet the timing requirements of the module selected.

2. TMS, TDI/TCLK, and TCK pullup resistors are implemented in all versions.

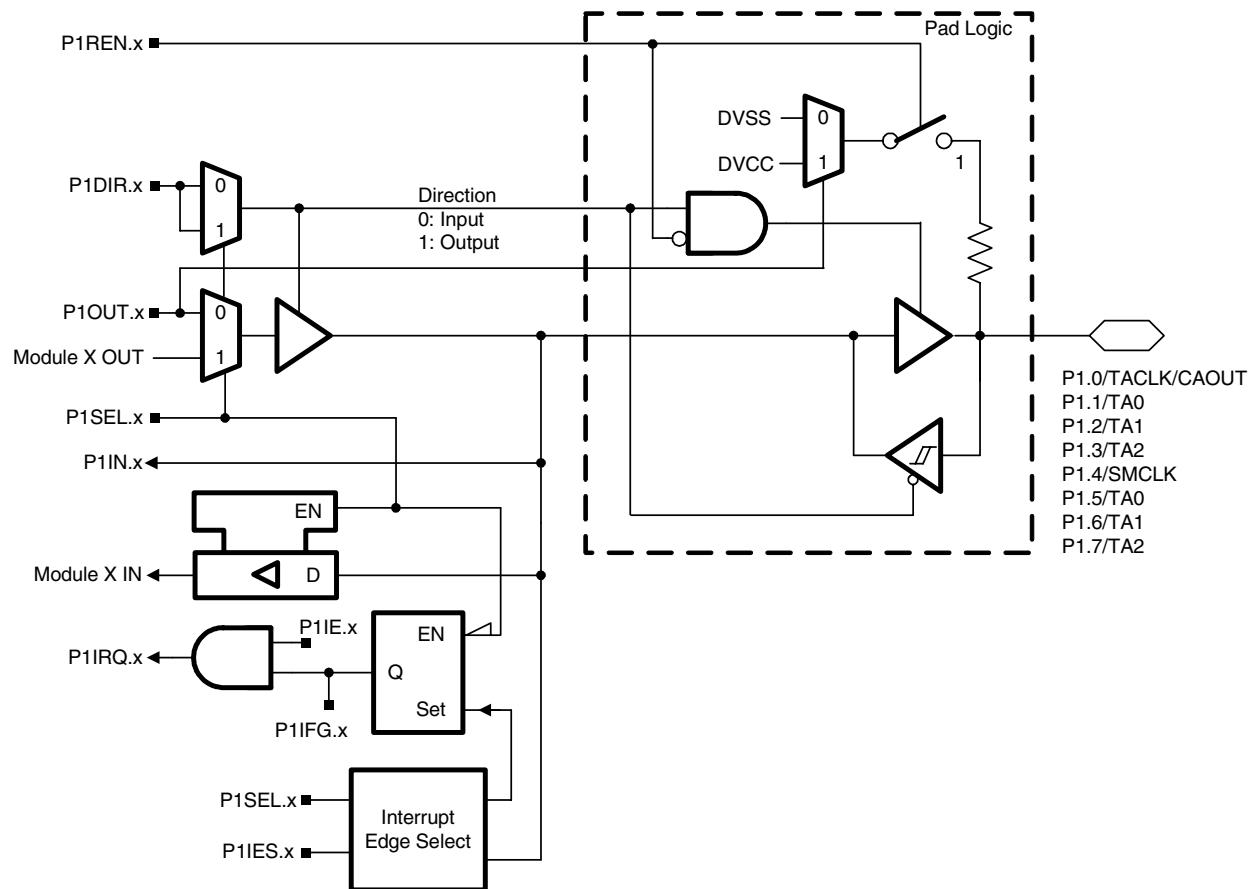
JTAG fuse (see Note 1)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V _{CC(FB)} Supply voltage during fuse-blow condition	T _A = 25°C	2.5		V
V _{FB} Voltage level on TDI/TCLK for fuse blow (F versions)		6	7	V
I _{FB} Supply current into TDI/TCLK during fuse blow			100	mA
t _{FB} Time to blow fuse			1	ms

NOTE 1: Once the fuse is blown, no further access to the MSP430 JTAG/Test and emulation features is possible. The JTAG block is switched to bypass mode.

APPLICATION INFORMATION

Port P1 pin schematic: P1.0 to P1.7, input/output with Schmitt trigger



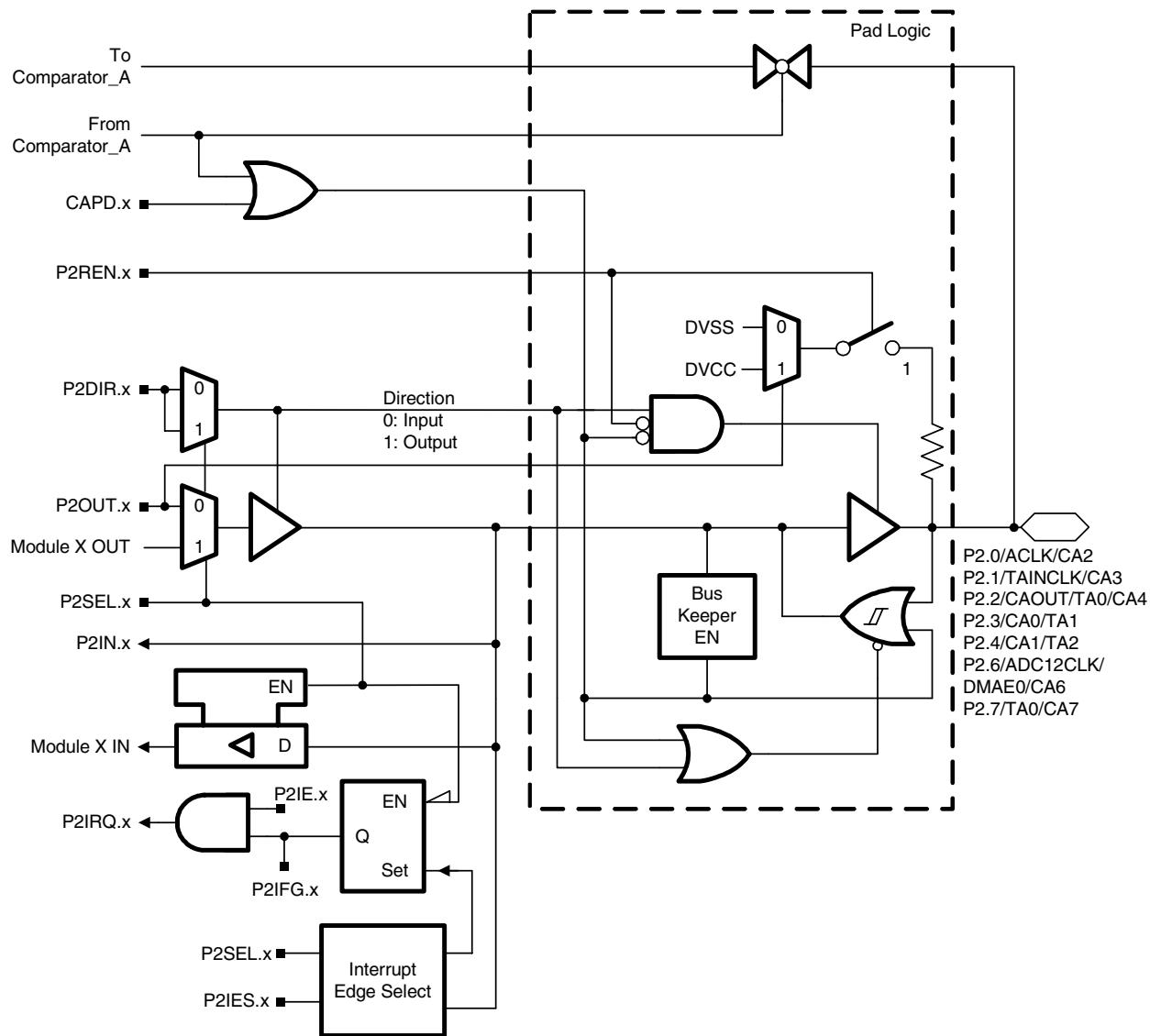
MSP430F241x, MSP430F261x MIXED SIGNAL MICROCONTROLLER

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Port P1 (P1.0 to P1.7) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P1DIR.X	P1SEL.X
P1.0/TACLK/CAOUT	0	P1.0 (I/O)	I: 0; O: 1	0
		Timer_A3.TACLK	0	1
		CAOUT	1	1
P1.1/TA0	1	P1.1 (I/O)	I: 0; O: 1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA0	1	1
P1.2/TA1	2	P1.2 (I/O)	I: 0; O: 1	0
		Timer_A3.CCI1A	0	1
		Timer_A3.TA1	1	1
P1.3/TA2	3	P1.3 (I/O)	I: 0; O: 1	0
		Timer_A3.CCI2A	0	1
		Timer_A3.TA2	1	1
P1.4/SMCLK	4	P1.4 (I/O)	I: 0; O: 1	0
		SMCLK	1	1
P1.5/TA0	5	P1.5 (I/O)	I: 0; O: 1	0
		Timer_A3.TA0	1	1
P1.6/TA1	6	P1.6 (I/O)	I: 0; O: 1	0
		Timer_A3.TA1	1	1
P1.7/TA2	7	P1.7 (I/O)	I: 0; O: 1	0
		Timer_A3.TA2	1	1

Port P2 pin schematic: P2.0 to P2.4, P2.6, and P2.7, input/output with Schmitt trigger



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Port P2.0, P2.3, P2.4, P2.6 and P2.7 pin functions

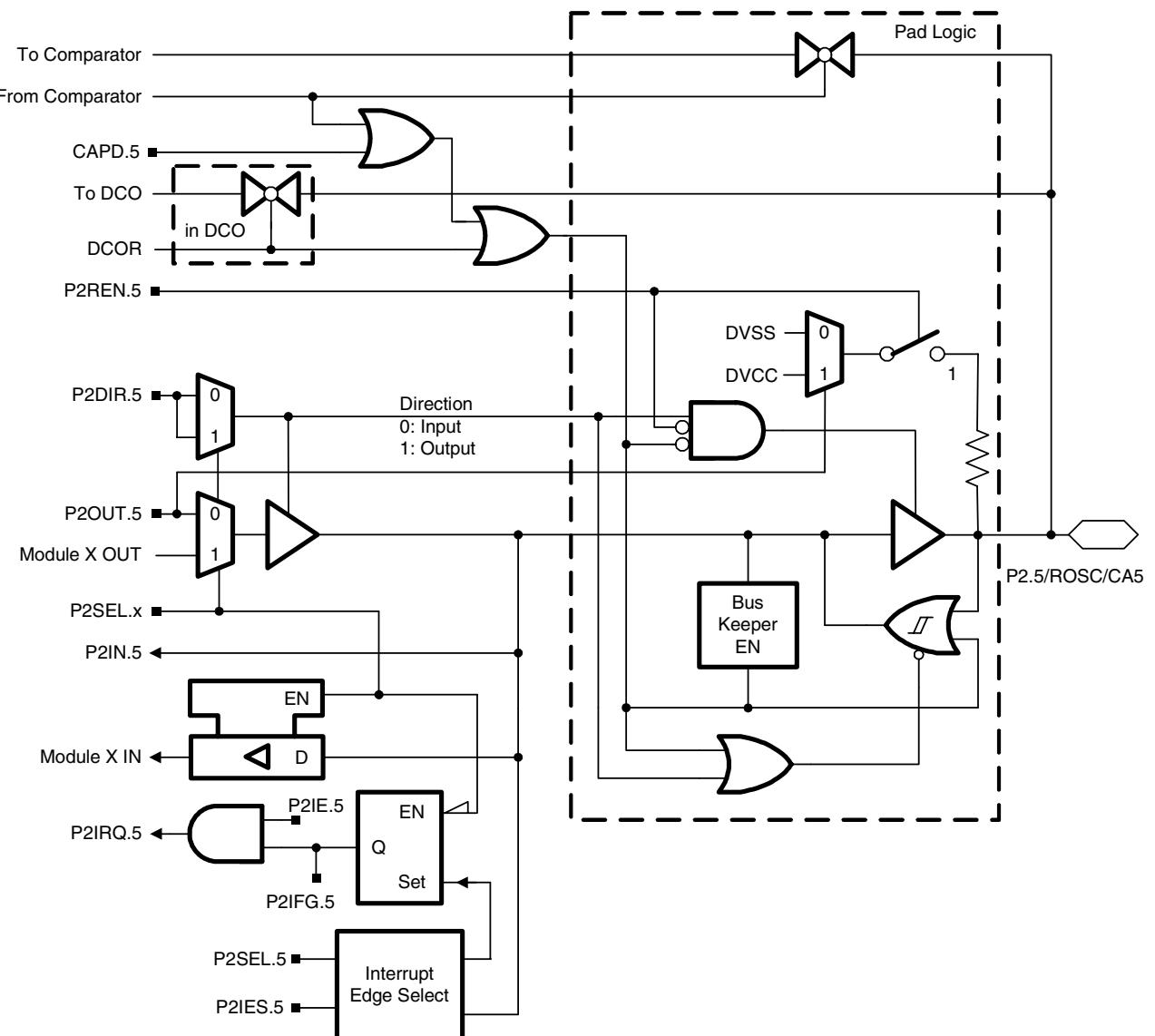
PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			CAPD.x	P2DIR.X	P2SEL.X
P2.0/ACLK/CA2	0	P2.0 (I/O)	0	I: 0; O: 1	0
		ACLK	0	1	1
		CA2	1	X	X
P2.1/TA1/NCLK/CA3	1	P2.1 (I/O)	0	I: 0; O: 1	0
		Timer_A3.NCLK	0	0	1
		DV _{SS}	0	1	1
		CA3	1	X	X
P2.2/CAOUT/TA0/CA4	2	P2.2 (I/O)	0	I: 0; O: 1	0
		CAOUT	0	1	1
		Timer_A3.CC10B	0	0	1
		CA4	1	X	X
P2.3/CA0/TA1	3	P2.3 (I/O)	0	I: 0; O: 1	0
		Timer_A3.TA1	0	1	1
		CA0	1	X	X
P2.4/CA1/TA2	4	P2.4 (I/O)	0	I: 0; O: 1	0
		Timer_A3.TA2	0	1	X
		CA1	1	X	1
P2.6/ADC12CLK/DMAE0/CA6	6	P2.6 (I/O)	0	I: 0; O: 1	0
		ADC12CLK	0	1	1
		DMAE0	0	0	1
		CA6	1	X	X
P2.7/TA0/CA7	7	P2.7 (I/O)	0	I: 0; O: 1	0
		Timer_A3.TA0	0	1	1
		CA7	1	X	X

NOTE: X: Don't care



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Port P2 pin schematic: P2.5, input/output with Schmitt trigger



Port P2.5 pin functions

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS			
			CAPD	DCOR	P2DIR.5	P2SEL.5
P2.5/Rosc/CA5	5	P2.5 (I/O)	0	0	I: 0; O: 1	0
		Rosc (see Note 2)	0	1	X	X
		DVss	0	0	1	1
		CA5	1 or selected	0	X	X

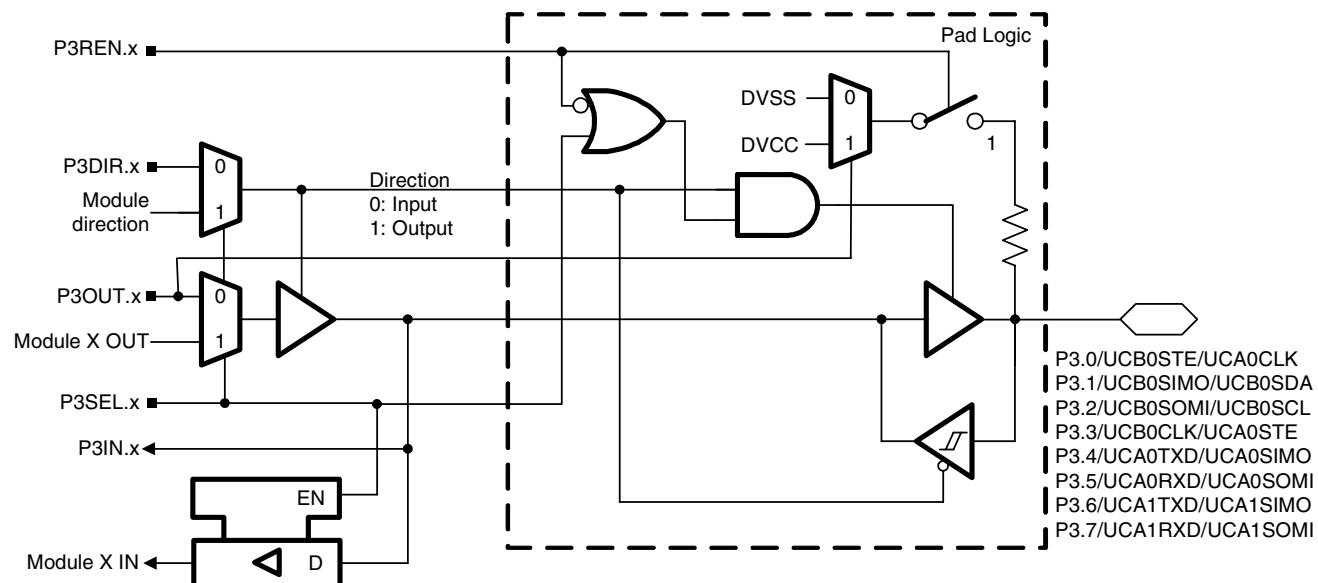
NOTES: 1. X: Don't care

2. If Rosc is used it is connected to an external resistor.

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Port P3 pin schematic: P3.0 to P3.7, input/output with Schmitt trigger



Port P3.0 to P3.7 pin functions

PIN NAME (P3.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P3DIR.X	P3SEL.X
P3.0/UCB0STE/ UCA0CLK	0	P3.0 (I/O)	I: 0; O: 1	0
		UCB0STE/UCA0CLK (see Note 2 and 4)	X	1
P3.1/UCB0SIMO/ UCB0SDA	1	P3.1 (I/O)	I: 0; O: 1	0
		UCB0SIMO/UCB0SDA (see Note 2 and 3)	X	1
P3.2/UCB0SOMI/ UCB0SCL	2	P3.2 (I/O)	I: 0; O: 1	0
		UCB0SOMI/UCB0SCL (see Note 2 and 3)	X	1
P3.3/UCB0CLK/ UCA0STE	3	P3.3 (I/O)	I: 0; O: 1	0
		UCB0CLK/UCA0STE (see Note 2)	X	1
P3.4/UCA0TXD/ UCA0SIMO	4	P3.4 (I/O)	I: 0; O: 1	0
		UCA0TXD/UCA0SIMO (see Note 2)	X	1
P3.5/UCA0RXD/ UCA0SOMI	5	P3.5 (I/O)	I: 0; O: 1	0
		UCA0RXD/UCA0SOMI (see Note 2)	X	1
P3.6/UCA1TXD/ UCA1SIMO	6	P3.6 (I/O)	I: 0; O: 1	0
		UCA1TXD/UCA1SIMO (see Note 2)	X	1
P3.7/UCA1RXD/ UCA1SOMI	7	P3.7 (I/O)	I: 0; O: 1	0
		UCA1RXD/UCA1SOMI (see Note 2)	X	1

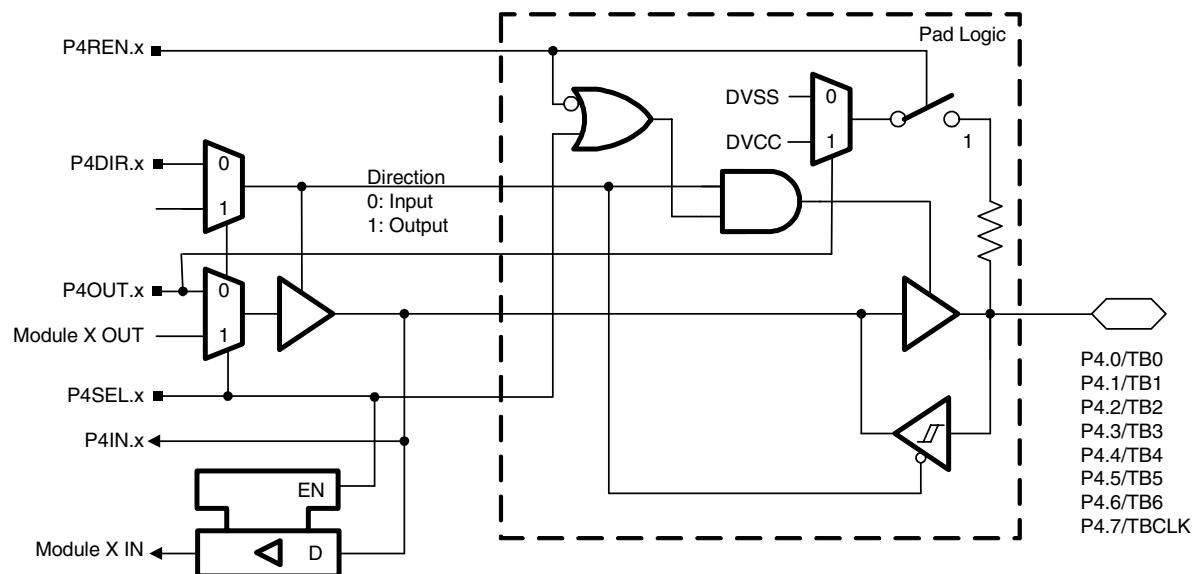
NOTES: 1. X: Don't care

2. The pin direction is controlled by the USCI module.

3. In case the I2C functionality is selected the output drives only the logical 0 to V_{SS} level.

4. UCA0CLK function takes precedence over UCB0STE function. If the pin is required as UCA0CLK input or output, USCI A0/B0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.

Port P4 pin schematic: P4.0 to P4.7, input/output with Schmitt trigger



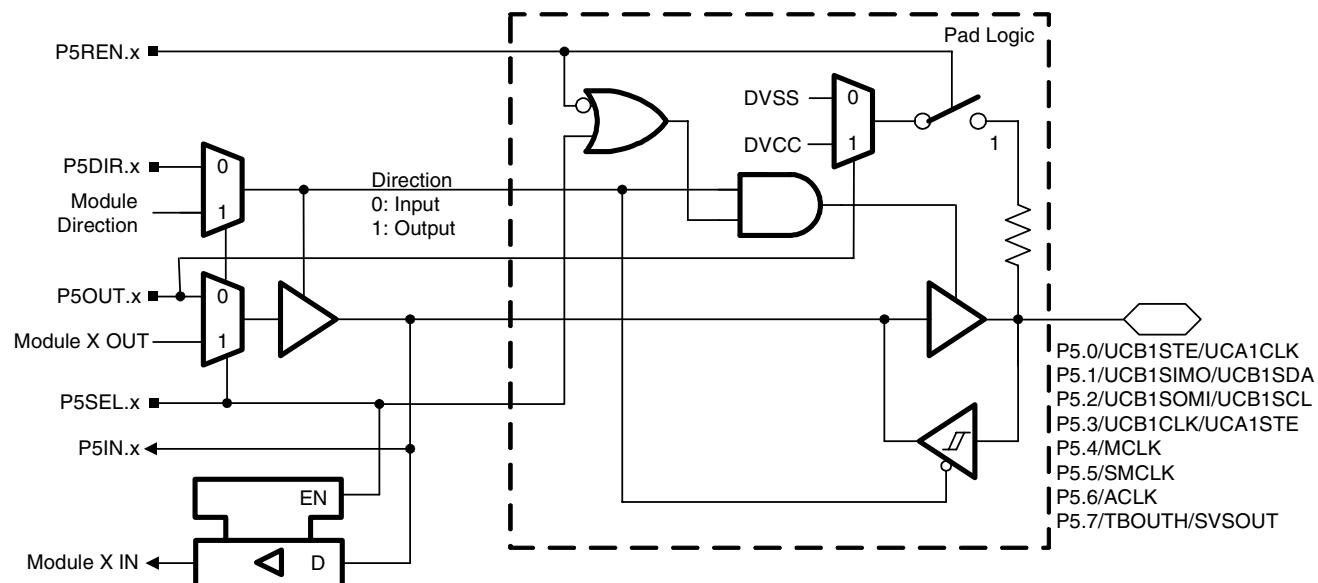
Port P4.0 to P4.7 pin functions

PIN NAME (P4.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P4DIR.x	P4SEL.x
P4.0/TB0	0	P4.0 (I/O)	I: 0; O: 1	0
		Timer_B7.CC10A and Timer_B7.CC10B	0	1
		Timer_B7.TB0	1	1
P4.1/TB1	1	P4.1 (I/O)	I: 0; O: 1	0
		Timer_B7.CC11A and Timer_B7.CC11B	0	1
		Timer_B7.TB1	1	1
P4.2/TB2	2	P4.2 (I/O)	I: 0; O: 1	0
		Timer_B7.CC12A and Timer_B7.CC12B	0	1
		Timer_B7.TB2	1	1
P4.3/TB3	3	P4.3 (I/O)	I: 0; O: 1	0
		Timer_B7.CC13A and Timer_B7.CC13B	0	1
		Timer_B7.TB3	1	1
P4.4/TB4	4	P4.4 (I/O)	I: 0; O: 1	0
		Timer_B7.CC14A and Timer_B7.CC14B	0	1
		Timer_B7.TB4	1	1
P4.5/TB5	5	P4.5 (I/O)	I: 0; O: 1	0
		Timer_B7.CC15A and Timer_B7.CC15B	0	1
		Timer_B7.TB5	1	1
P4.6/TB6	6	P4.6 (I/O)	I: 0; O: 1	0
		Timer_B7.CC16A and Timer_B7.CC16B	0	1
		Timer_B7.TB6	1	1
P4.7/TBCLK	7	P4.7 (I/O)	I: 0; O: 1	0
		Timer_B7.TBCLK	1	1

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Port P5 pin schematic: P5.0 to P5.7, input/output with Schmitt trigger



Port P5.0 to P5.7 pin functions

PIN NAME (P5.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P5DIR.X	P5SEL.X
P5.0/UCB1STE/ UCA1CLK	0	P5.0 (I/O)	I: 0; O: 1	0
		UCB1STE/UCA1CLK (see Note 2 and 4)	X	1
P5.1/UCB1SIMO/ UCB1SDA	1	P5.1 (I/O)	I: 0; O: 1	0
		UCB1SIMO/UCB1SDA (see Note 2 and 3)	X	1
P5.2/UCB1SOMI/ UCB1SCL	2	P5.2 (I/O)	I: 0; O: 1	0
		UCB1SOMI/UCB1SCL (see Note 2 and 3)	X	1
P5.3/UCB1CLK/ UCA1STE	3	P5.3 (I/O)	I: 0; O: 1	0
		UCB1CLK/UCA1STE (see Note 2)	X	1
P5.4/MCLK	4	P5.0 (I/O)	I: 0; O: 1	0
		MCLK	1	1
P5.5/SMCLK	5	P5.1 (I/O)	I: 0; O: 1	0
		SMCLK	1	1
P5.6/ACLK	6	P5.2 (I/O)	I: 0; O: 1	0
		ACLK	1	1
P5.7/TBOUTH/ SVSOUT	7	P5.7 (I/O)	I: 0; O: 1	0
		TBOUTH	0	1
		SVSOUT	1	1

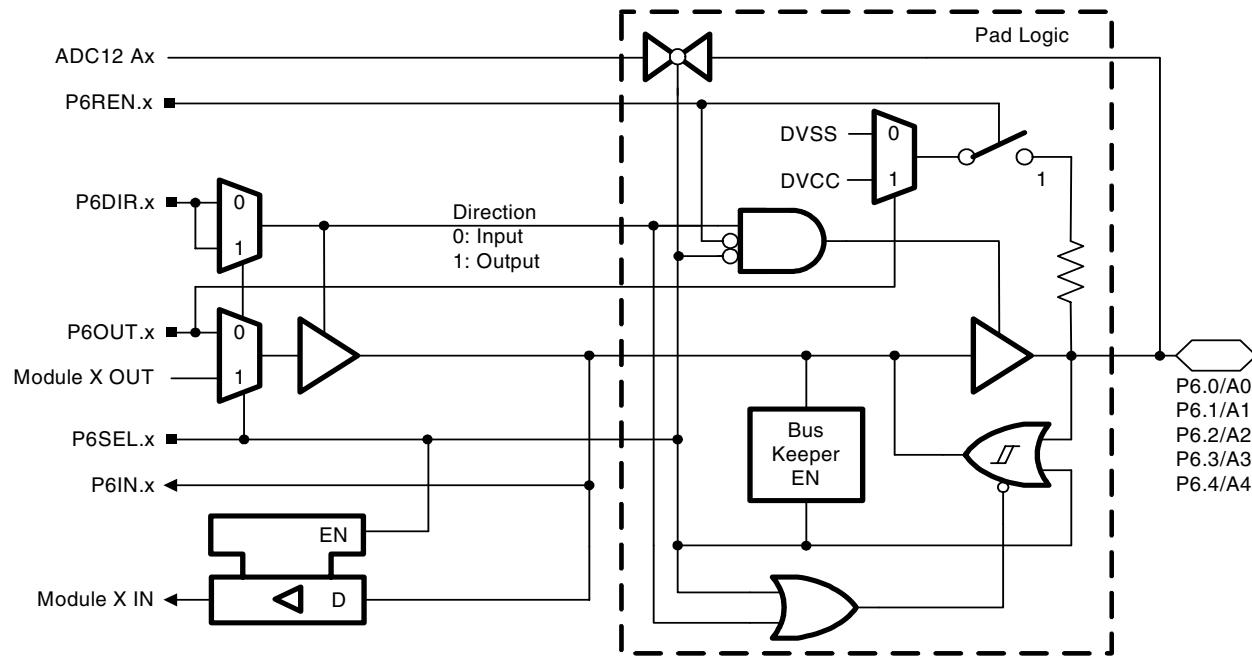
NOTES: 1. X: Don't care

2. The pin direction is controlled by the USCI module.

3. In case the I2C functionality is selected the output drives only the logical 0 to V_{SS} level.

4. UCA1CLK function takes precedence over UCB1STE function. If the pin is required as UCA1CLK input or output USCI A1/B1 will be forced to 3-wire SPI mode if 4-wire SPI mode is selected.

Port P6 pin schematic: P6.0 to P6.4, input/output with Schmitt trigger



Port P6.0 to P6.4 pin functions

PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P6DIR.x	P6SEL.x
P6.0/A0	0	P6.0 (I/O) A0 (see Note 2)	I: 0; O: 1	0
	1		X	X
P6.1/A1	1	P6.1 (I/O) A1 (see Note 2)	I: 0; O: 1	0
	2		X	X
P6.2/A2	2	P6.2 (I/O) A2 (see Note 2)	I: 0; O: 1	0
	3		X	X
P6.3/A3	3	P6.3 (I/O) A3 (see Note 2)	I: 0; O: 1	0
	4		X	X
P6.4/A4	4	P6.4 (I/O) A4 (see Note 2)	I: 0; O: 1	0
	5		X	X

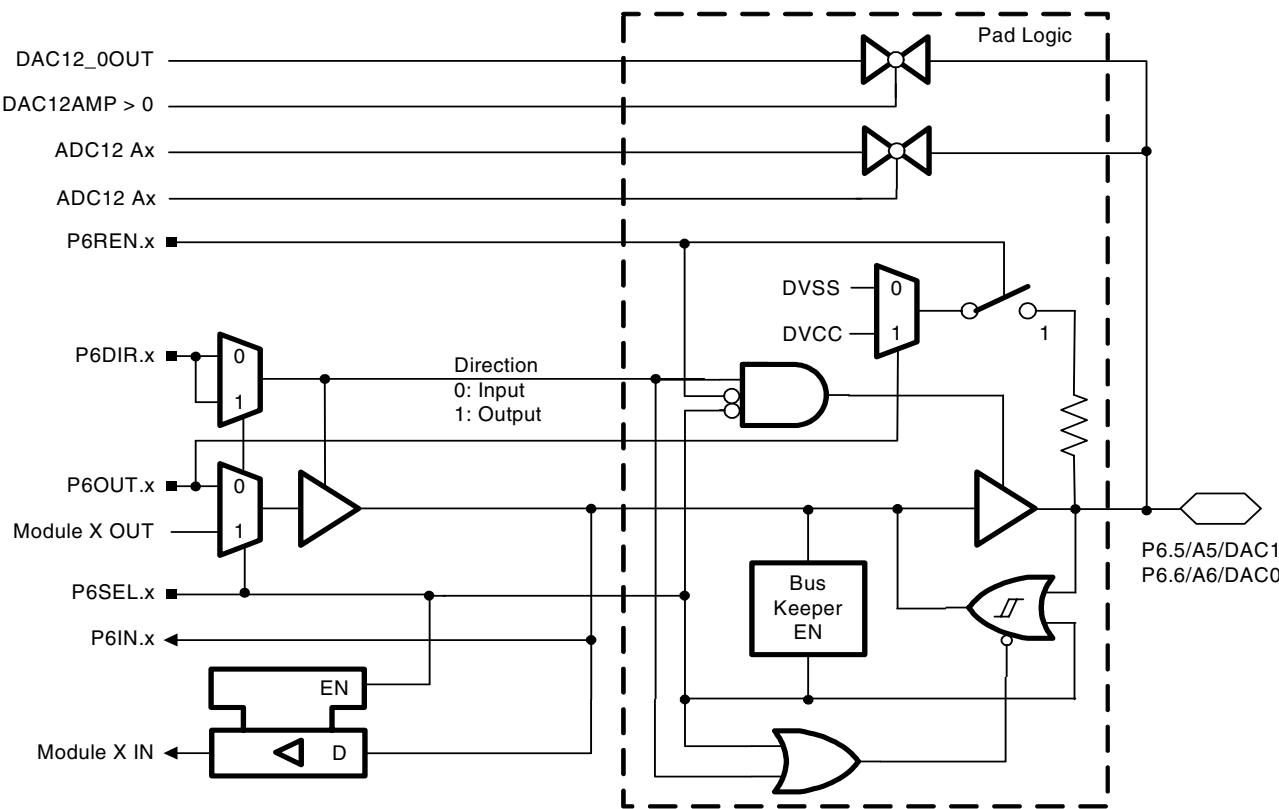
NOTES: 1. X: Don't care

2. The ADC12 channel Ax is connected to AVss internally if not selected.

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Port P6 pin schematic: P6.5 and P6.6, input/output with Schmitt trigger



Port P6.5 to P6.6 pin functions

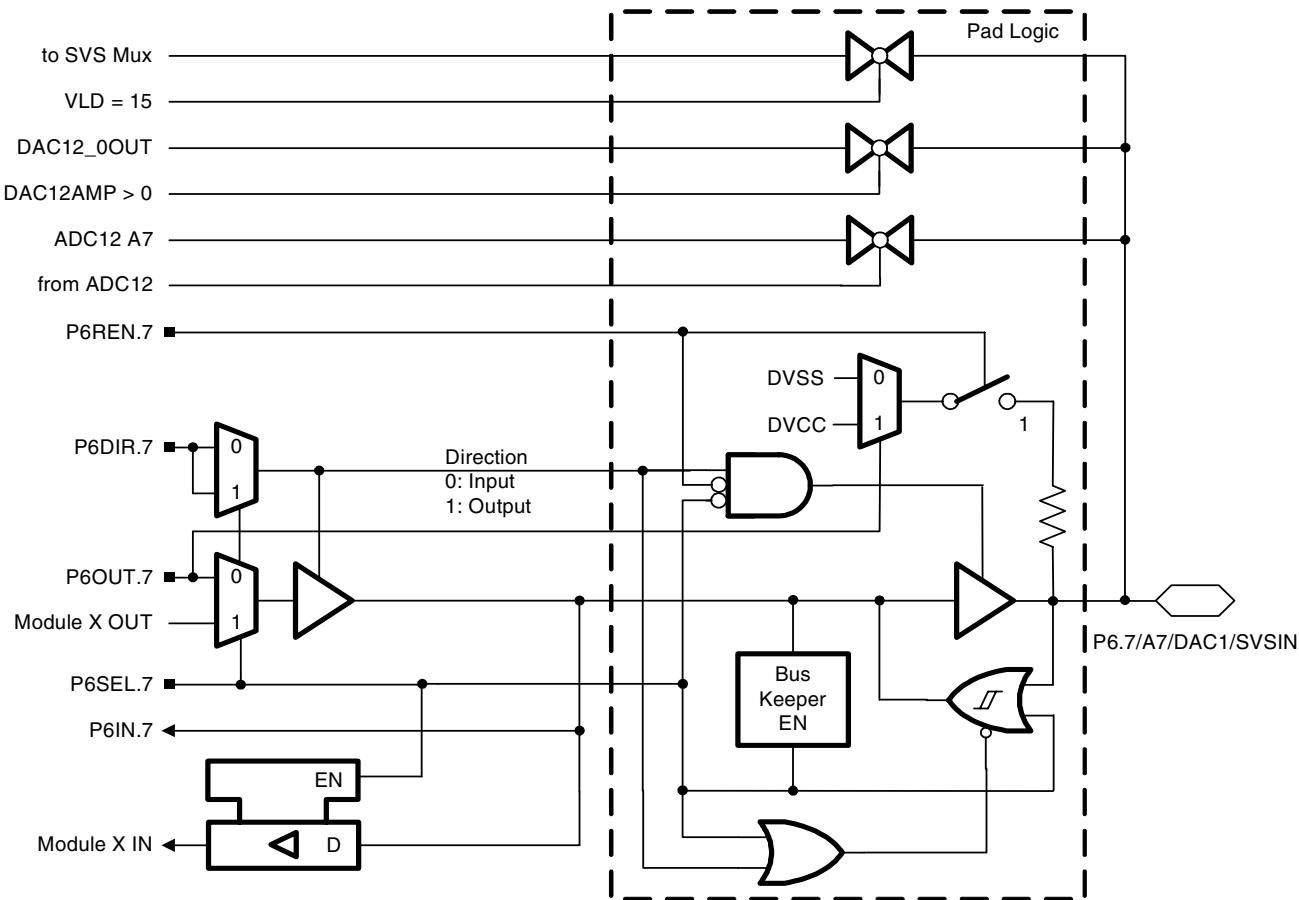
PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P6DIR.x	P6SEL.x	CAPD.x or DAC12AMP > 0
P6.5/A5/DAC1†	5	P6.5 (I/O)	I: 0; O: 1	0	0
		DVss	1	1	0
		A5 (see Note 2)	X	X	1
		DAC1 (DA12OPS= 1, see Note 3)	X	X	1
P6.6/A6/DAC0†	6	P6.6 (I/O)	I: 0; O: 1	0	0
		DVss	1	1	0
		A6 (see Note 2)	X	X	1
		DAC0 (DA12OPS= 0, see Note 3)	X	X	1

† MSP430F261x devices only

NOTES:

1. X: Don't care
2. The ADC12 channel Ax is connected to AVss internally if not selected.
3. The DAC outputs are floating if not selected.

Port P6 pin schematic: P6.7, input/output with Schmitt trigger



Port P6.7 pin functions

PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P6DIR.x	P6SEL.x
P6.7/A7/DAC1†/ SVSINT	7	P6.7 (I/O)	I: 0; O: 1	0
		DV _{SS}	1	1
		A7 (see Note 2)	X	X
		DAC1 (DA12OPS= 0, see Note 3)	X	X
		SVSIN (VLD = 15)	X	X

NOTES: 1. X: Don't care

2. The ADC12 channel Ax is connected to AVss internally if not selected.

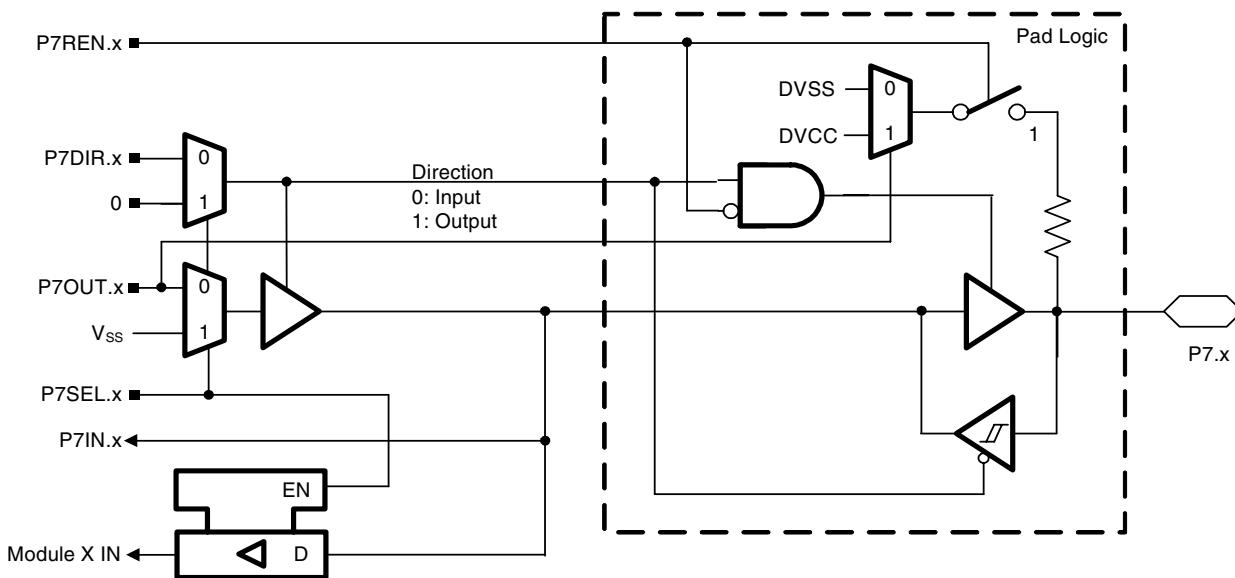
3. The DAC outputs are floating if not selected.

† MSP430F261x devices only

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Port P7 pin schematic: P7.0 to P7.7, input/output with Schmitt trigger[†]

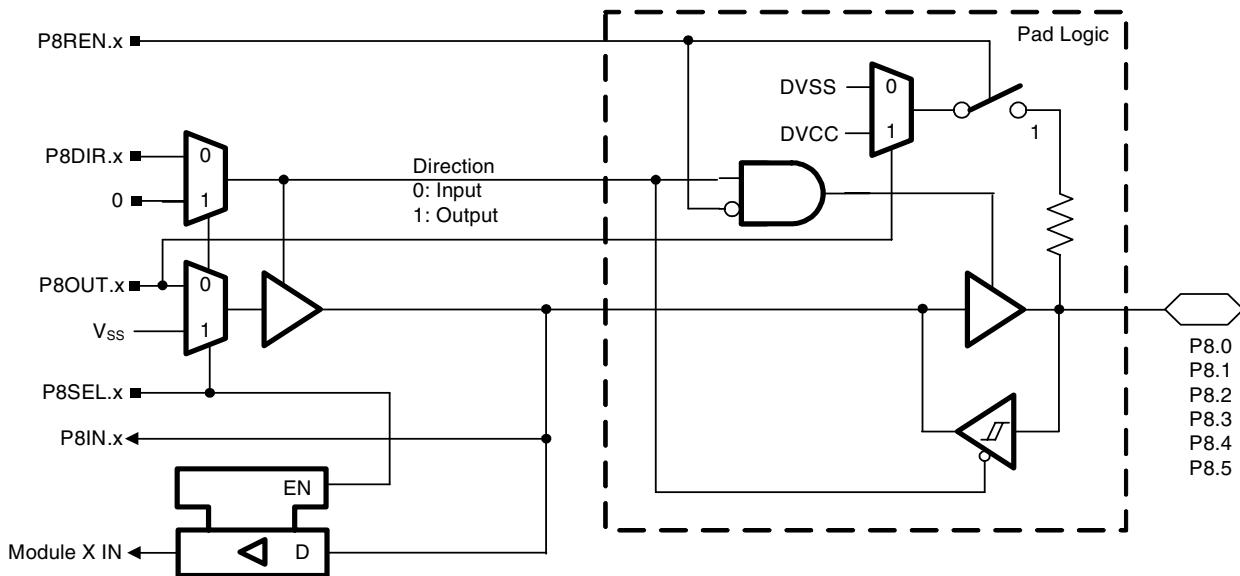


Port P7.0 to P7.7 pin functions[†]

PIN NAME (P7.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P7DIR.x	P7SEL.x
P7.0	0	P7.0 (I/O)	I: 0; O: 1	0
		Input	X	1
P7.1	1	P7.1 (I/O)	I: 0; O: 1	0
		Input	X	1
P7.2	2	P7.2 (I/O)	I: 0; O: 1	0
		Input	X	1
P7.3	3	P7.3 (I/O)	I: 0; O: 1	0
		Input	X	1
P7.4	4	P7.4 (I/O)	I: 0; O: 1	0
		Input	X	1
P7.5	5	P7.5 (I/O)	I: 0; O: 1	0
		Input	X	1
P7.6	6	P7.6 (I/O)	I: 0; O: 1	0
		Input	X	1
P7.7	7	P7.7 (I/O)	I: 0; O: 1	0
		Input	X	1

[†] 80-pin devices only

Port P8 pin schematic: P8.0 to P8.5, input/output with Schmitt trigger[†]



Port P8.0 to P8.5 pin functions[†]

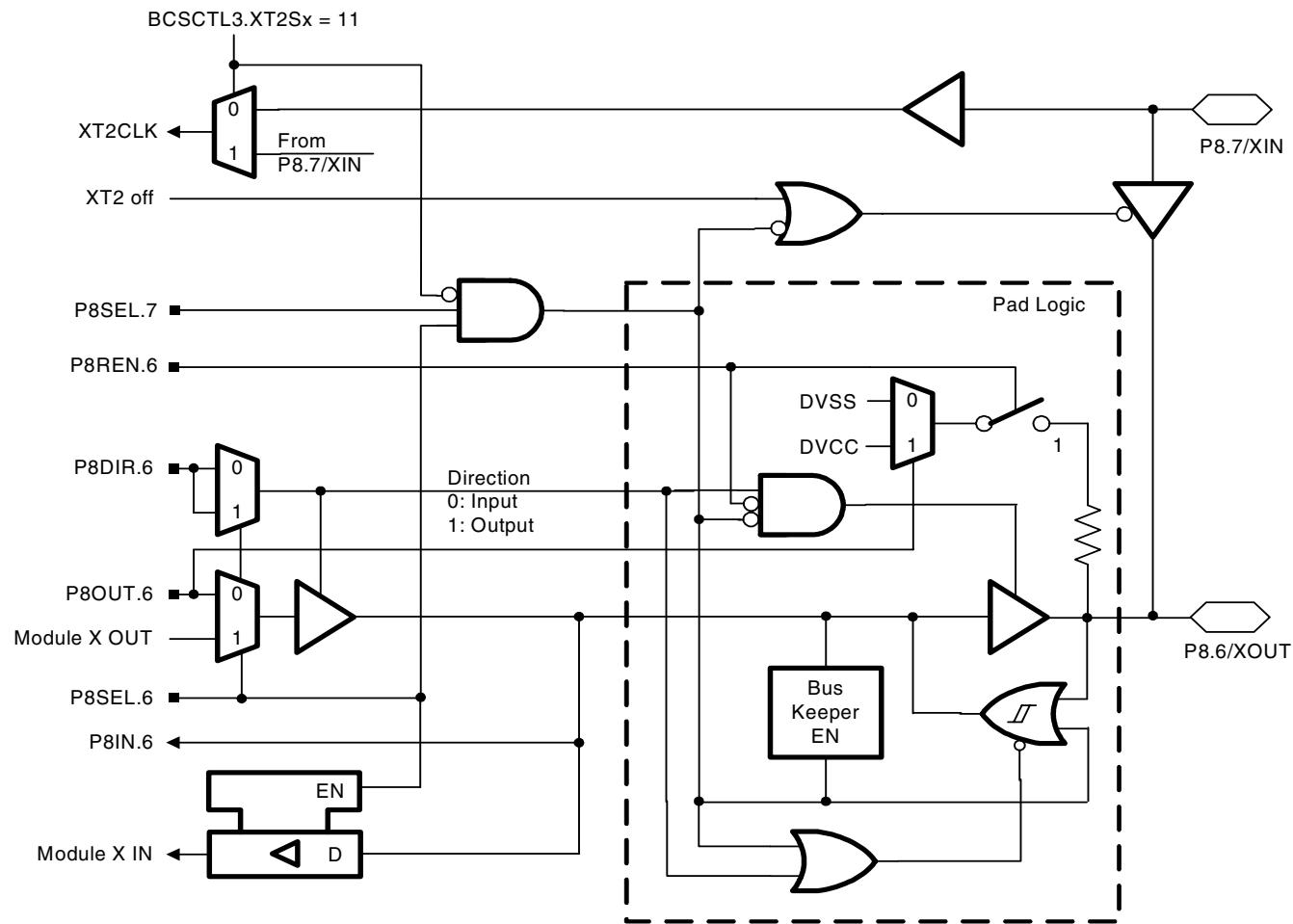
PIN NAME (P8.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P8DIR.x	P8SEL.x
P8.0	0	P8.0 (I/O)	I: 0; O: 1	0
		Input	X	1
P8.1	1	P8.1 (I/O)	I: 0; O: 1	0
		Input	X	1
P8.2	2	P8.2 (I/O)	I: 0; O: 1	0
		Input	X	1
P8.3	3	P8.3 (I/O)	I: 0; O: 1	0
		Input	X	1
P8.4	4	P8.4 (I/O)	I: 0; O: 1	0
		Input	X	1
P8.5	5	P8.5 (I/O)	I: 0; O: 1	0
		Input	X	1

[†] 80-pin devices only

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Port P8 pin schematic: P8.6, input/output with Schmitt trigger†

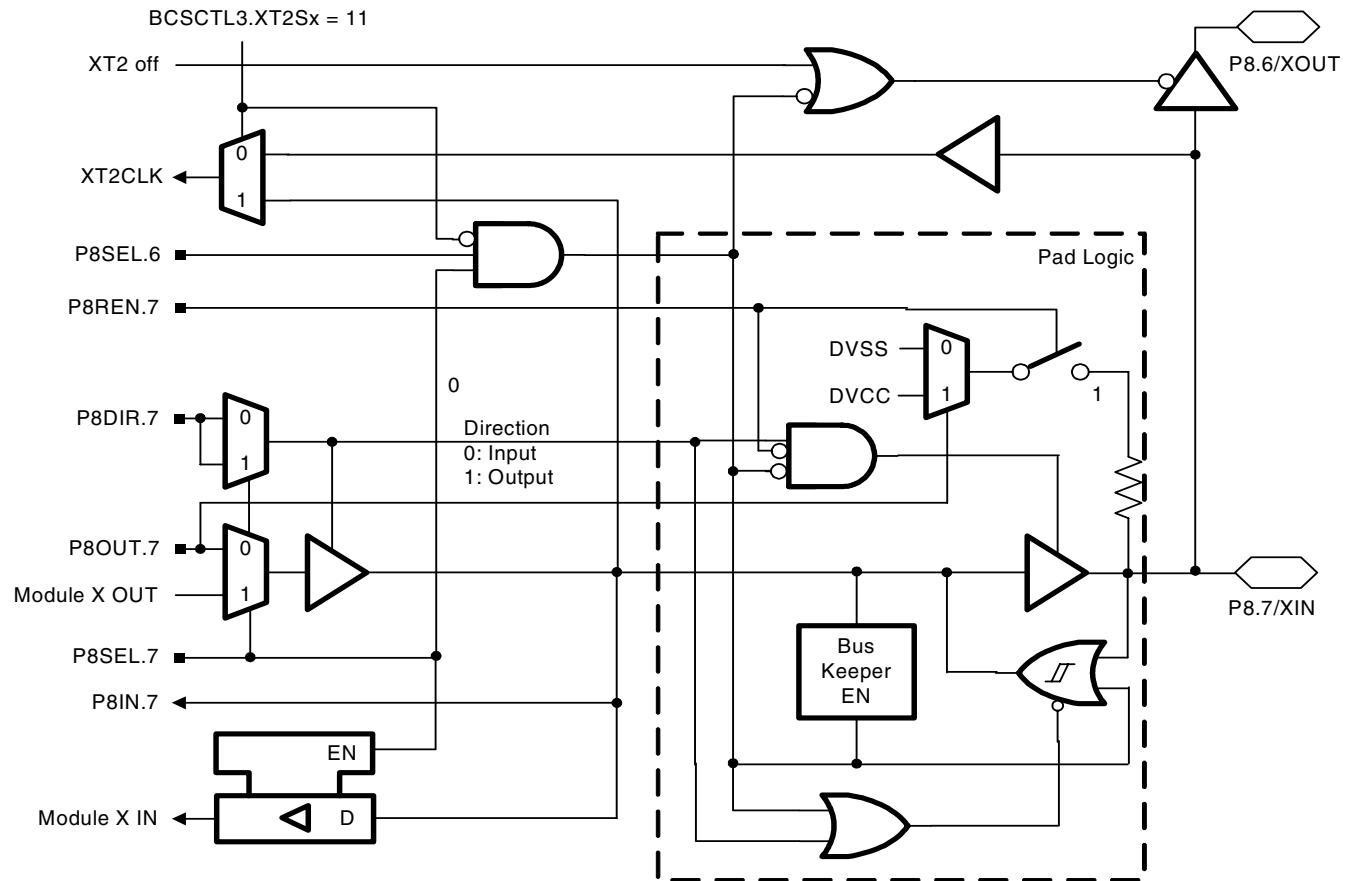


Port P8.6 pin functions†

PIN NAME (P8.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P8DIR.x	P8SEL.x
P8.6/XOUT	6	P8.6 (I/O)	I: 0; O: 1	0
		XOUT (default)	0	1
		DV _{SS}	1	1

† 80-pin devices only

Port P8 pin schematic: P8.7, input/output with Schmitt trigger[†]



Port P8.7 pin functions[†]

PIN NAME (P8.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P8DIR.x	P8SEL.x
P8.7/XIN	7	P8.7 (I/O)	I: 0; O: 1	0
		XIN (default)	0	1
		V _{SS}	1	1

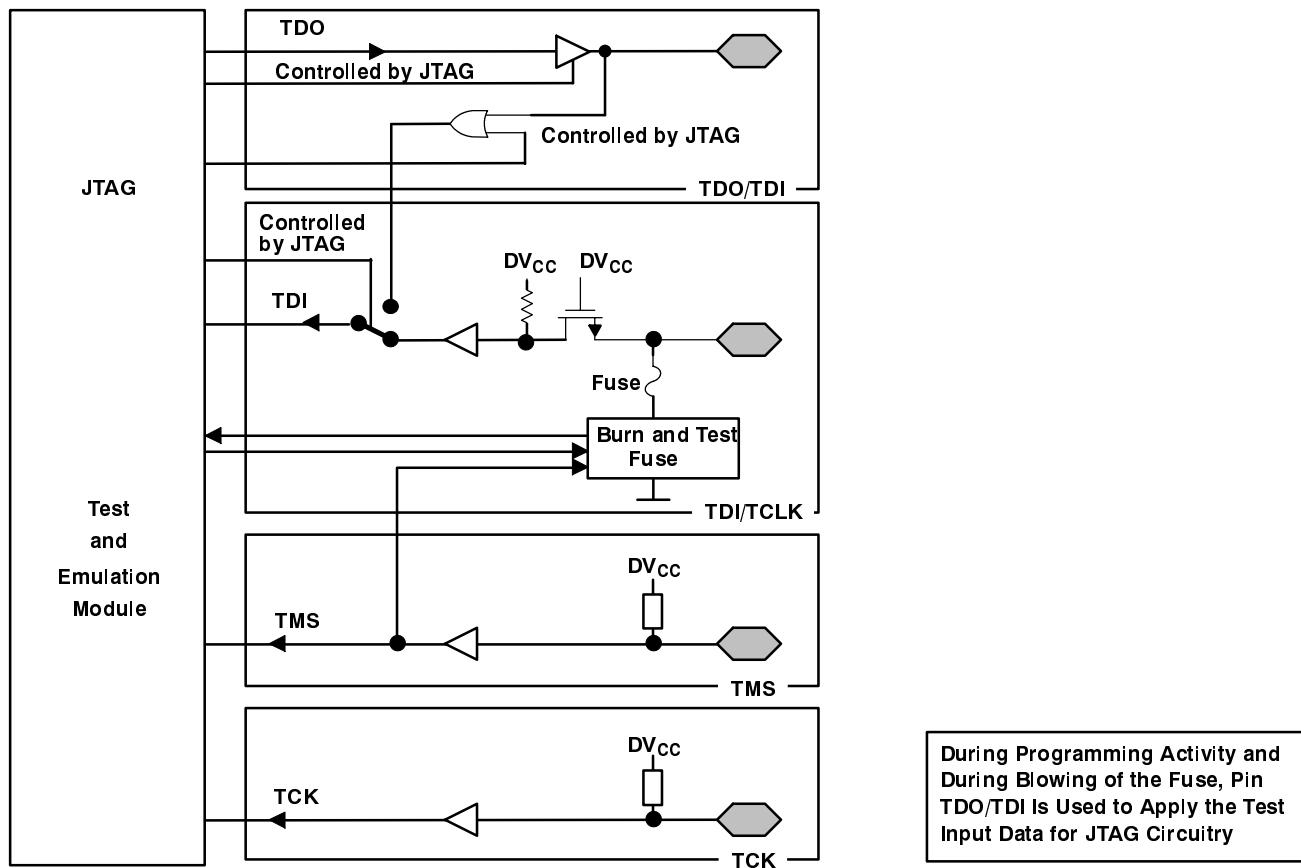
[†] 80-pin devices only

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APPLICATION INFORMATION

JTAG pins: TMS, TCK, TDI/TCLK, TDO/TDI, input/output with Schmitt trigger



APPLICATION INFORMATION

JTAG fuse check mode

MSP430 devices that have the fuse on the TDI/TCLK terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current, I_{TF} , of 1 mA at 3 V or 2.5 mA at 5 V can flow from the TDI/TCLK pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if the TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current flows only when the fuse check mode is active and the TMS pin is in a low state (see Figure 49). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).

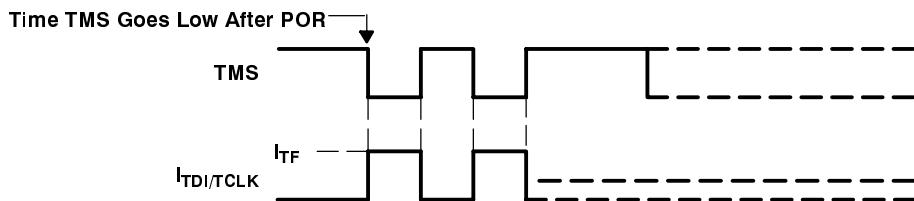


Figure 49. Fuse Check Mode Current

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Data Sheet Revision History

LITERATURE NUMBER	SUMMARY
SLAS541	Product Preview release
SLAS541A	Production Data release Corrected the format and the content shown on the first page. Corrected pin number of P3.6 and P3.7 in 64-pin package in the terminal function list. Corrected the port schematics. Corrected "calibration data" section (page 20). Typos and formatting corrected. Added the figure "typical characteristics - LPM4 current" (Page 33).
SLAS541B	Added preview of MSP430F261x BGA devices.
SLAS541C	Release to market of MSP430F261x BGA devices
SLAS541D	Added the ESD disclaimer (page 1). Added reserved BGA pins to the terminal function list (pages 10 and following). Corrected the references in the output port parameters (page 36). Corrected the cumulative program time of the flash (page 75).
SLAS541E	Corrected LFXT1Sx values in Figures 23 and 24 (page 52). Corrected XT2Sx values in Figures 25 and 26 (page 54). Corrected $t_{CMErase}$ MIN value from 200 ms to 20 ms and removed two notes in the flash memory table (page 75).
SLAS541F	Renamed Tags Used by the ADC Calibration Tags table to Tags used by the TLV Structure (page 20). Changed value of TAG_ADC12_1 from 0x10 to 0x08 in Tags used by the TLV Structure (page 20). Added CAOUT to P1.0/TACLK, Changed Timer_A3.CC10A to Timer_A3.CC11A and Timer_A3.TA0 to Timer_A3.TA1 in P1.2/TA1 row, Changed Timer_A3.CC10A to Timer_A3.CC12A and Timer_A3.TA0 to Timer_A3.TA2 in P1.3/TA2 row in Port P1 (P1.0 to P1.7) pin functions table (page 78). Changed TA0 to Timer_A3.CC10B in P2.2/CAOUT/TA0/CA4 row of Port P2.0, P2.3, P2.4, P2.6 and P2.7 pin functions table (page 80).

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
MSP430F2416TPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2416TPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2416TPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2416TPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2416TZQW	ACTIVE	BGA MI CROSTA R JUNI OR	ZQW	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR
MSP430F2416TZWR	ACTIVE	BGA MI CROSTA R JUNI OR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR
MSP430F2417TPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2417TPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2417TPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2417TPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2417TZQW	ACTIVE	BGA MI CROSTA R JUNI OR	ZQW	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR
MSP430F2417TZWR	ACTIVE	BGA MI CROSTA R JUNI OR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR
MSP430F2418TPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2418TPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2418TPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2418TPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2418TZQW	ACTIVE	BGA MI CROSTA R JUNI OR	ZQW	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR
MSP430F2418TZWR	ACTIVE	BGA MI CROSTA R JUNI OR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR
MSP430F2419TPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2419TPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
MSP430F2419TPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2419TPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2419TZQW	ACTIVE	BGA MI CROSTA R JUNI OR	ZQW	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR
MSP430F2419TZQWR	ACTIVE	BGA MI CROSTA R JUNI OR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR
MSP430F2616TPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2616TPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2616TPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2616TPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2616TZQW	ACTIVE	BGA MI CROSTA R JUNI OR	ZQW	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR
MSP430F2616TZQWR	ACTIVE	BGA MI CROSTA R JUNI OR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR
MSP430F2617TPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2617TPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2617TPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2617TPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2617TZQW	ACTIVE	BGA MI CROSTA R JUNI OR	ZQW	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR
MSP430F2617TZQWR	ACTIVE	BGA MI CROSTA R JUNI OR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR
MSP430F2618TPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2618TPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2618TPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2618TPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2618TZQW	ACTIVE	BGA MI	ZQW	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
		CROSTA R JUNI OR				no Sb/Br)		
MSP430F2618TZQWR	ACTIVE	BGA MI CROSTA R JUNI OR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR
MSP430F2619TPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2619TPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2619TPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2619TPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F2619TZQW	ACTIVE	BGA MI CROSTA R JUNI OR	ZQW	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR
MSP430F2619TZQWR	ACTIVE	BGA MI CROSTA R JUNI OR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF MSP430F2618 :

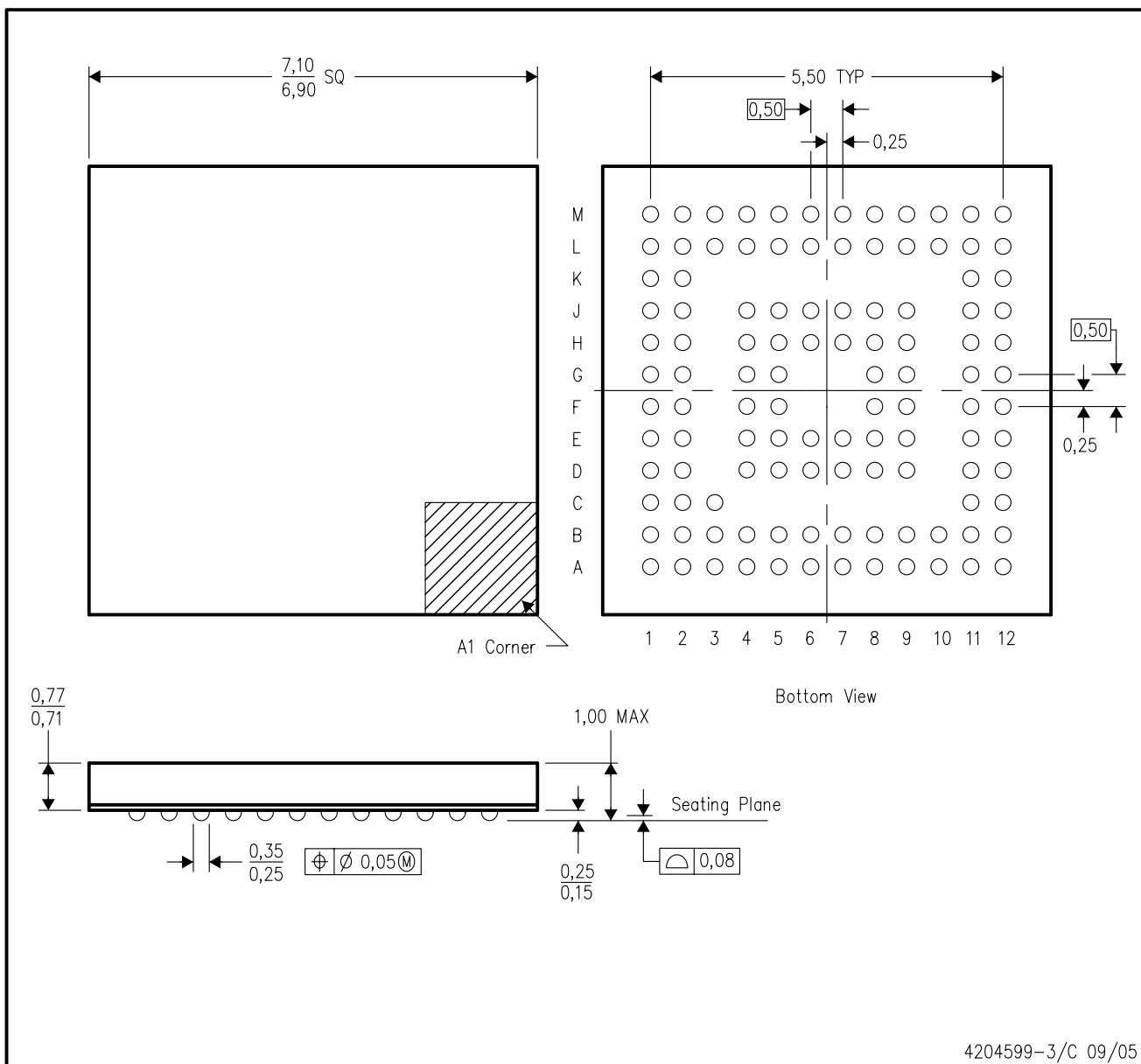
- Enhanced Product: [MSP430F2618-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

ZQW (S-PBGA-N113)

PLASTIC BALL GRID ARRAY

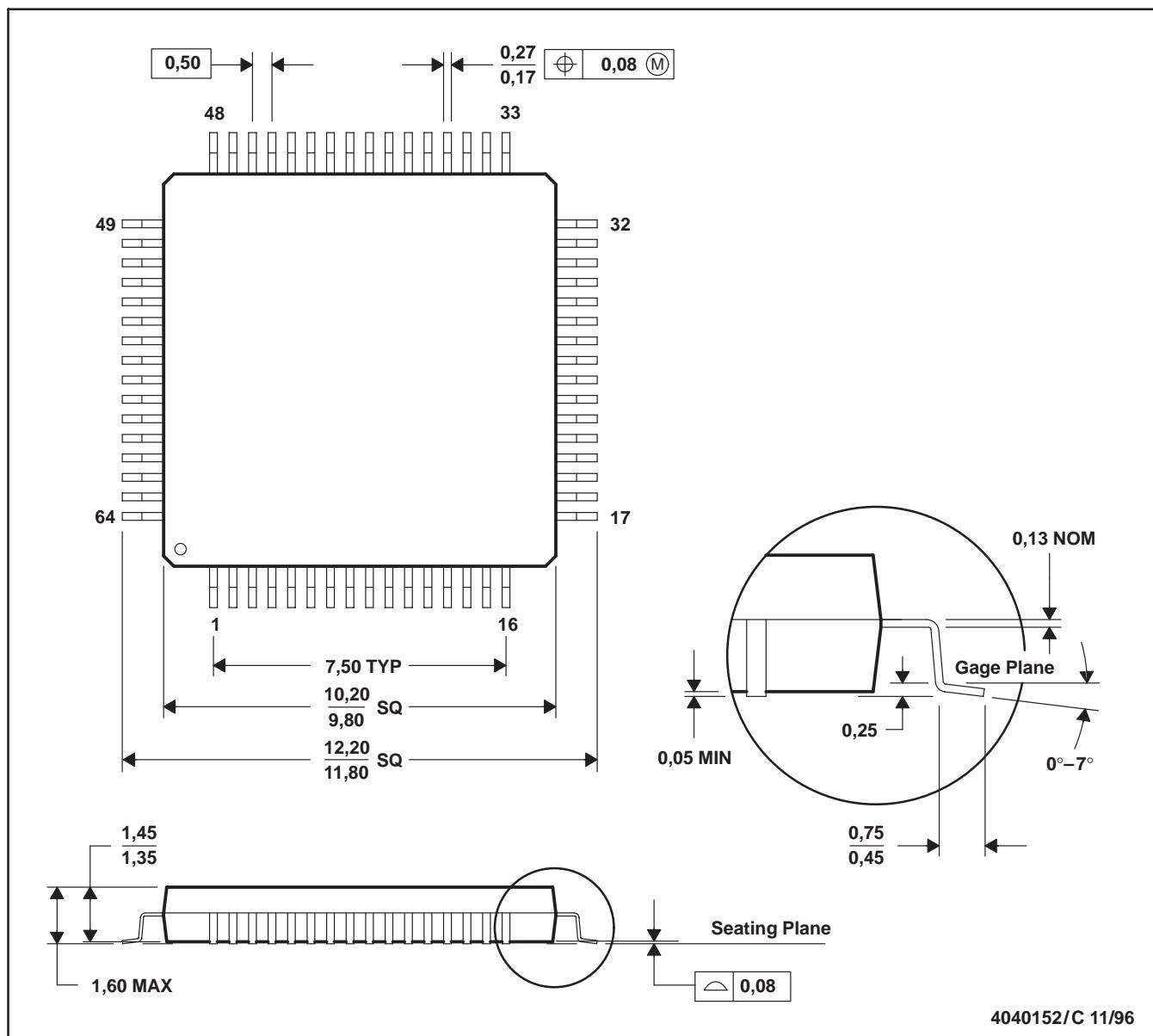


- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Falls within JEDEC MO-225
 - This is a lead-free solder ball design.

4204599-3/C 09/05

PM (S-PQFP-G64)

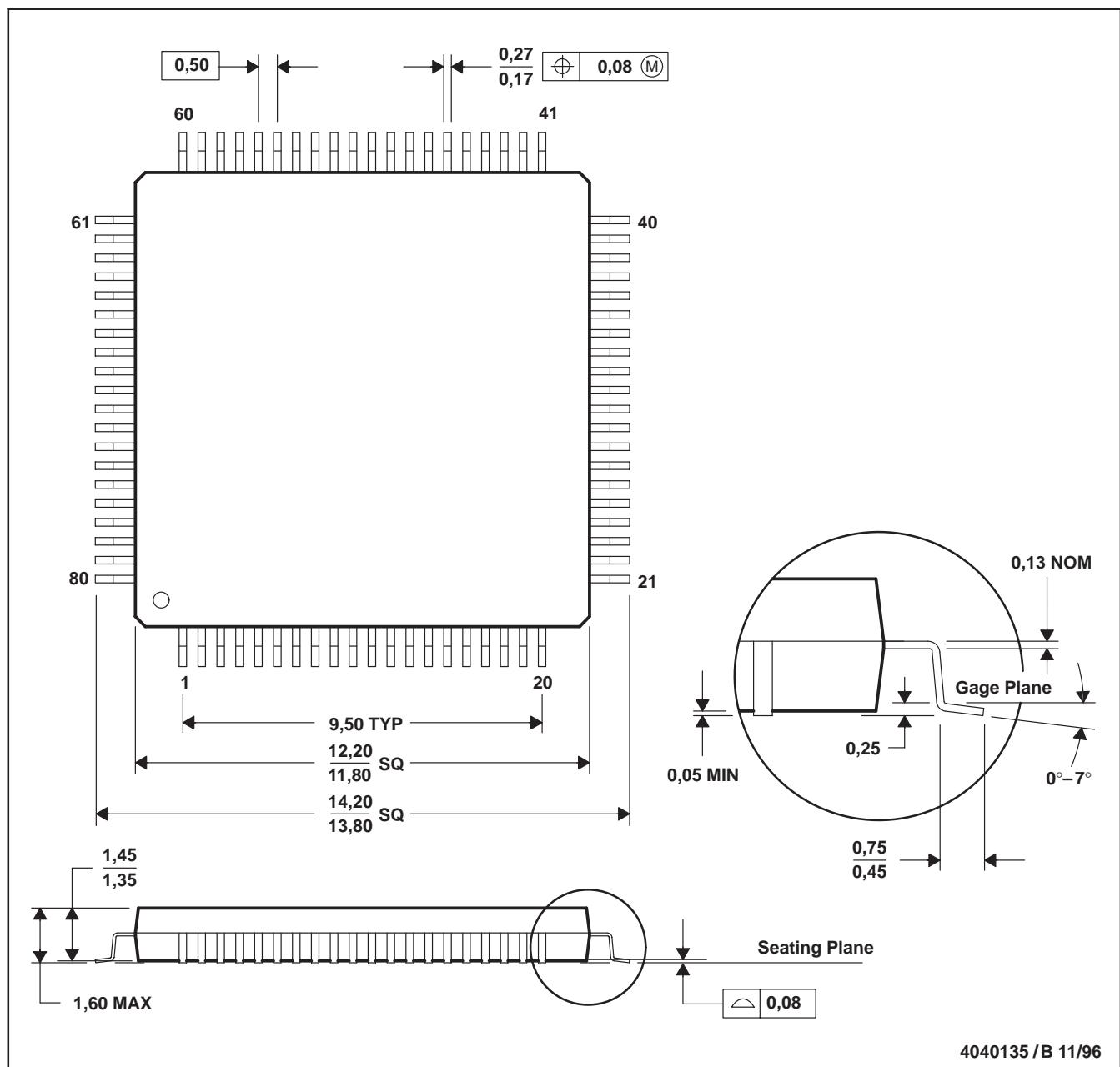
PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-026
 - D. May also be thermally enhanced plastic with leads connected to the die pads.

PN (S-PQFP-G80)

PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026



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