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80960HA/HD/HT
32-BIT HIGH-PERFORMANCE SUPERSCALAR PROCESSOR

- ■ **32-Bit Parallel Architecture**
  - — **Load/Store Architecture**
  - — **Sixteen 32-Bit Global Registers**
  - — **Sixteen 32-Bit Local Registers**
  - — **1.2 Gbyte Internal Bandwidth (75 MHz)**
  - — **On-Chip Register Cache**
- ■ **Processor Core Clock**
  - — **80960HA is 1x Bus Clock**
  - — **80960HD is 2x Bus Clock**
  - — **80960HT is 3x Bus Clock**
- ■ **Binary Compatible with Other 80960 Processors**
- ■ **Issue Up To 150 Million Instructions per Second**
- ■ **High-Performance On-Chip Storage**
  - — **16 Kbyte Four-Way Set-Associative Instruction Cache**
  - — **8 Kbyte Four-Way Set-Associative Data Cache**
  - — **2 Kbyte General Purpose RAM**
  - — **Separate 128-Bit Internal Paths For Instructions/Data**

- ■ **3.3 V Supply Voltage**
  - — **5 V Tolerant Inputs**
  - — **TTL Compatible Outputs**
- ■ **Guarded Memory Unit**
  - — **Provides Memory Protection**
  - — **User/Supervisor Read/Write/Execute**
- ■ **32-Bit Demultiplexed Burst Bus**
  - — **Per-Byte Parity Generation/Checking**
  - — **Address Pipelining Option**
  - — **Fully Programmable Wait State Generator**
  - — **Supports 8-, 16- or 32-Bit Bus Widths**
  - — **160 Mbyte/s External Bandwidth (40 MHz)**
- ■ **High-Speed Interrupt Controller**
  - — **Up to 240 External Interrupts**
  - — **31 Fully Programmable Priorities**
  - — **Separate, Non-maskable Interrupt Pin**
- ■ **Dual On-Chip 32-Bit Timers**
  - — **Auto Reload Capability and One-Shot**
  - — **CLKIN Prescaling, ÷1, 2, 4 or 8**
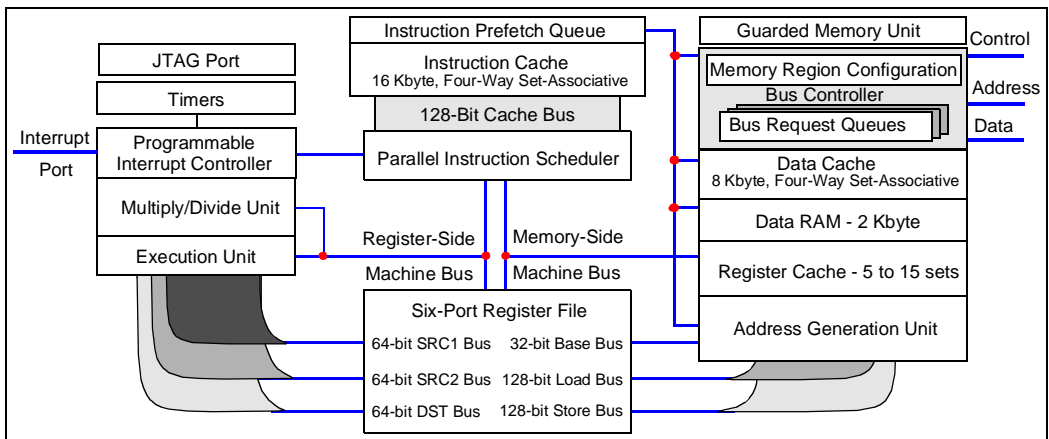- ■ **JTAG Support - IEEE 1149.1 Compliant**

Figure 1. 80960Hx Block Diagram

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80960HA/HD/HT
32-BIT HIGH-PERFORMANCE SUPERSCALAR PROCESSOR

ADVANCE INFORMATION

Contents

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FIGURES

ADVANCE INFORMATION

TABLES

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1.0 ABOUT THIS DOCUMENT

This document describes the parametric performance of Intel's 80960Hx embedded superscalar microprocessors. Detailed descriptions for functional topics — other than parametric performance — are published in the *i960® Hx Microprocessor User's Guide* (272484).

In this document, "80960Hx" and "i960 Hx processor" refer to the products described in Table 1. Throughout this document, information that is specific to each is clearly indicated.

2.0 INTEL'S 80960Hx PROCESSOR

Intel's 80960Hx processor provides new performance levels while maintaining backward compatibility (pin* and software) with the i960 CA/CF processor. This newest member of the family of i960 32-bit, RISC-style, embedded processors allows customers to create scalable designs that meet multiple price and performance points. This is accomplished by providing processors that can run at the bus speed or faster using Intel's clock multiplying technology (Table 1).The 80960Hx core is capable of issuing 150 million instructions per second, using a sophisticated instruction scheduler that allows the processor to sustain a throughput of two instructions every core clock, with a peak performance of three instructions per clock. The 80960Hx-series comprises three processors, which differ in the ratio of core clock speed to external bus speed.

Table 1. 80960Hx Product Description

Product	Core	Voltage	Operating Frequency (bus/core)
80960HA	1x	3.3 V*	25/25, 33/33, 40/40
80960HD	2x	3.3 V*	16/32, 25/50, 33/66, 40/80
80960HT	3x	3.3 V*	20/60, 25/75

NOTE: *Processor inputs are 5 V tolerant.

In addition to expanded clock frequency options, the 80960Hx provides essential enhancements for an emerging class of high-performance embedded applications. Features include a larger instruction cache, data cache, and data RAM than any other

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* Though not drop-in replaceable. Customers can design systems that accept either 80960Hx or Cx processors.

80960 processor to date. It also boasts a 32-bit demultiplexed and pipelined burst bus, fast interrupt mechanism, guarded memory unit, wait state generator, dual programmable timers, ONCE and IEEE 1149.1-compliant boundary scan test and debug support, and new instructions.

2.1 The i960® Processor Family

The i960 processor family is a 32-bit RISC architecture created by Intel to serve the needs of embedded applications. The embedded market includes applications as diverse as industrial automation, avionics, image processing, graphics and communications.

Because all members of the i960 processor family share a common core architecture, i960 applications are code-compatible. Each new processor in the family adds its own special set of functions to the core to satisfy the needs of a specific application or range of applications in the embedded market.

2.2 Key 80960Hx Features

2.2.1 Execution Architecture

Independent instruction paths inside the processor allow the execution of multiple, out-of-sequence instructions per clock. Register and resource scoreboarding interlocks maintain the logical integrity of sequential instructions that are being executed in parallel. To sustain execution of multiple instructions in each clock cycle, the processor decodes multiple instructions in parallel and simultaneously issues these instructions to parallel processing units. The various processing units are then able to independently access instruction operands in parallel from a common register set.

Local Register Cache integrated on-chip provides automatic register management on call/return instructions. Upon a call instruction, the processor allocates a set of local registers for the called procedure, then stores the registers for the previous procedure in the on-chip register cache. As additional procedures are called, the cache stores the associated registers such that the most recently called procedure is the first available by the next return (**ret**) instruction. The processor can store up to fifteen register sets, after which the oldest sets are stored (spilled) into external memory.

ADVANCE INFORMATION

The 80960Hx supports the 80960 architecturally-defined branch prediction mechanism. This allows many branches to execute with no pipeline break. With the 80960Hx's efficient pipeline, a branch can take as few as zero clocks to execute. The maximum penalty for an incorrect prediction is two core clocks.

2.2.2 Pipelined, Burst Bus

A 32-bit high performance bus controller interfaces the 80960Hx core to the external memory and peripherals. The Bus Control Unit features a maximum transfer rate of 160 Mbytes per second (at a 40 MHz external bus clock frequency). A key advantage of this design is its versatility. The user can independently program the physical and logical attributes of system memory. Physical attributes include wait state profile, bus width, and parity. Logical attributes include cacheability and Big or Little Endian byte order. Internally programmable wait states and 16 separately configurable physical memory regions allow the processor to interface with a variety of memory subsystems with minimum system complexity. To reduce the effect of wait states, the bus design is decoupled from the core. This lets the processor execute instructions while the bus performs memory accesses independently.

The Bus Controller's key features include:

- Demultiplexed, Burst Bus to support most efficient DRAM access modes
- Address Pipelining to reduce memory cost while maintaining performance
- 32-, 16- and 8-bit modes to facilitate I/O interfacing
- Full internal wait state generation to reduce system cost
- Little and Big Endian support
- Unaligned Access support implemented in hardware
- Three-deep request queue to decouple the bus from the core
- Independent physical and logical address space characteristics

2.2.3 On-Chip Caches and Data RAM

As shown in Figure 1, the 80960Hx provides generous on-chip cache and storage features to decouple CPU execution from the external bus. The processor includes a 16 Kbyte instruction cache, an 8 Kbyte data cache and 2 Kbytes of Data RAM. The caches are organized as 4-way set associative.

Stores that hit the data cache are written through to memory. The data cache performs write allocation on cache misses. A fifteen-set stack frame cache allows the processor to rapidly allocate and deallocate local registers. All of the on-chip RAM sustains a 4-word (128-bit) access every clock cycle.

2.2.4 Priority Interrupt Controller

The interrupt unit provides the mechanism for the low latency and high throughput interrupt service essential for embedded applications. A priority interrupt controller provides full programmability of 240 interrupt sources with a typical interrupt task switch (latency) time of 17 core clocks. The controller supports 31 priority levels. Interrupts are prioritized and signaled within 10 core clocks of the request. If the interrupt has a higher priority than the processor priority, the context switch to the interrupt routine would typically complete in another 7 bus clocks.

External agents post interrupts via the 8-bit external interrupt port. The Interrupt unit also handles the two internal sources from the Timers. Interrupts can be level- or edge-triggered.

2.2.5 Guarded Memory Unit

The Guarded Memory Unit (GMU) provides memory protection without the address translation found in Memory Management Units. The GMU contains two memory protection schemes: one prevents illegal memory accesses, the other detects memory access violations. Both signal a fault to the processor. The programmable protection modes are: user read, write or execute; and supervisor read, write or execute.

2.2.6 Dual Programmable Timers

The processor provides two independent 32-bit timers, with four programmable clock rates. The user configures the timers via the Timer Unit registers. These registers are memory-mapped within the 80960Hx, addressable on 32-bit boundaries. The timers have a single-shot mode and auto-reload capabilities for continuous operation. Each timer has an independent interrupt request to the processor's interrupt controller.

ADVANCE INFORMATION

2.2.7 Processor Self Test

When a system error is detected, the $\overline{FAIL}$ pin is asserted, a fail code message is driven onto the address bus, and the processor stops execution at the point of failure. The only way to resume normal operation is to perform a RESET operation. Because System Error generation can occur sometime after the bus confidence test and even after initialization during normal processor operation, the $\overline{FAIL}$ pin is HIGH (logic "1") before the detection of a System Error.

The processor uses only one read bus-transaction to signal the fail code message; the address of the bus transaction is the fail code itself. The fail code is of the form: **0xfeffff***nn*; bits 6 to 0 contain a mask recording the possible failures. Bit 7, when set to 1, indicates that the mask contains failures from the internal Built-In Self-Test (BIST); when 0, the mask indicates other failures.

Systems should ignore reserved bits 0 and 1. This is also true for bits 5 and 6 when bit 7 is clear (=0).

The mask is shown in Table 2 and Table 3.

Table 2. Fail Codes For BIST (bit 7 = 1)

Bit	When Set:
6	On-chip Data-RAM failure detected by BIST.
5	Internal Microcode ROM failure detected by BIST.
4	Instruction cache failure detected by BIST.
3	Data cache failure detected by BIST.
2	Local-register cache or processor core failure detected by BIST.
1	Reserved. Always zero.
0	Reserved. Always zero.

Table 3. Remaining Fail Codes (bit 7 = 0)

Bit	When Set:
6	Reserved. Always one.
5	Reserved. Always one.
4	A data structure within the IMI is not aligned to a word boundary.
3	A System Error during normal operation has occurred.
2	The Bus Confidence test has failed.
1	Reserved. Always zero.
0	Reserved. Always zero.

2.3 Instruction Set Summary

Table 4 summarizes the 80960Hx instruction set by logical groupings.

Table 4. 80960Hx Instruction Set

Data Movement	Arithmetic	Logical	Bit / Bit Field / Byte
Load	Add	And	Set Bit
Store	Subtract	Not And	Clear Bit
Move	Multiply	And Not	Not Bit
Load Address	Divide	Or	Alter Bit
Conditional Select[2]	Remainder	Exclusive Or	Scan For Bit
	Modulo	Not Or	Span Over Bit
	Shift	Or Not	Extract
	Extended Shift	Nor	Modify
	Extended Multiply	Exclusive Nor	Scan Byte for Equal
	Extended Divide	Not	Byte Swap[2]
	Add with Carry	Nand	
	Subtract with Carry		
	Rotate		
	Conditional Add[2]		
	Conditional Subtract[2]		
Comparison	**Branch**	**Call/Return**	**Fault**
Compare	Unconditional Branch	Call	Conditional Fault
Conditional Compare	Conditional Branch	Call Extended	Synchronize Faults
Compare and Increment	Compare and Branch	Call System	
Compare and Decrement		Return	
Compare Byte[2]		Branch and Link	
Compare Short[2]			
Test Condition Code			
Check Bit			
Debug	**Processor Mgmt**	**Atomic**	**Cache Control**
Modify Trace Controls	Flush Local Registers	Atomic Add	Instruction Cache Control[1,2]
Mark	Modify Arithmetic Controls	Atomic Modify	Data Cache Control[1,2]
Force Mark	Modify Process Controls		
	Interrupt Enable/Disable[1,2]		
	System Control[1]		

NOTES:

1. 80960Hx extensions to the 80960 core instruction set.
2. 80960Hx extensions to the 80960Cx instruction set.

ADVANCE INFORMATION

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3.0   PACKAGE INFORMATION

This section describes the pins, pinouts and thermal characteristics for the 80960Hx in the 168-pin ceramic Pin Grid Array (PGA) package, 208-pin PowerQuad2[*] (PQ4). For complete package specifications and information, see the Intel *Packaging* Handbook (Order# 240800).

3.1   Pin Descriptions

This section defines the 80960Hx pins. Table 5 presents the legend for interpreting the pin descriptions in Table 6. All pins float while the processor is in the ONCE mode, except TDO, which can be driven active according to normal JTAG specifications.

Table 5. Pin Description Nomenclature

Symbol	Description
I	Input only pin.
O	Output only pin.
I/O	Pin can be input or output.
-	Pin must be connected as indicated for proper device functionality.
S(E)	Synchronous edge sensitive input. This input must meet the setup and hold times relative to CLKIN to ensure proper operation of the processor.
S(L)	Synchronous level sensitive input. This input must meet the setup and hold times relative to CLKIN to ensure proper operation of the processor.
A(E)	Asynchronous edge-sensitive input.
A(L)	Asynchronous level-sensitive input.
H(...)	While the processor bus is in the HOLD state (HLDA asserted), the pin: H(1) is driven to V_{CC} H(0) is driven to V_{SS} H(Z) floats H(Q) continues to be a valid output
B(...)	While the processor is in the bus backoff state ($\overline{BOFF}$ asserted), the pin: B(1) is driven to V_{CC} B(0) is driven to V_{SS} B(Z) floats B(Q) continues to be a valid output
R(...)	While the processor's $\overline{RESET}$ pin is asserted, the pin: R(1) is driven to V_{CC} R(0) is driven to V_{SS} R(Z) floats R(Q) continues to be a valid output

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[*]PowerQuad is a trademark of Amkor Electronics.

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Table 6. 80960Hx Processor Family Pin Descriptions (Sheet 1 of 5)

Name	Type	Description
A31:2	**O** H(Z) B(Z) R(Z)	**ADDRESS BUS** carries the upper 30 bits of the physical address. A31 is the most significant address bit and A2 is the least significant. During a bus access, A31:2 identify all external addresses to word (4-byte) boundaries. The byte enable signals indicate the selected byte in each word. During burst accesses, A3 and A2 increment to indicate successive addresses.
D31:0	**I/O** S(L) H(Z) B(Z) R(Z)	**DATA BUS** carries 32, 16, or 8-bit data quantities depending on bus width configuration. The least significant bit of the data is carried on D0 and the most significant on D31. The lower 8 data lines (D7:0) are used when the bus is configured for 8-bit data. When configured for 16-bit data, D15:0 are used.
DP3:0	**I/O** S(L) H(Z) B(Z) R(Z)	**DATA PARITY** carries parity information for the data bus. Each parity bit is assigned a group of 8 data bus pins as follows: DP3 generates/checks parity for D31:24 DP2 generates/checks parity for D23:16 DP1 generates/checks parity for D15:8 DP0 generates/checks parity for D7:0 Parity information is generated for a processor write cycle and is checked for a processor read cycle. Parity checking and polarity are programmable. Parity generation/checking is only performed for the size of the data accessed.
$\overline{\text{PCHK}}$	**O** H(Q) B(Q) R(1)	**PARITY CHECK** indicates the result of a parity check operation. An asserted $\overline{\text{PCHK}}$ indicates that the previous bus read access resulted in a parity check error.
$\overline{\text{BE3:0}}$	**O** H(Z) B(Z) R(1)	**BYTE ENABLES** select which of the four bytes addressed by A31:2 are active during a bus access. Byte enable encoding is dependent on the bus width of the memory region accessed: *32-bit bus:* $\overline{\text{BE3}}$ enables D31:24 $\overline{\text{BE2}}$ enables D23:16 $\overline{\text{BE1}}$ enables D15:8 $\overline{\text{BE0}}$ enables D7:0 *16-bit bus:* $\overline{\text{BE3}}$ becomes Byte High Enable (enables D15:8) $\overline{\text{BE2}}$ is not used (state is undefined) $\overline{\text{BE1}}$ becomes Address Bit 1 (A1) $\overline{\text{BE0}}$ becomes Byte Low Enable (enables D7:0) *8-bit bus:* $\overline{\text{BE3}}$ is not used (state is undefined) $\overline{\text{BE2}}$ is not used (state is undefined) $\overline{\text{BE1}}$ Address Bit 1 (A1) $\overline{\text{BE0}}$ Address Bit 0 (A0)
W/$\overline{\text{R}}$	**O** H(Z) B(Z) R(0)	**WRITE/READ** is low for read accesses and high for write accesses. W/$\overline{\text{R}}$ becomes valid during the address phase of a bus cycle and remains valid until the end of the cycle for non-pipelined accesses. For pipelined accesses, W/$\overline{\text{R}}$ changes state when the next address is presented. 0= Read 1= Write

ADVANCE INFORMATION

Table 6. 80960Hx Processor Family Pin Descriptions (Sheet 2 of 5)

Name	Type	Description
D/$\overline{\text{C}}$	O H(Z) B(Z) R(0)	**DATA/CODE** indicates that a bus access is a data access or an instruction access. D/$\overline{\text{C}}$ has the same timing as W/$\overline{\text{R}}$. 0 = Code 1 = Data
$\overline{\text{SUP}}$	O H(Z) B(Z) R(1)	**SUPERVISOR ACCESS** indicates whether the current bus access originates from a request issued while in supervisor mode or user mode. $\overline{\text{SUP}}$ can be used by the memory subsystem to isolate supervisor code and data structures from non-supervisor access. 0 = Supervisor Mode 1 = User Mode
$\overline{\text{ADS}}$	O H(Z) B(Z) R(1)	**ADDRESS STROBE** indicates a valid address and the start of a new bus access. $\overline{\text{ADS}}$ is asserted for the first clock of a bus access.
$\overline{\text{READY}}$	I S(L)	$\overline{\text{READY}}$, when enabled for a memory region, is asserted by the memory subsystem to indicate the completion of a data transfer. $\overline{\text{READY}}$ is used to indicate that read data on the bus is valid, or that a write transfer has completed. $\overline{\text{READY}}$ works in conjunction with the internal wait state generator to accommodate various memory speeds. $\overline{\text{READY}}$ is sampled after any programmed wait states: • During each data cycle of a burst access • During the data cycle of a non-burst access
$\overline{\text{BTERM}}$	I S(L)	**BURST TERMINATE**, when enabled for a memory region, is asserted by the memory subsystem to terminate a burst access in progress. When $\overline{\text{BTERM}}$ is asserted, the current burst access is terminated and another address cycle occurs.
$\overline{\text{WAIT}}$	O H(Z) B(Z) R(1)	**WAIT** indicates the status of the internal wait-state generator. $\overline{\text{WAIT}}$ is asserted when the internal wait state generator generates N_{WAD}, N_{RAD}, N_{WDD} and N_{RDD} wait states. $\overline{\text{WAIT}}$ can be used to derive a write data strobe.
$\overline{\text{BLAST}}$	O H(Z) B(Z) R(1)	**BURST LAST** indicates the last transfer in a bus access. $\overline{\text{BLAST}}$ is asserted in the last data transfer of burst and non-burst accesses after the internal wait-state generator reaches zero. $\overline{\text{BLAST}}$ remains active as long as wait states are inserted via the $\overline{\text{READY}}$ pin. $\overline{\text{BLAST}}$ becomes inactive after the final data transfer in a bus cycle.
DT/$\overline{\text{R}}$	O H(Z) B(Z) R(0)	**DATA TRANSMIT/RECEIVE** indicates direction for data transceivers. DT/$\overline{\text{R}}$ is used with $\overline{\text{DEN}}$ to provide control for data transceivers connected to the data bus. DT/$\overline{\text{R}}$ is driven low to indicate the processor expects data (a read cycle). DT/$\overline{\text{R}}$ is driven high when the processor is "transmitting" data (a store cycle). DT/$\overline{\text{R}}$ only changes state when $\overline{\text{DEN}}$ is high. 0 = Data Receive 1 = Data Transmit

ADVANCE INFORMATION

Table 6. 80960Hx Processor Family Pin Descriptions (Sheet 3 of 5)

Name	Type	Description
$\overline{\text{DEN}}$	O H(Z) B(Z) R(1)	**DATA ENABLE** indicates data transfer cycles during a bus access. $\overline{\text{DEN}}$ is asserted at the start of the first data cycle in a bus access and de-asserted at the end of the last data cycle. $\overline{\text{DEN}}$ remains asserted for an entire bus request, even when that request spans several bus accesses. For example, a ldq instruction starting at an unaligned quad word boundary is one bus request spanning at least two bus accesses. $\overline{\text{DEN}}$ remains asserted throughout all the accesses (including $\overline{\text{ADS}}$ states) and de-asserts when the lqd instruction request is satisfied. $\overline{\text{DEN}}$ is used with DT/$\overline{\text{R}}$ to provide control for data transceivers connected to the data bus. $\overline{\text{DEN}}$ remains asserted for sequential reads from pipelined memory regions.
$\overline{\text{LOCK}}$	O H(Z) B(Z) R(1)	**BUS LOCK** indicates that an atomic read-modify-write operation is in progress. $\overline{\text{LOCK}}$ may be used by the memory subsystem to prevent external agents from accessing memory that is currently involved in an atomic operation (e.g., a semaphore). $\overline{\text{LOCK}}$ is asserted in the first clock of an atomic operation and de-asserted when $\overline{\text{BLAST}}$ is deasserted in the last bus cycle.
HOLD	I S(L)	**HOLD REQUEST** signals that an external agent requests access to the processor's address, data, and control buses. When HOLD is asserted, the processor: • Completes the current bus request. • Asserts HOLDA and floats the address, data, and control buses. When HOLD is deasserted, the HOLDA pin is deasserted and the processor reassumes control of the address, data, and control pins.
HOLDA	O H(1) B(0) R(Q)	**HOLD ACKNOWLEDGE** indicates to an external master that the processor has relinquished control of the bus. The processor grants HOLD requests and enters the HOLDA state while the $\overline{\text{RESET}}$ pin is asserted. HOLDA is never granted while $\overline{\text{LOCK}}$ is asserted.
$\overline{\text{BOFF}}$	I S(L)	**BUS BACKOFF** forces the processor to immediately relinquish control of the bus on the next clock cycle. When $\overline{\text{READY}}$/$\overline{\text{BTERM}}$ is enabled and: • When $\overline{\text{BOFF}}$ is asserted, the address, data, and control buses are floated on the next clock cycle and the current access is aborted. • When $\overline{\text{BOFF}}$ is deasserted, the processor resumes by regenerating the aborted bus access. See Figure 16, Bus Backoff (BOFF) Timings (pg. 38), for $\overline{\text{BOFF}}$ timing requirements.
BREQ	O H(Q) B(Q) R(0)	**BUS REQUEST** indicates that a bus request is pending in the bus controller, but the processor *is not stalled* pending the result of the bus operation. BREQ can be used with BSTALL to indicate to an external bus arbiter the processor's bus ownership requirements.
BSTALL	O H(Q) B(Q) R(0)	**BUS STALL** indicates that the processor has stalled pending the result of a request in the bus controller. When BSTALL is asserted, the processor *must* regain bus ownership to continue processing (i.e., it can no longer execute strictly out of on-chip cache memory).

ADVANCE INFORMATION

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Table 6. 80960Hx Processor Family Pin Descriptions (Sheet 4 of 5)

Name	Type	Description
CT3:0	O H(Z) B(Z) R(Z)	**CYCLE TYPE** indicates the type of bus cycle currently being started or processor state. CT3:0 encoding follows: Cycle Type .... $\overline{\text{ADS}}$ ..... CT3:0 Program-initiated access using 8-bit bus ..... 0 ..... 0000 Program-initiated access using 16-bit bus ... 0 ..... 0001 Program-initiated access using 32-bit bus ... 0 ..... 0010 Event-initiated access using 8-bit bus .... 0 ..... 0100 Event-initiated access using 16-bit bus ...... 0 ..... 0101 Event-initiated access using 32-bit bus ...... 0 ..... 0110 Reserved .... 0 ..... 0X11 Reserved for future products .... 0 ..... 1XXX Reserved .... 1 XXXX
$\overline{\text{XINT7:0}}$	I A(E) A(L)	**EXTERNAL INTERRUPT** pins are used to request interrupt service. These pins can be configured in three modes: *Dedicated Mode:* Each pin is assigned a dedicated interrupt level. Dedicated inputs can be programmed to be level (low or high) or edge (rising or falling) sensitive. *Expanded Mode:* All eight pins act as a vectored interrupt source. The interrupt pins are level sensitive in this mode. *Mixed Mode:* The $\overline{\text{XINT7:5}}$ pins act as dedicated sources and the $\overline{\text{XINT4:0}}$ pins act as the five most significant bits of a vectored source. The least significant bits of the vectored source are set to "010" internally.
$\overline{\text{NMI}}$	I A(E)	**NON-MASKABLE INTERRUPT** causes a non-maskable interrupt event to occur. $\overline{\text{NMI}}$ is the highest priority interrupt source. $\overline{\text{NMI}}$ is falling edge triggered.
CLKIN	I	**CLOCK INPUT** provides the time base for the 80960Hx. All internal circuitry is synchronized to CLKIN. All input and output timings are specified relative to CLKIN. For the 80960HD, the 2x internal clock is derived by multiplying the CLKIN frequency by 2. For the 80960HT, the 3x internal clock is derived by multiplying the CLKIN frequency by 3.
$\overline{\text{RESET}}$	I A(L)	$\overline{\text{RESET}}$ forces the device into reset. $\overline{\text{RESET}}$ causes all external and internal signals to return to their reset state (if defined). The rising edge of $\overline{\text{RESET}}$ starts the processor boot sequence.
STEST	I S(L)	**SELF TEST**, when asserted during the rising edge of $\overline{\text{RESET}}$, causes the processor to execute its built in self-test.
$\overline{\text{FAIL}}$	O H(Q) B(Q) R(0) P(1)	$\overline{\text{FAIL}}$ indicates a failure of the processor's built-in self-test performed during initialization. $\overline{\text{FAIL}}$ is asserted immediately out of reset and toggles during self-test to indicate the status of individual tests. If self-test passes, $\overline{\text{FAIL}}$ is de-asserted and the processor branches to the user's initialization code. Should self-test fail, the $\overline{\text{FAIL}}$ pin is asserted and the processor ceases execution.
$\overline{\text{ONCE}}$	I	**ON-CIRCUIT EMULATION** control: the processor samples this pin during reset. If it is asserted low at the end of reset, the processor enters ONCE mode. In ONCE mode, the processor stops all clocks and floats all output pins except the TDO pin. $\overline{\text{ONCE}}$ includes a nominal 80 kΩ internal pull-up resistor.
TCK	I	**TEST CLOCK** provides the clocking function for IEEE 1149.1 Boundary Scan testing.

ADVANCE INFORMATION

Table 6. 80960Hx Processor Family Pin Descriptions (Sheet 5 of 5)

Name	Type	Description
TDI	I	**TEST DATA INPUT** is the serial input pin for IEEE 1149.1 Boundary Scan testing.
TDO	O	**TEST DATA OUTPUT** is the serial output pin for IEEE 1149.1 Boundary Scan testing. ONCE does not disable this pin.
$\overline{\text{TRST}}$	I	**TEST RESET** asynchronously resets the Test Access Port (TAP) controller. $\overline{\text{TRST}}$ must be held low at least 10,000 clock cycles after power-up. One method is to provide $\overline{\text{TRST}}$ with a separate power-on-reset circuit. $\overline{\text{TRST}}$ includes a nominal 65 kΩ internal pull-up resistor. Pull this pin low when not in use.
TMS	I	**TEST MODE SELECT** is sampled at the rising edge of TCK. TCK controls the sequence of TAP controller state changes for IEEE 1149.1 Boundary Scan testing. TMS includes a nominal 80 kΩ internal pull-up resistor.
V_{CC5}	I	**5 V REFERENCE VOLTAGE** input is the reference voltage for the 5 V-tolerant I/O buffers. This signal should be connected to +5 V for use with inputs which exceed 3.3 V. If all inputs are from 3.3 V components, this pin should be connected to 3.3 V.
V_{CCPLL}	I	**PLL VOLTAGE** is the +3.3 VDC analog input for the PLL.
VOLDET	O	**VOLTAGE DETECT** signal allows external system logic to distinguish between a 5 V 80960Cx processor and the 3.3 V 80960Hx processor. This signal is active low for a 3.3 V 80960Hx (it is high impedance for 5 V 80960Cx). This pin is available only on the PGA version. 0 = 80960Hx 1 = 80960Cx

ADVANCE INFORMATION

3.2 80960Hx Mechanical Data

3.2.1 80960Hx PGA Pinout

Figures 2 depicts the complete 80960Hx PGA pinout as viewed from the top side of the component (i.e., pins facing down). Figures 3 shows the complete 80960Hx PGA pinout as viewed from the pin-side of the package (i.e., pins facing up). Table 8 lists the 80960Hx pin names with package location. See Section 4.3, Recommended Connections (pg. 27) for specifications and recommended connections.
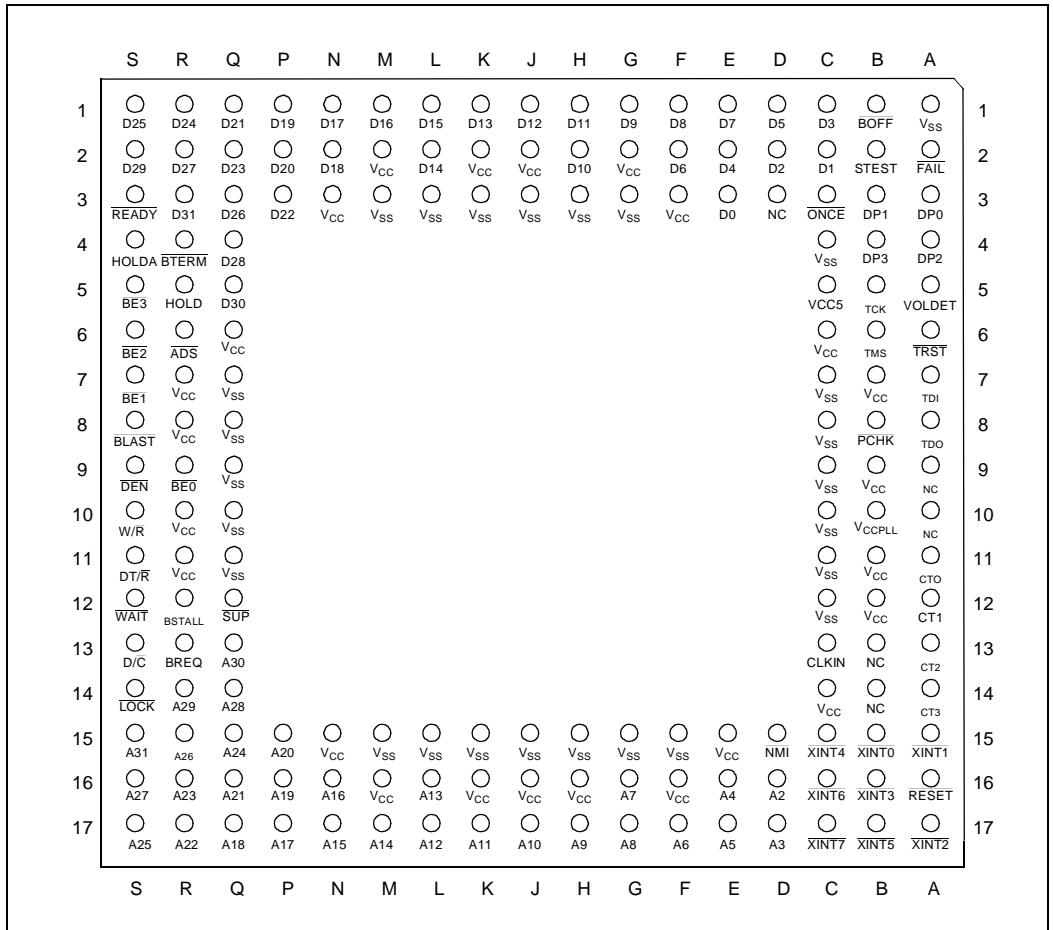
Figure 2. 80960Hx 168-Pin PGA Pinout — View from Top (Pins Facing Down)
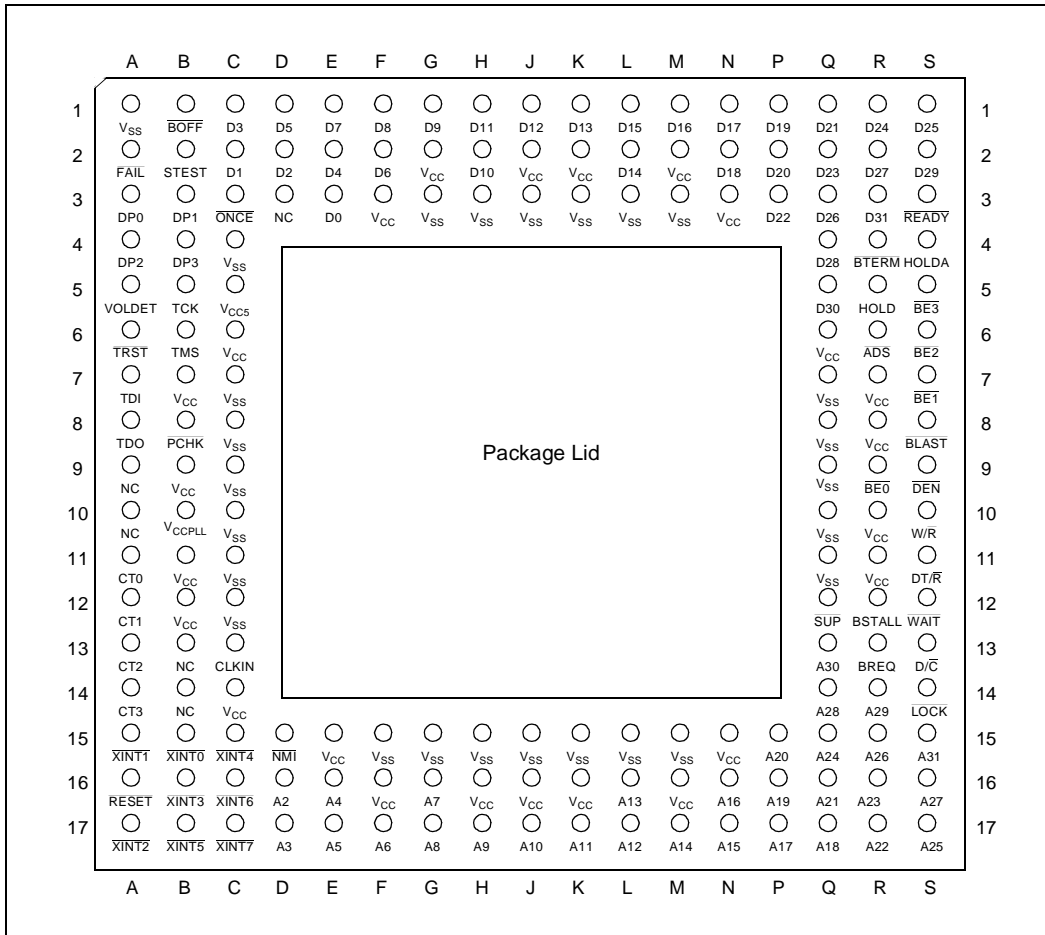
Figure 3. 80960Hx 168-Pin PGA Pinout — View from Bottom (Pins Facing Up)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S
1	V_{SS}	$\overline{BOFF}$	D3	D5	D7	D8	D9	D11	D12	D13	D15	D16	D17	D19	D21	D24	D25
2	$\overline{FAIL}$	STEST	D1	D2	D4	D6	V_{CC}	D10	V_{CC}	V_{CC}	D14	V_{CC}	D18	D20	D23	D27	D29
3	DP0	DP1	$\overline{ONCE}$	NC	D0	V_{CC}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{CC}	D22	D26	D31	$\overline{READY}$
4	DP2	DP3	V_{SS}					Package Lid							D28	BTERM	HOLDA
5	VOLDET	TCK	V_{CC5}												D30	HOLD	$\overline{BE3}$
6	$\overline{TRST}$	TMS	V_{CC}												V_{CC}	$\overline{ADS}$	BE2
7	TDI	V_{CC}	V_{SS}												V_{SS}	V_{CC}	$\overline{BE1}$
8	TDO	PCHK	V_{SS}												V_{SS}	V_{CC}	BLAST
9	NC	V_{CC}	V_{SS}												V_{SS}	$\overline{BE0}$	$\overline{DEN}$
10	NC	V_{CCPLL}	V_{SS}												V_{SS}	V_{CC}	W/R
11	CT0	V_{CC}	V_{SS}												V_{SS}	V_{CC}	$DT/\overline{R}$
12	CT1	V_{CC}	V_{SS}												SUP	BSTALL	WAIT
13	CT2	NC	CLKIN												A30	BREQ	$D/\overline{C}$
14	CT3	NC	V_{CC}												A28	A29	$\overline{LOCK}$
15	$\overline{XINT1}$	$\overline{XINT0}$	$\overline{XINT4}$	$\overline{NMI}$	V_{CC}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{CC}	A20	A24	A26	A31
16	RESET	$\overline{XINT3}$	$\overline{XINT6}$	A2	A4	V_{CC}	A7	V_{CC}	V_{CC}	V_{CC}	A13	V_{CC}	A16	A19	A21	A23	A27
17	$\overline{XINT2}$	$\overline{XINT5}$	$\overline{XINT7}$	A3	A5	A6	A8	A9	A10	A11	A12	A14	A15	A17	A18	A22	A25

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Table 7. 80960Hx 168-Pin PGA Pinout — Signal Name Order (Sheet 1 of 2)

Signal Name	PGA Pin	Signal Name	PGA Pin	Signal Name	PGA Pin	Signal Name	PGA Pin
A2	D16	$\overline{ADS}$	R6	D14	L2	$\overline{LOCK}$	S14
A3	D17	$\overline{BE0}$	R9	D15	L1	NC	A9
A4	E16	$\overline{BE1}$	S7	D16	M1	NC	A10
A5	E17	$\overline{BE2}$	S6	D17	N1	NC	B13
A6	F17	$\overline{BE3}$	S5	D18	N2	NC	B14
A7	G16	$\overline{BLAST}$	S8	D19	P1	NC	D3
A8	G17	$\overline{BOFF}$	B1	D20	P2	$\overline{NMI}$	D15
A9	H17	BREQ	R13	D21	Q1	$\overline{ONCE}$	C3
A10	J17	BSTALL	R12	D22	P3	$\overline{PCHK}$	B8
A11	K17	$\overline{BTERM}$	R4	D23	Q2	$\overline{READY}$	S3
A12	L17	CLKIN	C13	D24	R1	$\overline{RESET}$	A16
A13	L16	CT0	A11	D25	S1	STEST	B2
A14	M17	CT1	A12	D26	Q3	$\overline{SUP}$	Q12
A15	N17	CT2	A13	D27	R2	TCK	B5
A16	N16	CT3	A14	D28	Q4	TDI	A7
A17	P17	$D/\overline{C}$	S13	D29	S2	TDO	A8
A18	Q17	D0	E3	D30	Q5	TMS	B6
A19	P16	D1	C2	D31	R3	$\overline{TRST}$	A6
A20	P15	D2	D2	DEN	S9	V$_{CC}$	B7
A21	Q16	D3	C1	DP0	A3	V$_{CC}$	B9
A22	R17	D4	E2	DP1	B3	V$_{CC}$	B11
A23	R16	D5	D1	DP2	A4	V$_{CC}$	B12
A24	Q15	D6	F2	DP3	B4	V$_{CC}$	C6
A25	S17	D7	E1	$DT/\overline{R}$	S11	V$_{CC}$	C14
A26	R15	D8	F1	$\overline{FAIL}$	A2	V$_{CC}$	E15
A27	S16	D9	G1	—	—	V$_{CC}$	F3
A28	Q14	D10	H2	—	—	V$_{CC}$	F16
A29	R14	D11	H1	—	—	V$_{CC}$	G2
A30	Q13	D12	J1	HOLD	R5	V$_{CC}$	H16
A31	S15	D13	K1	HOLDA	S4	V$_{CC}$	J2
V$_{CC}$	J16	V$_{CCPLL}$	B10	V$_{SS}$	H3	V$_{SS}$	Q10
V$_{CC}$	K2	VOLDET	A5	V$_{SS}$	H15	V$_{SS}$	Q11
V$_{CC}$	K16	V$_{SS}$	A1	V$_{SS}$	J3	$W/\overline{R}$	S10

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Table 7. 80960Hx 168-Pin PGA Pinout — Signal Name Order (Sheet 2 of 2)

Signal Name	PGA Pin	Signal Name	PGA Pin	Signal Name	PGA Pin	Signal Name	PGA Pin
V_{CC}	M2	V_{SS}	C4	V_{SS}	J15	$\overline{WAIT}$	S12
V_{CC}	M16	V_{SS}	C7	V_{SS}	K3	$\overline{XINT0}$	B15
V_{CC}	N3	V_{SS}	C8	V_{SS}	K15	$\overline{XINT1}$	A15
V_{CC}	N15	V_{SS}	C9	V_{SS}	L3	$\overline{XINT2}$	A17
V_{CC}	Q6	V_{SS}	C10	V_{SS}	L15	$\overline{XINT3}$	B16
V_{CC}	R7	V_{SS}	C11	V_{SS}	M3	$\overline{XINT4}$	C15
V_{CC}	R8	V_{SS}	C12	V_{SS}	M15	$\overline{XINT5}$	B17
V_{CC}	R10	V_{SS}	F15	V_{SS}	Q7	$\overline{XINT6}$	C16
V_{CC}	R11	V_{SS}	G3	V_{SS}	Q8	$\overline{XINT7}$	C17
V_{CC5}	C5	V_{SS}	G15	V_{SS}	Q9	—	—

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Table 8. 80960Hx 168-Pin PGA Pinout — Pin Number Order (Sheet 1 of 2)

PGA Pin	Signal Name	PGA Pin	Signal Name	PGA Pin	Signal Name	PGA Pin	Signal Name
A1	V_{SS}	B14	NC	E15	V_{CC}	K15	V_{SS}
A2	$\overline{FAIL}$	B15	$\overline{XINT0}$	E16	A4	K16	V_{CC}
A3	DP0	B16	$\overline{XINT3}$	E17	A5	K17	A11
A4	DP2	B17	$\overline{XINT5}$	F1	D8	L1	D15
A5	VOLDET	C1	D3	F2	D6	L2	D14
A6	$\overline{TRST}$	C2	D1	F3	V_{CC}	L3	V_{SS}
A7	TDI	C3	$\overline{ONCE}$	F15	V_{SS}	L15	V_{SS}
A8	TDO	C4	V_{SS}	F16	V_{CC}	L16	A13
A9	NC	C5	VCC5	F17	A6	L17	A12
A10	NC	C6	V_{CC}	G1	D9	M1	D16
A11	CT0	C7	V_{SS}	G2	V_{CC}	M2	V_{CC}
A12	CT1	C8	V_{SS}	G3	V_{SS}	M3	V_{SS}
A13	CT2	C9	V_{SS}	G15	V_{SS}	M15	V_{SS}
A14	CT3	C10	V_{SS}	G16	A7	M16	V_{CC}
A15	$\overline{XINT1}$	C11	V_{SS}	G17	A8	M17	A14
A16	$\overline{RESET}$	C12	V_{SS}	H1	D11	N1	D17
A17	$\overline{XINT2}$	C13	CLKIN	H2	D10	N2	D18
B1	$\overline{BOFF}$	C14	V_{CC}	H3	V_{SS}	N3	V_{CC}
B2	STEST	C15	$\overline{XINT4}$	H15	V_{SS}	N15	V_{CC}
B3	DP1	C16	$\overline{XINT6}$	H16	V_{CC}	N16	A16
B4	DP3	C17	$\overline{XINT7}$	H17	A9	N17	A15
B5	TCK	D1	D5	J1	D12	P1	D19
B6	TMS	D2	D2	J2	V_{CC}	P2	D20
B7	V_{CC}	D3	NC	J3	V_{SS}	P3	D22
B8	$\overline{PCHK}$	D15	$\overline{NMI}$	J15	V_{SS}	P15	A20
B9	V_{CC}	D16	A2	J16	V_{CC}	P16	A19
B10	V_{CCPLL}	D17	A3	J17	A10	P17	A17
B11	V_{CC}	E1	D7	K1	D13	Q1	D21
B12	V_{CC}	E2	D4	K2	V_{CC}	Q2	D23
B13	NC	E3	D0	K3	V_{SS}	Q3	D26

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Table 8. 80960Hx 168-Pin PGA Pinout — Pin Number Order (Sheet 2 of 2)

PGA Pin	Signal Name	PGA Pin	Signal Name	PGA Pin	Signal Name	PGA Pin	Signal Name
Q4	D28	Q16	A21	R11	V_{CC}	S6	$\overline{BE2}$
Q5	D30	Q17	A18	R12	BSTALL	S7	$\overline{BE1}$
Q6	V_{CC}	R1	D24	R13	BREQ	S8	$\overline{BLAST}$
Q7	V_{SS}	R2	D27	R14	A29	S9	$\overline{DEN}$
Q8	V_{SS}	R3	D31	R15	A26	S10	W/$\overline{R}$
Q9	V_{SS}	R4	$\overline{BTERM}$	R16	A23	S11	$\overline{DT}$/R
Q10	V_{SS}	R5	HOLD	R17	A22	S12	$\overline{WAIT}$
Q11	V_{SS}	R6	$\overline{ADS}$	S1	D25	S13	D/$\overline{C}$
Q12	$\overline{SUP}$	R7	V_{CC}	S2	D29	S14	$\overline{LOCK}$
Q13	A30	R8	V_{CC}	S3	$\overline{READY}$	S15	A31
Q14	A28	R9	$\overline{BE0}$	S4	HOLDA	S16	A27
Q15	A24	R10	V_{CC}	S5	$\overline{BE3}$	S17	A25

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3.2.2 80960Hx PQ4 Pinout
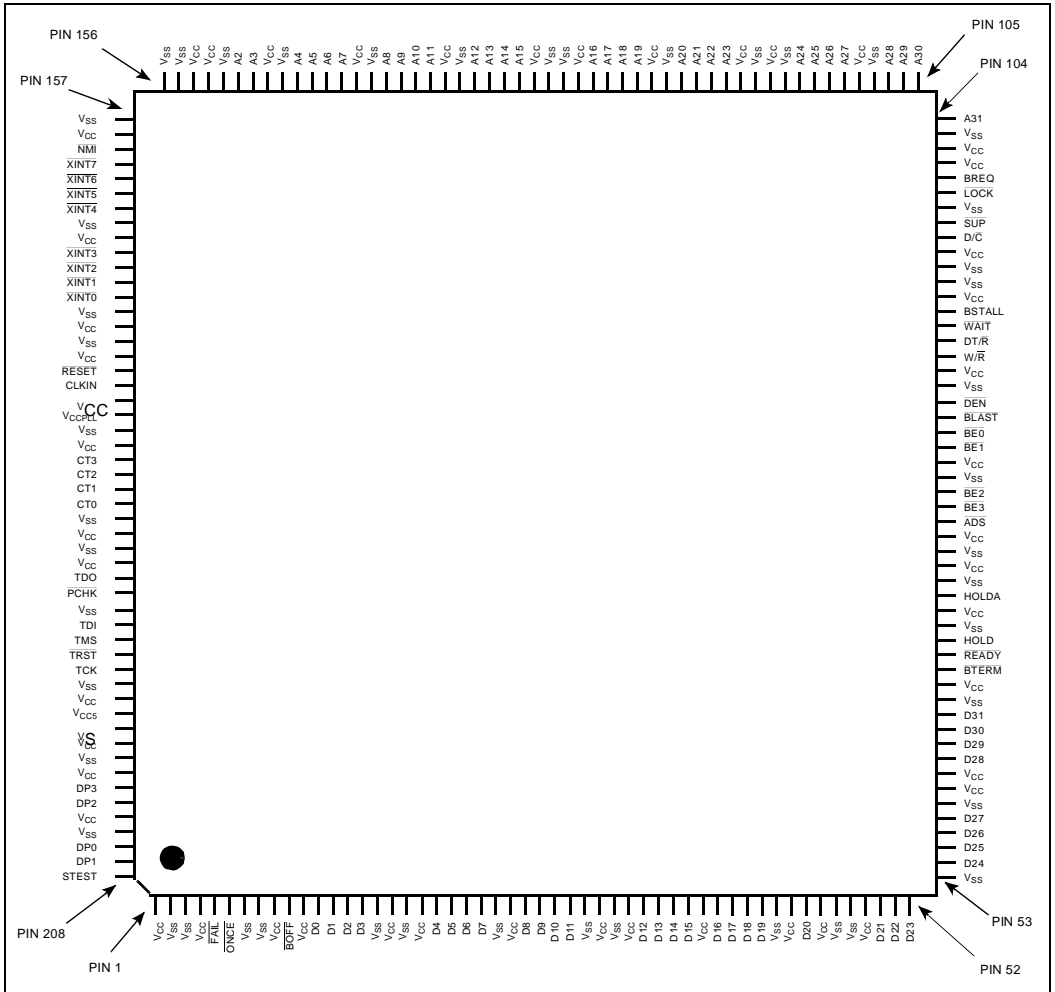
Figure 4. 80960Hx 208-Pin PQ4 Pinout

17

Table 9. 80960Hx PQ4 Pinout — Signal Name Order (Sheet 1 of 2)

Signal Name	PQ4 Pin	Signal Name	PQ4 Pin	Signal Name	PQ4 Pin	Signal Name	PQ4 Pin
A2	151	$\overline{BE0}$	83	D16	39	$\overline{PCHK}$	189
A3	150	$\overline{BE1}$	82	D17	40	$\overline{READY}$	68
A4	147	$\overline{BE2}$	79	D18	41	$\overline{RESET}$	174
A5	146	$\overline{BE3}$	78	D19	42	STEST	208
A6	145	$\overline{BLAST}$	84	D20	45	$\overline{SUP}$	97
A7	144	$\overline{BOFF}$	10	D21	50	TCK	194
A8	141	BREQ	100	D22	51	TD0	188
A9	140	BSTALL	91	D23	52	TDI	191
A10	139	$\overline{BTERM}$	67	D24	54	TMS	192
A11	138	CLKIN	175	D25	55	$\overline{TRST}$	193
A12	135	CT0	183	D26	56	V_{CC}	1
A13	134	CT1	182	D27	57	V_{CC}	4
A14	133	CT2	181	D28	61	V_{CC}	9
A15	132	CT3	180	D29	62	V_{CC}	11
A16	127	$D/\overline{C}$	96	D30	63	V_{CC}	17
A17	126	D0	12	D31	64	V_{CC}	19
A18	125	D1	13	$\overline{DEN}$	85	V_{CC}	25
A19	124	D2	14	DP0	206	V_{CC}	31
A20	121	D3	15	DP1	207	V_{CC}	33
A21	120	D4	20	DP2	203	V_{CC}	38
A22	119	D5	21	$\overline{DP3}$	202	V_{CC}	44
A23	118	D6	22	$DT/\overline{R}$	89	V_{CC}	46
A24	113	D7	23	$\overline{FAIL}$	5	V_{CC}	49
A25	112	D8	26	—	—	V_{CC}	59
A26	111	D9	27	—	—	V_{CC}	60
A27	110	D10	28	—	—	V_{CC}	66
A28	107	D11	29	HOLD	69	V_{CC}	71
A29	106	D12	34	HOLDA	72	V_{CC}	74
A30	105	D13	35	$\overline{LOCK}$	99	V_{CC}	76
A31	104	D14	36	$\overline{NMI}$	159	V_{CC}	81
$\overline{ADS}$	77	D15	37	$\overline{ONCE}$	6	V_{CC}	87

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Table 9. 80960Hx PQ4 Pinout — Signal Name Order (Sheet 2 of 2)

Signal Name	PQ4 Pin	Signal Name	PQ4 Pin	Signal Name	PQ4 Pin	Signal Name	PQ4 Pin
V_{CC}	92	V_{CC}	187	V_{SS}	70	V_{SS}	164
V_{CC}	95	V_{CC}	196	V_{SS}	73	V_{SS}	170
V_{CC}	101	V_{CC}	199	V_{SS}	75	V_{SS}	172
V_{CC}	102	V_{CC}	201	V_{SS}	80	V_{SS}	178
V_{CC}	109	V_{CC}	204	V_{SS}	86	V_{SS}	184
V_{CC}	115	VCC5	197	V_{SS}	93	V_{SS}	186
V_{CC}	117	V_{CCPLL}	177	V_{SS}	94	V_{SS}	190
V_{CC}	123	V_{SS}	2	V_{SS}	98	V_{SS}	195
V_{CC}	128	V_{SS}	3	V_{SS}	103	V_{SS}	198
V_{CC}	131	V_{SS}	7	V_{SS}	108	V_{SS}	200
V_{CC}	137	V_{SS}	8	V_{SS}	114	V_{SS}	205
V_{CC}	143	V_{SS}	16	V_{SS}	116	W/$\overline{R}$	88
V_{CC}	149	V_{SS}	18	V_{SS}	122	$\overline{WAIT}$	90
V_{CC}	153	V_{SS}	24	V_{SS}	129	$\overline{XINT0}$	169
V_{CC}	154	V_{SS}	30	V_{SS}	130	$\overline{XINT1}$	168
V_{CC}	158	V_{SS}	32	V_{SS}	136	$\overline{XINT2}$	167
V_{CC}	165	V_{SS}	43	V_{SS}	142	$\overline{XINT3}$	166
V_{CC}	171	V_{SS}	47	V_{SS}	148	$\overline{XINT4}$	163
V_{CC}	173	V_{SS}	48	V_{SS}	152	$\overline{XINT5}$	162
V_{CC}	176	V_{SS}	53	V_{SS}	155	$\overline{XINT6}$	161
V_{CC}	179	V_{SS}	58	V_{SS}	156	$\overline{XINT7}$	160
V_{CC}	185	V_{SS}	65	V_{SS}	157	—	—

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Table 10. 80960Hx PQ4 Pinout — Pin Number Order (Sheet 1 of 2)

PQ4 Pin	Signal Name	PQ4 Pin	Signal Name	PQ4 Pin	Signal Name	PQ4 Pin	Signal Name
1	V_{CC}	31	V_{CC}	61	D28	91	BSTALL
2	V_{SS}	32	V_{SS}	62	D29	92	V_{CC}
3	V_{SS}	33	V_{CC}	63	D30	93	V_{SS}
4	V_{CC}	34	D12	64	D31	94	V_{SS}
5	$\overline{FAIL}$	35	D13	65	V_{SS}	95	V_{CC}
6	$\overline{ONCE}$	36	D14	66	V_{CC}	96	D/$\overline{C}$
7	V_{SS}	37	D15	67	$\overline{BTERM}$	97	$\overline{SUP}$
8	V_{SS}	38	V_{CC}	68	$\overline{READY}$	98	V_{SS}
9	V_{CC}	39	D16	69	HOLD	99	$\overline{LOCK}$
10	$\overline{BOFF}$	40	D17	70	V_{SS}	100	BREQ
11	V_{CC}	41	D18	71	V_{CC}	101	V_{CC}
12	D0	42	D19	72	HOLDA	102	V_{CC}
13	D1	43	V_{SS}	73	V_{SS}	103	V_{SS}
14	D2	44	V_{CC}	74	V_{CC}	104	A31
15	D3	45	D20	75	V_{SS}	105	A30
16	V_{SS}	46	V_{CC}	76	V_{CC}	106	A29
17	V_{CC}	47	V_{SS}	77	$\overline{ADS}$	107	A28
18	V_{SS}	48	V_{SS}	78	$\overline{BE3}$	108	V_{SS}
19	V_{CC}	49	V_{CC}	79	$\overline{BE2}$	109	V_{CC}
20	D4	50	D21	80	V_{SS}	110	A27
21	D5	51	D22	81	V_{CC}	111	A26
22	D6	52	D23	82	$\overline{BE1}$	112	A25
23	D7	53	V_{SS}	83	$\overline{BE0}$	113	A24
24	V_{SS}	54	D24	84	$\overline{BLAST}$	114	V_{SS}
25	V_{CC}	55	D25	85	$\overline{DEN}$	115	V_{CC}
26	D8	56	D26	86	V_{SS}	116	V_{SS}
27	D9	57	D27	87	V_{CC}	117	V_{CC}
28	D10	58	V_{SS}	88	W/$\overline{R}$	118	A23
29	D11	59	V_{CC}	89	DT/$\overline{R}$	119	A22
30	V_{SS}	60	V_{CC}	90	$\overline{WAIT}$	120	A21

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Table 10. 80960Hx PQ4 Pinout — Pin Number Order (Sheet 2 of 2)

PQ4 Pin	Signal Name	PQ4 Pin	Signal Name	PQ4 Pin	Signal Name	PQ4 Pin	Signal Name
121	A20	143	V_{CC}	165	V_{CC}	187	V_{CC}
122	V_{SS}	144	A7	166	$\overline{XINT3}$	188	TD0
123	V_{CC}	145	A6	167	$\overline{XINT2}$	189	$\overline{PCHK}$
124	A19	146	A5	168	$\overline{XINT1}$	190	V_{SS}
125	A18	147	A4	169	$\overline{XINT0}$	191	TDI
126	A17	148	V_{SS}	170	V_{SS}	192	TMS
127	A16	149	V_{CC}	171	V_{CC}	193	$\overline{TRST}$
128	V_{CC}	150	A3	172	V_{SS}	194	TCK
129	V_{SS}	151	A2	173	V_{CC}	195	V_{SS}
130	V_{SS}	152	V_{SS}	174	$\overline{RESET}$	196	V_{CC}
131	V_{CC}	153	V_{CC}	175	CLKIN	197	VCC5
132	A15	154	V_{CC}	176	V_{CC}	198	V_{SS}
133	A14	155	V_{SS}	177	V_{CCPLL}	199	V_{CC}
134	A13	156	V_{SS}	178	V_{SS}	200	V_{SS}
135	A12	157	V_{SS}	179	V_{CC}	201	V_{CC}
136	V_{SS}	158	V_{CC}	180	CT3	202	DP3
137	V_{CC}	159	$\overline{NMI}$	181	CT2	203	DP2
138	A11	160	$\overline{XINT7}$	182	CT1	204	V_{CC}
139	A10	161	$\overline{XINT6}$	183	CT0	205	V_{SS}
140	A9	162	$\overline{XINT5}$	184	V_{SS}	206	DP0
141	A8	163	$\overline{XINT4}$	185	V_{CC}	207	DP1
142	V_{SS}	164	V_{SS}	186	V_{SS}	208	STEST

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3.3   Package Thermal Specifications

The 80960Hx is specified for operation when T_C (case temperature) is within the range of 0°C–85°C. T_C may be measured in any environment to determine whether the 80960Hx is within the specified operating range. Measure the case temperature at the center of the top surface, opposite the pins. Refer to Figures 5.

T_A (ambient temperature) is calculated from θ_{CA} (thermal resistance from case to ambient) using the equation:

$$T_A = T_C - P*\theta_{CA}$$

Table 11 shows the maximum T_A allowable (without exceeding T_C) at various airflows and operating frequencies (f_{CLKIN}).

Note that T_A is greatly improved by attaching fins or a heatsink to the package. P (maximum power consumption) is calculated by using the typical I_{CC} as tabulated in Section 4.5, DC Specifications (pg. 29) and V_{CC} of 3.3 V.

Measure PGA/PQ4 temperature at center of top surface
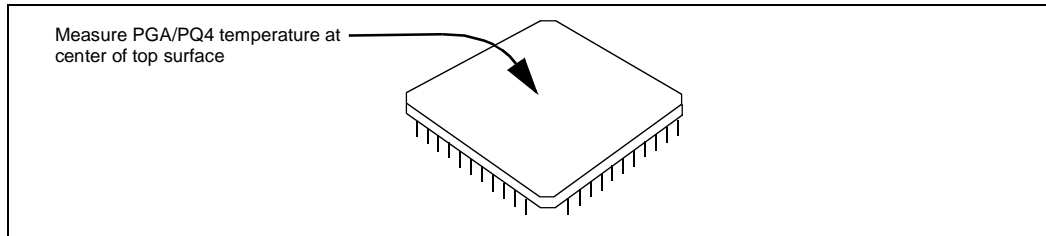
Figure 5. Measuring 80960Hx PGA Case Temperature

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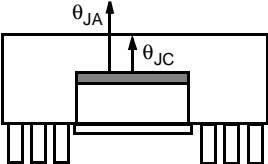
Table 11. Maximum T_A at Various Airflows in °C (PGA Package Only)

			Airflow-ft/min (m/sec)					
		f_{CLKIN} (MHz)	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
Core 1X Bus Clock	T_A with Heatsink*	25 33 40	69 63 59	74 70 67	78 75 73	79 77 75	80 79 77	80 79 77
	T_A without Heatsink	25 33 40	64 56 50	67 62 56	71 67 63	74 70 67	75 72 69	76 74 71
Core 2X Bus Clock	T_A with Heatsink*	16 25 33 40	68 58 49 41	73 66 60 55	77 73 69 65	79 75 71 68	80 77 74 72	80 77 74 72
	T_A without Heatsink	16 25 33 40	62 49 38 27	66 56 46 38	71 62 55 48	73 66 60 55	75 68 63 58	76 71 66 62
Core 3X Bus Clock	T_A with Heatsink*	20 25	53 45	63 58	71 67	73 70	76 73	76 73
	T_A without Heatsink	20 25	43 33	51 42	58 51	63 58	66 61	68 64

NOTE: *0.285" high unidirectional heatsink (Al alloy 6061, 50 mil fin width, 150 mil center-to-center fin spacing).

Table 12. 80960Hx 168-Pin PGA Package Thermal Characteristics

Thermal Resistance — °C/Watt						
Parameter	Airflow — ft./min (m/sec)					
	0 (0)	200 (1.01)	400 (2.03)	600 (3.07)	800 (4.06)	1000 (5.07)
θ Junction-to-Case (Case measured as shown in Figures 5)	1.5	1.5	1.5	1.5	1.5	1.5
θ Case-to-Ambient (No Heatsink)	17	14	11	9	8	7
θ Case-to-Ambient (With Heatsink)*	13	9	6	5	4	4

θ_{JA} θ_{JC}

NOTES:

1. This table applies to 80960Hx PGA plugged into socket or soldered directly to board.

2. $\theta_{JA} = \theta_{JC} + \theta_{CA}$

*0.285" high unidirectional heatsink (Al alloy 6061, 50 mil fin width, 150 mil center-to-center fin spacing).

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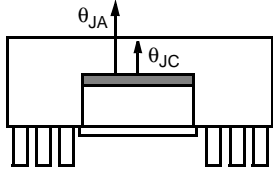
Table 13. Maximum T$_A$ at Various Airflows in °C (PQ4 Package Only)

| | | f$_{CLKIN}$ (MHz) | Airflow-ft/min (m/sec) | | | | | |
			0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
Core 1X Bus Clock	T$_A$ with Heatsink*	25	71	76	79	79	80	80
		33	67	74	77	77	79	79
		40	63	71	75	75	77	77
	T$_A$ without Heatsink	25	70	73	75	75	76	76
		33	65	68	72	72	74	74
		40	61	65	69	69	71	71
Core 2X Bus Clock	T$_A$ with Heatsink*	16	71	76	79	79	80	80
		25	62	71	75	75	77	77
		33	55	66	71	71	74	74
		40	48	62	68	68	72	72
	T$_A$ without Heatsink	16	69	72	75	75	76	76
		25	60	64	68	68	71	71
		33	52	57	63	63	66	66
		40	42	51	58	58	62	62
Core 3X Bus Clock	T$_A$ with Heatsink*	20	58	68	73	73	76	76
		25	51	64	70	70	73	73
	T$_A$ without Heatsink	20	56	61	66	66	68	68
		25	48	55	61	61	64	64

NOTE: *0.285" high unidirectional heatsink (Al alloy 6061, 50 mil fin width, 150 mil center-to-center fin spacing).

Table 14. 80960Hx 208-Pin PQ4 Package Thermal Characteristics

| Thermal Resistance — °C/Watt | | | | | | |
| Parameter | Airflow — ft./min (m/sec) | | | | | |
	0 (0)	200 (1.01)	400 (2.03)	600 (3.07)	800 (4.06)	1000 (5.07)
θ Junction-to-Case (Case measured as shown in Figures 5)	1	1	1	1	1	1
θ Case-to-Ambient (No Heatsink)	12	10	8	8	7	7
θ Case-to-Ambient (With Heatsink)*	11	7	5	5	4	4

NOTES:

1. This table applies to 80960Hx PQ4 plugged into socket or soldered directly to board.

2. $\theta_{JA} = \theta_{JC} + \theta_{CA}$

*0.285" high unidirectional heatsink (Al alloy 6061, 50 mil fin width, 150 mil center-to-center fin spacing).

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3.4   Heat Sink Adhesives

Intel recommends silicone-based adhesives to attach heat sinks to the PGA package. There is no particular recommendation concerning the PQ4 package.

3.5   PowerQuad4 Plastic Package

The 80960Hx family is available in an improved version of the common 208-lead SQFP plastic package called the PowerQuad4* (PQ4). The PQ4 package dimensions and lead pitch are identical to the SQFP package and the former PQ2 package, so the PQ4 fits into the same board footprint. The advantage of the PQ4 package is the superior thermal conductivity that allows the plastic version of

the 80960Hx to operate with the same 0 - 85°C temperature specifications as the more expensive ceramic PGA package.

The PQ4 package integrates a copper heat sink within the package to dissipate heat effectively. See Table 13 and Table 14 on page 24.

3.6   Stepping Register Information

The memory-mapped register at FF008710H contains the 80960Hx Device ID. The ID is identical to the ID obtained from a JTAG Query. Figures 6 defines the current 80960Hx Device IDs. The value for device identification is compliant with the IEEE 1149.1 specification and Intel standards. Table 15 describes the fields of the device ID.
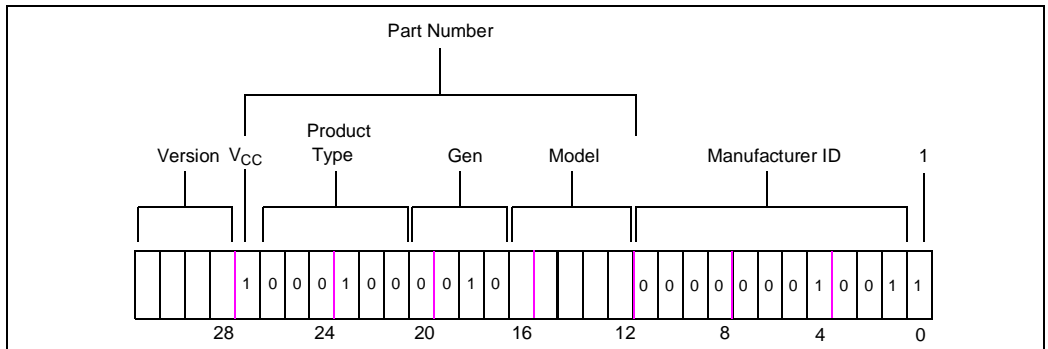
Figure 6. 80960Hx Device Identification Register

Table 15. Fields of 80960Hx Device ID

Field	Value	Definition
Version	See Table 17	Indicates major stepping changes.
V_{CC}	1 = 3.3 V device	Indicates that a device is 3.3 V.
Product Type	00 0100 (Indicates i960 CPU)	Designates type of product.
Generation Type	0010 = H-series	Indicates the generation (or series) the product belongs to.
Model	See Table 16	Indicates member within a series and specific model information.
Manufacturer ID	000 0000 1001 (Indicates Intel)	Manufacturer ID assigned by IEEE.

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Table 16. 80960Hx Device ID Model Types

Device	Version	V$_{CC}$	Product	Gen.	Model	Manufacturer ID	'1'
80960HA	See Table 17	1	000100	0010	00000	00000001001	1
80960HD		1	000100	0010	00001	00000001001	1
80960HT		1	000100	0010	00010	00000001001	1

Table 17. Device ID Version Numbers for Different Steppings

Stepping	Version
A0	0000
A1	0001
A2	0001
B0, B2	0010

NOTE: This data sheet applies to the B2 stepping.

3.7 Sources for Accessories

The following is a list of suggested sources for 80960Hx accessories. This is neither an endorsement nor a warranty of the performance of any of the listed products and/or companies.

Sockets

• 3M Textool Test and Interconnection Products
  6801 River Place Blvd. MS 130-3N-29
  Austin, TX 78726-9000
  (800) 328-0411 FAX: (800) 932-9373

• Concept Mfg, Inc. (Decoupling Sockets)
  400 Walnut St. Suite 609
  Redwood City, CA 94063
  (415) 365-1162 FAX: (415) 365-1164

Heatsinks/Fins

• Thermalloy, Inc.
  2021 West Valley View Lane
  Dallas, TX 75234-8993
  (972) 243-4321 FAX: (972) 241-4656

• Wakefield Engineering, Inc.
  60 Audubon Road
  Wakefield, MA 01880
  (617) 245-5900 FAX: (617) 246-0874

• Aavid Thermal Technologies, Inc.
  One Kool Path
  Laconia. NH 03247-0400
  (603) 523-3400

ADVANCE INFORMATION

4.0   ELECTRICAL SPECIFICATIONS

4.1   Absolute Maximum Ratings

Parameter	Maximum Rating
Storage Temperature	–65°C to +150°C
Case Temperature Under Bias	–65°C to +110°C
Supply Voltage wrt. V$_{SS}$	–0.5 V to + 4.6 V
Voltage on V$_{CC5}$ wrt. V$_{SS}$	–0.5 V to + 6.5 V
Voltage on Other Pins wrt. V$_{SS}$	–0.5 V to V$_{CC}$ + 0.5 V

NOTICE: This document contains information on products in the sampling and initial production phases of development. It is valid for the devices indicated in the revision history. The specifications within this data sheet are subject to change without notice. Verify with your local Intel sales office that you have the latest data sheet before finalizing a design.

WARNING: *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

4.2   Operating Conditions

Table 18. Operating Conditions

Symbol	Parameter	Min	Max	Units
V$_{CC}$	Supply Voltage	3.15	3.45	V
V$_{CC5}$	Input Protection Bias	3.15	5.5	V
f$_{CLKIN}$ 1xcore	Input Clock Frequency - 1x Core (80960HA)	16	40	MHz
f$_{CLKIN}$ 2xcore	Input Clock Frequency - 2x Core (80960HD)	16	40	MHz
f$_{CLKIN}$ 3xcore	Input Clock Frequency - 3x Core (80960HT)	16	25	MHz
T$_C$	Case Temp Under Bias (PGA and PQ4 Packages)	0	85	^{o}C

4.3   Recommended Connections

Power and ground connections must be made to multiple V$_{CC}$ and V$_{SS}$ (GND) pins. Every 80960Hx-based circuit board should include power (V$_{CC}$) and ground (V$_{SS}$) planes for power distribution. Every V$_{CC}$ pin must be connected to the power plane; every V$_{SS}$ pin must be connected to the ground plane. Pins identified as "NC" —no connect pins—**must not** be connected in the system.

Liberal decoupling capacitance should be placed near the 80960Hx. The processor can cause transient power surges when its numerous output buffers transition, particularly when connected to large capacitive loads.

Low inductance capacitors and interconnects are recommended for best high-frequency electrical performance. Inductance can be reduced by shortening the board traces between the processor and decoupling capacitors as much as possible. Capacitors specifically designed for PGA packages offer the lowest possible inductance.

For reliable operation, always connect unused inputs to an appropriate signal level. In particular, any unused interrupt ($\overline{\text{XINT7:0}}$, $\overline{\text{NMI}}$) input should be connected to V$_{CC}$ through a pull-up resistor, as should $\overline{\text{BTERM}}$ if not used. Pull-up resistors should be in the in the range of 20 KΩ for each pin tied high. If $\overline{\text{READY}}$ or HOLD are not used, the unused input should be connected to ground. **N.C. pins must always remain unconnected.**

4.4   V$_{CC5}$ Pin Requirements (V$_{DIFF}$)

In mixed voltage systems that drive 80960Hx processor inputs in excess of 3.3 V, the V$_{CC5}$ pin must be connected to the system's 5 V supply. To limit current flow into the V$_{CC5}$ pin, there is a limit to the voltage differential between the V$_{CC5}$ pin and the other V$_{CC}$ pins. The voltage differential between the 80960Hx V$_{CC5}$ pin and its 3.3 V V$_{CC}$ pins should never exceed 2.25 V. This limit applies to power-up, power-down, and steady-state operation. Table 19 outlines this requirement.

Meeting this requirement ensures proper operation and guarantees that the current draw into the V$_{CC5}$ pin does not exceed the specification.

If the voltage difference requirements cannot be met due to system design limitations, an alternate solution may be employed. As shown in Figure 7, a minimum of 100 Ω series resistor may be used to limit the current into the V$_{CC5}$ pin. This resistor ensures that current drawn by the V$_{CC5}$ pin does not exceed the maximum rating for this pin.
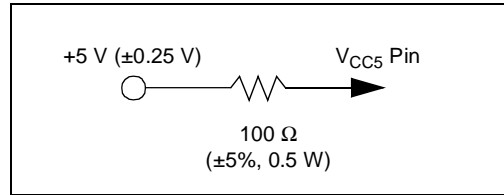
Figure 7.   V$_{CC5}$ Current-Limiting Resistor

This resistor is not necessary in systems that can guarantee the V$_{DIFF}$ specification.

In 3.3 V-only systems and systems that drive 80960Hx pins from 3.3 V logic, connect the V$_{CC5}$ pin directly to the 3.3 V V$_{CC}$ plane.

Table 19. V$_{DIFF}$ Specification for Dual Power Supply Requirements (3.3 V, 5 V)

Symbol	Parameter	Min	Max	Units	Notes
V$_{DIFF}$	V$_{CC5}$-V$_{CC}$ Difference		2.25	V	V$_{CC5}$ input should not exceed V$_{CC}$ by more than 2.25 V during power-up and power-down, or during steady-state operation.

ADVANCE INFORMATION

4.5   DC Specifications

Table 20. 80960Hx DC Characteristics (Sheet 1 of 2)

Per the conditions described in Section 4.3, Recommended Connections (pg. 27).

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{IL}	Input Low Voltage	− 0.3		+0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC5} + 0.3	V	(4)
V_{OL}	Output Low Voltage All outputs except $\overline{FAIL}$			0.4 0.2	V	I_{OL} = 3 mA I_{OL} = 100 µA
V_{OL}	Output Low Voltage $\overline{FAIL}$ pin			0.4	V	I_{OL} = 5 mA
V_{OH}	Output High Voltage	2.4 V_{CC} − 0.2			V V	I_{OH} = −3 mA I_{OH} = − 100 µA
I_{LI}	Input Leakage Current Non-Test Inputs TDI, TMS, $\overline{TRST}$ and $\overline{ONCE}$ pins	-1		1 -110	µA µA	0 ≤ V_{IN} ≤ V_{CC} V_{IN} = 0 V
I_{LO}	Output Leakage Current Non-Test Outputs TDO pin			1 5	µA µA	0.45 ≤ V_{OUT} ≤ V_{CC} 0.45 ≤ V_{OUT} ≤ V_{CC}
I_{CC} Active (Power Supply)	80960HA 25 33 40 80960HD 32 50 66 80 80960HT 60 75			579 765 927 631 985 1300 1578 1165 1455	mA	(4,5)
I_{CC} Active (Thermal)	80960HA 25 33 40 80960HD 32 50 66 80 80960HT 60 75		392 518 628 413 645 851 1034 752 938		mA	(4,6)
I_{CC} Test (Reset Mode)	80960HA 25 33 40 80960HD 32 50 66 80 80960HT 60 75			330 436 528 382 595 785 955 702 878	mA	(7,8)

Table 20. 80960Hx DC Characteristics (Sheet 2 of 2)

Per the conditions described in Section 4.3, Recommended Connections (pg. 27).

Symbol	Parameter	Min	Typ	Max	Units	Notes
I_{CC} Test (ONCE mode)				25	mA	(7)
I_{CC5} Current on the V_{CC5} Pin	80960HA 80960HD 80960HT			200 200 200	µA	(9)
C_{IN}	Input Capacitance for: PQ4 PGA			 12	pF pF	 F_C = 1 MHz
C_{OUT}	Output Capacitance of each output pin			12	pF	F_C = 1 MHz (3)
$C_{I/O}$	I/O Pin Capacitance			12	pF	F_C = 1 MHz
R_{PU}	Internal Pull-Up Resistance for $\overline{ONCE}$, TMS, TDI and $\overline{TRST}$	30	65	100	kΩ	

NOTES:

1. I_{CC} Maximum is measured at worst case frequency, V_{CC}, and temperature, with device operating and outputs loaded to the test conditions described in Section 4.6.1, AC Test Conditions (pg. 34).
2. I_{CC} Typical is not tested.
3. Output Capacitance is the capacitive load of a floating output.
4. ICE inputs are not 5V tolerant.
   V_{OH} = 2.0 V → V_{CC} + 0.3 V
5. Measured with device operating and outputs loaded to the test conditions in Figure 8, AC Test Load (pg. 34). Input signals rise to V_{CC} and fall to V_{SS}.
6. I_{CC} Active (Power Supply) value is provided for selecting your system's power supply. It is measured using one of the worst case instruction mixes with V_{CC} = 3.45 V. This parameter is characterized but not tested.
7. I_{CC} Active (Thermal) value is provided for your system's thermal management. Typical I_{CC} is measured with V_{CC} = 3.3 V and temperature = 25°C. This parameter is characterized but not tested.
8. I_{CC} Test (Power modes) refers to the I_{CC} values that are tested when the 80960HA/HD/HT is in Reset mode or ONCE mode with V_{CC} = 3.45 V.
9. Worst case is V_{CC} = 3.45 V, 0°C.
10. is tested at V_{CC} = 3.0 V, V_{CC5} = 5.25 V.

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4.6 AC Specifications

Table 21. 80960Hx AC Characteristics (Sheet 1 of 2)

Per the conditions in Section 4.2, Operating Conditions (pg. 27) and Section 4.6.1, AC Test Conditions (pg. 34).

Symbol	Parameter		Min	Max	Units	Notes
align	**Input Clock (1,7)**					
T_F	CLKIN Frequency	80960HA 80960HD 80960HT	16 16 16	40 40 25	MHz MHz MHz	
T	CLKIN Period	80960HA 80960HD 80960HT	25 25 40	62.5 62.5 62.5	ns ns ns	
T_{CS}	CLKIN Period Stability		-250	+250	ps	(11)
T_{CH}	CLKIN High Time		8		ns	(11)
T_{CL}	CLKIN Low Time	80960HA 80960HD 80960HT	8 8 8		ns ns ns	(11)
T_{CR}	CLKIN Rise Time		0	4	ns	(11)
T_{CF}	CLKIN Fall Time		0	4	ns	(11)
	Synchronous Outputs (1,2,3,6)					
T_{OV1}, T_{OH1}	Output Valid Delay and Output Hold for all outputs except DT/$\overline{R}$, $\overline{BLAST}$, $\overline{BSTALL}$ and BREQ for 3.3 V inputs and I/O's.		1.5	9.5	ns	(13)
	Same as above, but for 5.5 V inputs and I/O's.		1.5	12.5	ns	
T_{OV2}, T_{OH2}	Output Valid Delay and Output Hold for DT/R		T/2 + 1.5	T/2 + 9.5	ns	
T_{OV3}, T_{OH3}	Output Valid Delay and Output Hold for $\overline{BLAST}$		1.5	9	ns	
T_{OV4}, T_{OH4}	Output Valid Delay and Output Hold for BREQ and $\overline{BSTALL}$		0.5	9	ns	
T_{OV5}, T_{OH5}	Output Valid Delay and Output Hold for A3:2		1.5	8.5		
T_{OF}	Output Float for all outputs		1.5	9	ns	(11)
	Synchronous Inputs (1,7,8,9)					
T_{IS1}	Input Setup for all inputs except $\overline{READY}$, $\overline{BTERM}$, HOLD, and $\overline{BOFF}$		2.5		ns	
T_{IH1}	Input Hold for all inputs except $\overline{READY}$, $\overline{BTERM}$, HOLD, and $\overline{BOFF}$		2.5		ns	
T_{IS2}	Input Setup for $\overline{READY}$, $\overline{BTERM}$, HOLD, and $\overline{BOFF}$		6		ns	
T_{IH2}	Input Hold for $\overline{READY}$, $\overline{BTERM}$, HOLD, and $\overline{BOFF}$		2.5		ns	

NOTE:
See Table 22, AC Characteristics Notes (pg. 33) for all notes related to AC specifications.

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Table 21. 80960Hx AC Characteristics (Sheet 2 of 2)

Per the conditions in Section 4.2, Operating Conditions (pg. 27) and Section 4.6.1, AC Test Conditions (pg. 34).

Symbol	Parameter	Min	Max	Units	Notes
Relative Output Timings (1,2,3,6,10)					
T$_{AVSH1}$	A31:2 Valid to ADS Rising	T − 5	T + 5	ns	(10)
T$_{AVSH2}$	BE3:0, W/R, SUP, D/C Valid to ADS Rising	T − 5	T + 5	ns	(10)
T$_{AVEL1}$	A31:2 Valid to DEN Falling	T − 5	T + 5	ns	(10)
T$_{AVEL2}$	BE3:0, W/R, SUP Valid to DEN Falling	T − 5	T + 5	ns	(10)
T$_{NLQV}$	WAIT Falling to Output Data Valid	-5	5	ns	(10)
T$_{DVNH}$	Output Data Valid to WAIT Rising	-5 + N*T	5 + N*T	ns	(4,10)
T$_{NLNH}$	WAIT Falling to WAIT Rising	-4 + N*T	4 + N*T	ns	(4,10)
T$_{NHQX}$	Output Data Hold after WAIT Rising	-5 + (N+1)*T	5 + (N+1)*T	ns	(5,10)
T$_{EHTV}$	DT/R Hold after DEN High	T/2 − 5	Infinite	ns	(10)
T$_{TVEL}$	DT/R Valid to DEN Falling	T/2 − 4		ns	(10)
Relative Input Timings (1,7,10)					
T$_{IS7}$	XINT7:0, NMI Input Setup	6		ns	(9)
T$_{IH7}$	XINT7:0, NMI Input Hold	2.5		ns	(9)
T$_{IS8}$	RESET Input Setup	3		ns	(8)
T$_{IH8}$	RESET Input Hold	T/4 + 1		ns	(8)

NOTE:
See Table 22, AC Characteristics Notes (pg. 33) for all notes related to AC specifications.

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Table 22. AC Characteristics Notes

NOTES:

1. See Section 4.6.2, AC Timing Waveforms (pg. 34) for waveforms and definitions.

2. See Figure 25, Output Delay or Hold vs. Load Capacitance (pg. 42) for capacitive derating information for output delays and hold times.

3. See Figure 22, Rise and Fall Time Derating at 85°C and Minimum VCC (pg. 41) for capacitive derating information for rise and fall times.

4. Where N is the number of N_{RAD}, N_{RDD}, N_{WAD} or N_{WDD} wait states that are programmed in the Bus Controller Region Table. $\overline{WAIT}$ never goes active when there are no wait states in an access.

5. N = Number of wait states inserted with $\overline{READY}$.

6. These specifications are guaranteed by the processor.

7. These specifications must be met by the system for proper operation of the processor.

8. $\overline{RESET}$ is an asynchronous input that has no required setup and hold time for proper operation. However, to guarantee the device exits the reset mode synchronized to a particular clock edge, the rising edge of $\overline{RESET}$ must meet setup and hold times to the rising edge of the CLKIN.

9. The interrupt pins are synchronized internally by the 80960Hx. They have no required setup or hold times for proper operation. These pins are sampled by the interrupt controller every clock and must be active for at least two consecutive CLKIN rising edges when asserting them asynchronously. To guarantee recognition at a particular clock edge, the setup and hold times shown must be met.

10. Relative Output timings are not tested.

11. Not tested.

12. The processor minimizes changes to the bus signals when transitioning from a bus cycle to an idle bus for the following signals: A31:4, $\overline{SUP}$, CT3:0, D/$\overline{C}$, $\overline{LOCK}$, W/$\overline{R}$, $\overline{BE3:0}$.

13. Worst-case T_{OV} condition occurs on I/O pins when pins transition from a floating high input to driving a low output state. The Data Bus pins encounter this condition during a read followed by a write. 5 V signals take 3 ns longer to discharge than 3.3 V signals at 50 pF loads.

Table 23. 80960Hx Boundary Scan Test Signal Timings (Sheet 1 of 2)

Symbol	Parameter	Min	Max	Units	Notes
T_{BSF}	TCK Frequency	0	8	MHz	
T_{BSC}	TCK Period	125	Infinite	ns	
T_{BSCH}	TCK High Time	40		ns	Measured at 1.5 V (1)
T_{BSCL}	TCK Low Time	40		ns	Measured at 1.5 V (1)
T_{BSCR}	TCK Rise Time		8	ns	0.8 V to 2.0 V (1)
T_{BSCF}	TCK Fall Time		8	ns	2.0 V to 0.8 V (1)
T_{BSIS1}	Input Setup to TCK — TDI, TMS	8		ns	
T_{BSIH1}	Input Hold from TCK — TDI, TMS	10		ns	
T_{BSOV1}	TDO Valid Delay	3	30	ns	

NOTE:

1. Not tested.

Table 23. 80960Hx Boundary Scan Test Signal Timings (Sheet 2 of 2)

Symbol	Parameter	Min	Max	Units	Notes
T$_{BSOF1}$	TDO Float Delay		36	ns	(1)
T$_{BSOV2}$	All Outputs (Non-Test) Valid Delay	3	30	ns	Relative to TCK
T$_{BSOF2}$	All Outputs (Non-Test) Float Delay		36	ns	Relative to TCK (1)
T$_{BSIS2}$	Input Setup to TCK - All Inputs (Non-Test)	8		ns	
T$_{BSIH2}$	Input Hold from TCK - All Inputs (Non-Test)	10		ns	

NOTE:

1. Not tested.

4.6.1   AC Test Conditions

AC values in are derived using the 50 pF load shown in Figure 8. shows how timings vary with load capacitance. Input waveforms (except for CLKIN) are assumed to have a rise and fall time of ≤ 2 ns from 0.8 V to 2.0 V.

4.6.2   AC Timing Waveforms

Figure 8. AC Test Load

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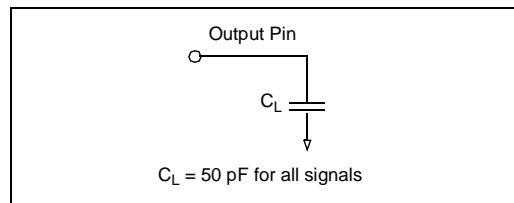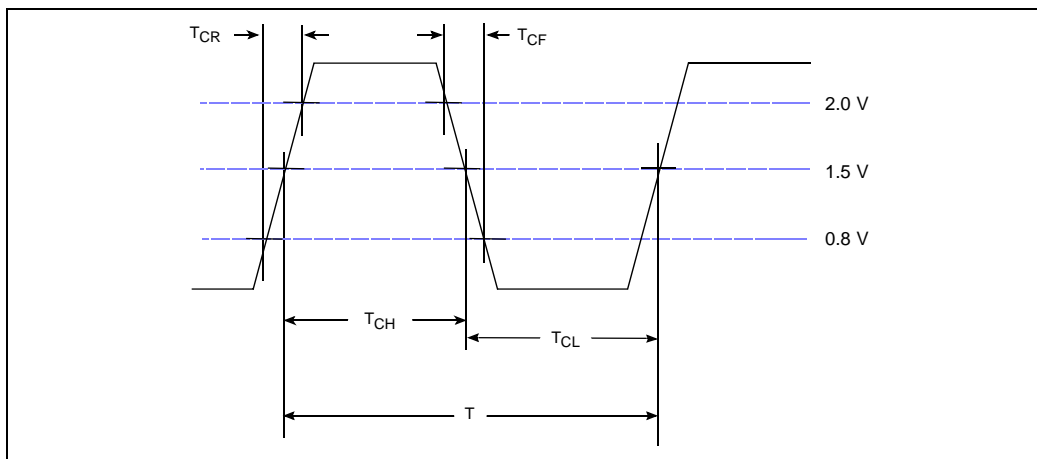
Figure 9. CLKIN Waveform
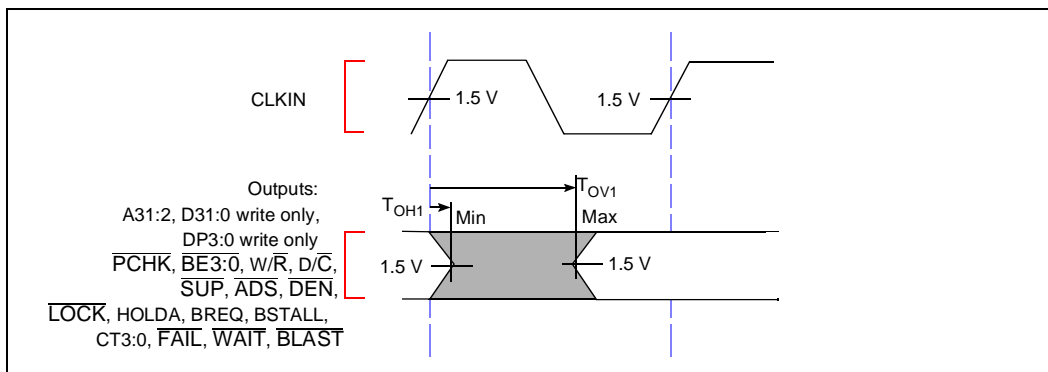
Figure 10. Output Delay Waveform
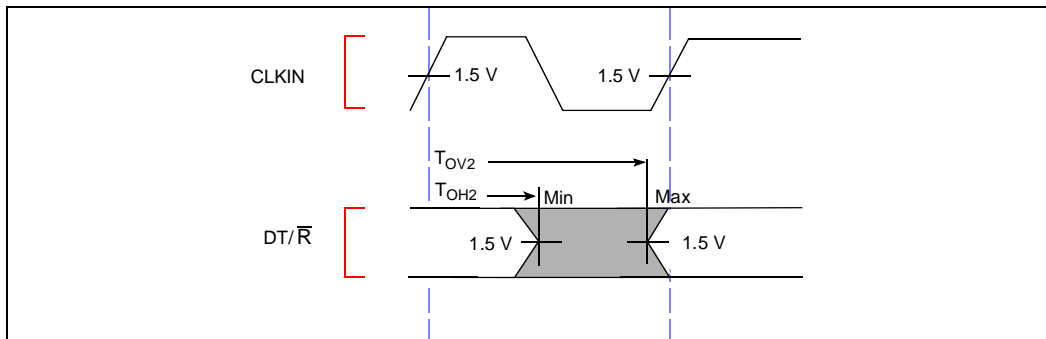
Figure 11. Output Delay Waveform
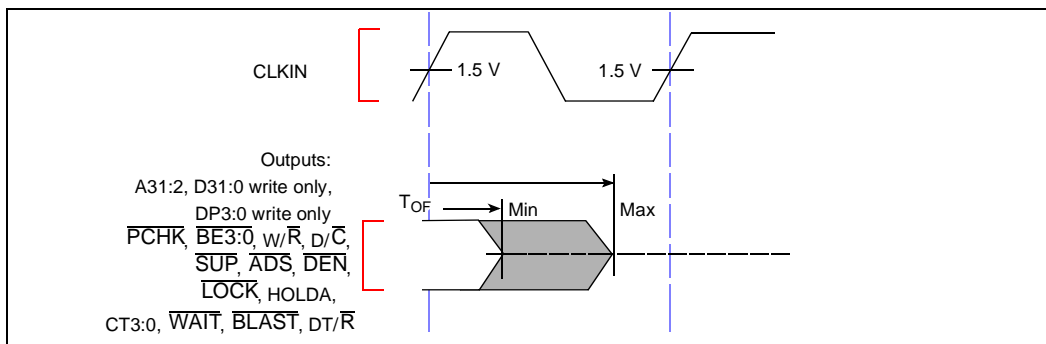
Figure 12. Output Float Waveform
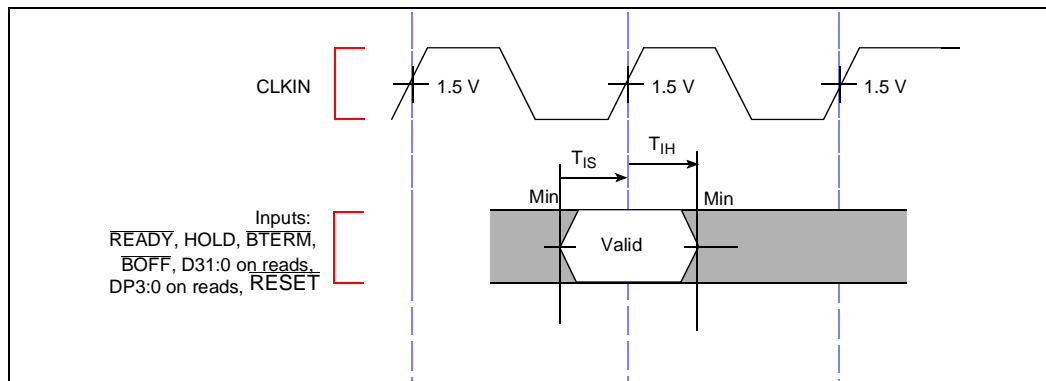
Figure 13. Input Setup and Hold Waveform

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NOTE: A and B edges are established by de-assertion of $\overline{\text{RESET}}$. See Figure 29, Cold Reset Waveform (pg. 45).
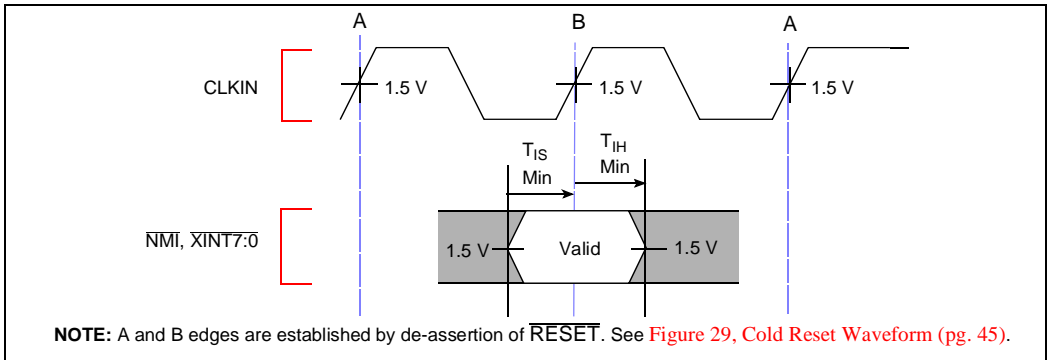
Figure 14. $\overline{\text{NMI}}$, $\overline{\text{XINT7:0}}$ Input Setup and Hold Waveform

$\textbf{T}_{\textbf{OV}}$ $\textbf{T}_{\textbf{OH}}$ — OUTPUT DELAY - The maximum output delay is referred to as the Output Valid Delay (T_{OV}). The minimum output delay is referred to as the Output Hold (T_{OH}).

$\textbf{T}_{\textbf{IS}}$ $\textbf{T}_{\textbf{IH}}$ — INPUT SETUP AND HOLD - The input setup and hold requirements specify the sampling window during which synchronous inputs must be stable for correct processor operation.
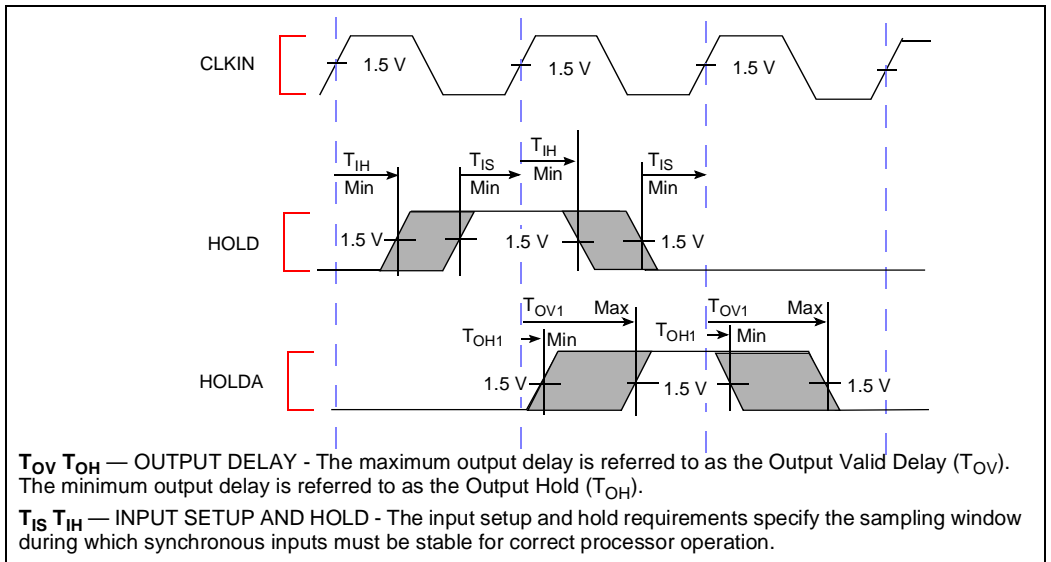
Figure 15. Hold Acknowledge Timings
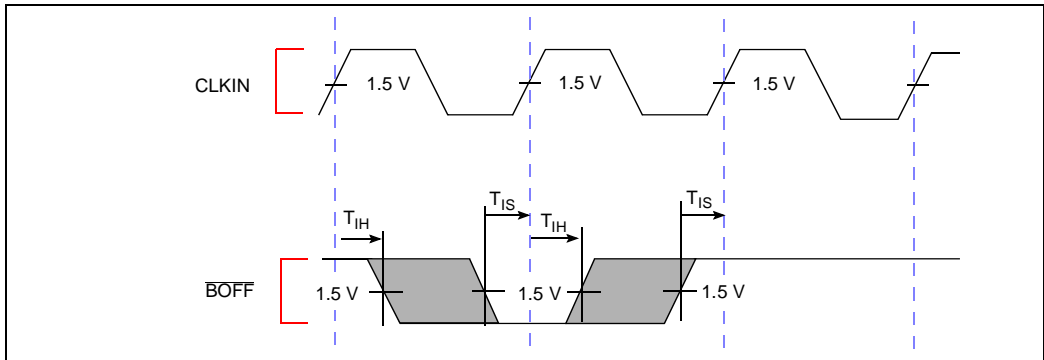
Figure 16. Bus Backoff (BOFF) Timings
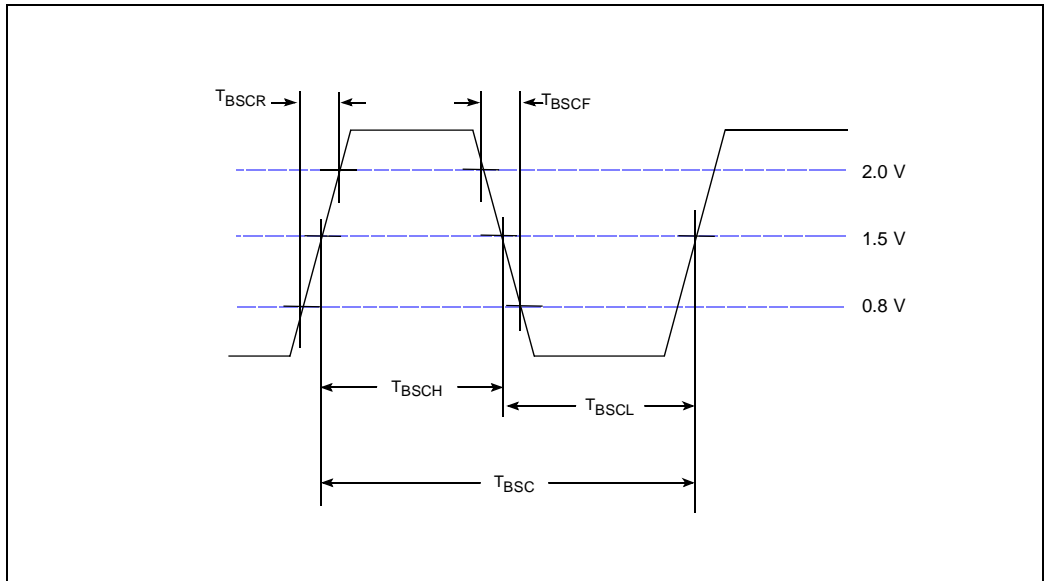
Figure 17. TCK Waveform

ADVANCE INFORMATION
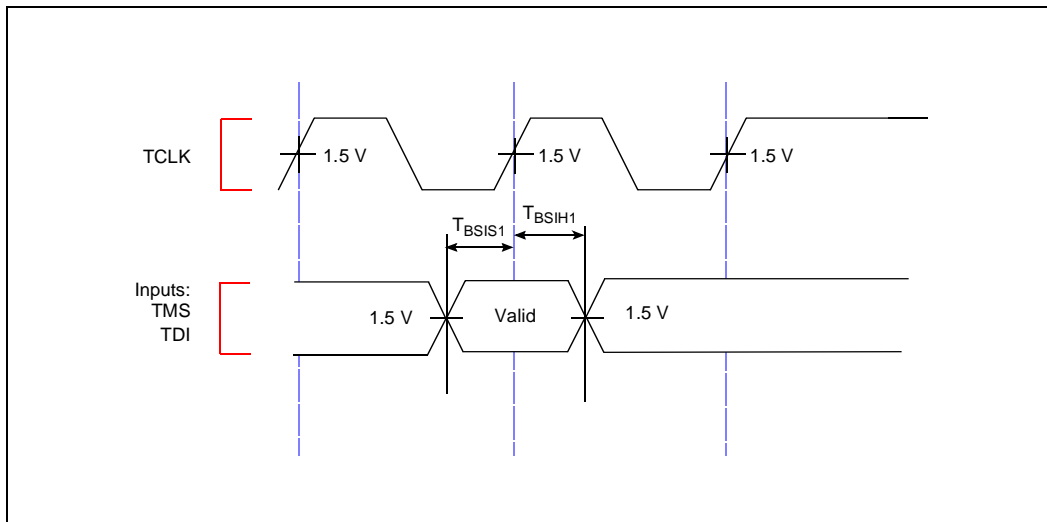
Figure 18. Input Setup and Hold Waveforms for T_{BSIS1} and T_{BSIH1}
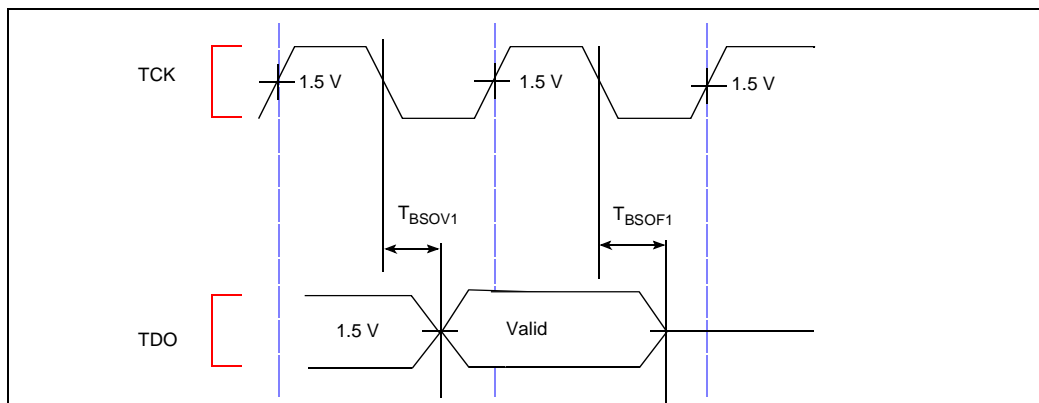
Figure 19. Output Delay and Output Float for T_{BSOV1} and T_{BSOF1}
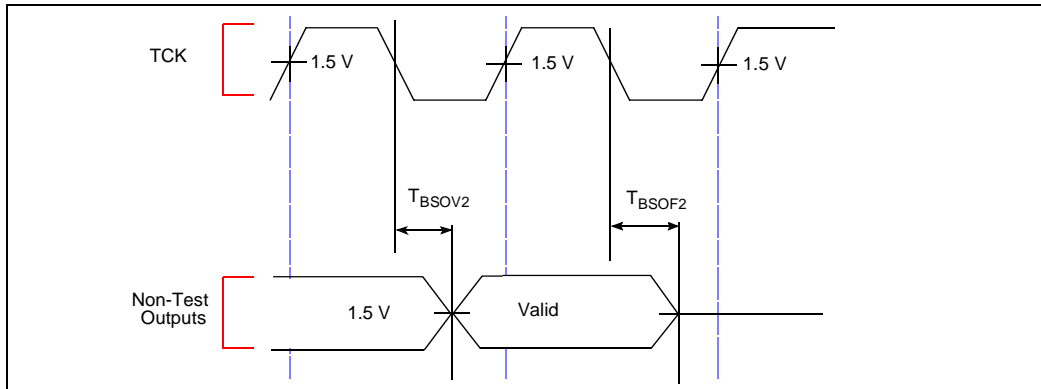
Figure 20. Output Delay and Output Float Waveform for T$_{BSOV2}$ and T$_{BSOF2}$
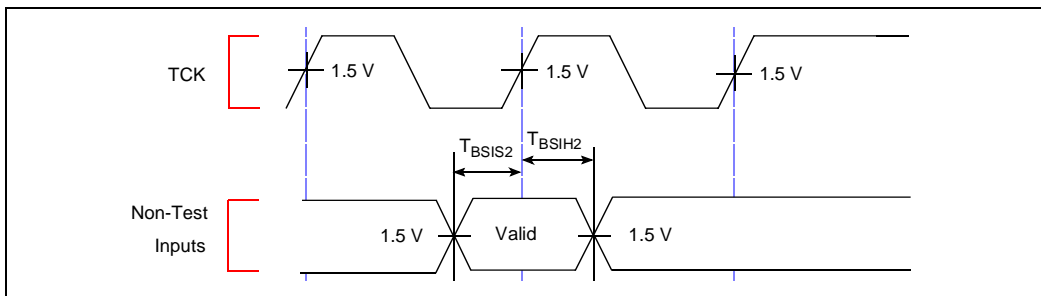
Figure 21. Input Setup and Hold Waveform for T$_{BSIS2}$ and T$_{BSIH2}$

ADVANCE INFORMATION
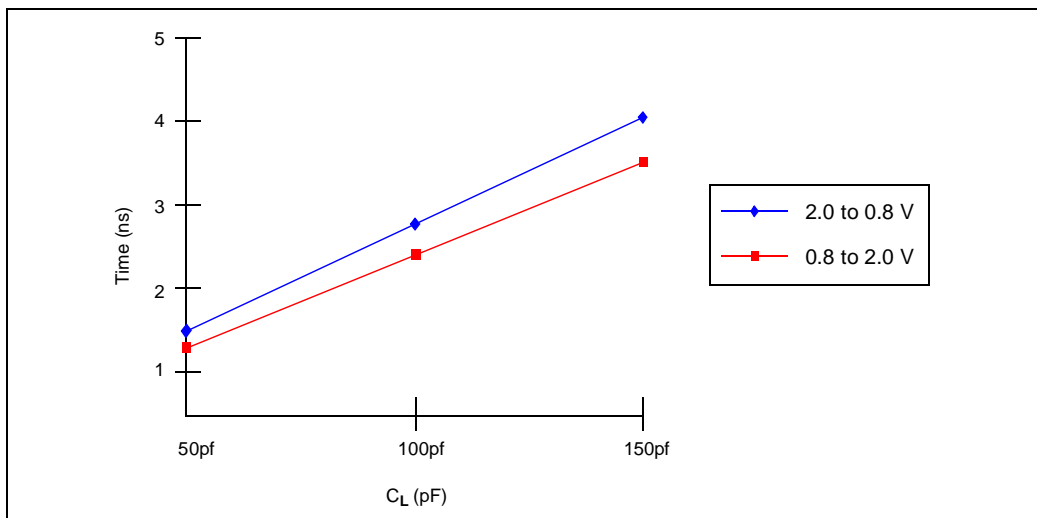
Figure 22. Rise and Fall Time Derating at 85°C and Minimum V$_{CC}$
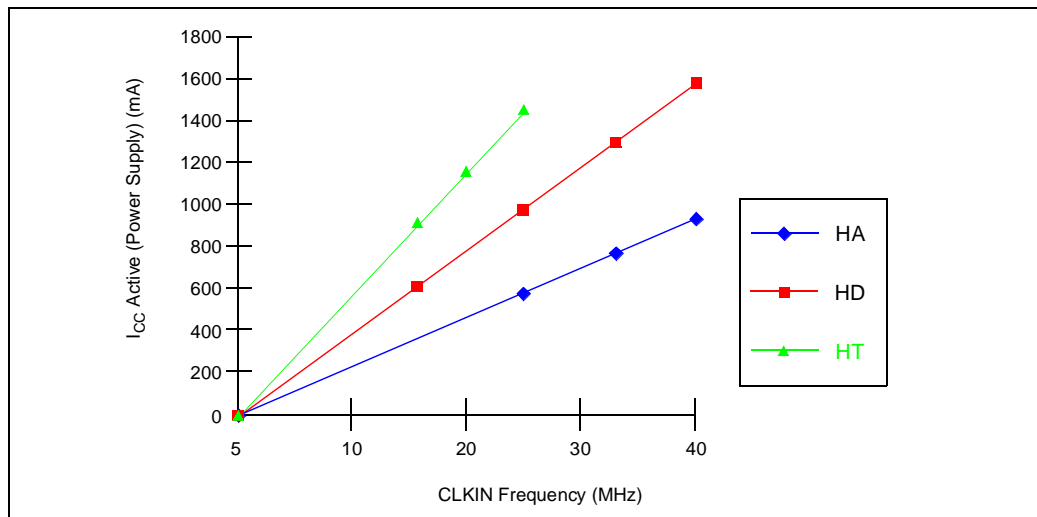
Figure 23. I$_{CC}$ Active (Power Supply) vs. Frequency
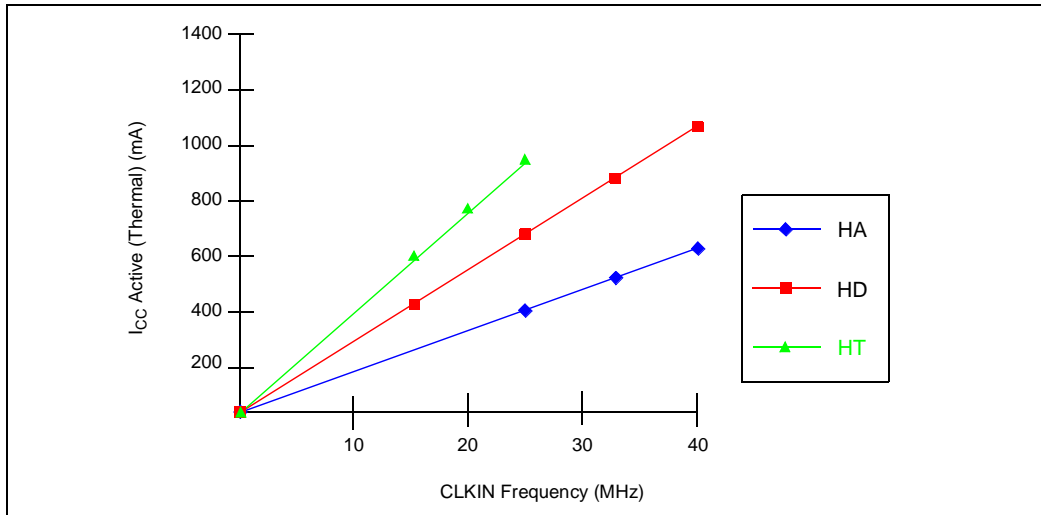
Figure 24. I$_{CC}$ Active (Thermal) vs. Frequency

Figure 25. Output Delay or Hold vs. Load Capacitance

ADVANCE INFORMATION
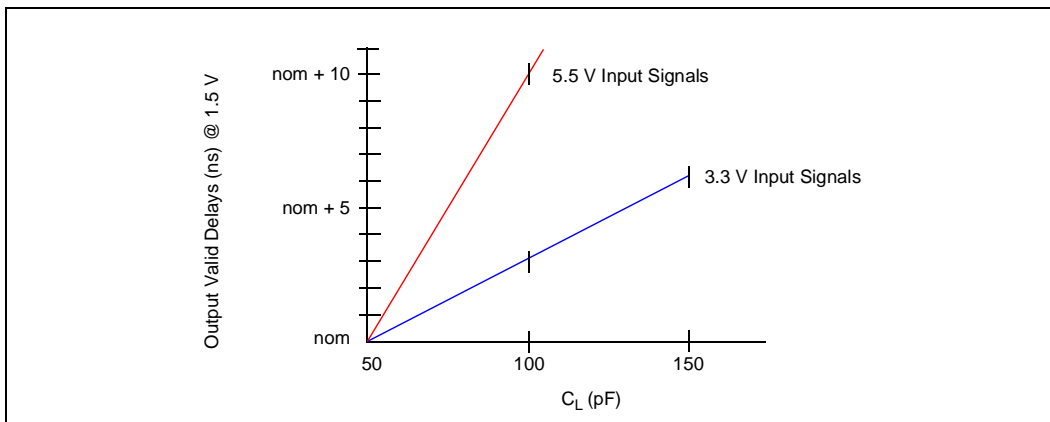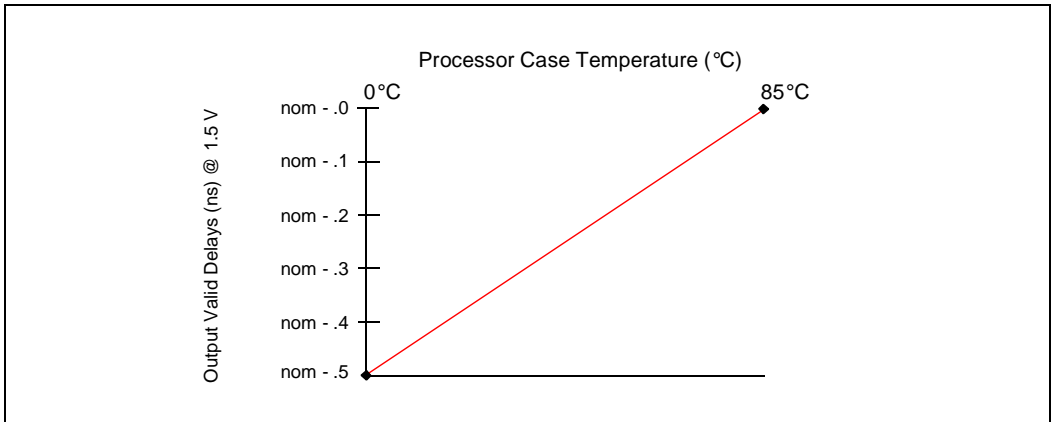
Figure 26. Output Delay vs. Temperature
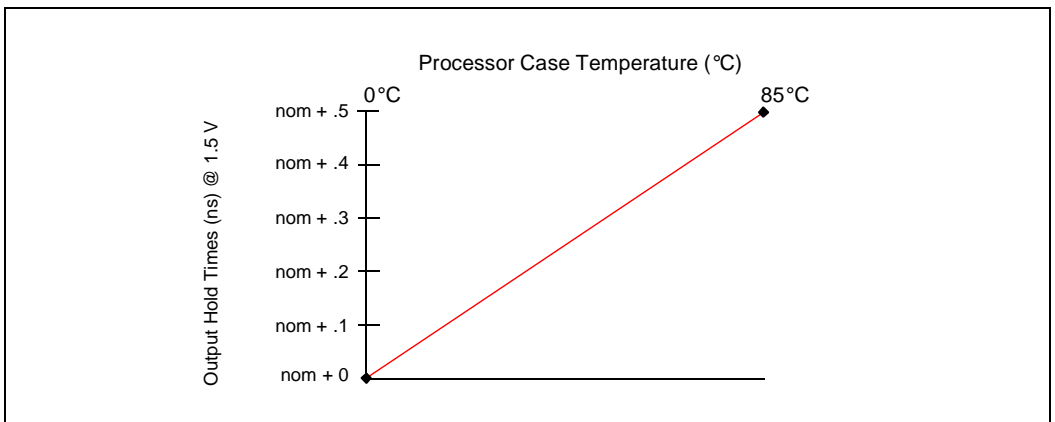
Figure 27. Output Hold Times vs. Temperature
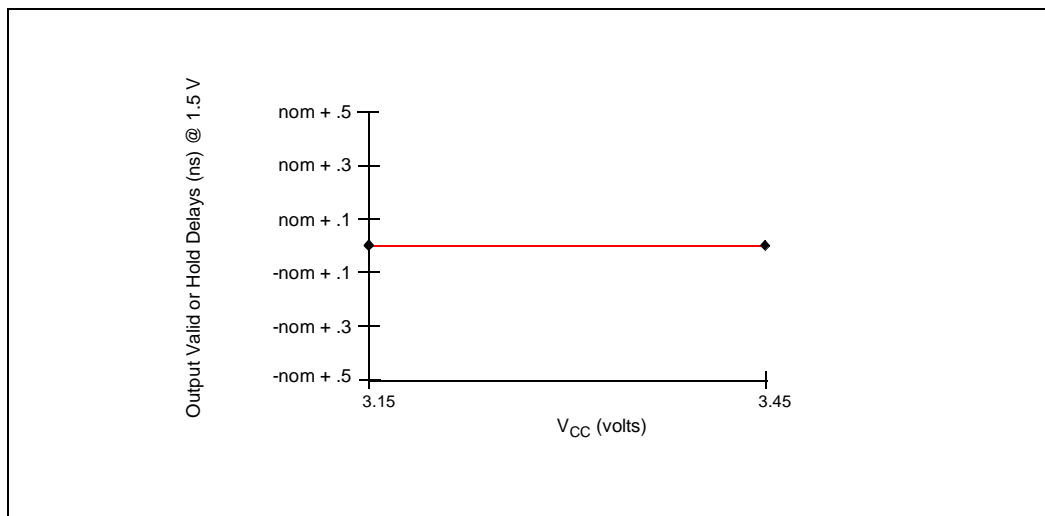
Figure 28. Output Delay vs. V$_{CC}$

ADVANCE INFORMATION

5.0   BUS WAVEFORMS

Figure 29. Cold Reset Waveform

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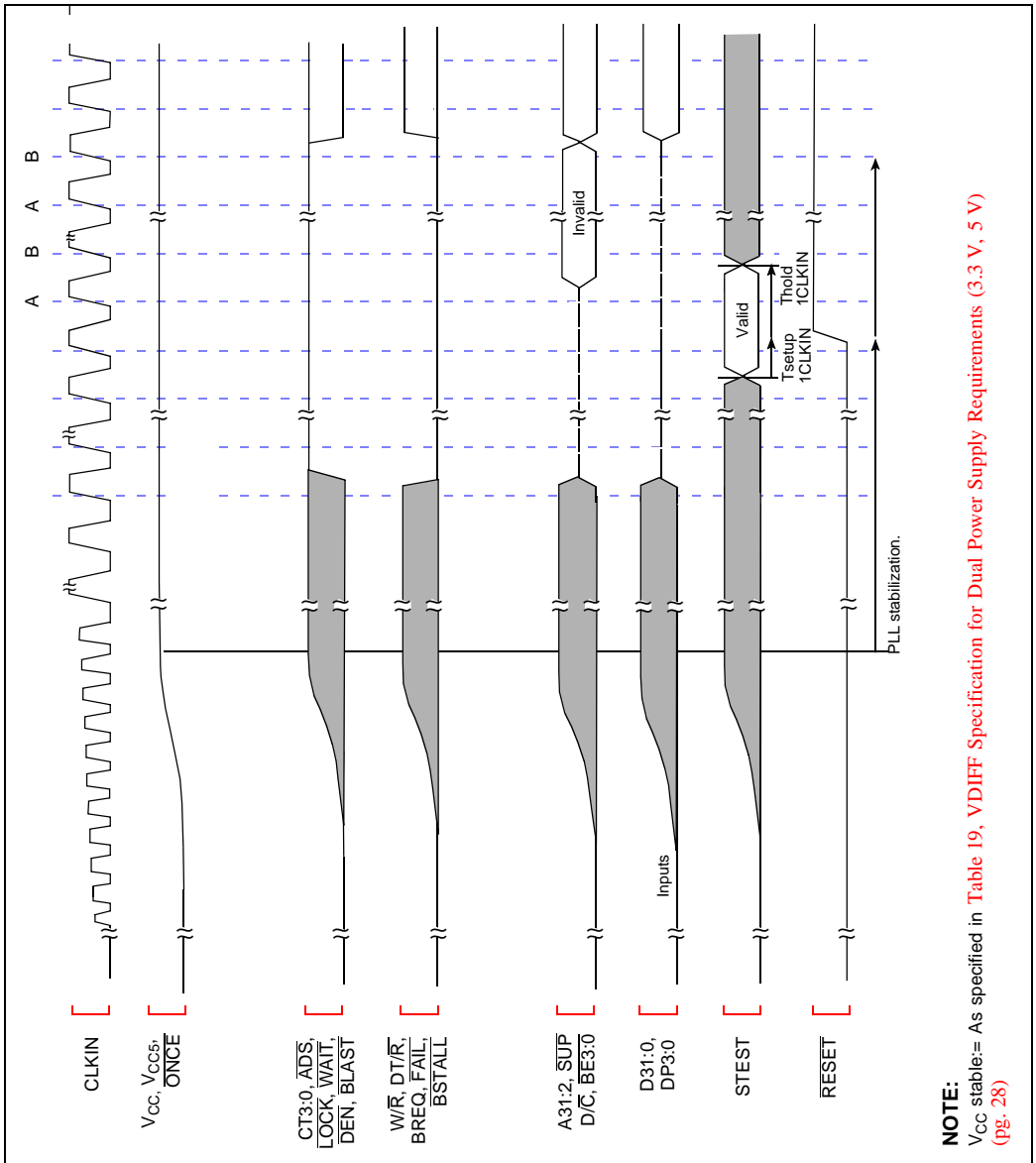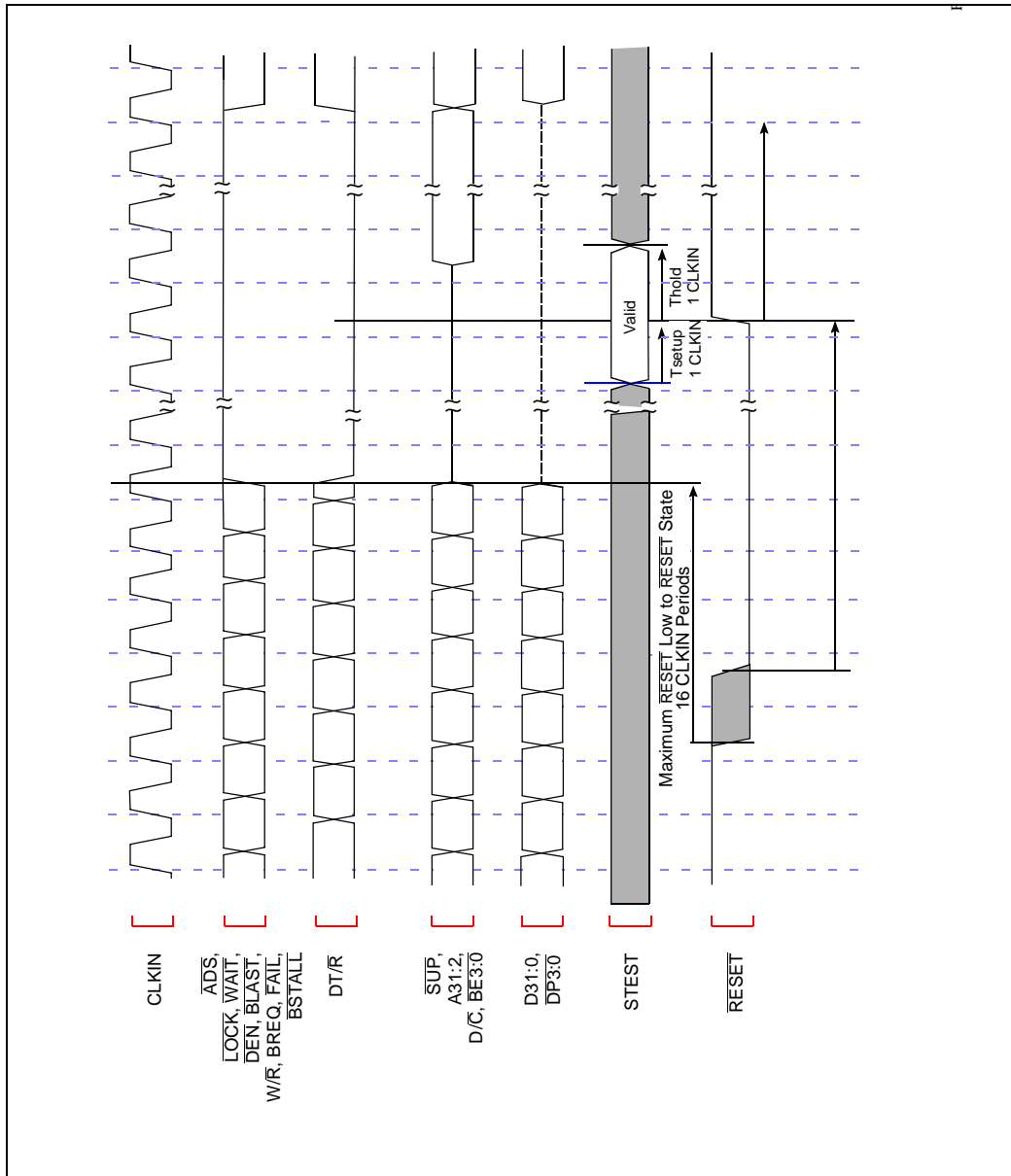
Figure 30. Warm Reset Waveform

ADVANCE INFORMATION
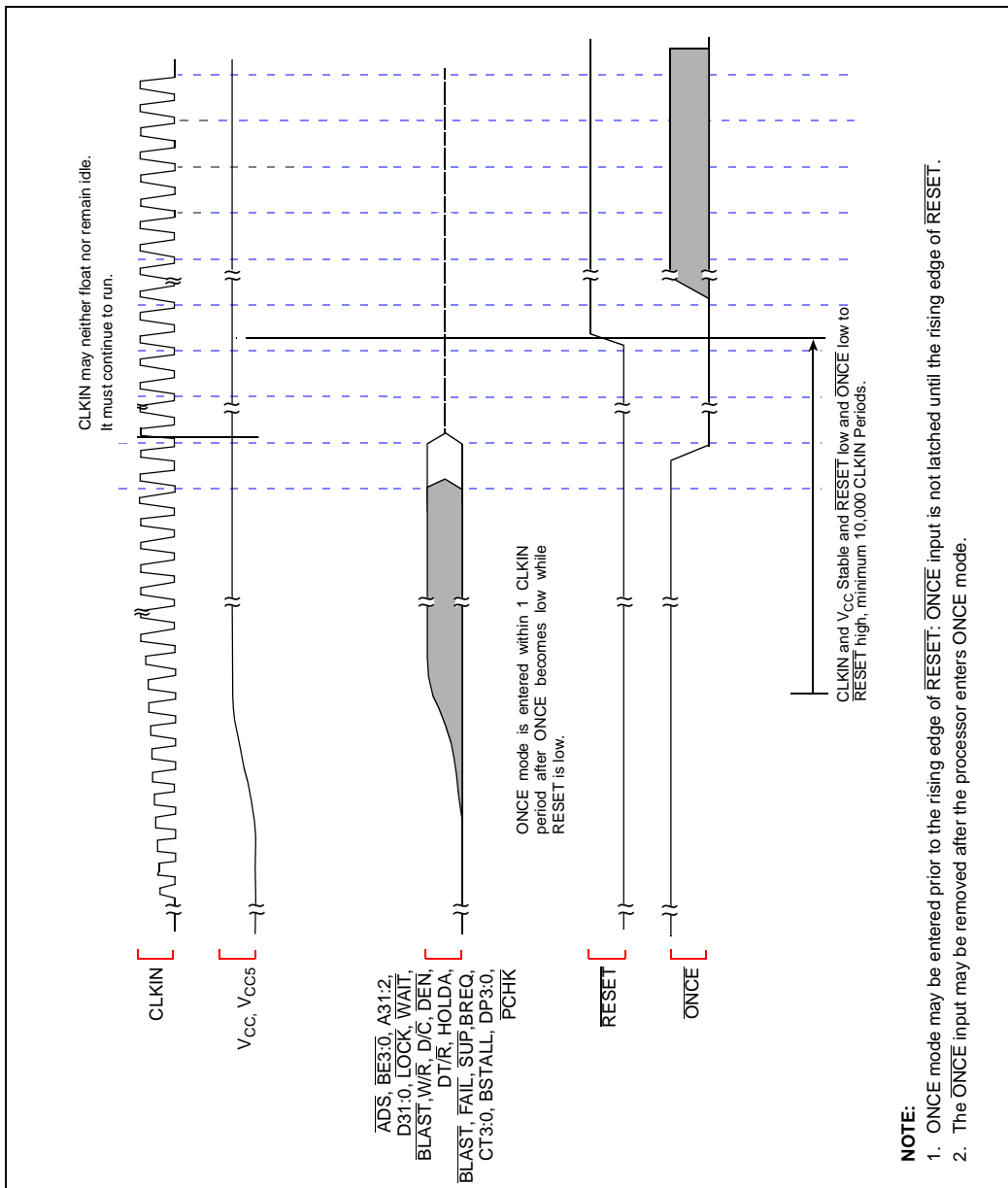
Figure 31. Entering ONCE Mode

CLKIN may neither float nor remain idle.
It must continue to run.

ONCE mode is entered within 1 CLKIN period after ONCE becomes low while RESET is low.

CLKIN and V_{CC} Stable and RESET low and ONCE low to RESET high, minimum 10,000 CLKIN Periods.

CLKIN

V_{CC}, V_{CC5}

$\overline{ADS}$, $\overline{BE3:0}$, A31:2, D31:0, $\overline{LOCK}$, $\overline{WAIT}$, $\overline{BLAST}$, W/$\overline{R}$, D/$\overline{C}$, $\overline{DEN}$, DT/$\overline{R}$, $\overline{HOLDA}$, $\overline{BLAST}$, $\overline{FAIL}$, $\overline{SUP}$, $\overline{BREQ}$, CT3:0, $\overline{BSTALL}$, DP3:0, $\overline{PCHK}$

$\overline{RESET}$

$\overline{ONCE}$

CLKIN and V_{CC} Stable and RESET low and ONCE low to RESET high, minimum 10,000 CLKIN Periods.

NOTE:
1. ONCE mode may be entered prior to the rising edge of $\overline{RESET}$. $\overline{ONCE}$ input is not latched until the rising edge of $\overline{RESET}$.
2. The $\overline{ONCE}$ input may be removed after the processor enters ONCE mode.

PMCON Function	External Ready Control	Burst	Pipe-Lining	Bus Width	Odd Parity	Parity Enable	N_{XDA}	N_{WDD}	N_{WAD}	N_{RDD}	N_{RAD}
Bit	29	28	24	23-22	21	20	19-16	15-14	12-8	7-6	4-0
Value	Disabled 0	Disabled 0	OFF 0	X xx	X x	Enabled 1	0 0000	0 00	0 00000	0 00	0 00000

NOTICE: Bits 31-30, 27-25, 13, and 5 are reserved.

Figure 32. Non-Burst, Non-Pipelined Requests without Wait States

ADVANCE INFORMATION

PMCON Function	External Ready Control	Burst	Pipe-Lining	Bus Width	Odd Parity	Parity Enable	N$_{XDA}$	N$_{WDD}$	N$_{WAD}$	N$_{RDD}$	N$_{RAD}$
Bit	29	28	24	23-22	21	20	19-16	15-14	12-8	7-6	4-0
Value	Disabled 0	Disabled 0	OFF 0	X xx	X x	Enabled 1	1 0001	X xx	X xxxxx	X xx	3 00011

NOTICE: Bits 31-30, 27-25, 13, and 5 are reserved.
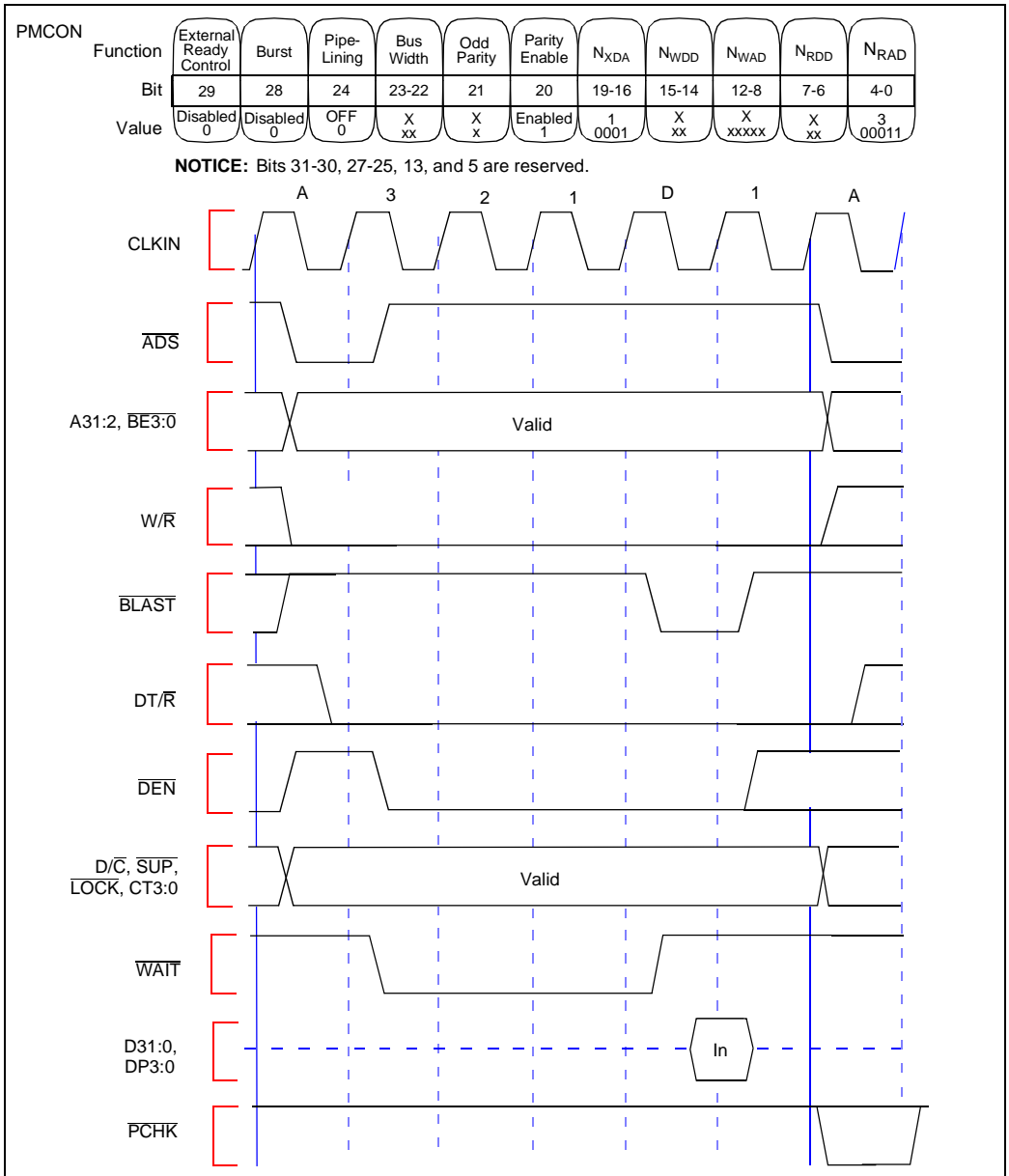
Figure 33. Non-Burst, Non-Pipelined Read Request with Wait States

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PMCON		External Ready Control	Burst	Pipe-Lining	Bus Width	Odd Parity	Parity Enable	N_XDA	N_WDD	N_WAD	N_RDD	N_RAD
	Function	External Ready Control	Burst	Pipe-Lining	Bus Width	Odd Parity	Parity Enable	N_XDA	N_WDD	N_WAD	N_RDD	N_RAD
	Bit	29	28	24	23-22	21	20	19-16	15-14	12-8	7-6	4-0
	Value	Disabled 0	Disabled 0	OFF 0	X xx	X x	Enabled 1	1 0001	X xxxxx	3 00011	X xx	X xxxxx

NOTICE: Bits 31-30, 27-25, 13, and 5 are reserved.
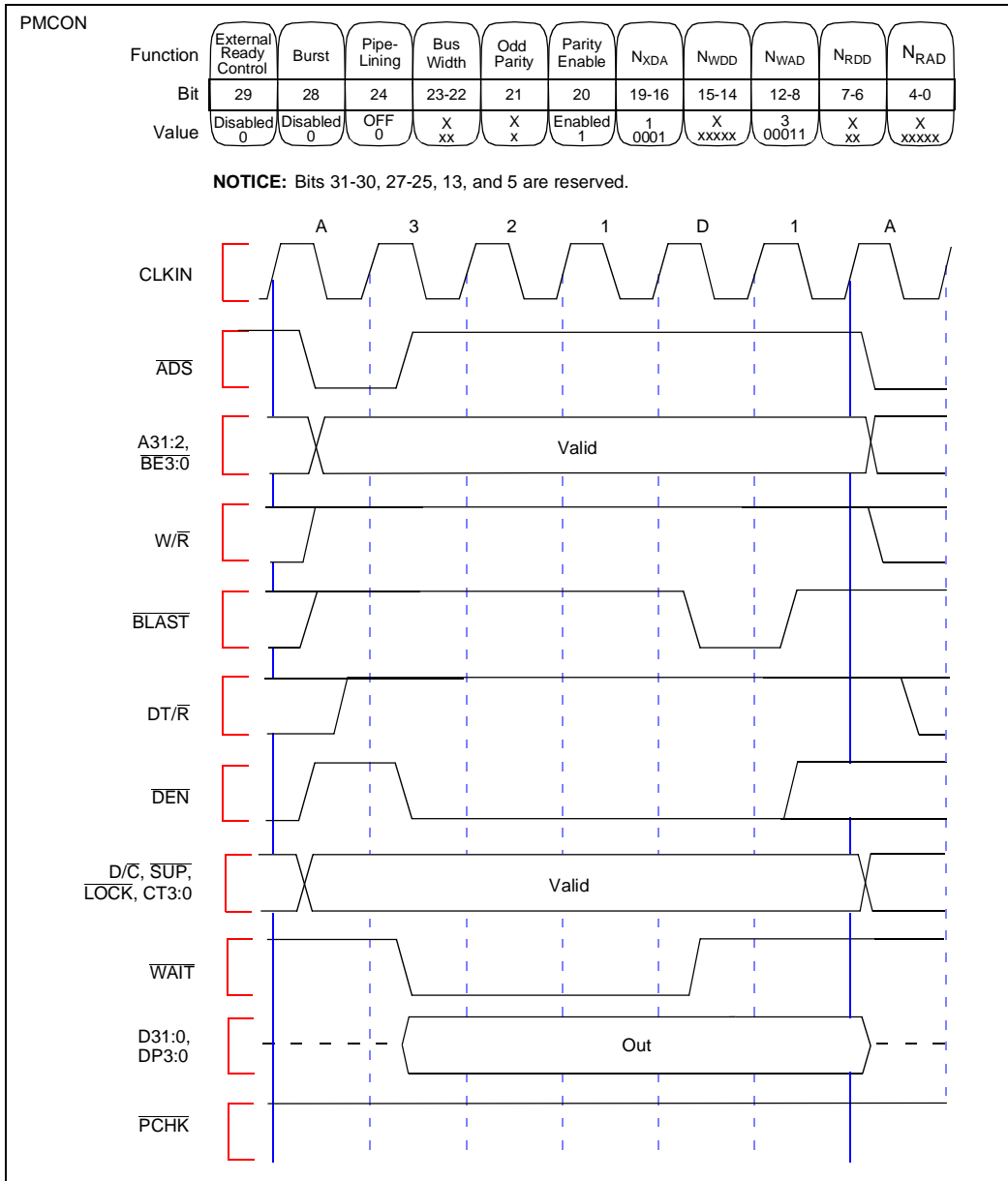
Figure 34. Non-Burst, Non-Pipelined Write Request with Wait States

ADVANCE INFORMATION

PMCON											
Function	External Ready Control	Burst	Pipe-Lining	Bus Width	Odd Parity	Parity Enable	N_{XDA}	N_{WDD}	N_{WAD}	N_{RDD}	N_{RAD}
Bit	29	28	24	23-22	21	20	19-16	15-14	12-8	7-6	4-0
Value	Disabled 0	Enabled 1	OFF 0	32-Bit 10	X x	Enabled 1	0 0000	X xx	X xxxxx	0 00	0 00000

NOTICE: Bits 31-30, 27-25, 13, and 5 are reserved.

Figure 35. Burst, Non-Pipelined Read Request without Wait States, 32-Bit Bus

PMCON

Function	External Ready Control	Burst	Pipe-Lining	Bus Width	Odd Parity	Parity Enable	N_{XDA}	N_{WDD}	N_{WAD}	N_{RDD}	N_{RAD}
Bit	29	28	24	23-22	21	20	19-16	15-14	12-8	7-6	4-0
Value	Disabled 0	Enabled 1	OFF 0	32-Bit 10	X x	Enabled 1	1 0001	X xx	X xxxxx	1 01	2 00010

NOTICE: Bits 31-30, 27-25, 13, and 5 are reserved.

Figure 36. Burst, Non-Pipelined Read Request with Wait States, 32-Bit Bus

NOTICE: Bits 31-30, 27-25, 13, and 5 are reserved.

PMCON Function	External Ready Control	Burst	Pipe-Lining	Bus Width	Odd Parity	Parity Enable	N_{XDA}	N_{WDD}	N_{WAD}	N_{RDD}	N_{RAD}
Bit	29	28	24	23-22	21	20	19-16	15-14	12-8	7-6	4-0
Value	Disabled 0	Enabled 1	OFF 0	32-Bit 10	X x	Enabled 1	0 0000	0 00	0 00000	X xx	X xxxxx
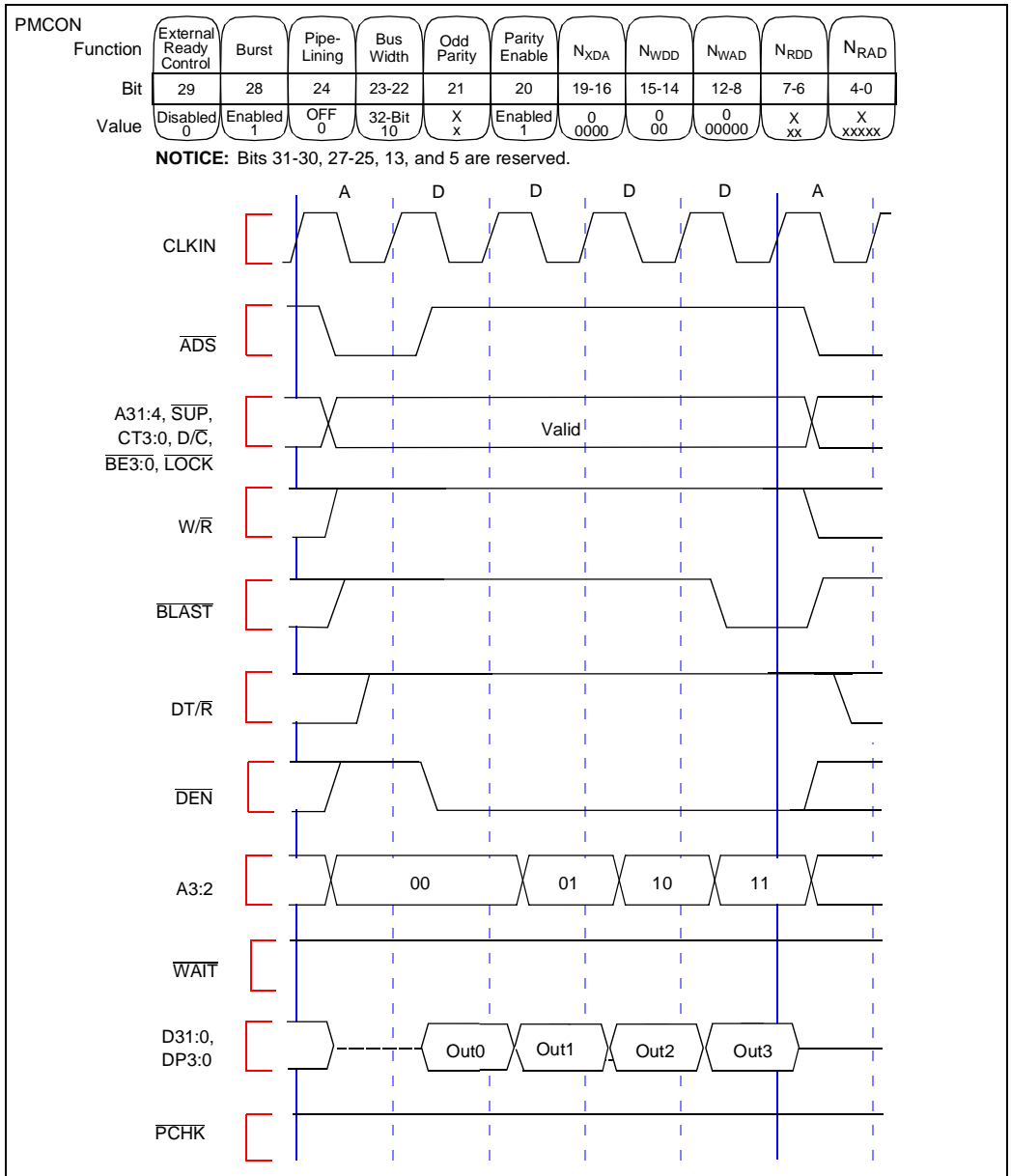
Figure 37. Burst, Non-Pipelined Write Request without Wait States, 32-Bit Bus

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PMCON

Function	External Ready Control	Burst	Pipe-Lining	Bus Width	Odd Parity	Parity Enable	N_{XDA}	N_{WDD}	N_{WAD}	N_{RDD}	N_{RAD}
Bit	29	28	24	23-22	21	20	19-16	15-14	12-8	7-6	4-0
Value	Disabled 0	Enabled 1	OFF 0	32-bit 10	X x	Enabled 1	1 0001	1 01	2 00010	X xx	X xxxxx

NOTICE: Bits 31-30, 27-25, 13, and 5 are reserved.
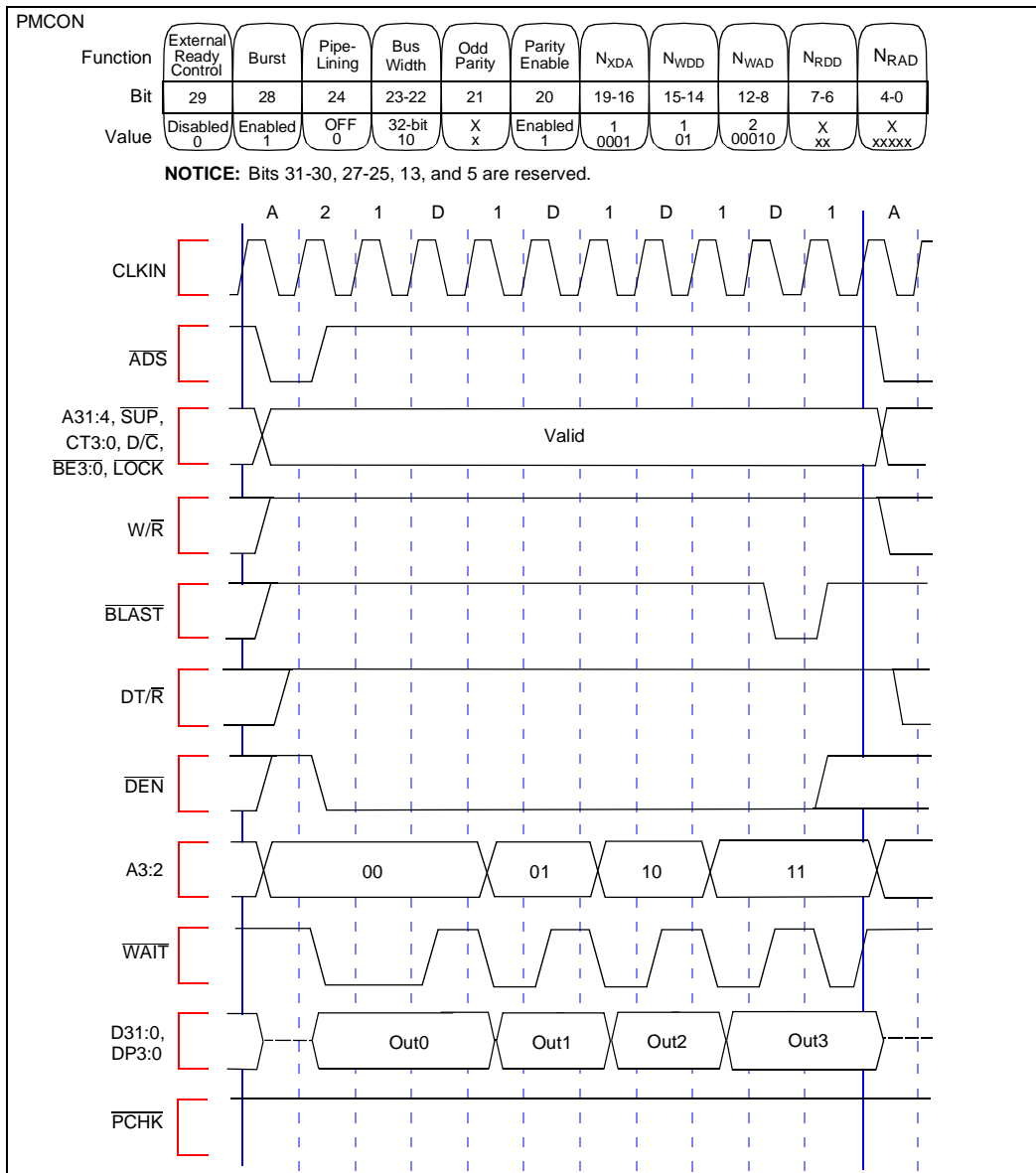
Figure 38. Burst, Non-Pipelined Write Request with Wait States, 32-Bit Bus

ADVANCE INFORMATION

PMCON Function	External Ready Control	Burst	Pipe-Lining	Bus Width	Odd Parity	Parity Enable	N$_{XDA}$	N$_{WDD}$	N$_{WAD}$	N$_{RDD}$	N$_{RAD}$
Bit	29	28	24	23-22	21	20	19-16	15-14	12-8	7-6	4-0
Value	Disabled 0	Enabled 1	OFF 0	16-Bit 01	X x	Enabled 1	1 0001	X xx	X xxxxx	1 01	2 00010

NOTICE: Bits 31-30, 27-25, 13, and 5 are reserved.
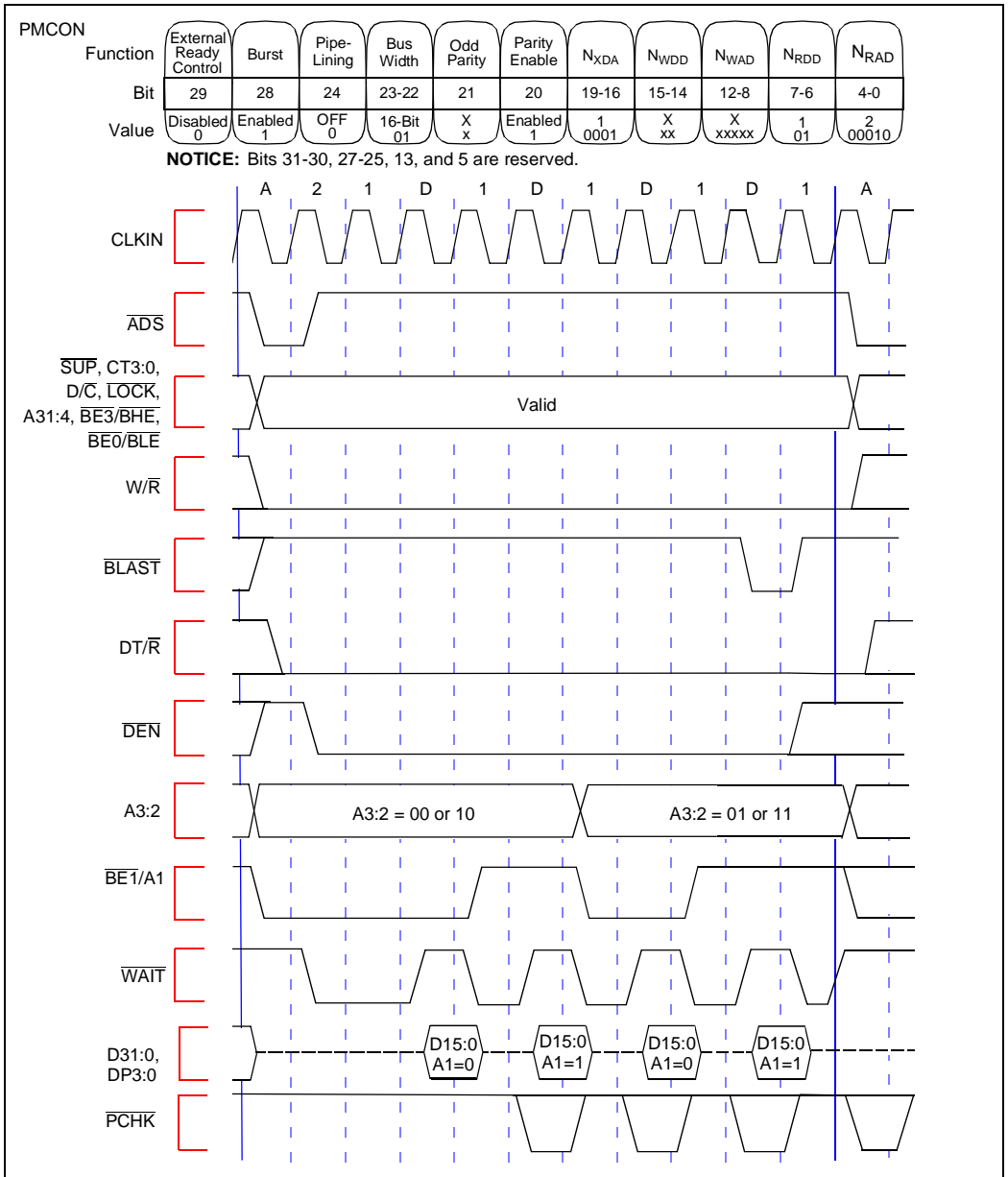
Figure 39. Burst, Non-Pipelined Read Request with Wait States, 16-Bit Bus

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PMCON											
Function	External Ready Control	Burst	Pipe-Lining	Bus Width	Odd Parity	Parity Enable	N$_{XDA}$	N$_{WDD}$	N$_{WAD}$	N$_{RDD}$	N$_{RAD}$
Bit	29	28	24	23-22	21	20	19-16	15-14	12-8	7-6	4-0
Value	Disabled 0	Enabled 1	OFF 0	8-Bit 00	X x	Enabled 1	1 0001	X xx	X xxxxx	1 01	2 00010

NOTICE: Bits 31-30, 27-25, 13, and 5 are reserved.
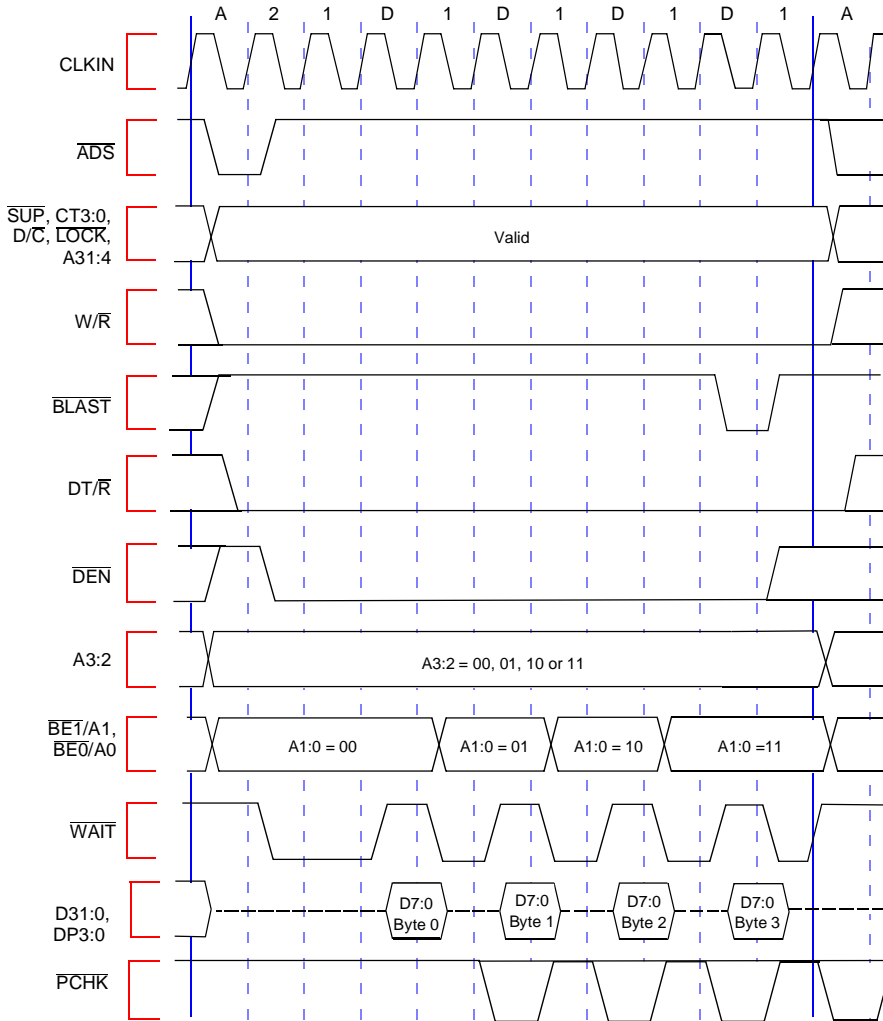
Figure 40. Burst, Non-Pipelined Read Request with Wait States, 8-Bit Bus

ADVANCE INFORMATION

PMCON Function	External Ready Control	Burst	Pipe-Lining	Bus Width	Odd Parity	Parity Enable	N_{XDA}	N_{WDD}	N_{WAD}	N_{RDD}	N_{RAD}
Bit	29	28	24	23-22	21	20	19-16	15-14	12-8	7-6	4-0
Value	X x	Disabled 0	ON 1	32-Bit 10	X x	Enabled 1	X xxxx	X xx	X xxxxx	X xx	0 00000

PMCON Function: External Ready Control (N_{XDA}), Burst, Pipe-Lining, Bus Width, Odd Parity, Parity Enable, N_{XDA}, N_{WDD}, N_{WAD}, N_{RDD}, N_{RAD}

NOTICE: Bits 31-30, 27-25, 13, and 5 are reserved.

1. Non-pipelined request concludes, pipelined reads begin.
2. Pipelined reads conclude, non-pipelined requests begin.

Figure 41. Non-Burst, Pipelined Read Request without Wait States, 32-Bit Bus

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PMCON Function	External Ready Control	Burst	Pipe-Lining	Bus Width	Odd Parity	Parity Enable	N_XDA	N_WDD	N_WAD	N_RDD	N_RAD
Bit	29	28	24	23-22	21	20	19-16	15-14	12-8	7-6	4-0
Value	X x	Disabled 0	ON 1	32-Bit 10	X x	Enabled 1	X xxxx	X xx	X xxxxx	X xx	1 00001

NOTICE: Bits 31-30, 27-25, 13, and 5 are reserved.

1. Non-pipelined request concludes, pipelined reads begin
2. Pipelined reads conclude, non-pipelined requests begin
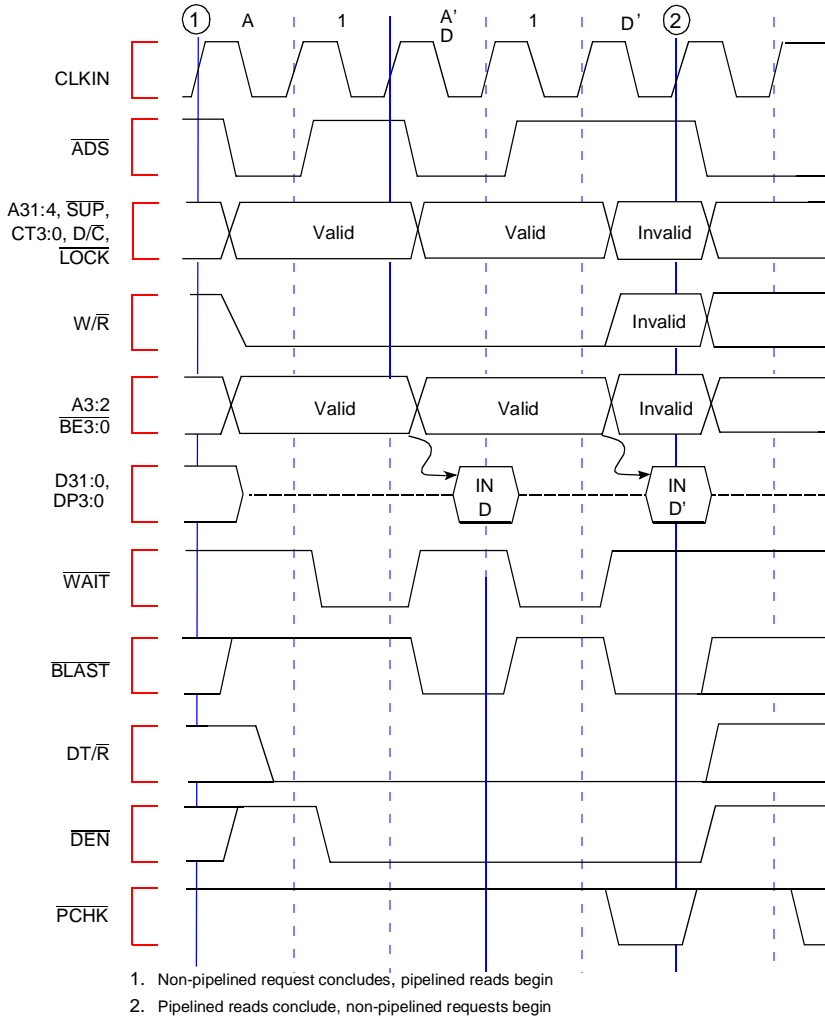
Figure 42. Non-Burst, Pipelined Read Request with Wait States, 32-Bit Bus

ADVANCE INFORMATION

PMCON Function	External Ready Control	Burst	Pipe-Lining	Bus Width	Odd Parity	Parity Enable	N_{XDA}	N_{WDD}	N_{WAD}	N_{RDD}	N_{RAD}
Bit	29	28	24	23-22	21	20	19-16	15-14	12-8	7-6	4-0
Value	X x	Enabled 1	ON 1	32-Bit 10	X x	Enabled 1	X xxxx	X xx	X xxxxx	0 00	0 00000

NOTICE: Bits 31-30, 27-25, 13, and 5 are reserved.

1. Non-pipelined request concludes, pipelined reads begin
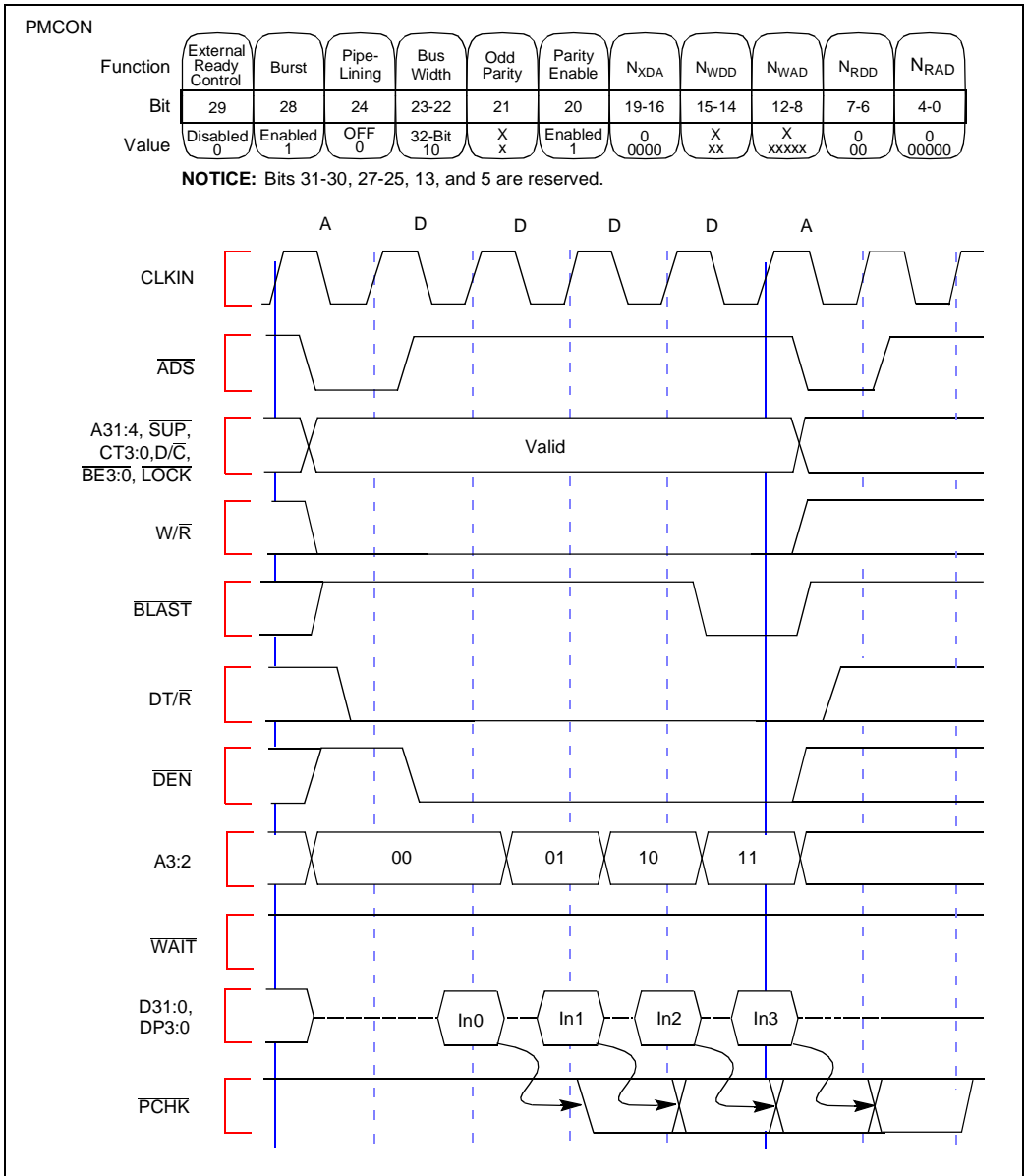2. Pipelined reads conclude, non-pipelined requests begin

Figure 43. Burst, Pipelined Read Request without Wait States, 32-Bit Bus

PMCON Function	External Ready Control	Burst	Pipe-Lining	Bus Width	Odd Parity	Parity Enable	N_XDA	N_WDD	N_WAD	N_RDD	N_RAD
Bit	29	28	24	23-22	21	20	19-16	15-14	12-8	7-6	4-0
Value	X x	Enabled 1	ON 1	32-Bit 10	X x	Enabled 1	X xxxx	X xx	X xxxxx	1 01	2 00010

NOTICE: Bits 31-30, 27-25, 13, and 5 are reserved.

1. Non-pipelined request concludes, pipelined reads begin.
2. Pipelined reads conclude, non-pipelined requests begin.
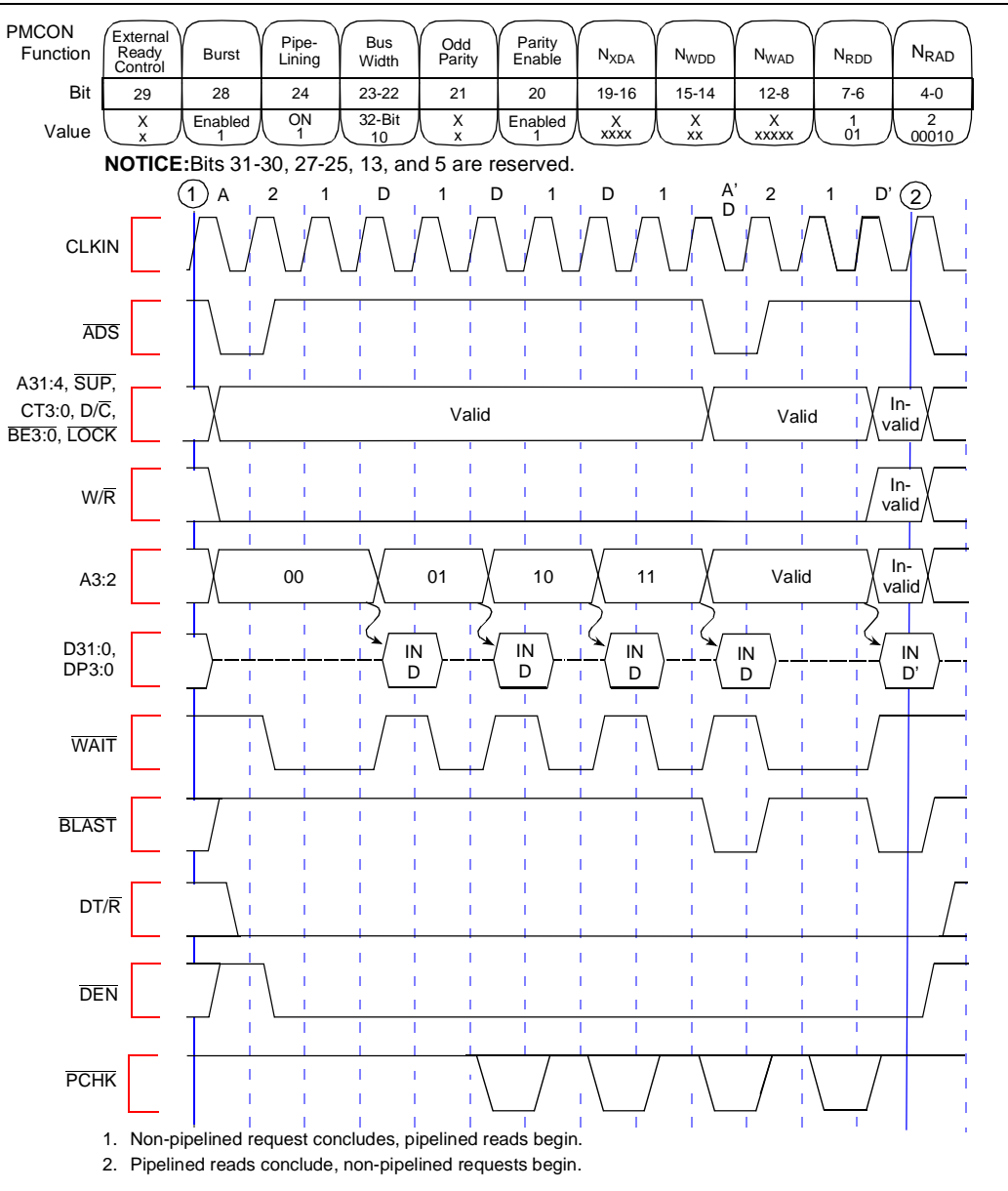
Figure 44. Burst, Pipelined Read Request with Wait States, 32-Bit Bus

ADVANCE INFORMATION
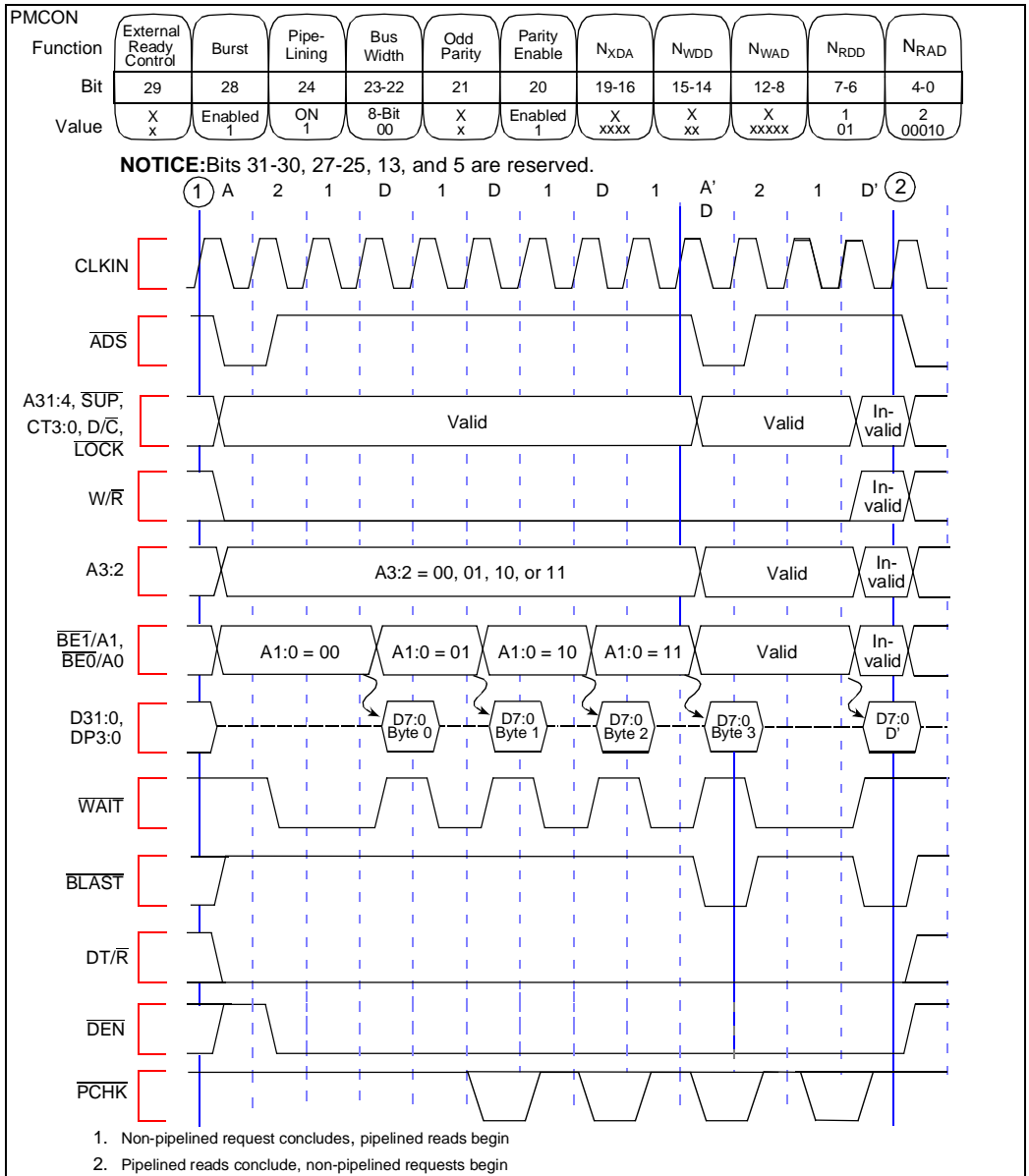
Figure 45. Burst, Pipelined Read Request with Wait States, 8-Bit Bus

PMCON Function	External Ready Control	Burst	Pipe-Lining	Bus Width	Odd Parity	Parity Enable	N$_{XDA}$	N$_{WDD}$	N$_{WAD}$	N$_{RDD}$	N$_{RAD}$
Bit	29	28	24	23-22	21	20	19-16	15-14	12-8	7-6	4-0
Value	X x	Enabled 1	ON 1	16-Bit 01	X x	Enabled 1	X xxxx	X xx	X xxxxx	1 01	2 00010
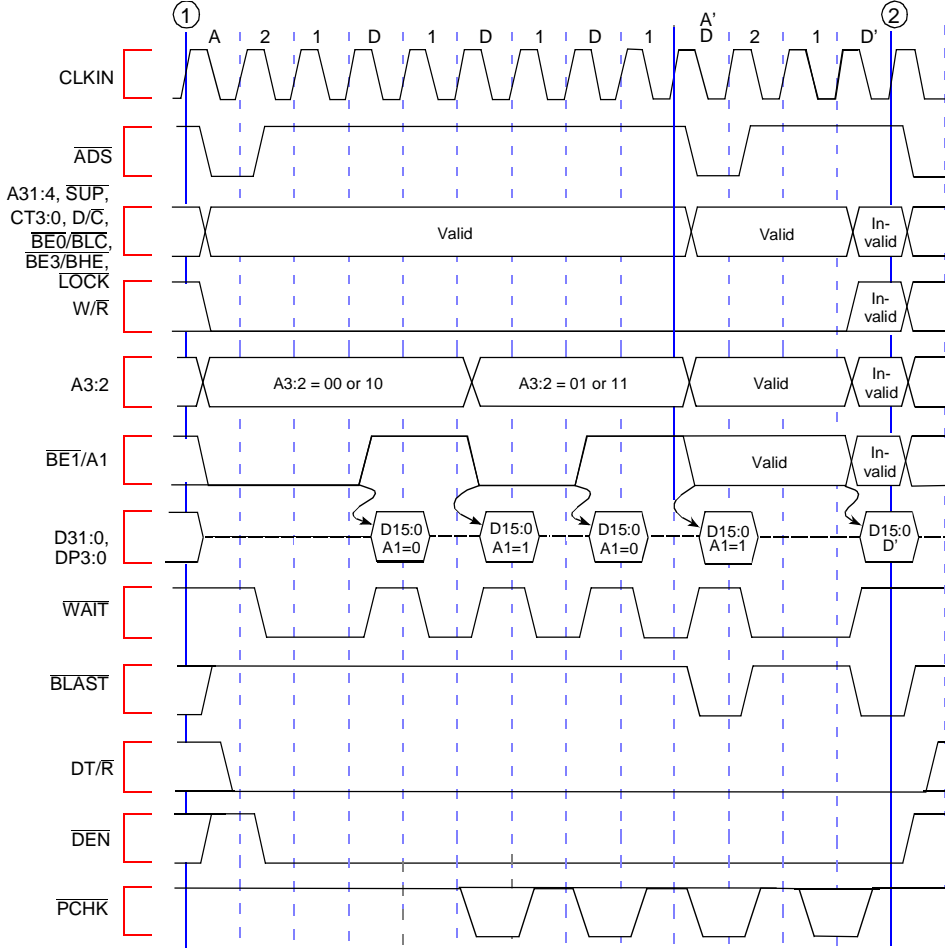
NOTICE: Bits 31-30, 27-25, 13, and 5 are reserved.

1. Non-pipelined request concludes, pipelined reads begin
2. Pipelined reads conclude, non-pipelined requests begin

Figure 46. Burst, Pipelined Read Request with Wait States, 16-Bit Bus

ADVANCE INFORMATION
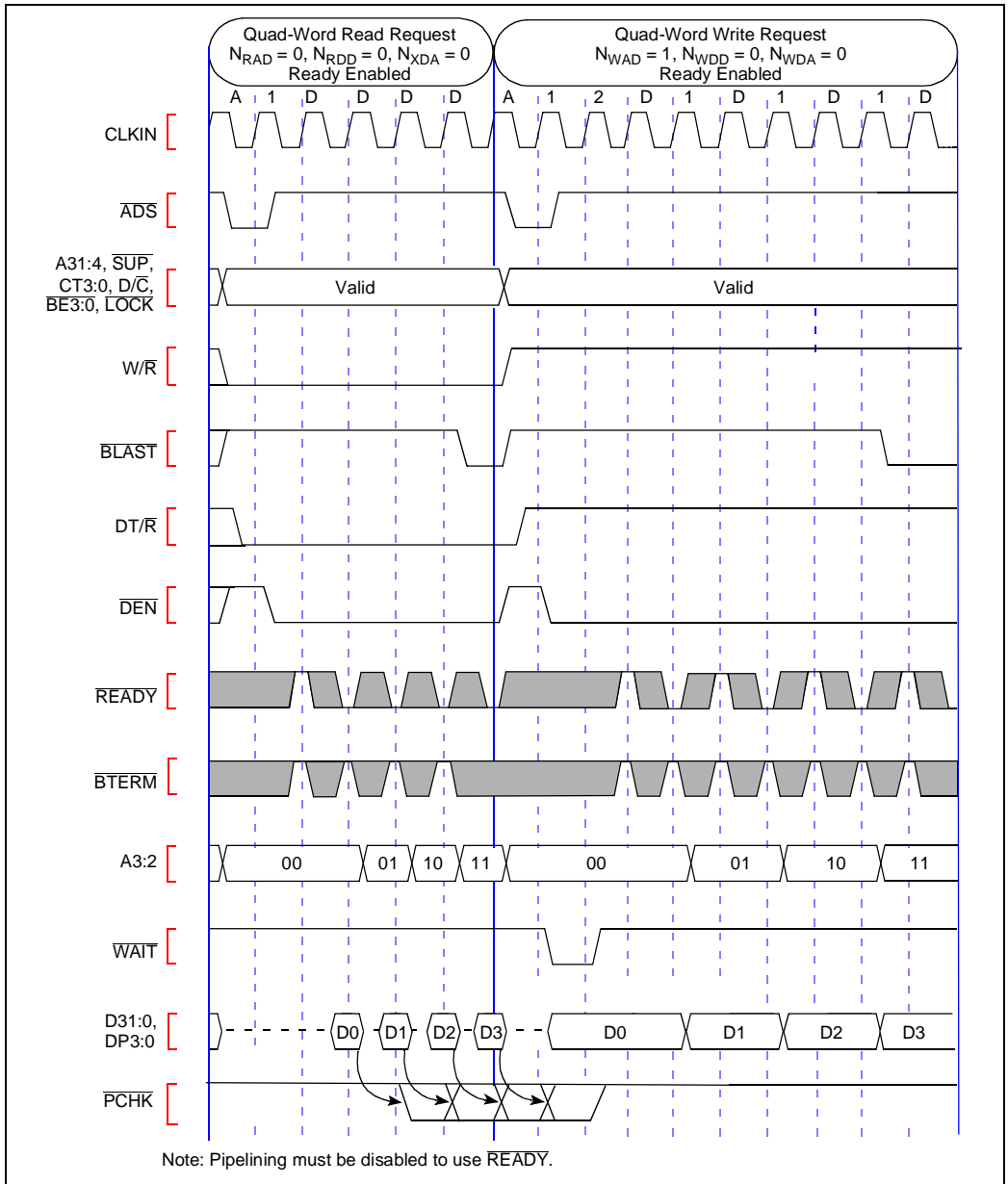
Figure 47. Using External READY
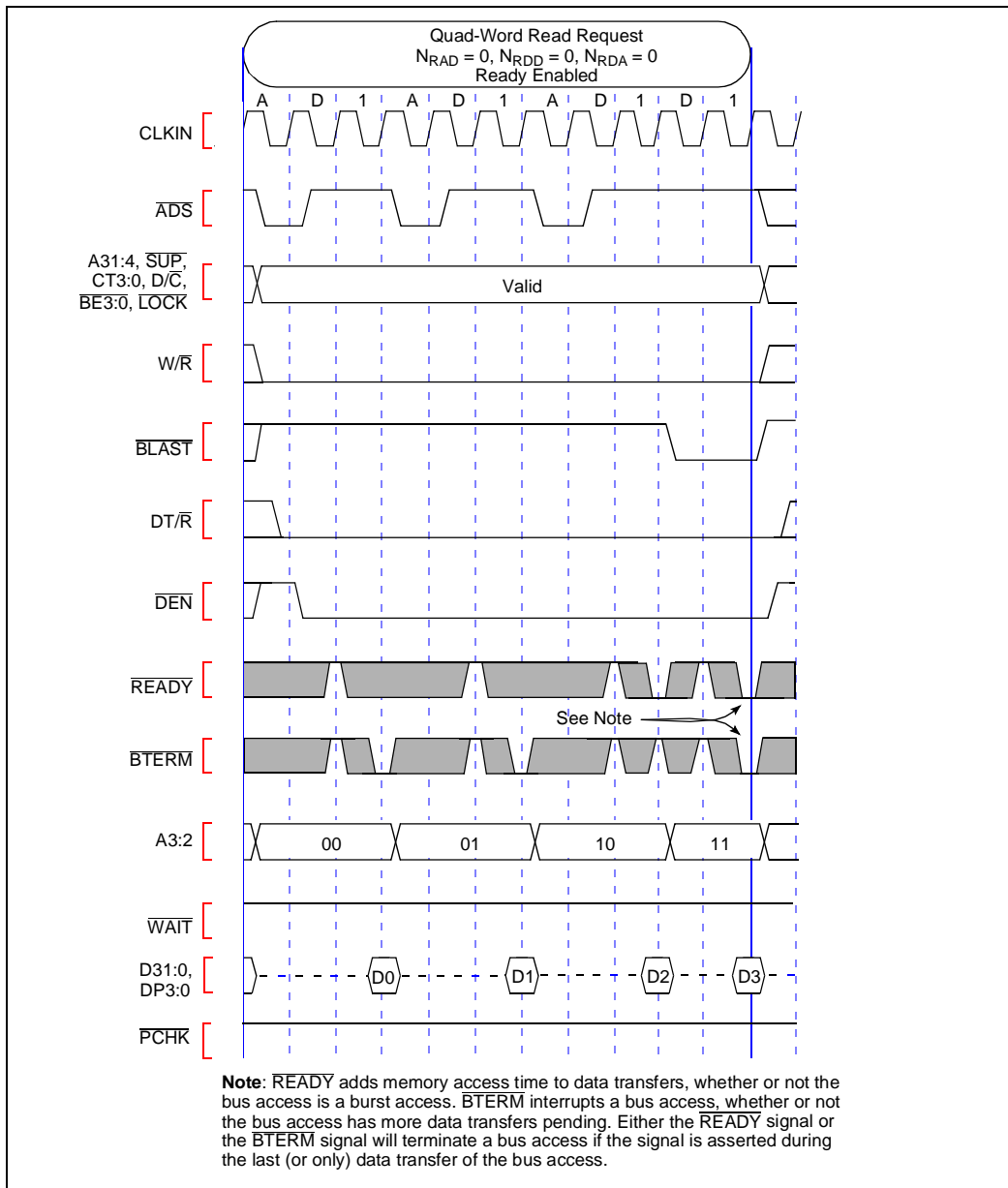
Figure 48. Terminating a Burst with $\overline{\text{BTERM}}$

ADVANCE INFORMATION
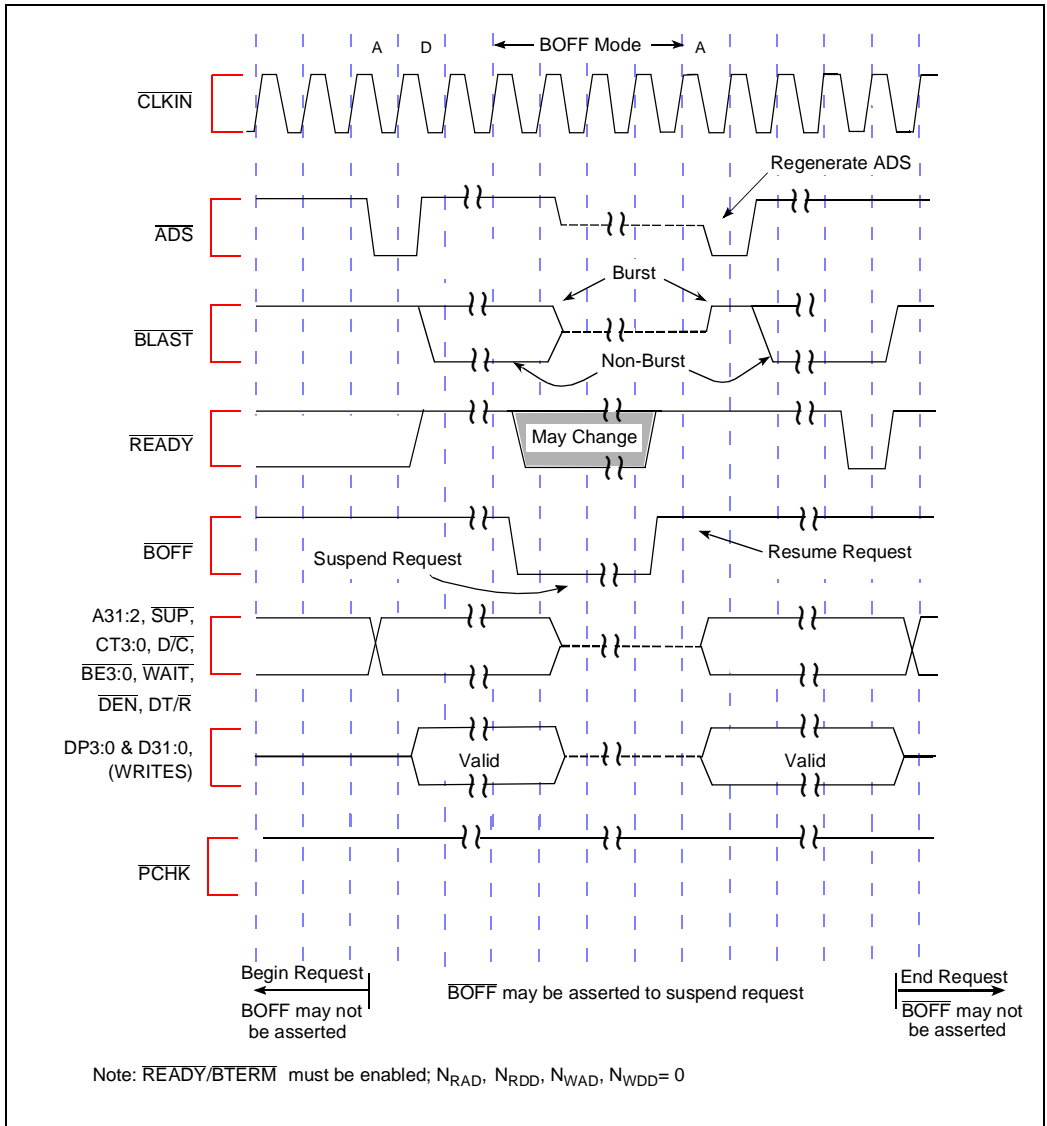
Figure 49. BOFF Functional Timing. BOFF occurs during a burst or non-burst data cycle.

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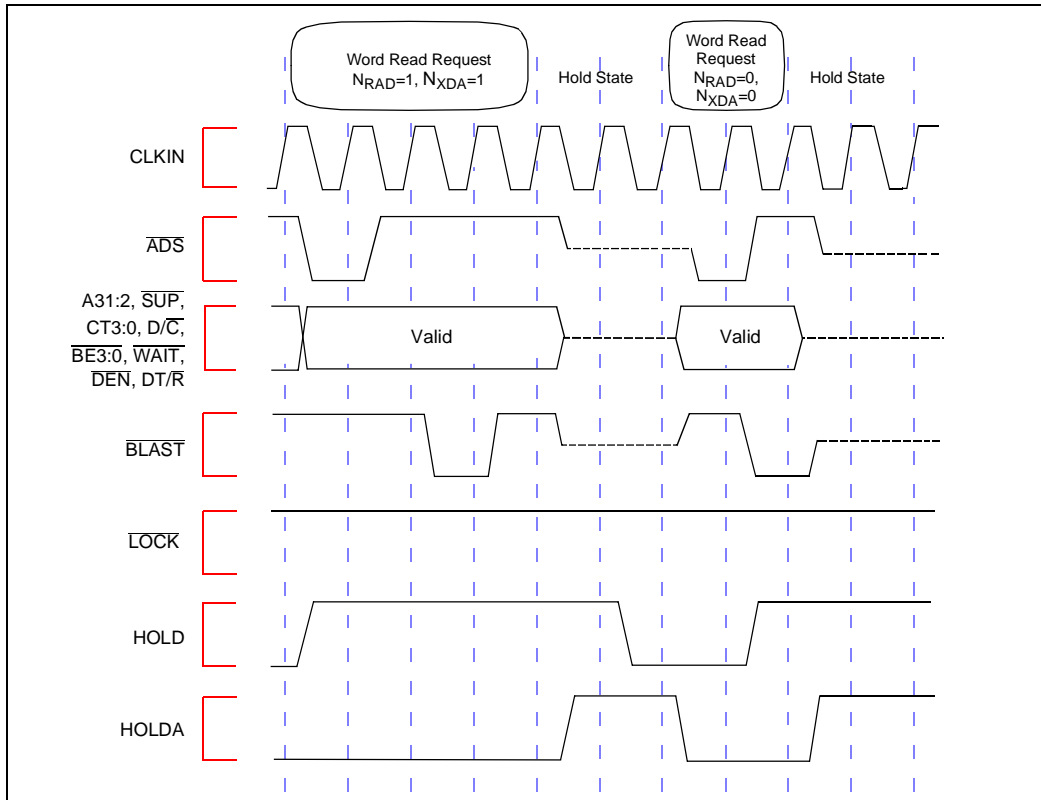
Figure 50. HOLD Functional Timing

ADVANCE INFORMATION
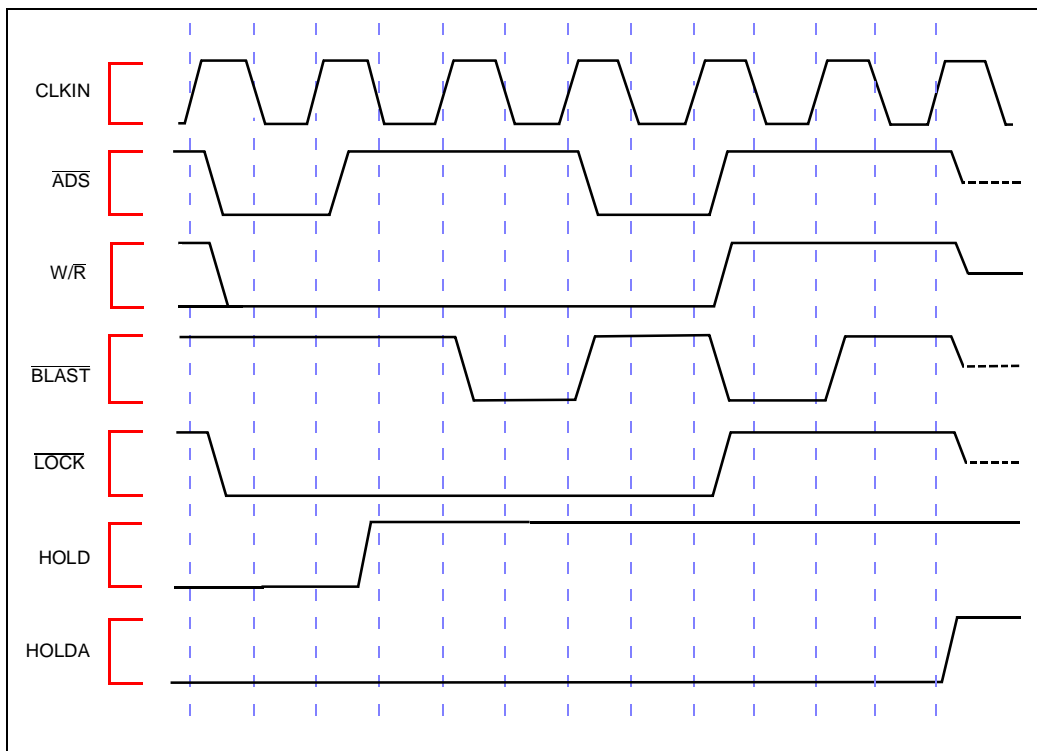
Figure 51. Lock Delays HOLDA Timing

		(Internal Self-Test) Pass		(Bus Test) Pass
		— Fail — —		— — Fail — —
80960HA:	257,517 Cycles	30 Cycles	113 Cycles	
80960HD:	128,761 Cycles	15 Cycles	94 Cycles	
80960HT:	85,840 Cycles	10 Cycles	90 Cycles	

Figure 52. $\overline{\text{FAIL}}$ Functional Timing

ADVANCE INFORMATION

Figure 53. A Summary of Aligned and Unaligned Transfers for 32-Bit Regions

NOTE:

1. All requests that are less than a word in size and are cacheable will be promoted to a word to be cached. This causes adjacent requests to occur for full words to the same address.

ADVANCE INFORMATION

Figure 54. A Summary of Aligned and Unaligned Transfers for 32-Bit Regions (Continued)

NOTE:

1. All requests that are less than a word in size and are cacheable will be promoted to a word to be cached. This causes adjacent requests to occur for full words to the same address.

Byte Offset

0   4   8   12   16   20   24

Word Offset

0   1   2   3   4   5   6

**Short
16-Bit Bus**

Short

Byte, Byte

Short

Byte, Byte

**Word
16-Bit Bus**

Two Short Burst

Byte, Short, Byte

(Short)*2

Byte, Short, Byte

Two Short Burst

**Double Word
16-Bit Bus**

Four Short Burst

(Byte, Short, Byte) *2

(Short) *4

(Byte, Short, Byte)*2

(Two Short Burst)*2

Four Short Burst

**Triple Word
16-Bit Bus**

Four Short Burst, Two Short Burst

(Byte, Short, Byte) *3

(Short) *6

(Byte, Short, Byte) *3

(Two Short Burst) *3

(Two Short Burst) *3

**Quad Word
16-Bit Bus**

(Four Short Burst)*2

(Byte, Short, Byte) *4

(Short) *8

(Byte, Short, Byte) *4

(Two Short Burst)*4

(Two Short Burst) *4

Figure 55. A Summary of Aligned and Unaligned Transfers for 16-Bit Bus

ADVANCE INFORMATION
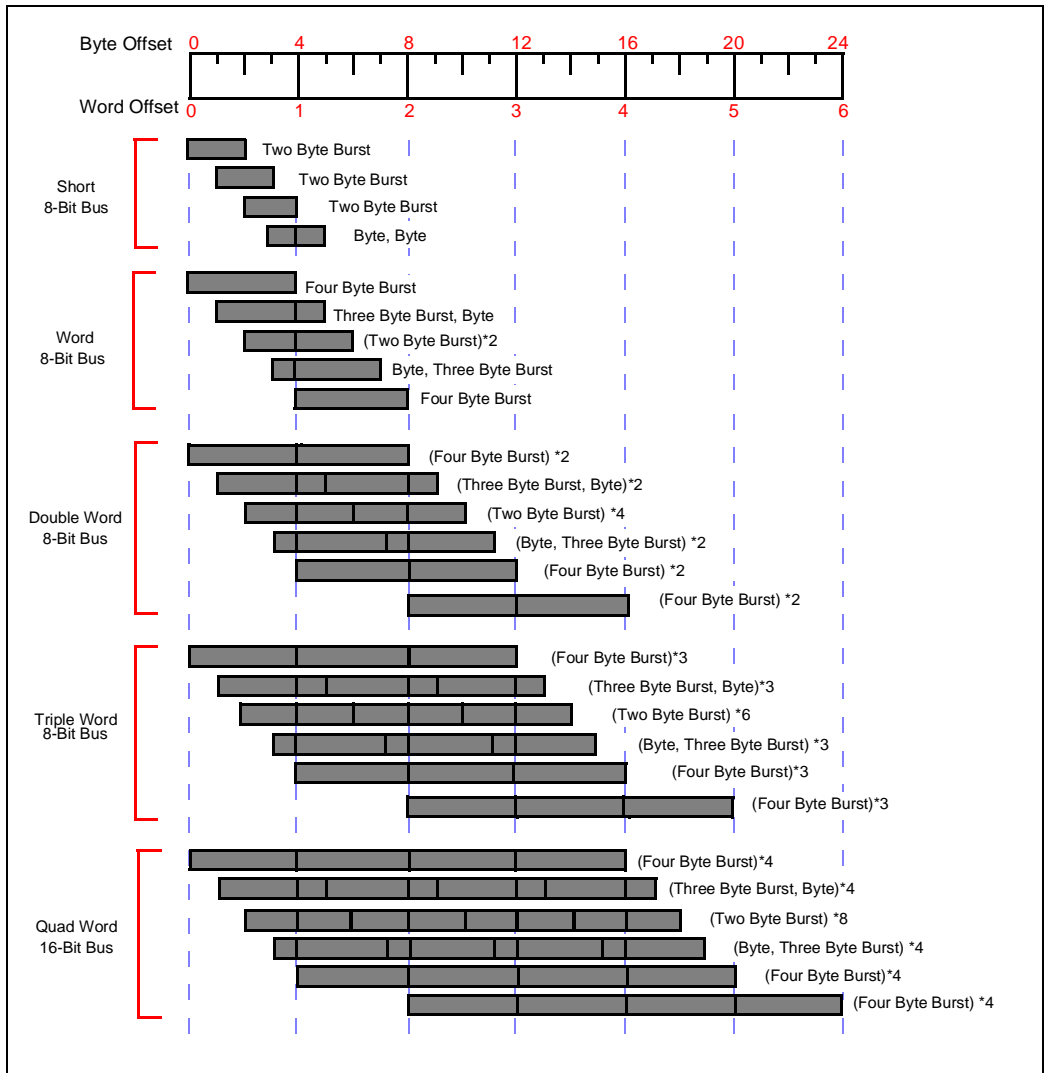
Figure 56. A Summary of Aligned and Unaligned Transfers for 8-Bit Bus

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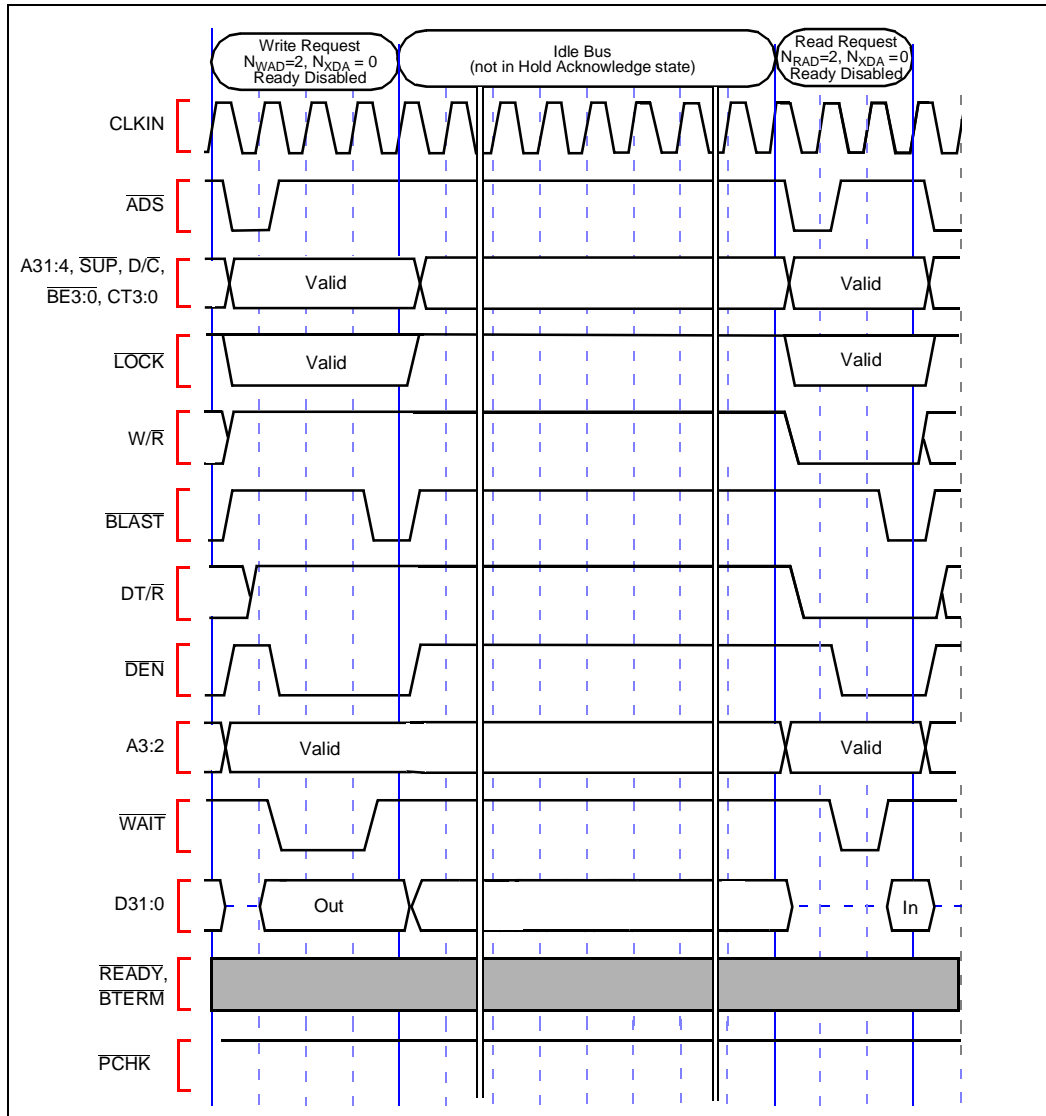
Figure 57. Idle Bus Operation

ADVANCE INFORMATION

Tb

BOFF

$\overline{BOFF}$

$\overline{BOFF}$

!BOFF

$\overline{BOFF}$

Ta

!BOFF and $\overline{READY}$ and !BLAST or
$\overline{BOFF}$ and $\overline{BTERM}$ and !BLAST or !BOFF and
!HOLD and $\overline{BLAST}$ and REQUEST and N_{XDA} = 0

!$\overline{BOFF}$ and READ and N_{rad} = 0 or
!$\overline{BOFF}$ and WRITE and N_{wad} = 0

READ and N_{rad} > 0 or
WRITE and N_{wad} > 0

!RESET and
!HOLD and
REQUEST

Tdw^3

W_dCNT > 1

W_dCNT = 1

READ and N_{rdd} > 0 or
WRITE and N_{wdd} > 0

Td^1

!$\overline{BOFF}$ and READ and N_{rdd} = 0
and !$\overline{BLAST}$ or !$\overline{BOFF}$ and
WRITE and N_{wdd} = 0 and !BLAST or
READY!

Taw^2

W_aCNT = 1

W_aCNT > 1

$\overline{!BOFF}$ and
$\overline{BLAST}$ and
N_{xda} > 0

Trw^4

W_xCNT > 1

!HOLD and W_xCNT=1
and REQUEST

!BOFF and
HOLD and BLAST
and N_{xda}= 0

!$\overline{BOFF}$ and !HOLD and
$\overline{BLAST}$ and N_{xda} = 0
and !REQUEST

To

$\overline{RESET}$ and
!$\overline{ONCE}$

$\overline{ONCE}$ and
$\overline{RESET}$

Ti

!HOLD and W_xCNT=1
and !REQUEST

W_xCNT=1 and
HOLD

HOLD

HOLD

Th

HOLD

!HOLD

$\overline{RESET}$

KEY:
To = ONCE
Ti = IDLE
Th = HOLD
Ta = ADDRESS
Td = DATA
Tb = BOFF'ed
Taw= address to data wait
Tdw= data to data wait
Tdw= data to address wait
REQUEST= One or more
requests in the bus queue.
READ= The current
access is a read.
WRITE= The current
access is a write.

NOTE:

1. When the PMCON for the region has External Ready Control enabled, wait states are inserted as long as $\overline{READY}$ and $\overline{BTERM}$ are de-asserted. When Read Pipelining is enabled, the Ta state of the subsequent read access is concurrent with the last data cycle of the access. Because External Ready Control is disabled for Read Pipelining, the address cycle occurs during $\overline{BLAST}$.
2. W_aCNT is decremented during T_{aw}
3. W_dCNT is decremented during T_{dw}
4. W_xCNT is decremented during T_{rw}

Figure 58. Bus States

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5.1   80960Hx Boundary Scan Chain

Table 24. 80960Hx Boundary Scan Chain (Sheet 1 of 4)

#	BOUNDARY SCAN CELL	CELL TYPE	COMMENT
1	DP3	Bidirectional	
2	DP2	Bidirectional	
3	DP0	Bidirectional	
4	DP1	Bidirectional	
5	STEST	Input	
6	FAILBAR	Output	
7	Enable for FAILBAR, BSTALL and BREQ	Control	
8	ONCEBAR	Input	
9	BOFFBAR	Input	
10	D0	Bidirectional	
11	D1	Bidirectional	
12	D2	Bidirectional	
13	D3	Bidirectional	
14	D4	Bidirectional	
15	D5	Bidirectional	
16	D6	Bidirectional	
17	D7	Bidirectional	
18	Enable for DP(3:0) and D(31:0)	Control	
19	D8	Bidirectional	
20	D9	Bidirectional	
21	D10	Bidirectional	
22	D11	Bidirectional	
23	D12	Bidirectional	
24	D13	Bidirectional	
25	D14	Bidirectional	
26	D15	Bidirectional	
27	D16	Bidirectional	
28	D17	Bidirectional	

NOTE:

1. Cell#1 connects to TDO and cell #112 connects to TDI.

2. All outputs are three-state.

3. In output and bidirectional signals, a logical "1" on the enable signal enables the output. A logical "0" three-states the output.

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Table 24. 80960Hx Boundary Scan Chain (Sheet 2 of 4)

#	BOUNDARY SCAN CELL	CELL TYPE	COMMENT
29	D18	Bidirectional	
30	D19	Bidirectional	
31	D20	Bidirectional	
32	D21	Bidirectional	
33	D22	Bidirectional	
34	D23	Bidirectional	
35	D24	Bidirectional	
36	D25	Bidirectional	
37	D26	Bidirectional	
38	D27	Bidirectional	
39	D28	Bidirectional	
40	D29	Bidirectional	
41	D30	Bidirectional	
42	D31	Bidirectional	
43	BTERMBAR	Input	
44	RDYBAR	Input	Appears as READYBAR in BSDL file.
45	HOLD	Input	
46	HOLDA	Output	
47	Enable for HOLDA control	Control	
48	ADSBAR	Output	
49	BE3BAR	Output	Appears as BEBAR(3:0) in BSDL file.
50	BE2BAR	Output	
51	BE1BAR	Output	
52	BE0BAR	Output	
53	BLASTBAR	Output	
54	DENBAR	Output	
55	WRRDBAR	Output	Appears as WRBAR in BSDL file.
56	DTRBAR	Output	
57	Enable for DTRBAR	Control	

NOTE:

1. Cell#1 connects to TDO and cell #112 connects to TDI.

2. All outputs are three-state.

3. In output and bidirectional signals, a logical "1" on the enable signal enables the output. A logical "0" three-states the output.

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Table 24. 80960Hx Boundary Scan Chain (Sheet 3 of 4)

#	BOUNDARY SCAN CELL	CELL TYPE	COMMENT
58	WAITBAR	Output	
59	BSTALL	Output	
60	DATACODBAR	Output	Appears as DCBAR in BSDL file.
61	USERSUPBAR	Output	Appears as SUPBAR in BSDL file.
62	Enable for ADSBAR, BEBAR, BLASTBAR, DENBAR, WRRDBAR, WAITBAR, DCBAR, SUPBAR and LOCKBAR,	Control	
63	LOCKBAR	Output	
64	BREQ	Output	
65	A31	Output	
66	A30	Output	
67	A29	Output	
68	A28	Output	
69	A27	Output	
70	A26	Output	
71	A25	Output	
72	A24	Output	
73	A23	Output	
74	A22	Output	
75	A21	Output	
76	A20	Output	
77	A19	Output	
78	A18	Output	
79	A17	Output	
80	A16	Output	
81	Enable for A(31:0) and CT(3:0)	Control	
82	A15	Output	
83	A14	Output	
84	A13	Output	
85	A12	Output	

NOTE:

1. Cell#1 connects to TDO and cell #112 connects to TDI.

2. All outputs are three-state.

3. In output and bidirectional signals, a logical "1" on the enable signal enables the output. A logical "0" three-states the output.

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Table 24. 80960Hx Boundary Scan Chain (Sheet 4 of 4)

#	BOUNDARY SCAN CELL	CELL TYPE	COMMENT
86	A11	Output	
87	A10	Output	
88	A9	Output	
89	A8	Output	
90	A7	Output	
91	A6	Output	
92	A5	Output	
93	A4	Output	
94	A3	Output	
95	A2	Output	
96	NMIBAR	Input	
97	XINT7BAR	Input	Appears as XINTBAR(7:0) in BSDL file.
98	XINT6BAR	Input	
99	XINT5BAR	Input	
100	XINT4BAR	Input	
101	XINT3BAR	Input	
102	XINT2BAR	Input	
103	XINT1BAR	Input	
104	XINT0BAR	Input	
105	RESETBAR	Input	
106	CLKIN	Input	
107	CT3	Output	Appears as CT(3:0) in BSDL file.
108	CT2	Output	
109	CT1	Output	
110	CT0	Output	
111	PCHK	Output	Appears as PCHKBAR in BSDL file.
112	PCHK enable	Control	

NOTE:

1. Cell#1 connects to TDO and cell #112 connects to TDI.

2. All outputs are three-state.

3. In output and bidirectional signals, a logical "1" on the enable signal enables the output. A logical "0" three-states the output.

ADVANCE INFORMATION

5.2   Boundary Scan Description Language Example

Boundary-Scan Description Language (BSDL) Example 5-2 meets the de facto standard means of describing essential features of ANSI/IEEE 1149.1-1993 compliant devices.

Example 5-1. Boundary-Scan Description Language (BSDL) for PGA Package Example (Sheet 1 of 9)

```
--Copyright Intel Corp. 1995
--*********************************************************************************************************************

--Intel Corporation makes no warranty for the use of its products and assumes no responsibility for any
errors which may appear in this document nor does it make a commitment to update the information
contained herein.

--*********************************************************************************************************************

--Boundary-Scan Description Language (BSDL Version 0.0) is a de-facto standard means of describing
essential features of ANSI/IEEE 1149.1-1990 compliant devices. This language is under consideration by
the IEEE for formal inclusion within a supplement to the 1149.1-1990 standard. The generation of the
supplement entails an extensive IEEE review and a formal acceptance balloting procedure which may
change the resultant form of the language. Be aware that this process may extend well into 1993, and at this
time the IEEE does not endorse or hold an opinion on the language.
*********************************************************************************************************************

--

-- i960(R) Processor BSDL Model
```

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Example 5-1. Boundary-Scan Description Language (BSDL) for PGA Package Example (Sheet 2 of 9)

```
-- Project code HA
-- File **NOT** verified electrically
-- --------------------------------------------------------
-- Rev. 0.8    26 Jun  1997  Updated for B-2 stepping
-- Rev 0.7    18 Dec  1995  Updated for A-1 stepping.
-- Rev 0.6    08 Dec  1994
-- Rev 0.5    21 Nov  1994
-- Rev 0.4    31 Oct  1994
-- Rev 0.3    26 July 1994
-- Rev 0.2    22 June 1994
-- Rev 0.1    16 Mar  1994
-- Rev 0.0    30 Aug  1993
entity Ha_Processor is
  generic(PHYSICAL_PIN_MAP : string:= "PGA");

  port (A      : out    bit_vector(2 to 31);
        ADSBAR   : out    bit;
        BEBAR    : out    bit_vector(0 to 3);
        BLASTBAR  : out    bit;
        BOFFBAR   : in     bit;
        BREQ     : out    bit;
        BSTALL   : out    bit;
        BTERMBAR  : in     bit;
        CT       : out    bit_vector(0 to 3);
        CLKIN    : in     bit;
        D        : inout  bit_vector(0 to 31);
        DENBAR   : out    bit;
        DP       : inout  bit_vector(0 to 3);
        DTRBAR   : out    bit;
        DCBAR    : out    bit;
        FAILBAR  : out    bit;
        HOLD     : in     bit;
        HOLDA    : out    bit;
        LOCKBAR  : out    bit;
        NMIBAR   : in     bit;
        ONCEBAR  : in     bit;
        PCHKBAR  : out    bit;
        READYBAR : in     bit;
        RESETBAR : in     bit;
        STEST    : in     bit;
```

ADVANCE INFORMATION

```
        SUPBAR   : out    bit;
        TCK      : in     bit;
        TDI      : in     bit;
        TDO      : out    bit;
        TMS      : in     bit;
        TRST     : in     bit;
        WAITBAR  : out    bit;
        WRBAR    : out    bit;
        XINTBAR  : in     bit_vector(0 to 7);
        FIVEVREF : linkage bit;
        VCCPLL   : linkage bit;
        VOLTDET  : out    bit;
        VCC1     : linkage bit_vector(0 to 23);
        VCC2     : linkage bit_vector(0 to 20);
        VSS1     : linkage bit_vector(0 to 25);
        VSS2     : linkage bit_vector(0 to 22);
        NC       : linkage bit_vector(0 to 4)

    );

    use STD_1149_1_1990.all;
    use i960ha_a.all;


    attribute PIN_MAP of Ha_Processor : entity is PHYSICAL_PIN_MAP;
     constant PGA:PIN_MAP_STRING :=
        "A        : (D16, D17, E16, E17, F17, G16, G17, H17, J17, K17,"&
        "           L17, L16, M17, N17, N16, P17, Q17, P16, P15, Q16,"&
        "           R17, R16, Q15, S17, R15, S16, Q14, R14, Q13, S15),"&
        "ADSBAR   : R06,"&
        "BEBAR    : (R09, S07, S06, S05),"&
        "BLASTBAR : S08,"&
        "BOFFBAR  : B01,"&
        "BREQ     : R13,"&
        "BSTALL   : R12,"&
        "BTERMBAR : R04,"&
        "CT       : (A11, A12, A13, A14),"&
        "CLKIN    : C13,"&
```

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Example 5-1. Boundary-Scan Description Language (BSDL) for PGA Package Example (Sheet 4 of 9)

```
"D      : (E03, C02, D02, C01, E02, D01, F02, E01, F01, G01,"&
"        H02, H01, J01, K01, L02, L01, M01, N01, N02, P01,"&
"        P02, Q01, P03, Q02, R01, S01, Q03, R02, Q04, S02,"&
"        Q05, R03),"&
"DENBAR   : S09,"&
"DP      : (A03, B03, A04, B04),"&
"DTRBAR   : S11,"&
"DCBAR    : S13,"&
"FAILBAR  : A02,"&
"HOLD     : R05,"&
"HOLDA    : S04,"&
"LOCKBAR  : S14,"&
"NMIBAR   : D15,"&
"ONCEBAR  : C03,"&
"PCHKBAR  : B08,"&
"READYBAR : S03,"&
"RESETBAR : A16,"&
"STEST    : B02,"&
"SUPBAR   : Q12,"&
"TCK      : B05,"&
"TDI      : A07,"&
"TDO      : A08,"&
"TMS      : B06,"&
"TRST     : A06,"&
"WAITBAR  : S12,"&
"WRBAR    : S10,"&
"XINTBAR  : (B15, A15, A17, B16, C15, B17, C16, C17),"&
"FIVEVREF : C05,"&
"VOLTDET  : A05,"&
"VCCPLL   : B10,"&
"VCC1     : (M02, K02, J02, G02, N03, F03, C06, B07, B09, B11,"&
"          B12, C14, E15, F16, H16, J16, K16, M16, N15, Q06,"&
"          R07, R08, R10, R11),"&
"VSS1     : (G03, H03, J03, K03, L03, M03, C07, C08, C09, C10,"&
"          C11, C12, Q07, Q08, Q09, Q10, Q11, F15, G15, H15,"&
"          J15, K15, L15, M15, A01, C04),"&
"NC       : (A09, A10, B13, B14, D03)";
```

ADVANCE INFORMATION   81

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Example 5-1. Boundary-Scan Description Language (BSDL) for PGA Package Example (Sheet 5 of 9)

```
attribute Tap_Scan_In    of  TDI   : signal is true;
attribute Tap_Scan_Mode  of  TMS   : signal is true;
attribute Tap_Scan_Out   of  TDO   : signal is true;
attribute Tap_Scan_Reset of  TRST  : signal is true;
attribute Tap_Scan_Clock of  TCK   : signal is (66.0e6, BOTH);


attribute Instruction_Length of Ha_Processor: entity is 4;


attribute Instruction_Opcode of Ha_Processor: entity is


  "BYPASS    (1111)," &
  "EXTEST    (0000)," &
  "SAMPLE    (0001)," &
  "IDCODE    (0010)," &
  "RUBIST    (0111)," &
  "CLAMP     (0100)," &
  "HIGHZ     (1000)," &
  "Reserved  (1011, 1100)";


attribute Instruction_Capture of Ha_Processor: entity is "0001";


attribute Instruction_Private of Ha_Processor: entity is "Reserved" ;


attribute Idcode_Register of Ha_Processor: entity is
  "0010"               & --version,
  "1000100001000000"    & --part number
  "00000001001"         & --manufacturers identity
  "1";                  --required by the standard
attribute Register_Access of Ha_Processor: entity is
  "Runbist[32]    (RUBIST)," &
  "Bypass         (CLAMP, HIGHZ)";


{************************************************************************}
{  The first cell, cell 0, is closest to TDO                }
{ BC_1:Control, Output3  CBSC_1:Bidir  BC_4: Input, Clock        }
{************************************************************************}
```

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Example 5-1. Boundary-Scan Description Language (BSDL) for PGA Package Example (Sheet 6 of 9)

```
attribute Boundary_Cells of Ha_Processor: entity is "BC_4, BC_1, CBSC_1";
attribute Boundary_Length of Ha_Processor: entity is 112;
attribute Boundary_Register of Ha_Processor: entity is

 "0 (CBSC_1, DP(3),     bidir, X, 17, 1, Z)," &
 "1 (CBSC_1, DP(2),     bidir, X, 17, 1, Z)," &
 "2 (CBSC_1, DP(0),     bidir, X, 17, 1, Z)," &
 "3 (CBSC_1, DP(1),     bidir, X, 17, 1, Z)," &
 "4 (BC_4,   STEST,     input, X)," &
 "5 (BC_1,   FAILBAR,   output3, X,  6,  1, Z)," &
 "6 (BC_1,   *,         control, 1)," &
 "7 (BC_4,   ONCEBAR,   input, X)," &
 "8 (BC_4,   BOFFBAR,   input, X)," &
 "9 (CBSC_1, D(0),      bidir, X, 17, 1, Z)," &
 "10 (CBSC_1, D(1),     bidir, X, 17, 1, Z)," &
 "11 (CBSC_1, D(2),     bidir, X, 17, 1, Z)," &
 "12 (CBSC_1, D(3),     bidir, X, 17, 1, Z)," &
 "13 (CBSC_1, D(4),     bidir, X, 17, 1, Z)," &
 "14 (CBSC_1, D(5),     bidir, X, 17, 1, Z)," &
 "15 (CBSC_1, D(6),     bidir, X, 17, 1, Z)," &
 "16 (CBSC_1, D(7),     bidir, X, 17, 1, Z)," &
 "17 (BC_1,   *,        control, 1)," &
 "18 (CBSC_1, D(8),     bidir, X, 17, 1, Z)," &
 "19 (CBSC_1, D(9),     bidir, X, 17, 1, Z)," &
 "20 (CBSC_1, D(10),    bidir, X, 17, 1, Z)," &
 "21 (CBSC_1, D(11),    bidir, X, 17, 1, Z)," &
 "22 (CBSC_1, D(12),    bidir, X, 17, 1, Z)," &
 "23 (CBSC_1, D(13),    bidir, X, 17, 1, Z)," &
 "24 (CBSC_1, D(14),    bidir, X, 17, 1, Z)," &
 "25 (CBSC_1, D(15),    bidir, X, 17, 1, Z)," &
 "26 (CBSC_1, D(16),    bidir, X, 17, 1, Z)," &
 "27 (CBSC_1, D(17),    bidir, X, 17, 1, Z)," &
 "28 (CBSC_1, D(18),    bidir, X, 17, 1, Z)," &
 "29 (CBSC_1, D(19),    bidir, X, 17, 1, Z)," &
 "30 (CBSC_1, D(20),    bidir, X, 17, 1, Z)," &
 "31 (CBSC_1, D(21),    bidir, X, 17, 1, Z)," &
 "32 (CBSC_1, D(22),    bidir, X, 17, 1, Z)," &
 "33 (CBSC_1, D(23),    bidir, X, 17, 1, Z)," &
```

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Example 5-1. Boundary-Scan Description Language (BSDL) for PGA Package Example (Sheet 7 of 9)

```
"34 (CBSC_1, D(24),      bidir,  X,  17, 1,  Z),"  &
"35 (CBSC_1, D(25),      bidir,  X,  17, 1,  Z),"  &
"36 (CBSC_1, D(26),      bidir,  X,  17, 1,  Z),"  &
"37 (CBSC_1, D(27),      bidir,  X,  17, 1,  Z),"  &
"38 (CBSC_1, D(28),      bidir,  X,  17, 1,  Z),"  &
"39 (CBSC_1, D(29),      bidir,  X,  17, 1,  Z),"  &
"40 (CBSC_1, D(30),      bidir,  X,  17, 1,  Z),"  &
"41 (CBSC_1, D(31),      bidir,  X,  17, 1,  Z),"  &
"42 (BC_4,   BTERMBAR,   input,  X),"  &
"43 (BC_4,   READYBAR,   input,  X),"  &
"44 (BC_4,   HOLD,       input,  X),"  &
"45 (BC_1,   HOLDA,      output3, X,  46, 1,  Z),"  &
"46 (BC_1,   *,          control, 1),"  &
"47 (BC_1,   ADSBAR,     output3, X,  61, 1,  Z),"  &
"48 (BC_1,   BEBAR(3),   output3, X,  61, 1,  Z),"  &
"49 (BC_1,   BEBAR(2),   output3, X,  61, 1,  Z),"  &
"50 (BC_1,   BEBAR(1),   output3, X,  61, 1,  Z),"  &
"51 (BC_1,   BEBAR(0),   output3, X,  61, 1,  Z),"  &
"52 (BC_1,   BLASTBAR,   output3, X,  61, 1,  Z),"  &
"53 (BC_1,   DENBAR,     output3, X,  61, 1,  Z),"  &
"54 (BC_1,   WRBAR,      output3, X,  61, 1,  Z),"  &
"55 (BC_1,   DTRBAR,     output3, X,  56, 1,  Z),"  &
"56 (BC_1,   *,          control, 1),"  &
"57 (BC_1,   WAITBAR,    output3, X,  61, 1,  Z),"  &
"58 (BC_1,   BSTALL,     output3, X,  6,  1,  Z),"  &
"59 (BC_1,   DCBAR,      output3, X,  61, 1,  Z),"  &
"60 (BC_1,   SUPBAR,     output3, X,  61, 1,  Z),"  &
"61 (BC_1,   *,          control, 1),"  &
"62 (BC_1,   LOCKBAR,    output3, X,  61, 1,  Z),"  &
"63 (BC_1,   BREQ,       output3, X,  6,  1,  Z),"  &
"64 (BC_1,   A(31),      output3, X,  80, 1,  Z),"  &
"65 (BC_1,   A(30),      output3, X,  80, 1,  Z),"  &
"66 (BC_1,   A(29),      output3, X,  80, 1,  Z),"  &
"67 (BC_1,   A(28),      output3, X,  80, 1,  Z),"  &
"68 (BC_1,   A(27),      output3, X,  80, 1,  Z),"  &
"69 (BC_1,   A(26),      output3, X,  80, 1,  Z),"  &
"70 (BC_1,   A(25),      output3, X,  80, 1,  Z),"  &
"71 (BC_1,   A(24),      output3, X,  80, 1,  Z),"  &
```

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Example 5-1. Boundary-Scan Description Language (BSDL) for PGA Package Example (Sheet 8 of 9)

```
"72 (BC_1, A(23),    output3, X, 80, 1, Z)," &
"73 (BC_1, A(22),    output3, X, 80, 1, Z)," &
"74 (BC_1, A(21),    output3, X, 80, 1, Z)," &
"75 (BC_1, A(20),    output3, X, 80, 1, Z)," &
"76 (BC_1, A(19),    output3, X, 80, 1, Z)," &
"77 (BC_1, A(18),    output3, X, 80, 1, Z)," &
"78 (BC_1, A(17),    output3, X, 80, 1, Z)," &
"79 (BC_1, A(16),    output3, X, 80, 1, Z)," &
"80 (BC_1, *,        control, 1)," &
"81 (BC_1, A(15),    output3, X, 80, 1, Z)," &
"82 (BC_1, A(14),    output3, X, 80, 1, Z)," &
"83 (BC_1, A(13),    output3, X, 80, 1, Z)," &
"84 (BC_1, A(12),    output3, X, 80, 1, Z)," &
"85 (BC_1, A(11),    output3, X, 80, 1, Z)," &
"86 (BC_1, A(10),    output3, X, 80, 1, Z)," &
"87 (BC_1, A(9),     output3, X, 80, 1, Z)," &
"88 (BC_1, A(8),     output3, X, 80, 1, Z)," &
"89 (BC_1, A(7),     output3, X, 80, 1, Z)," &
"90 (BC_1, A(6),     output3, X, 80, 1, Z)," &
"91 (BC_1, A(5),     output3, X, 80, 1, Z)," &
"92 (BC_1, A(4),     output3, X, 80, 1, Z)," &
"93 (BC_1, A(3),     output3, X, 80, 1, Z)," &
"94 (BC_1, A(2),     output3, X, 80, 1, Z)," &
"95 (BC_4, NMIBAR,     input,  X)," &
"96 (BC_4, XINTBAR(7), input,  X)," &
"97 (BC_4, XINTBAR(6), input,  X)," &
"98 (BC_4, XINTBAR(5), input,  X)," &
"99 (BC_4, XINTBAR(4), input,  X)," &
"100(BC_4, XINTBAR(3), input,  X)," &
"101(BC_4, XINTBAR(2), input,  X)," &
"102(BC_4, XINTBAR(1), input,  X)," &
"103(BC_4, XINTBAR(0), input,  X)," &
"104(BC_4, RESETBAR,  input,  X)," &
"105(BC_4, CLKIN,     input,  X)," &
"106(BC_1, CT(3),     output3, X, 80, 1, Z)," &
```

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Example 5-1. Boundary-Scan Description Language (BSDL) for PGA Package Example (Sheet 9 of 9)

```
    "107(BC_1, CT(2),      output3, X,  80, 1, Z)," &
    "108(BC_1, CT(1),      output3, X,  80, 1, Z)," &
    "109(BC_1, CT(0),      output3, X,  80, 1, Z)," &
    "110(BC_1, PCHKBAR,    output3, X, 111, 1, Z)," &
    "111(BC_1, *,          control, 1)";
end Ha_Processor;
```

Example 5-2. Boundary-Scan Description Language (BSDL) for PQ4 Package Example (Sheet 1 of 8)

```
-- Copyright Intel Corporation 1995, 1996
--*************************************************************************************************************************
--Intel Corporation makes no warranty for the use of its products and assumes no responsibility for any
errors which may appear in this document nor does it make a commitment to update the information
contained herein.
--*************************************************************************************************************************
--Boundary-Scan Description Language (BSDL Version 0.0) is a de-facto
--standard means of describing essential features of ANSI/IEEE 1149.1-1990 compliant devices.  This
language is under consideration by the IEEE for formal inclusion within a supplement to the 1149.1-1990
standard.  The generation of the supplement entails an extensive IEEE review and a formal acceptance
balloting procedure which may change the resultant form of the language.  Be aware that this process may
extend well into 1993, and at this time the IEEE does not endorse or hold an opinion on the language.
-- i960(R) Processor BSDL Model
-- Project code HA
-- File **NOT** verified electrically
-- ------------------------------------------------------------------------
-- Rev 0.9    26 Jun  1997  Updated for B-2 stepping
-- Rev 0.8     4 Apr  1996  Changed for PQ2 Package
-- Rev 0.7    18 Dec  1995  Updated for A-1 stepping.
-- Rev 0.6    08 Dec  1994
-- Rev 0.5    21 Nov  1994
-- Rev 0.4    31 Oct  1994
-- Rev 0.3    26 July 1994
-- Rev 0.2    22 June 1994
-- Rev 0.1    16 Mar  1994
-- Rev 0.0    30 Aug  1993
```

Example 5-2. Boundary-Scan Description Language (BSDL) for PQ4 Package Example (Sheet 2 of 8)

```
entity Ha_Processor is
  generic(PHYSICAL_PIN_MAP : string:= "PQ4");
  port (A        : out    bit_vector(2 to 31);
       ADSBAR    : out    bit;
       BEBAR     : out    bit_vector(0 to 3);
       BLASTBAR  : out    bit;
       BOFFBAR   : in     bit;
       BREQ      : out    bit;
       BSTALL    : out    bit;
       BTERMBAR  : in     bit;
       CT        : out    bit_vector(0 to 3);
       CLKIN     : in     bit;
       D         : inout  bit_vector(0 to 31);
       DENBAR    : out    bit;
       DP        : inout  bit_vector(0 to 3);
       DTRBAR    : out    bit;
       DCBAR     : out    bit;
       FAILBAR   : out    bit;
       HOLD      : in     bit;
       HOLDA     : out    bit;
       LOCKBAR   : out    bit;
       NMIBAR    : in     bit;
       ONCEBAR   : in     bit;
       PCHKBAR   : out    bit;
       READYBAR  : in     bit;
       RESETBAR  : in     bit;
       STEST     : in     bit;
       SUPBAR    : out    bit;
       TCK       : in     bit;
       TDI       : in     bit;
       TDO       : out    bit;
       TMS       : in     bit;
       TRST      : in     bit;
       WAITBAR   : out    bit;
       WRBAR     : out    bit;
       XINTBAR   : in     bit_vector(0 to 7);
       FIVEVREF  : linkage bit;
       VCCPLL    : linkage bit;
```

ADVANCE INFORMATION   87

Example 5-2. Boundary-Scan Description Language (BSDL) for PQ4 Package Example (Sheet 3 of 8)

```
    VCC1     : linkage bit_vector(0 to 23);
    VCC2     : linkage bit_vector(0 to 23);
    VSS1     : linkage bit_vector(0 to 23);
    VSS2     : linkage bit_vector(0 to 23)

);

use STD_1149_1_1990.all;
use i960ha_a.all;



attribute PIN_MAP of Ha_Processor : entity is PHYSICAL_PIN_MAP;
 constant PQ4:PIN_MAP_STRING :=

   "A        : (151, 150, 147, 146, 145, 144, 141, 140, 139, 138,"&
   "           135, 134, 133, 132, 127, 126, 125, 124, 121, 120,"&
   "           119, 118, 113, 112, 111, 110, 107, 106, 105, 104),"&
   "ADSBAR   : 77,"&
   "BEBAR    : (83, 82, 79, 78),"&
   "BLASTBAR  : 84,"&
   "BOFFBAR  : 10,"&
   "BREQ     : 100,"&
   "BSTALL   : 91,"&
   "BTERMBAR  : 67,"&
   "CT       : (183, 182, 181, 180),"&
   "CLKIN    : 175,"&
   "D        : (12, 13, 14, 15, 20, 21, 22, 23, 26, 27, 28, 29,"&
   "            34, 35, 36, 37, 39, 40, 41, 42, 45, 50, 51, 52,"&
   "            54, 55, 56, 57, 61, 62, 63, 64),"&
   "DENBAR   : 85,"&
   "DP       : (206, 207, 203, 202),"&
   "DTRBAR   : 89,"&
   "DCBAR    : 96,"&
   "FAILBAR  : 5,"&
   "HOLD     : 69,"&
   "HOLDA    : 72,"&
   "LOCKBAR  : 99,"&
   "NMIBAR   : 159,"&
```

ADVANCE INFORMATION

Example 5-2. Boundary-Scan Description Language (BSDL) for PQ4 Package Example (Sheet 4 of 8)

```
      "ONCEBAR   : 6,"&
      "PCHKBAR   : 189,"&
      "READYBAR  : 68,"&
      "RESETBAR  : 174,"&
      "STEST     : 208,"&
      "SUPBAR    : 97,"&
      "TCK       : 194,"&
      "TDI       : 191,"&
      "TDO       : 188,"&
      "TMS       : 192,"&
      "TRST      : 193,"&
      "WAITBAR   : 90,"&
      "WRBAR     : 88,"&
      "XINTBAR   : (169, 168, 167, 166, 163, 162, 161, 160),"&
      "FIVEVREF  : 197,"&
      "VCCPLL    : 177,"&
      "VCC1      : (1, 4, 9, 11, 17, 19, 25, 31, 33, 38, 44, 46,"&
      "               49, 59, 60, 66, 71, 74, 76, 81, 87, 92, 95, 101),"&
      "VCC2      : (102, 109, 115, 117, 123, 128, 131, 137, 143, 149,"&
      "               153, 154, 158, 165, 171, 173, 176, 179, 185, 187,"&
      "               196, 199, 201, 204),"&
      "VSS1      : (2, 3, 7, 8, 16, 18, 24, 30, 32, 43, 47, 48,"&
      "               53, 58, 65, 70, 73, 75, 80, 86, 93, 94, 98, 103),"&
      "VSS2      : (108, 114, 116, 122, 129, 130, 136, 142, 148, 152,"&
      "               155, 156, 157, 164, 170, 172, 178, 184, 186, 190,"&
      "               195, 198, 200, 205)";


attribute Tap_Scan_In    of  TDI  : signal is true;
attribute Tap_Scan_Mode  of  TMS  : signal is true;
attribute Tap_Scan_Out   of  TDO  : signal is true;
attribute Tap_Scan_Reset of  TRST : signal is true;
attribute Tap_Scan_Clock of  TCK  : signal is (66.0e6, BOTH);


attribute Instruction_Length of Ha_Processor: entity is 4;


attribute Instruction_Opcode of Ha_Processor: entity is
```

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Example 5-2. Boundary-Scan Description Language (BSDL) for PQ4 Package Example (Sheet 5 of 8)

```
    "BYPASS     (1111)," &
    "EXTEST     (0000)," &
    "SAMPLE     (0001)," &
    "IDCODE     (0010)," &
    "RUBIST     (0111)," &
    "CLAMP      (0100)," &
    "HIGHZ      (1000)," &
    "Reserved   (1011, 1100)";

  attribute Instruction_Capture of Ha_Processor: entity is "0001";

  attribute Instruction_Private of Ha_Processor: entity is "Reserved" ;

  attribute Idcode_Register of Ha_Processor: entity is
    "0010"                    & --version,
    "1000100001000000"        & --part number
    "00000001001"             & --manufacturers identity
    "1";                        --required by the standard

  attribute Register_Access of Ha_Processor: entity is
    "Runbist[32]    (RUBIST)," &
    "Bypass         (CLAMP, HIGHZ)";
********************************************************************************
{  The first cell, cell 0, is closest to TDO                }
{  BC_1:Control, Output3  CBSC_1:Bidir  BC_4: Input, Clock        }
********************************************************************************

  attribute Boundary_Cells of Ha_Processor: entity is "BC_4, BC_1, CBSC_1";
  attribute Boundary_Length of Ha_Processor: entity is 112;
  attribute Boundary_Register of Ha_Processor: entity is

    "0 (CBSC_1,  DP(3),      bidir,  X,   17, 1,  Z)," &
    "1 (CBSC_1,  DP(2),      bidir,  X,   17, 1,  Z)," &
    "2 (CBSC_1,  DP(0),      bidir,  X,   17, 1,  Z)," &
    "3 (CBSC_1,  DP(1),      bidir,  X,   17, 1,  Z)," &
    "4 (BC_4,    STEST,      input,  X)," &
    "5 (BC_1,    FAILBAR,     output3, X,  6, 1,  Z)," &
```

ADVANCE INFORMATION

Example 5-2. Boundary-Scan Description Language (BSDL) for PQ4 Package Example (Sheet 6 of 8)

```
"6  (BC_1,   *,        control, 1)," &
"7  (BC_4,   ONCEBAR,  input, X)," &
"8  (BC_4,   BOFFBAR,   input, X)," &
"9  (CBSC_1, D(0),     bidir, X, 17, 1, Z)," &
"10 (CBSC_1, D(1),     bidir, X, 17, 1, Z)," &
"11 (CBSC_1, D(2),     bidir, X, 17, 1, Z)," &
"12 (CBSC_1, D(3),     bidir, X, 17, 1, Z)," &
"13 (CBSC_1, D(4),     bidir, X, 17, 1, Z)," &
"14 (CBSC_1, D(5),     bidir, X, 17, 1, Z)," &
"15 (CBSC_1, D(6),     bidir, X, 17, 1, Z)," &
"16 (CBSC_1, D(7),     bidir, X, 17, 1, Z)," &
"17 (BC_1,   *,        control, 1)," &
"18 (CBSC_1, D(8),     bidir, X, 17, 1, Z)," &
"19 (CBSC_1, D(9),     bidir, X, 17, 1, Z)," &
"20 (CBSC_1, D(10),    bidir, X, 17, 1, Z)," &
"21 (CBSC_1, D(11),    bidir, X, 17, 1, Z)," &
"22 (CBSC_1, D(12),    bidir, X, 17, 1, Z)," &
"23 (CBSC_1, D(13),    bidir, X, 17, 1, Z)," &
"24 (CBSC_1, D(14),    bidir, X, 17, 1, Z)," &
"25 (CBSC_1, D(15),    bidir, X, 17, 1, Z)," &
"26 (CBSC_1, D(16),    bidir, X, 17, 1, Z)," &
"27 (CBSC_1, D(17),    bidir, X, 17, 1, Z)," &
"28 (CBSC_1, D(18),    bidir, X, 17, 1, Z)," &
"29 (CBSC_1, D(19),    bidir, X, 17, 1, Z)," &
"30 (CBSC_1, D(20),    bidir, X, 17, 1, Z)," &
"31 (CBSC_1, D(21),    bidir, X, 17, 1, Z)," &
"32 (CBSC_1, D(22),    bidir, X, 17, 1, Z)," &
"33 (CBSC_1, D(23),    bidir, X, 17, 1, Z)," &
"34 (CBSC_1, D(24),    bidir, X, 17, 1, Z)," &
"35 (CBSC_1, D(25),    bidir, X, 17, 1, Z)," &
"36 (CBSC_1, D(26),    bidir, X, 17, 1, Z)," &
"37 (CBSC_1, D(27),    bidir, X, 17, 1, Z)," &
"38 (CBSC_1, D(28),    bidir, X, 17, 1, Z)," &
"39 (CBSC_1, D(29),    bidir, X, 17, 1, Z)," &
"40 (CBSC_1, D(30),    bidir, X, 17, 1, Z)," &
```

Example 5-2. Boundary-Scan Description Language (BSDL) for PQ4 Package Example (Sheet 7 of 8)

```
"41 (CBSC_1, D(31),    bidir,  X, 17, 1, Z)," &
"42 (BC_4, BTERMBAR,  input,  X)," &
"43 (BC_4, READYBAR,  input,  X)," &
"44 (BC_4, HOLD,      input,  X)," &
"45 (BC_1, HOLDA,     output3, X, 46, 1, Z)," &
"46 (BC_1, *,         control, 1)," &
"47 (BC_1, ADSBAR,    output3, X, 61, 1, Z)," &
"48 (BC_1, BEBAR(3),  output3, X, 61, 1, Z)," &
"49 (BC_1, BEBAR(2),  output3, X, 61, 1, Z)," &
"50 (BC_1, BEBAR(1),  output3, X, 61, 1, Z)," &
"51 (BC_1, BEBAR(0),  output3, X, 61, 1, Z)," &
"52 (BC_1, BLASTBAR,  output3, X, 61, 1, Z)," &
"53 (BC_1, DENBAR,    output3, X, 61, 1, Z)," &
"54 (BC_1, WRBAR,     output3, X, 61, 1, Z)," &
"55 (BC_1, DTRBAR,    output3, X, 56, 1, Z)," &
"56 (BC_1, *,         control, 1)," &
"57 (BC_1, WAITBAR,   output3, X, 61, 1, Z)," &
"58 (BC_1, BSTALL,    output3, X, 6, 1, Z)," &
"59 (BC_1, DCBAR,     output3, X, 61, 1, Z)," &
"60 (BC_1, SUPBAR,    output3, X, 61, 1, Z)," &
"61 (BC_1, *,         control, 1)," &
"62 (BC_1, LOCKBAR,   output3, X, 61, 1, Z)," &
"63 (BC_1, BREQ,      output3, X, 6, 1, Z)," &
"64 (BC_1, A(31),     output3, X, 80, 1, Z)," &
"65 (BC_1, A(30),     output3, X, 80, 1, Z)," &
"66 (BC_1, A(29),     output3, X, 80, 1, Z)," &
"67 (BC_1, A(28),     output3, X, 80, 1, Z)," &
"68 (BC_1, A(27),     output3, X, 80, 1, Z)," &
"69 (BC_1, A(26),     output3, X, 80, 1, Z)," &
"70 (BC_1, A(25),     output3, X, 80, 1, Z)," &
"71 (BC_1, A(24),     output3, X, 80, 1, Z)," &
"72 (BC_1, A(23),     output3, X, 80, 1, Z)," &
"73 (BC_1, A(22),     output3, X, 80, 1, Z)," &
"74 (BC_1, A(21),     output3, X, 80, 1, Z)," &
"75 (BC_1, A(20),     output3, X, 80, 1, Z)," &
```

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Example 5-2. Boundary-Scan Description Language (BSDL) for PQ4 Package Example (Sheet 8 of 8)

```
"76 (BC_1, A(19),    output3, X, 80, 1, Z)," &
"77 (BC_1, A(18),    output3, X, 80, 1, Z)," &
"78 (BC_1, A(17),    output3, X, 80, 1, Z)," &
"79 (BC_1, A(16),    output3, X, 80, 1, Z)," &
"80 (BC_1, *,        control, 1)," &
"81 (BC_1, A(15),    output3, X, 80, 1, Z)," &
"82 (BC_1, A(14),    output3, X, 80, 1, Z)," &
"83 (BC_1, A(13),    output3, X, 80, 1, Z)," &
"84 (BC_1, A(12),    output3, X, 80, 1, Z)," &
"85 (BC_1, A(11),    output3, X, 80, 1, Z)," &
"86 (BC_1, A(10),    output3, X, 80, 1, Z)," &
"87 (BC_1, A(9),     output3, X, 80, 1, Z)," &
"88 (BC_1, A(8),     output3, X, 80, 1, Z)," &
"89 (BC_1, A(7),     output3, X, 80, 1, Z)," &
"90 (BC_1, A(6),     output3, X, 80, 1, Z)," &
"91 (BC_1, A(5),     output3, X, 80, 1, Z)," &
"92 (BC_1, A(4),     output3, X, 80, 1, Z)," &
"93 (BC_1, A(3),     output3, X, 80, 1, Z)," &
"94 (BC_1, A(2),     output3, X, 80, 1, Z)," &
"95 (BC_4, NMIBAR,    input, X)," &
"96 (BC_4, XINTBAR(7), input,  X)," &
"97 (BC_4, XINTBAR(6), input,  X)," &
"98 (BC_4, XINTBAR(5), input,  X)," &
"99 (BC_4, XINTBAR(4), input,  X)," &
"100(BC_4, XINTBAR(3), input,  X)," &
"101(BC_4, XINTBAR(2), input,  X)," &
"102(BC_4, XINTBAR(1), input,  X)," &
"103(BC_4, XINTBAR(0), input,  X)," &
"104(BC_4, RESETBAR,   input,  X)," &
"105(BC_4, CLKIN,      input,  X)," &
"106(BC_1, CT(3),     output3, X, 80, 1, Z)," &
"107(BC_1, CT(2),     output3, X, 80, 1, Z)," &
"108(BC_1, CT(1),     output3, X, 80, 1, Z)," &
"109(BC_1, CT(0),     output3, X, 80, 1, Z)," &
"110(BC_1, PCHKBAR,   output3, X, 111,1, Z)," &
"111(BC_1, *,        control, 1)";
end Ha_Processor;
```

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Table 25. Data Sheet Version -004 to -005 Revision History

Section	Description
Section 1	Added descriptive text to first sentence.
Section 1	Removed reference to future revisions providing electrical characteristics.
Section 1	Removed note
Table 1	Added 40/80 to 80960HD Operating Frequency
Table 6	Removed P(7) from CT3:0.
Section 3.2.2	Replaced PQ2 with PQ4 from this section throughout rest of data sheet.
Table 11	Revised all table values.
Table 13	Revised all table values.
Section 3.5	Added descriptive text to second sentence.
Table 17	Added B2 reference.
Section 3.7	Corrected 3M and Thermalloy phone numbers. Added Aavid information. Removed Augat reference.
Section 4.1	Update Notice text.
Table 18	Revised 2xcore "Maximum" value. Added PQ4 to T_C "Parameter".
Table 20	Revised I_{CC} (Power Supply, Thermal and Reset) "Typical" and "Maximum" values. Put overbar on R_{PU} "ONCE" parameter.
Table 21	Removed ".0" from single digit numbers. Revised T_F maximum value of 33.33 to 40. Revised T minimum value of 30 to 25.
Table 22	In #12: overbar to SUP and BE3:0.
Figure 15	Removed subscript "1" from footnote values T_{OV}, T_{OH}.
Figure 23	Revised all graph lines.
Figure 24	Revised all graph lines.
Example 5-1	Added Rev. 0.8 text. Changed "attribute Idcode_Register of Ha_Processor" (sheet 5 of 8) value to "0010".
Example 5-2	Added Rev. 0.9 text. Changed "attribute Idcode_Register of Ha_Processor" (sheet 5 of 8) value to "0010".
Table 25	Added version -005 revisions.

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