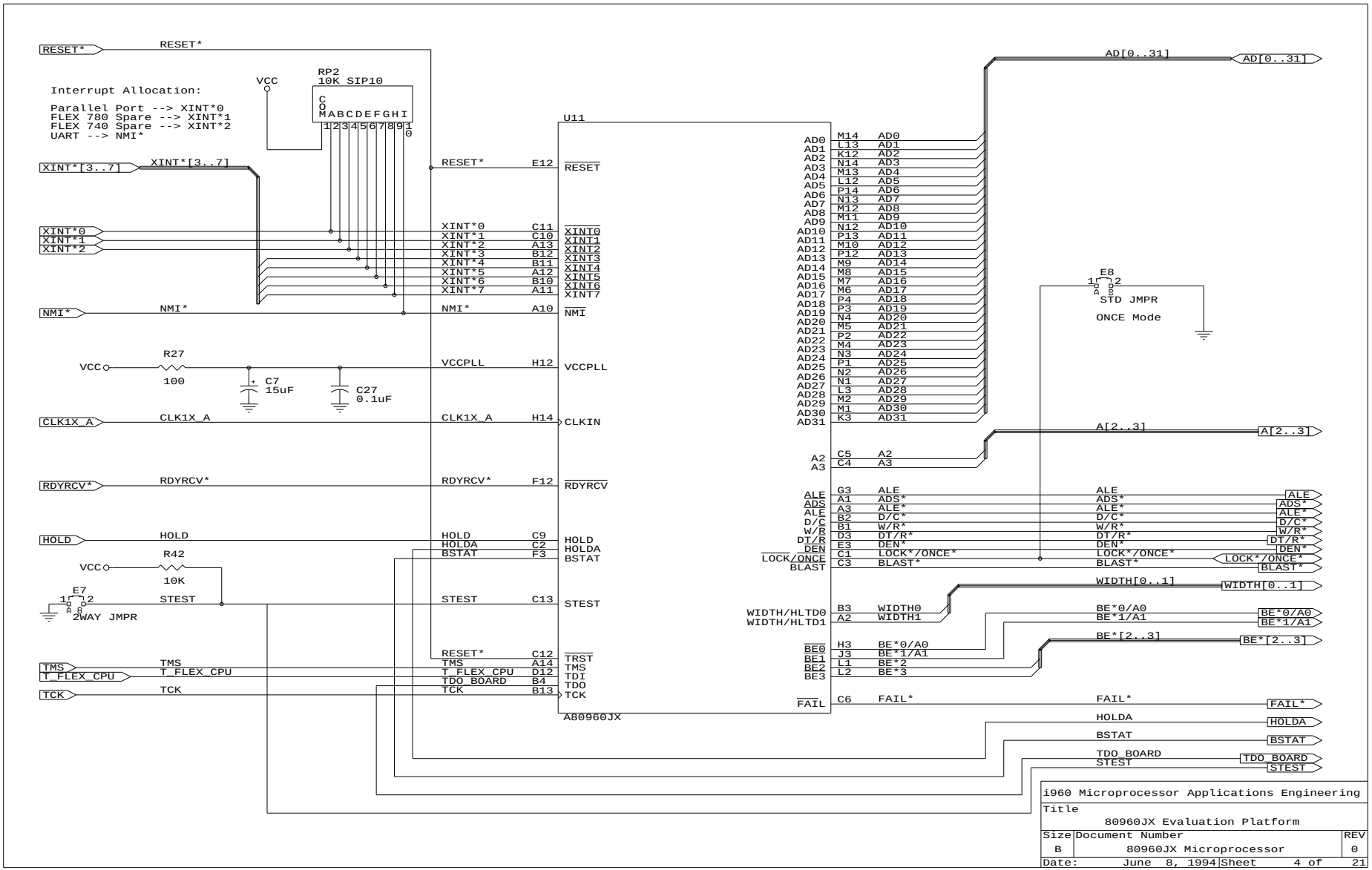
RESET*
Interrupt Allocation:
Parallel Port --> XINT*0
FLEX 780 Spare --> XINT*1
FLEX 740 Spare --> XINT*2
UART --> NMI*
VCC
RP2
10K SIP10
C
O
M A B C D E F G H I
1 2 3 4 5 6 7 8 9 10
XINT*[3..7]
XINT*0
XINT*1
XINT*2
NMI*
VCC
R27
100
C7
15uF
C27
0.1uF
CLK1X_A
RDYRCV*
HOLD
VCC
R42
10K
E7
2WAY JMPR
STEST
TMS
T_FLEX_CPU
TCK
U11
A80960JX
AD[0..31]
E8
STD JMPR
ONCE Mode
A[2..3]
ALE
ADS*
D/C*
W/R*
DT/R*
DEN*
LOCK*/ONCE*
BLAST*
WIDTH[0..1]
BE*0/A0
BE*1/A1
BE*[2..3]
FAIL*
HOLDA
BSTAT
TDO_BOARD
STEST
i960 Microprocessor Applications Engineering
Title
80960JX Evaluation Platform
Size B
Document Number
80960JX Microprocessor
REV 0
Date: June 8, 1994
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