Symbolic Scheduling

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***Abstract*—This paper focuses on the symbolic scheduling algorithm of an HLS (high-level synthesis) algorithm (1) for high-level test generation. For high-level synthesis applications, we know conflicts are bound to happen. To resolve decision conflicts during test generation, a high-level test generation algorithm called SWIFT is proposed, which incorporates a symbolic scheduling procedure derived from high-level synthesis applications. SWIFT generates functional tests based on the induced fault model to ensure the detection of low-level structural faults. SWIFT generates test sequences that cover all gate-level stuck-at faults when applied to functional models of representative 74Xseries, ISCAS-85, and ISCAS-89 circuits. Surprisingly, despite being derived from a high-level functional description of the circuit under test, the majority of these test sequences are provably minimal or near-minimal in size.**

***Index Terms*—high-level synthesis, symbolic scheduling, test generation**

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