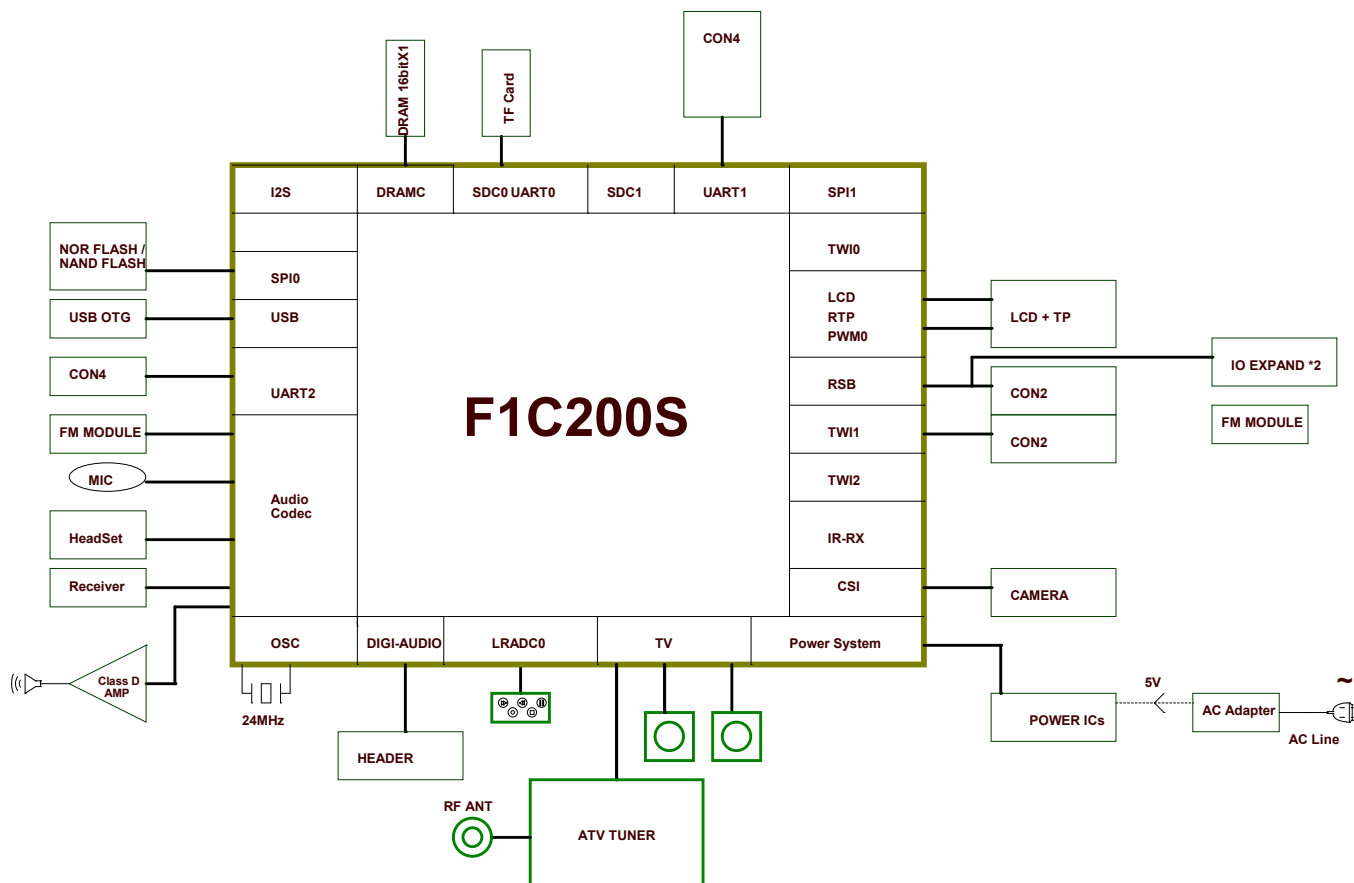


D

C

B

A



5

4

3

2

1



AllWinner Technology Co., Ltd

Design Name

AW_F1C200s_V10

Size

A3

Page Name

BLOCK DIAGRAM

Date

Friday, April 06, 2018

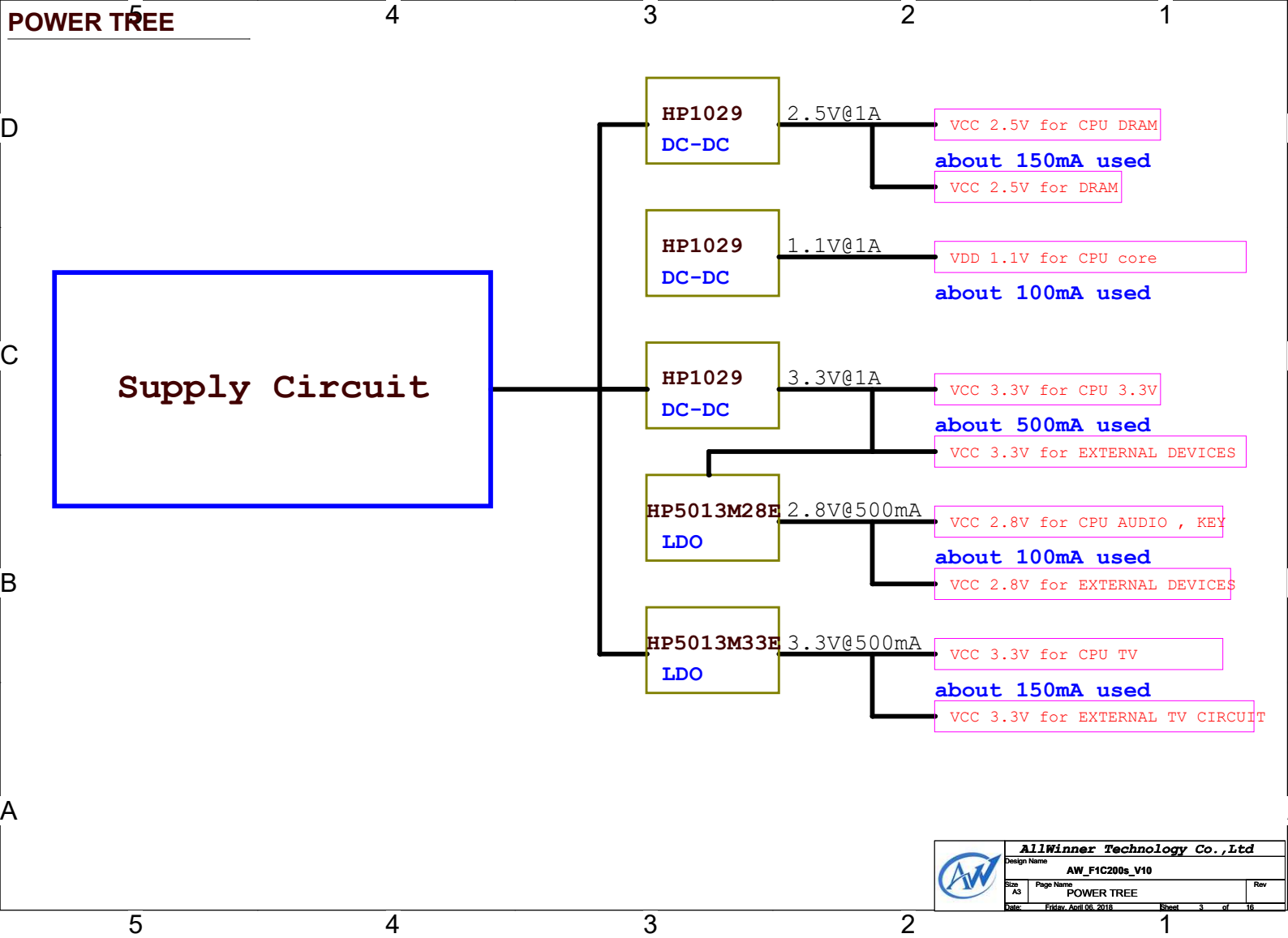
Sheet

2

of

16

Rev



D

C

B

A


5

4

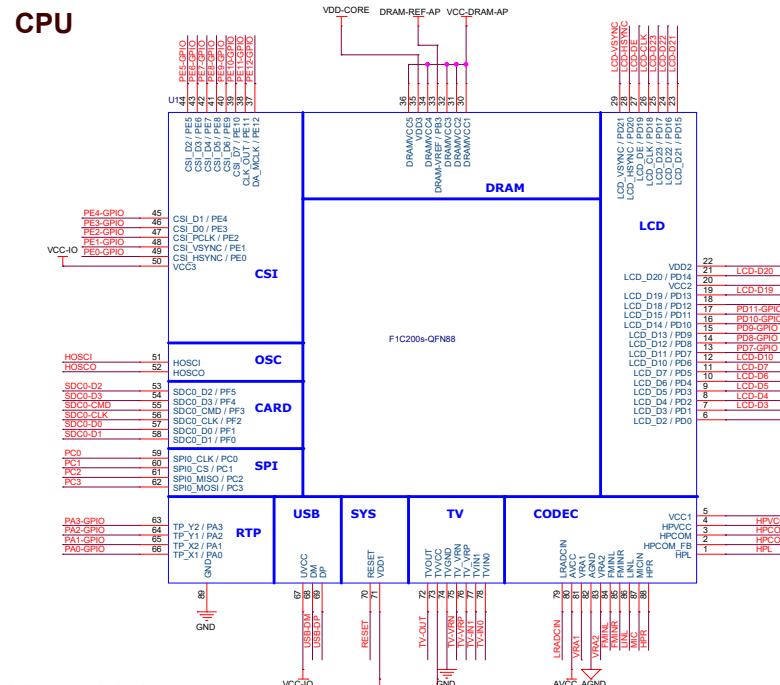
3

2

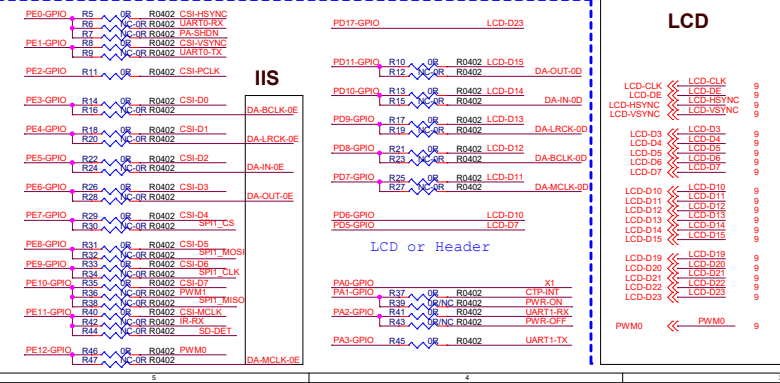
1

		Aliwinner Technology Co., Ltd	
		Design Name AW_F1C200s_V10	
Size	A3	Page Name	Rev
GPIO ASSIGNMENT			
Date: Friday, April 06, 2018		Sheet	4 of 18

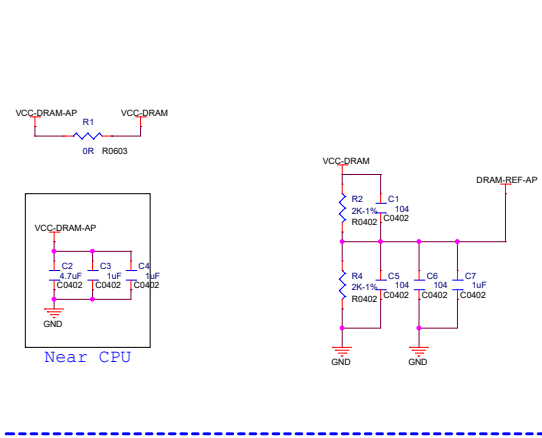
CPU



Pin multiplex




DDR1 2.5V



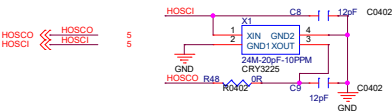
SYS HOSCO <-> HOSCO 6 HOSCI <-> HOSCI 6 RESET <-> RESET 6	CSI CSI-D0 <-> CSI-D0 12 CSI-D1 <-> CSI-D1 12 CSI-D2 <-> CSI-D2 12 CSI-D3 <-> CSI-D3 12 CSI-D4 <-> CSI-D4 12 CSI-D5 <-> CSI-D5 12 CSI-D6 <-> CSI-D6 12 CSI-D7 <-> CSI-D7 12 CSI-HSYNC <-> CSI-HSYNC 12 CSI-PSYNC <-> CSI-PSYNC 12 CSI-PCLK <-> CSI-PCLK 12 CSI-MCLK <-> CSI-MCLK 12	TV TV-OUT <-> TV-OUT 12,14 TV-VRN <-> TV-VRN 6 TV-VRP <-> TV-VRP 6 TV-IN1 <-> TV-IN1 12,14 TV-IND <-> TV-IND 12,14	IIC RSB-SCK <-> RSB-SCK 14 RSB-SDA <-> RSB-SDA 14
UART UART0-TX <-> UART0-TX 14 UART0-RX <-> UART0-RX 14 UART1-TX <-> UART1-TX 14 UART1-RX <-> UART1-RX 14	eMMC or SPI NOR SDC1-CLK <-> PC0 8 SDC1-CMD <-> PC1 8 SDC1-D0 <-> PC2 8 eMMC_RST <-> PC3 8	IIS DA-MCLK-0 <-> DA-MCLK-0 5,14 DA-BCLK-0 <-> DA-BCLK-0 5,14 DA-LRCK-0 <-> DA-LRCK-0 5,14 DA-OUT-0 <-> DA-OUT-0 5,14 DA-IN-0 <-> DA-IN-0 5,14 DA-MCLK-0E <-> DA-MCLK-0E 5,14 DA-BCLK-0E <-> DA-BCLK-0E 5,14 DA-LRCK-0E <-> DA-LRCK-0E 5,14 DA-OUT-0E <-> DA-OUT-0E 5,14 DA-IN-0E <-> DA-IN-0E 5,14	ADC LRADCIN <-> LRADCIN 6,13 X1 <-> X1 6,9
XR819MD or SD WL-WAKE-HOST <-> WL-WAKE-HOST 6 WL-RESTN <-> WL-RESTN 6 SDC0-CLK <-> SDC0-CLK 8 SDC0-D0 <-> SDC0-D0 8 SDC0-D1 <-> SDC0-D1 8 SDC0-D2 <-> SDC0-D2 8 SDC0-D3 <-> SDC0-D3 8 SDC0-DET <-> SDC0-DET 5	SD SP1_CS <-> SP1_CS 5 SP1_CLK <-> SP1_CLK 5 SP1_MOSI <-> SP1_MOSI 5 SP1_MISO <-> SP1_MISO 5 SD-DET <-> SD-DET 5	ADUIO LINL <-> LINL 10,12 VRA1 <-> VRA1 6 VRA2 <-> VRA2 6 HPVCC <-> HPVCC 6 HPL <-> HPL 10 HPR <-> HPR 10 HPCM <-> HPCM 10 HPCOM-FB <-> HPCOM-FB 10 MIC <-> MIC 5,10 FMINL <-> FMINL 10,14 FMINR <-> FMINR 10,14	GPIO 5 CTP-INT <-> CTP-INT 5 CTP-RST <-> CTP-RST 5 IR-RX <-> IR-RX 10 PA-SHDN <-> PA-SHDN 5 PWM1 <-> PWM1 5 PWR-ON <-> PWR-ON 5 PWR-OFF <-> PWR-OFF

MIC <-> MIC 5,10

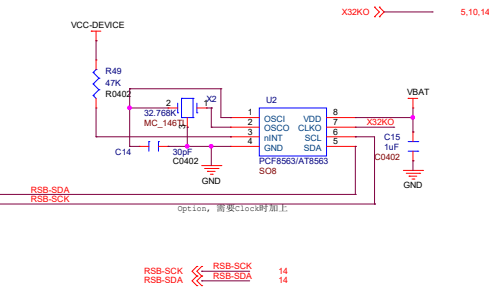


Allwinner Technology Co., Ltd
Design Name
AW_F1C200s_V10
Size AS Page Name CPU DDR1 Rev
Date Friday, April 06, 2018 Sheet 5 of 16

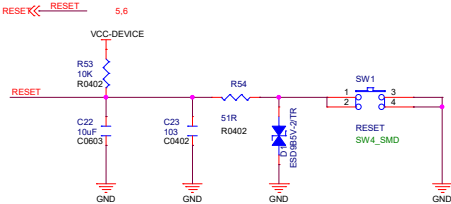
OSC



RTC

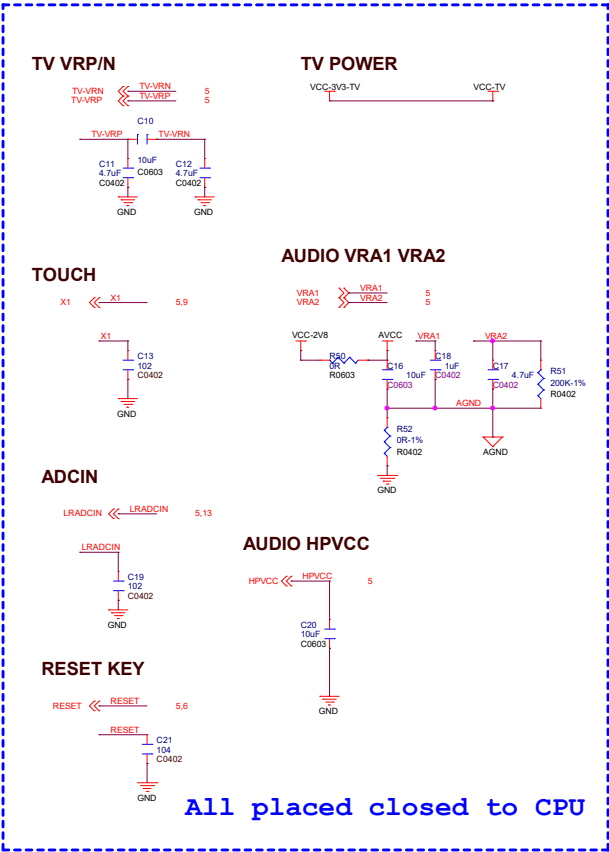


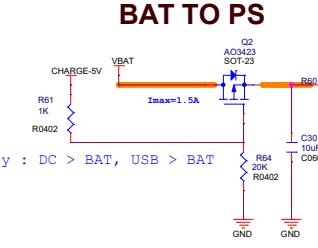
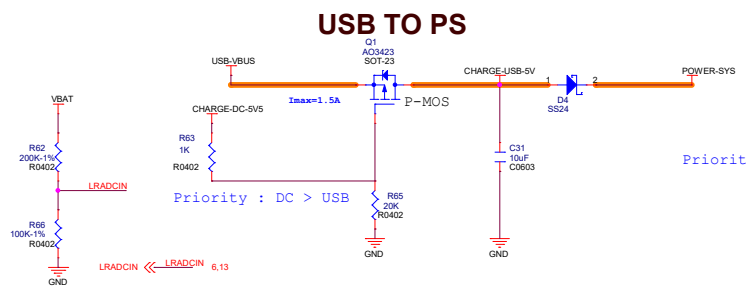
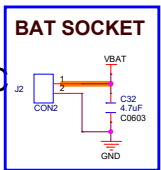
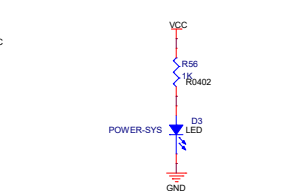
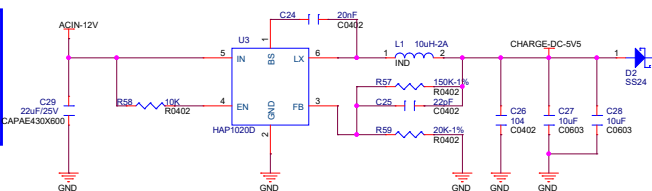
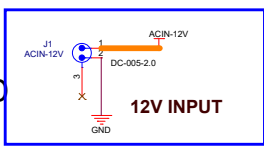
RESET



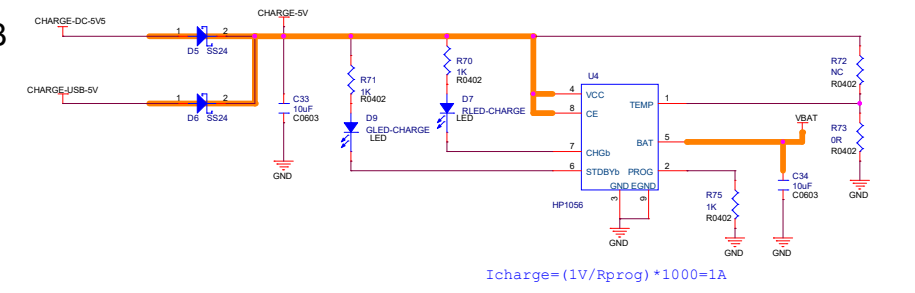
Low maintain 22ms to (3.3V * 0.2)

Beside CPU



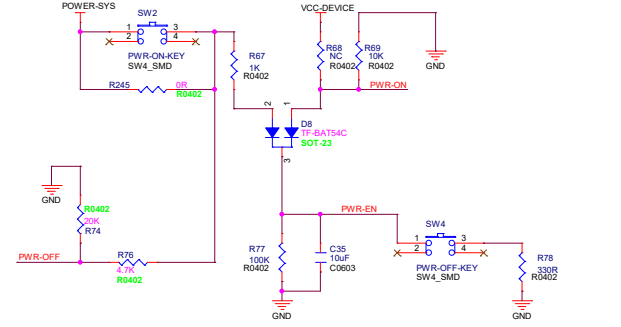


CHARGE CONTROL

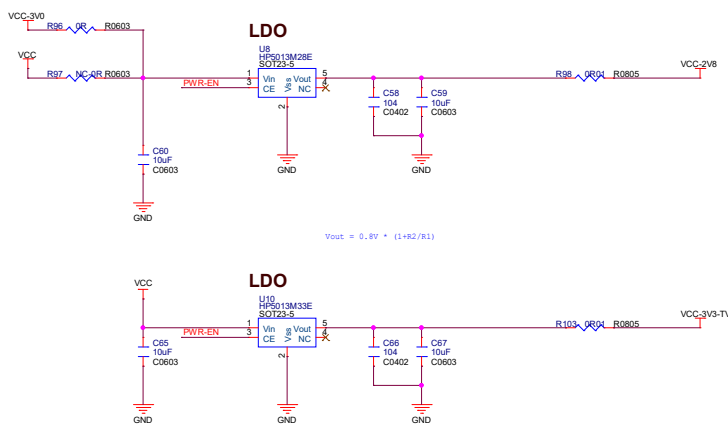
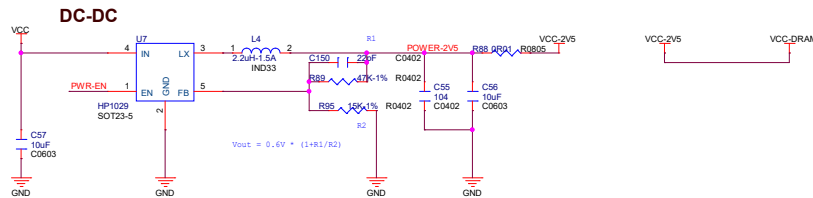
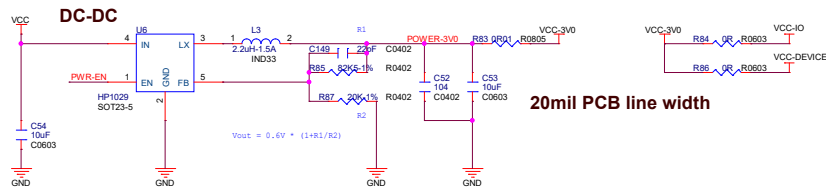
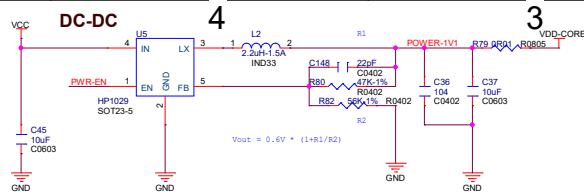


- Layout: power line 60mil
- Layout: power line 40mil
- Layout: power line 30mil

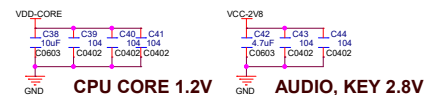
POWER-ON KEY



power up :SW KEY on , power down : PWR-EN keep high for 1000ms
Layout Guide : POWER-SW 's ON , OFF silkscreen text needed

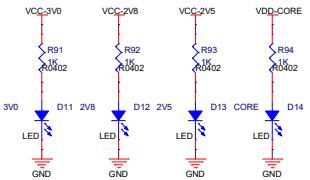
POWER 2⁵

CPU decouple cap 1

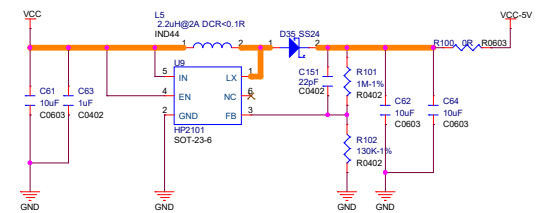



**Ensure one Power pin with a cap
place caps closed to CPU**

POWER LED

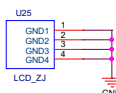
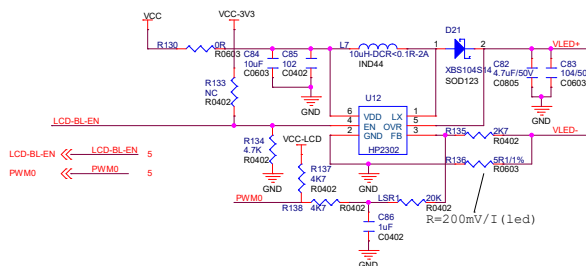
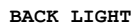
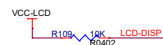
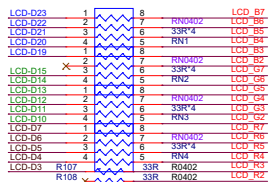


place at a same domain



	AllWinner Technology Co., Ltd		
	Design Name AW_F1C200s_V10		
	Size A3	Page Name POWER	Rev
	Date: Friday, April 06, 2018 Sheet 8 of 16		

5	4	3	2	1
---	---	---	---	---



AllWinner Technology Co.,Ltd			
Design Name AW_F1C200s_V10			
Size A3	Page Name LCD		Rev
Date:	Saturday, April 07, 2018	Sheet	9 of 16

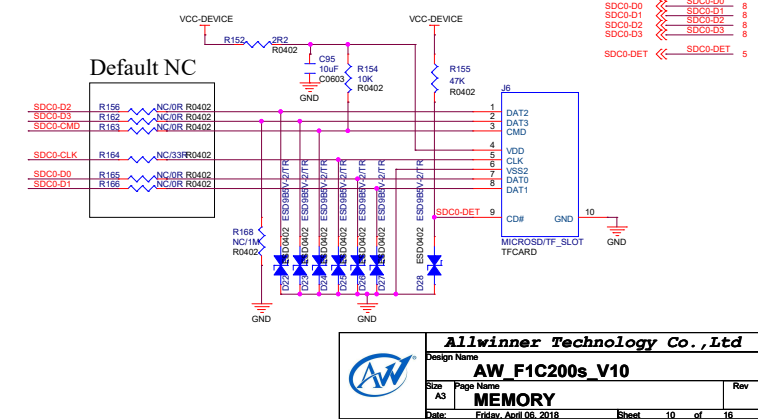
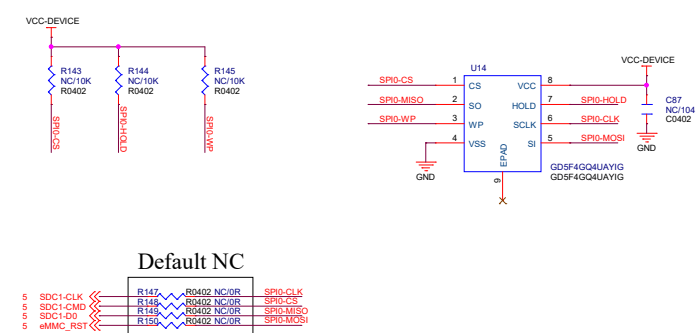
4

C

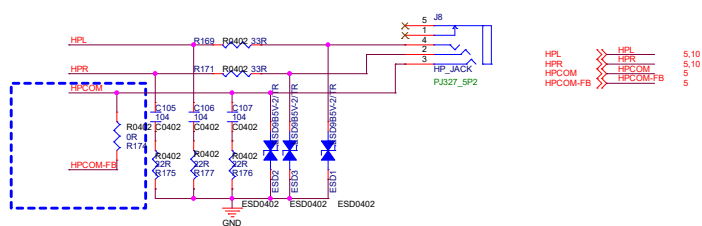
B

A

2

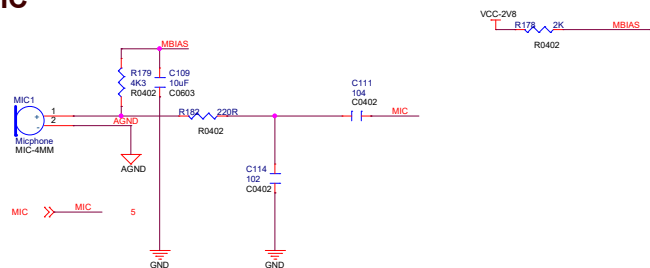


HEADPHONE

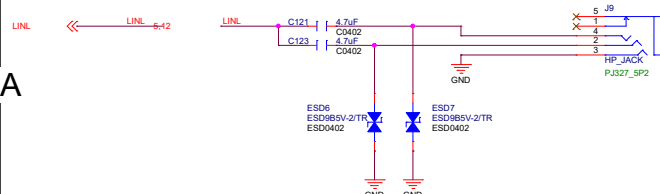


place closed to HP JACK

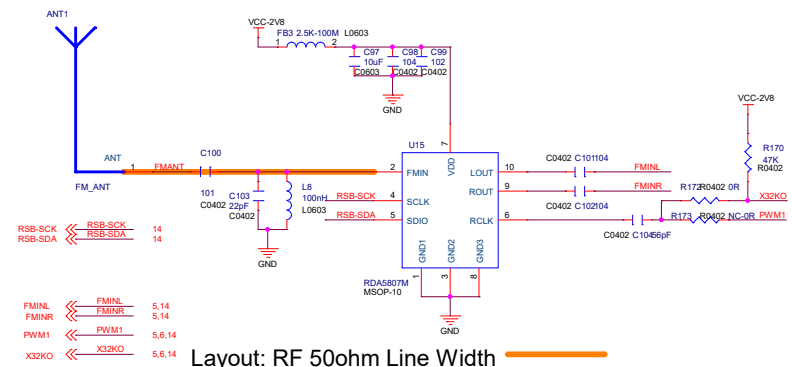
MIC



LINE IN

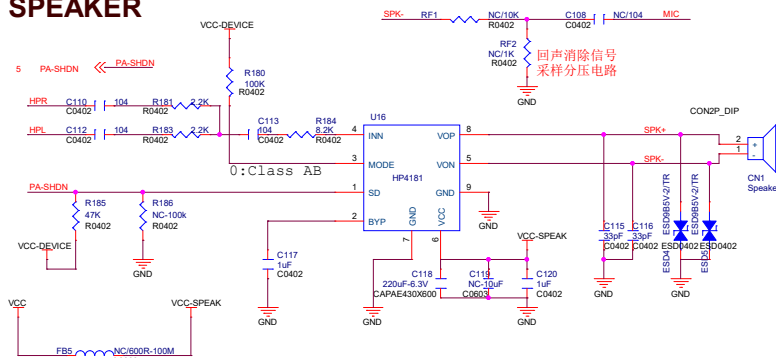


3
FM

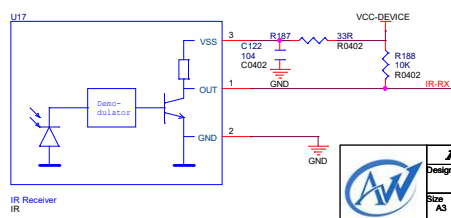



Layout: RF 50ohm Line Width

SPEAKER

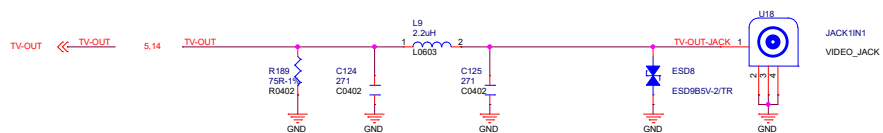


IR MODULE

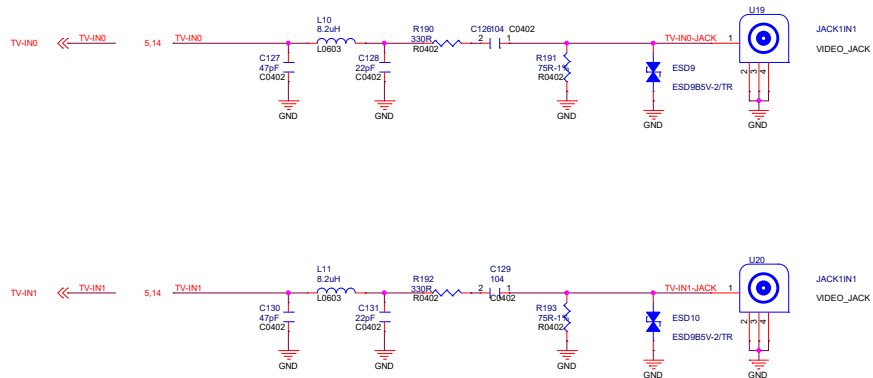


	AllWinner Technology Co., Ltd		
	Design Name AW_F1C200s_V10		
	Size A3	Page Name AUDIO	Rev
	Date: Friday, April 06, 2018		
		Sheet 11 of 16	

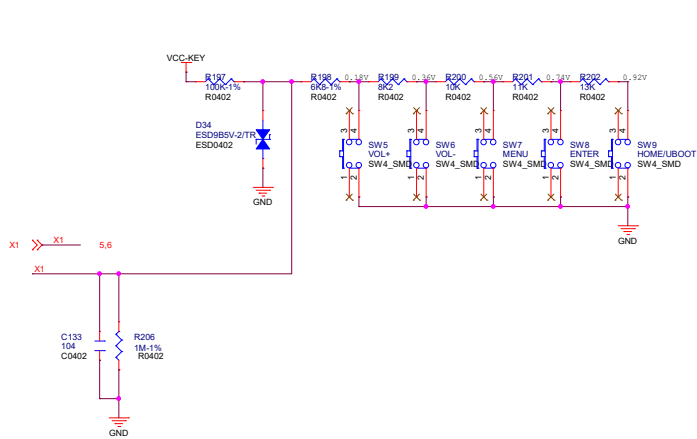
TV OUT



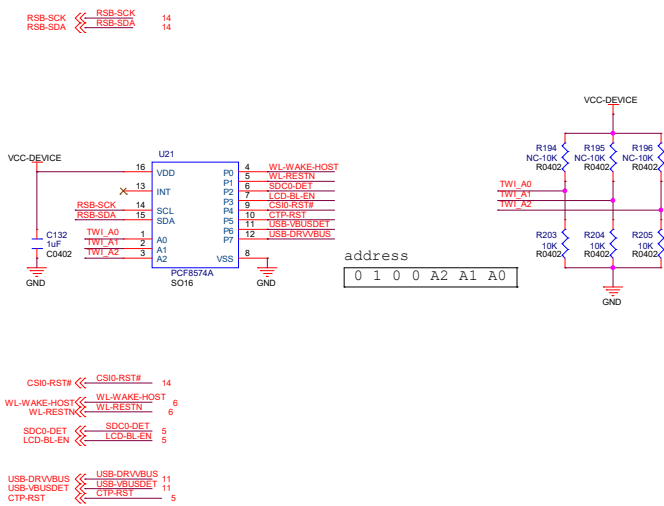
TV IN



KEY

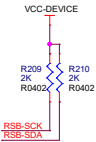


IO EXPAND



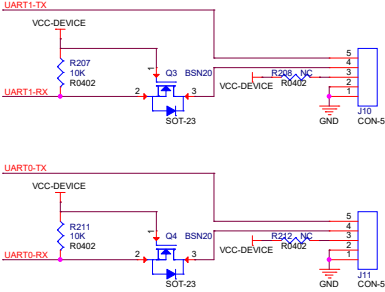
TWI RSB

RSB-SCK
RSB-SDA

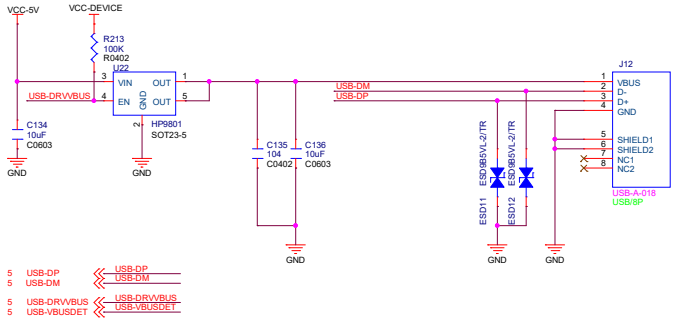


UART

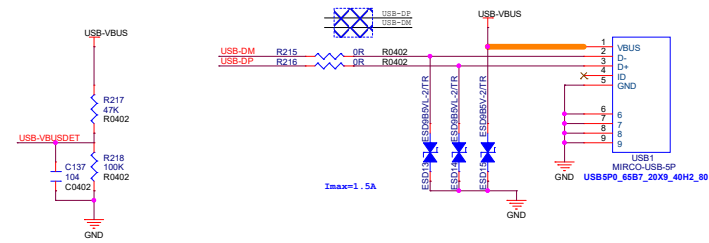
UART1-TX
UART1-RX
UART0-TX
UART0-RX



USB OTG

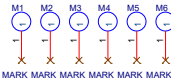
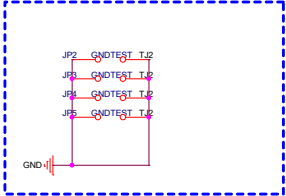


Differential pairs
Z0= 90 ohm



TEST POINT

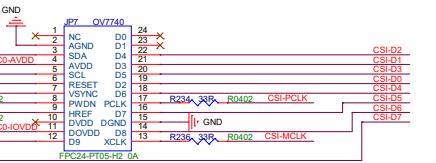
在板子的
周围摆放



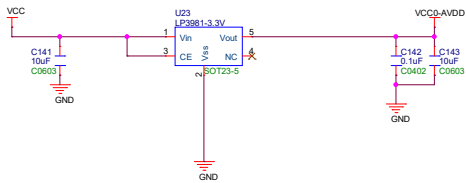
CAMERA

5,6,13,15 RSB-SCK
5,6,13,15 RSB-SDA

CSI-D0
CSI-D1
CSI-D2
CSI-D3
CSI-D4
CSI-D5
CSI-D6
CSI-D7
CSI-VSYNC
CSI-HSYNC
CSI-PCLK
CSI-MCLK



默认GC0308



I2S

RSB-SCK
RSB-SDA

DA-MCLK-OD
DA-MCLK-OE

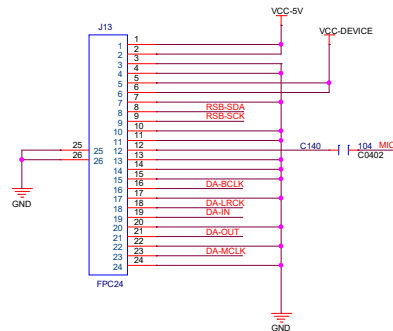
DA-BCLK-OD
DA-BCLK-OE

DA-LRCK-OD
DA-LRCK-OE

DA-OUT-OD
DA-OUT-OE

DA-IN-OD
DA-IN-OE

MIC



Allwinner Technology Co., Ltd

Design Name
AW_F1C200s_V10

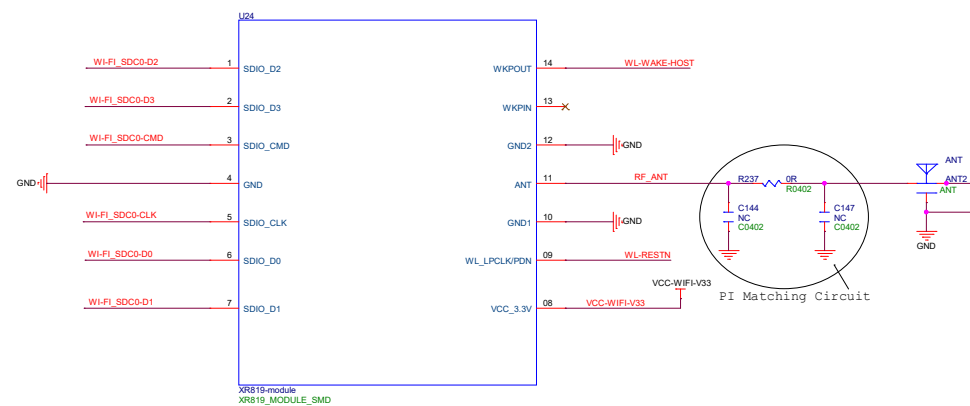
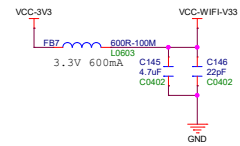
Size
A3


Page Name
CAMERA DIGI-AUDIO

Date
Friday, April 06, 2018

Sheet
15 of 16

XR819 ON BOARD



		Allwinner Technology Co., Ltd	
		Design Name	AW_F1C200s_V10
Size	Page Name	Rev	
Custom	XR819		
Date:	Friday, April 08, 2018	Sheet	16 of 16