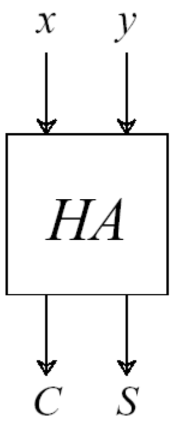
LAB 1

DESIGN OF ARITHMETIC CIRCUIT

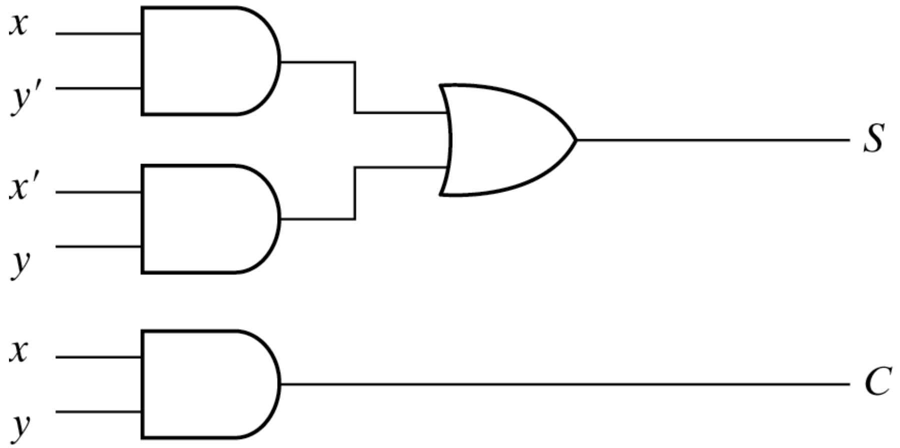
Adder

- The most basic arithmetic operation is the addition of 2 bits. A combinational circuit that performs this operation is called a *half-adder*.
- A combinational circuit that performs the addition of 3 bits is called a *full-adder*, which can be implemented by 2 half-adders.

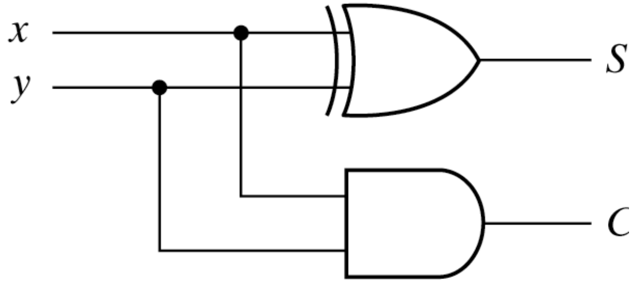


x	y	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Half Adder

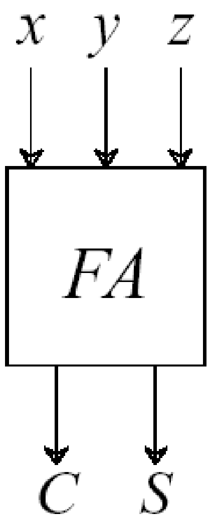


(a) $S = xy' + x'y$
$C = xy$



(b) $S = x \oplus y$
$C = xy$

Full Adder



x	y	z	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Full Adder

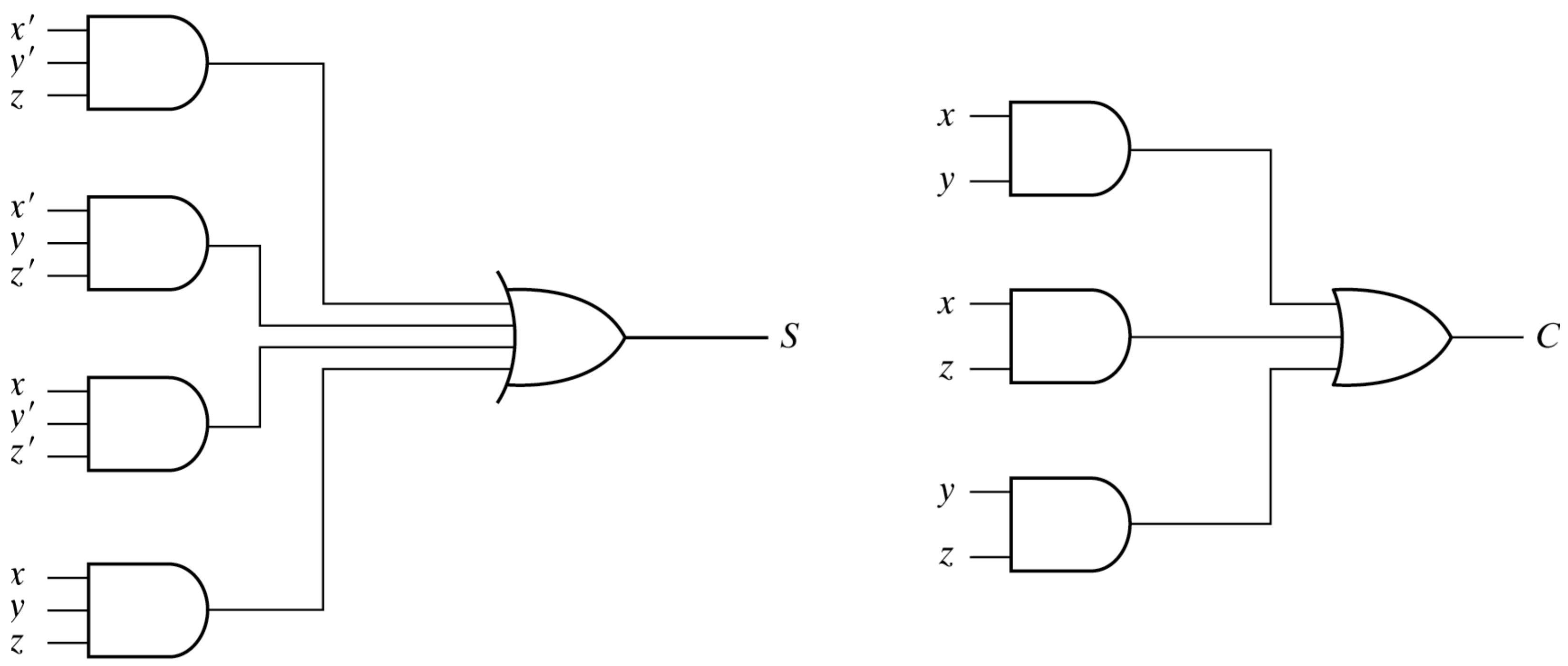
x \ yz	00	01	11	10
0		1		1
1	1		1	

$$S = x'y'z + x'yz' + xy'z' + xyz$$

x \ yz	00	01	11	10
0			1	
1		1	1	1

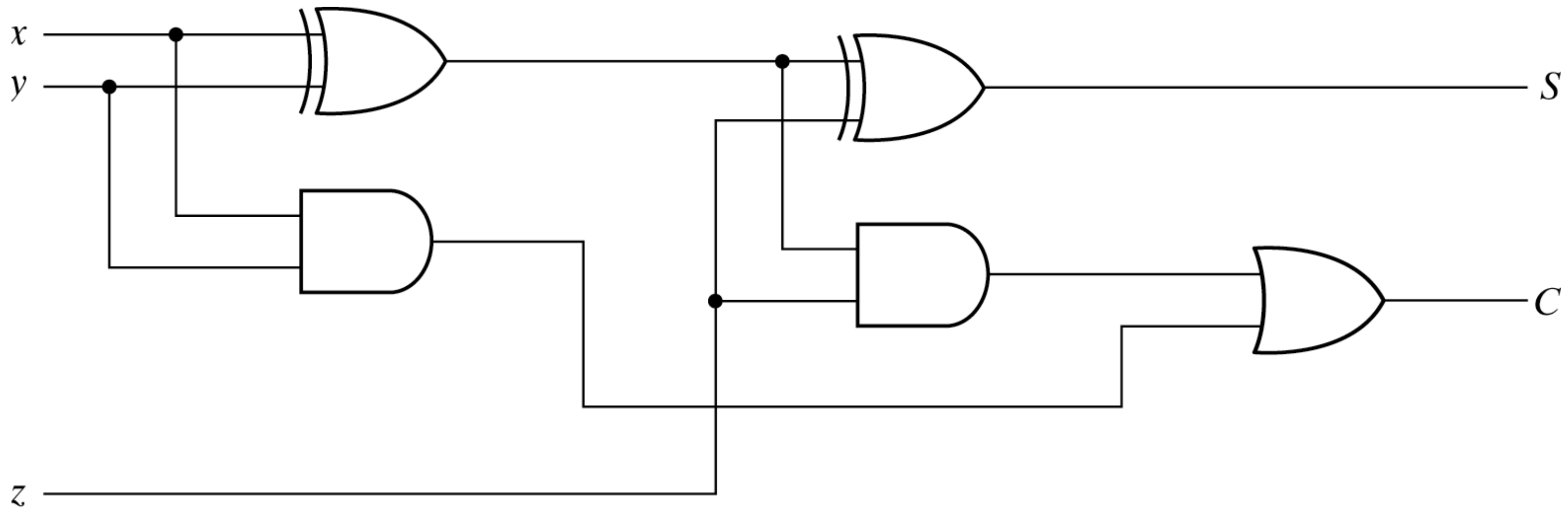
$$C = xy + xz + yz$$

Implementation of FA



Implementation of FA

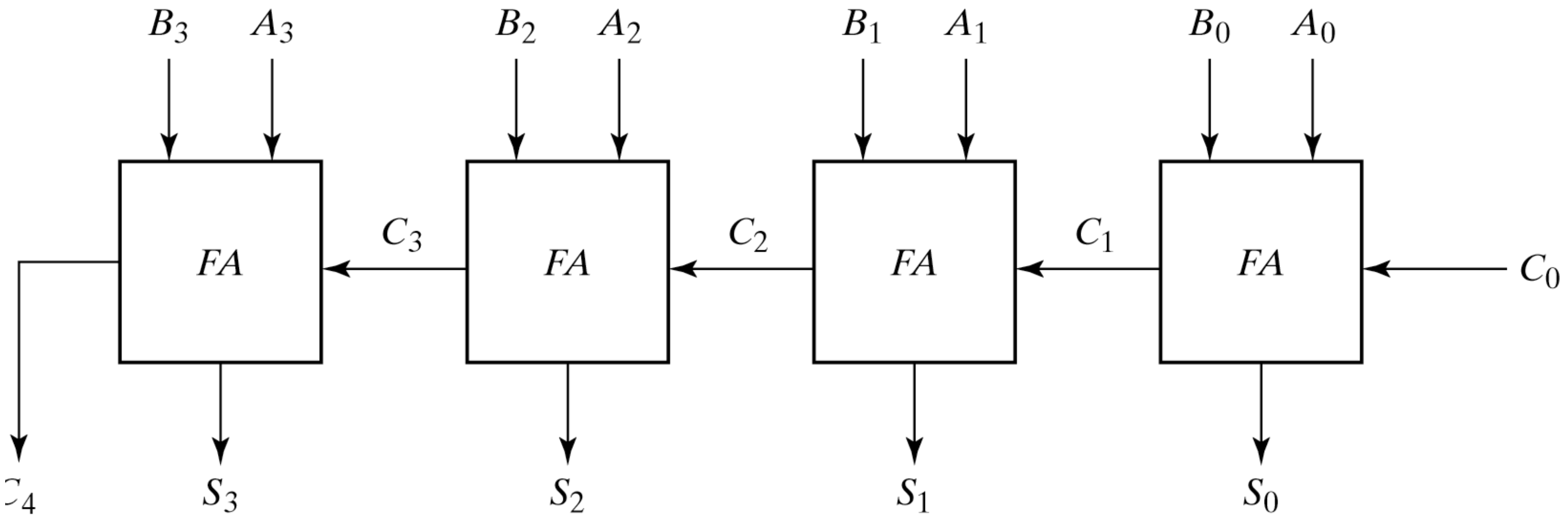
(with two half adder)



$S = xy'z' + x'yz' + xyz + x'y'z$
$\quad = z'(xy' + x'y) + z\,(xy + x'y')$
$\quad = z'(xy' + xy') + z\,(xy' + x'y)'$
$\quad = z \oplus (x \oplus y)$

$C = x'yz + xy'z + xyz' + xyz$
$\quad = x'yz + xy'z + xy$
$\quad = z\,(x'y + xy') + xy$
$\quad = z\,(x \oplus y) + xy$

Binary Adder



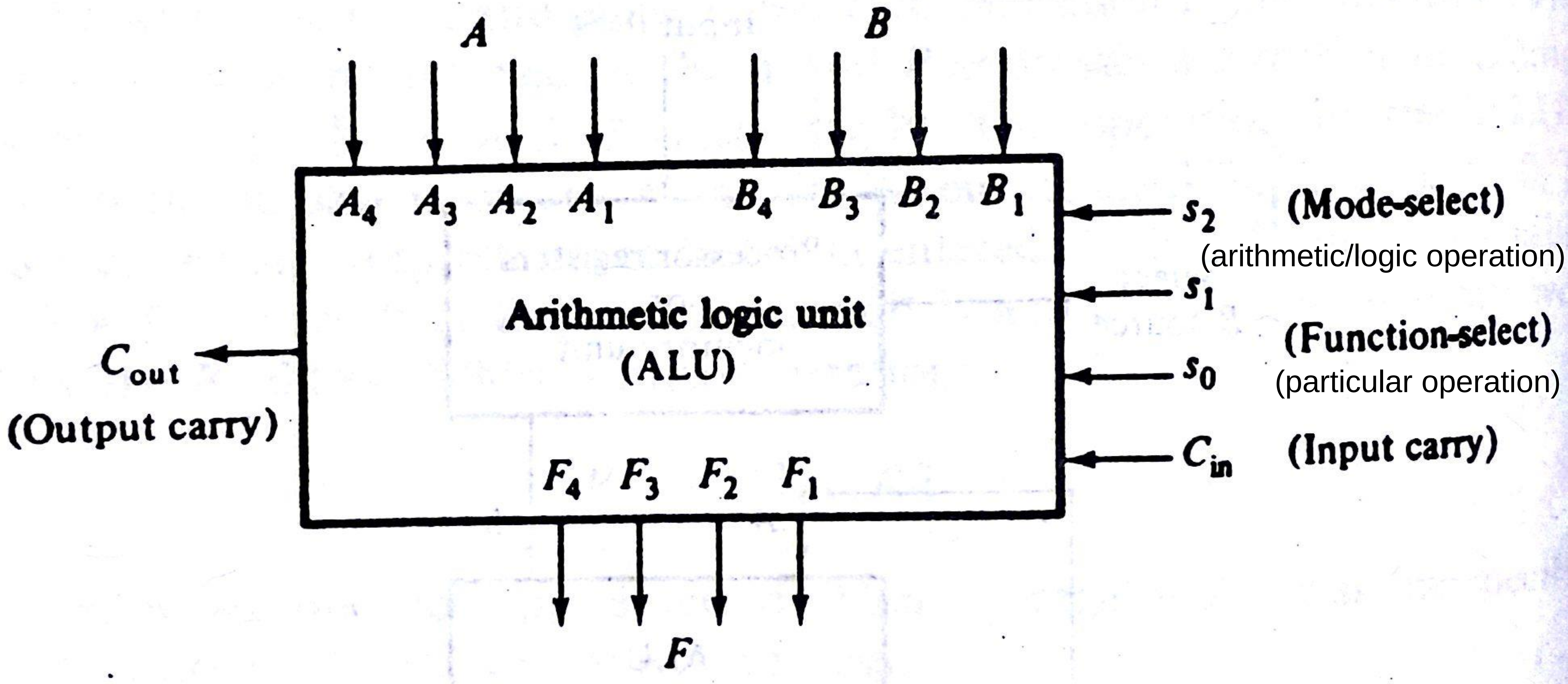


Figure 9-5 Block diagram of a 4-bit ALU

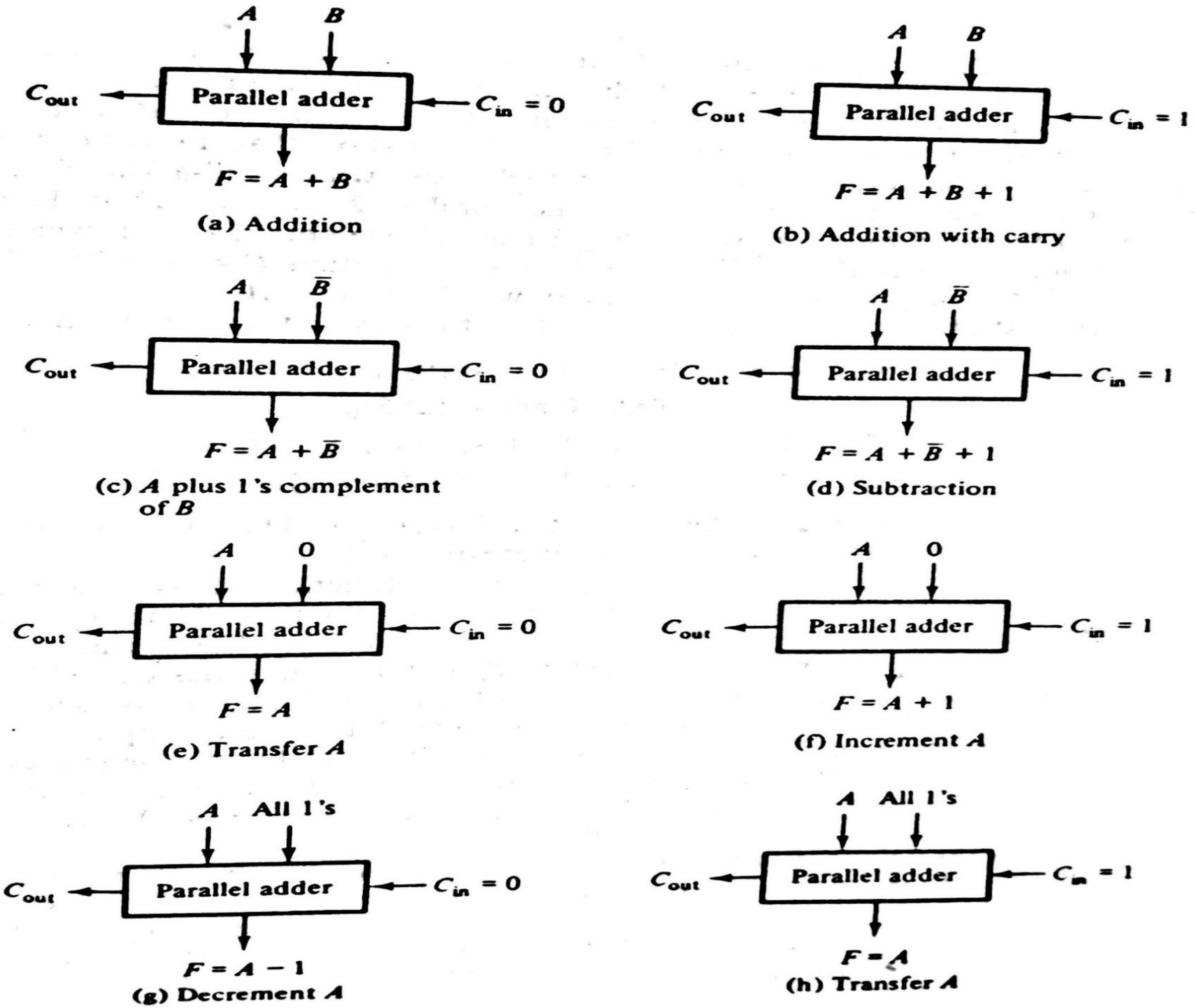


Figure 9-6 Operations obtained by controlling one set of inputs to a parallel adder

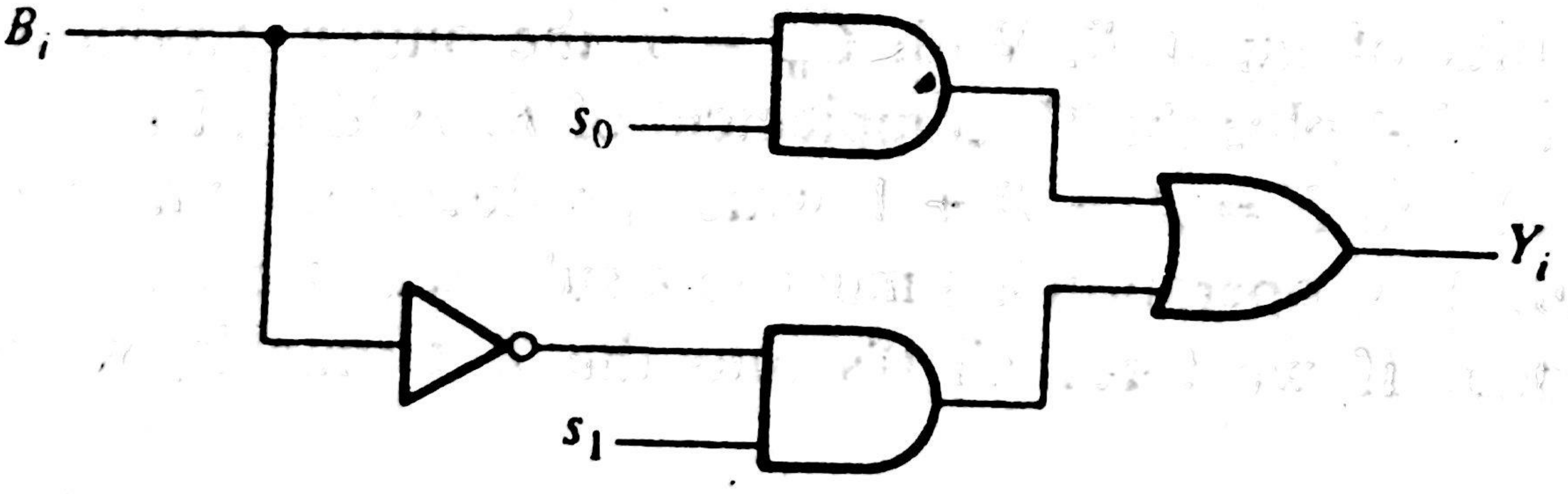
$F = A + 0 = A$, which transfers input A into output F. Adding 1 through C_{in} as in Fig. 9-6(f), we obtain $F = A + 1$, which is the increment operation.

The condition illustrated in Fig. 9-6(g) inserts all 1's into the B terminals. This produces the decrement operation $F = A - 1$. To show that this condition is indeed a decrement operation, consider a parallel adder with n full-adder circuits. When the output carry is 1, it represents the number 2^n because 2^n in binary consists of a 1 followed by n 0's. Subtracting 1 from 2^n, we obtain $2^n - 1$, which in binary is a number of n 1's. Adding $2^n - 1$ to A, we obtain $F = A + 2^n - 1 = 2^n + A - 1$. If the output carry 2^n is removed, we obtain $F = A - 1$.

To demonstrate with a numerical example, let $n = 8$ and $A = 9$. Then:

$$\begin{aligned}
A &= 0000\ \ 1001 = (9)_{10} \\
2^n &= 1\ 0000\ \ 0000 = (256)_{10} \\
2^n - 1 &= 1111\ \ 1111 = (255)_{10} \\
A + 2^n - 1 &= 1\ 0000\ \ 1000 = (256 + 8)_{10}
\end{aligned}$$

Removing the output carry $2^n = 256$, we obtain $8 = 9 - 1$. Thus, we have decremented A by 1 by adding to it a binary number with all 1's.



s_1	s_0	Y_i
0	0	0
0	1	B_i
1	0	B_i'
1	1	1

Figure 9-7 True/complement, one/zero circuit

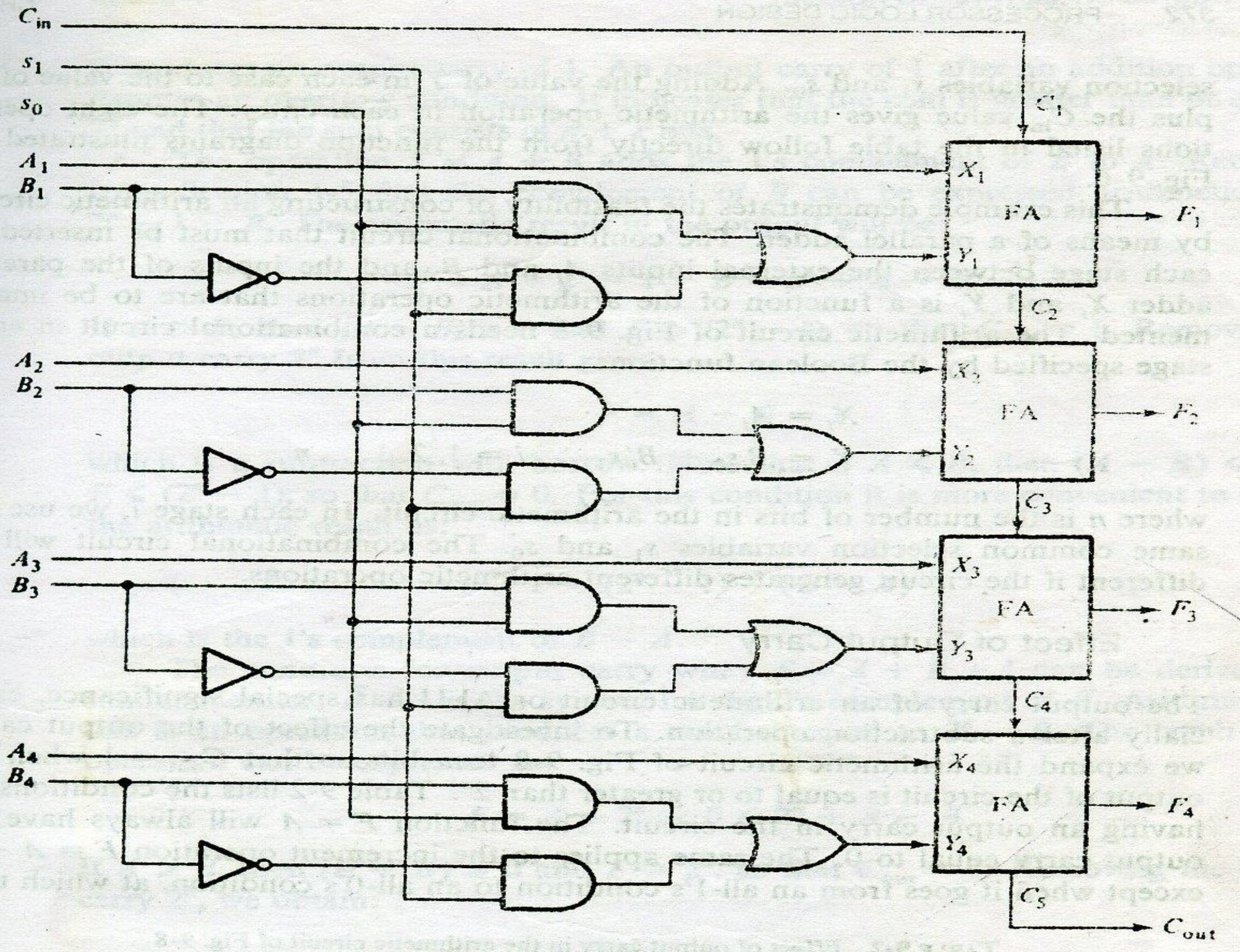


Figure 9-8 Logic diagram of arithmetic circuit

Function select			Y equals	Output equals	Function
s_1	s_0	C_{in}			
0	0	0	0	$F = A$	Transfer A
0	0	1	0	$F = A + 1$	Increment A
0	1	0	B	$F = A + B$	Add B to A
0	1	1	B	$F = A + B + 1$	Add B to A plus 1
1	0	0	$\overline{B}$	$F = A + \overline{B}$	Add 1's complement of B to A
1	0	1	$\overline{B}$	$F = A + \overline{B} + 1$	Add 2's complement of B to A
1	1	0	All 1's	$F = A - 1$	Decrement A
1	1	1	All 1's	$F = A$	Transfer A

Enough Talk, Let’s Work ☺