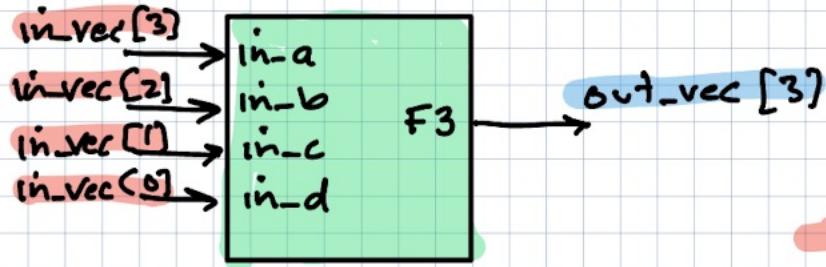


logic_functions_top

logic_func3 func3

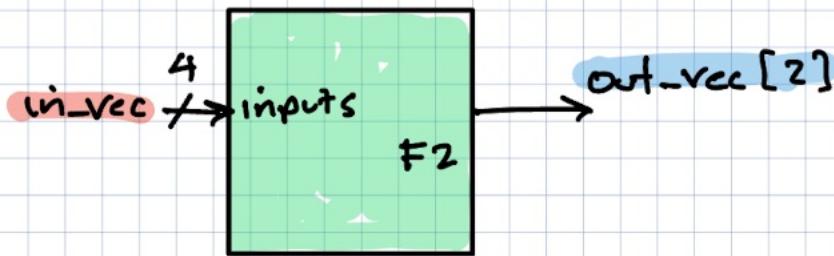


inputs

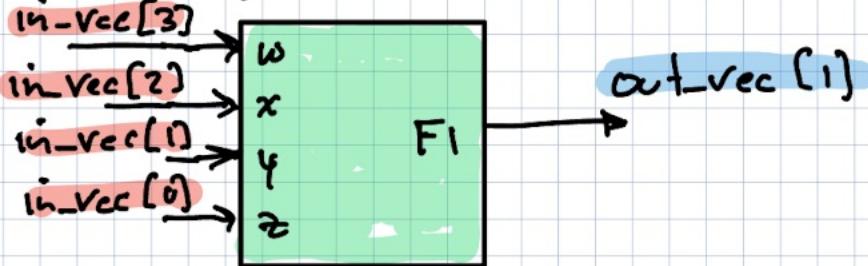
outputs

wires

logic_func2 func2



logic_func1 func1



logic_func0 func0

