第1章 计算机设计基础

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1.4 实现技术的趋势

- 摩尔定律（Moore Law）
- 1965年，他预测工业界集成在一个计算机芯片上的元件数量每年翻一番。 1975年，他更新预测为每两年翻一番。

这已经成为半导体工业界在降低电子器件成本的同时提供更强大芯片的指导原则。

实现技术的趋势

- 集成电路逻辑技术
  - 晶体管密度：增加 35% per year
  - Die size（芯片尺寸）： 10%-20% per year
  - 每个芯片晶体管数量:40-55% per year
- 半导体DRAM
  - 容量：25-40% per year
  - 访问速度： about 10% per year
- 磁盘技术
  - 密度： 30% p.y. Before 1990; 60% p.y. 1990-1996
  - 100% p.y. 1996-2004 ; 30% p.y. after 2004
  - 容量： about 60% per year
- 网络
  - 带宽： 10Mb ⟶ 100Mb ⟶ 1Gb
    10 years 5 years

设计者常常为下一代实现技术进行设计。

特别注意

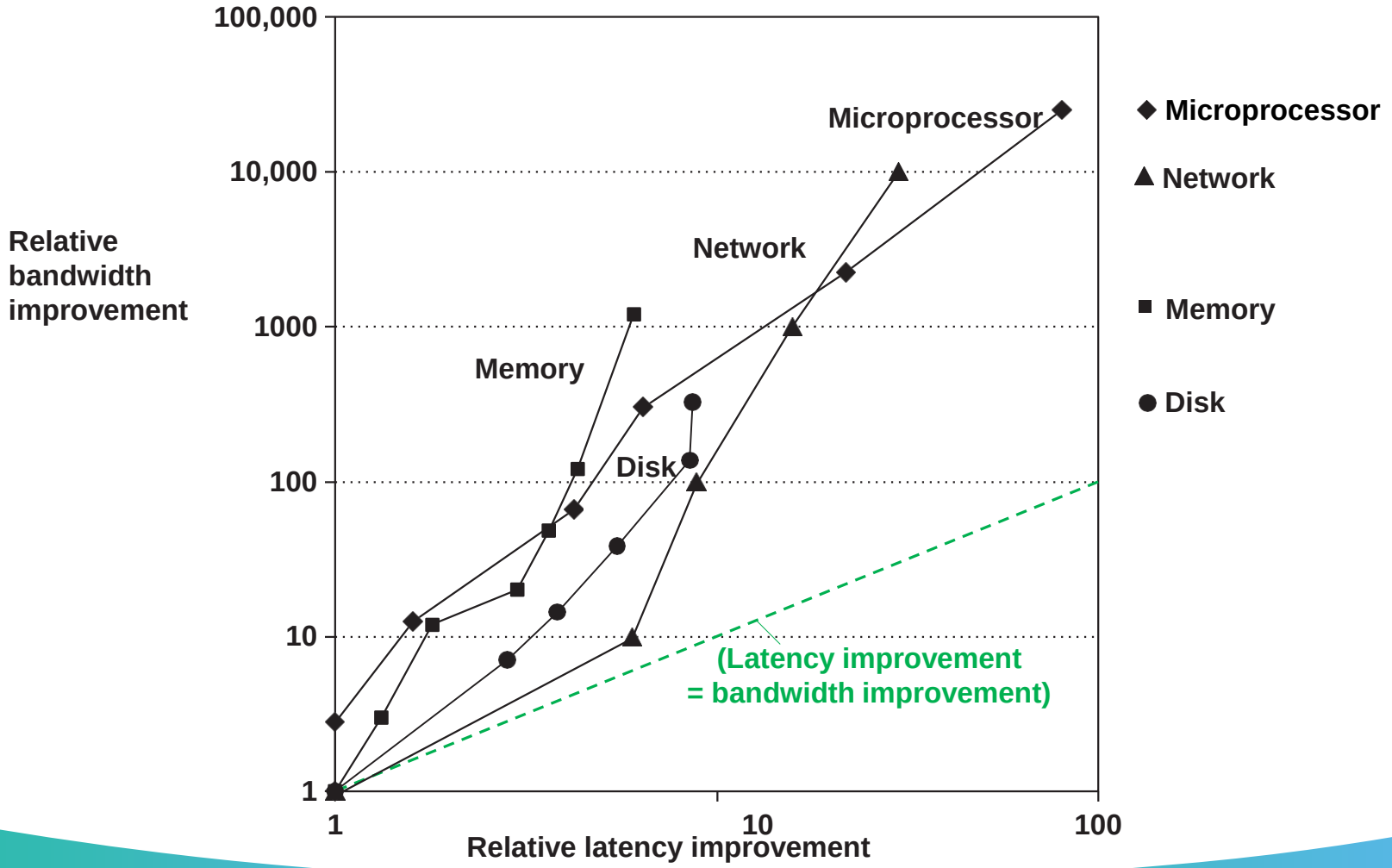
- 经验法则（A rule of thumb）
  - 成本减少速度与密度增加速度成比例

- 技术阈值（Technology thresholds）：对设计有重大影响
  - 实现技术在持续改进到阈值，就会使设计发生飞跃

  例如：1980年代末，单芯片可集成百万只晶体管，使得一级Cache可以与CPU集成在一个芯片上。

- 带宽/吞吐量：在给定时间完成的工作总量
- 时延/响应时间: 一个事件从开始到完成的时间
- 带宽改进优于时延
- 经验法则（Rule of thumb）
  - 带宽增加速度与时延平方改进速度成比例

性能趋势： 带宽改进优于时延



集成电路 技术挑战

- 集成电路特征:特征尺寸 (feature size)
  - 10 microns in 1971 → 0.18microns in 2001 → 0.09 microns in 2006 → 65nm →40nm →32nm in 2011 →7nm in 2018
  - 经验法则：晶体管性能改进与特征尺寸减少成线性关系。
- 集成电路密度改进既是机会也是挑战：
  - 纳米效应：特征尺寸减少→连线缩短→单位长度的电阻和电容增加→ 信号延迟增大（与电阻和电容的乘积成正比）

    （特征尺寸减少→晶体管越小→漏电流越大→ 功耗增大/单位面积）
- 导线信号延迟---主要的设计限制，与工艺有关

Figure 1.11

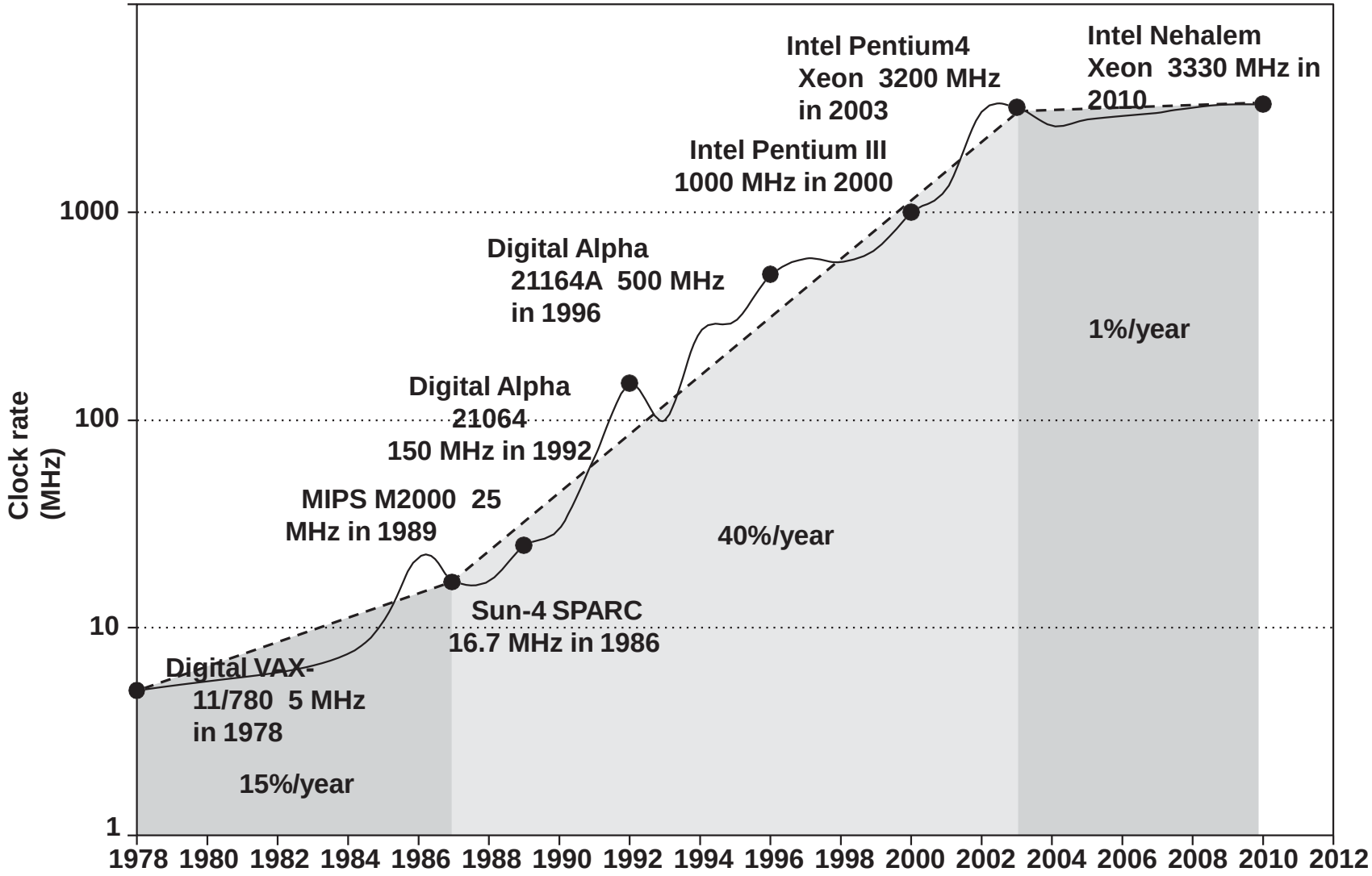


Figure 1.11 Growth in clock rate of microprocessors.

Exercise 1.8(a)

- One challenge for architects is that the design created today will require several years of implementation, verification, and testing before appearing on the market. This means that the architect must project what the technology will be like several years in advance. Sometimes, this is difficult to do.
- (a) According to the trend in device scaling observed by Moore's law, the number of transistors on a chip in 2015 should be how many times the number in 2005?

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The ability of the microprocessor to ride the improvements in integrated circuit technology led to a higher rate of performance improvement—roughly 35% growth per year. Integrated circuit logic technology—Transistor density increases by about 35% per year.

a. $(1.35)^{10}$ = approximately 20.1

Exercise 1.8(b)

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- (b) The increase in clock rates once mirrored this trend. Had clock rates continued to climb at the same rate as in the 1990s, approximately how fast would clock rates be in 2015?

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The clock of Intel Pentium4 Xeon was 3200 MHz in 2003
The clock was increased by 40% in the 1990s

$3200 \times (1.4)^{12}$ = approximately 181,420.5

Exercise 1.8(c)

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- (c) At the current rate of increase, what are the clock rates now projected to be in 2015?

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- (c) At the current rate of increase, what are the clock rates now projected to be in 2015?

The clock of Intel Pentium4 Xeon was 3200 MHz in 2003
The clock was increased by 1% in the 2000s

c. $3200 \times (1.01)^{12}$ = approximately 3605.8

Exercise 1.8(d)

- One challenge for architects is that the design created today will require several years of implementation, verification, and testing before appearing on the market. This means that the architect must project what the technology will be like several years in advance. Sometimes, this is difficult to do.
- (d) What has limited the rate of growth of the clock rate, and what are architects doing with the extra transistors now to increase performance?

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d. Power density, which is the power consumed over the increasingly small area, has created too much heat for heat sinks to dissipate. This has limited the activity of the transistors on the chip. Instead of increasing the clock rate, manufacturers are placing multiple cores on the chip.

Exercise 1.8(e)

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- (e) The rate of growth for DRAM capacity has also slowed down. For 20 years, DRAM capacity improved by 60% each year. That rate dropped to 40% each year and now improvement is 25 to 40% per year. If this trend continues, what will be the approximate rate of growth for DRAM capacity by 2020?

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e. Anything in the 15–24% range would be a reasonable conclusion based on the decline in the rate over history. As the sudden stop in clock rate shows, though, even the declines do not always follow predictions.