第1章 计算机设计基础

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1.6 成本的趋势

- *元器件成本是设计者需要考虑的一个方面*
- *影响成本的主要因素：*
  - Time----元器件价格随着时间而下降（实现技术没有实质性改进）。因为随着时间推移产出率不断增高。
  - Volume （产量）----提高意味着制造效率提高
  - Commodification（商品）----元器件供应商之间的竞争会降低成本

每个集成电路成本的计算：

$$\text{集成电路成本} = \frac{\text{芯片成本} + \text{掩膜成本} + \text{芯片测试成本} + \text{封装成本}}{\text{最终测试成品率}}$$

$$\text{芯片成本} = \frac{\text{晶园成本}}{\text{每片晶园的芯片数} \times \text{芯片成品率}}$$

$$\text{每片晶圆的芯片数} = \frac{\text{晶圆面积}}{\text{芯片面积}} - \frac{\text{晶圆周长}}{\text{芯片对角线长}}$$

$$\text{芯片成品率} = \text{晶圆成品率} \times \left(1 + \frac{\text{单位面积的缺陷数} \times \text{芯片面积}}{\alpha}\right)^{-\alpha}$$

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结论1，芯片面积直接影响芯片成本：

芯片面积大 → 晶圆上芯片数减少 →芯片成本上升

4e:

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假设为100%

- α是取决于制造工艺复杂性的一个参数，与掩膜的层数成正比。

对于目前复杂的CMOS工艺来说，合适的估计是 $\alpha = 4$ 。

- 单位面积缺陷数是衡量材料与工艺的一个指标，典型值为 $0.5 \sim 1/cm^2$

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5e:

$$\boldsymbol{Die\ yield = Wafer\ yield/(1 + Defects\ per\ unit\ area * Die\ area)^N}$$

Assume the *Wafer yield* is 100%

Defects per unit area is a measure of the random manufacturing defects that occur. In 2010, the value was typically 0.1 to 0.3 defects per square inch, or 0.016 to 0.057 defects per square centimeter, for a 40 nm process.

For 40 nm processes in 2010, N ranged from 11.5 to 15.5.

例：龙芯2F的硅片成本

- **龙芯2F面积为43平方毫米**
- **晶片成品率 ＝ $(1+b*晶片面积/a)^{-a}$ =78%**
  - b为单位面积缺陷数，设为0.6
  - a为衡量复杂度的参数，设为4
- **每个12寸晶圆的晶片数 ＝ (晶圆的面积/晶片的面积)－(晶圆的周长/$(2*晶片面积)^{1/2}$) =1592**
- **好的晶片数为1242个**
- **设90nm的12寸晶元成本为3000美元**
- **每个2F的晶元成本为2.4美元**

例子：直径为30cm的晶圆上有多少边长为1.5cm的芯片？

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- 答：芯片面积为（1.5cm）^{2} = 2.25 cm^2

$$\text{每片晶圆的芯片数} = \frac{\pi \times (30/2)^2}{2.25} - \frac{\pi \times 30}{2.12} = 270$$

类似的，直径30cm晶圆上边长为1 cm的芯片数为：640

例(4e)：设单位面积残次密度为0.4/cm^2，且 α=4.0，分别求边长1.5cm和1.0cm芯片的成品率。

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答：

$$\text{1.5cm芯片成品率} = \left(1 + \frac{0.4 \times 2.25}{4.0}\right)^{-4} = 0.44$$

$$\text{1.0cm芯片成品率} = \left(1 + \frac{0.4 \times 1.00}{4.0}\right)^{-4} = 0.68$$

结论2：芯片面积大→成品率更低→ 芯片成本上升

直径30cm晶圆有270 ×0.44=120个面积2.25cm^{2}成品芯片，
或者有640 ×0.68=435个面积1cm^{2}成品芯片。

- 2006年，设30cm空白晶圆成本是5500美元，

  1个$1.00cm^2$的芯片成本----5500/435=13 美元

  1个$2.25cm^2$的芯片成本----5500/120=46 美元

推论：芯片面积增加到2倍，则成本增加到约4倍。

Example

- **Find the die yield for dies that are 1.5 cm on a side and 1.0 cm on a side, assuming a defect density of 0.031 per cm^2 and N is 13.5.**

$$\boldsymbol{Die\ yield} = 1/(\mathbf{1} + \boldsymbol{Defects\ per\ unit\ area} * \boldsymbol{Die\ area})^{\boldsymbol{N}}$$

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- **Answer:**

The total die areas are 2.25 cm^2 and 1.00 cm^2. For the larger die, the yield is

$$\text{Die yield} = 1/(1 + 0.031 \times 2.25)^{13.5} = 0.40$$

For the smaller die, the yield is

$$\text{Die yield} = 1/(1 + 0.031 \times 1.00)^{13.5} = 0.66$$

That is, less than half of all the large dies are good but two-thirds of the small dies are good.

Exercise1.1

Chip	Die size (mm^2)	Estimated defect rate (per cm^2)	Manufacturing size (nm)	Transistors (millions)
IBM Power5	389	.30	130	276
Sun Niagara	380	.75	90	279
AMD Opteron	199	.75	90	233

Figure 1.22 Manufacturing cost factors for several modern processors.

Figure 1.22 gives the relevant chip statistics that influence the cost of several current chips.

a. **What is the yield for the IBM Power5?**

b. **Why does the IBM Power5 have a lower defect rate than the Niagara and Opteron?**

$$Die\ yield = \left(1 + \frac{Defects\ per\ unit\ area\ * Die\ area}{\alpha}\right)^{-\alpha}$$

α=4.0

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a. Yield $=(1+\frac{0.3*3.89}{4})^{-4}=0.36$

b. It is fabricated in a larger technology, which is an older plant. As plants age, their process gets tuned, and the defect rate decreases.