EEE104 – Digital Electronics

Lecture 17

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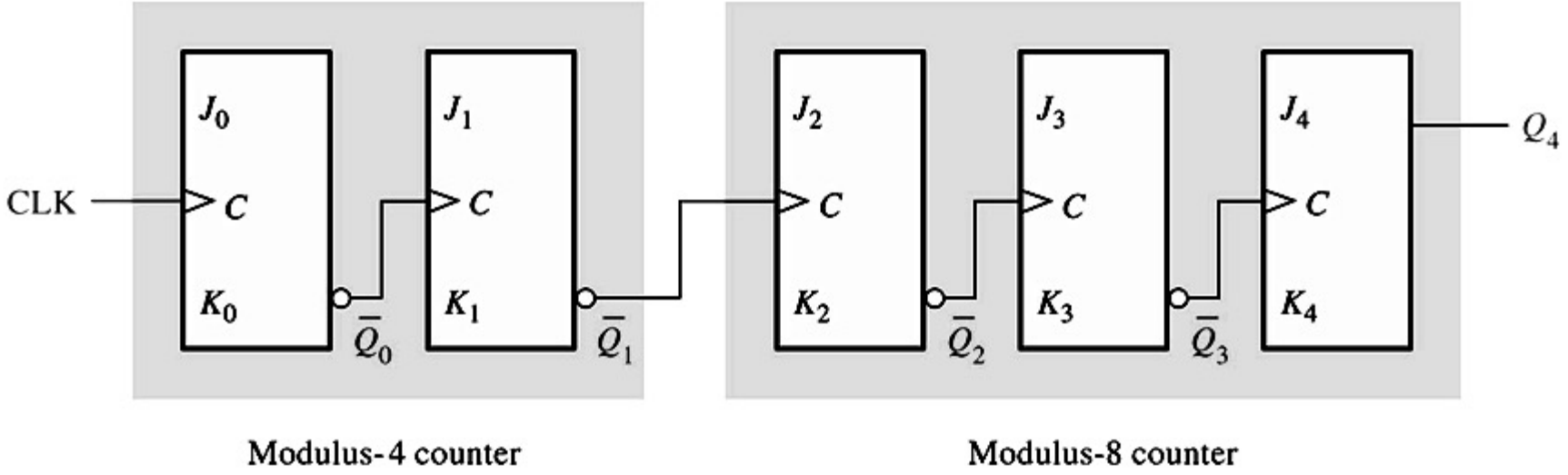
In This Session

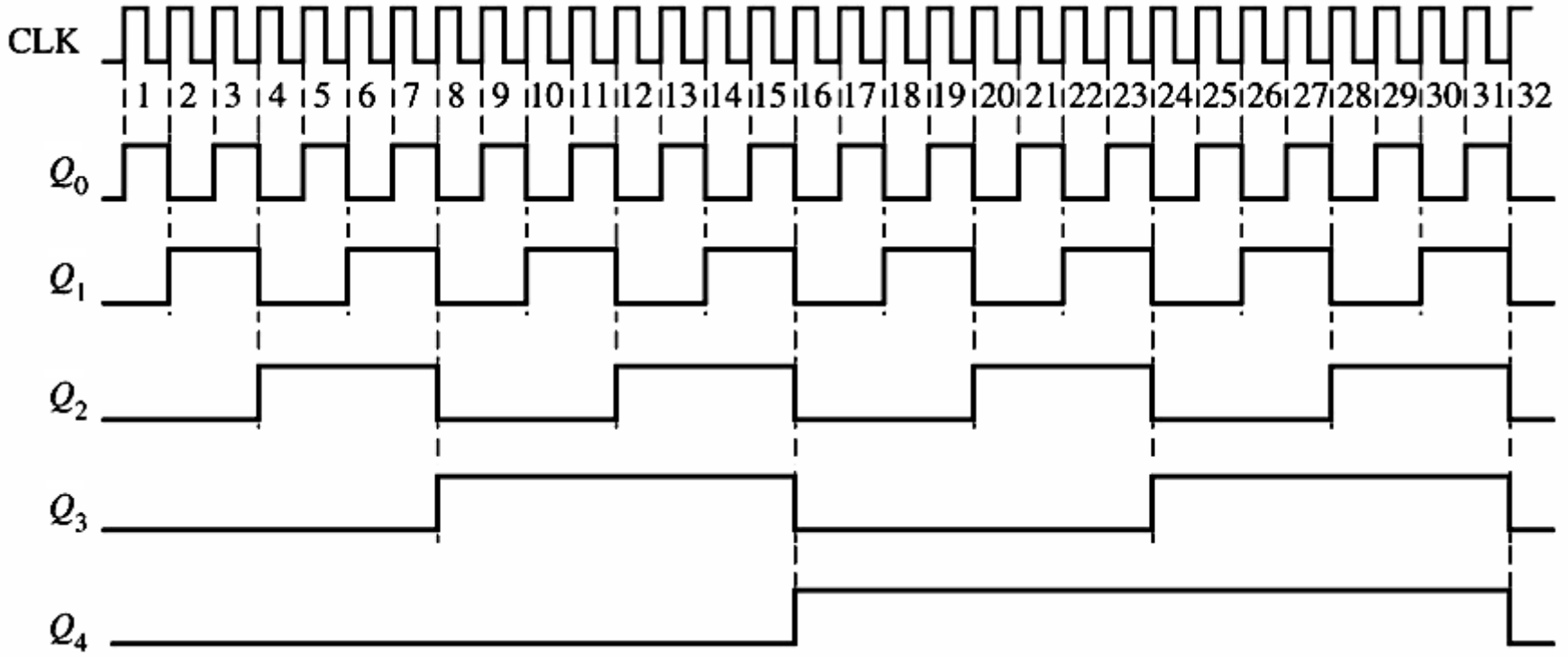
- Cascaded Counters
- Counter Decoding
- Counter Applications

Cascaded Counters

- **Cascading** means that the output of one counter drives the input of the next counter.
- Counters can be cascaded to achieve higher-modulus operation.



Cascaded Counters

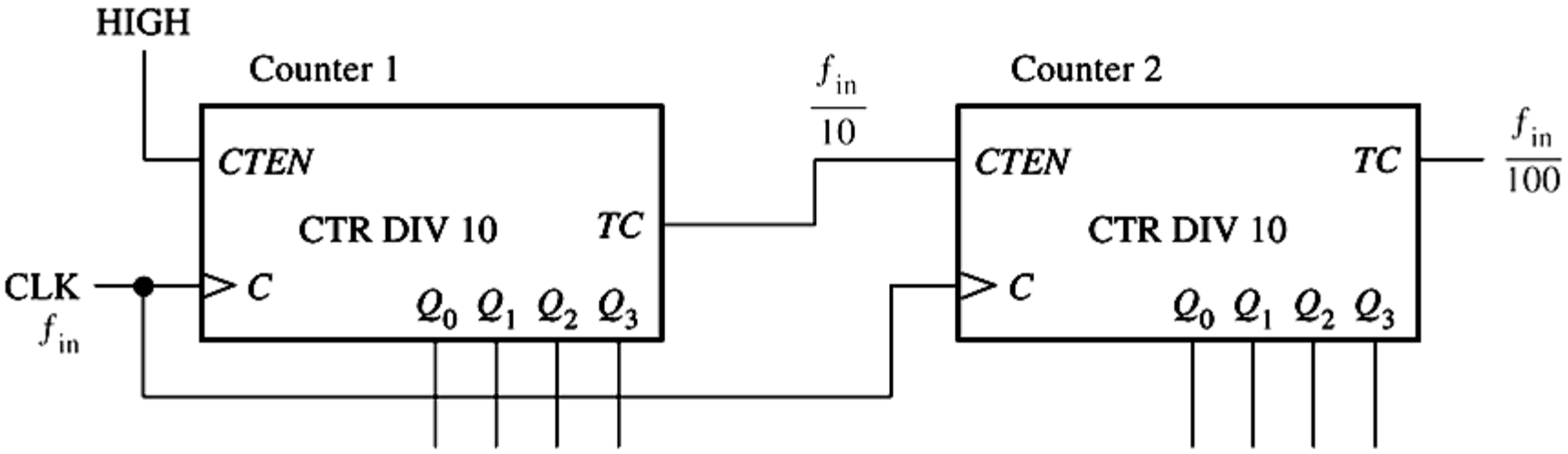


- The overall modulus of cascaded counters equals to the product of the individual moduli.

Cascaded Counters

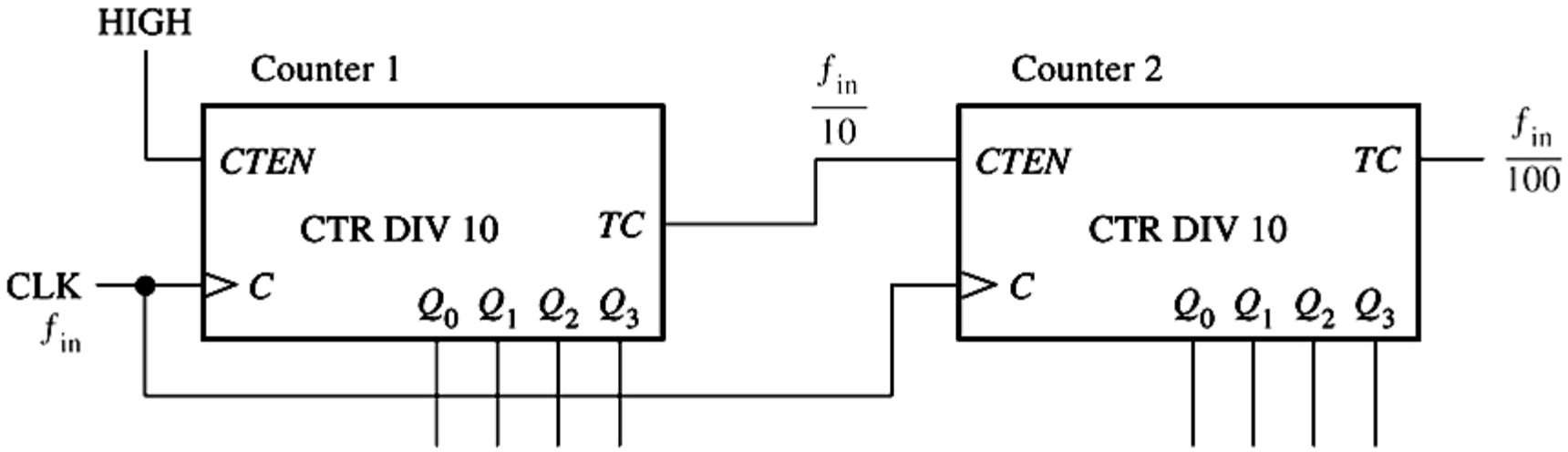
For IC synchronous counters

- The count enable (CTEN) of counter 1 is HIGH.
- The terminal count (TC) output of counter 1 is connected to CTEN of counter 2.



Cascaded Counters

- At first, TC = LOW, only counter 1 counts.
- When counter 1 reaches its terminal count 9, TC = HIGH, which enables counter 2 to increment at the rising edge of the next CLK.
- Then counter 1 is cleared and TC becomes LOW.



Cascaded Counters

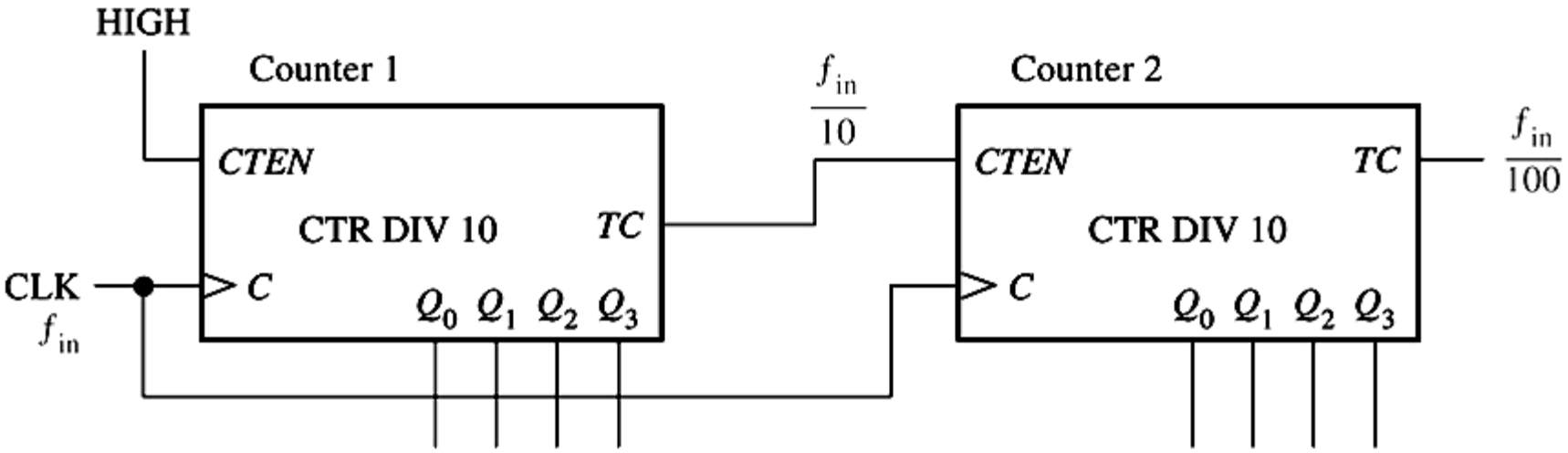
00 TC1=0

01

.....

09 TC1=1

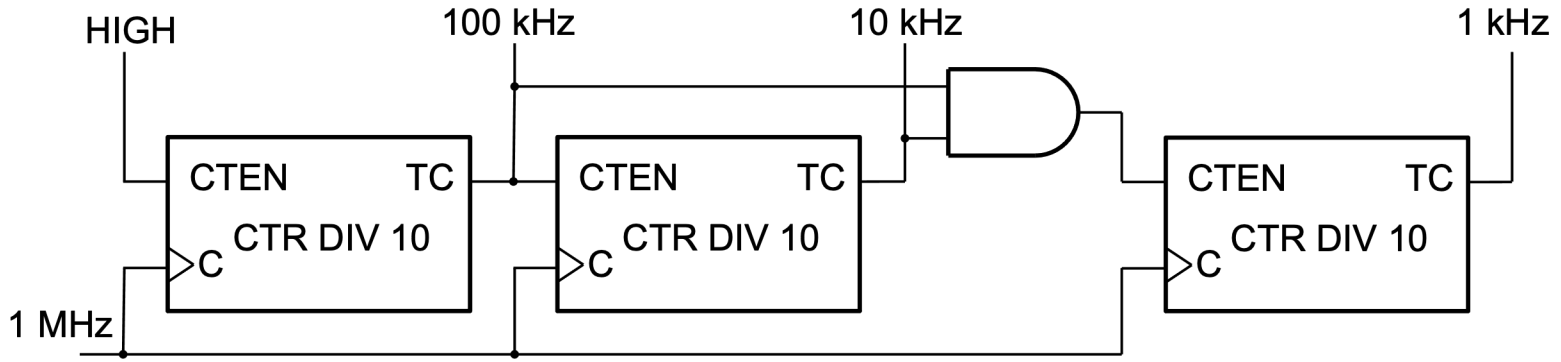
10 TC1=0



Cascaded Counters

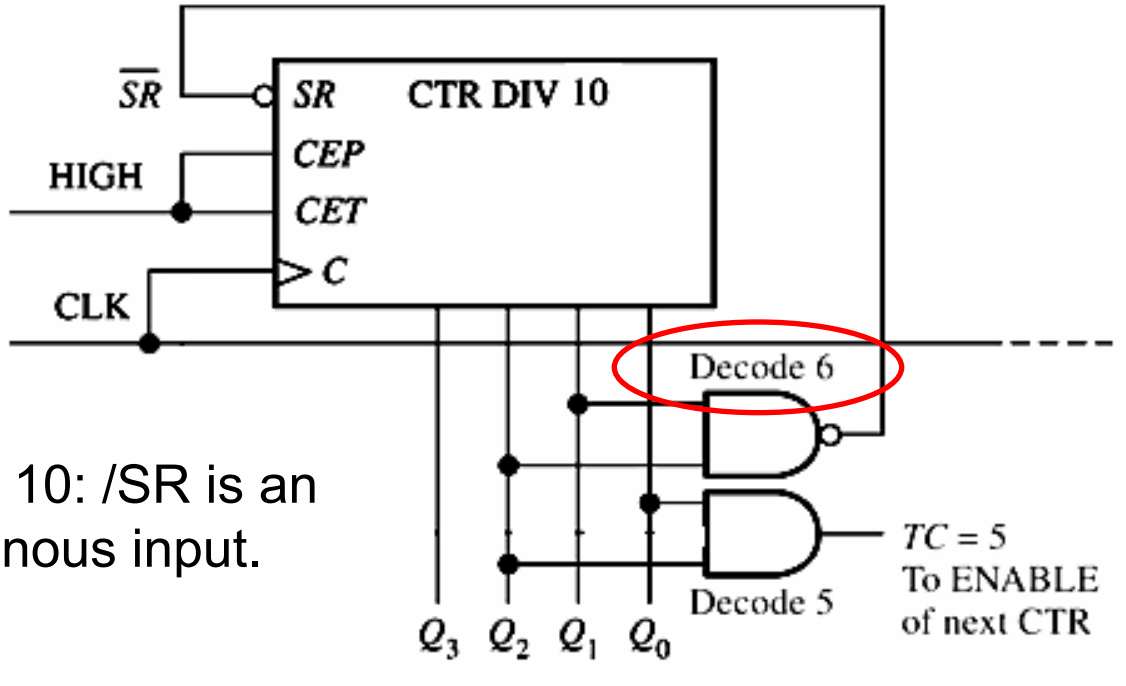
Cascaded counters can be used as

- A higher-modulus counter
- A frequency divider – to generate a lower-frenquency and synchronized clock.



Cascaded Counters

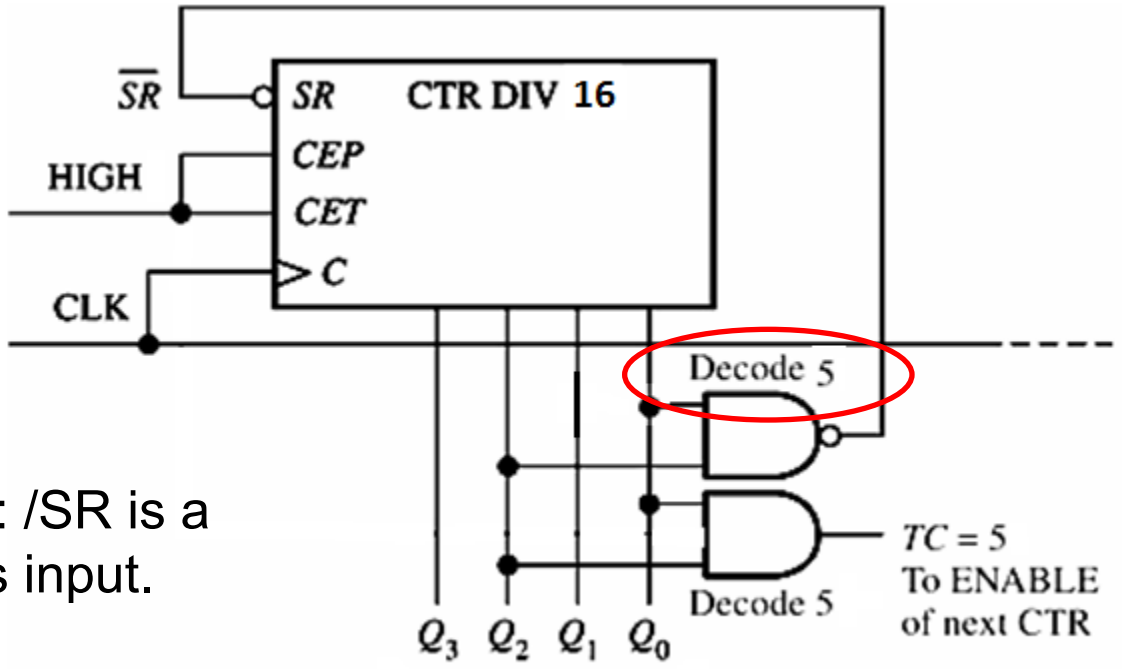
Truncated sequences can be realized by *decoding the terminal count and then clearing the counters*, e.g. a divide-by-6 counter



CTR DIV 10: /SR is an asynchronous input.

Cascaded Counters

Truncated sequences can be realized by *decoding the terminal count and then clearing the counters*, e.g. a divide-by-6 counter

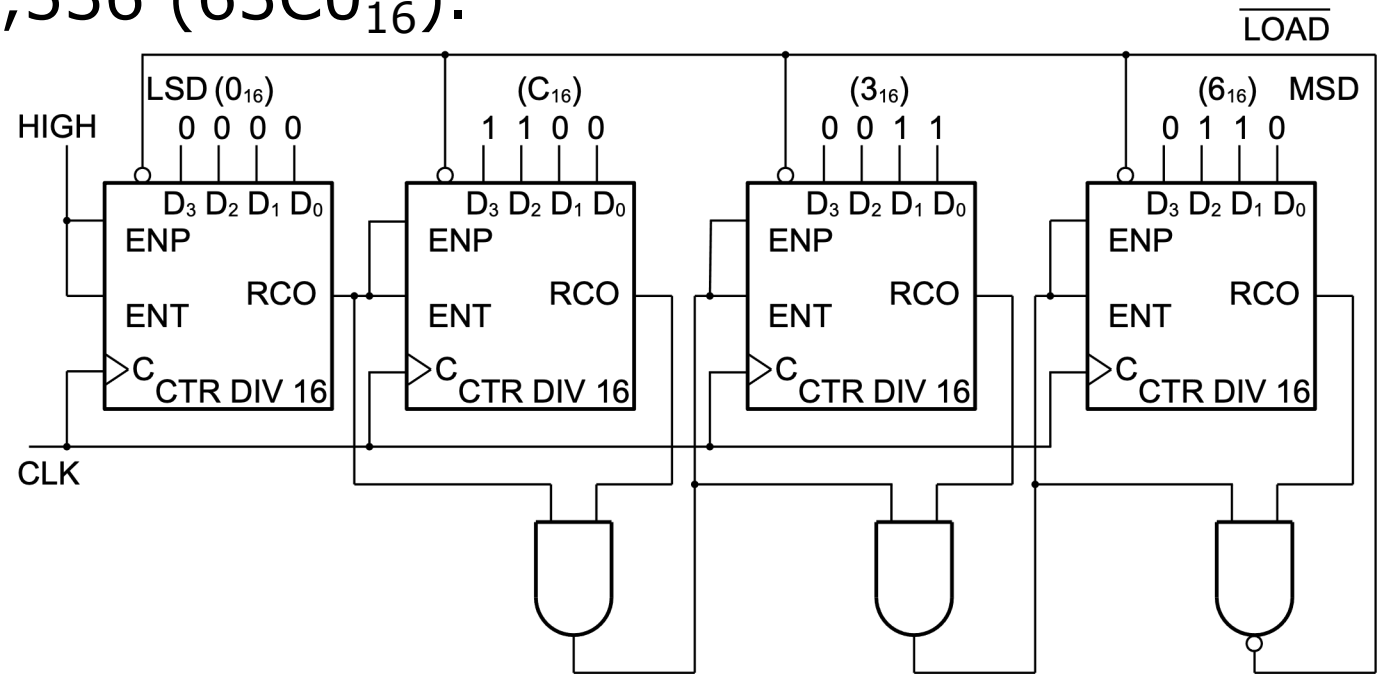


CTR DIV 16: /SR is a synchronous input.

Cascaded Counters

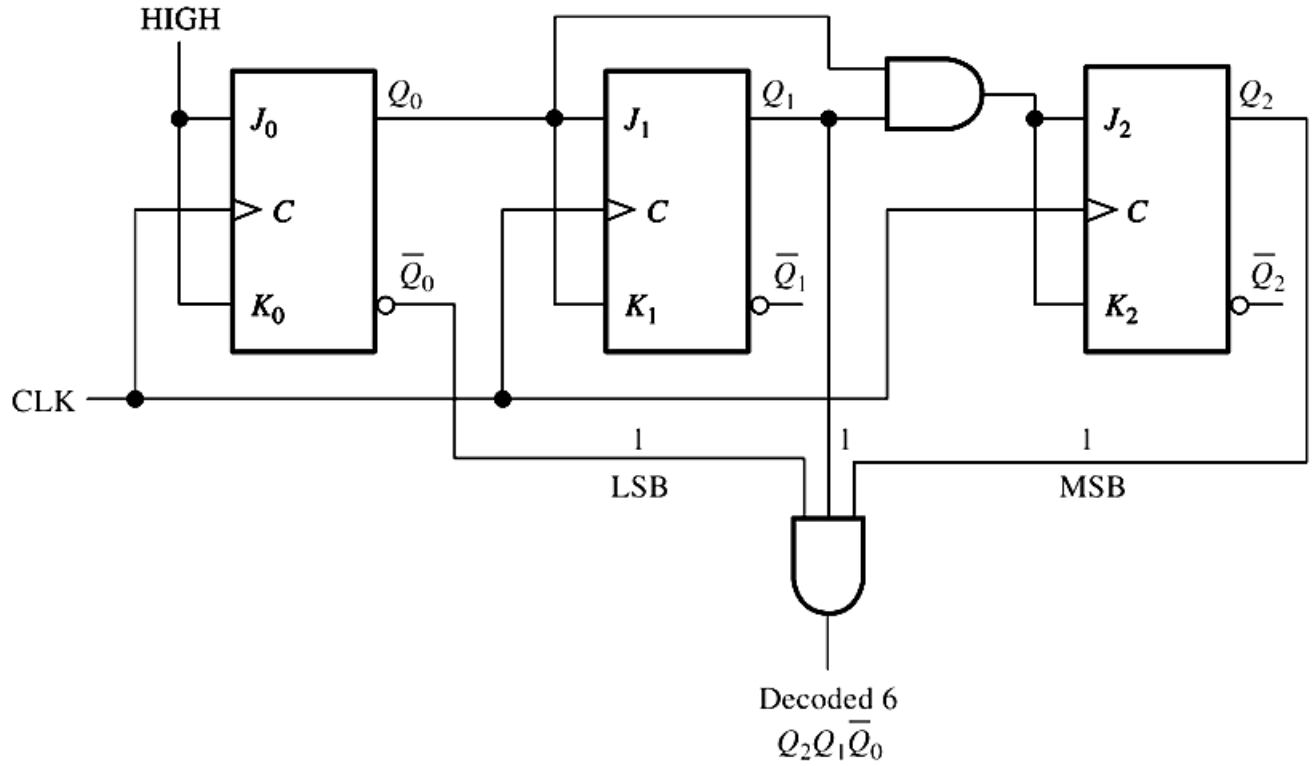
Truncated sequences can also be realized by *loading an initial count at the terminal count*.

E.g. in a divide-by-40,000 counter, at the last count 65,535, output is HIGH, which loads a count 25,536 ($63C0_{16}$).



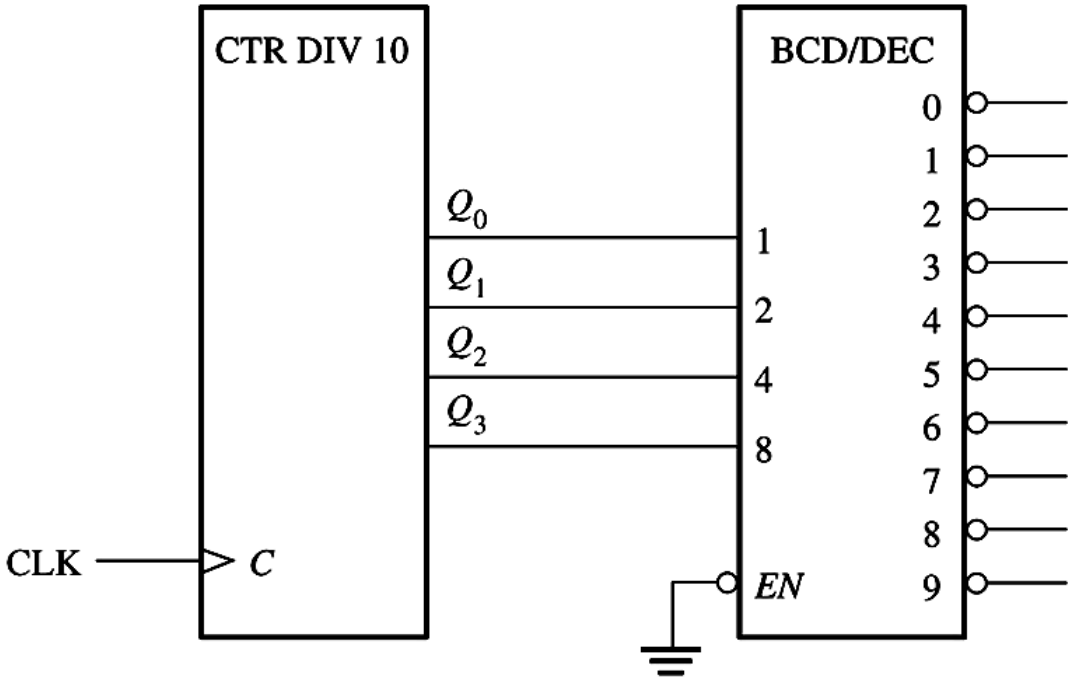
Counter Decoding

The *decoding of a counter* is to determine when a certain state appears in the sequence, e.g to decode state 6 (110).

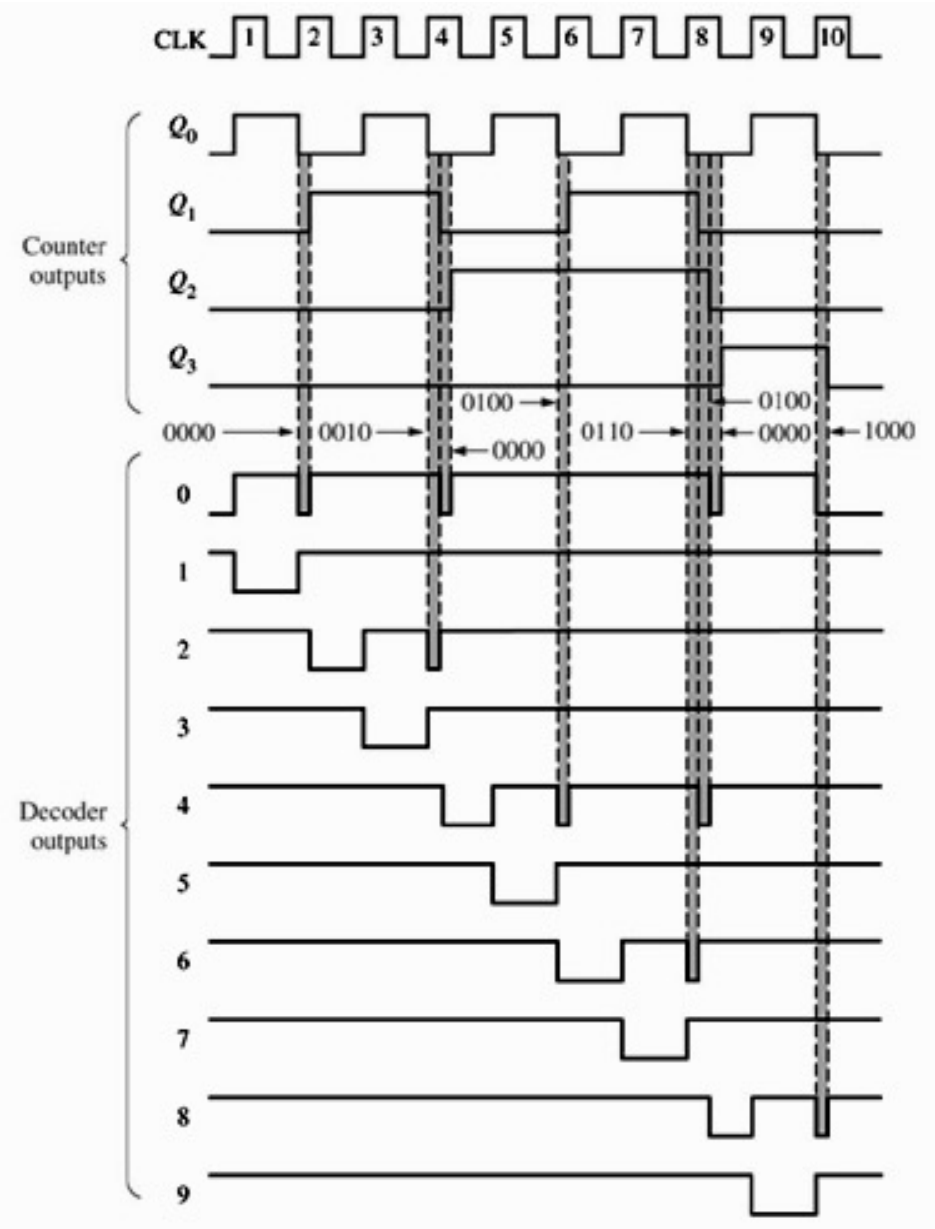


Counter Decoding

- In an asynchronous counter, the propagation delays create transitional states.
- They produce glitches on the output of the decoder.

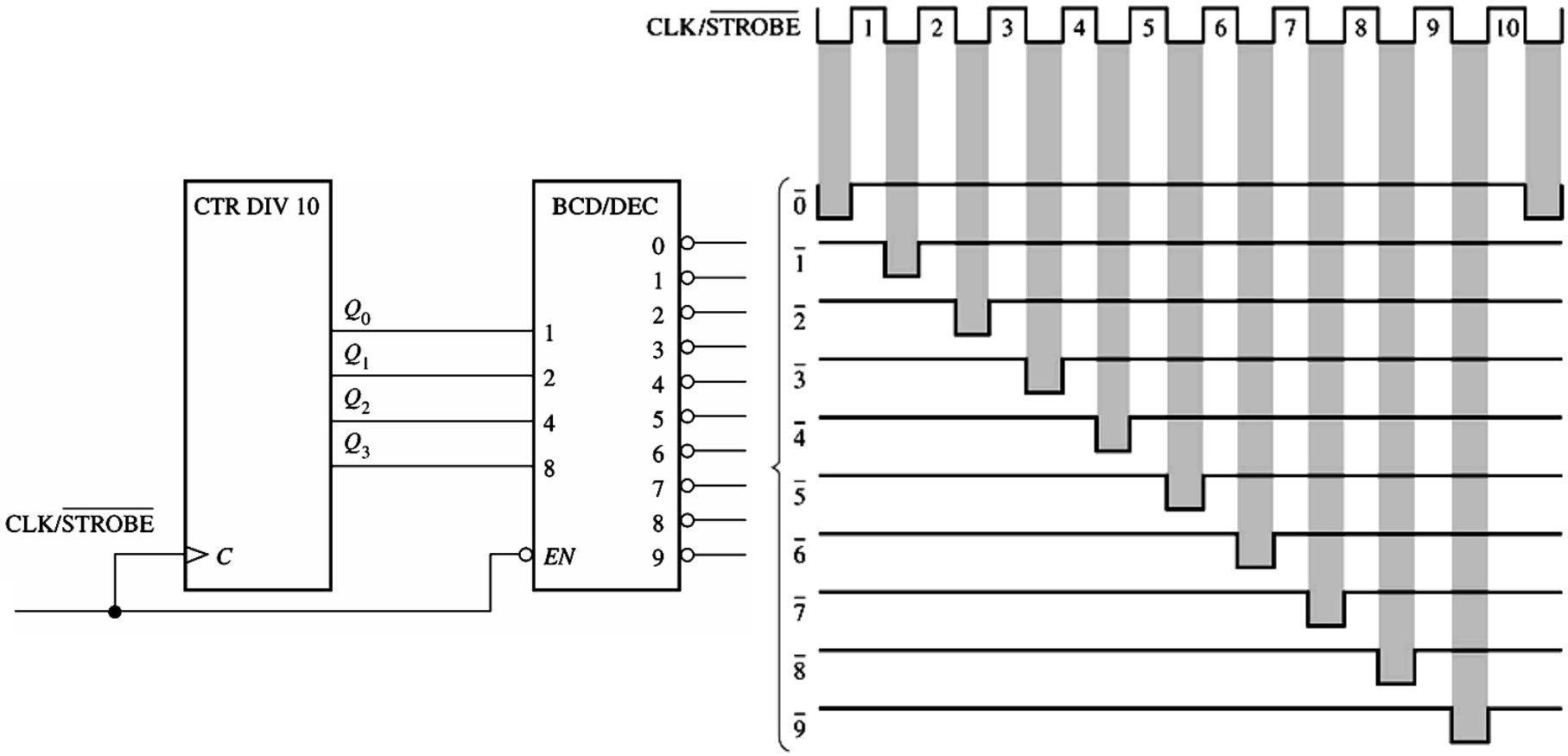


Counter Decoding

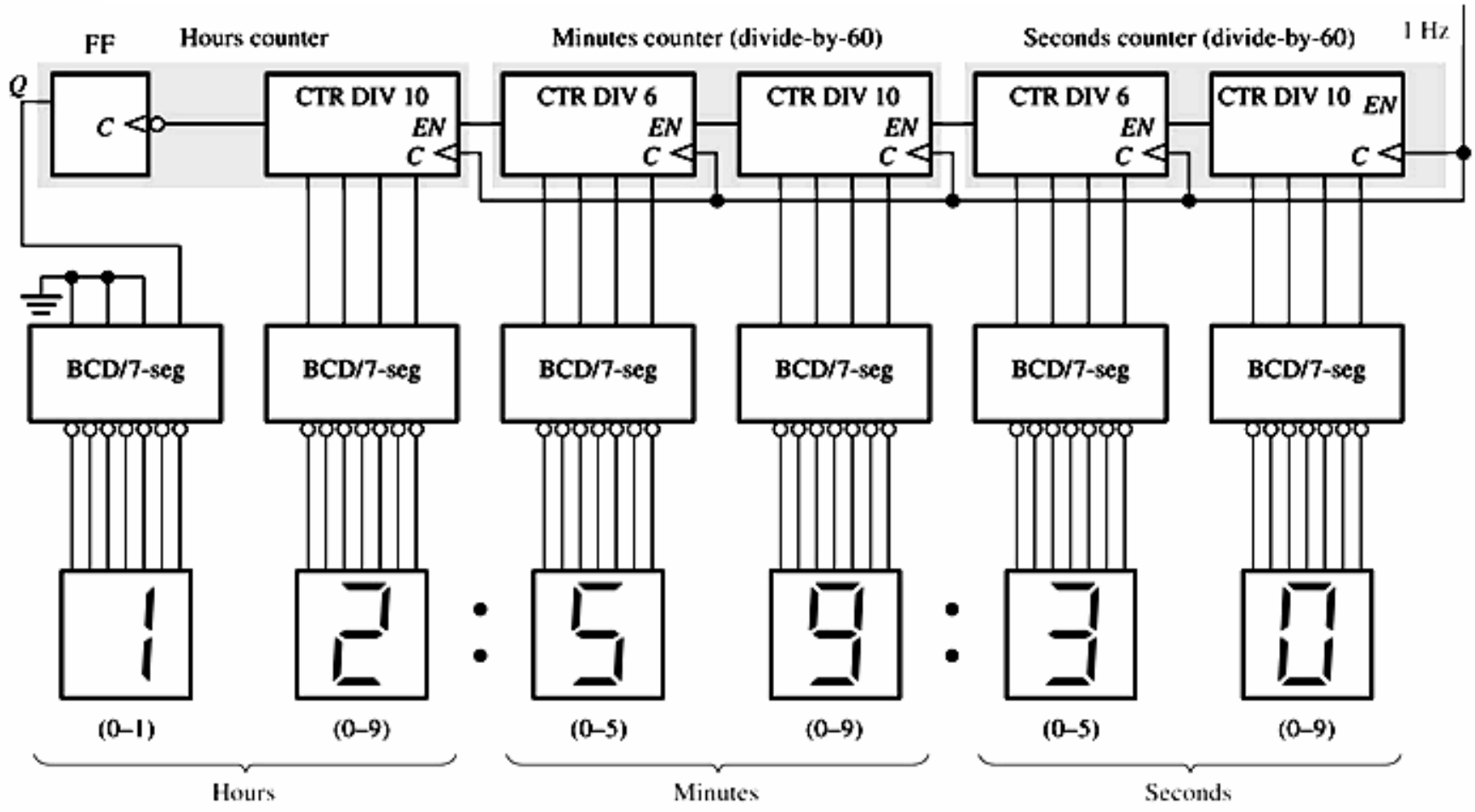


Counter Decoding

- A remedy is to enable the decoded outputs after the transitional states.

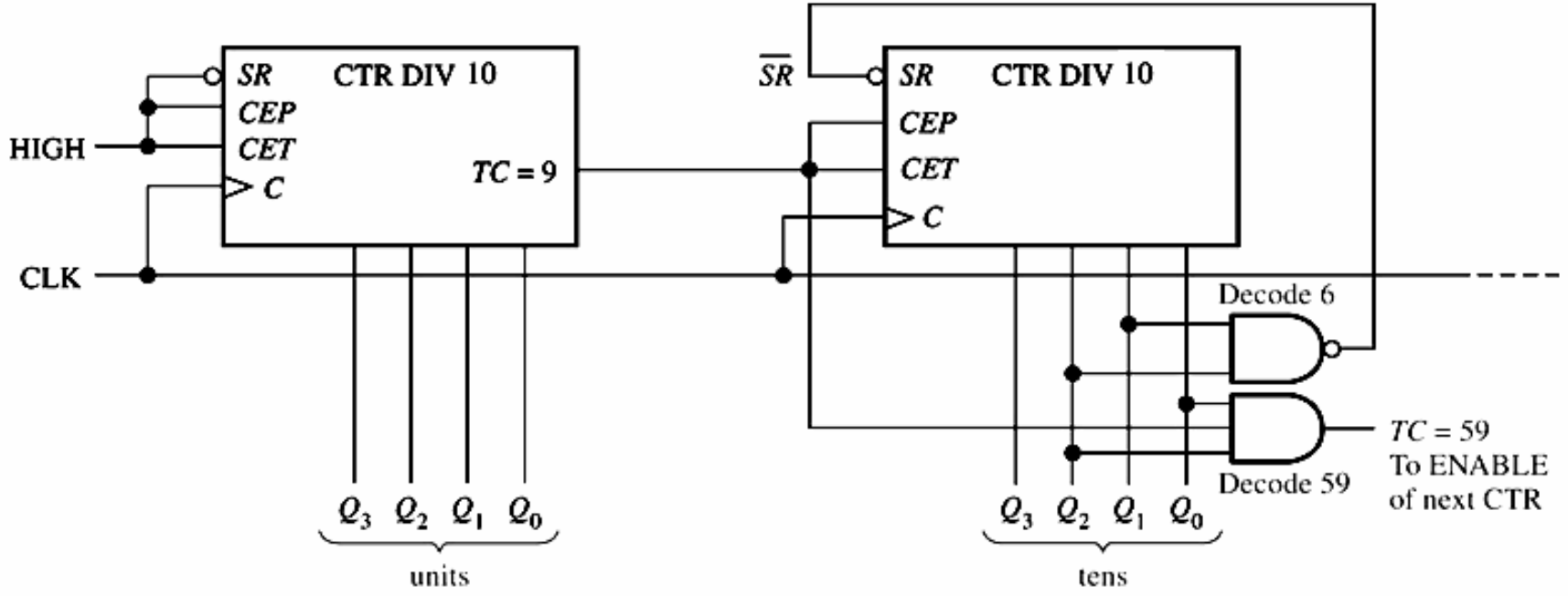


Counter Applications – Digital Clock

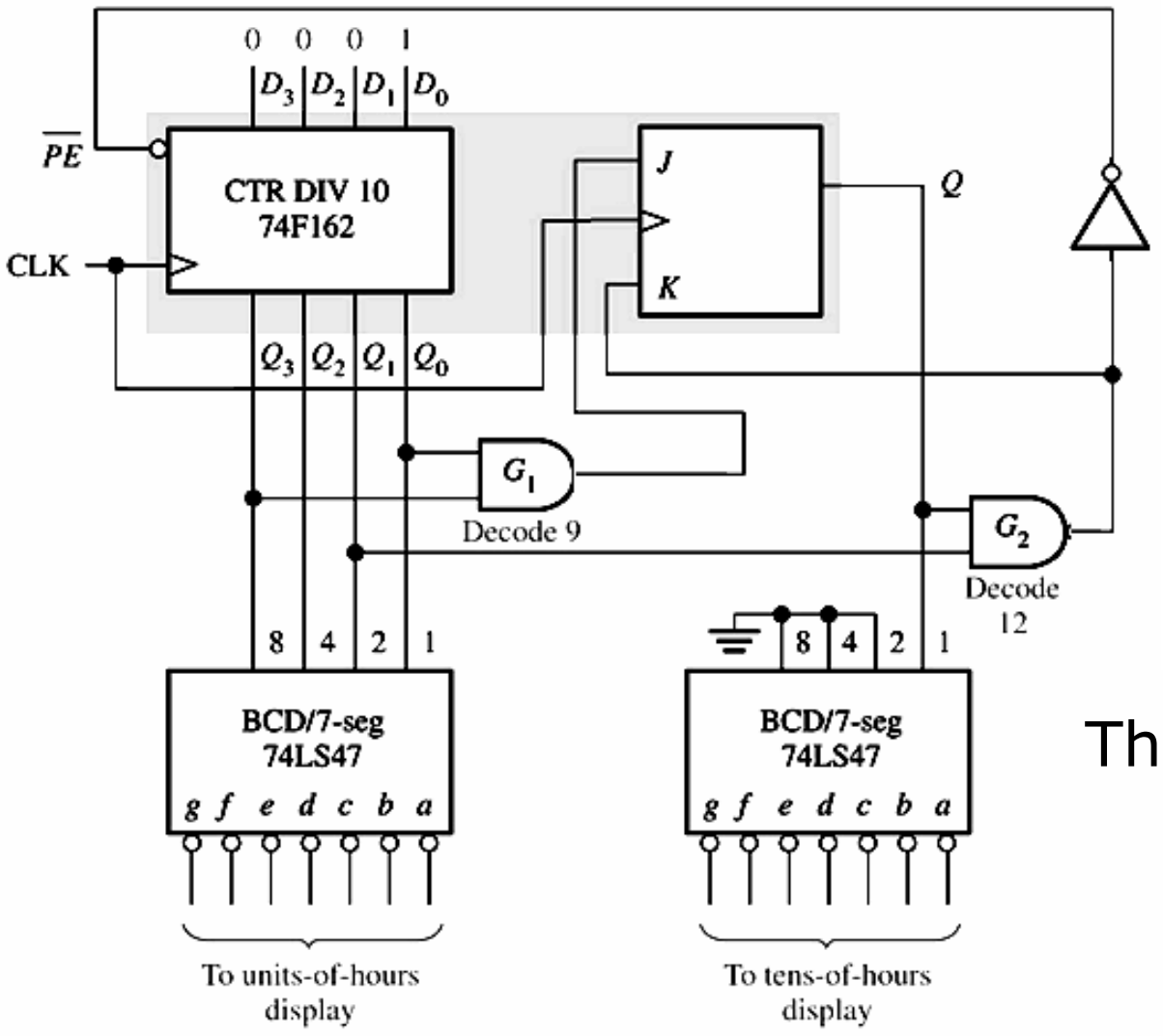


Counter Applications – Digital Clock

The *seconds* and *minutes* counters: divide-by-60 counters



Counter Applications – Digital Clock



00 J=0, K=0
01
……
09 J=1, K=0
10 J=0, K=0
11
12 J=0, K=1, /PE=0
01 J=0, K=0
……

The hours counters