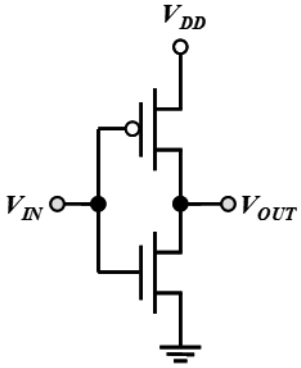
Homework 2 on Silicon CMOS Logic Circuits & Layout

in the module

EEE201 CMOS Digital Integrated Circuits

1. In the following CMOS inverter logic gate, assume the transistor size of $(W/L)_n$ = 0.8μm/0.20μm and $(W/L)_p$ = 1.6μm/0.20μm and V_{DD} = 3.0 V.



(a). Determine the operation modes (e.g. cut-off, linear or saturation) of the NMOS and PMOS transistors respectively at V_{in} = 0.2 V, 0.9 V, 1.5 V, 2.1 V, and 2.8 V. Using a table to list the operation modes is recommended. (Note: You may need to do multiple calculations for the data point V_{in} = 1.5 V with V_{in} = 1.4 V or 1.6 V).

(b). Using the tabulated results in (a) or otherwise, determine the current flowing through both the NMOS and PMOS transistors at the different input voltage V_{in} in (a).

(c). Using *Matlab* or *Excel*, plot a graph of the current against the input voltage V_{in}.

(d). Using the above results in (a) and (b) or otherwise, determine the output voltage V_{out} at the different input voltage V_{in} in (a).

(e). Using *Matlab* or *Excel*, plot a graph of the **voltage transfer characteristics** (**VTC**) (i.e. output voltage V_{out} versus input voltage V_{in}) of the CMOS inverter with the five sets of data points obtained.

It is given that the **threshold voltage** $\boldsymbol{V_{Ton}}$ = 0.50 V and $\boldsymbol{\mu_n C_{ox}}$ = 430 μA/V² for the NMOS transistor while $\boldsymbol{V_{Top}}$ = -0.50 V and $\boldsymbol{\mu_p C_{ox}}$ = 210 μA/V² for the PMOS transistor. Assume the long-channel approximation of the MOSFET and there is no body effect (i.e. the body terminal of the MOSFETs are properly connected respectively to ground and V_{DD}).

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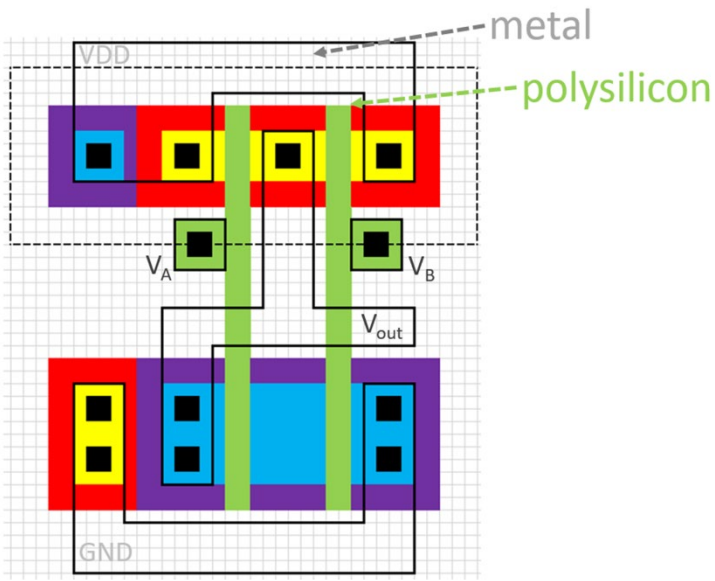
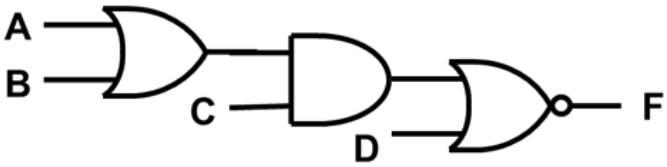
2. The drawn mask layout of a CMOS logic gate is shown below. Assume a *p*-type silicon substrate.



(a). Draw the schematic diagram of the CMOS transistor circuit using standard circuit symbols. Make sure that all the terminals of the transistors and the circuits are clearly labeled.

(b). Using the scalable CMOS layout design rules or also called λ layout design rules, determine the transistor size (i.e. W/L) of each transistor of the logic circuit.

3. The logic gate schematic of a digital circuit is shown below.



Draw the schematic diagram of the logic circuit of CMOS implementation (i.e. using PMOS and NMOS transistors in the complementary way to minimise the static power dissipation) with the smallest possible number of transistors. You must use standard circuit symbols.

4. The schematic circuit diagram (on the left) and cross-sectional structure (on the right) of a **dynamic random access memory** (**DRAM**) unit cell is shown below.

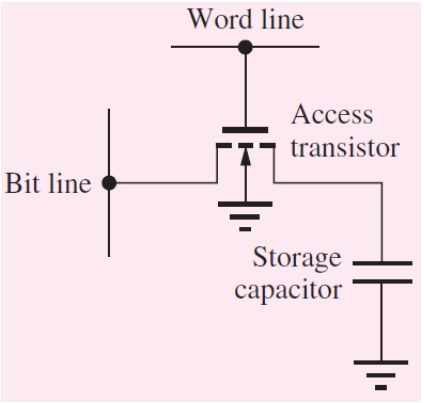
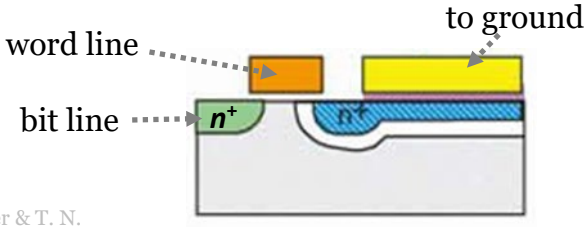


Image from: R. C. Jaeger & T. N. Blalock, *Microelectronic Circuit Design*, 4e, © 2010 McGraw-Hill, USA.

Image Source: DailyTech; available at: https://electronics.stackexchange.com/questions/306002/why-does-a-dram-cell-necessarily-contain-a-capacitor.



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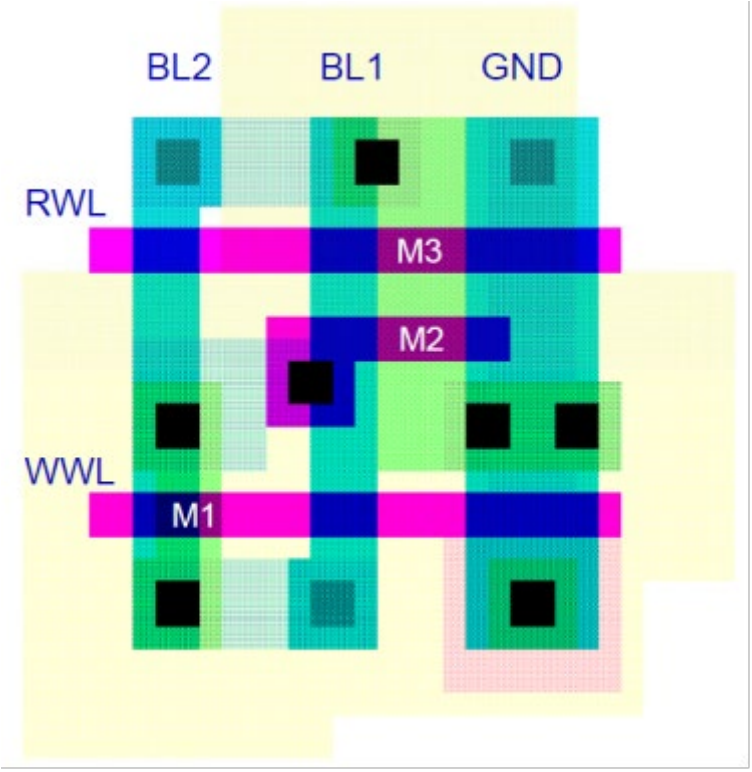
(a). If the **storage capacitor** is implemented using a **MOS capacitor** (as shown in the cross-sectional structure above) of the smallest possible size according to the λ-layout design rules for an n-channel MOS transistor, sketch the layout of the **DRAM cell**.

(b). Instead of using only one transistor for the implementation of a DRAM cell, three transistors can be used for an improved implementation. The IC layout of a three-transistor (3T) DRAM cell is shown below. Sketch the schematic circuit diagram of such a 3T DRAM cell. Proper labels must be included. Hint: The 3T DRAM cell is similar to the 1T implementation but with additional transistors and signal connections.



The annotations in the above layout are: BL1 as bit line 1, BL1 as bit line 2, RWL as read word line, WWL as write word line, M1 as MOSFET1, M2 as MOSFET2, and M3 as MOSFET3.

Note: In all the calculations, please show your steps clearly. When you find the values of some material parameters (not provided in the questions), please cite the source(s) explicitly as a footnote or include a section of references at the end. If it is necessary, make approximations in your calculations but state clearly the approximations you make.

***Optional* Extra Questions**

5. The CMOS logic inverter in Q1 can be implemented with different transistor sizes, in particular the channel width W while the channel length L should remain the same as the minimum feature size (2λ in the scalable CMOS layout design rules).

(a). If PMOS transistor in Q1 has $(W/L)_p$ = 16μm/0.20μm, determine the output voltage V_{out} when V_{in} = 0.2 V, 0.9 V, 1.5 V, 2.1 V, and 2.8 V.

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(b). If PMOS transistor in Q1 has $(W/L)_p$ = 0.8μm/0.20μm, the same as that of the NMOS transistor in Q1, determine the output voltage V_{out} when V_{in} = 0.2 V, 0.9 V, 1.5 V, 2.1 V, and 2.8 V.

(c). Using *Matlab* or *Excel*, plot a graph of the **voltage transfer characteristics** (**VTC**) of the CMOS inverters in Q5(a), Q5(b) and Q1 using the data obtained. What shifting trend do you see by comparing the three curves?

(d). With the PMOS transistor sizes $(W/L)_p$ = 16μm/0.20μm in Q5(a), determine the current flowing through both the NMOS and PMOS transistors when V_{in} = 0.2 V, 0.9 V, 1.5 V, 2.1 V, and 2.8 V.

(e). With the PMOS transistor sizes $(W/L)_p$ = 0.8μm/0.20μm in Q5(b), determine the current flowing through both the NMOS and PMOS transistors when V_{in} = 0.2 V, 0.9 V, 1.5 V, 2.1 V, and 2.8 V.

(f). Using *Matlab* or *Excel*, plot a graph of the current against the input voltage V_{in} for the CMOS inverters in Q5(d), Q5(e) and Q1 using the data obtained. What trend of the peak current do you see by comparing the three curves?

6. If only one type of MOS transistors (usually ***n***-type MOSFETs) can be fabricated on a wafer, the logic inverter can also be implemented using two NMOS transistors.

(a). If PMOS transistor in Q1 is replaced with an NMOS transistor but with the gate and drain tied together (hence serving as an active load). The two NMOS transistors have the same $(W/L)_n$ = 0.8μm/0.20μm, determine the output voltage V_{out} when V_{in} = 0.2 V, 0.9 V, 1.5 V, 2.1 V, and 2.8 V.

(b). If NMOS transistor in Q6(a) with the gate and drain tied together has $(W/L)_n$ = 8μm/0.20μm while the other NMOS transistor keeps the $(W/L)_n$ = 0.8μm/0.20μm, determine the output voltage V_{out} when V_{in} = 0.2 V, 0.9 V, 1.5 V, 2.1 V, and 2.8 V.

(c). Using *Matlab* or *Excel*, plot a graph of the **voltage transfer characteristics** (**VTC**) of the CMOS inverters in Q6(a), Q6(b) and Q1 using the data obtained. What shifting trend do you see by comparing the three curves?

(d). Using the condition in Q6(a), determine the current flowing through both NMOS transistors when V_{in} = 0.2 V, 0.9 V, 1.5 V, 2.1 V, and 2.8 V.

(e). Using the condition in Q6(b), determine the current flowing through both the NMOS and PMOS transistors when V_{in} = 0.2 V, 0.9 V, 1.5 V, 2.1 V, and 2.8 V.

(f). Using *Matlab* or *Excel*, plot a graph of the current against the input voltage V_{in} for the NMOS inverters in Q6(d), Q6(e) and Q1 using the data obtained. What trend of the peak current do you see by comparing the three curves?

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7. In the CMOS implementation of the logic inverter, the PMOS transistor's channel width *W* can be made larger. In the implementation using two NMOS transistors, the same transistor sizes can be adopted.

(a). Using the condition in Q1, determine V_{OH}, V_{OL}, V_{IH}, and V_{IL} of the CMOS logic inverter. Hence, find out the noise margins NM_H and NM_L.

(b). Using the condition in Q5(a), determine V_{OH}, V_{OL}, V_{IH}, and V_{IL} of the CMOS logic inverter with the much larger PMOS transistor sizes. Hence, find out the noise margins NM_H and NM_L.

(c). Using the condition in Q6(a), determine V_{OH}, V_{OL}, V_{IH}, and V_{IL} of the NMOS logic inverter (which would occupy a considerably smaller chip area compared with the CMOS counterpart). Hence, find out the noise margins NM_H and NM_L.

(d). Tabulate the results of V_{OH}, V_{OL}, V_{IH}, V_{IL}, NM_H and NM_L in Q7(a), Q7(b) and Q7(c). By comparison of the results, which implementation of the logic inverter would give the behaviour closest to the ideal?

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