Lecture 8

of

EEE201

CMOS Digital Integrated Circuits

Department of Electrical & Electronic Engineering

Xi'an Jiaotong-Liverpool University (XJTLU)

Tuesday, 7th November 2023

- **Building CMOS Logic Inverter**
  - Intuitive understanding from switch model
  - transistor size determination
  - CMOS IC layout

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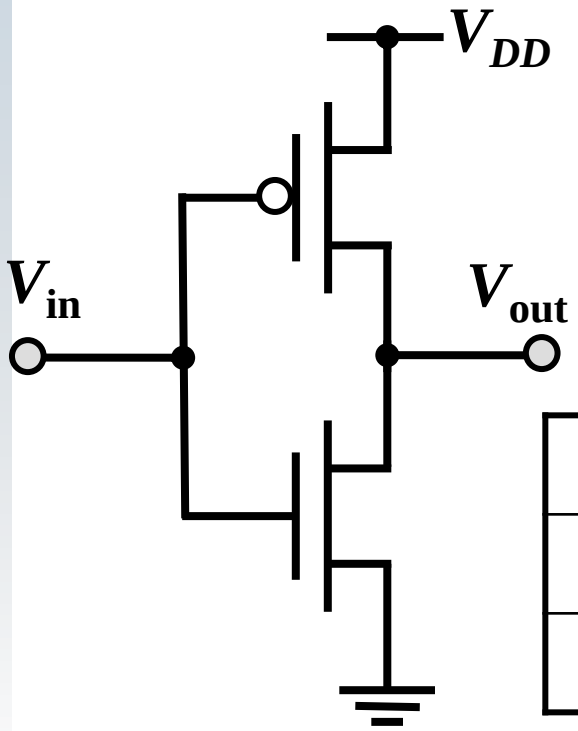
CMOS Logic Inverter

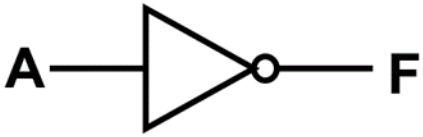
(one ***p***MOS & one ***n***MOS)

- As the very first fundamental logic gate, a **logic inverter** (i.e. NOT logic gate) can be implemented using one ***p***MOSFET stacking over one ***n***MOSFET.



- Based on the device operation of the MOSFETs, we can easily find out the input-output relationship for the logic NOT function.

V_{in}	V_{out}
0 V	V_{DD}
V_{DD}	0 V



$F = \overline{A}$

A	F
0	1
1	0

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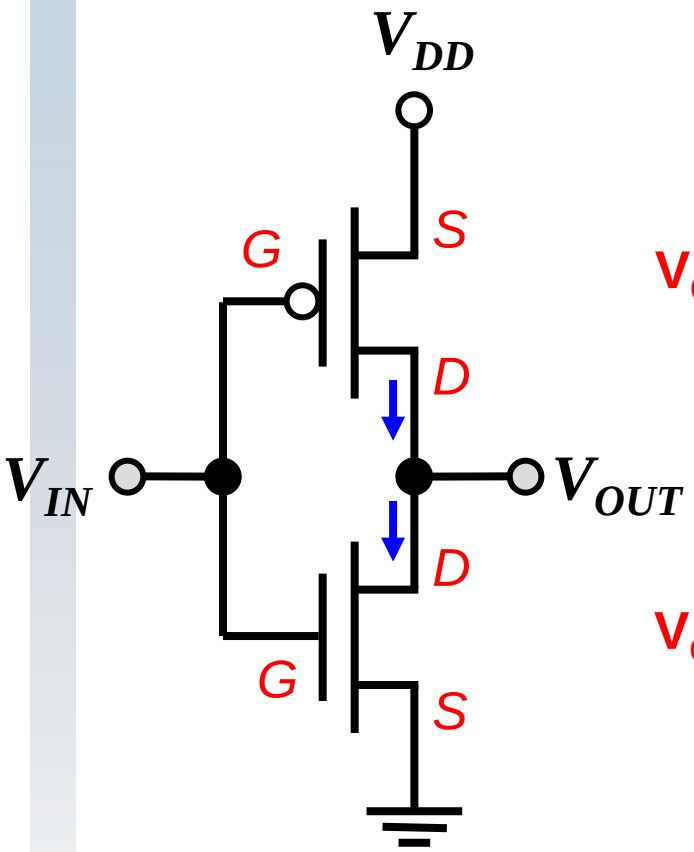
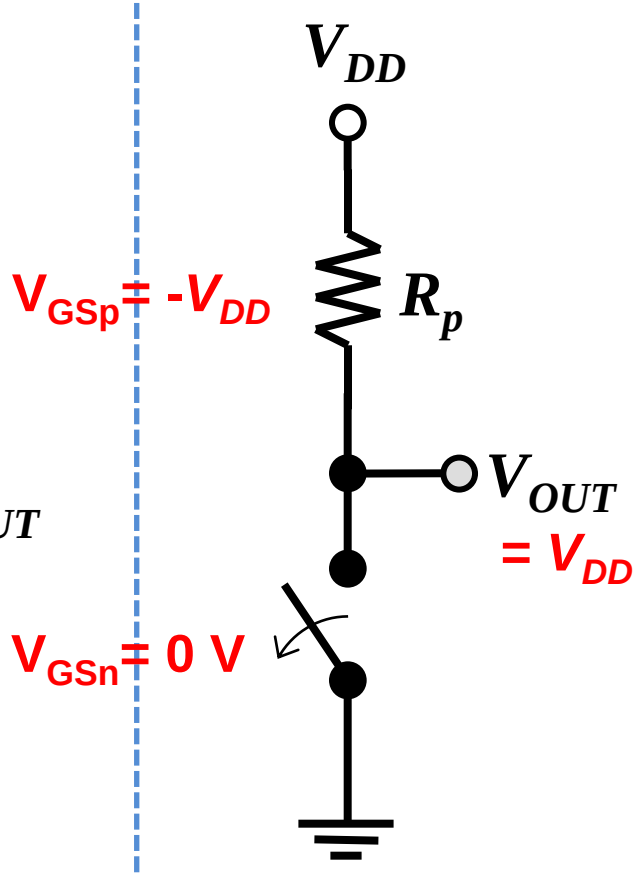
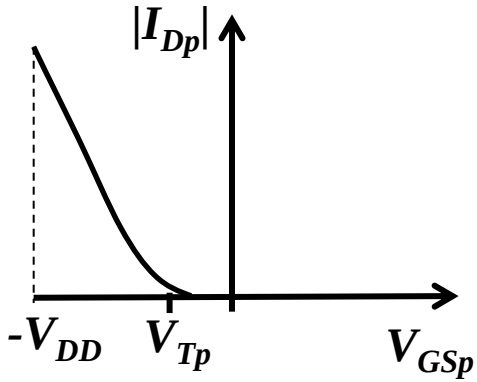
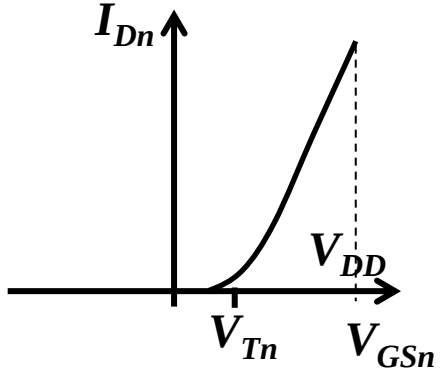
CMOS Logic Inverter - V_{in} = 0 V

(switch model for intuitive perspective)









$$V_{IN} = 0\ \text{V}$$

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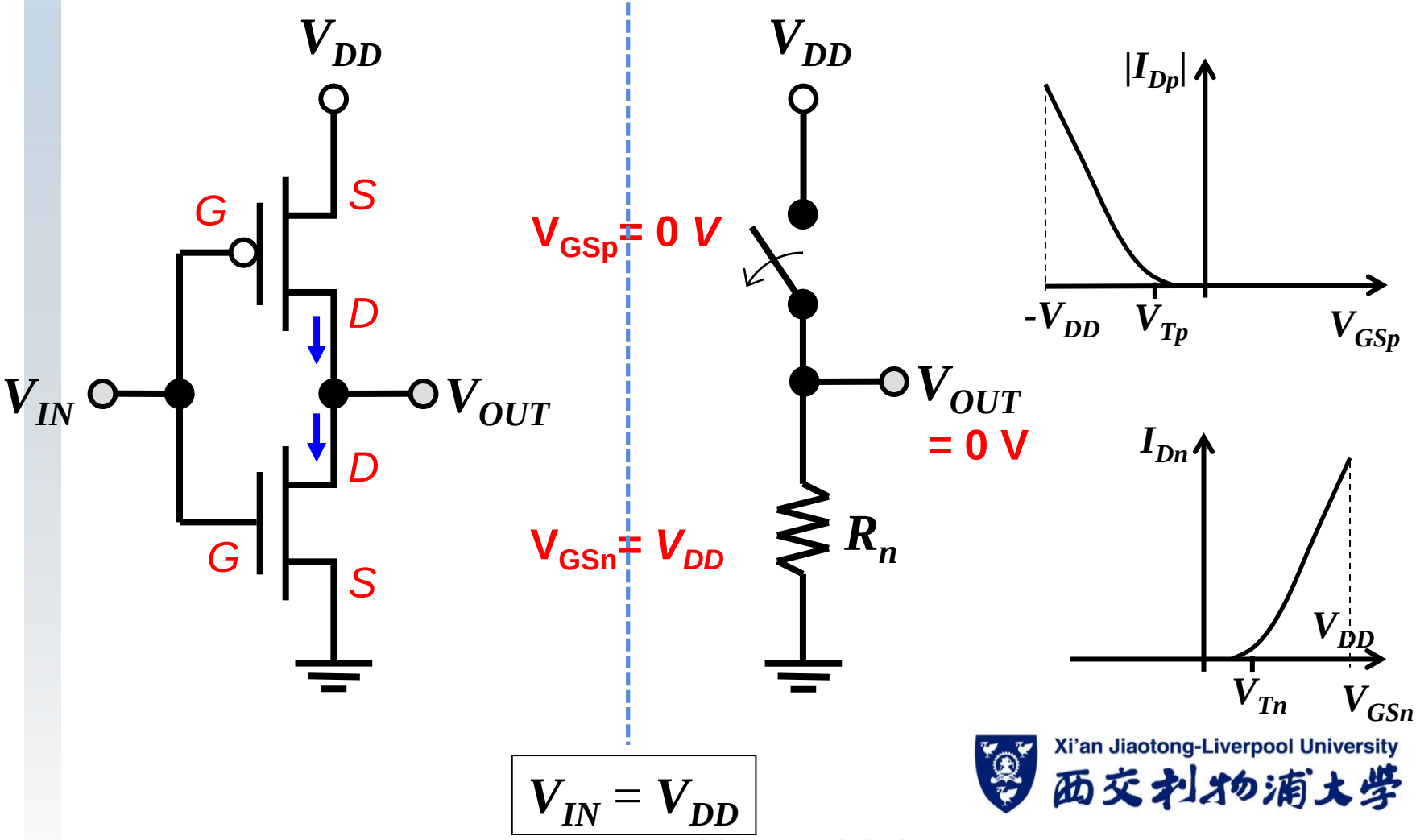
CMOS Logic Inverter - $V_{in} = V_{DD}$

(switch model for intuitive perspective)



$$V_{IN} = V_{DD}$$

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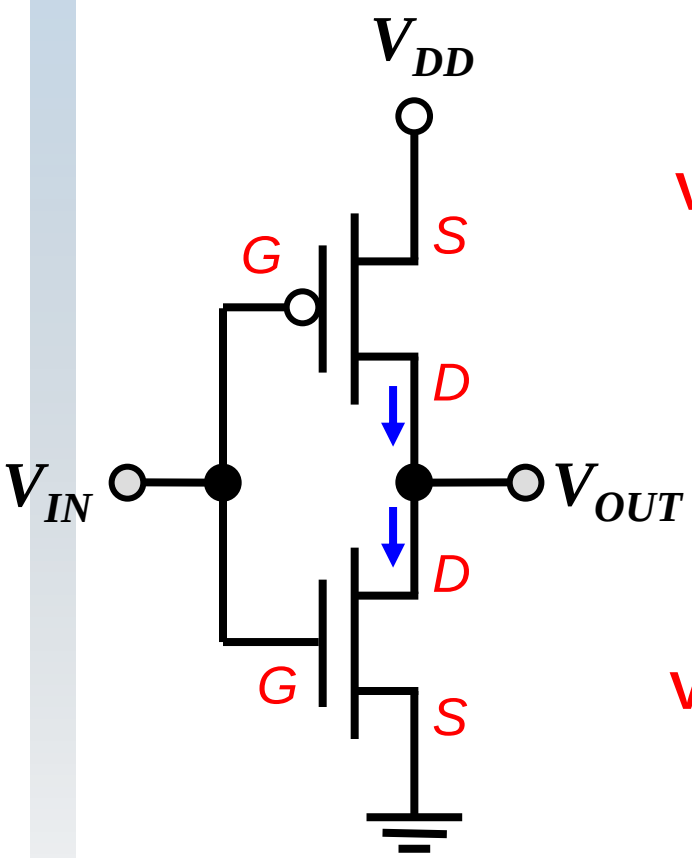
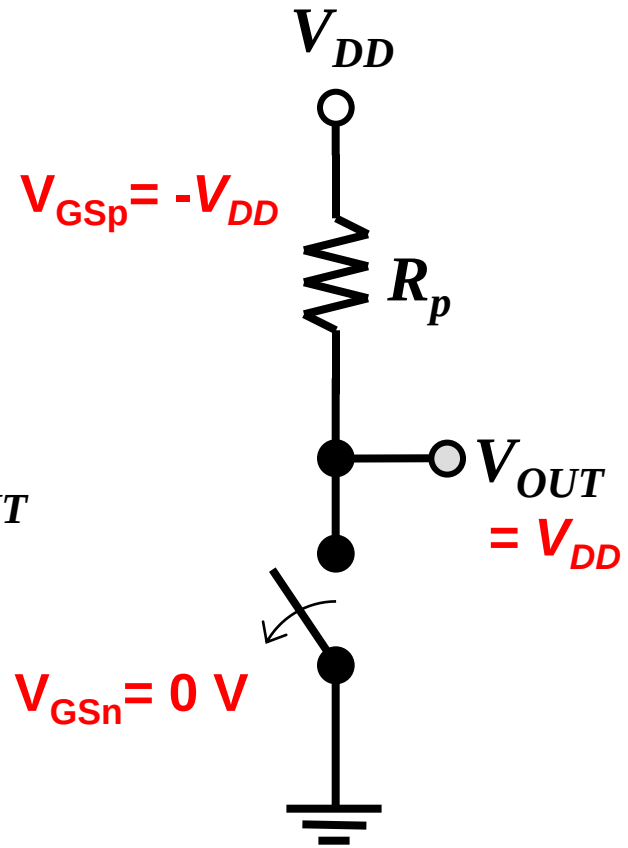
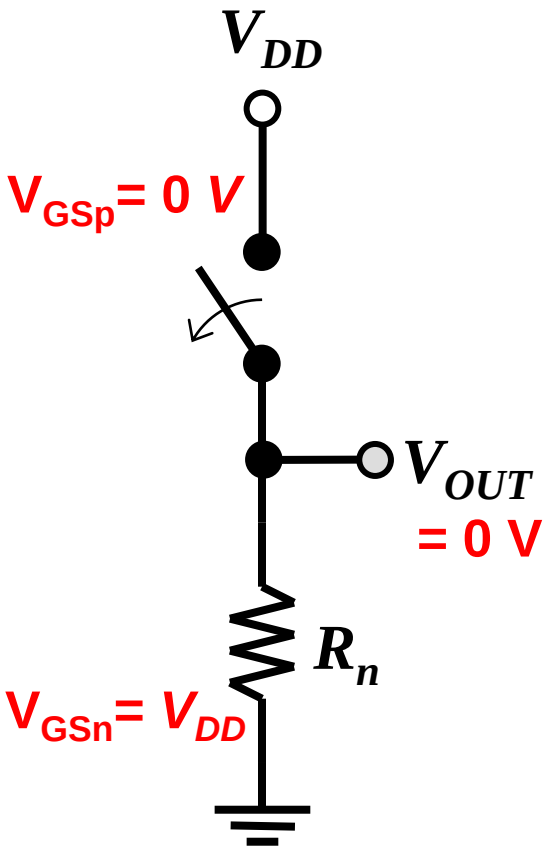
CMOS Logic Inverter

(only one switch is on in the steady state)

$V_{IN} = V_{DD}$







- Note the "zero" ***static*** **power consumption**.

$V_{IN} = 0$ V

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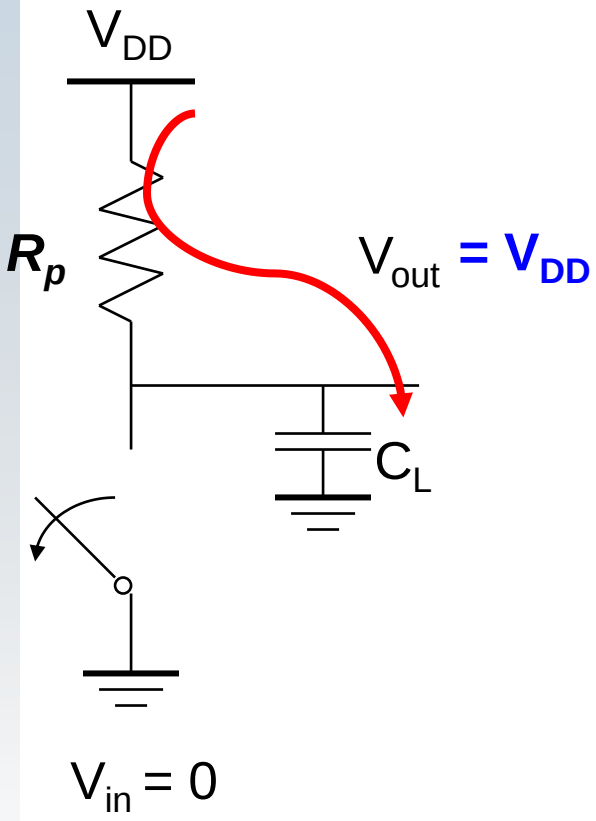
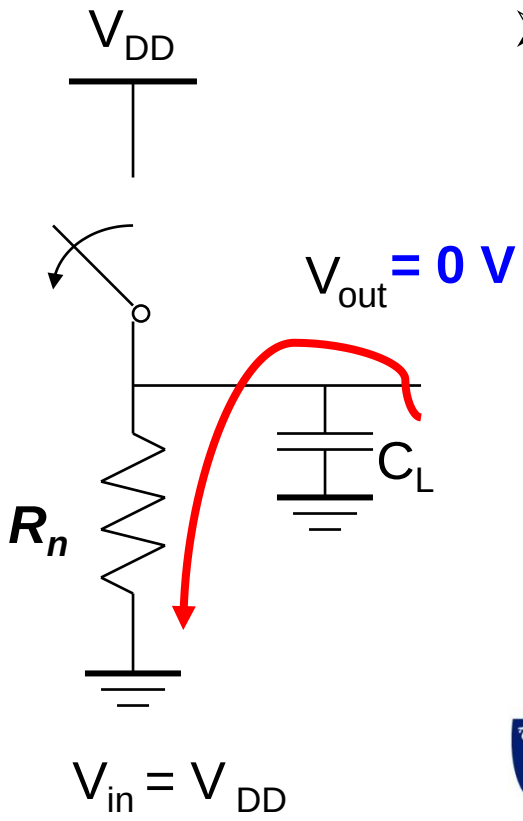
CMOS Logic Inverter

(***dynamic*** behaviour in ***charging*** & ***discharging*** capacitances)

- Since there are **capacitances** associated with the MOSFETs, there will be ***charging*** and ***discharging***.





- The logic gate response time is determined by the time to ***charge*** C_L through R_p (***discharge*** C_L through R_n).

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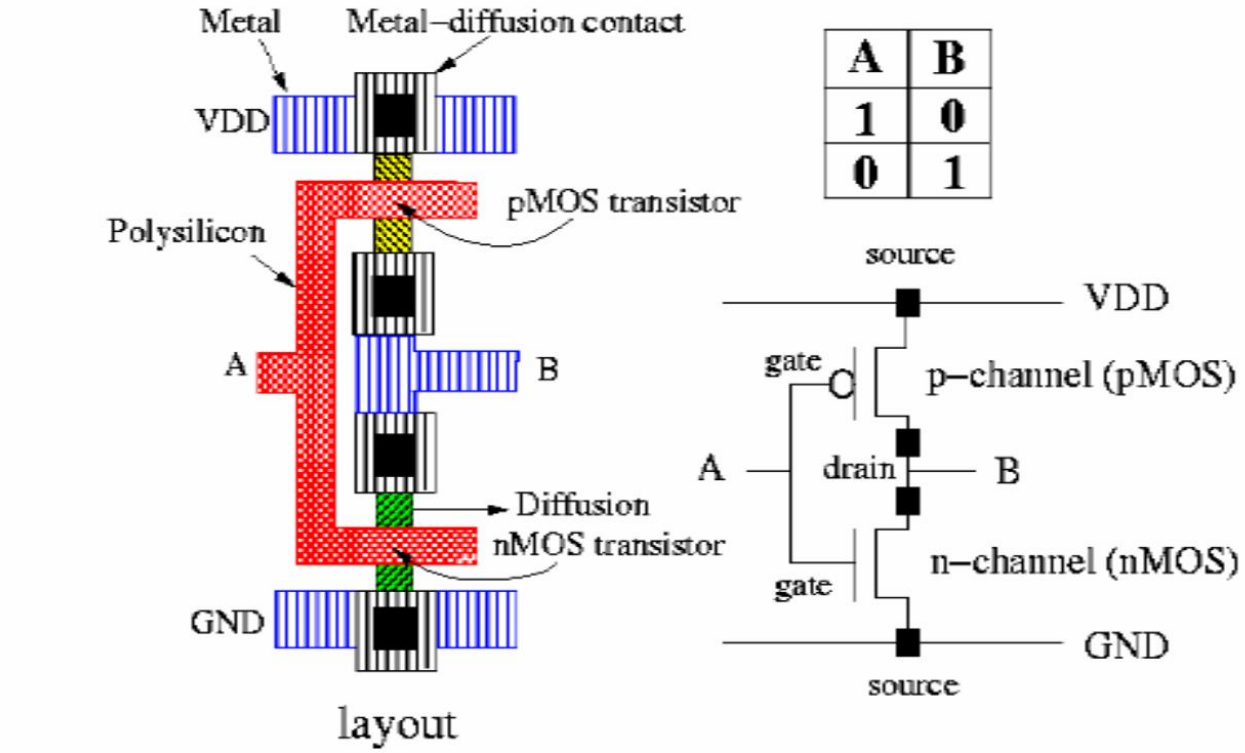
CMOS Logic Inverter – IC layout

(start from stick layout diagram)



A	B
1	0
0	1

- To design the IC layout of the logic gate, one approach is to start from the so-called stick layout.

metal 1: blue polysilicon: red p–diffusion: yellow (p–well: light yellow)

metal 2: brown contact/via: black n–diffusion: green (n–well: light green)

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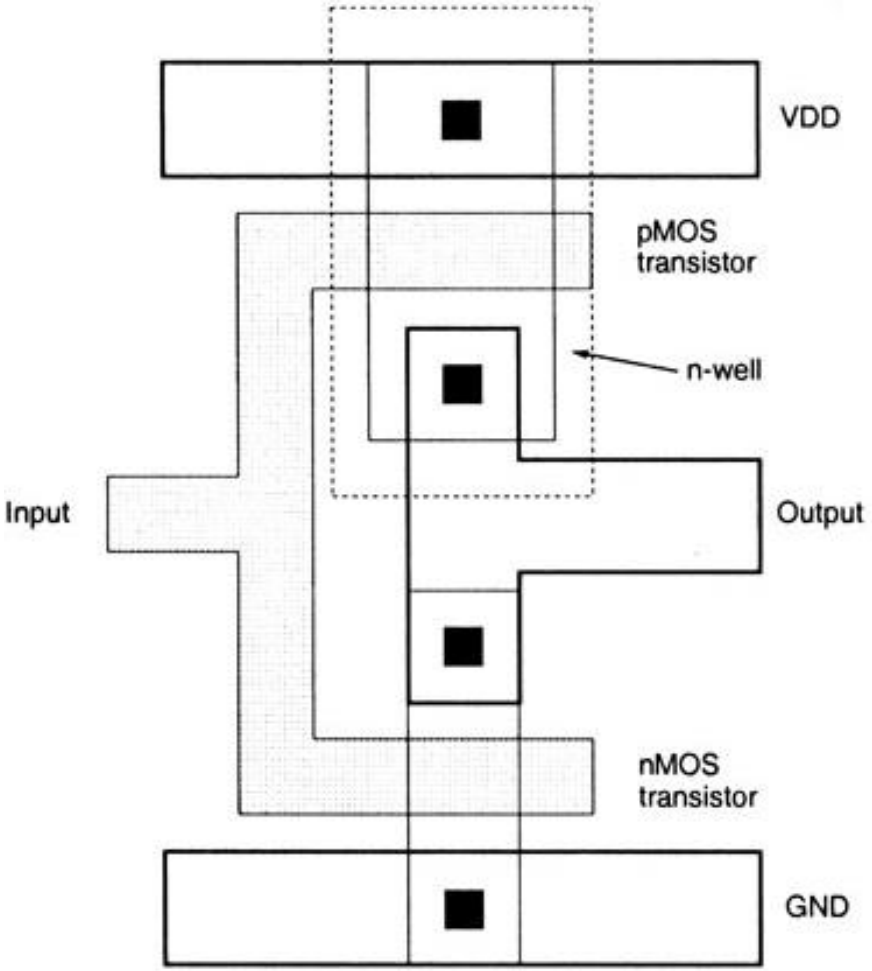
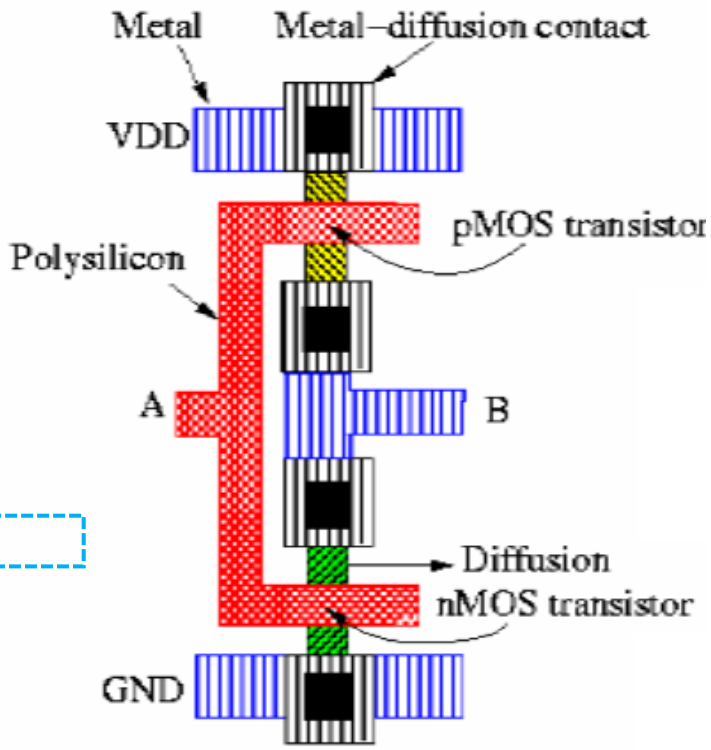
CMOS Logic Inverter – IC layout

(scratch to proper layout)





layout

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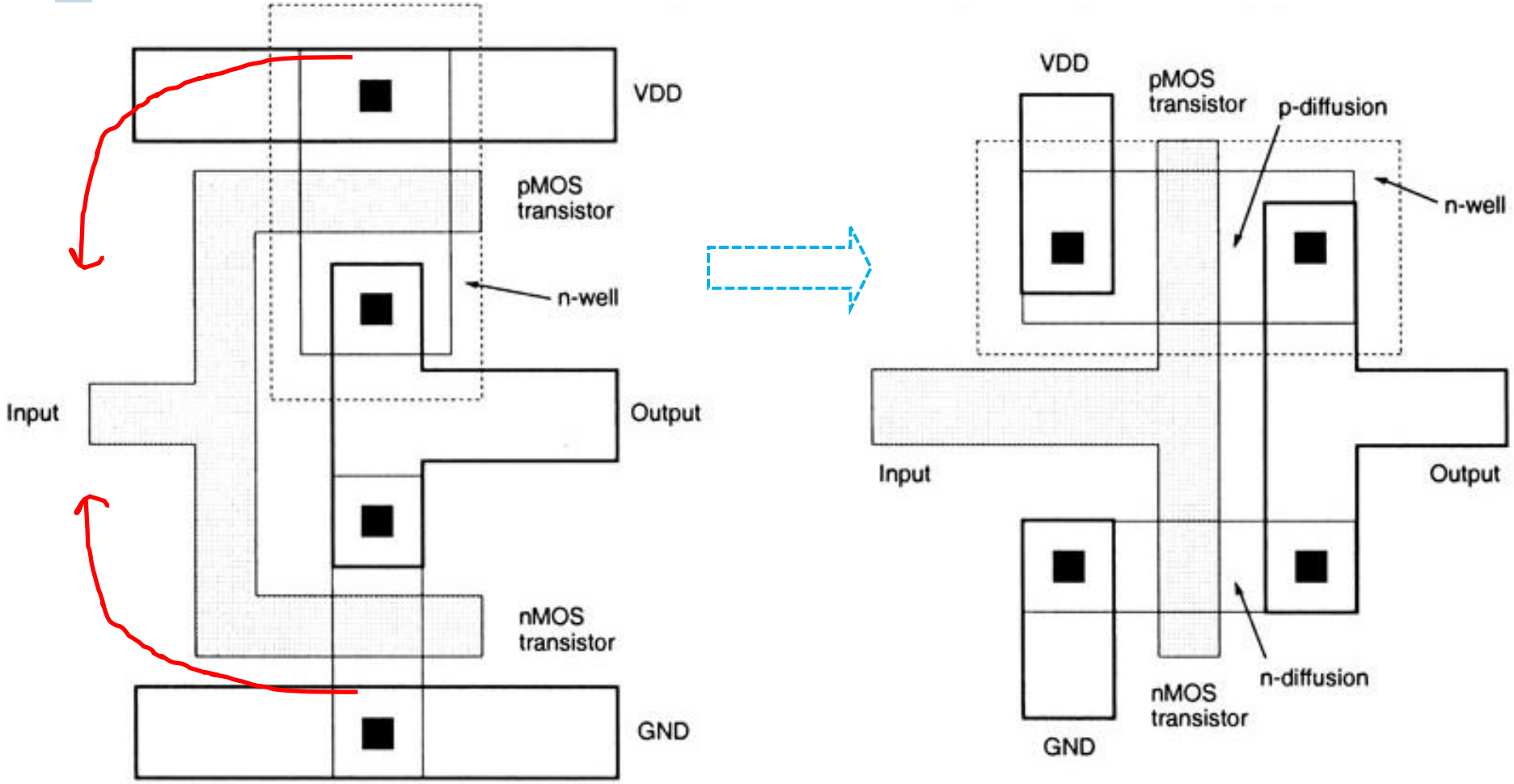
CMOS Logic Inverter – IC layout

(proper MOSFET layout orientation – less chip area)



CMOS Logic Inverter – IC layout

(MOS transistor sizes – essential design consideration)

- The sizes (W & L) of MOSFETs need to be designed in the layout.

If $V_{T0n} = |V_{T0p}|$

$I_{Dn} = I_{Dp}$

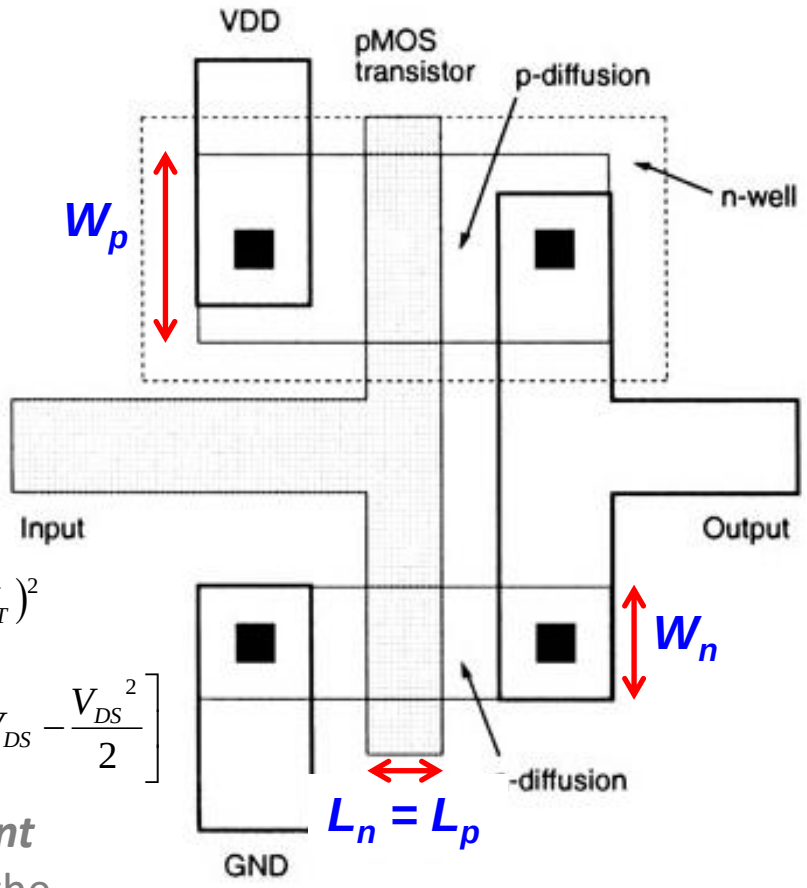
or $R_n = R_p$

$$\mu_n \left(\frac{W}{L}\right)_n = \mu_p \left(\frac{W}{L}\right)_p$$

$$I_{D,sat} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_T)^2$$

$$I_{D,lin} = \mu_n C_{ox}\left(\frac{W}{L}\right)\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$R_{n/p}$: ***equivalent*** **resistance** of the MOSFET when turned on



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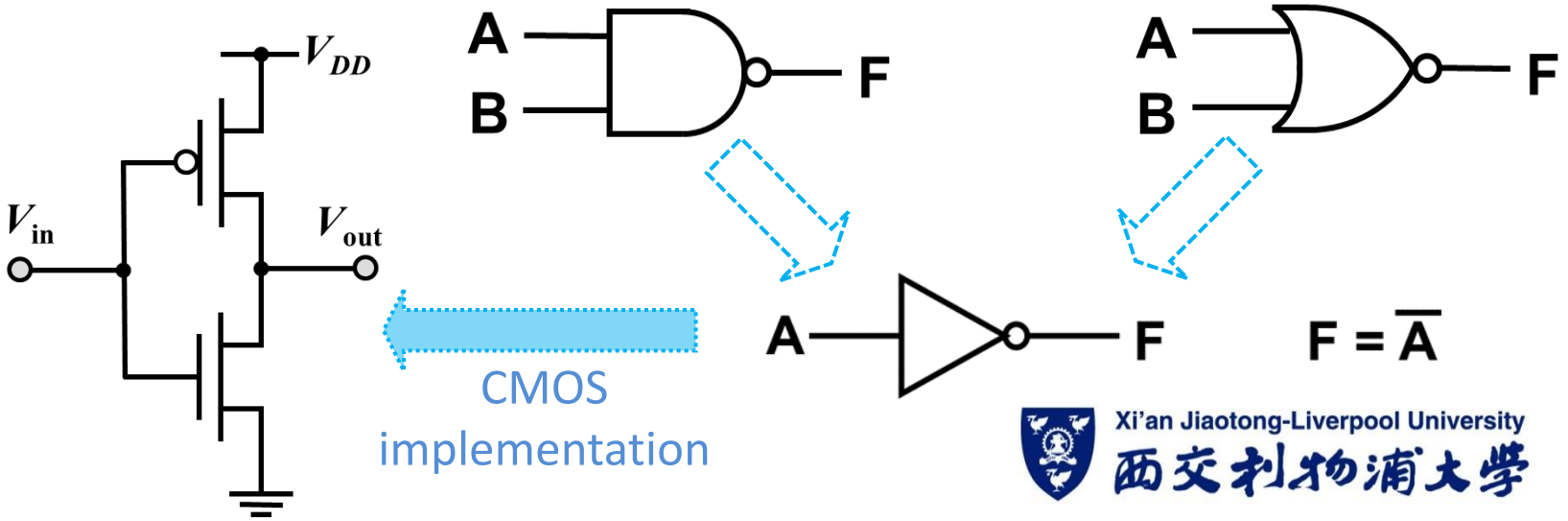
CMOS Logic Inverter

(one ***p***MOS & one ***n***MOS)

- The **logic inverter** is an important start for understanding the operation and characteristics of CMOS logic circuits.
  - Digital circuits of a NAND and NOR logic gates can be *reduced* to a logic inverter. (Do you know why?)



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