Lecture 12

of

EEE201

CMOS Digital Integrated Circuits

Department of Electrical & Electronic Engineering

Xi'an Jiaotong-Liverpool University (XJTLU)

Monday, 2nd December 2024

- **RAM & ROM**
  - memory architecture
  - memory cells of SRAM & DRAM
  - memory cell of EEPROM
  - address decoder

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Circuits for Storing Digital Data

(access time & storage density)

- To *process* **digital data**, **combinational logic circuits** are needed to perform logic functions (e.g. addition, multiplication, multiplexing).
- It is equally important to have electronic circuits to ***store*** **digital data** either temporarily or for a long time. Such digital circuits are **memory circuits**.
  - Short **access time** is expected in retrieving the *stored* digital data.
  - High **density** of **storage capacity** is always preferred whenever possible because of the ever increasing amounts of digital data (e.g. videos, images, music, etc.)

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Digital Memory Circuits
(RAM & ROM)

- The silicon CMOS technology that is good for realisation of **combinational logic circuits** in general can also be used to make **memory circuits**.
  - The semiconductor fabrication however may be modified for optimal manufacturing of memory circuits.
- There are two basic types of **memory circuits** which can be implemented using CMOS transistors for storing digital data *electronically*.
  - **random access memory** (**RAM**) – volatile
  - **read-only memory** (**ROM**) – non-volatile
  - A **volatile memory** loses its stored data when power is removed.

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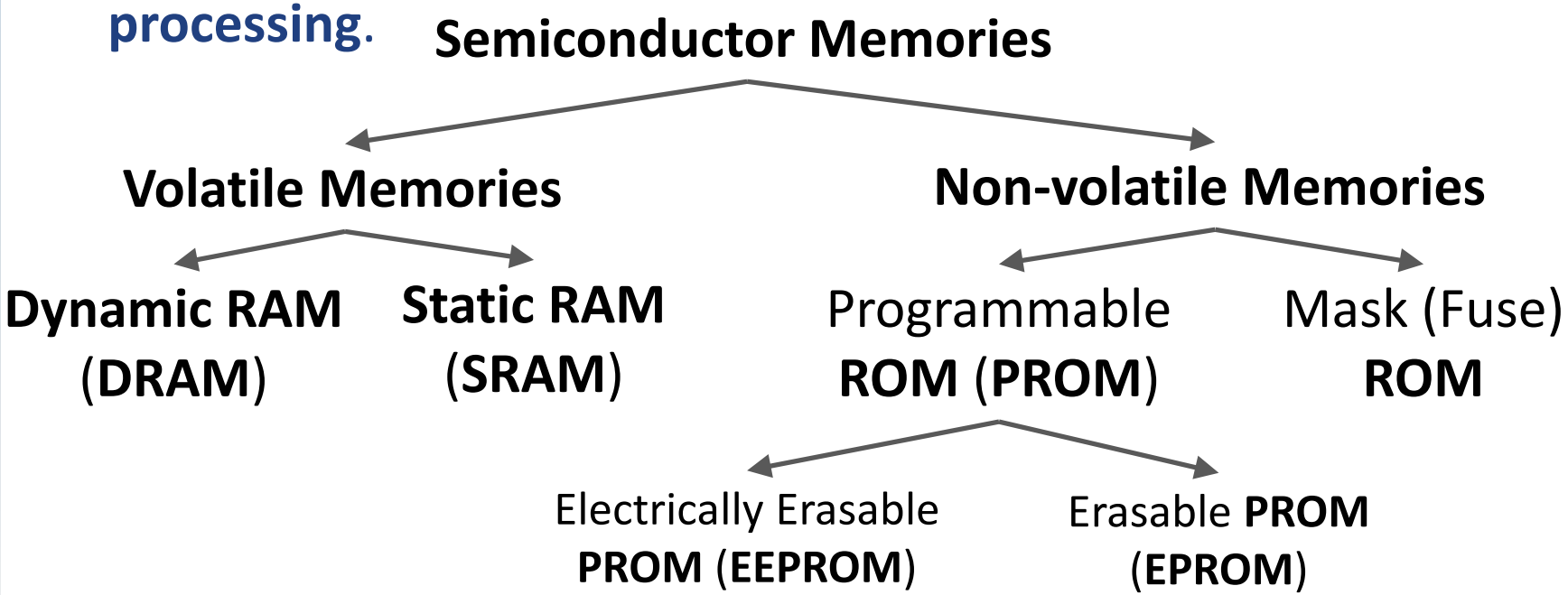
Semiconductor Memories

(memory types)

- Semiconductor memories are predominantly used for storing digital data with its fast *electronic* **retrieval** and **processing**.



  - Among **EEPROM**, there are **flash memory**, ferroelectric RAM, magnetoresistive RAM, resistive RAM, phase-change RAM

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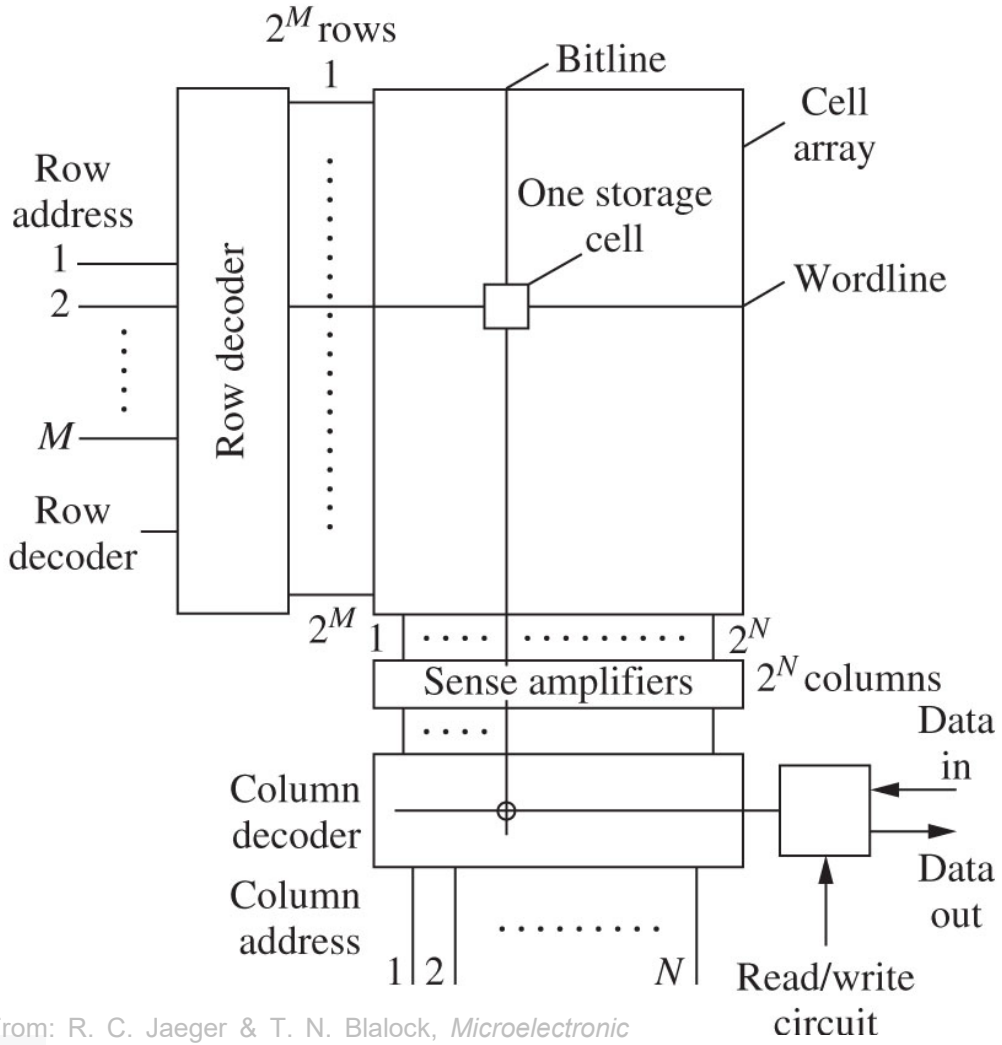
Memory Architecture

(array of storage cells)



From: R. C. Jaeger & T. N. Blalock, *Microelectronic Circuit Design*, 4e, © 2010 McGraw-Hill, USA.

- Both RAM and ROM share the same basic **memory architecture**.
  - It consists of an array of **storage cells** with 2^M columns and 2^N rows.
  - Each **storage cell** (or called **memory cell**) can store one **bit** of digital data "1" or "0".

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Storage Cell or Memory Cell

(varying from RAM to ROM)

- The **memory cell** varies from RAM to ROM.
- There are two types of RAM, namely **static RAM** (**S**RAM) and **dynamic RAM** (**D**RAM), and their **memory cells** are different.
  - The **SRAM** and **DRAM** have their trade-off in the **access time** and **memory density** (i.e. amounts of digital data stored per unit chip area). It is again **performance** and **cost *trade-off***.
- Regardless the types of RAM or ROM, the **memory cell** uses typically the **voltage** or **charge** to store digital data.
  - **Information** must be *represented* by **physical states** when stored or processed.

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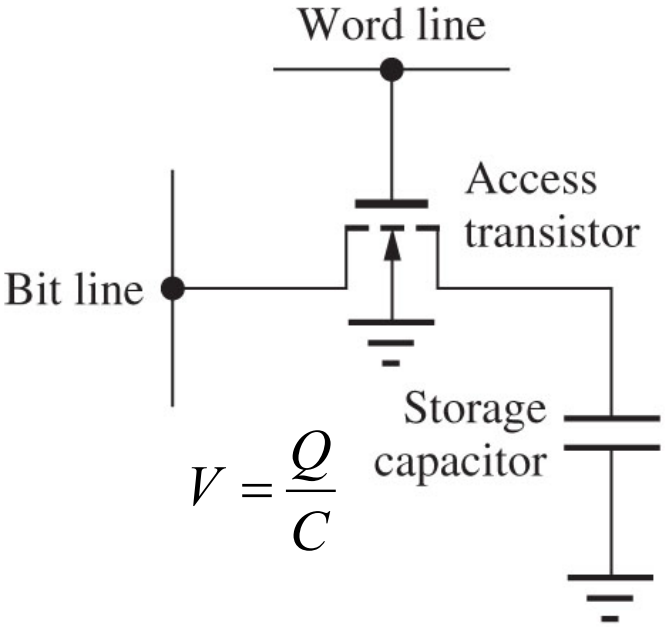
Memory Cell of Dynamic RAM

(one transistor & one capacitor)

- The **memory cell** of the **DRAM** typically consists of only two devices: a transistor and a capacitor.



  - The **charge** on the capacitor is used to store one bit of digital data.
  - Since the **charge** on the capacitor *decays* with a finite time constant (about a few millisecond), a ***periodic refresh*** is needed to restore the charge so that the DRAM does not lose the memory.
  - Using only two devices in each memory cell, DRAM can be of very high memory density.

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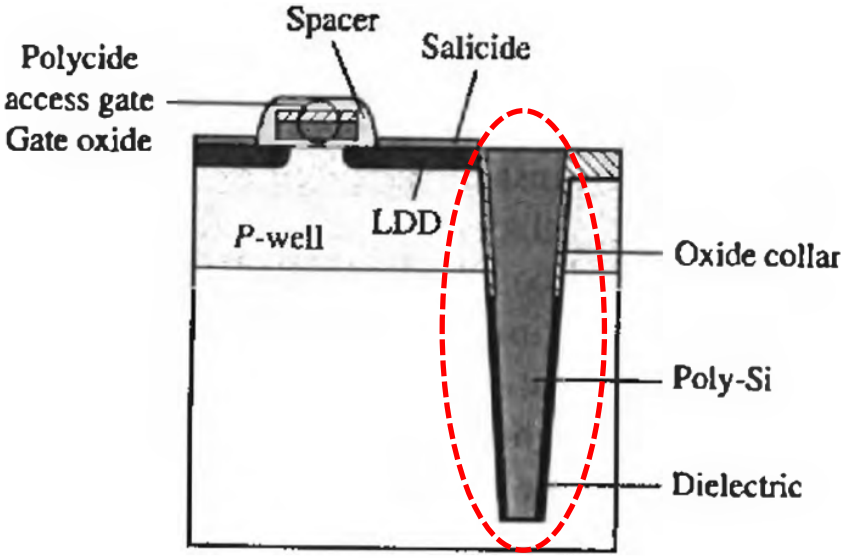
Memory Cell of Dynamic RAM

(DRAM cell structure)

- In the **DRAM memory cell**, the transistor is typically an nMOSFET.



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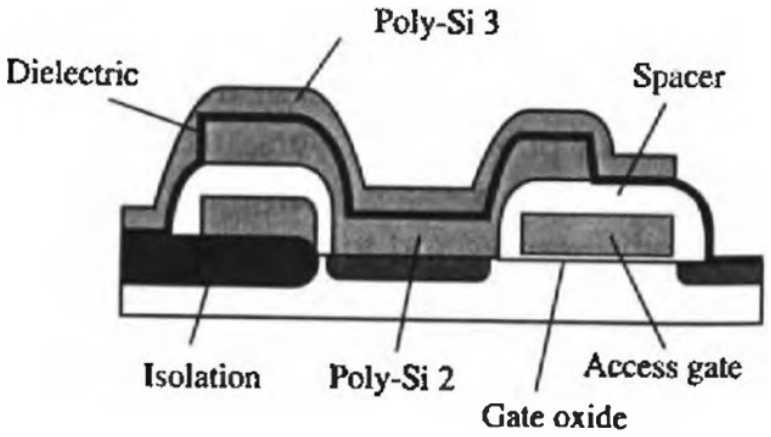

  - The capacitor can be a MOS capacitor, a deep-trench capacitor or a parallel-plate capacitor using the two layers of polysilicon.

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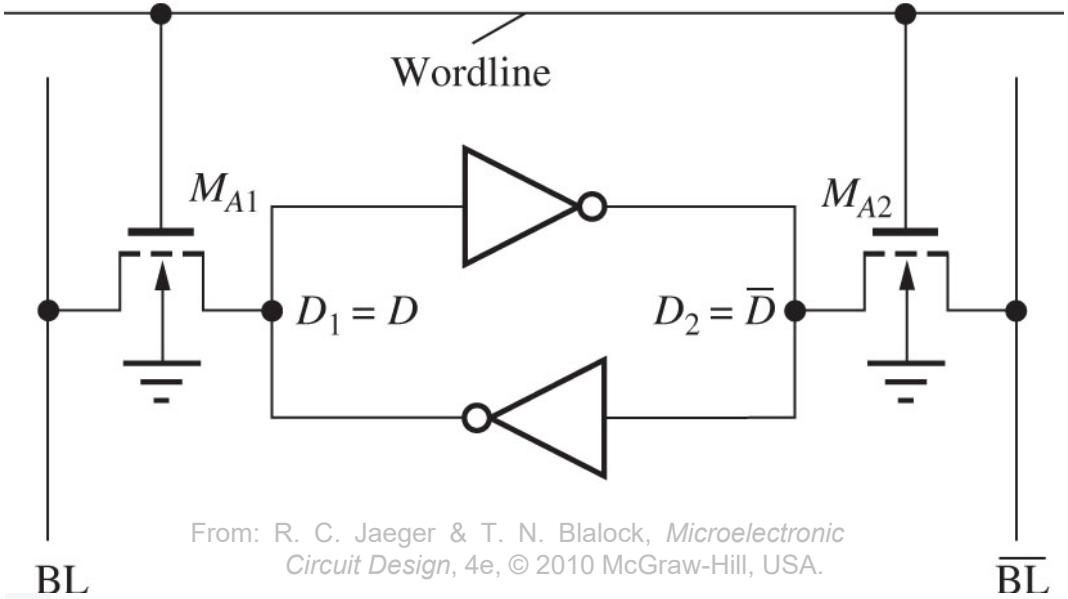
Memory Cell of Static RAM

(two inverters for bistable flip-flop)

- The **memory cell** of the **SRAM** consists of a basic bistable flip-flop circuit that needs only an applied DC voltage to retains its memory.
  - The bistable flip-flop circuit can be built by two **inverters**.



From: R. C. Jaeger & T. N. Blalock, *Microelectronic Circuit Design*, 4e, © 2010 McGraw-Hill, USA.

- Typically six transistors are used.
- Compared with the DRAM, no refresh cycle is needed to retain the memory.

  $\Rightarrow$ ***static*** RAM

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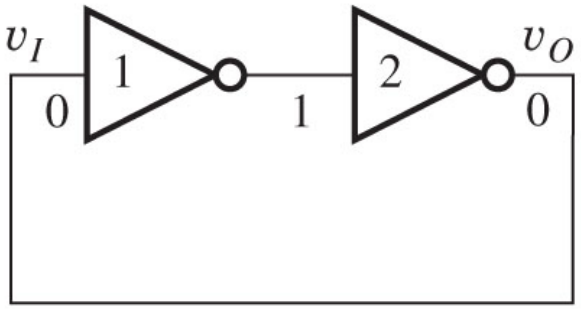
Memory Cell of Static RAM

(cross-coupled inverter pair)

- The basic electronic storage part in the SRAM cell consists of two **inverters** connected in a loop.



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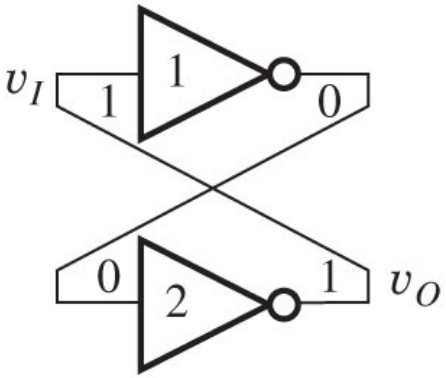

- The output of the second inverter is fed back to the input of the first inverter.
- It forms a logically stable configuration, having two stable states. It is therefore called a **bistable circuit**.
- The alternate representation in the form of a pair of ***cross-coupled*** **inverters** is often called a **latch**.
- The inverter **voltage transfer characteristics** can be used to study the circuit behaviour.

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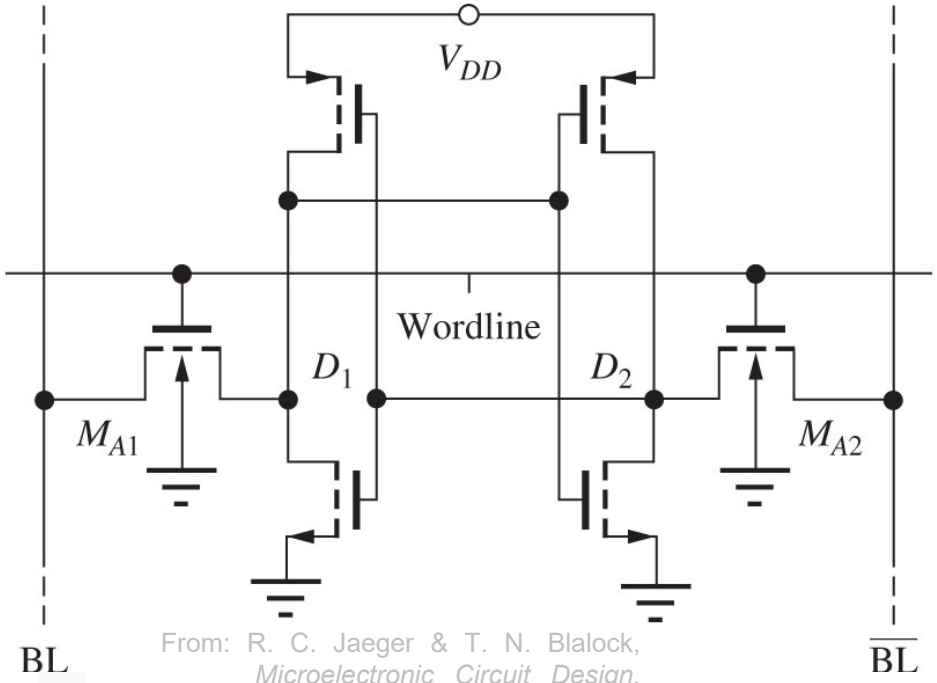
Memory Cell of Static RAM

(six transistor implementation)

- Two additional transistors are added to the two **bistable circuit** (i.e. two inverters in a loop) to isolate it from other memory cells and to provide an electrical path to read and write data to the cell.



From: R. C. Jaeger & T. N. Blalock, *Microelectronic Circuit Design*, 4e, © 2010 McGraw-Hill, USA.

- A CMOS logic inverter is formed by one ***p***-channel and one ***n***-channel MOSFETs.
- Such an implementation is called a ***six-transistor*** (6T) **SRAM cell**.

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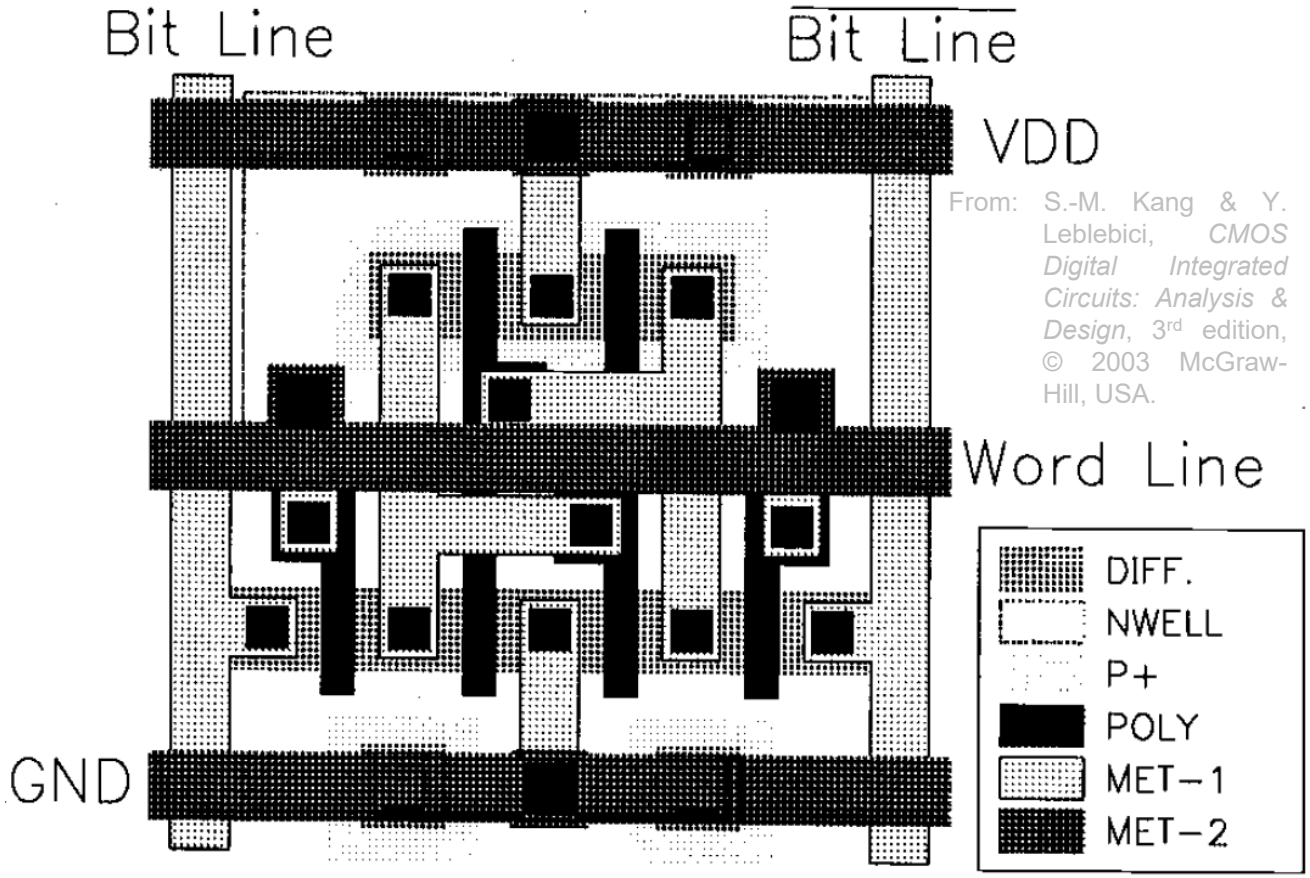
Memory Cell of Static RAM

(layout of 6T SRAM cell)



From: S.-M. Kang & Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis & Design*, 3rd edition, © 2003 McGraw-Hill, USA.

- The **6T SRAM cell** can be implemented with the IC layout as shown here.
- Note that the MOS transistor sizes are not optimised here.

- Can you recognise the six transistors and determine their rough sizes?

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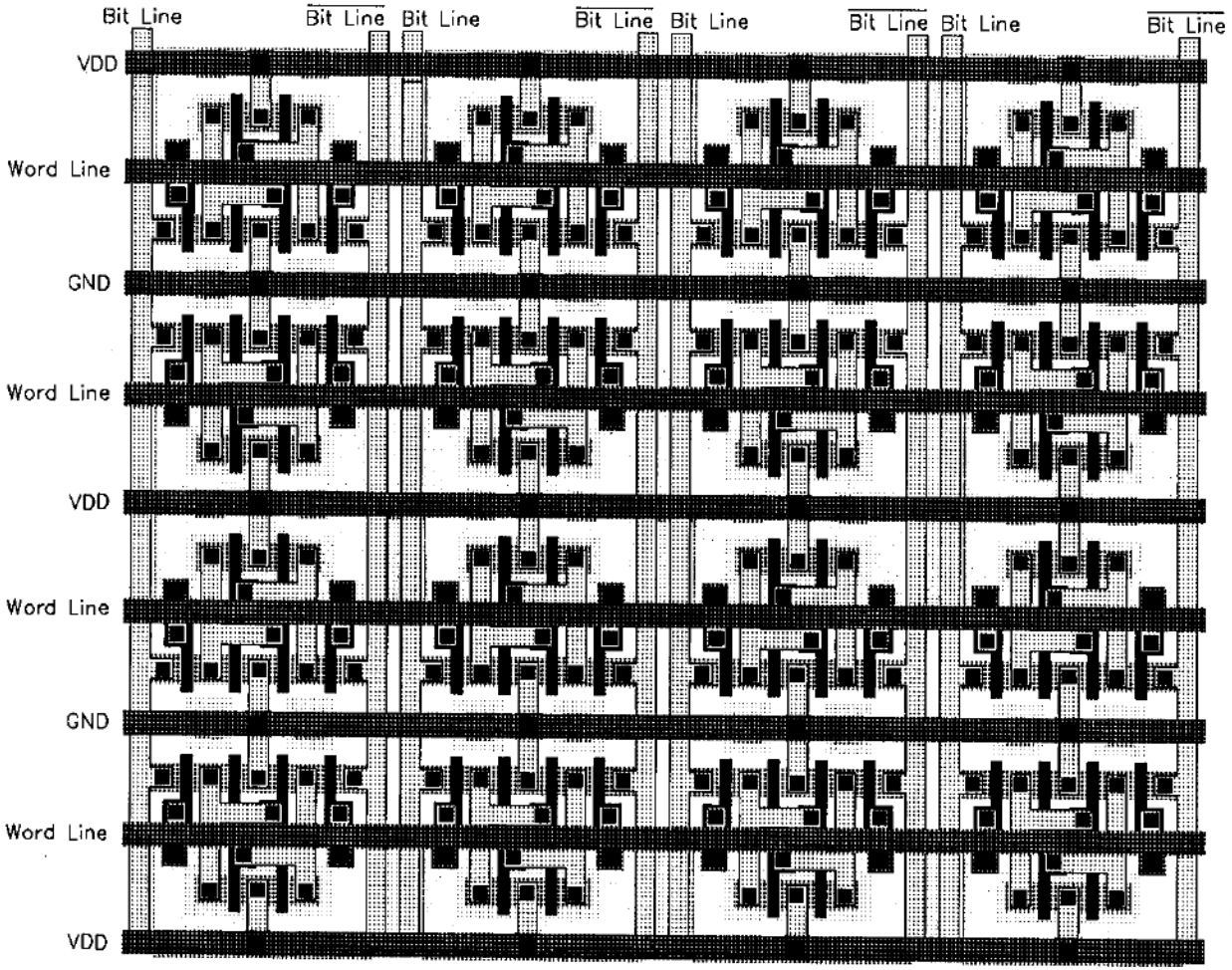
Memory Cell of Static RAM

(array of SRAM cells)



From: S.-M. Kang & Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis & Design*, 3rd edition, © 2003 McGraw-Hill, USA.

- The 6T SRAM cell layout are duplicated in an array of 2^M columns and 2^N rows for storing 2^{M+N} bits of digital data.
- The IC layout shown here is a 16-bit SRAM.

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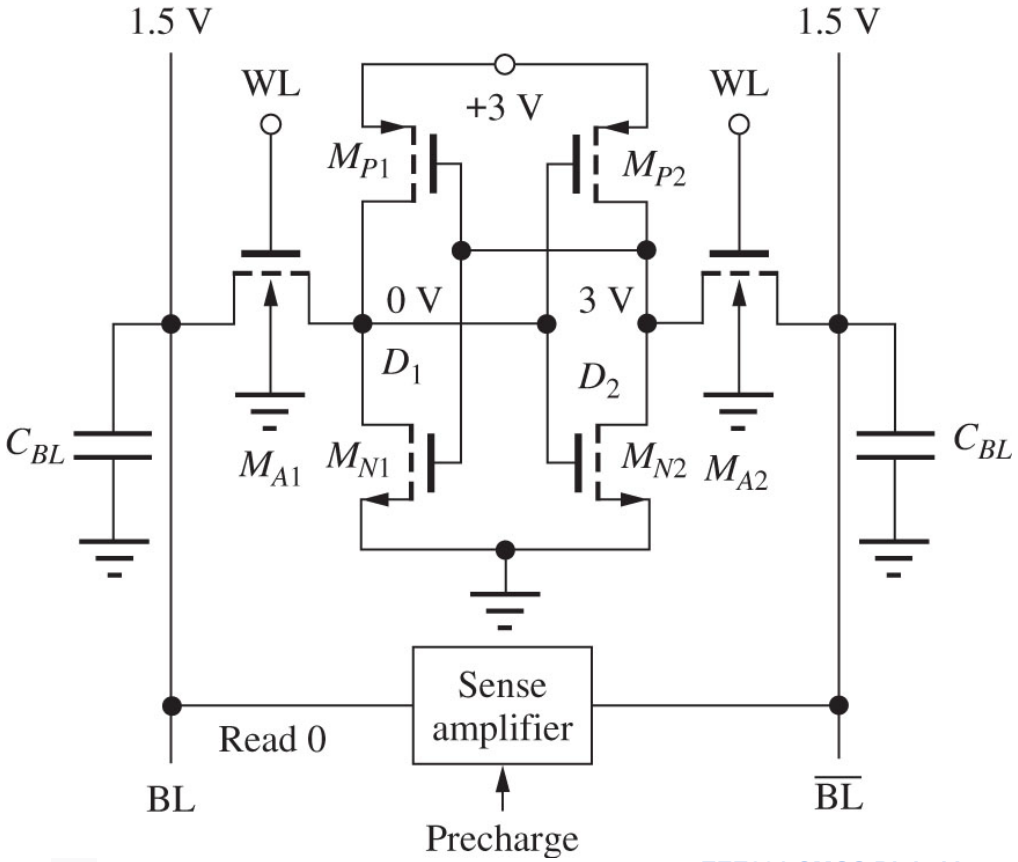
Memory Cell of Static RAM

(sense amplifier)

- To read data stored in the SRAM cell, a **sense amplifier** is needed to detect the voltages in the bistable circuit.



- The sense amplifier typically pre-charges the capacitors C_{BL} of the **bit line** (BL) to a voltage of half of the V_{DD}.
- When the **word line** (WL) is activated, voltage signals of the bistable circuit pass to C_{BL} via M_{A1} & M_{A2}.

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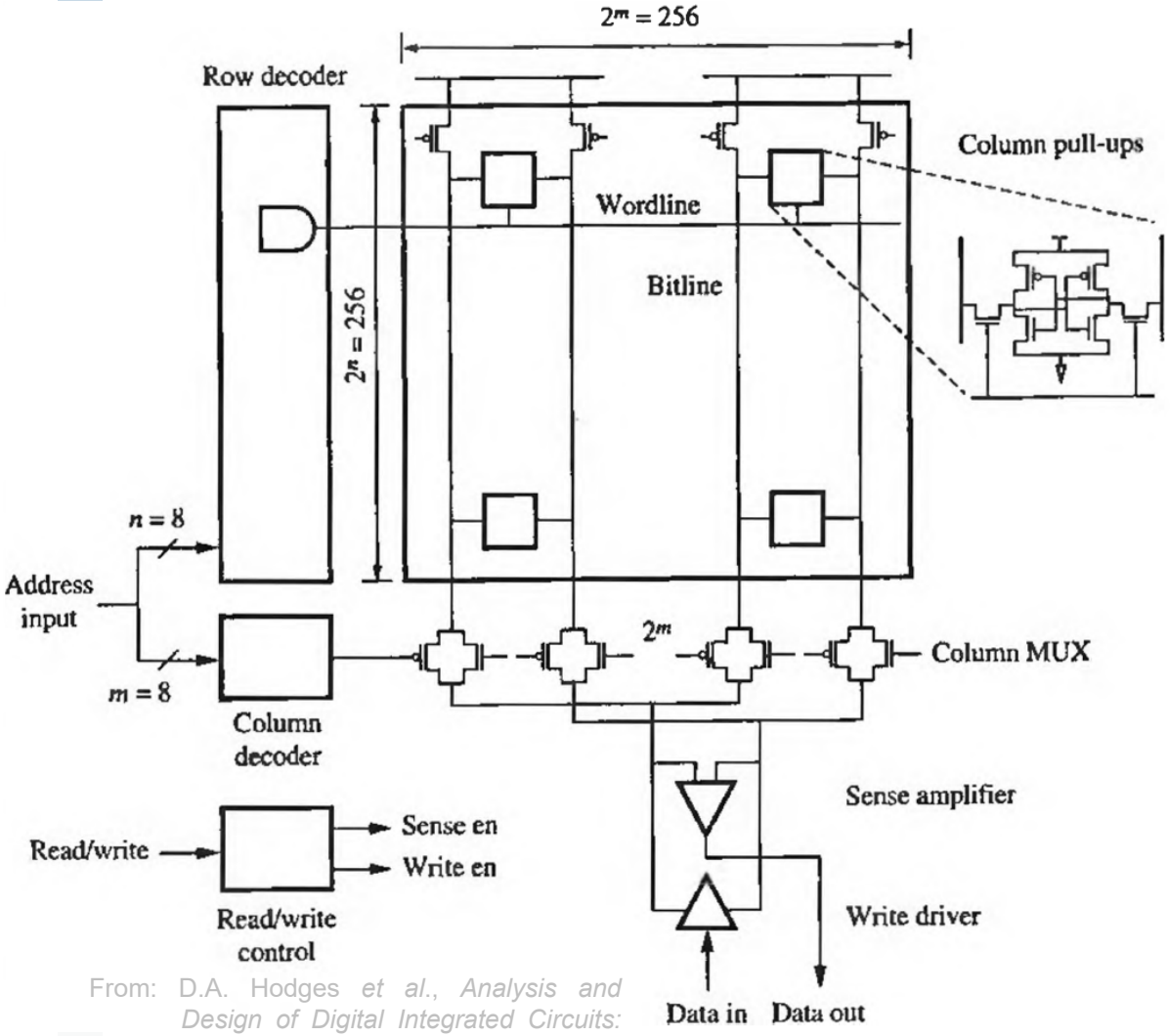
Memory Cell of Static RAM

(sense amplifier & read-write circuitry)



From: D.A. Hodges *et al.*, *Analysis and Design of Digital Integrated Circuits: In Deep Submicron Technology*, 3rd edition, © 2003 McGraw Hill, USA.

- The **sense amplifier** (and also the write driver) can be shared among multiple memory cells by using circuits to select the memory cells.

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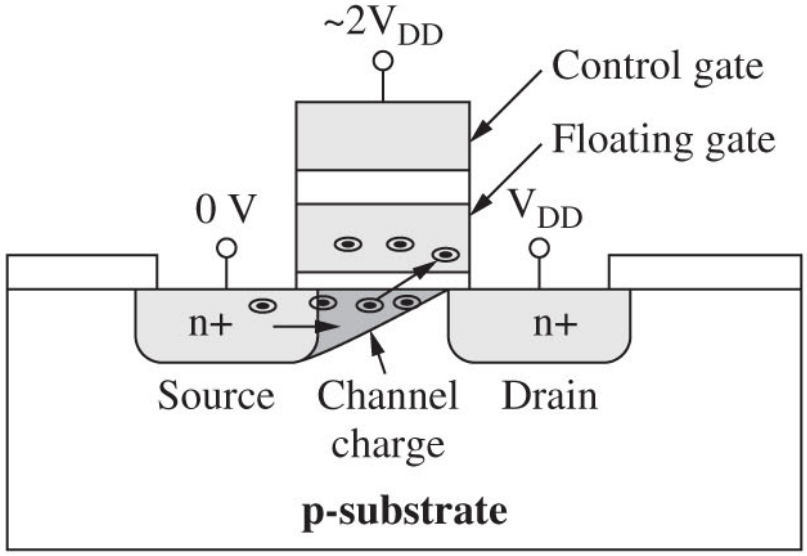
Memory Cell of EEPROM

(electrically erasable programmable)

- In the case of the ROM, the **memory cell** can consist of only one device (e.g. transistor).

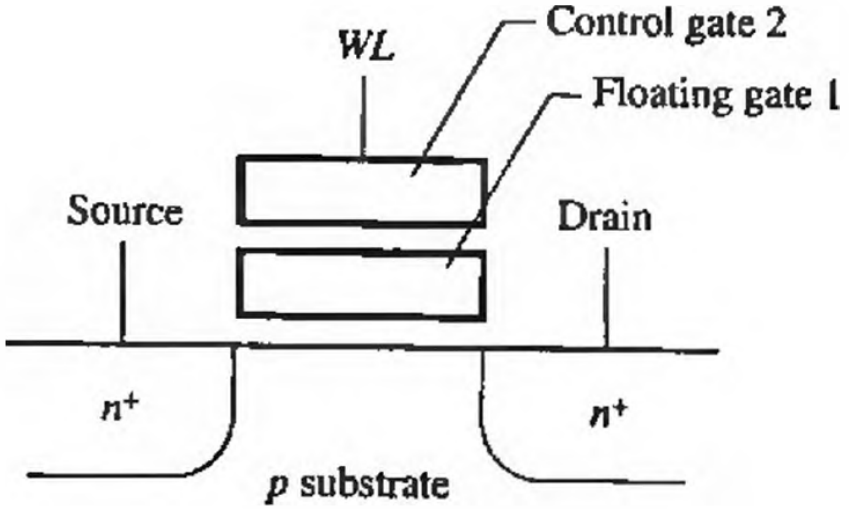


From: R. C. Jaeger & T. N. Blalock, *Microelectronic Circuit Design*, 4e, © 2010 McGraw-Hill, USA.

- In the **electrically erasable programmable** ROM (EEPROM), the device in the memory cell is a MOSFET with a **control gate** and a **floating gate**.
  - Charges (namely electrons) are stored in the floating gate.
  - Such EEPROM is also known as **flash memory**, used in USB memory sticks.

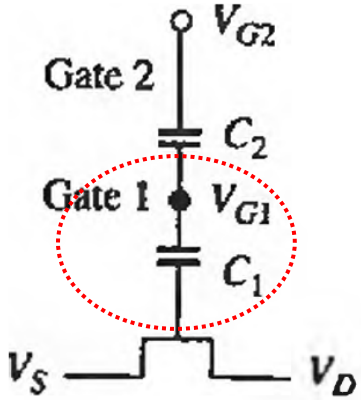
Memory Cell of EEPROM

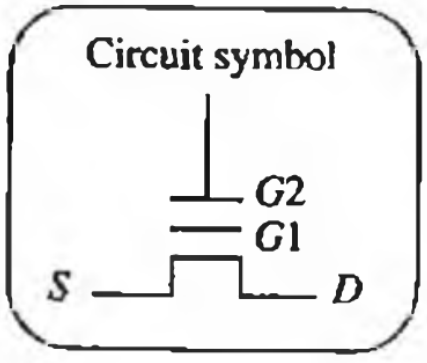
(floating gate for storing charges)



(a)

From: D.A. Hodges *et al.*, *Analysis and Design of Digital Integrated Circuits: In Deep Submicron Technology*, 3rd edition, © 2003 McGraw Hill, USA.





- The **EEPROM memory cell** is essentially a MOSFET, but with an additional internal node in the gate electrode.
  - Note the two gate capacitors in series in the equivalent circuit diagram; charges can be stored in the bottom capacitor C_1.

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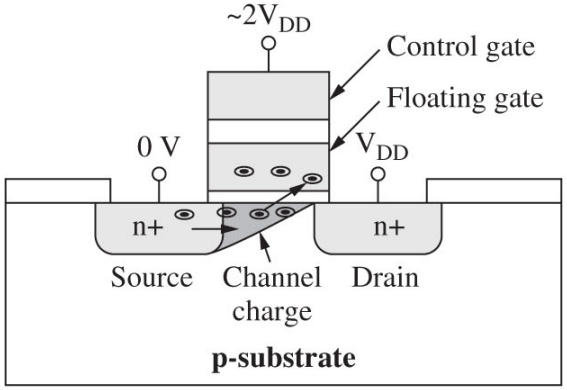
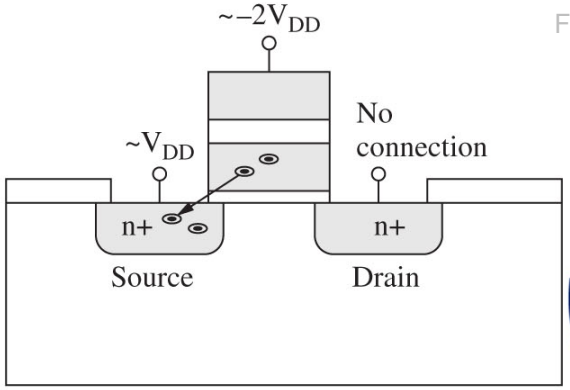
Memory Cell of EEPROM

(threshold voltage of MOS transistor)

- The presence of charges in the **floating gate** give a different **threshold voltage** V_{Tn} *sensed* at the control gate of the MOS transistor.
  - Reading data involves *sensing* the V_{Tn} of the transistor.
- Erasure of data requires a voltage (+ve or -ve) of larger magnitude applied to the **control gate** to introduce or remove charges into or from the **floating gate**.





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Memory Cell of EEPROM

(I-V curve of the MOSFET with a floating gate)

- The presence of electrons in the **floating gate** give a higher **threshold voltage** V_{Tn} *sensed* at the control gate of the nMOS transistor.

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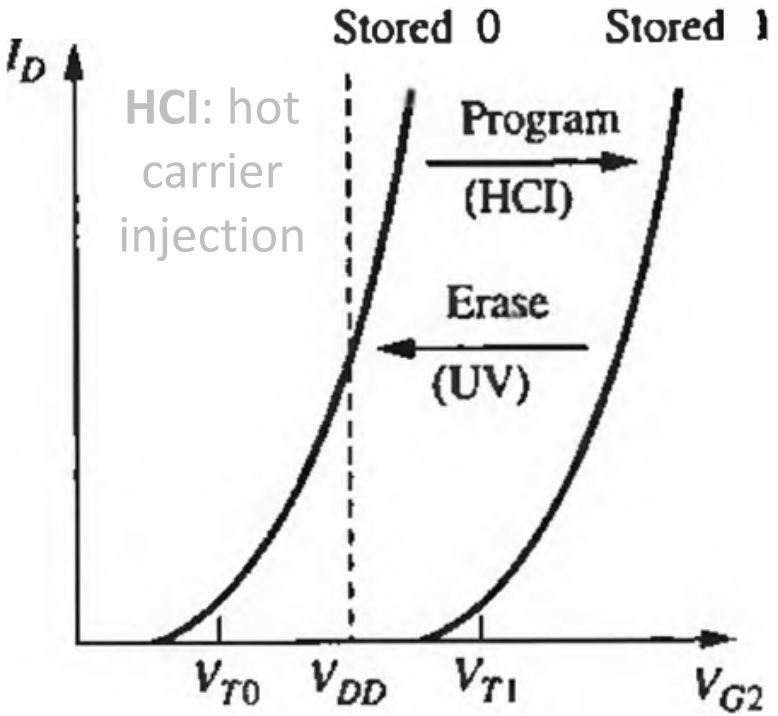

- After removal of electrons in the floating gate, V_{Tn} decreases when *sensed* at the control gate.
- The I_D-V_{GS} curve of the nMOS transistor is shifted horizontally accordingly.

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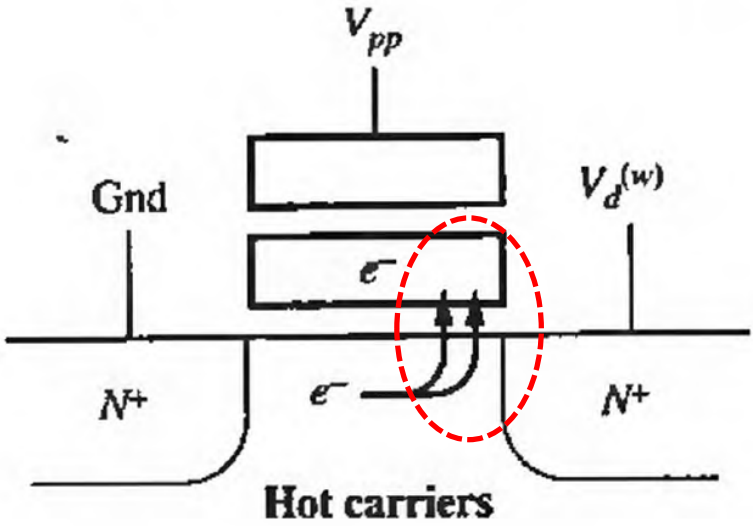
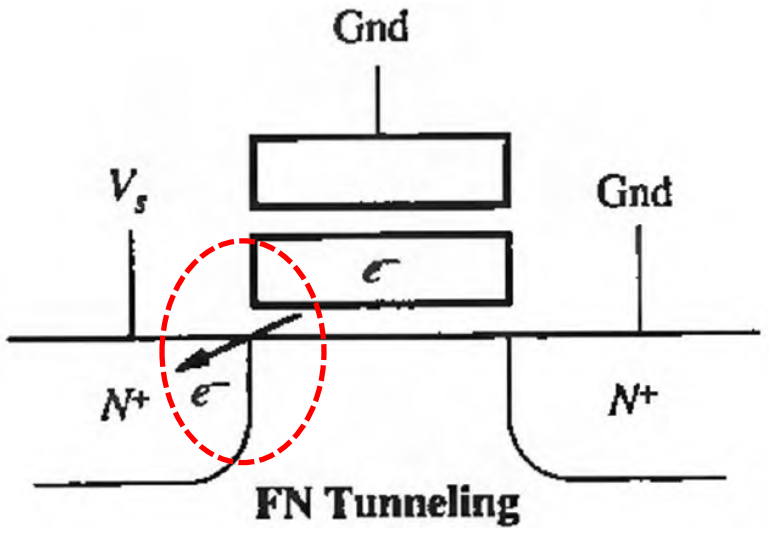
Memory Cell of EEPROM

(write & erasure processes)

- In writing data to the EEPROM memory cell, the charges (typically electrons) are injected to the floating gate at the drain end, by hot carrier injection (HCI).
  - In erasing data, electrons are removed at the source end from the floating gate.





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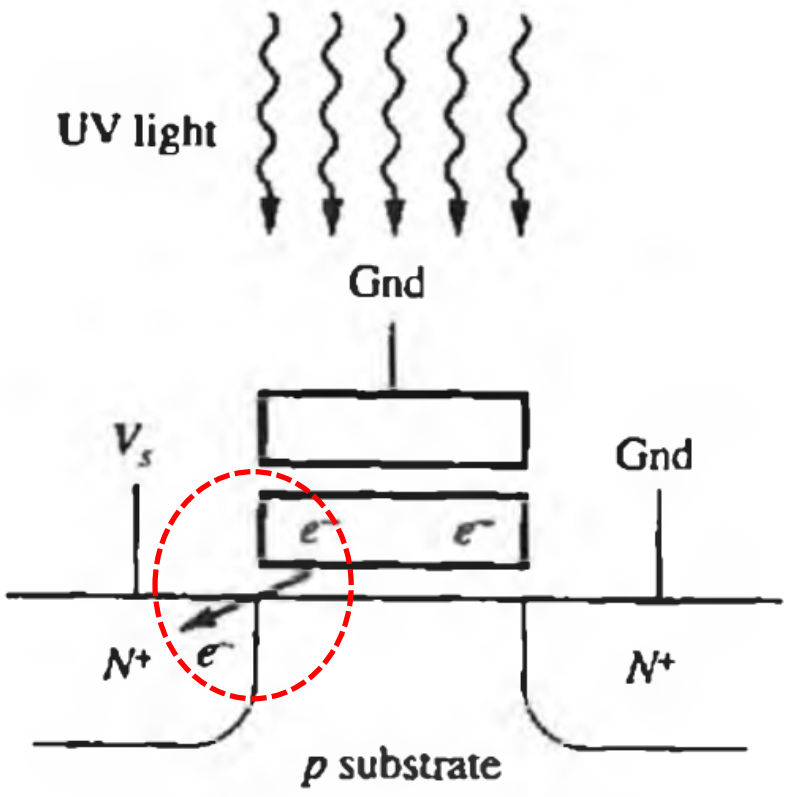
Memory Cell of EEPROM

(electrically erasable programmable)

- In some EEPROMs, the erasure of data can also be accomplished more easily with the use of UV light.



  - An electron can gain energy by absorbing a photon and hence overcoming the energy barrier to get away from the floating gate.

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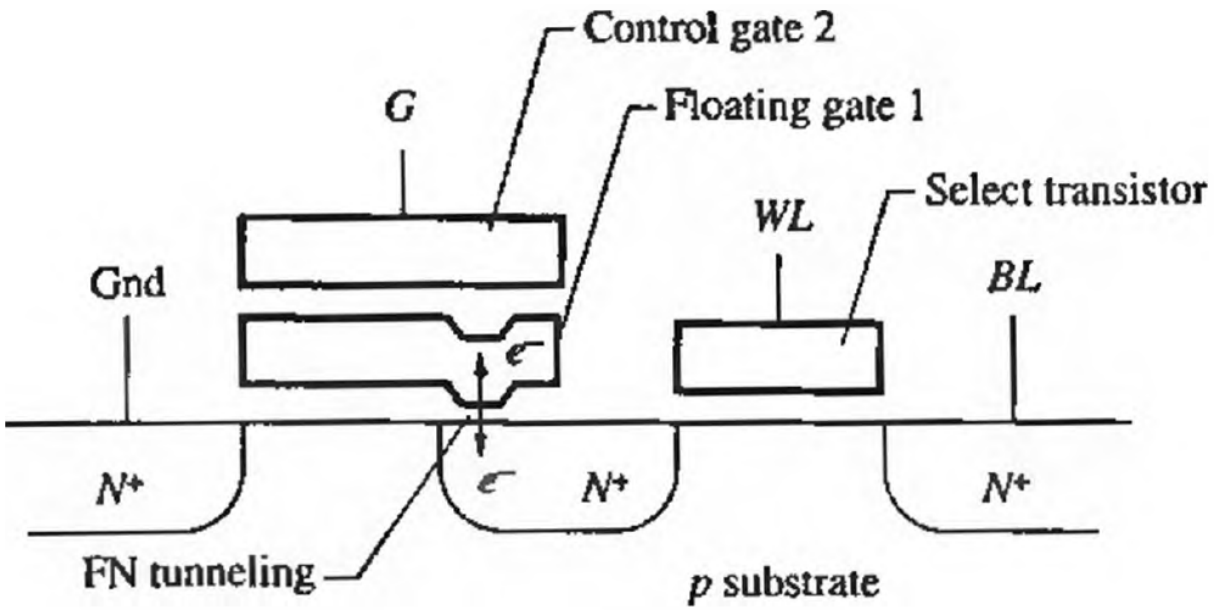
Memory Cell of EEPROM

(additional select transistor)

- In some EEPROMs, there is an additional transistor for selecting the memory cell to read/write data.



  - Despite certain reliability advantages, the bit density is lower in such EEPROM design.

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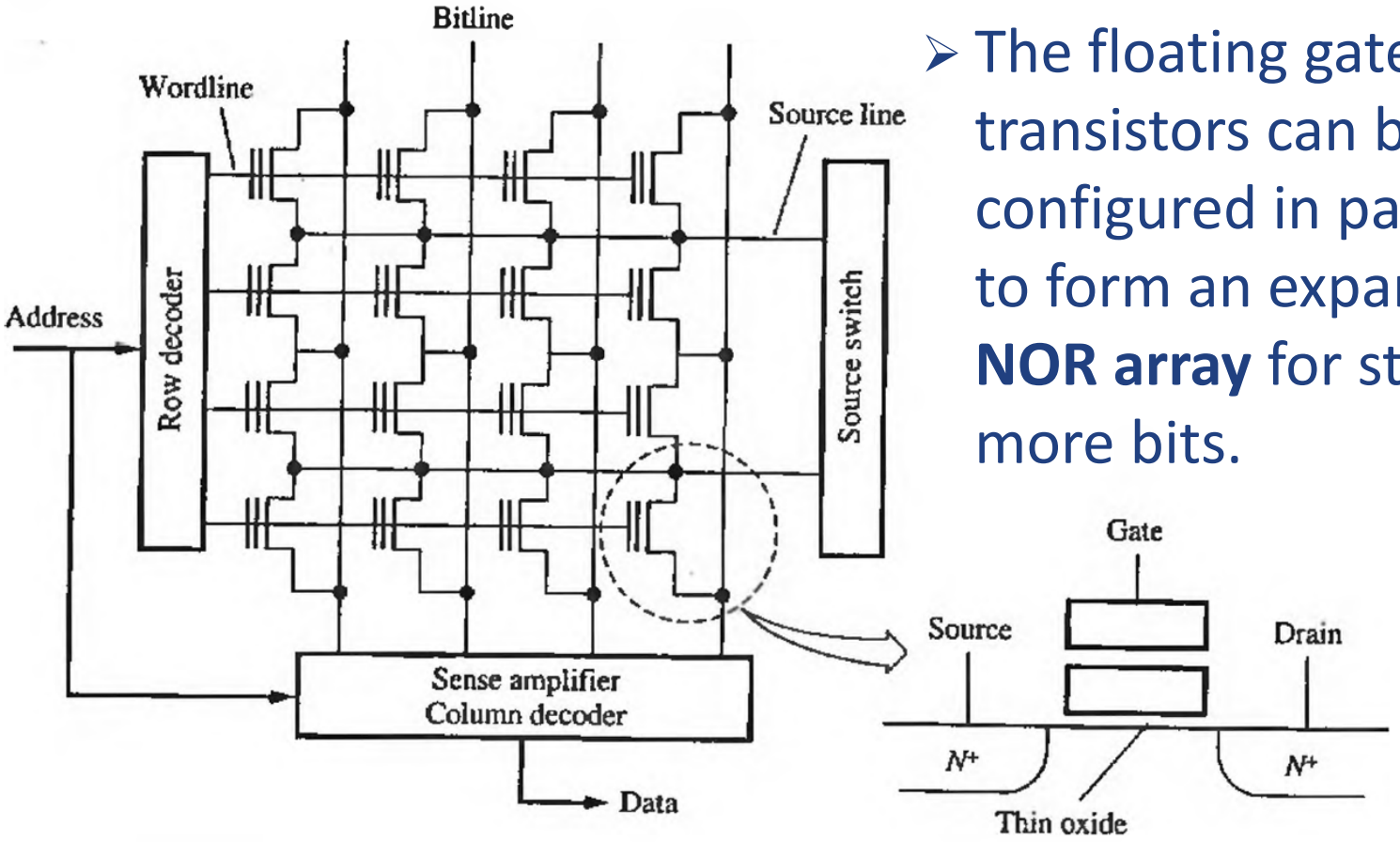
Flash Memory

(NOR array)



- The floating gate transistors can be configured in parallel to form an expandable **NOR array** for storing more bits.

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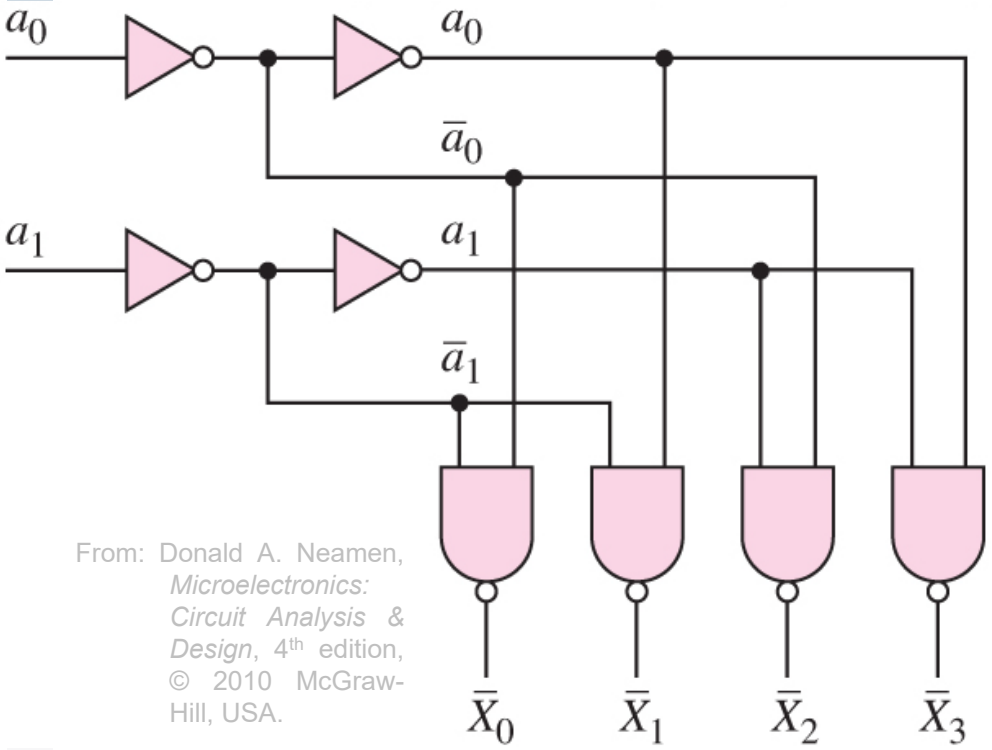
Address Decoder

(use combinational logic circuits)

- When the **memory cells** are arranged in an **array**, **address decoders** are needed to read/write data from/to specific cells.



From: Donald A. Neamen, *Microelectronics: Circuit Analysis & Design*, 4th edition, © 2010 McGraw-Hill, USA.

- **Address decoders** are **combinational logic circuits** and can be implemented using basic logic gates.
- A 2-bit address decoder shown here can address four rows or columns.

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SRAM vs. DRAM

(memory density)

- It can be seen that the **SRAM** cell occupies relatively much chip area.
  - As a result, the memory size of the **SRAM** can be quite limited. A modern microprocessor has 25 MB SRAM.
  - 1 MB = 1024 KB; 1 KB = 1024 byte = 2^{10} byte; 1 byte = 8 bit. How many SRAM cells are needed for storing 25MB digital data?
- With only one transistor and one capacitor, the DRAM cell uses up far less chip area than that of the SRAM.
  - The DRAM can have very high memory density (e.g. 16 GB). 1 GB = 1024 MB. But it has lower speed and larger power consumption.

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SRAM, DRAM & Flash Memory

(applications)

- With much faster read/write speed (typically 10 ns or less) of the **SRAM**, it is used as **cache memory** in microprocessors.
  - With its relatively lower cost but reasonable read/write speed, the **DRAM** is used as the main computational memory of the computer.
- The **flash memory** has only one transistor in the memory cell.
  - As a result, it has somewhat even higher memory density.
  - It is used for memory cards, USB memory sticks and solid-state drives.
  - However, its write speed can be very low (> 10 μs).

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