

Integrated Electronics & Design

IC Fabrication Techniques

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Reading: Chapter 4.0, 4.2, 4.3.1

Apr 2024

IC Fab. Tech. **OUTLINE**

- **Thin Film Formation**
- **Photolithography and Etching**
- **Doping**
- **IC Resistor**
- **Sheet Resistance**
- **Diode**
- **nMOSFET: Process Flow**
- **nMOSFET: Fab. and Layout**
- **nMOSFET: Layout Rules**



Thin film formation

- **Thermal oxidation**
- **CVD**
- **PVD**

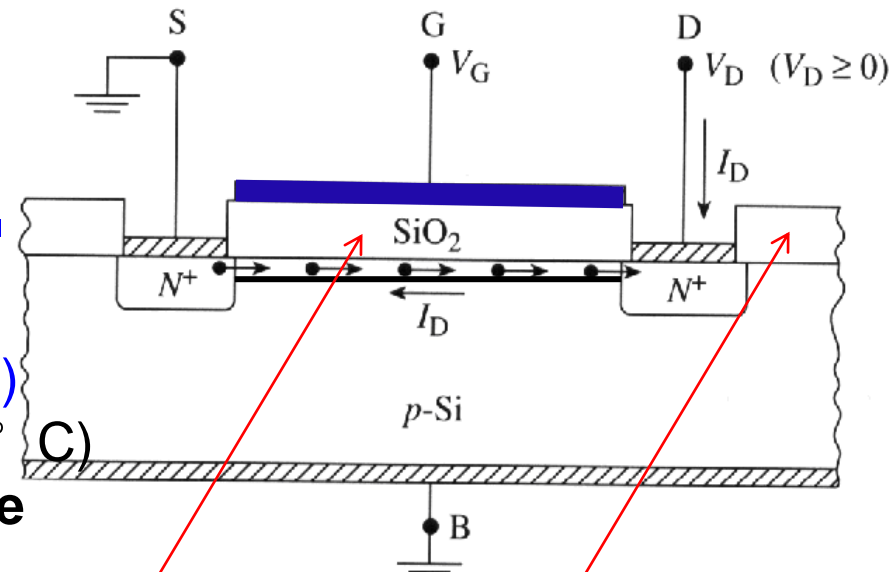
Thermal oxidation

- **Dry oxidation**

- $\text{Si} + \text{O}_2 \rightarrow \text{SiO}_2$ (900-1200° C)
- 700nm oxide: 10 hours (1200° C)
- **Good oxide quality: gate oxide**

- **Wet oxidation**

- $\text{Si} + \text{H}_2\text{O} \rightarrow \text{SiO}_2 + 2\text{H}_2$ (900-1200° C)
- 700nm oxide: 0.65 hours (1200° C)
- **Poor oxide quality: field oxide/diffusion barrier (diffusion mask)**



Gate oxide

Field oxide

H₂O or O₂

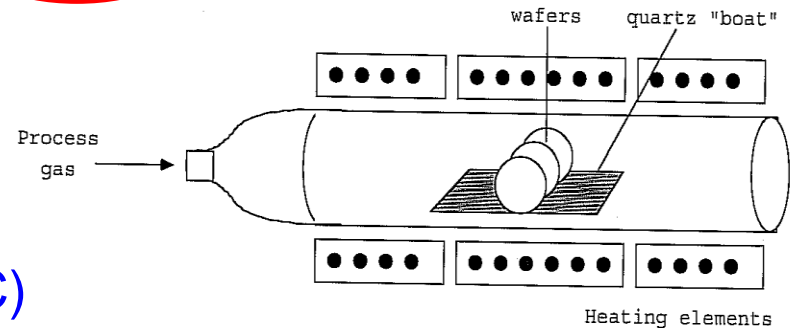
**Thermal
oxidation**

SiO₂

Si

Si

Thermal oxidation

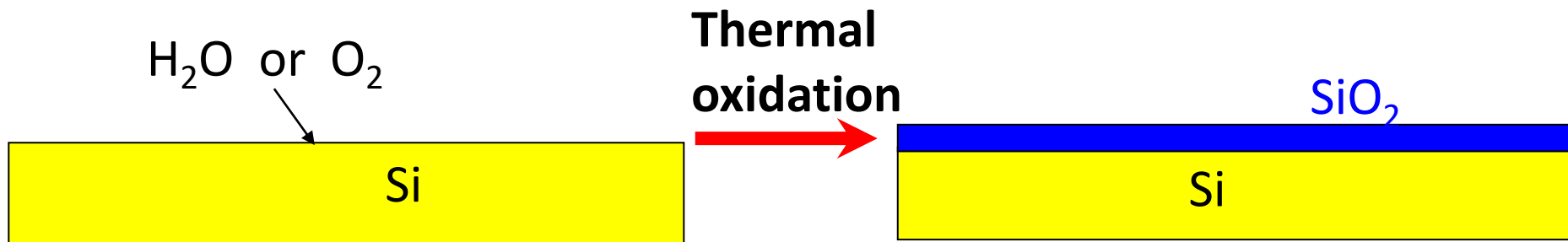


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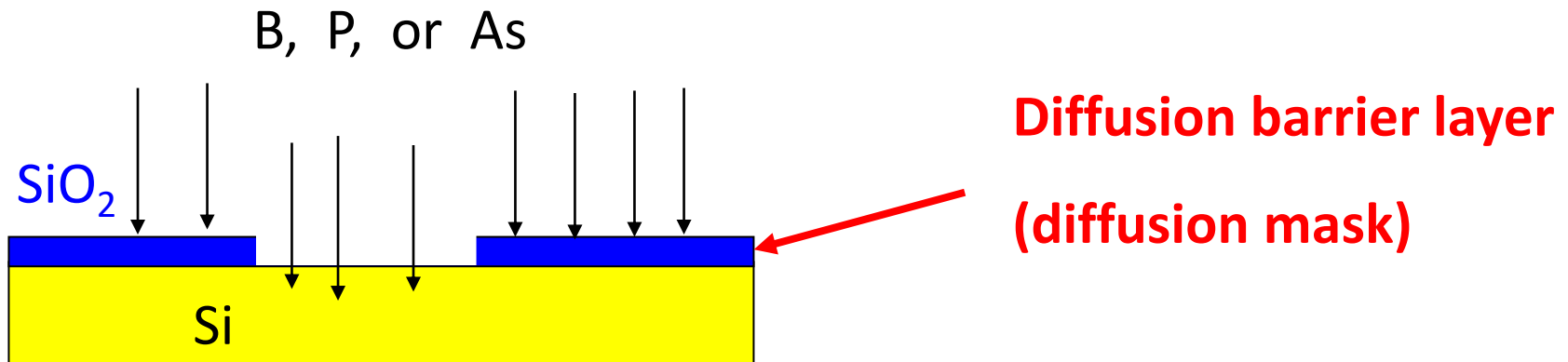
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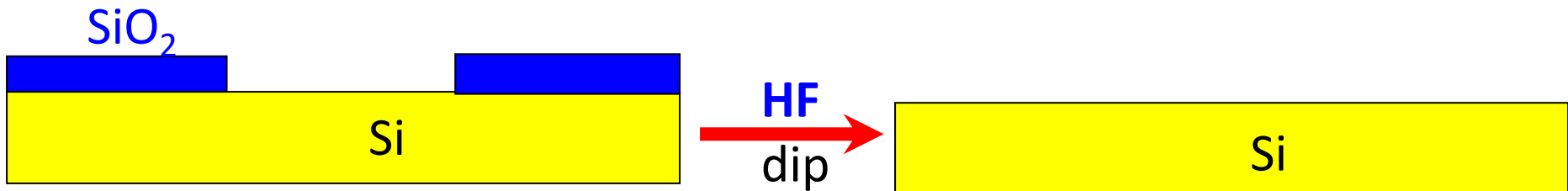


Thermal SiO₂ Properties

- (1) SiO₂ is a **good diffusion mask** for common dopants



- (2) Very **good etching selectivity** between Si and SiO₂.

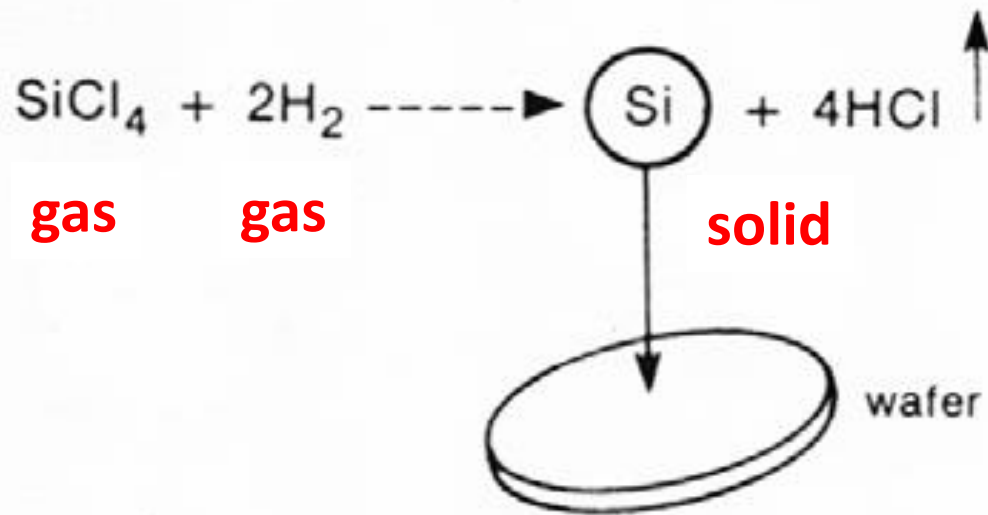


Thin film formation

- Thermal oxidation
- CVD
- PVD

Chemical Vapor Deposition (CVD)

- Thin film formation from vapor phase reactants. Deposited films range from metals to semiconductors to insulators.
- An essential process step in the manufacturing of microelectronic devices. High temperatures and low pressures are the most common process conditions, but are not necessary.
- All CVD involves using an energy source to break reactant gases into reactive species for deposition.



Si

Sub-Si (wafer)

Figure 12.4 Chemical vapor deposition of silicon from silicon tetrachloride.

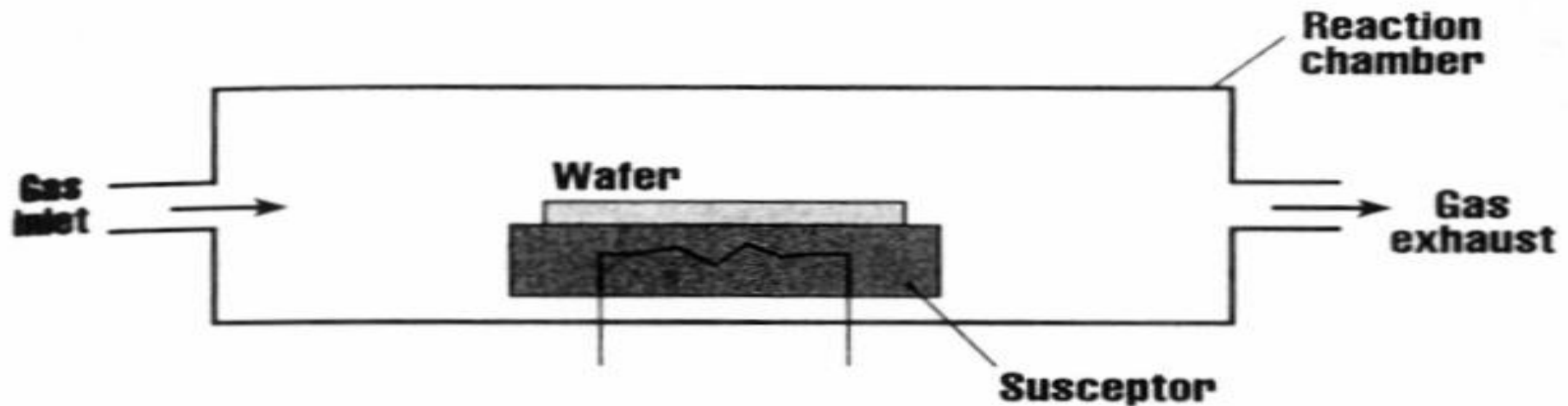


Figure 13-1 A simple prototype thermal CVD reactor.

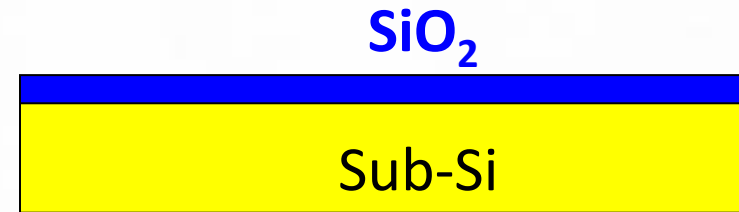
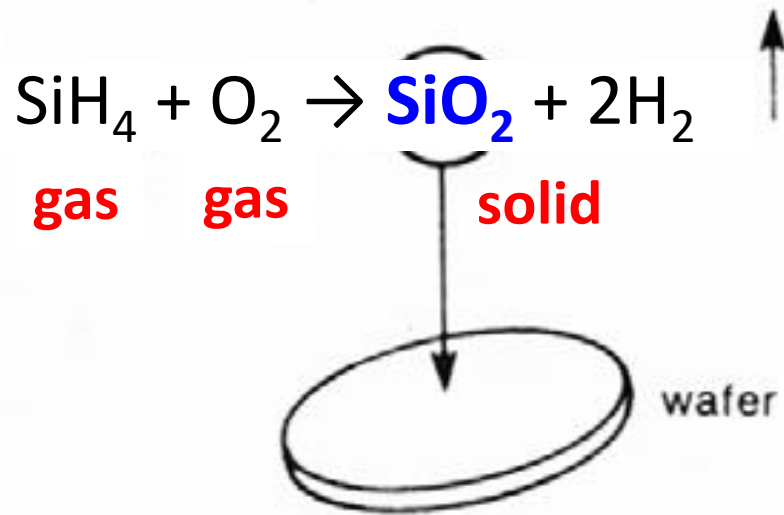


Figure Chemical vapor deposition of silicon from silicon tetrachloride.

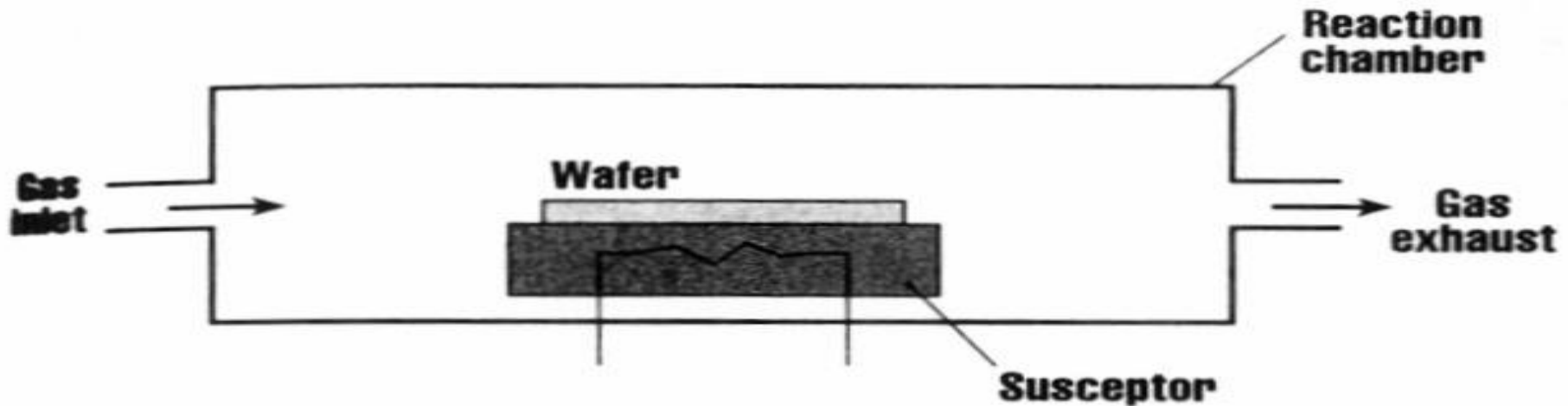
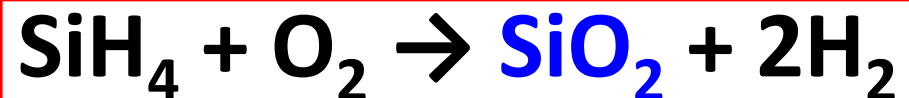


Figure A simple prototype thermal CVD reactor.

Examples of CVD

- Metals/Conductors – W, Al, Cu, doped poly-Si
- Insulators (dielectrics) – BPSG, Si_3N_4 , SiO_2
- Semiconductors – Si, Ge, InP, GaAsP



Thin film formation

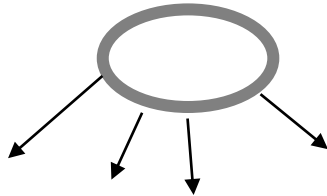
- Thermal oxidation
- CVD
- PVD

Physical Vapor Deposition (**PVD**)

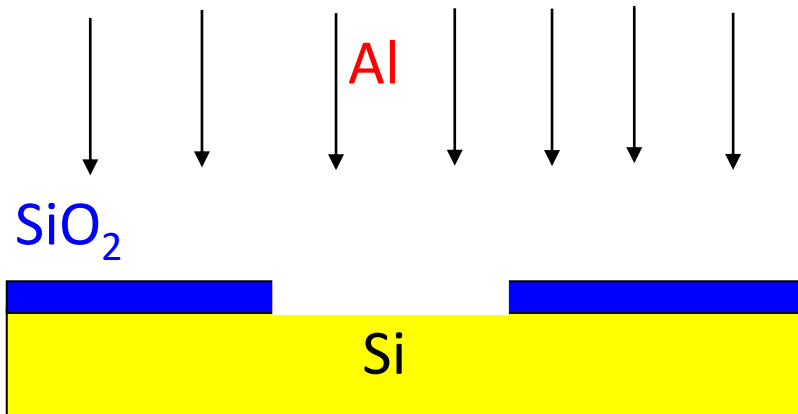
- No chemical reaction involved
 - **Evaporation**
 - **Sputtering**
 - ...
- Used to form **metal films** or **metal oxide films**, such as
 - Al
 - HfO₂
 - ...

Physical Vapor Deposition - **Evaporation**

Al ring



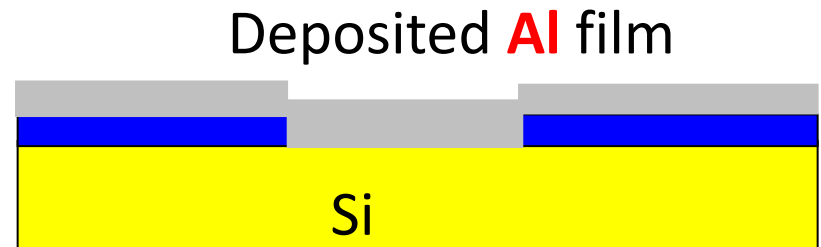
Evaporation Al
($T_{\text{source}} \gg T_{\text{boiling}}$ of Al , **700°C**)



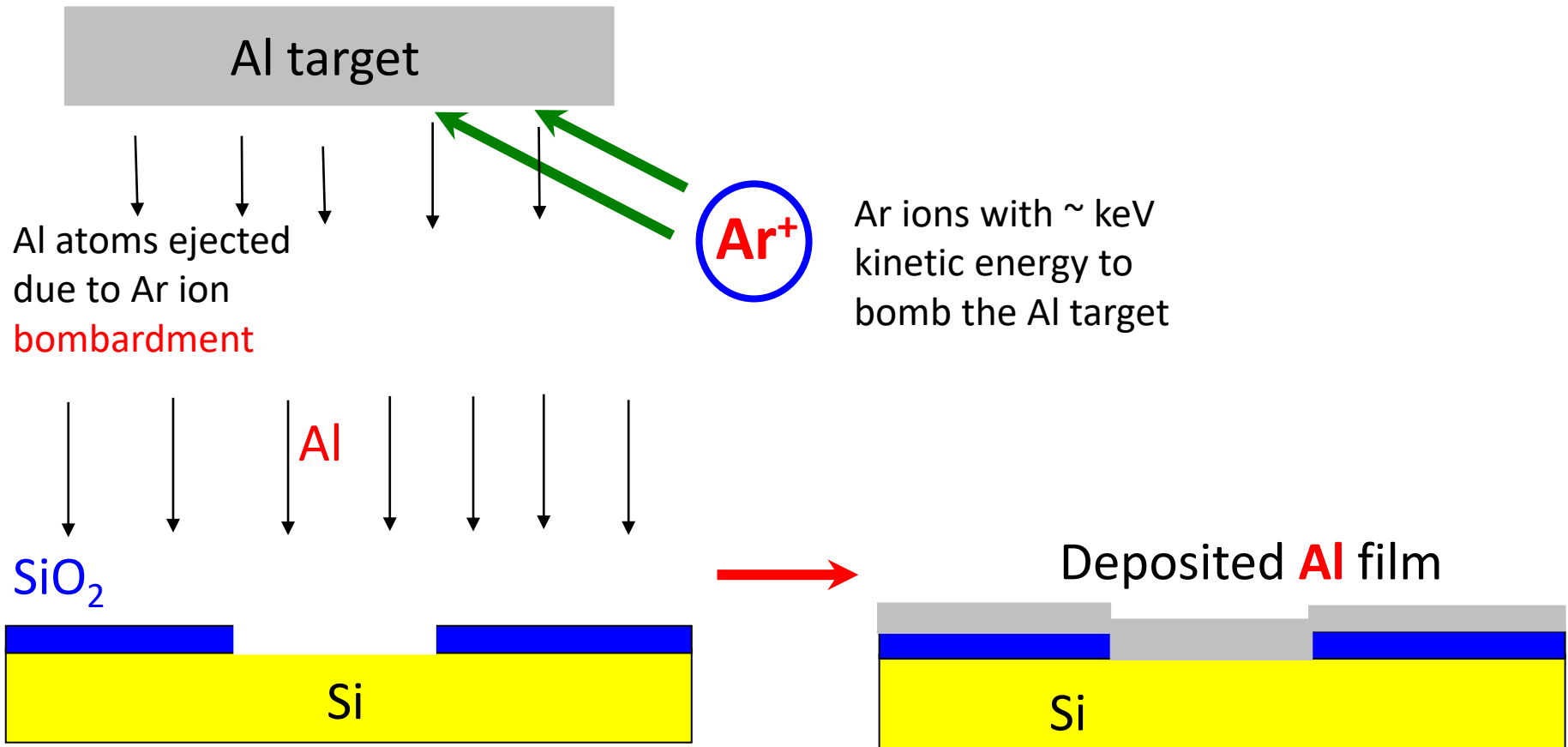
Boiling point

H₂O: 100°C

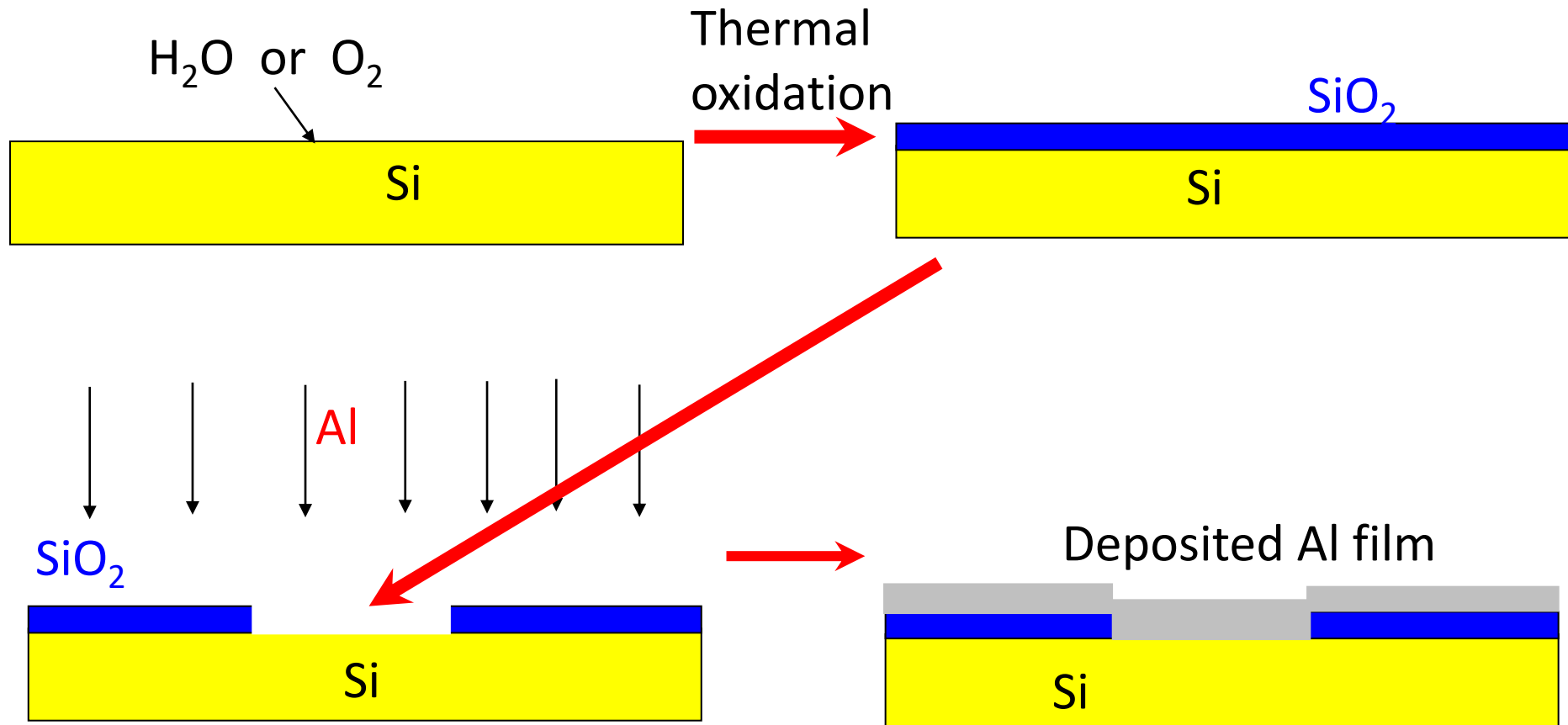
Al: 660°C



Physical Vapor Deposition - Sputtering



Physical Vapor Deposition - Sputtering



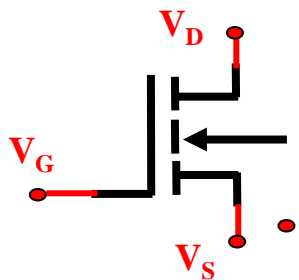
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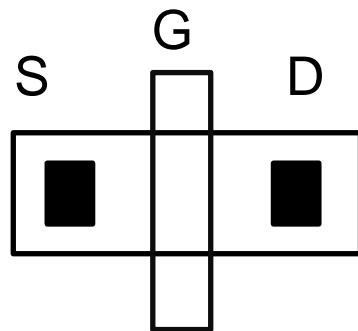


Photolithography & Etching

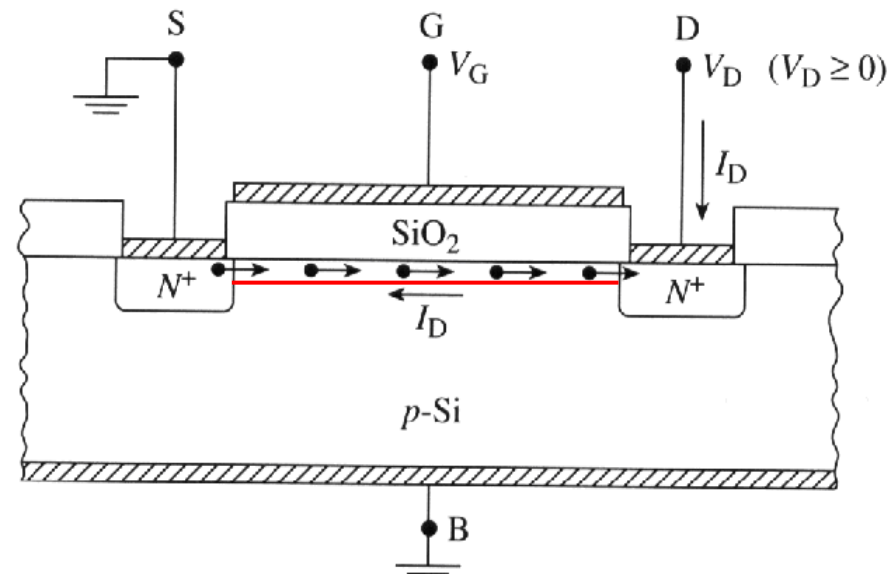
- 1: Glass photomask (mask)
- 2: Apply photoresist (coating)
- 3: UV exposure
- 4: Development
- 5: Etching



Circuit(电路符号)



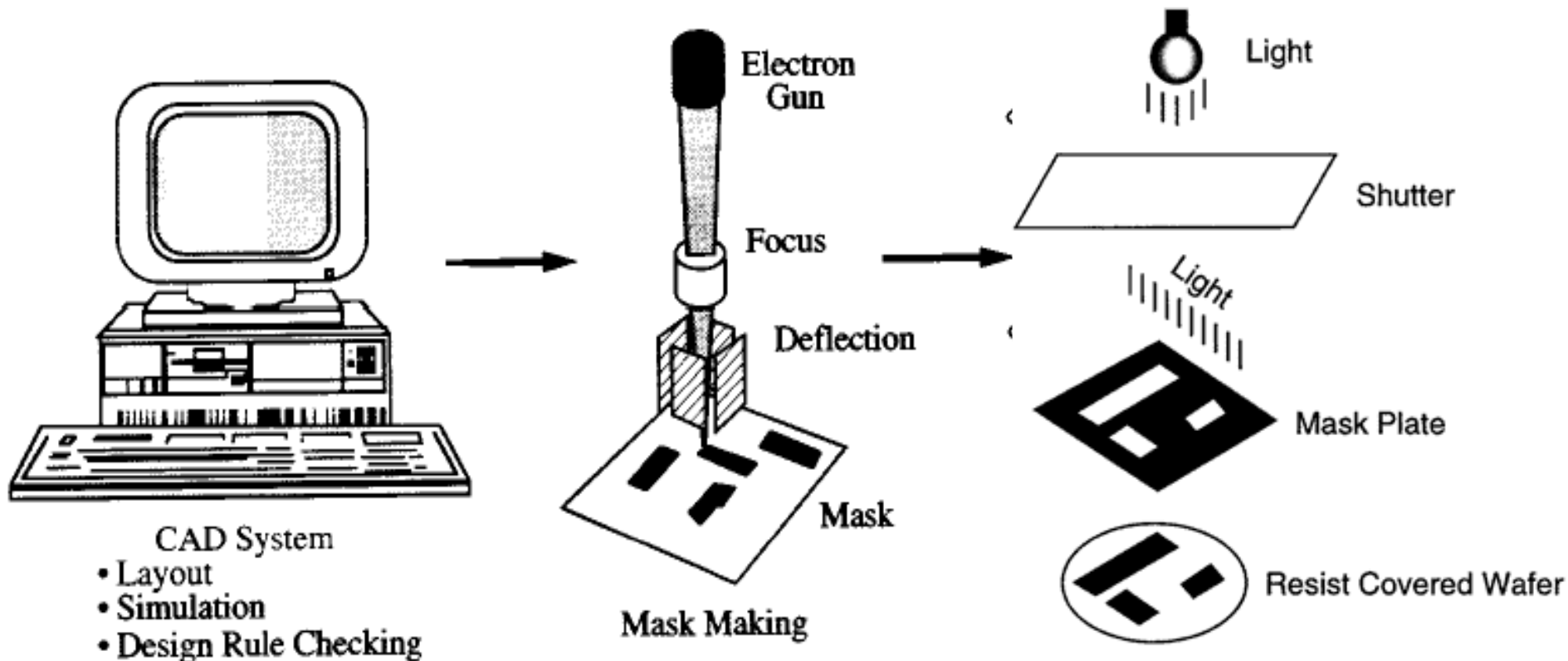
Layout(版图)



Photolithographic process

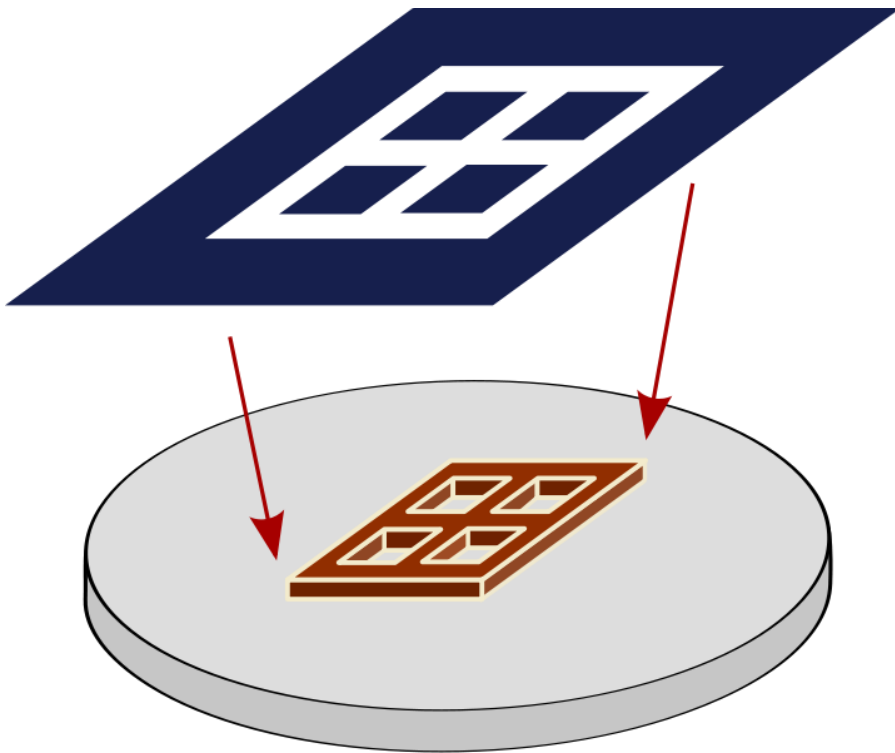
Design => Mask => Wafer

The process of using UV (Ultraviolet) light to transfer patterns from a glass mask onto a surface of the Si wafer.

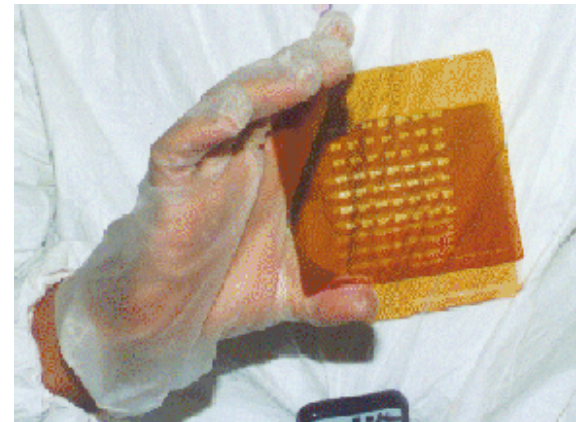
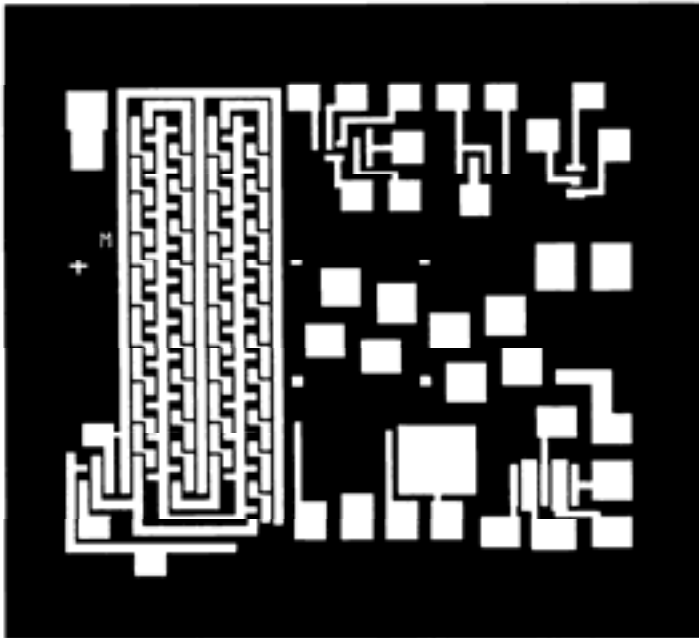
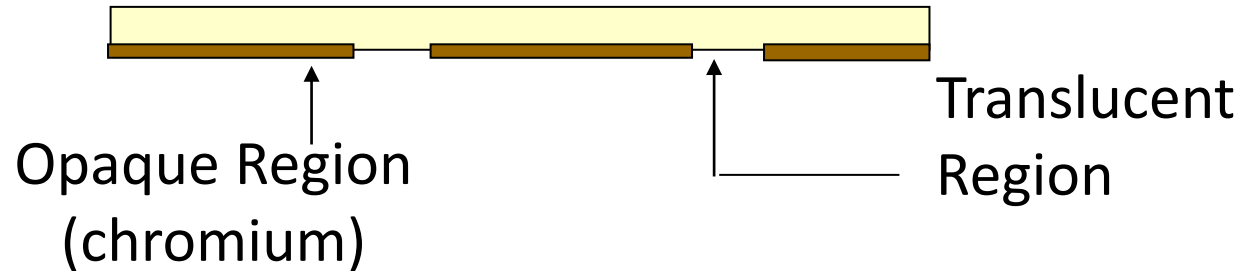


The photolithographic process

- The process of using UV (Ultraviolet) light to transfer patterns from a glass mask onto a surface of the Si wafer.



1. Glass Photomask (mask)



- One mask for **each lithography level** in process

Photolithography & Etching

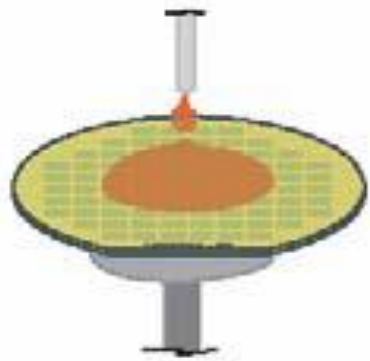
- 1: Glass photomask (mask)
- **2: Apply photoresist (coating)**
- 3: UV exposure
- 4: Development
- 5: Etching

2. Coating

PR
 SiO_2



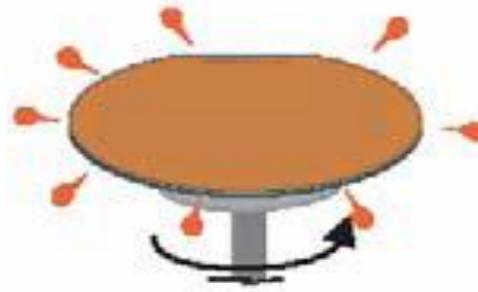
- **Spin coating** process:
 - A controlled volume of **photoresist** is dispensed onto a wafer
 - The wafer is spun at high speed to produce a **uniform photoresist film**.



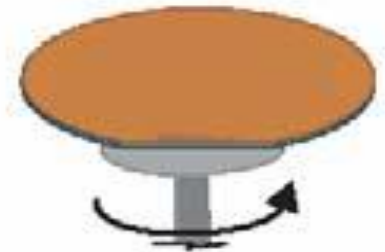
Dispense a controlled amount of photoresist



Allow the photoresist to spread across the wafer



Rapidly ramp up the coater spin speed throwing off excess photoresist



Spin at high speed to form a thin dry film of photoresist

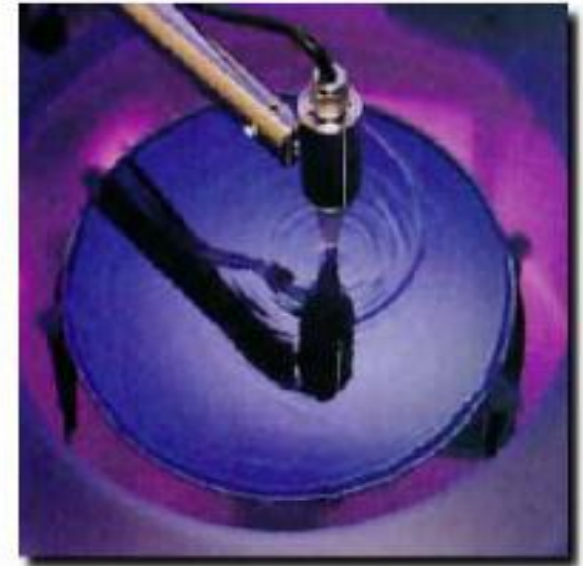
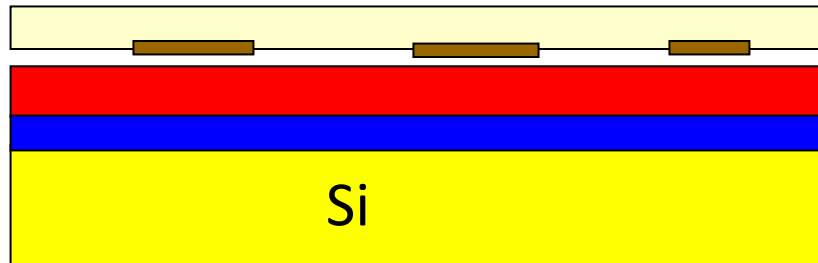
Using the mask

- Preparing the surface:
 - Grow a thin layer of SiO_2
 - Apply on top of the SiO_2 layer a **negative photoresist (PR1)**; thickness around $1\text{ }\mu\text{m}$

mask1

PR1

SiO_2



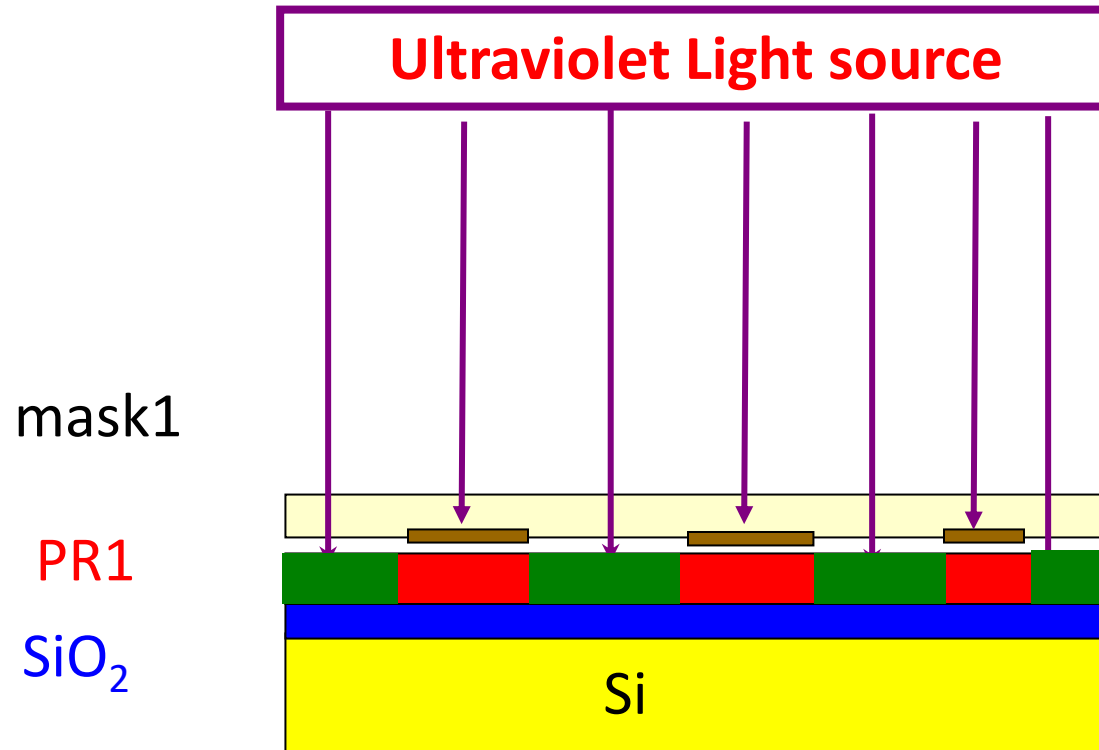
Spin photoresist

- **Place a mask (M1) in close proximity of the wafer**

Photolithography & Etching

- 1: Glass photomask (mask)
- 2: Apply photoresist (coating)
- **3: UV exposure**
- 4: Development
- 5: Etching

3. UV exposure



- After placing M1 in close proximity of the wafer, an project UV light through the mask into PR1;
- Induce changes in the polymer structure and these regions will be insoluble to an organic solvent.
- The regions where the mask was opaque will not be exposed.

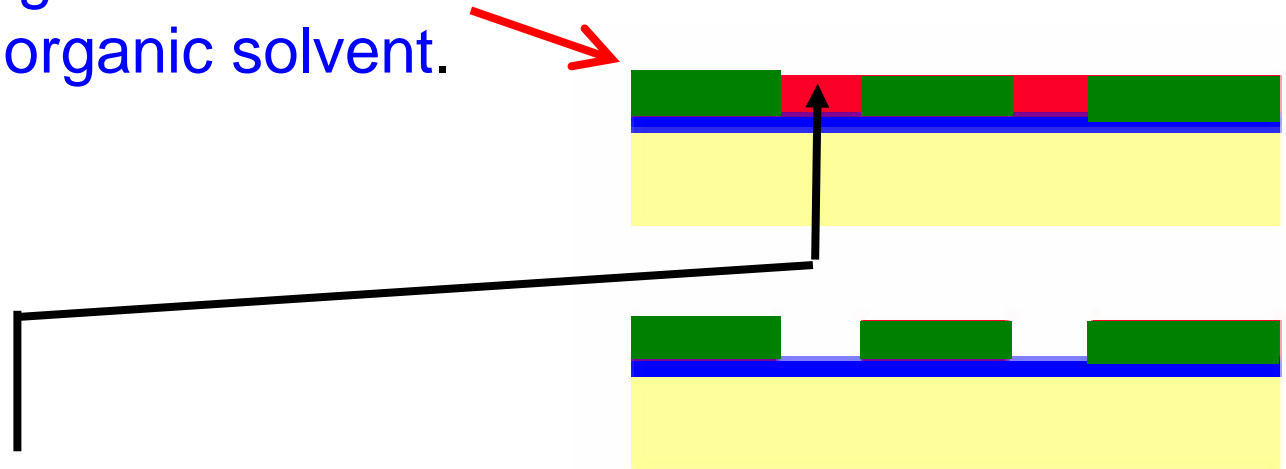
Photolithography & Etching

- 1: Glass photomask (mask)
- 2: Apply photoresist (coating)
- 3: UV exposure
- 4: **Development**
- 5: Etching



4. Development (negative resist)

The **exposed regions** will be **insoluble** to an **organic solvent**.

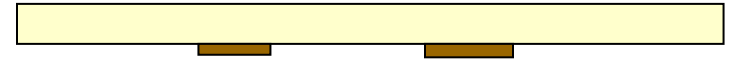


The regions, which is **not exposed**, will be **soluble** to an **organic solvent**

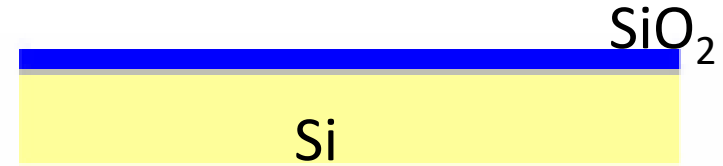
Process of Development

Process steps

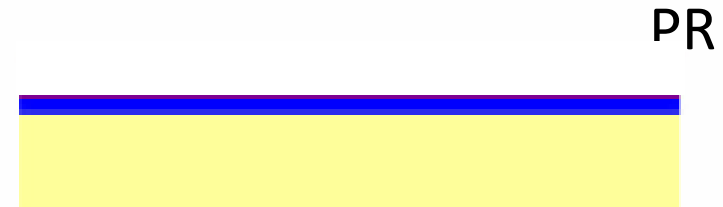
3. UV exp



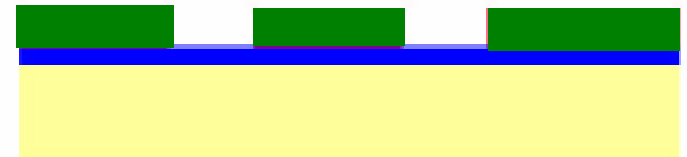
1. thin film



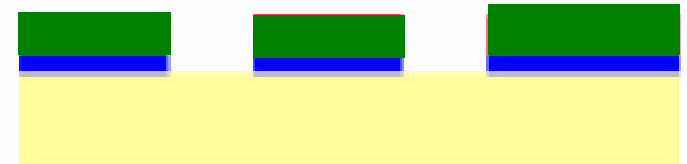
2. coating



4. develop



Etching ↓



Photolithography & Etching

- 1: Glass photomask (mask)
- 2: Apply photoresist (coating)
- 3: UV exposure
- 4: Development
- **5: Etching**

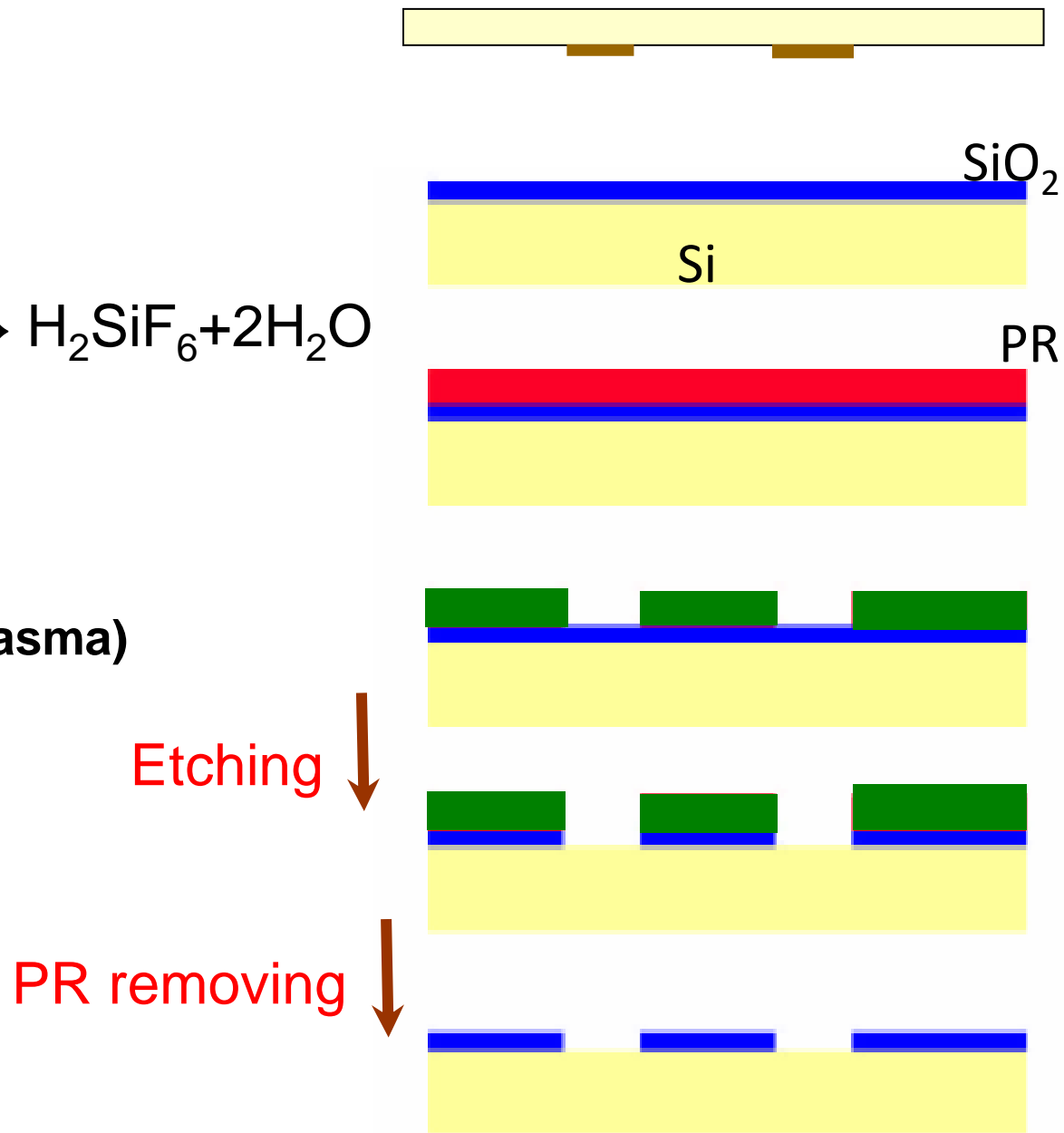
5. Etching

- **Wet Etching**

- $\text{SiO}_2 + 6\text{HF} \rightarrow \text{H}_2\text{SiF}_6 + 2\text{H}_2\text{O}$
(acid solution)

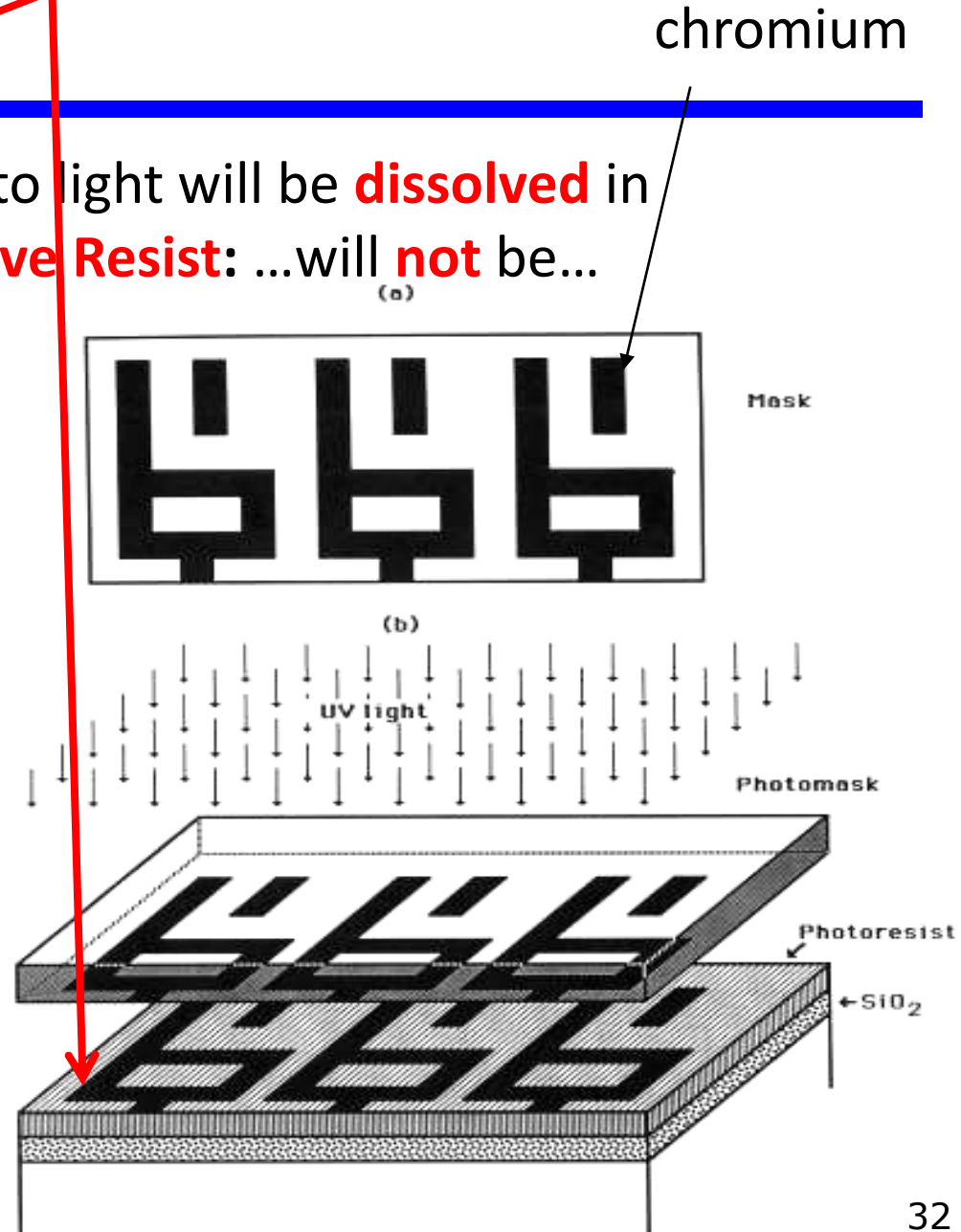
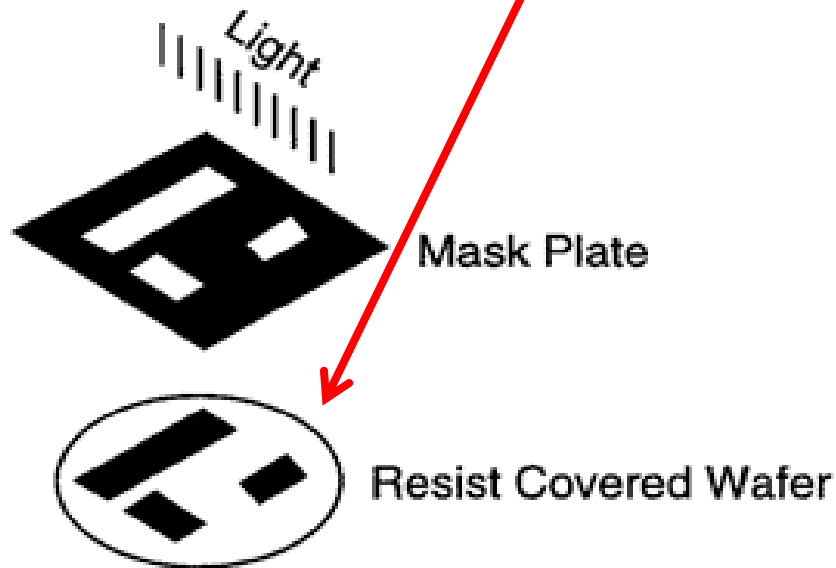
- **Dry Etching**

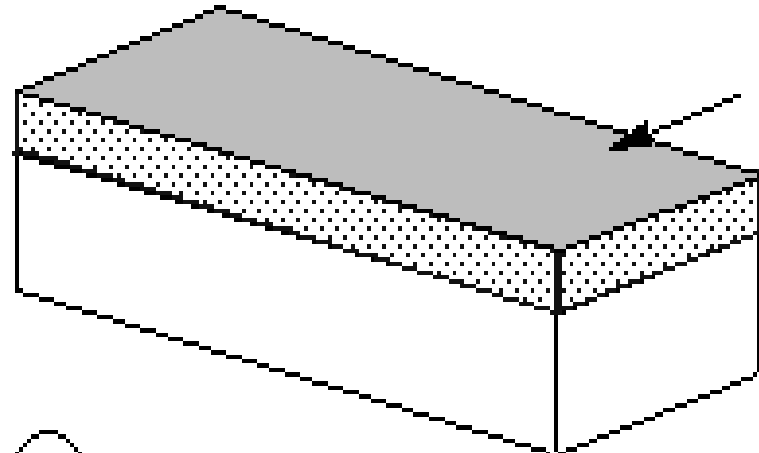
- REI (e.g. CF_4 plasma)



Photoresist

Positive Resist: Part exposed to light will be **dissolved** in development solution. **Negative Resist:** ...will **not** be...





① Photoresist Layering

Positive Photoresist

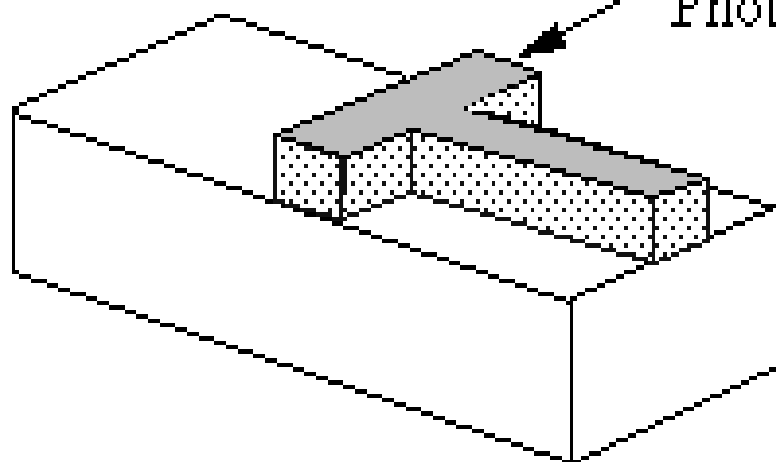
Mask

(clear field)

Exposed Photoresist

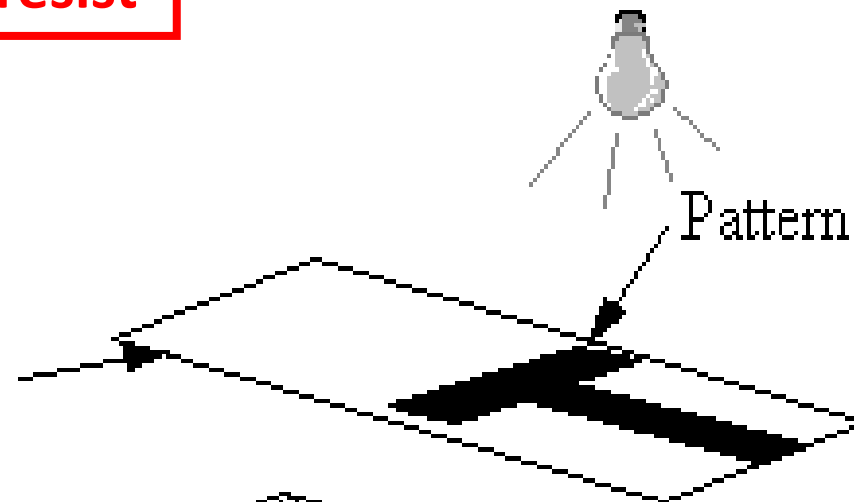
Protected Photoresist

Part **exposed to light** will be **dissolved** in development solution

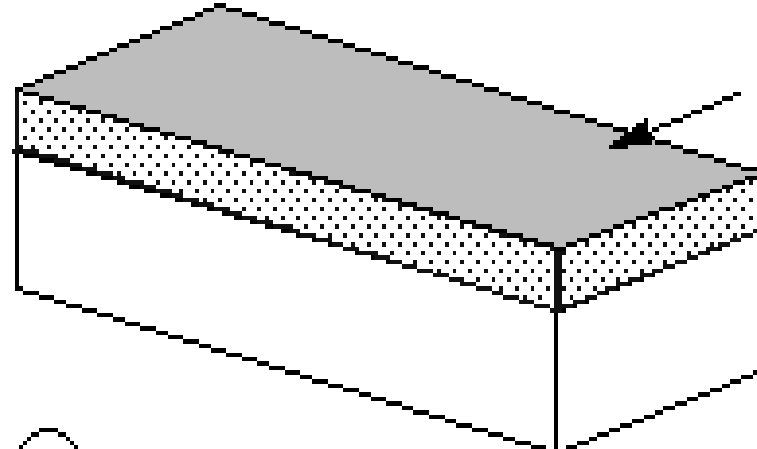


③ Developing

② UV Exposure



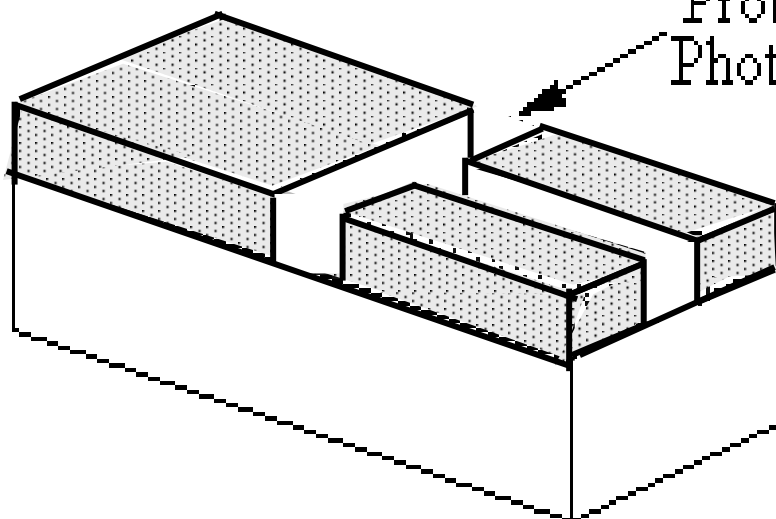
PHOTOMASKING
PROCESS



① Photoresist Layering

Negative Photoresist

Part **exposed** to light will **not** be **dissolved** in development solution

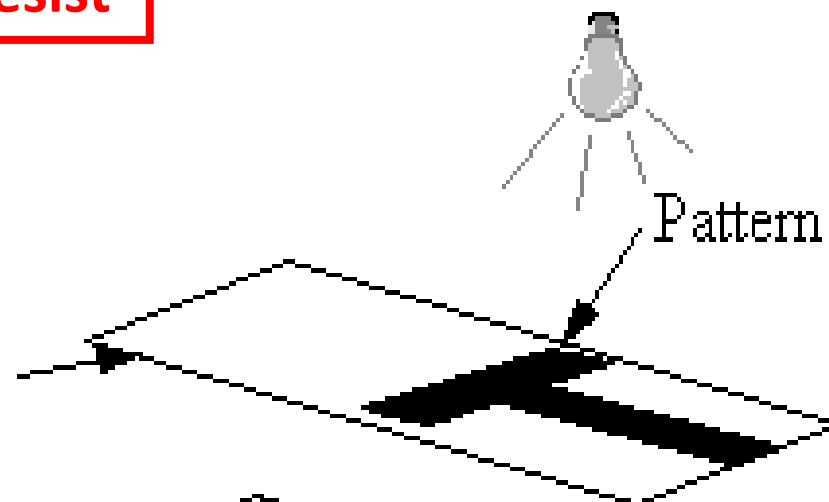


Mask (dark field)

Exposed Photoresist

Protected Photoresist

② UV Exposure

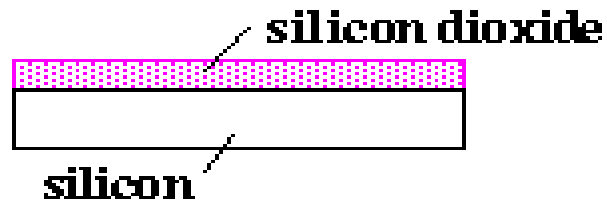


③ Developing

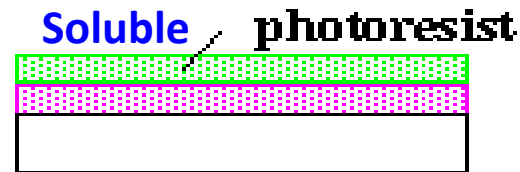
PHOTOMASKING PROCESS

Example 1: **negative** photoresist

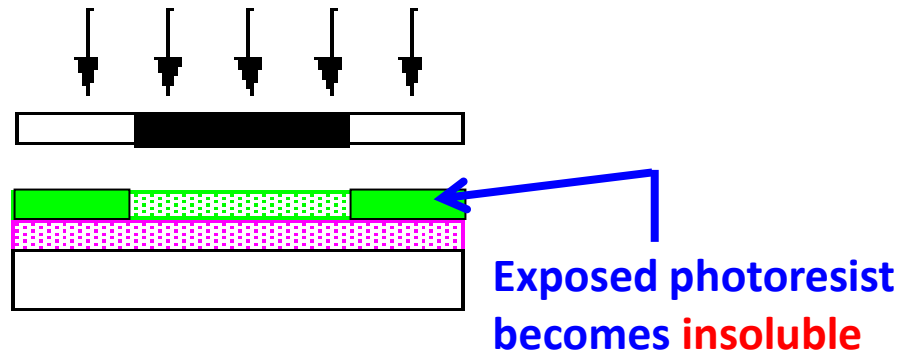
1. Wafer is oxidized



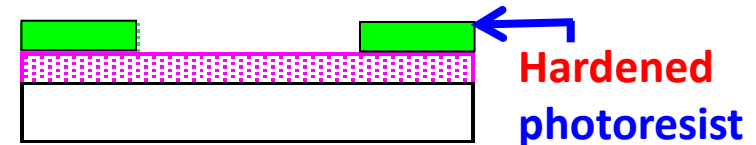
2. Oxidized wafer is covered with photoresist.



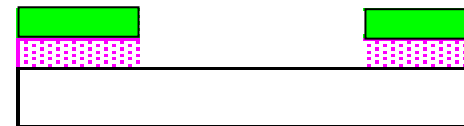
3. Wafer is exposed to UV light through a photomask.



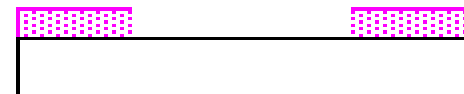
4. Unexposed photoresist is dissolved in developer solution.



5. Oxide now unprotected by photoresist is etched away in hydrofluoric acid. **HF**



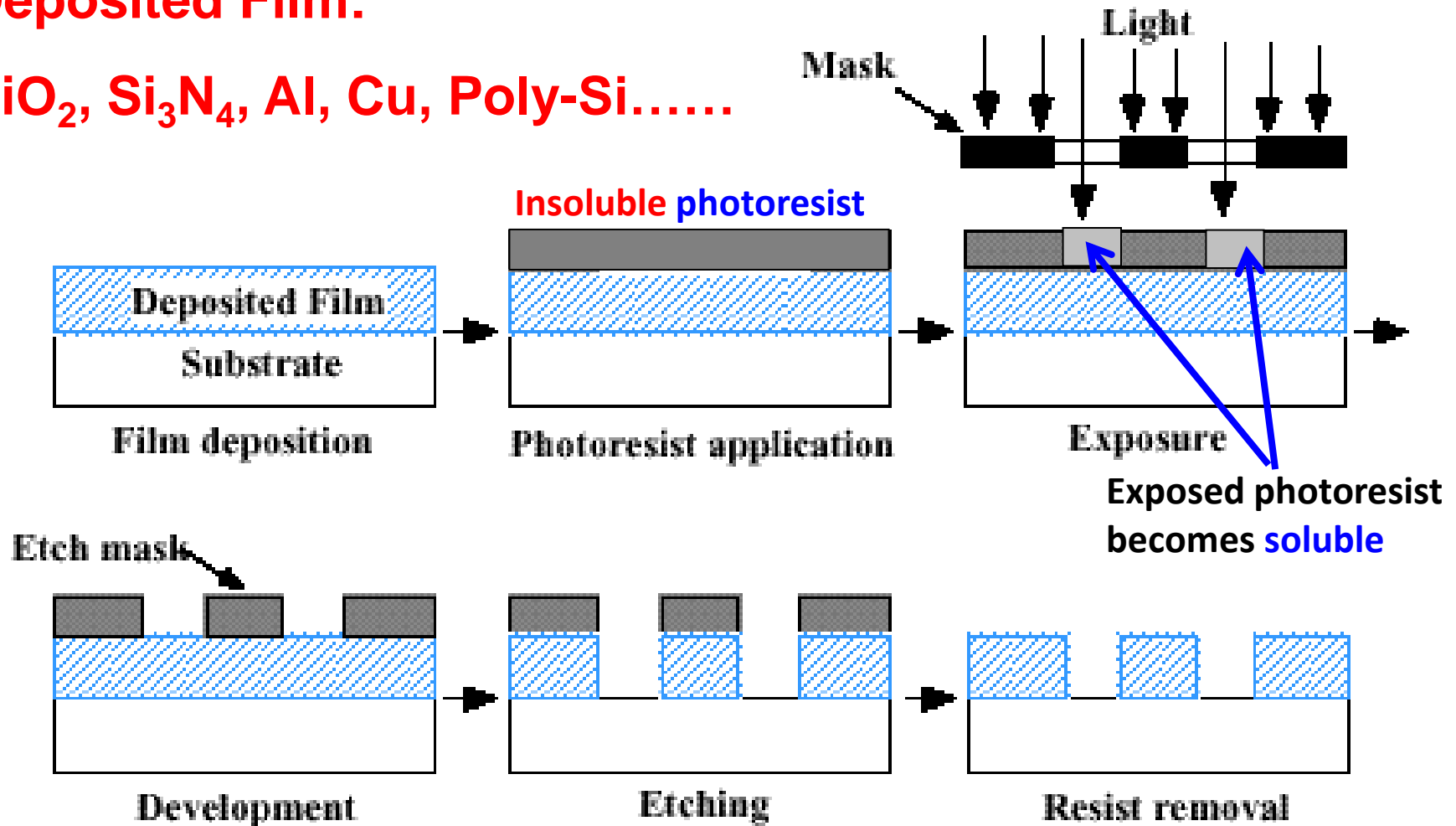
6. The rest of the photoresist is removed. Wafer is now ready for **doping**.



Example 2: **positive** photoresist

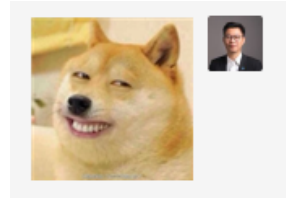
Deposited Film:

SiO_2 , Si_3N_4 , Al, Cu, Poly-Si.....



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- nMOSFET: Fab. and Layout
- nMOSFET: Layout Rules



Doping

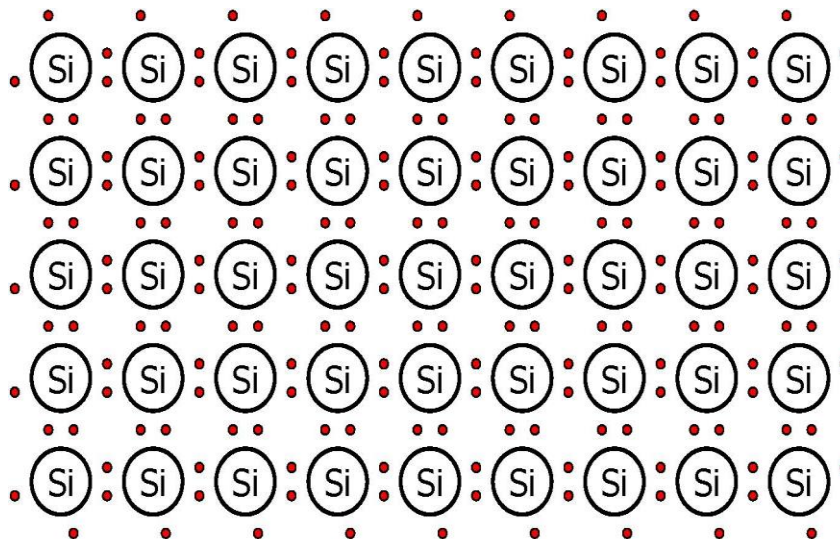
- **Thermal Diffusion**
- **Ion Implantation**

Intrinsic Semiconductor

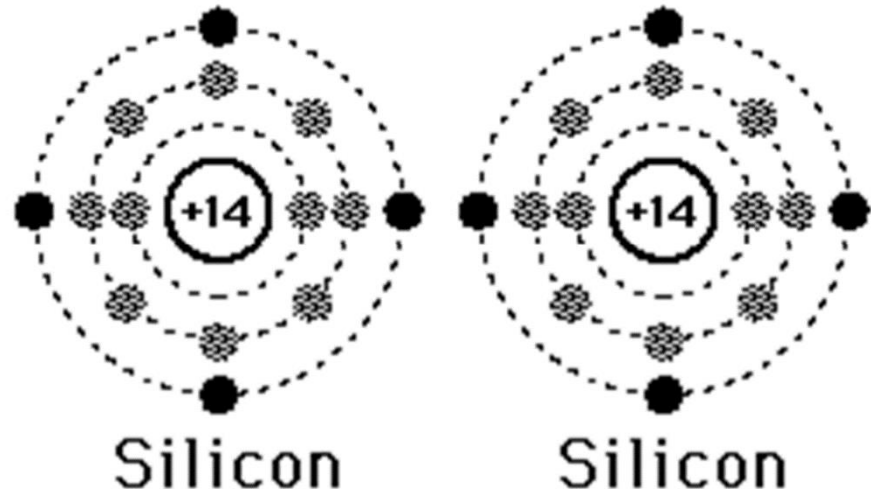
Lecture 3

Silicon has four valence electrons

- It covalently bonds with 4 adjacent atoms in the crystal lattice
- Increasing Temperature Causes Creation of Free Carriers. 10^{10}cm^{-3} free carriers at 23°C (out of $2 \times 10^{23}\text{cm}^{-3}$): Intrinsic Conductivity.

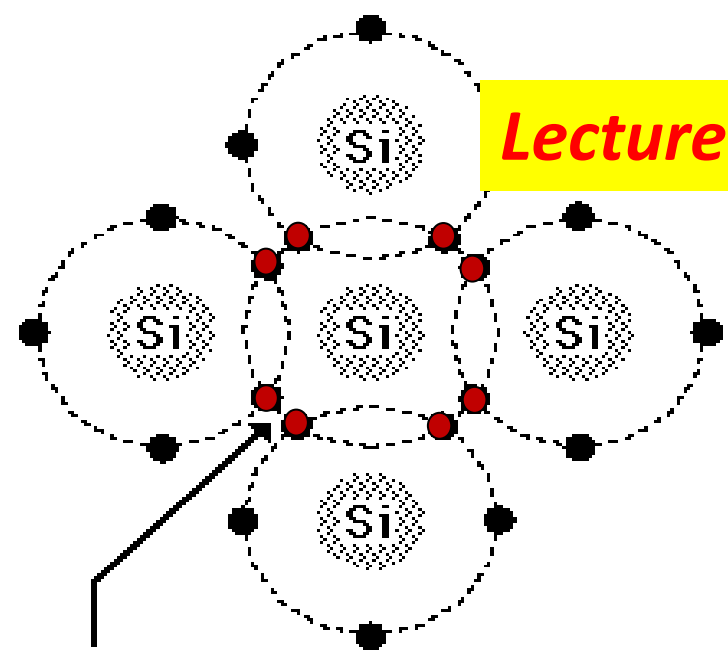
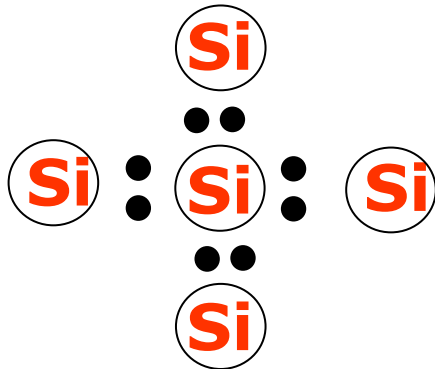


outmost orbit: **4 valence electrons**

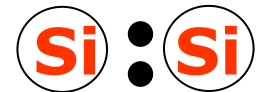


Intrinsic Semiconductors

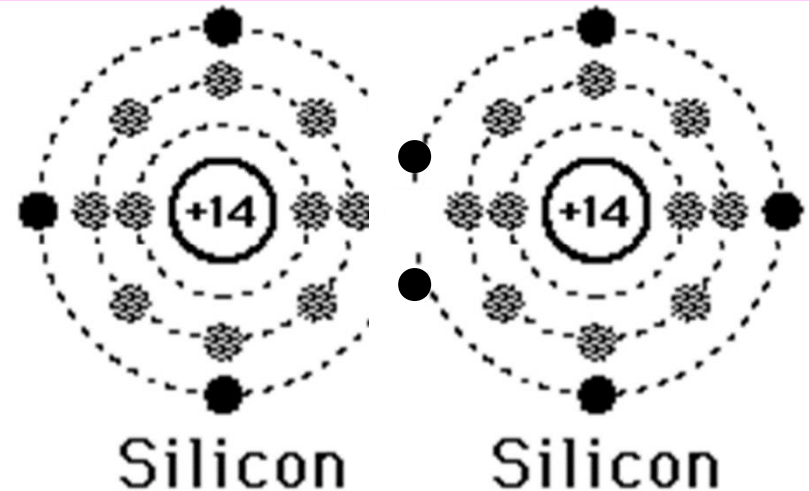
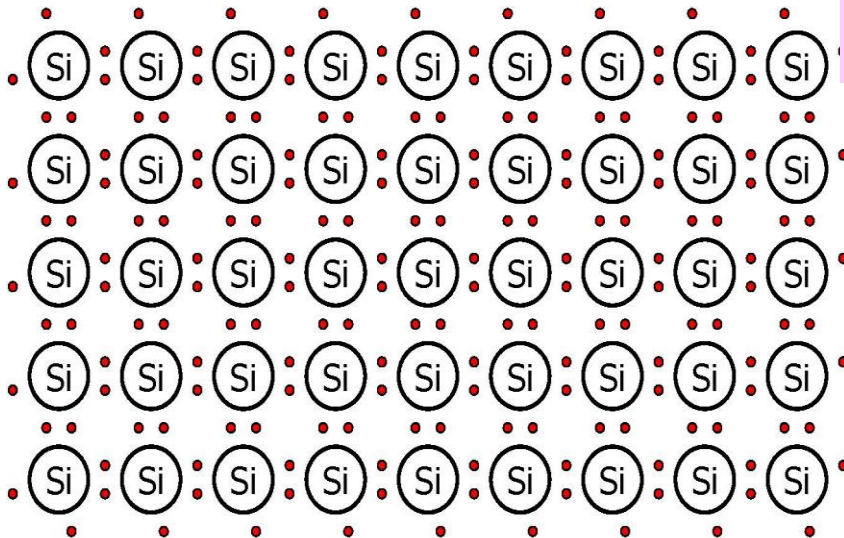
Lecture 3



Shared electrons
of a covalent
bond.



Covalent Bond : shared electrons

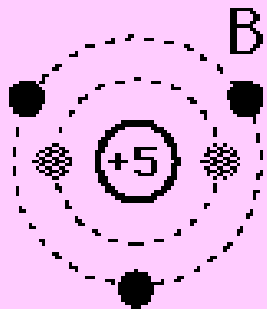


- The addition of a **small** percentage of **foreign atoms** in the regular crystal lattice of silicon or germanium produces dramatic changes in their electrical properties, producing n-type and p-type semiconductors.

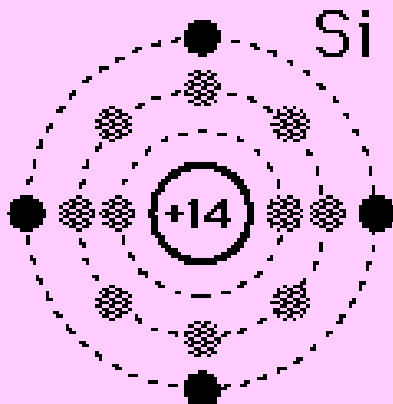
Element periodic table

Lecture 3

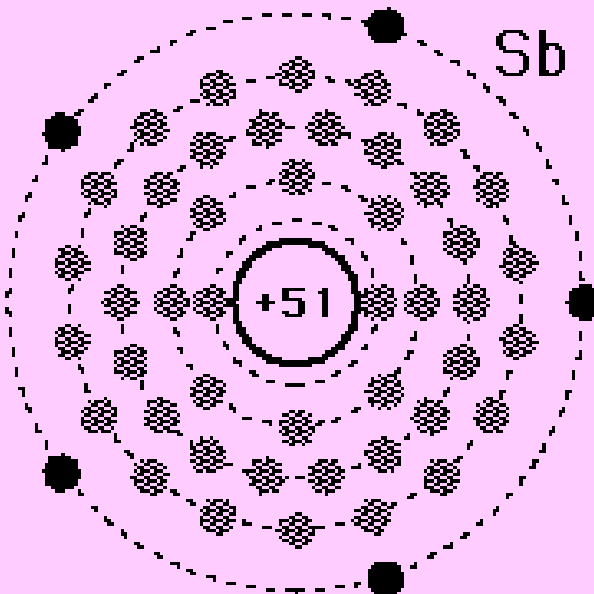
<div> <div>1 IA</div> <div>New Original</div> <div>2 IIA</div> <div>3 IIIB</div> <div>4 IVB</div> <div>5 VB</div> <div>6 VIB</div> <div>7 VIIB</div> <div>8 VIII</div> <div>9 VIII</div> <div>10 VIII</div> <div>11 IB</div> <div>12 IIB</div> <div>13 IIIA</div> <div>14 IVA</div> <div>15 VA</div> <div>16 VIA</div> <div>17 VIIA</div> <div>18 VIIIA</div> </div>																	
<div> <div>Alkali metals</div> <div>Alkaline earth metals</div> <div>Transition metals</div> <div>Lanthanide series</div> <div>Actinide series</div> <div>Poor metals</div> <div>Nonmetals</div> <div>Noble gases</div> <div>C Solid</div> <div>Br Liquid</div> <div>H Gas</div> <div>Tc Synthetic</div> </div>																	
1 H Hydrogen 1.00794	2 He Helium 4.002602																
3 Li Lithium 6.941	4 Be Beryllium 9.012182																
11 Na Sodium 22.989770	12 Mg Magnesium 24.3050																
19 K Potassium	20 Ca Calcium	21 Sc Scandium	22 Ti Titanium	23 V Vanadium	24 Cr Chromium	25 Mn Manganese	26 Fe Iron	27 Co Cobalt	28 Ni Nickel	29 Cu Copper	30 Zn Zinc	31 Ga Gallium	32 Ge Germanium	33 As Arsenic	34 Se Selenium	35 Br Bromine	36 Kr Krypton
37 Rb Rubidium	38 Sr Strontium	39 Y Yttrium	40 Zr Zirconium	41 Nb Niobium	42 Mo Molybdenum	43 Tc Technetium	44 Ru Ruthenium	45 Rh Rhodium	46 Pd Palladium	47 Ag Silver	48 Cd Cadmium	49 In Indium	50 Sn Tin	51 Sb Antimony	52 Te Tellurium	53 I Iodine	54 Xe Xenon
55 Cs Cesium	56 Ba Barium	57 La Lanthanum	58 Ce Cerium	59 Pr Praseodymium	60 Nd Neodymium	61 Pm Promethium	62 Sm Samarium	63 Eu Europium	64 Gd Gadolinium	65 Tb Terbium	66 Dy Dysprosium	67 Ho Holmium	68 Er Erbium	69 Tm Thulium	70 Yb Ytterbium	71 Lu Lutetium	72 Hf Hafnium
87 Fr Francium	88 Ra Radium	89 Ac Actinium	90 Th Thorium	91 Pa Protactinium	92 U Uranium	93 Np Neptunium	94 Pu Plutonium	95 Am Americium	96 Cm Curium	97 Bk Berkelium	98 Cf Californium	99 Es Einsteinium	100 Fm Fermium	101 Md Mendelevium	102 No Nobelium	103 Lr Lawrencium	104 Rf Rutherfordium
119 Uue Ununennium	120 Uuh Unbinilium	121 Uus Untrium	122 Uuo Unbium														



Boron
3 Valence
Electrons



Silicon
4 Valence
Electrons



Antimony (5 Valence)

68 Er Erbium 167.259	69 Tm Thulium 168.93421	70 Yb Ytterbium 173.04	71 Lu Lutetium 174.967
100 Fm Fermium (257)	101 Md Mendelevium (258)	102 No Nobelium (259)	103 Lr Lawrencium (262)

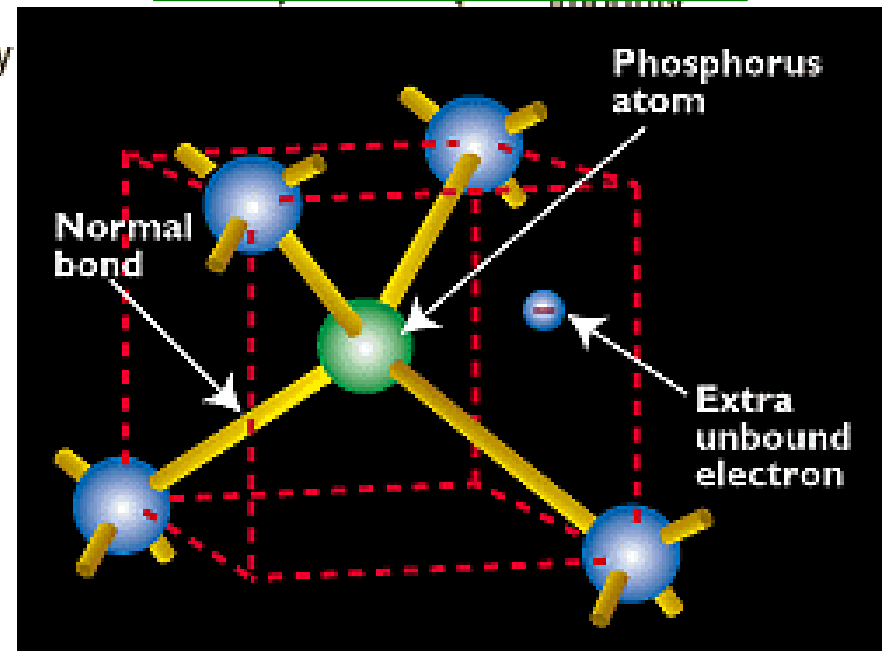
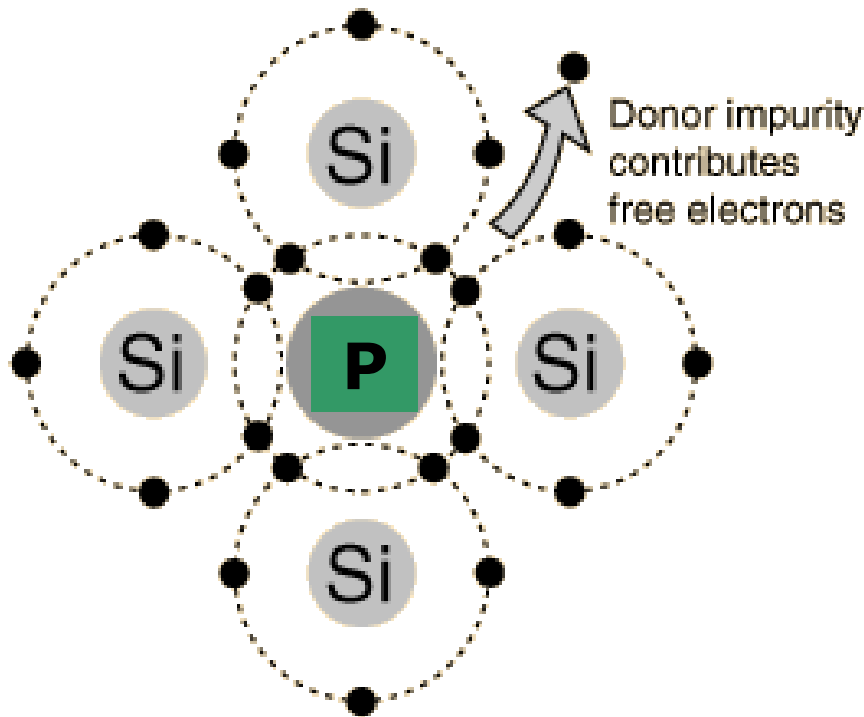
Doping (N type)

Column V elements are donors, e.g. P, As, Sb

By substituting a Si atom with a special impurity atom (**Column V** element), a conduction electron is created.

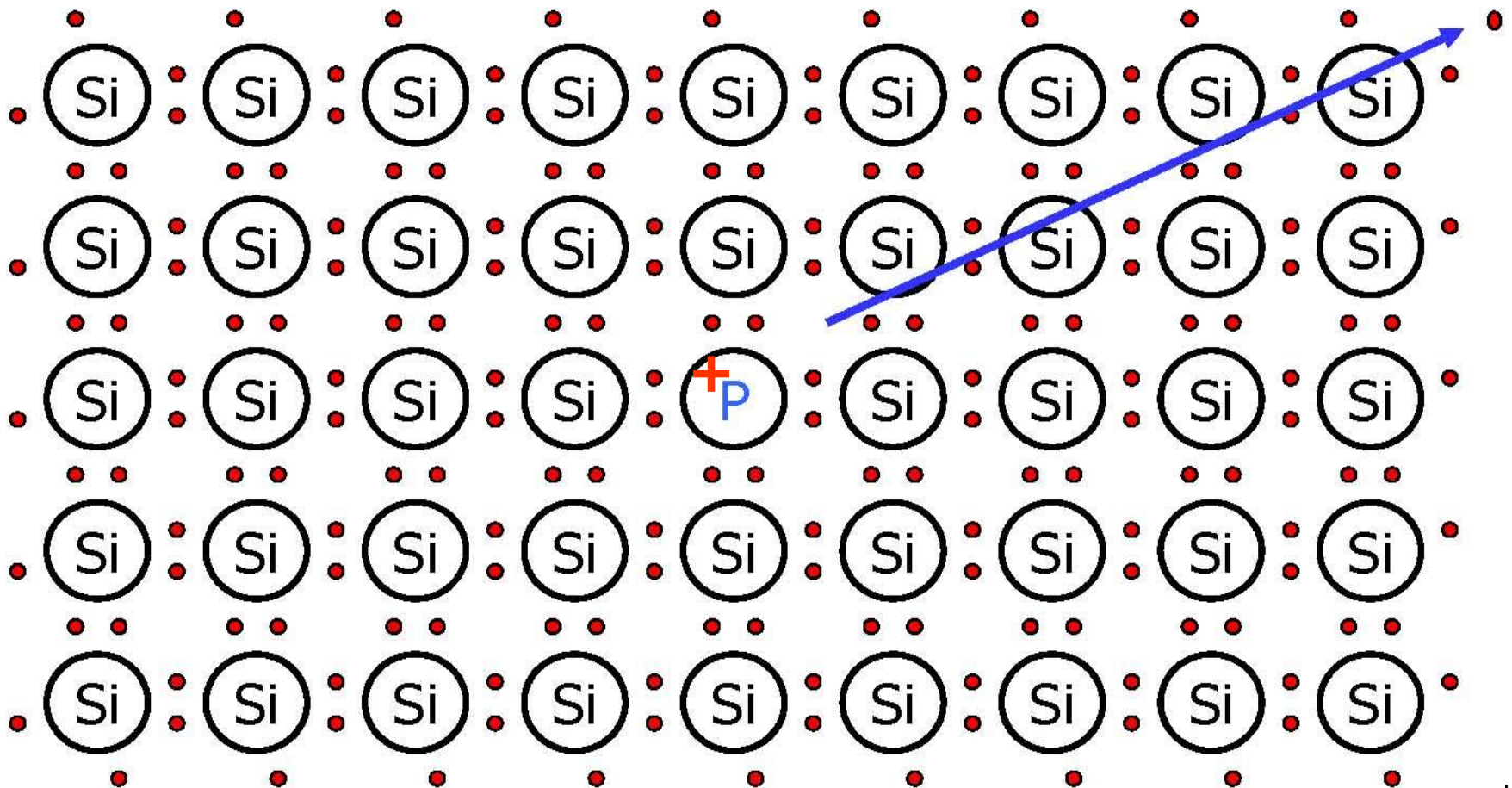
Lecture 3

Donors: P, As, Sb



Phosphorus has 5 valence electrons

- 'Donates' one conduction electron to lattice
- Our substrate has 10^{15}cm^{-3} phosphorus (1 in 10^8)

Free

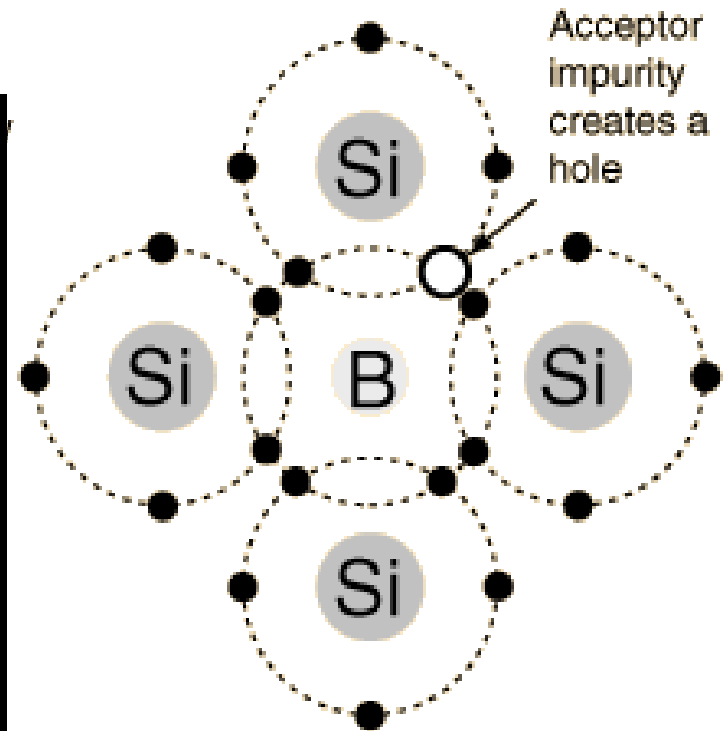
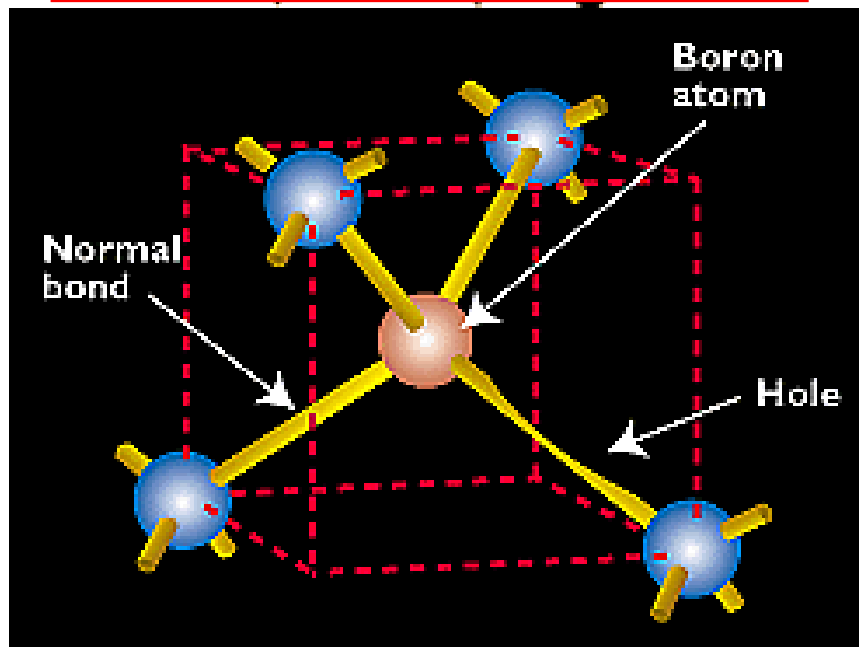
Doping (P type)

Column III elements are acceptors, e.g. B, Al, Ga

By substituting a Si atom with a special impurity atom (**Column III element**), a conduction hole is created.

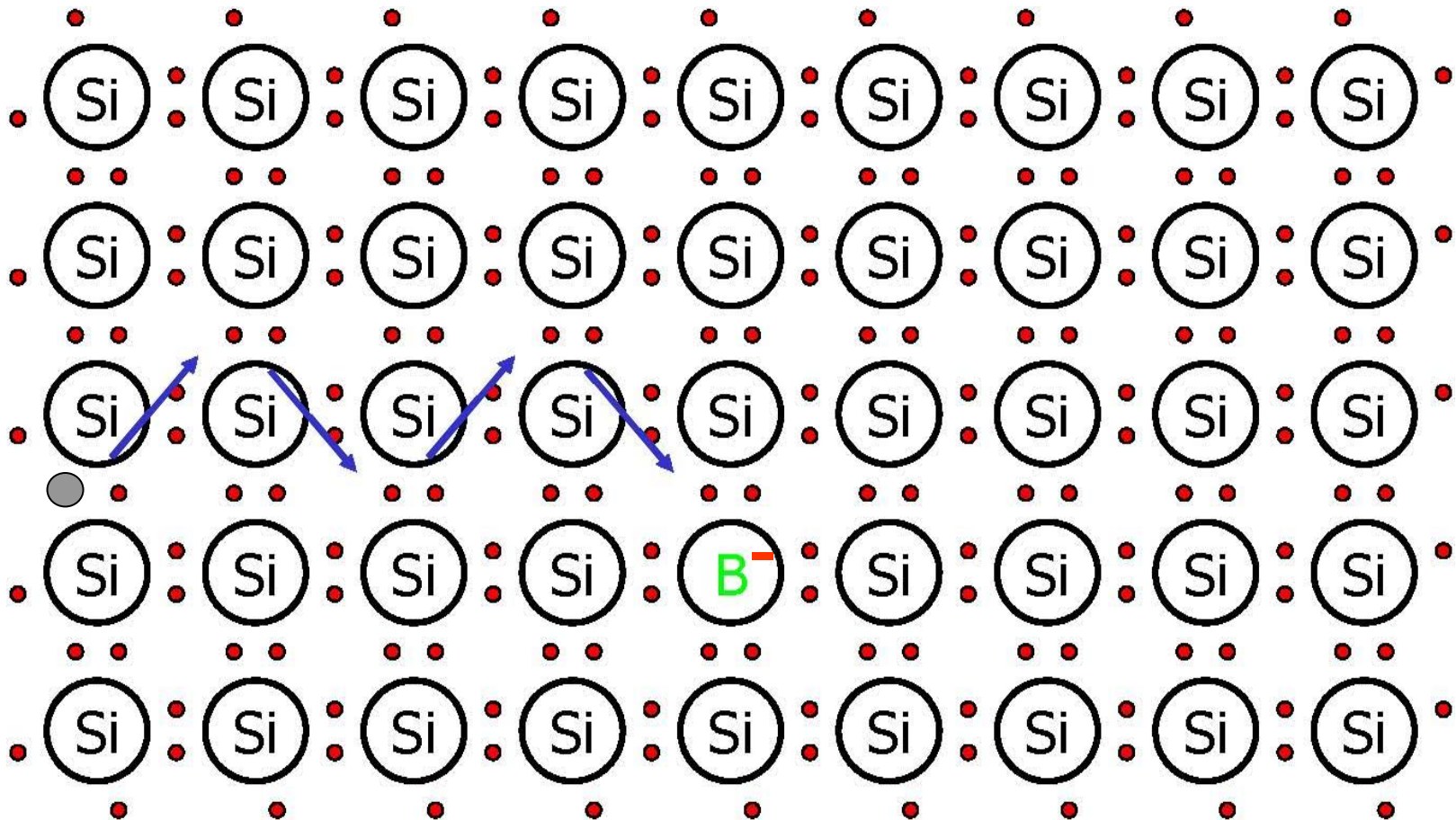
Lecture 3

Acceptors: B, Al, Ga, In

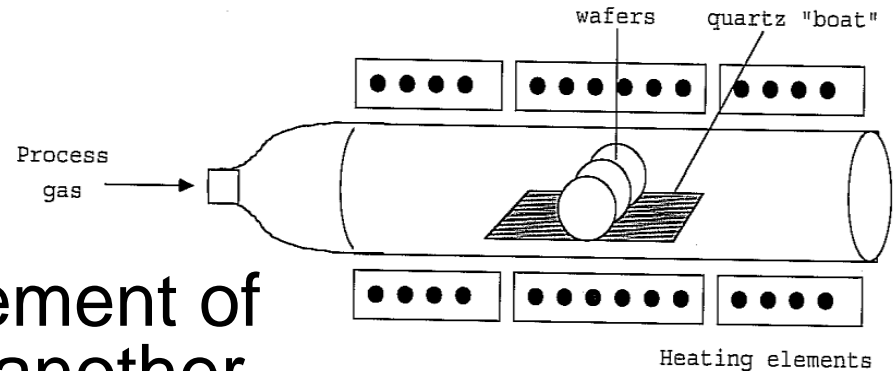


Boron has 3 valence electrons

- 'Accepts' one electron from lattice
- Creates a 'hole'



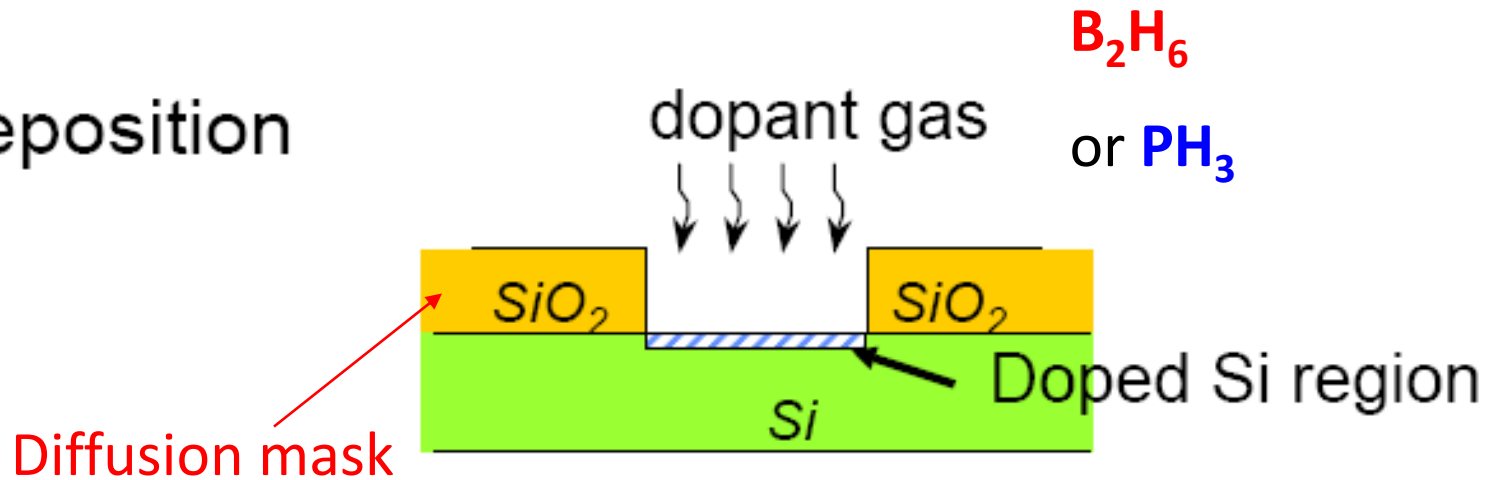
Diffusion



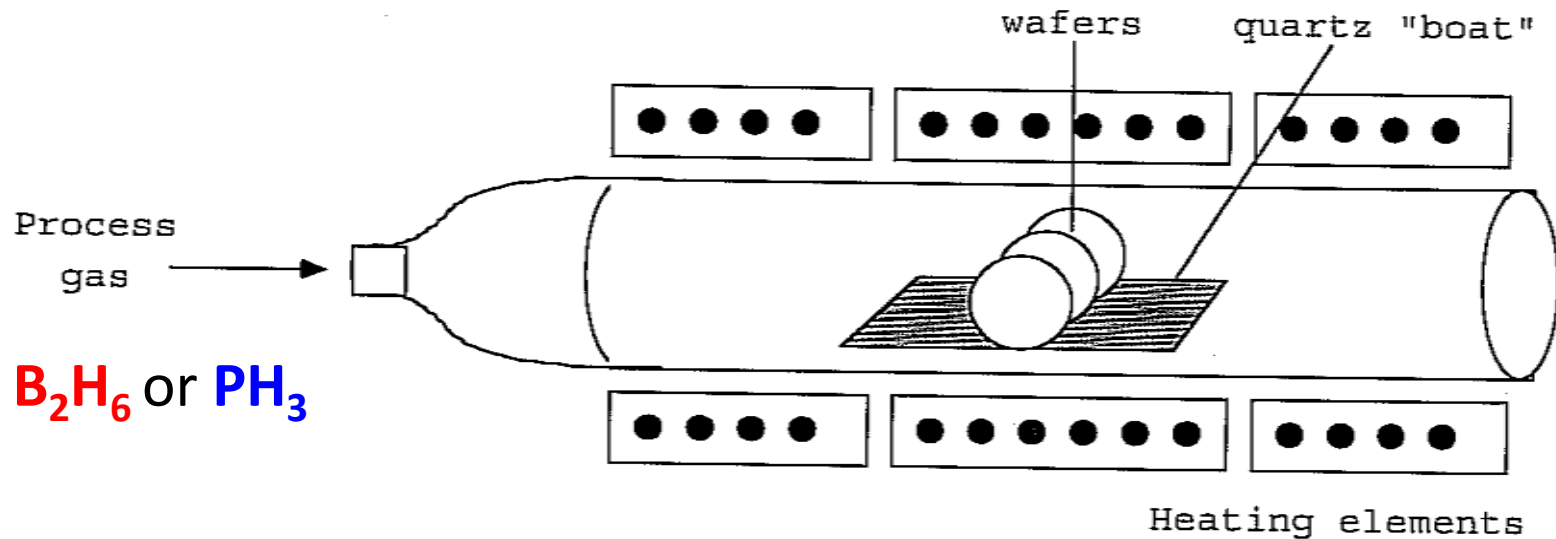
- **Diffusion** is the movement of one material through another from a region of **relatively higher concentration** into a region of **lower concentration**. There are **two steps** to thermal diffusion:
 - **Pre-deposition**
 - **Drive-in**
- **Dopant Diffusion Sources**
 - Gas Source: AsH_3 , PH_3 , B_2H_6

Dopant Diffusion

(1) Predeposition

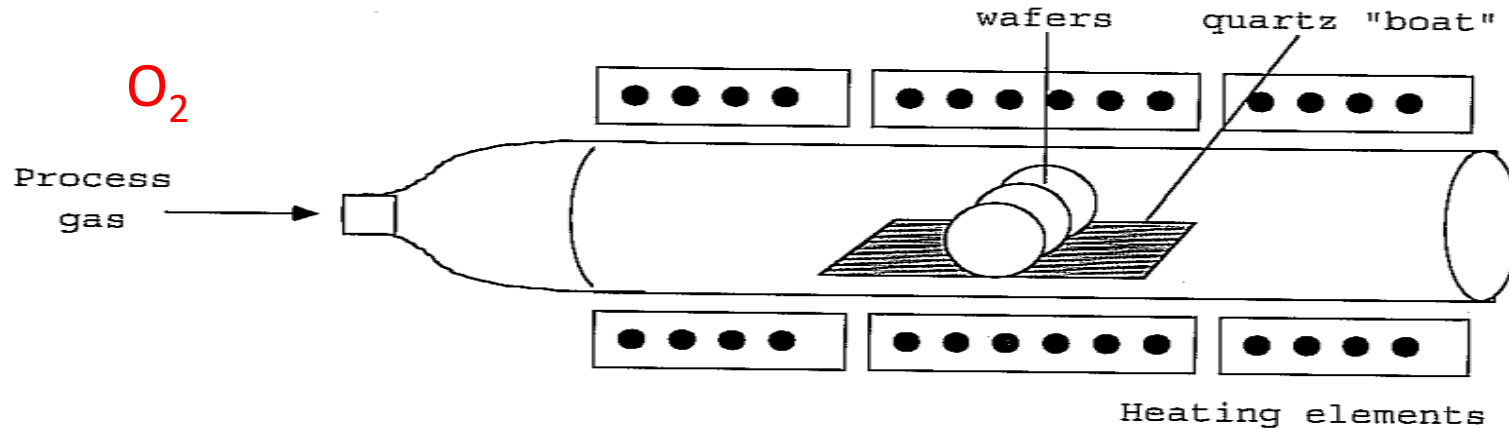


Furnace



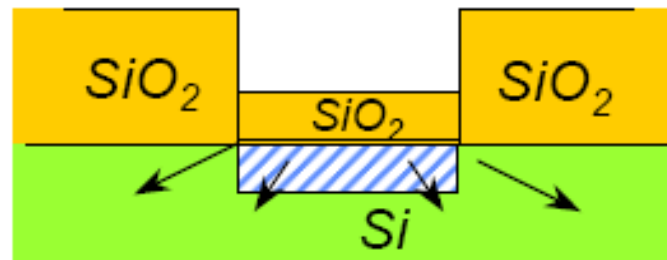
Dopant Diffusion

Furnace



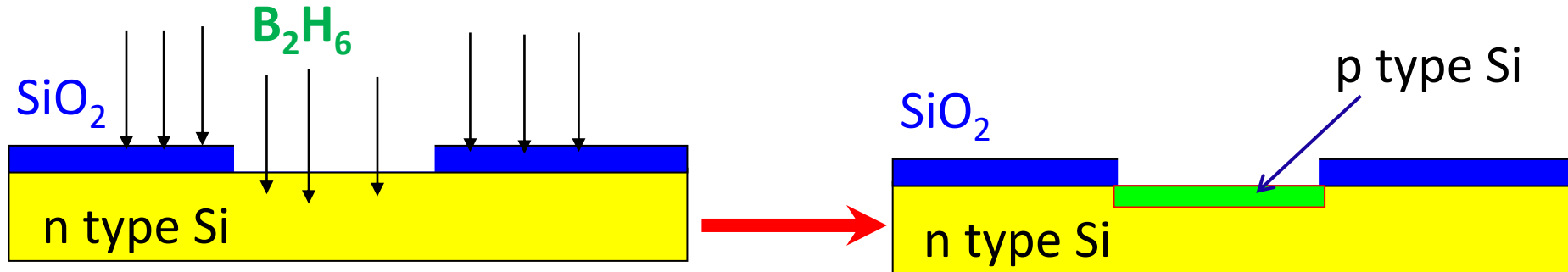
(2) Drive-in

Turn off dopant gas
or seal surface with oxide



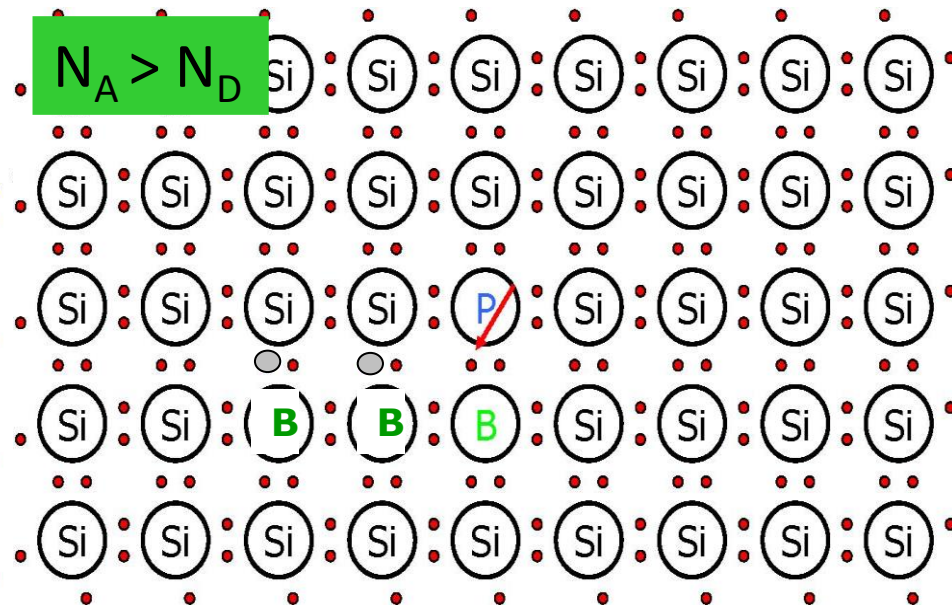
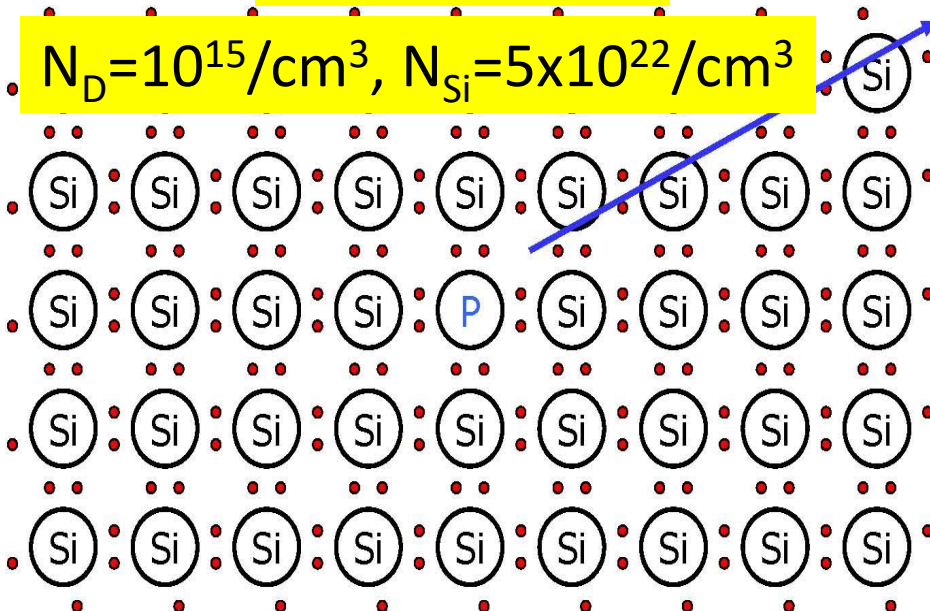
Note: Predeposition by diffusion can also be replaced by a shallow implantation step.

Thermal Diffusion Example



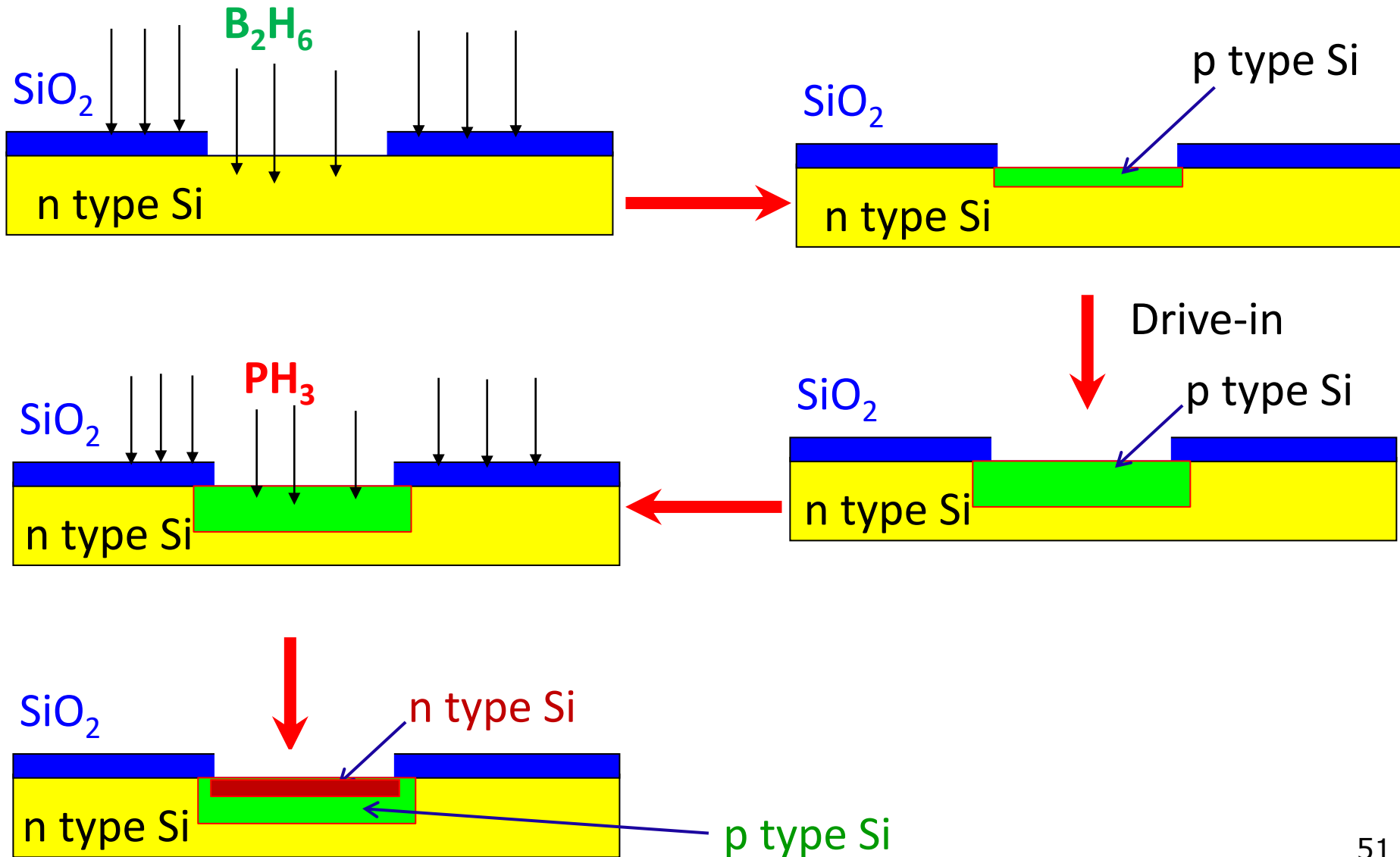
Yellow region

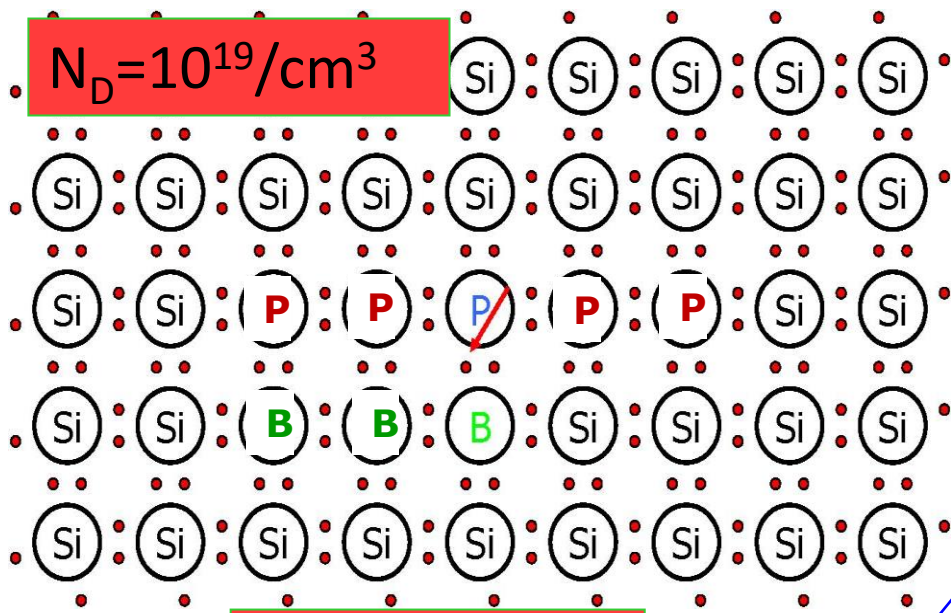
$$N_D = 10^{15}/\text{cm}^3, N_{\text{Si}} = 5 \times 10^{22}/\text{cm}^3$$



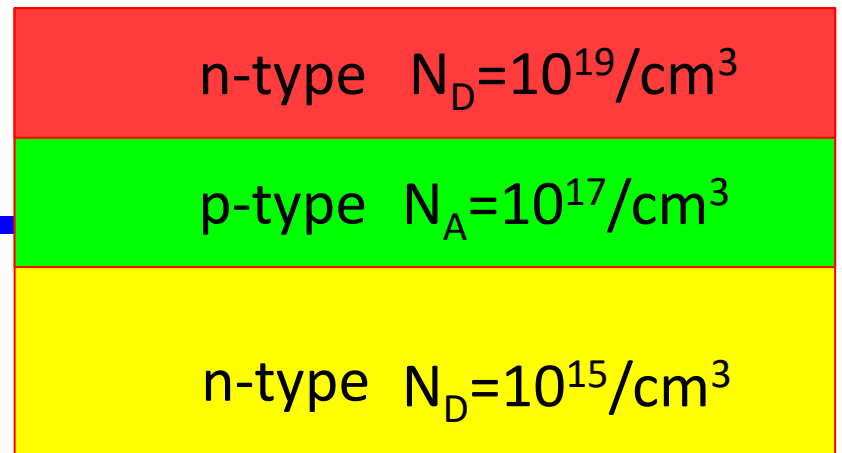
Green region

Thermal Diffusion Example

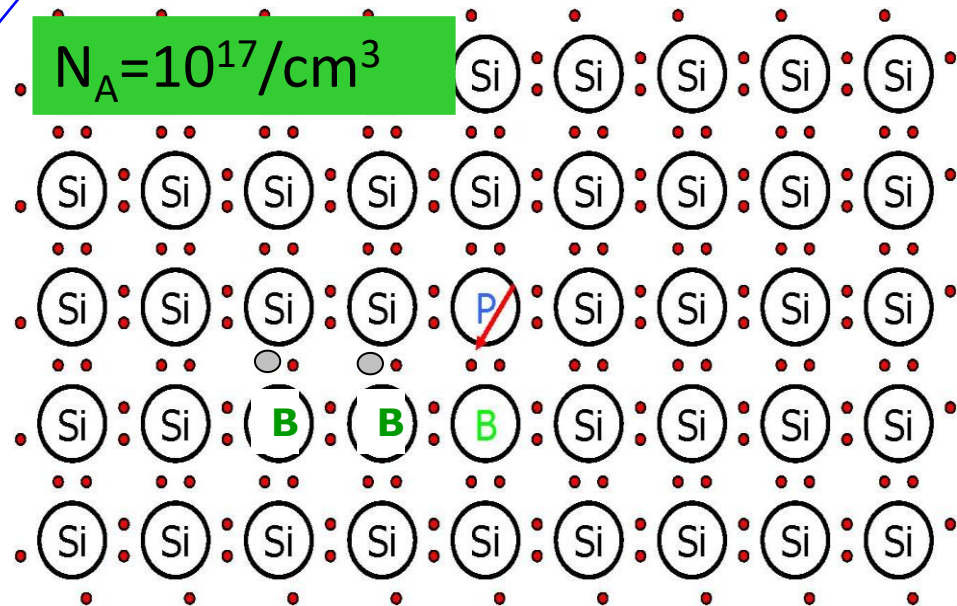




Brown region

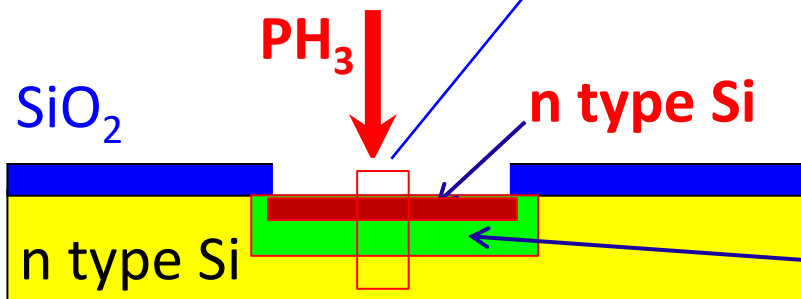


SiO_2



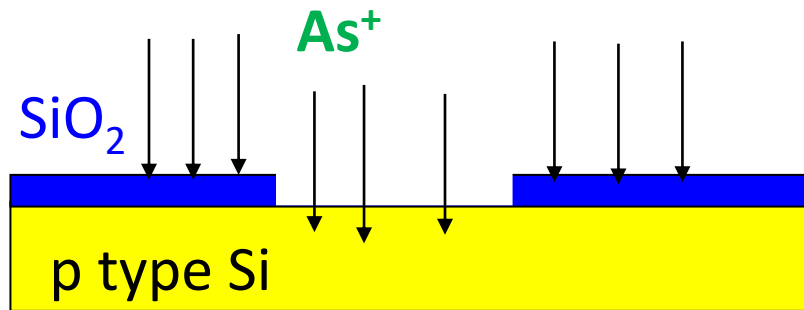
Green region

SiO_2

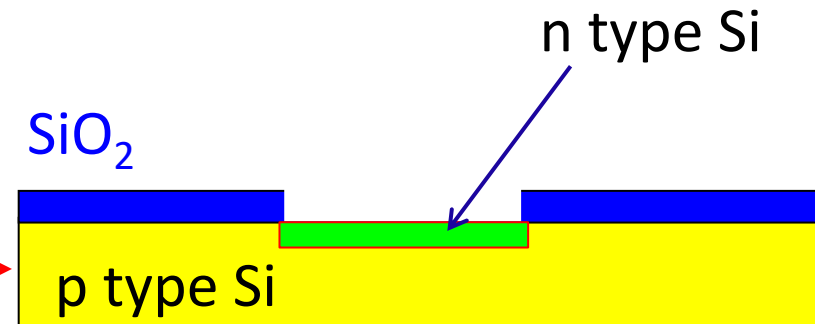


p type Si

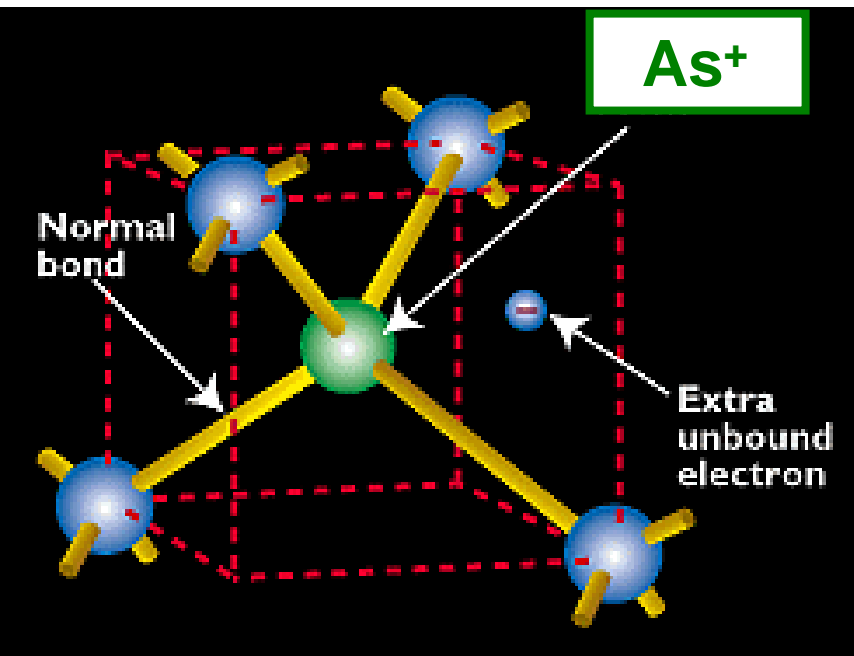
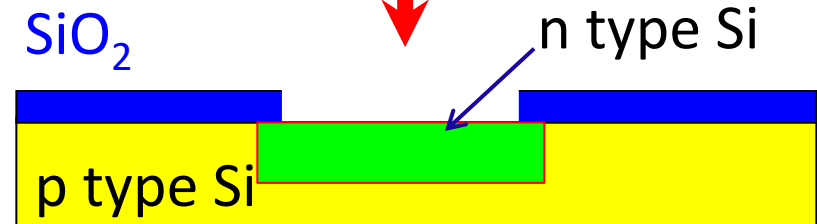
Ion Implantation



As⁺ with kinetic energy



annealing



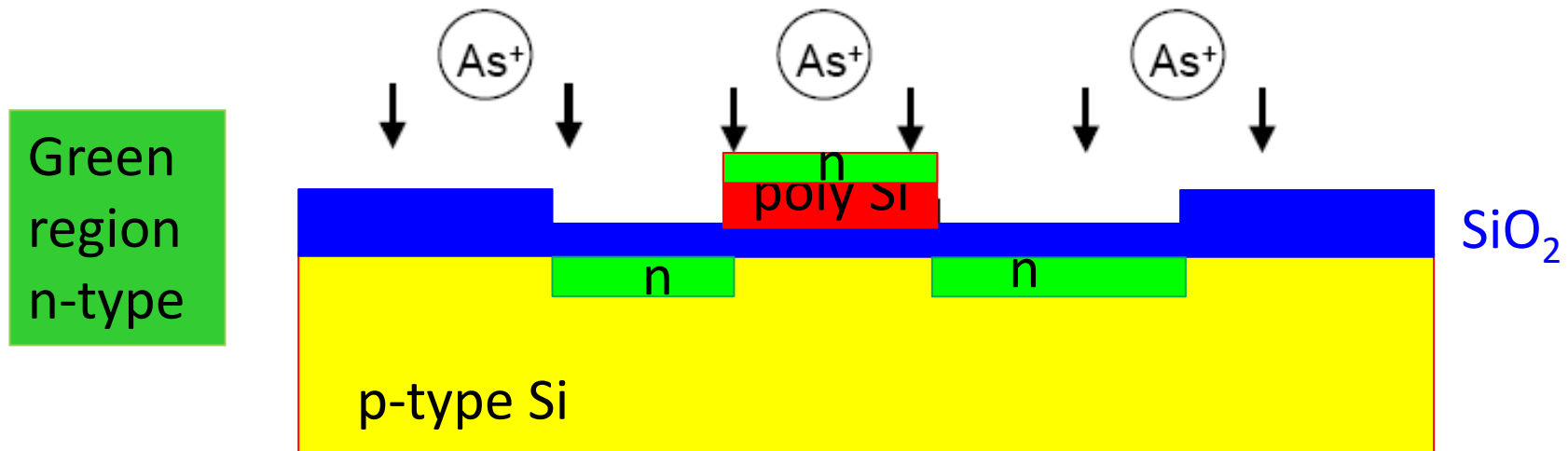
Implantation causes

- (1) damaged region
- (2) non-substitutional location

Advantages of Ion Implantation

- Precise control of dose and depth profile
- Low-temp. process (can use photoresist as mask)
- Wide selection of masking materials
e.g. photoresist, oxide, poly-Si, metal
- Less sensitive to surface cleaning procedures
- Excellent lateral dose uniformity (< 1% variation across 12" wafer)

Application example: self-aligned MOSFET source/drain regions



Annealing (Drive-in)

Implantation causes

(1) damaged region and disorder cluster

(2) non-substitutional location

To activate the implanted ions and to restore material properties, the semiconductor must be **annealed**.

Next week:

Fab. Tech. examples