Lecture 6

of

EEE201

CMOS Digital Integrated Circuits

Department of Electrical & Electronic Engineering

Xi'an Jiaotong-Liverpool University (XJTLU)

Tuesday, 24th October 2023

- **CMOS IC Fabrication**
  - connection between physical layout & structure
  - NMOS process & LOCOS
  - process steps in CMOS

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IC Fabrication & Layout Linkage

(why care about fabrication in layout design)

- In **integrated circuit** (**IC**) design, certain degree of knowledge about the **IC fabrication** will be helpful in creating the **physical layout**:
  - understand the **device structures** resulting from the **physical layout design** (i.e. knowing what you will get, especially by visualising the 2D or 3D structure)
  - understand better the **layout design rules** (from fabrication constraints)
  - avoid certain pitfalls in the circuits while designing the **physical layout**
  - obtain somewhat better device and circuit performance with optimised **IC layout**

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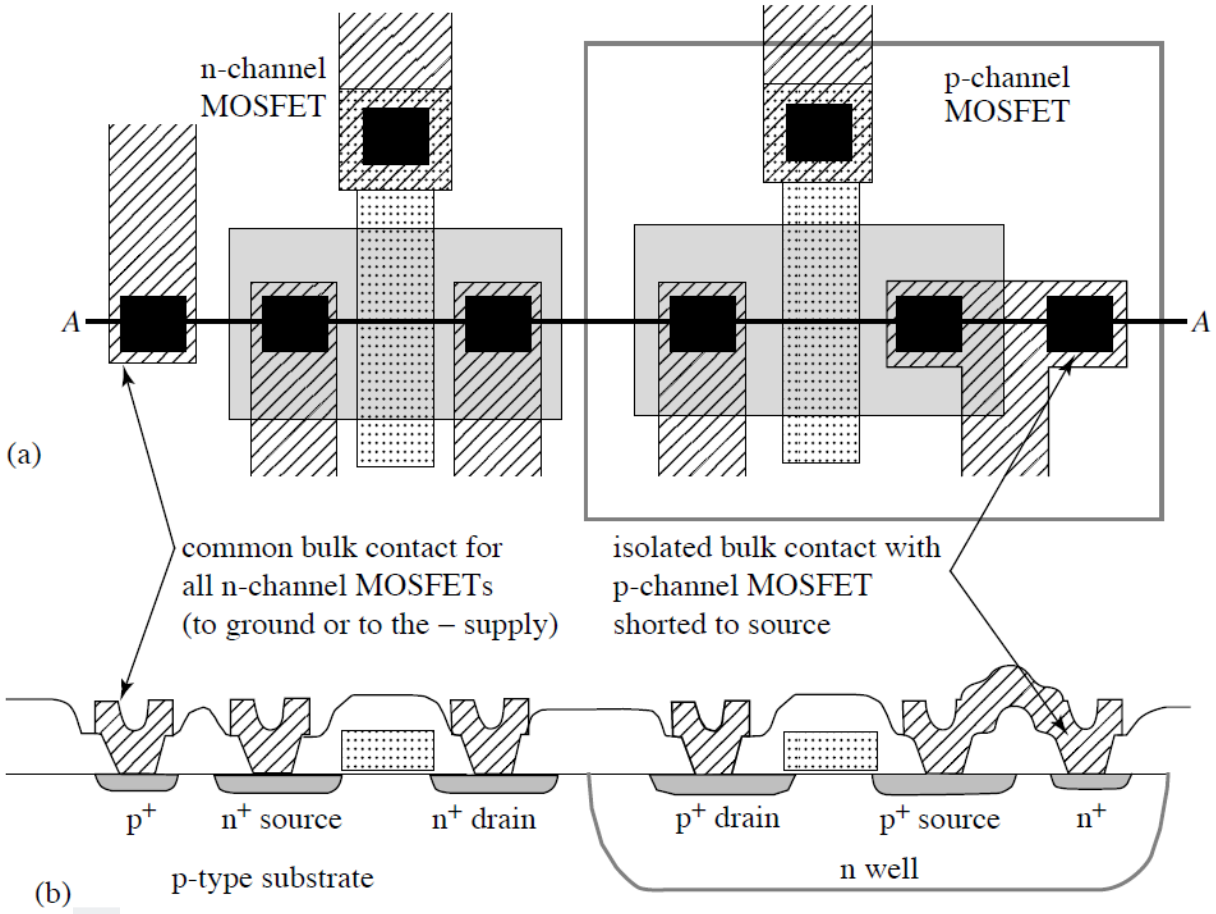
IC Fabrication & Layout Linkage

(CMOS transistors – nMOS & pMOS)



From: Roger T. Howe & Charles G. Sodini, *Microelectronics: An Integrated Approach*, © 1997 Prentice-Hall, USA.

- In studying EEE201, you should be able to draw the **transistor schematic circuit** from the **IC layout** (a) and sketch the corresponding cross-sectional structure (b) as shown on the left.

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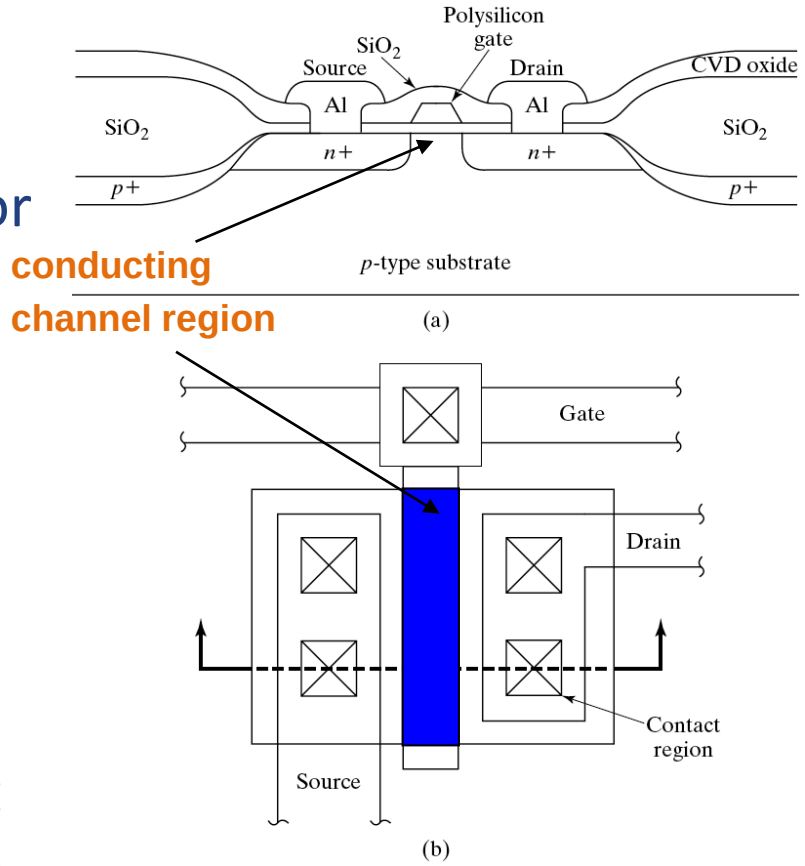
Basic Silicon CMOS Technology

(NMOS transistor)

- Structure of a basic NMOS transistor (Fig. (a)):
  - ***n***- and ***p***-type semiconductor regions (e.g. source/drain)
  - thick & thin oxides
  - etching openings (vias)
  - polysilicon (or metal) gate
  - metal (e.g. aluminium) interconnections
- Corresponding physical layout of the NMOS transistor (Fig. (b) shown on the right)



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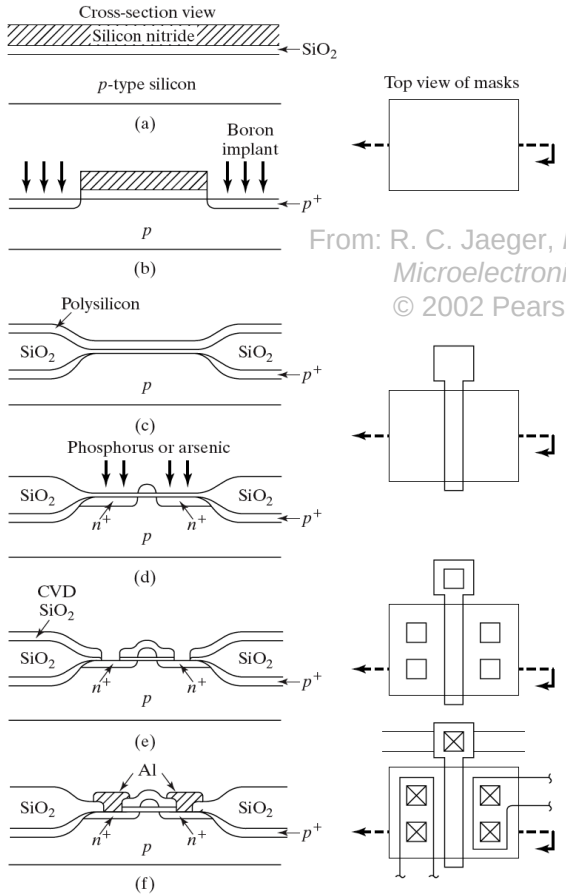
From: R. C. Jaeger, *Introduction to Microelectronic Fabrication*, 2nd Edition, © 2002 Pearson Education, USA.

Basic Silicon CMOS Technology

(sequence of fabrication steps - NMOS)



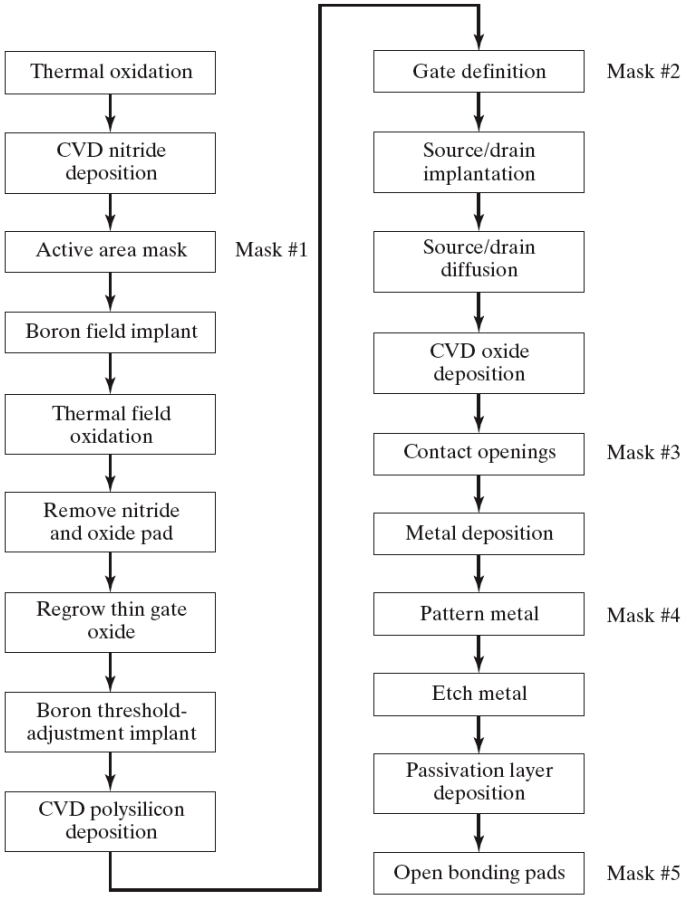
mask 1

From: R. C. Jaeger, *Introduction to Microelectronic Fabrication*, 2nd Edition, © 2002 Pearson Education, USA.

mask 2 (with mask 1 also shown)

mask 3 (with masks 1 & 2 also shown)

mask 4 (with masks 1 & 2 also shown)



- To make the NMOS transistor, certain sequence of fabrication steps are needed.

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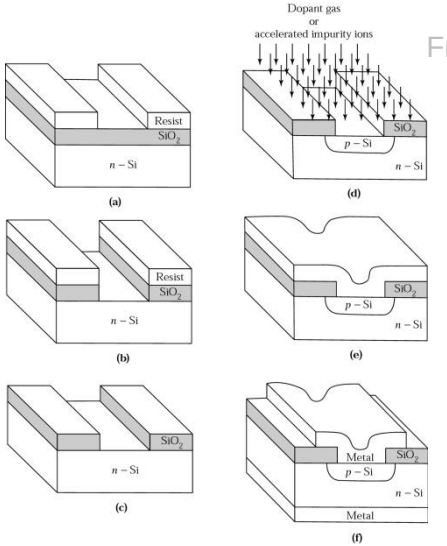
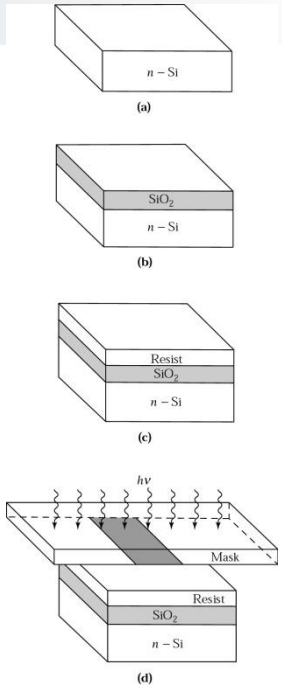
Basic Silicon CMOS Technology

(key processes)

- The key processes for the fabrication of the NMOS transistor are:
  - **thermal oxidation**
  - **photolithography**
  - **ion implantation**
  - diffusion formation
  - etching
  - **thin film deposition**



From: G. S. May and S. M. Sze, *Fundamentals of Semiconductor Fabrication*, © 2004 Wiley, USA.



- At least four **masks** are needed to define the structure of the NMOS transistor.
- Integrated circuit (IC) chips are usually covered with a **passivation** layer for isolating the metal interconnect from the ambient. An additional mask is then used to define **bonding pads**.

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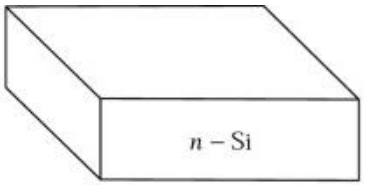
Basic Silicon CMOS Technology

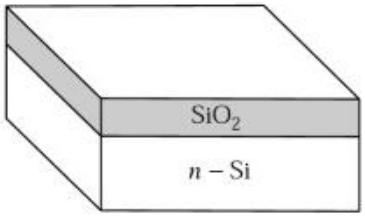
(silicon dioxide & thermal oxidation)

- With silicon (**Si**) as the starting material, a useful insulating layer of **silicon dioxide** (**SiO_2**) can be easily grown thermally or deposited on the wafer surface.

From: G. S. May and S. M. Sze, *Fundamentals of Semiconductor Fabrication*, © 2004 Wiley, USA.



(a)



(b)

- **Thermal oxidation** is the process of growing a **SiO_2** layer by oxidising the surface of the silicon wafer.
- The **gate oxide** of the MOSFET is typically formed by **thermal oxidation**.

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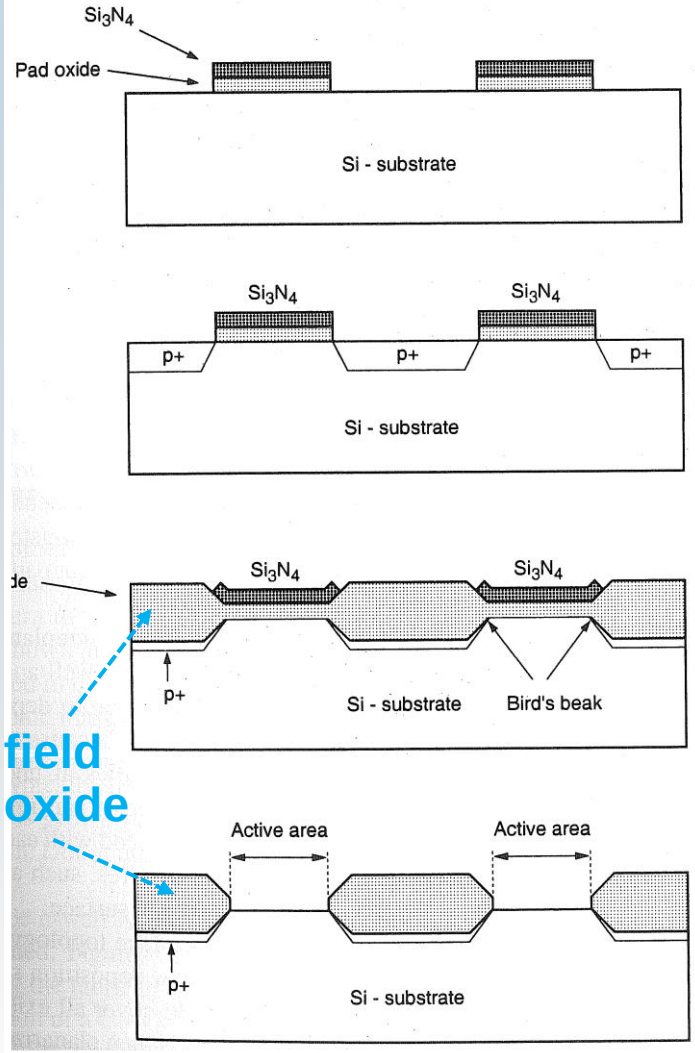
Thermal oxidation & LOCOS

(field oxide for lateral isolation)



- **Thermal oxidation** is also used in the formation of the so-called **field oxide**. In such a case, it is known as LOCOS (local oxidation of silicon)
  - LOCOS is for lateral insulation of transistors to avoid accidental electrical connections.
  - Modern CMOS technology uses shallow trench isolation (STI).

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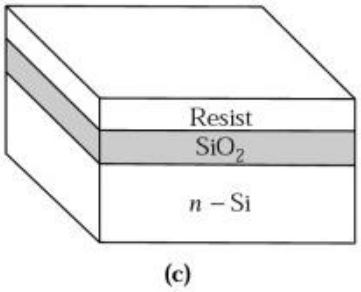
Photolithography

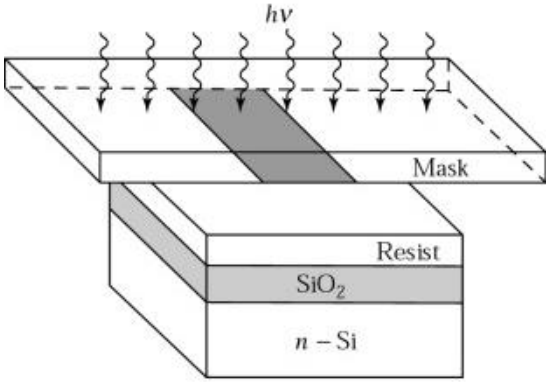
(transferring pattern onto wafer surface)

- **Lithography** is a set of process steps to ***print*** **patterns** from a **mask** onto the surface of a wafer substrate with very high precision.

From: G. S. May and S. M. Sze, *Fundamentals of Semiconductor Fabrication*, © 2004 Wiley, USA.



(c)



- In modern semiconductor manufacturing, virtually all ICs are manufactured using ***optical*** **lithography**, or simply **photolithography**.
  - The pattern transfer is through the **photoresist**, a light-sensitive polymer material.

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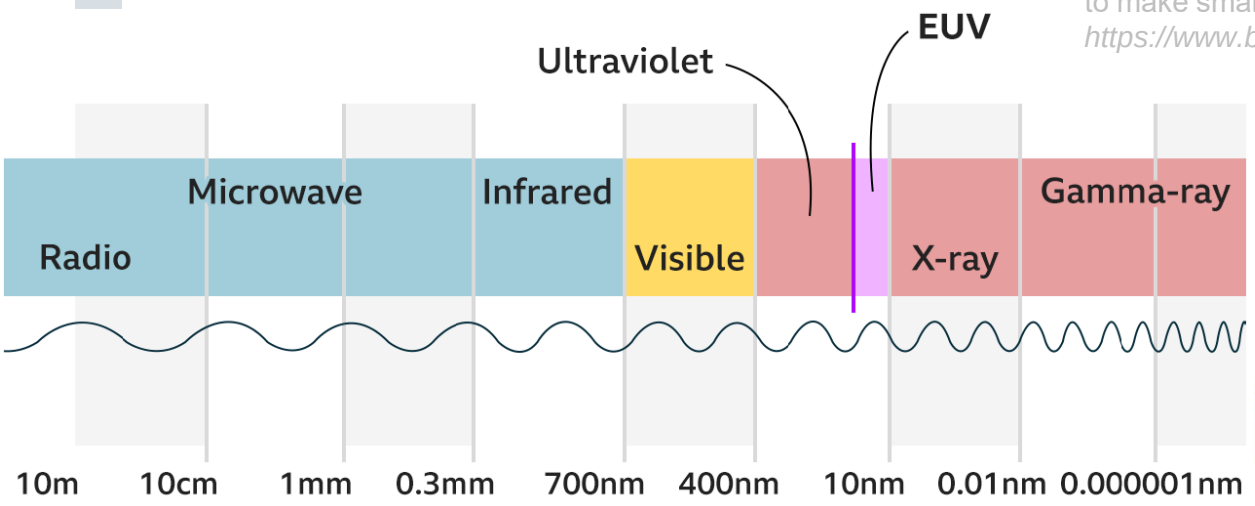
Photolithography

(use of EUV light)

- To define the very small structures in IC fabrication, **extreme ultra-violet** (**EUV**) light is used in **photolithography** in modern CMOS process.
  - In the state-of-the-art 5-nm CMOS technology for making the *iPhone 12* A14 microprocessor, the **EUV** light has a wavelength of **13.5 nm**.

From: BBC News, "Apple iPhone 12: The chip advance set to make smartphones smarter" available at: *https://www.bbc.com/news/technology-54510363*.



  - At XJTLU, the UV light in optical lithography is of of 365 nm.

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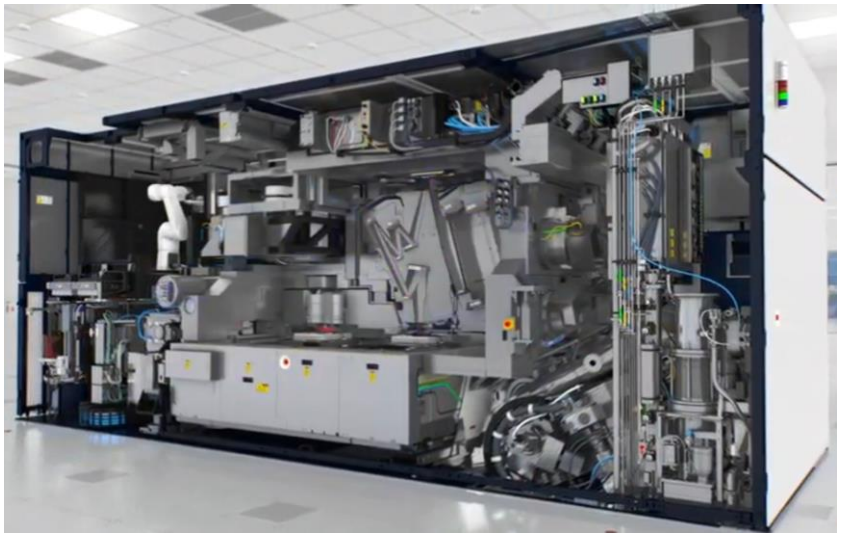
EUV Photolithography

(critical technology in nano-CMOS fabrication)

- As of 2020, **photolithography** below 10 nm in IC fabrication is only available from one Dutch company, ASML, in the whole world.
  - TSMC, Samsung, SMIC and others need the photolithography machines from ASML.

From: ASML, "EUV Lithography Systems: Lithography that shapes the future"; available at: *https://www.asml.com/en/products/euv-lithography-systems*



- TWINSCAN NXE:3400C

From: ASML's video, "EUV lithography in action - Inside the TWINSCAN NXE:3400 EUV lithography machine" available at: *https://www.youtube.com/watch?v=GBdMRUG69uc*

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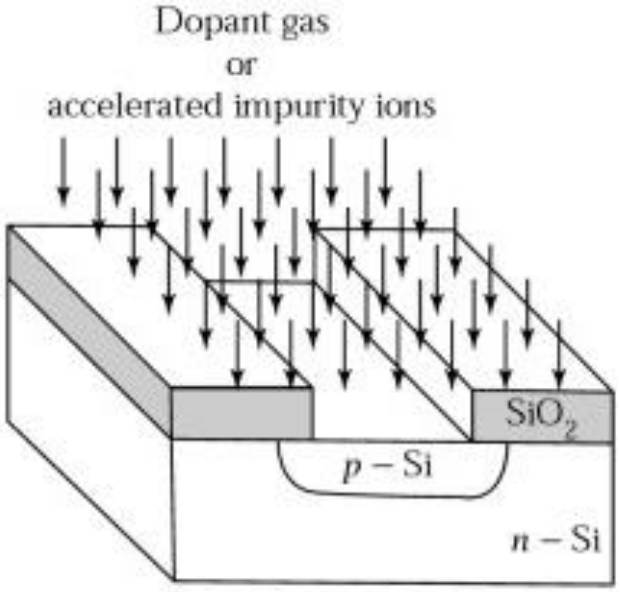
Selective Doping

(ion implantation or diffusion)

- To make the MOSFET, regions of semiconductor wafers are ***selectively*** doped to make the regions ***n***-type or ***p***-type thus creating electronic device structures such as the ***p***-***n*** junction.



- **Selective doping** is one of the key processes in fabricating semiconductor devices.
- **Ion implantation** and **diffusion** are two key methods of selective doping.

From: G. S. May and S. M. Sze, *Fundamentals of Semiconductor Fabrication*, © 2004 Wiley, USA.

Etching – chemical or physical

(selective removal of thin layer)

- **Etching** is a process for the ***selective*** **removal** of a thin layer of specified regions on the wafer surface. (It can be a **dielectric**, **semiconductor** or **metal** layer).

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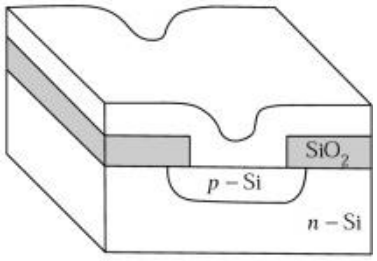
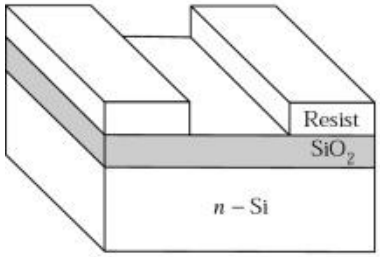
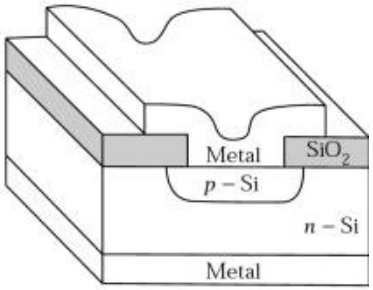


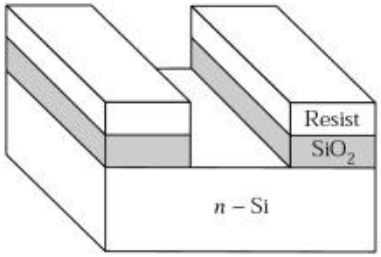
(e)



(a)



(f)



(b)

- The etching can be achieved by either ***chemical*** or **physical** processes or a combination of the two.

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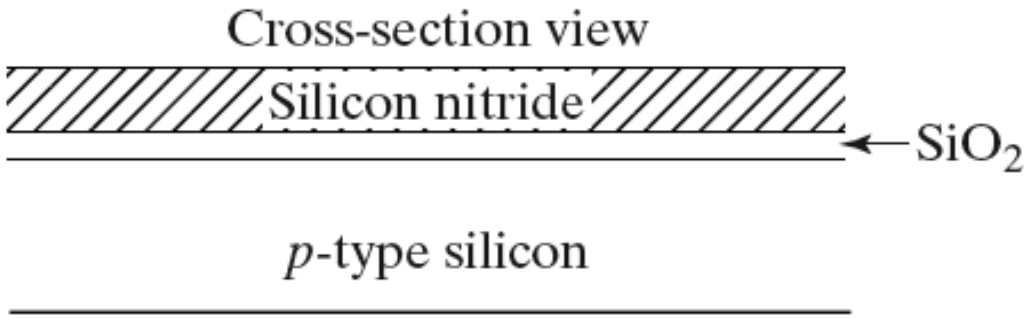
Thin Film Deposition

(deposit layer of material)

- In **thin film deposition**, a layer of material can be ***deposited*** on the **surface** of the wafer. In the fabrication of the MOSFETs, layers of **dielectric** and **metal** are usually deposited on the wafer.



From: R. C. Jaeger, *Introduction to Microelectronic Fabrication*, 2nd Edition, © 2002 Pearson Education, USA.

- The deposition can be either **physical** or **chemical**.
  - **physical vapor deposition** (**PVD**), including **evaporation** and **sputtering**
  - **chemical vapor deposition** (**CVD**)

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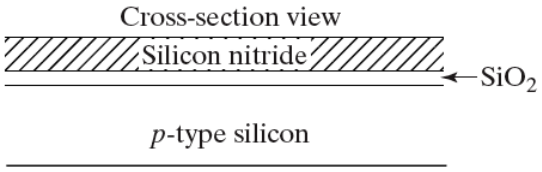
Basic Silicon CMOS Technology

(defining the active region)



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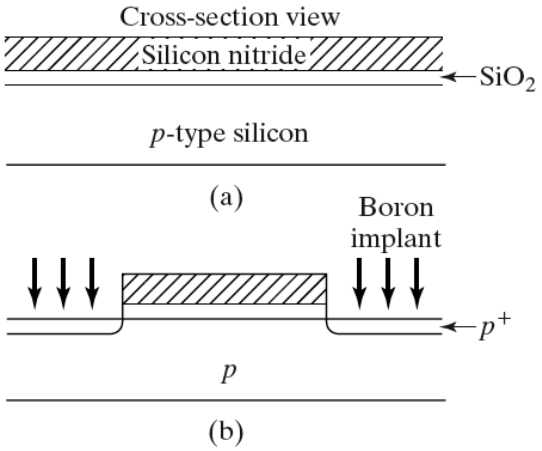
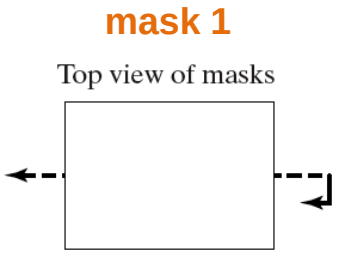
- The fabrication starts with a silicon wafer covered with **silicon nitride** (Si_3N_4) over a thin padding layer of **silicon dioxide** (SiO_2).





- Mask #1 is used to define the **active area** of the NMOS transistor.
- The wafer is etched leaving the **active region**.

- A **boron implant** is used to help control the **field oxide** threshold voltage.
  - for electrical isolation between transistors

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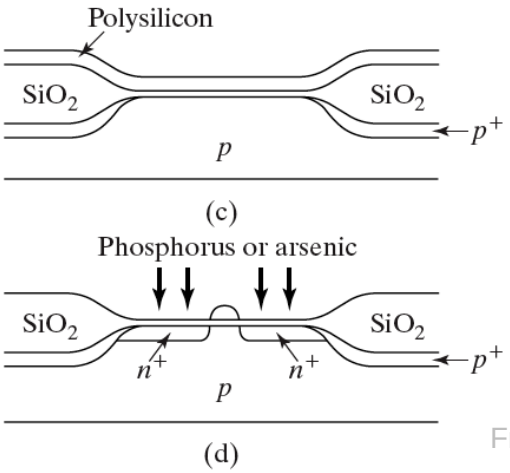
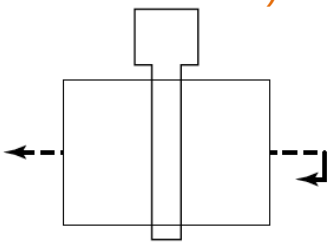
Basic Silicon CMOS Technology

(gate formation)



mask 2 (with mask 1 also shown)



- A multi-layer structure is formed after oxidation, nitride removal and polysilicon deposition (Fig. (c)).

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- Mask #2 is used to define the polysilicon gate of the NMOS transistor.
- The wafer is etched, leaving the polysilicon gate covering a thin layer of oxide (Fig. (d) as shown above).
- **Phosphorous** or **arsenic implant** is used to form the ***n***-type source and drain regions (Fig. (d)).

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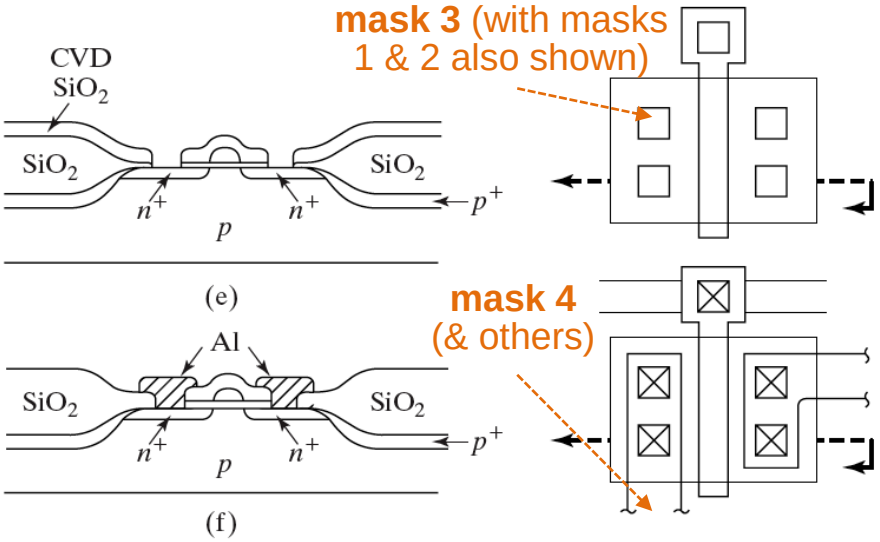
Basic Silicon CMOS Technology

(contact windows & metallisation)



From: R. C. Jaeger, *Introduction to Microelectronic Fabrication*, 2nd Edition, © 2002 Pearson Education, USA.

- After depositing a layer of SiO_2 for interlayer electrical insulation, the third mask (#3) is used to open **contact windows** (Fig. (e)) i.e. **vias** for source and drain regions.
- A **metal layer** is deposited and the **metal interconnect** for electrical conduction is defined by mask #4.
- The final structure of the NMOS transistor is formed (Fig. (f)). A **passivation** layer is added afterwards. And mask #5 is used to define **bonding pads**.

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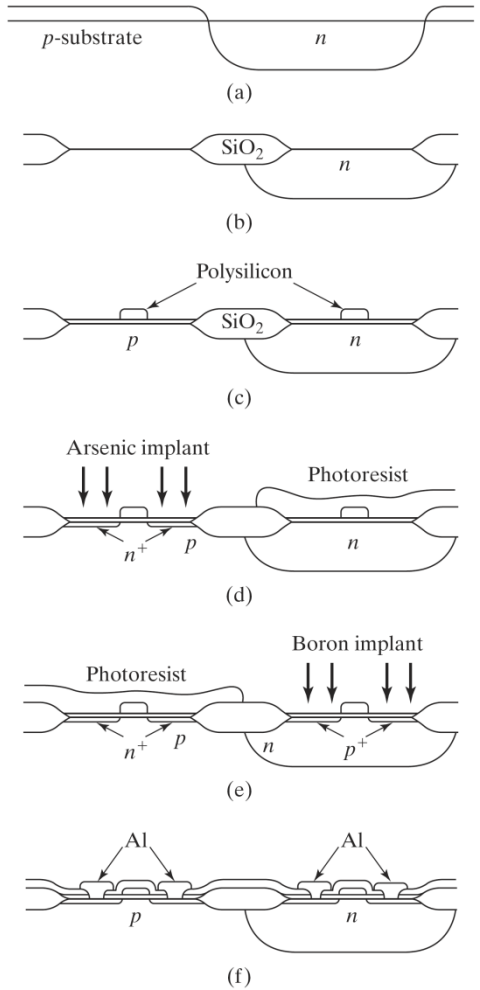
Basic Silicon CMOS Technology

(both NMOS & PMOS transistors)



- In **silicon CMOS** (Complementary Metal-Oxide Semiconductor) **technology**, both NMOS and PMOS transistors are fabricated on the same wafer.
- The key processing steps are essentially the same, consisting of **thermal oxidation**, **photolithography**, **ion implantation**, diffusion formation, **etching**, **thin film deposition.**
- Major steps of an ***n***-well CMOS (i.e. forming a PMOS transistor in an ***n***-well) technology is shown on the left.

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