EEE201 Coursework 1 – CMOS IC Design Project

Design Report

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Abstract:

This IC layout design project focuses on optimizing the switching speed of a CMOS NOR Gate while considering area, cost, and power consumption trade-offs. The width ratio of the Pull-Up Network (PUN) and Pull-Down Network (PDN) is set to 1:8 to enhance speed, though this sacrifices area efficiency, making the design less suitable for compact devices. The larger PMOS network also increases costs due to the complexities of P-type doping and the higher expense of PMOS transistors. Power consumption is affected by leakage currents through multiple PUN contacts. The layout design aims to minimize parasitic capacitances and inductances, adhering to design rules. Further exploration is needed in areas like multi-layer metal optimization and aging effects for improved reliability.

1. Introduction

1.1 Background

As low power loss networks, CMOS digital integrated circuits are useful in electronics industry, especially in the control system. Nonlinear oversampled controllers built by CMOS digital circuits effectively optimizes the switch behavior and significantly enhance the efficiency of DC-DC converters [1]. Among the CMOS logic gates, NOR gate function matters a lot, with function $F = \overline{A + B}$. Dadashi [2] suggests that the Domino dual-rail CMOS NOR gate, combined with Semi-Floating Gate (SFG), achieves a speed 20 times faster than the traditional NOR gate model.

1.2 Design Goal

My primary goal of this IC Layout design is to *optimize the switching speed of the CMOS NOR logic gate*, as switching speed is one of the crucial factors in advanced computer systems. For instance, insufficient numbers of high-speed PCIe channels can negatively affect the overall system performances [3]. However, optimizing switch-speed between PCIe TX and RX can enhance the system's performance [3].

2. Circuit Design at Schematic Level

2.1 CMOS NOR Gate Circuit Schematic

The NOR Gate Circuit Schematic is shown in Figure 1.

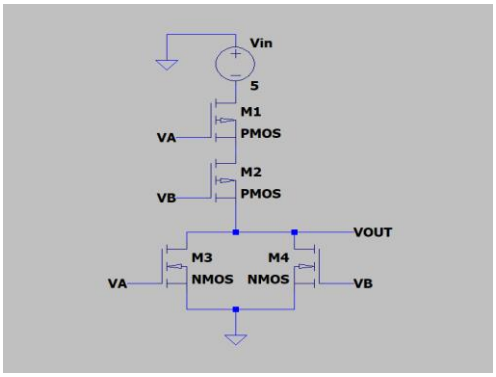

Figure 1. CMOS NOR Gate Circuit

2.2 Size Considerations of Two Networks

The Pull-Down Network (PDN) occupies a smaller area than that of the Pull-Up Network (PUN), so it is intuitive to consider the minimum size of the NMOS transistors layout. Based on the design rules, particularly the space between contacts and the active region, I first determine the width of the Active Region of the NMOS Network to be 4λ. Given my design goal of achieving higher speed as mentioned earlier, I set the W/L ratio of the PDN to PUN at $1:8$, resulting in a width of 32λ for the active region of PDN. As soon as the width of the active region is fixed, the remaining work is to follow the rules to adjust the minimum length.

2.3 CMOS NOR Gate Size Design

Assume the same rising and falling time for PUN and PDN, then consider the normal case where $VA = VB$, we have:

$$\mu_n * \left(\frac{2W_n}{L}\right) = \mu_p * \left(\frac{W_p}{2L}\right)$$

When $\mu_n = 2 * \mu_p$, then

$$W_P = 8W_n$$

The larger width of PUN results in a greater current driving the charging of the capacitor, thus reducing the time constant and improving switching speed.

2.4 Trade-off of Circuit Design

It is challenging to achieve both high speed and small chip area simultaneously. Therefore, I have prioritized improving the switching speed of the CMOS NOR gate to enhance computer system efficiency, ***as demonstrated in the design goals***.

2.5 Schematic Design Evaluations

In spite of the enhancement of switching speed, my design is not perfect for several reasons.

✧ *Parasitic Capacitors*

While my design effectively improves the switching speed, it falls short of considering the charging and discharging behaviors of parasitic capacitances in MOSFETS, which may require additional time to charge and discharge during the transitions, impacting switching speed.

✧ *Inductances of The Conductive Channels*

Aside from capacitances, inductances in the metal connections can also impact the switching speed. The change of current between stages can contribute to accumulated energy stored in inductances. If the circuit is required to operate in higher frequencies, the stored energy may pose delays to the system, reducing switching speed.

2.6 Comparison of alternative NOR Gate Circuits

Aside from applying CMOS logic, an alternative approach is to use NMOS transistors alone to build the NOR gate logic, as shown in Figure 2.

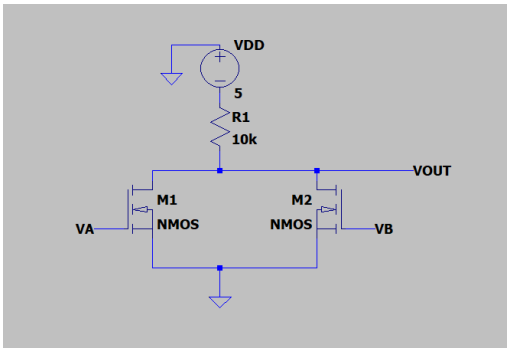

Figure 2. NMOS NOR Gate Alternative

Compared with CMOS NOR Gate, NMOS logic performs better in the switching speed. Because NMOS transistors possess a higher electron mobility, which reduces the time required for charging and discharging. However, CMOS NOR Gate largely reduces the power consumption, as CMOS circuits only conduct current during the transition states, avoiding steady current flow.

3. IC Layout Design

3.1 Overall Layout Visualization

The overall layout is shown as Figure 2.

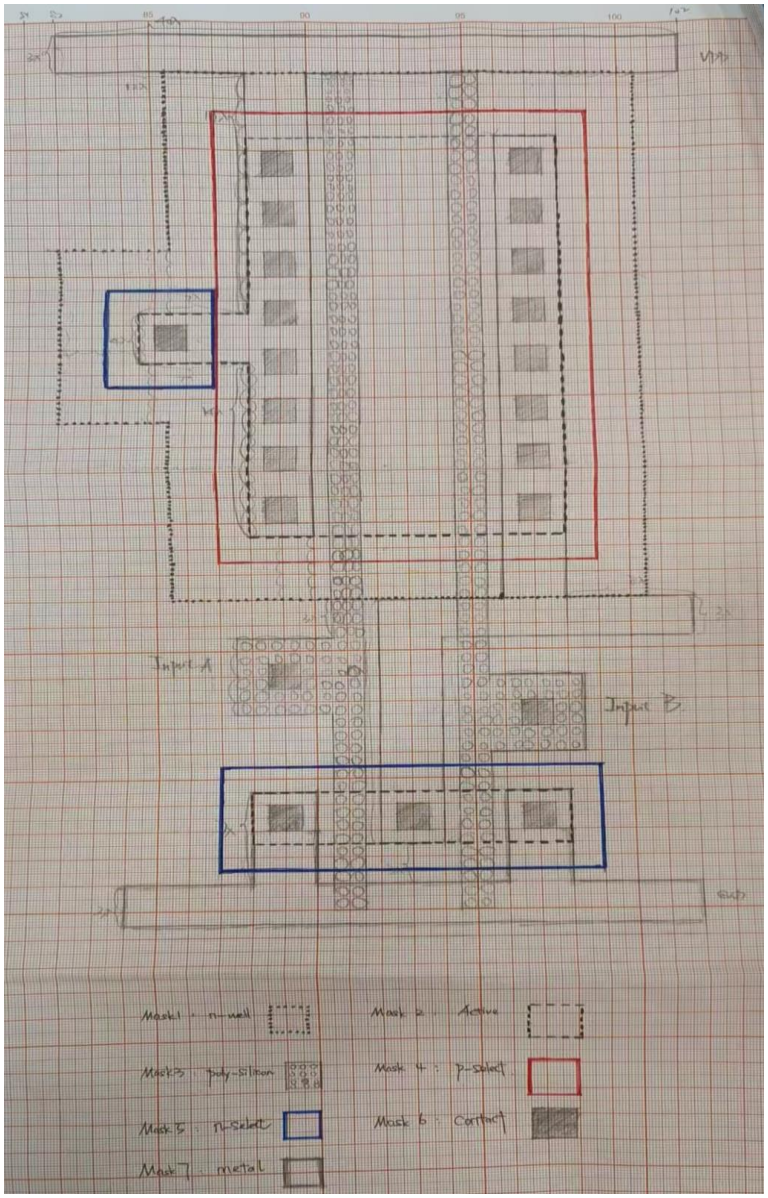

Figure 2. Overall Layout

3.2 Two Main Optimizations for Overall Layout

✧ *Isolated Bulk Contact*

Lecture 6 provides a graph of CMOS IC Fabrication, which shows that the isolated bulk contact with P-type doping has to be included within the n-well. Thus, the PUN should add a P-Select mask and the n-well needs to be modified from a standard rectangle to a rectangle with a protruding section. To consider this special contact, I refer to the guide of the spacing between n-well and P-Select, the distance between active region and P-Select. Note that I overlap P-Select with N-Select to minimize the layout area.

✧ *Two Input Contacts*

Lecture 9b shows that two input terminals should be clarified in the layout by connecting metal and contact. To determine the positions of two inputs, we should consider Input B initially. The upper boundary of Input B must maintain a 3λ spacing from the OUT terminal, while the lower boundary is spaced 3λ from the upper edge of the NMOS Network's active region. Then, the position of Input A can be determined by following the layout rules.

3.3 Design to Minimize Impacts from Capacitances and Inductances

✧ *Solutions for Capacitances*

To minimize the unwanted speed issues due to parasitic capacitances, I have tried my best to limit the length of gate and the distances between Source and Drain.

✧ *Solutions for Inductances*

Regarding inductances, I have focused on minimizing the length of metal lines while maintaining symmetry in the layout structure.

3.4 Significant Layout Rules for Design

✧ *Rules of Active*

To draw the layout, the first thing to determine is the width of two active regions. Since the NMOS Network possesses a narrower width than PMOS Network, I started by

determining the width of PDN active region. Following the design rules, the PDN minimum active region width is 4λ. Given my design goal of achieving higher speed as mentioned earlier, I set the W/L ratio of the PDN to PUN at $1:8$, resulting in a width of 32λ for the active region of PDN. As soon as the width of the active region is fixed, the remaining work is to follow the rules to adjust the minimum length. And I have aligned the boundaries of two active regions, with their lengths set to 20λ.

✧ *Rules of Contact*

It is also hard for me to determine size of Mask 6: Contact. I would like to illuminate my design of contact from three dimensions.

1. First, for contacts of PUN and PDN, since the widths of two active regions have been determined, I calculated the contact ratio, which matches the $Wp:Wn$ ratio of $1:8$ (One contact has the area of $2\lambda * 2\lambda$, the spacing between contacts is 1λ, the minimum space between contact and active region is 1λ).
2. Second, for bulk contacts, common bulk contacts in the PDN are grounded and not included in the layout, while isolated bulk contacts for the PUN are required, ***as discussed in section 3.2***.
3. Last but not least, for the input contacts, the spacing between contacts and metal is 2λ, not 1λ.

✧ *Rules of Polysilicon*

Since each pair of NMOS transistor and PMOS transistor shares the common gate, two gates span two active regions vertically. That means designing the gate requires careful consideration of the spacing between the gate and the other six masks, which is one of the most difficult design parts. **I adjusted the gate size multiple times**. Moreover, gate should be at least 3λ longer than Select Mask.

✧ *Rules of Metal 1*

The most challenging aspect of the layout design for me was determining the size for Mask 7: Metal 1. To determine the size of metal, I have to take 3 main factors into considerations.

1. First, Metal has its regulated spacing between active regions, which is 5λ, and we have 2 active regions.
2. Second, Gate (Polysilicon), also one part of the metal, with the minimum spacing 2λ, is especially critical for two inputs case. Notice that these inputs are located between PUN and PDN, and Input B has a spacing beneath the OUT and above the active region of PDN, thus Input B should be located at a position 3λ (the width of OUT metal) lower than Input A vertically.
3. Finally, to further optimize the layout, several factors like whether the lower boundary of VDD could be aligned to the upper boundary of that of n-well to save space, or whether it is feasible to align the upper boundary of GND to the lower boundary of P-Select should be considered.

3.5 Trade-off of Layout Design

To save the area and maintain the symmetry of the layout, I fix the total length and width of this layout as $40\lambda * 70\lambda$. For PUN, I aligned the lower boundary of VDD to the upper boundary of n-well, and also overlapped the boundary of P-select and N-select. For PDN, I controlled Input A to be 3λ lower than n-well, and Input B 3λ lower than OUT. For the polysilicon, it has a 5λ spacing under active region.

3.6 Layout Design Evaluations

My IC Layout is not perfect for several reasons.

✧ *Area Efficiency & Design Constraints*

Choosing to set the width ratio of the PUN and PDN to 1:8 to optimize the switching speed will sacrifice the goal of minimizing area ***as mentioned earlier***, thus my design may not be suitable for integration into small electronic devices where compact layouts are crucial.

✧ *Cost Considerations in Design Choices*

Engineers should also consider design costs to ensure industry applicability. Increasing the width of the PMOS network almost doubles the active region size

compared to $1:4$ ratio, resulting in a larger total area. If I choose to magnify the size of PMOS Network. Since PMOS transistors are more expensive than NMOS transistors for their lower mobility, which has to be compensated by larger width to supply the same current as NMOS transistors, thus increasing cost. Additionally, P-type doping fabrication process is more complicated and difficult to control, which contributes to extra cost.

✧ *Impact of Contacts on Power Consumption*

In this design, the PUN requires 8 contacts, double that of the 1:4 case. **As taught in Lecture 11b**, ideally, if we neglects the transitions, the DC power consumption of CMOS NOR Gate $P_{DC} \approx 0w$. In fact, PMOS transistors still conduct current even when their voltage is below V_{TP}, operating in the sub-threshold region and causing leakage current. Each contact represents a possible current path, and while the leakage current is small, it becomes non-negligible as more contacts are added to the PMOS network. This results in significant DC power consumption that cannot be ignored.

4. Summary & Conclusion

In summary, this IC Layout Design Project provides me an opportunity to draw a layout individually by hand, laying the foundation for my future career as an electronic engineer. Through optimizing mask sizes and spacings, I've enhanced my overall design thinking, though it is time-consuming. Moreover, I also appreciate the teaching assistants for guiding me with hints rather than direct answers, which encouraged independent problem-solving.

While this project develops our IC design skills, there are further areas for exploration. The actual layout of one electronic device requires optimization of multi-layer metal connections. For instance, wiring faults due to spots defects can be optimized by applying an exact cell unit technique to build a cost function to get the smallest area [4]. Additionally, aging effect of CMOS devices should be considered. Dadgour and Banerjee [5] proposes an adaptive Time-Borrowing-based method to improve reliability, reducing timing failure probabilities by approximately 10 times.

5. Reference

[1] Z. Lukić, A. Radić, A. Prodić and S. Effler, "Oversampled digital controller IC based on successive load-change estimation for dc-dc converters," 2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Palm Springs, CA, USA, 2010, pp. 315-320, doi: 10.1109/APEC.2010.5433654.

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[5] H. F. Dadgour and K. Banerjee, "A built-in aging detection and compensation technique for improving reliability of nanoscale CMOS designs," 2010 IEEE International Reliability Physics Symposium, Anaheim, CA, USA, 2010, pp. 822-825, doi: 10.1109/IRPS.2010.5488727.