Integrated Electronics & Design

nMOS logic IC design

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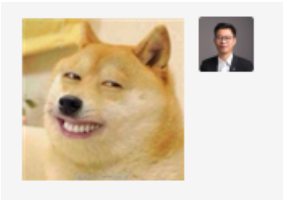
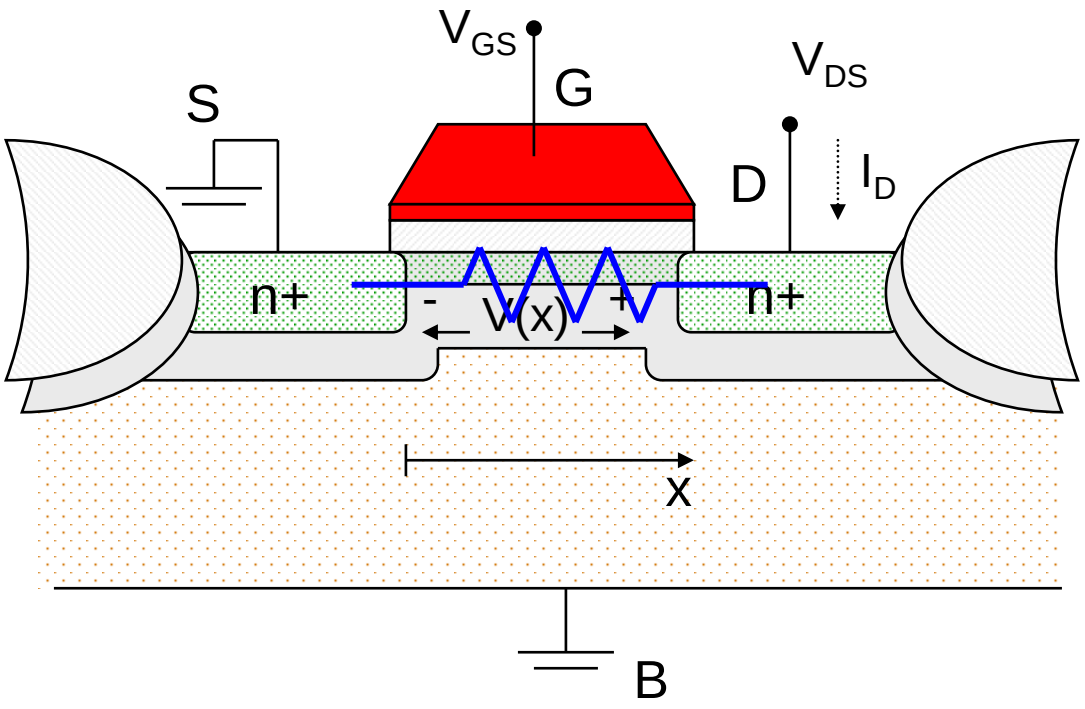
OUTLINE

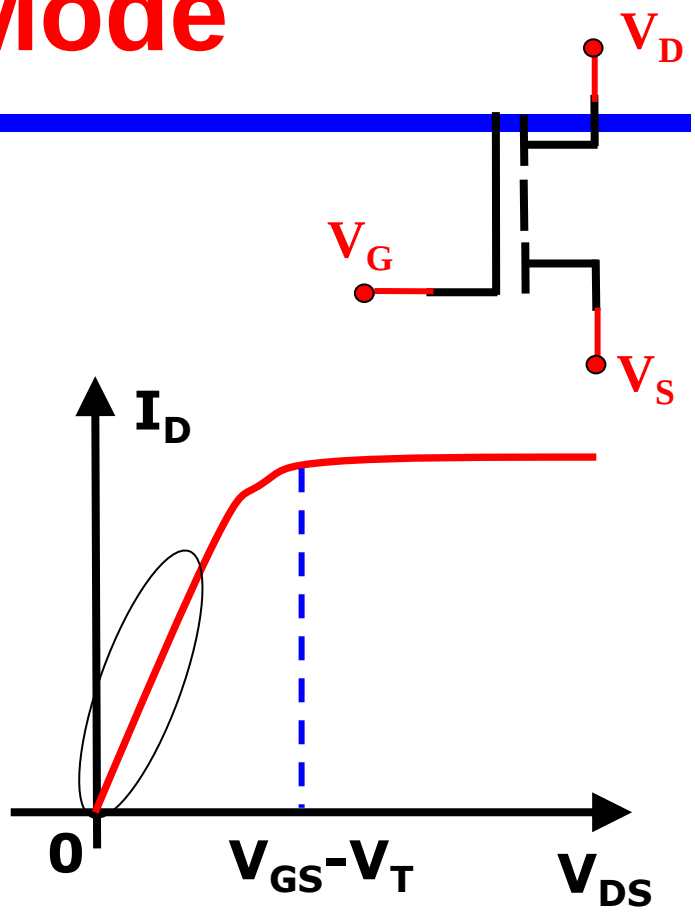
- **NMOS logic (examples)**
  - **Calculation**
  - Layout
- **Design Exercise**



Transistor in **Linear Mode**

Assuming $V_{GS} > V_T$





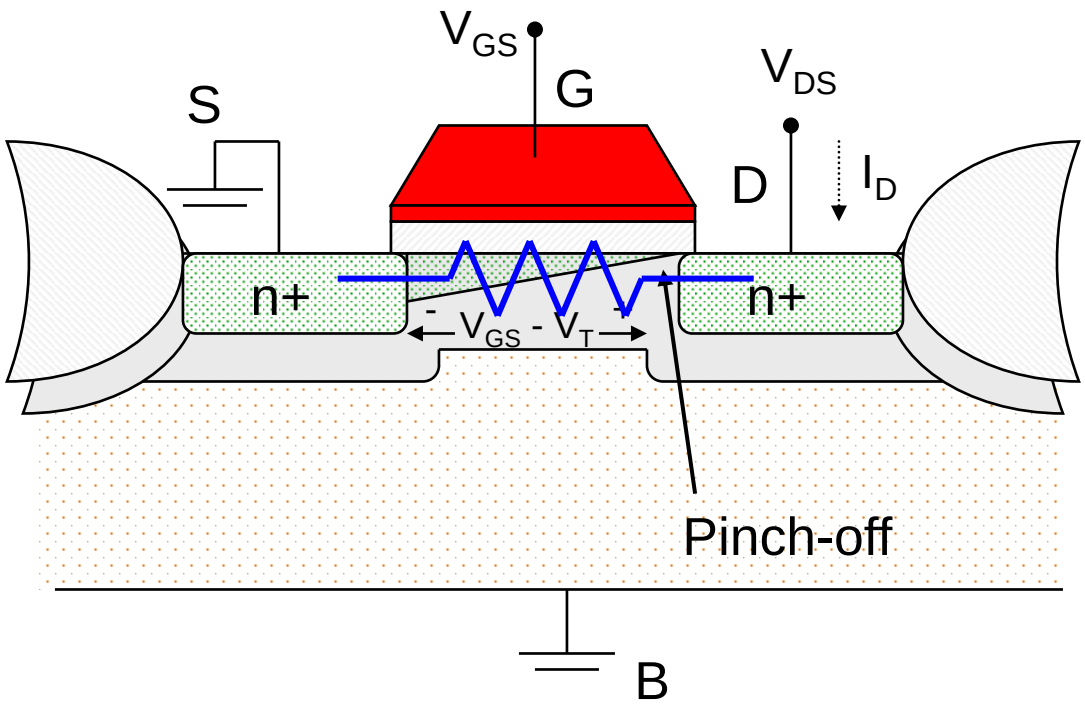
When $V_{DS} \leq V_{GS} - V_T$: $I_D = \beta_0 W/L [(V_{GS} - V_T)V_{DS} - V_{DS}^2/2]$

$\beta_0 = \mu_n C_{ox}$

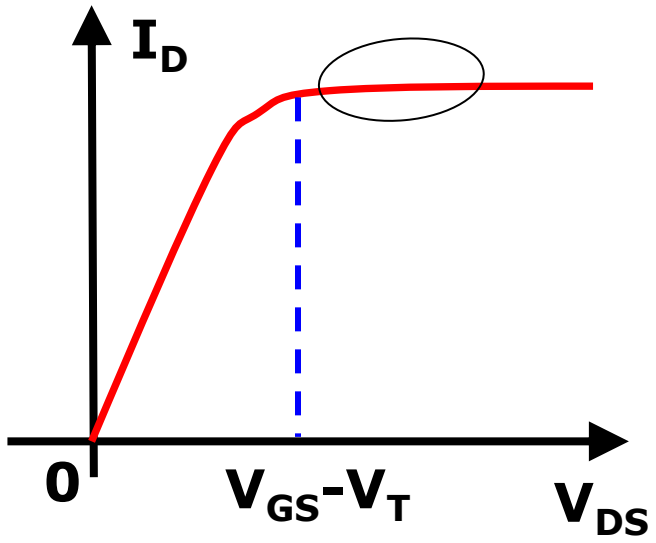
$R = V_{DS} / I_D$

Transistor in **Saturation Mode**

Assuming $V_{GS} > V_T$



$V_{DS} > V_{GS} - V_T$



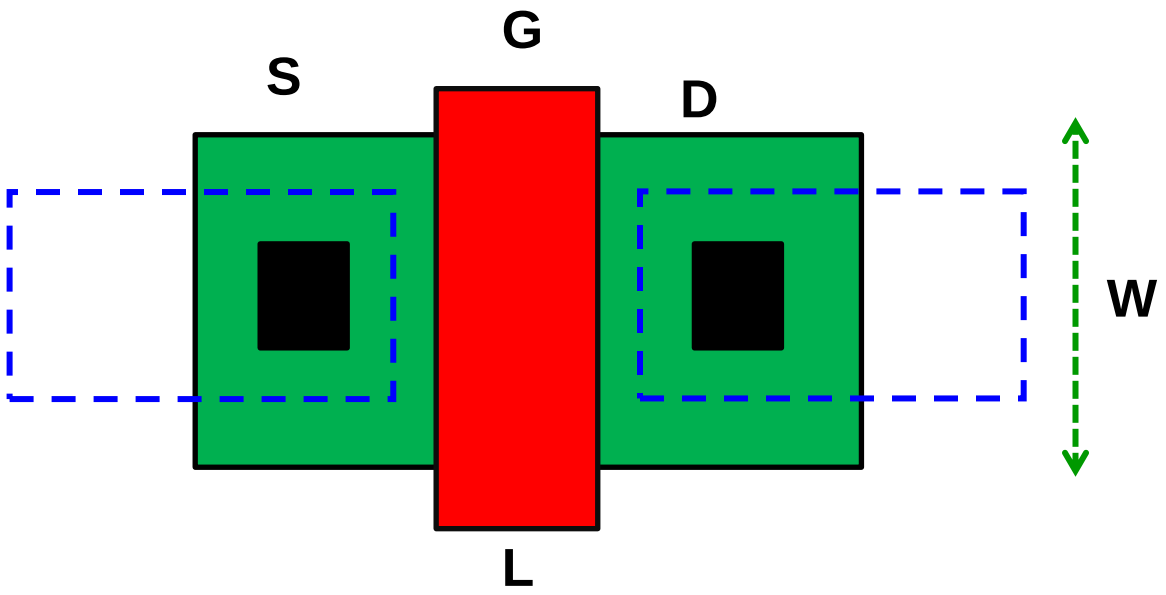
When $V_{DS} \geq V_{GS} - V_T$: $I_D = (\beta_0/2)\, W/L\, [(V_{GS} - V_T)^2]$

NMOS Logic (Inverter): Example 1

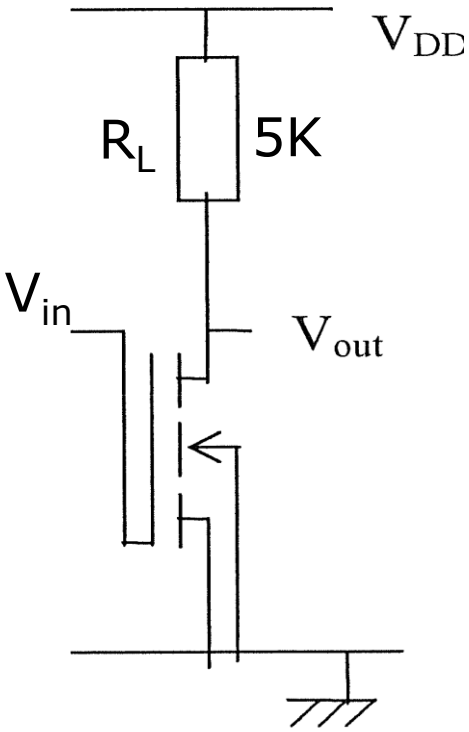
Calculate **W/L** with the following specification:
1) R_L=5k. 2) $\beta = \beta_0(W/L)$, and $\beta_0 = 1.8*10^{-4}AV^{-2}$.
3) V_T =0.3V. 4) V_{DD}=5V.

$\beta_0 = \mu C_{ox}$

The aspect ratio, W/L, is ??



Layout(版图)



NMOS Logic (**Inverter**): **Example 1**

Calculate **W/L** with the following specification:
1) R_L=5k. 2) $\beta = \beta_0(W/L)$, and $\beta_0 = 1.8*10^{-4}AV^{-2}$.
3) V_T =0.3V. 4) V_{DD}=5V.

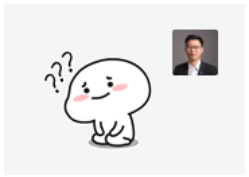
Solution:

If $V_{in} = V_{DD}$, **let V_{Out} = 0.1V << V_T**

Potential divider:

$$R_D/(R_D+R_L)=V_{Out}/V_{DD}=0.1/5=0.02$$

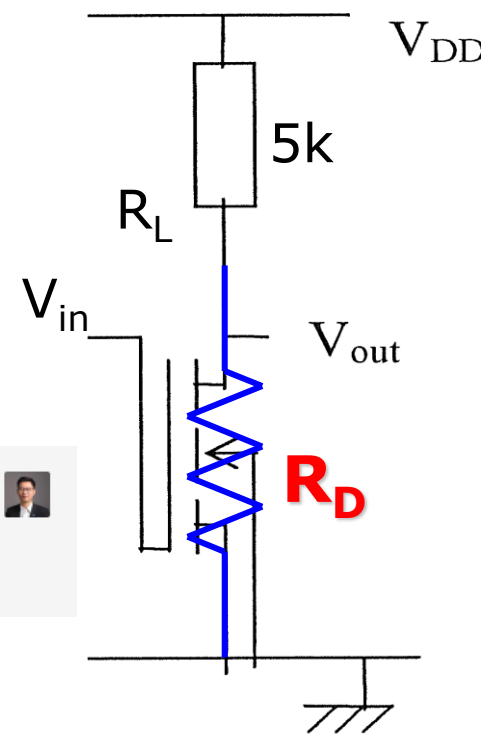
→ $R_D \approx 100\Omega$



$$I_D = \beta[(V_G-V_T)V_D-V_D^2/2] \approx \beta[(V_G-V_T)V_D]$$

$$R_D = V_{Out}/I_D = \{\beta[(V_{DD}-V_T)]\}^{-1} = 1/[\beta(5-0.3)] = 100\Omega$$

→ $\beta \approx 20*10^{-4}$. Therefore, the aspect ratio, W/L, is 12.



NMOS Logic (Inverter): Example 1

Calculate W/L with the following specification:
1) R_L=5k. 2) $\beta = \beta_0(W/L)$, and $\beta_0 = 1.8*10^{-4}AV^{-2}$.
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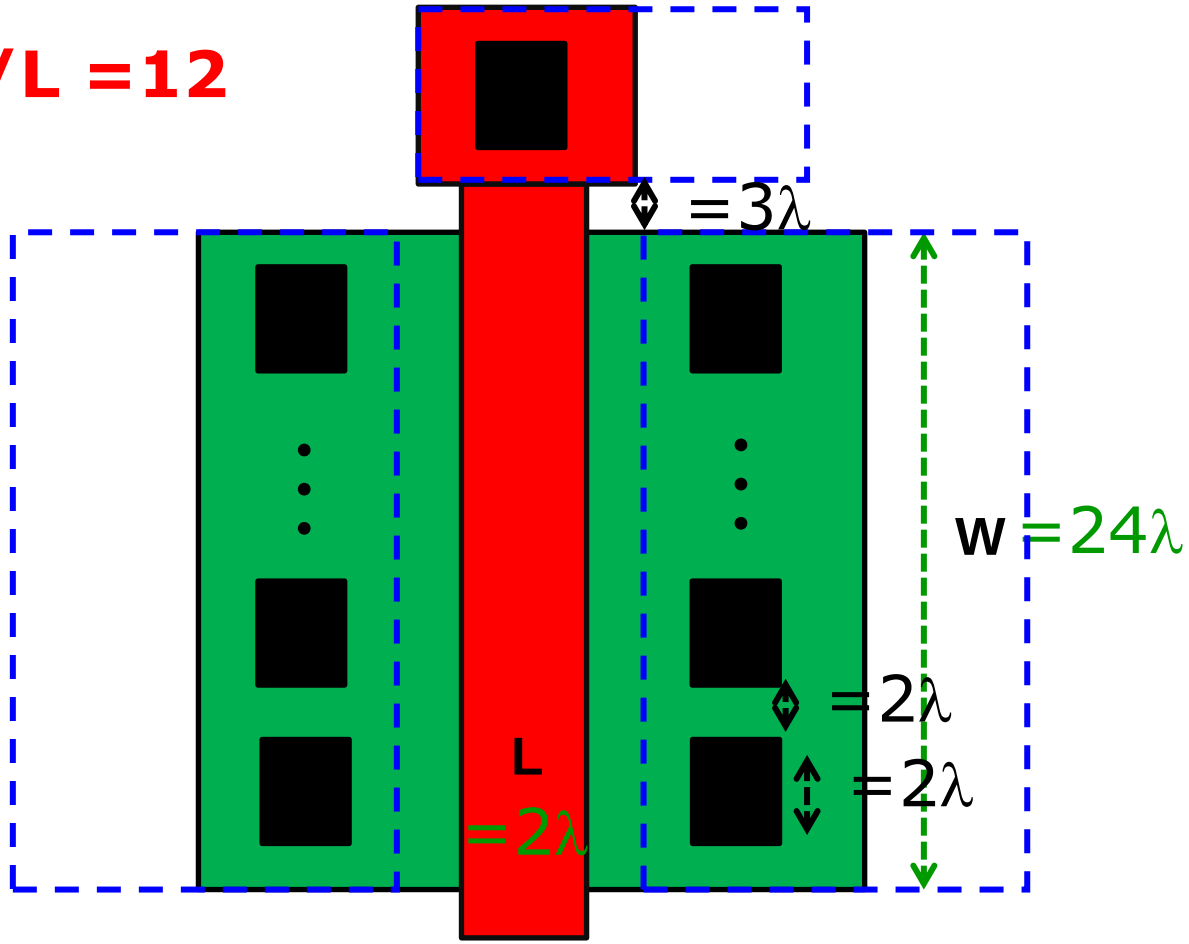
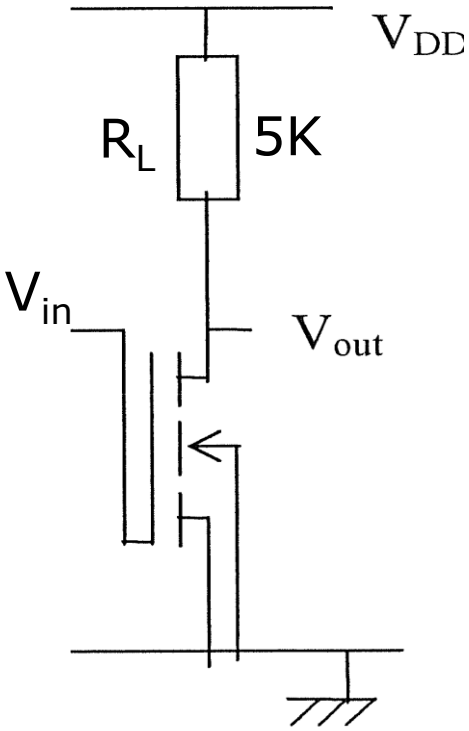
W/L =12

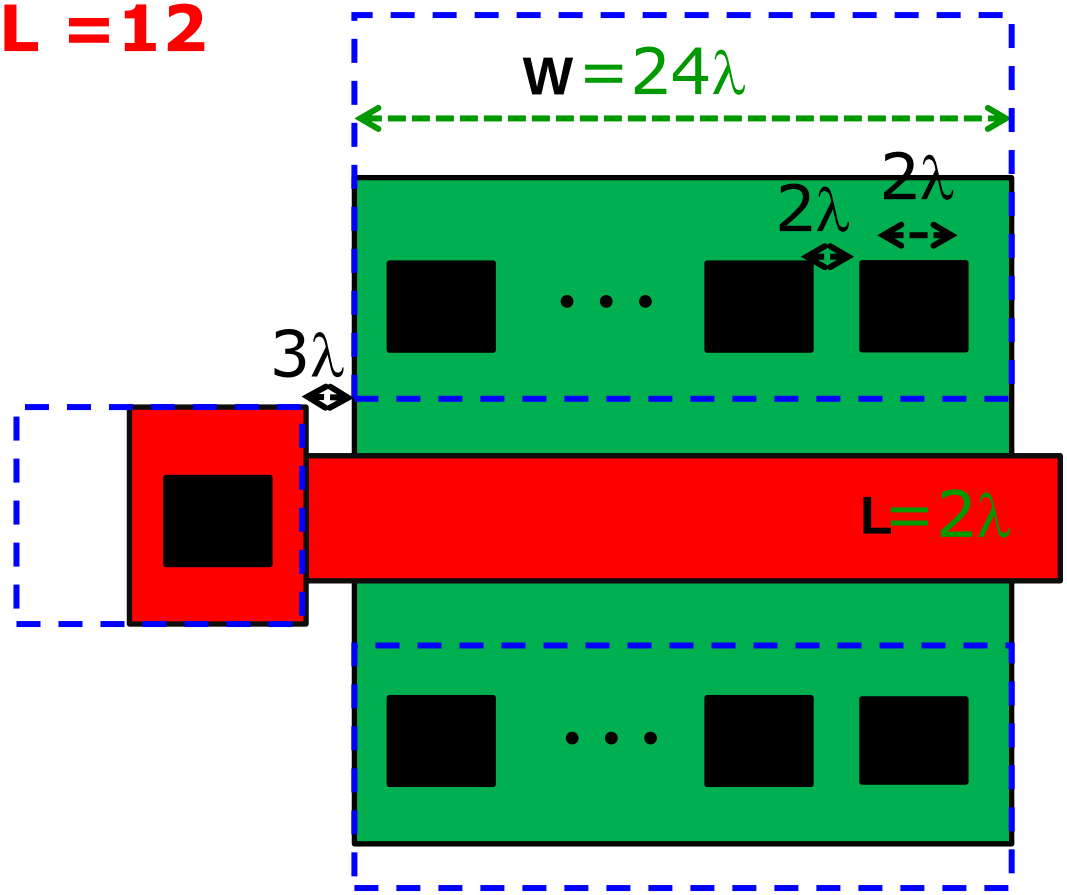


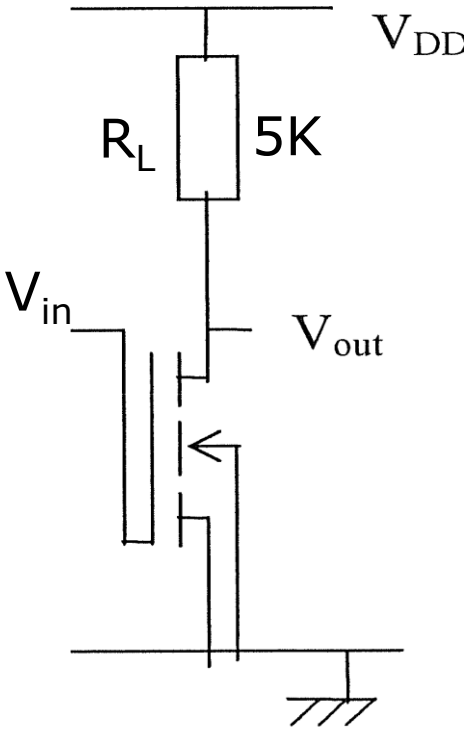


NMOS Logic (Inverter): Example 1

Calculate W/L with the following specification:
1) R_L=5k. 2) $\beta = \beta_0(W/L)$, and $\beta_0 = 1.8*10^{-4}AV^{-2}$.
3) V_T =0.3V. 4) V_{DD}=5V.

W/L =12

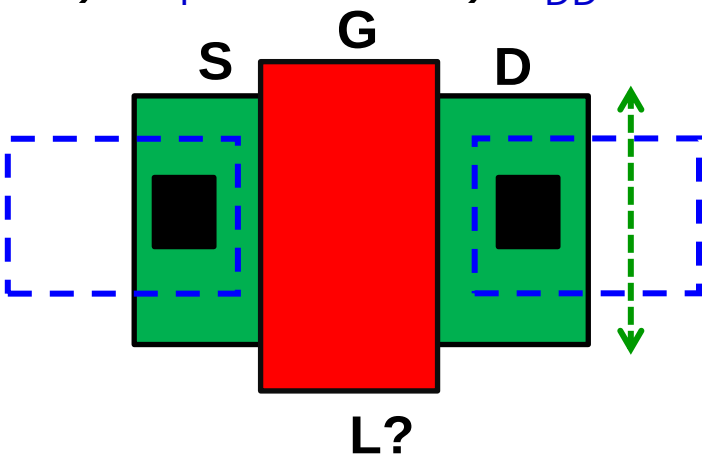


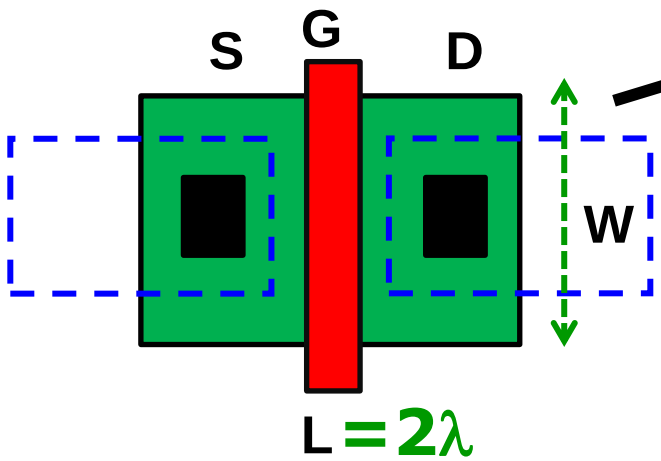


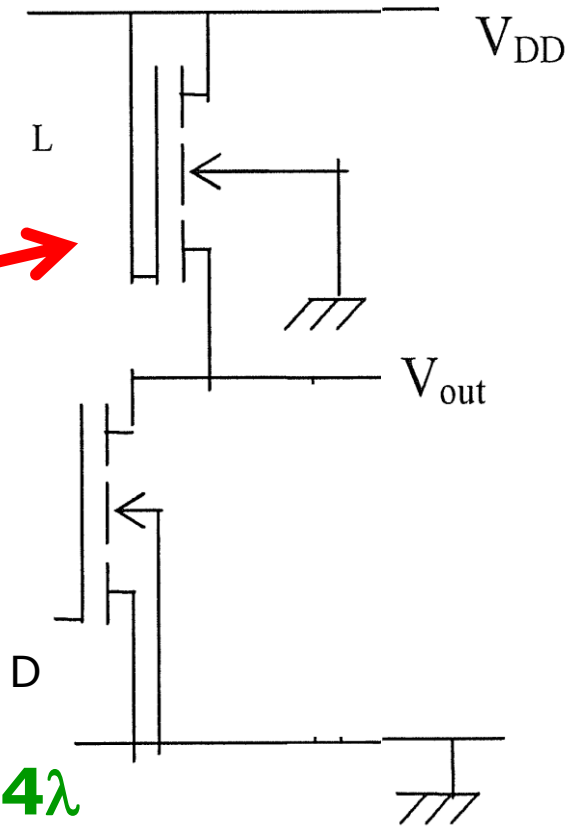
NMOS Logic (Inverter): Example 2

Calculate **W/L** of Load with the following specification:

1) **The aspect ratios of D is 12.**
2) $\beta = \beta_0(W/L)$, and $\beta_0 = 1.8*10^{-4}AV^{-2}$.
3) $V_T = 0.3V$. 4) $V_{DD}=5V$.







NMOS Logic (Inverter): Example 2

Calculate W/L of Load with the following specification:

1) **The aspect ratios of D is 12.**
2) $\beta = \beta_0(W/L)$, and $\beta_0 = 1.8*10^{-4}AV^{-2}$.
3) $V_T = 0.3V$. 4) $V_{DD}=5V$.

Solution:

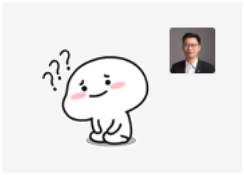
If $V_{in} = V_{DD}$, let $V_{Out} = 0.1V$:

$$I_D = \beta_D[(V_{in}-V_T)V_{Out}-V_{Out}^2/2]$$

$$\mathbf{R_D = V_{Out}/I_D = (12\beta_0[(V_{DD}-V_T)])^{-1} = 100\ \Omega}$$

$$[R_D/(R_D+R_L)]=V_{Out}/V_{DD}=0.1/5=0.02$$

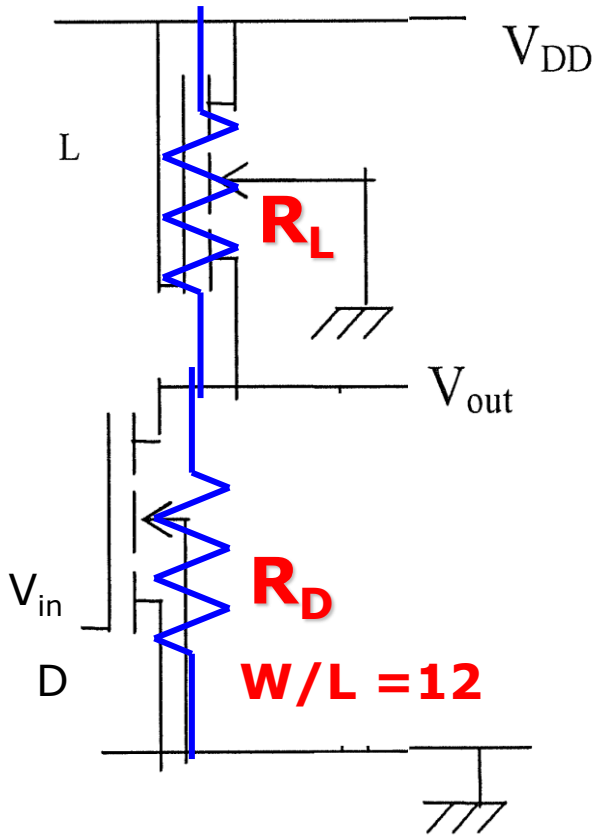
$$\rightarrow \mathbf{R_L \approx 5k\Omega}$$



$$\mathbf{I_D = \beta_L(V_{DD}-V_T)^2/2}$$

$$R_L = (V_{DD}-V_{out})/I_D = 4.9*2/[\beta_L(5-0.3)^2] = 5k\Omega$$

$$\rightarrow \beta_L = 8.9*10^{-5} \rightarrow \text{aspect ratio of load} = \underline{\mathbf{0.5}}$$



NMOS Logic (Inverter): Example 2

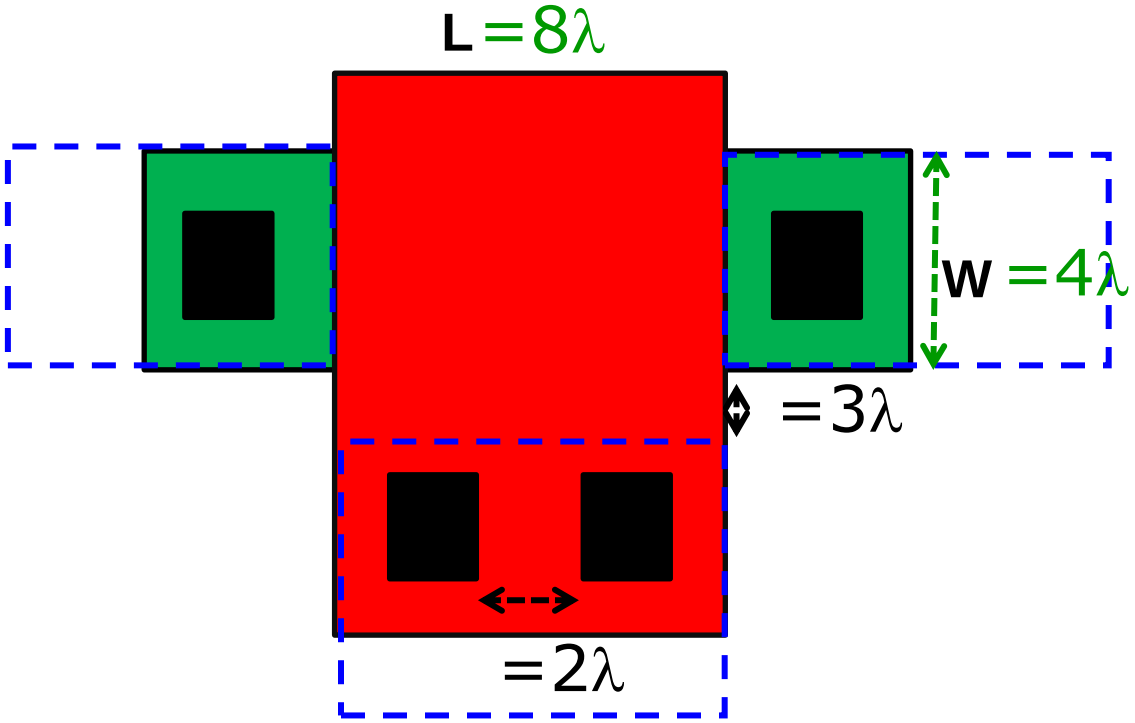
Calculate W/L of Load with the following specification:

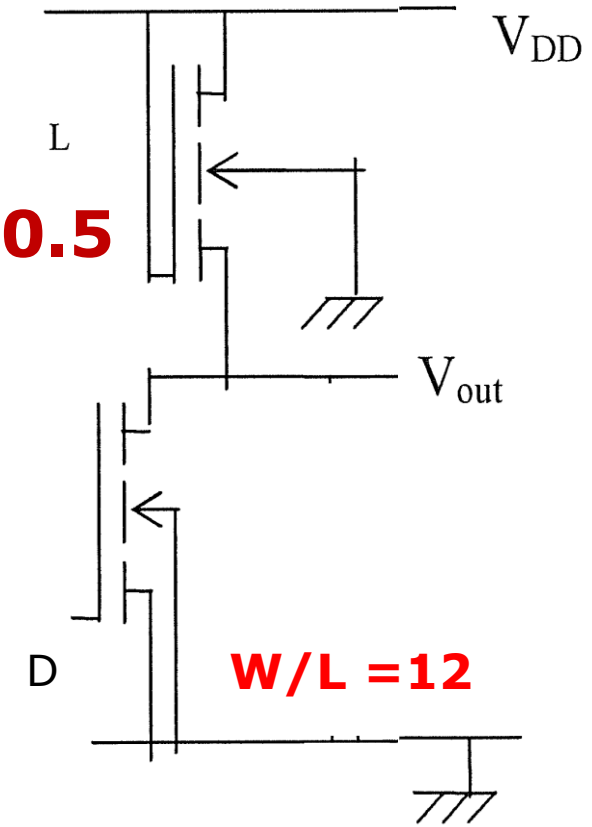
1) The aspect ratios of D is 12.

2) $\beta = \beta_0(W/L)$, and $\beta_0 = 1.8*10^{-4}AV^{-2}$.

3) $V_T = 0.3V$. 4) $V_{DD}=5V$.

W/L of Load= 0.5





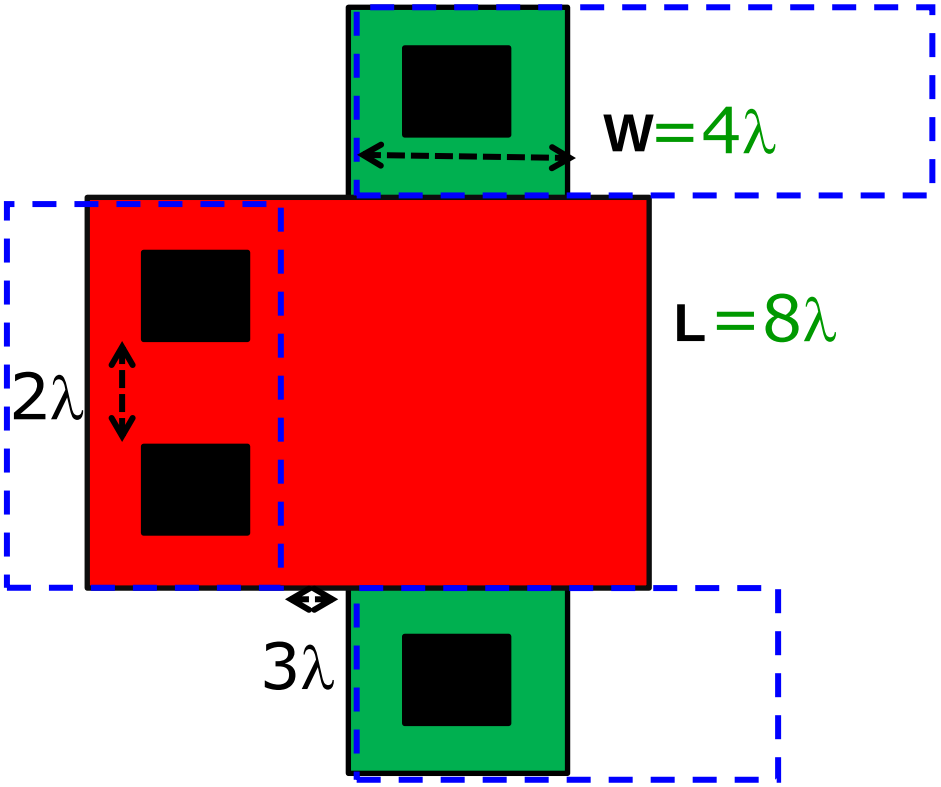
NMOS Logic (Inverter): Example 2

Calculate W/L of Load with the following specification:

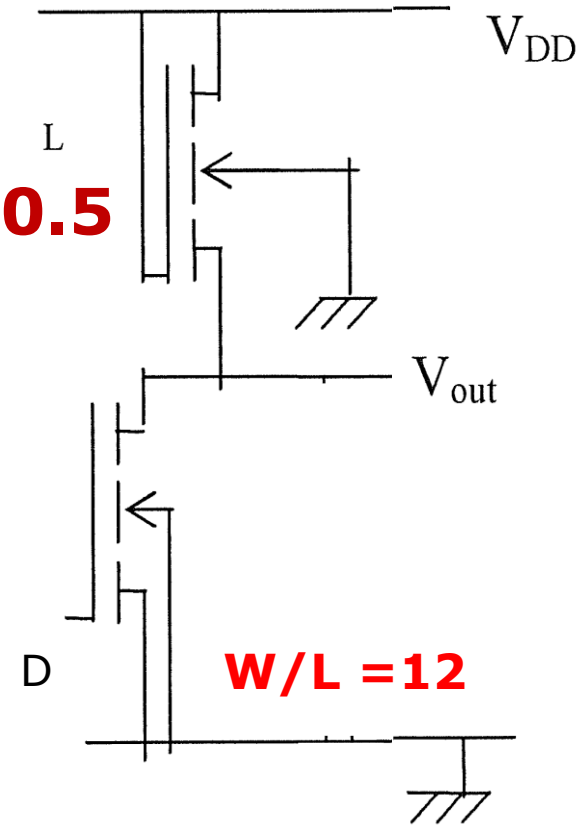
1) The aspect ratios of D is 12.

2) $\beta = \beta_0(W/L)$, and $\beta_0 = 1.8*10^{-4}AV^{-2}$.

3) $V_T = 0.3V$. 4) $V_{DD}=5V$.



W/L = 0.5



NMOS Logic (NOR): Example 3

Calculate W/L of Load with the following specification:

1) **The aspect ratios of D is 12.**
2) $\beta = \beta_0(W/L)$, and $\beta_0 = 1.8*10^{-4}AV^{-2}$.
3) $V_T = 0.3V$. 4) $V_{DD}=5V$.

Solution:

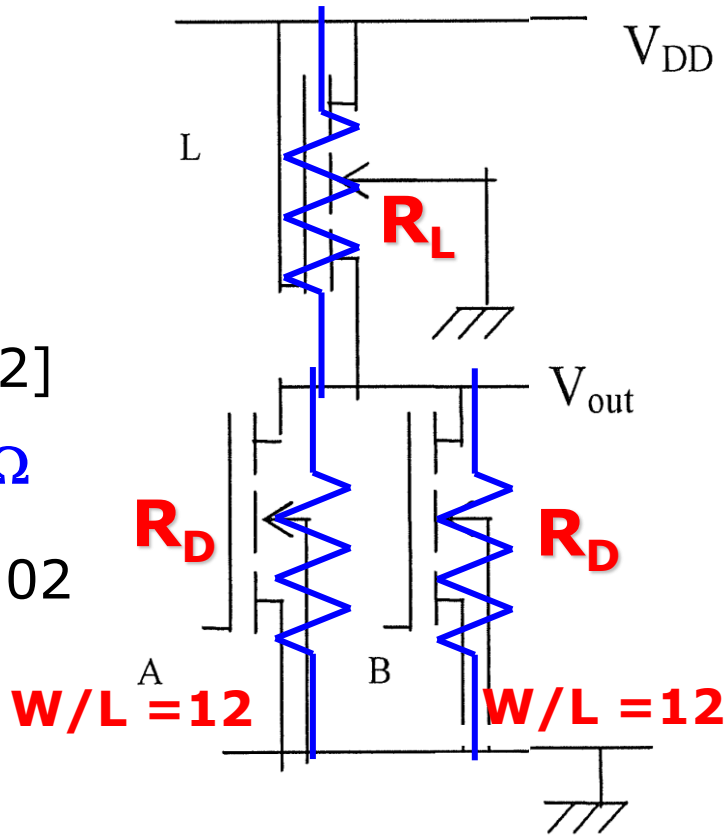
let $V_{Out} = 0.1V$:

$$I_D = \beta_D[(V_{inA}-V_T)V_{Out}-V_{Out}^2/2]$$

$$\mathbf{R_D = V_{Out}/I_D = (\beta_D[(V_{DD}-V_T)])^{-1} = 100\ \Omega}$$

$$[\mathbf{0.5}R_D/(\mathbf{0.5}R_D+R_L)]=V_{Out}/V_{DD}=0.1/5=0.02$$

$$\rightarrow \mathbf{R_L = 2.5k\Omega}$$



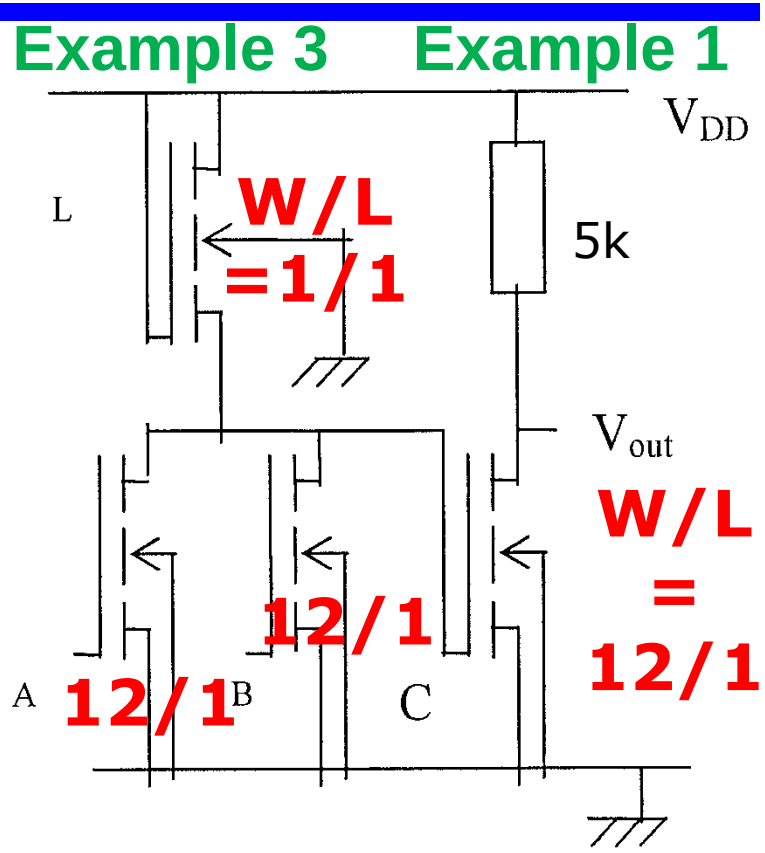
$$\mathbf{I_D = \beta_L(V_{DD}-V_T)^2/2}$$

$R_L = (V_{DD}-V_{out})/I_D = 4.9*2/[\beta_L(5-0.3)^2] = 2.5k\Omega$

$\rightarrow \beta_L = 1.8*10^{-4} \rightarrow$ aspect ratio of Load= **1**.

Example: Design Exercise 1

- It consists of an n channel NOR gate feeding an inverter.
- The transistors A and B are the termed driver MOSFETs.
- The process parameters are defined:
  - $2\lambda = 1\mu m$
  - $\beta_0 = 1.8 \times 10^{-4} AV^{-2}$
  - $V_T = 0.3V$
  - $V_{DD} = 5V$
  - $V_{in} = V_{DD}$
  - $R_S = 100\Omega/sq$



Example: Design Exercise 2

Layout design of the NMOS IC

- It consists of an n channel NOR gate feeding an inverter.
- The transistors A and B are the termed driver MOSFETs.
- The process parameters are defined:
  - $2\lambda = 1\mu m$
  - $\beta_0 = 1.8 \times 10^{-4} AV^{-2}$
  - $V_T = 0.3V$
  - $V_{DD} = 5V$
  - $V_{in} = V_{DD}$
  - $R_S = 100\Omega/sq$

$$\mu C_{ox} = \beta_0$$

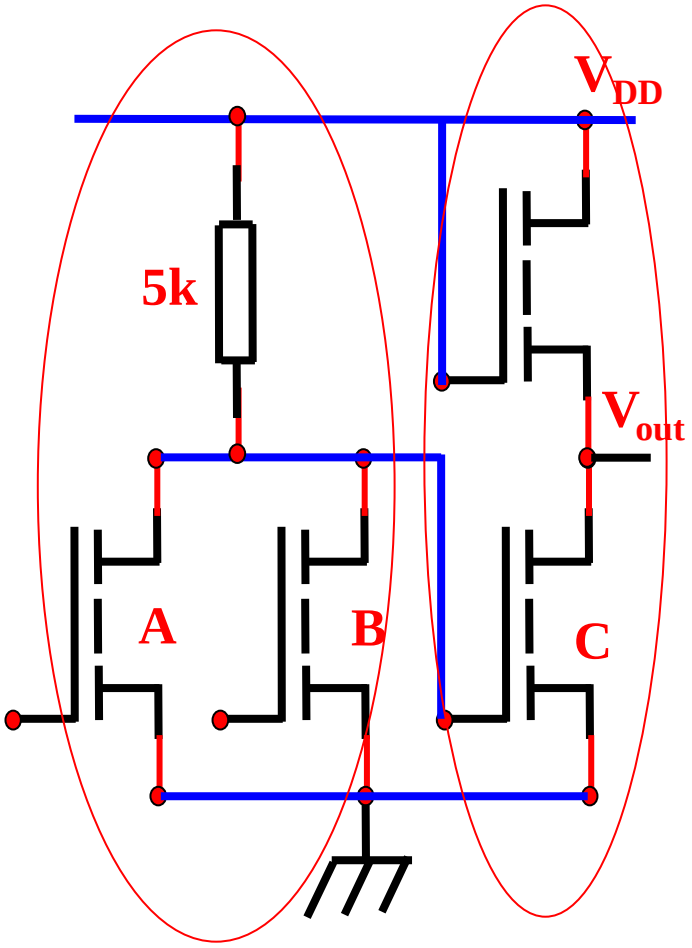


Fig.1

NMOS Logic (NOR): Example 4

Calculate W/L with the following specification:
1) R_L=5k. 2) $\beta = \beta_0(W/L)$, and $\beta_0 = 1.8*10^{-4}AV^{-2}$.
3) V_T =0.3V. 4) V_{DD}=5V.

Solution:

If $V_A=V_B=V_{DD}$, **let V_{Out} = 0.1V << V_T**

Potential divider:

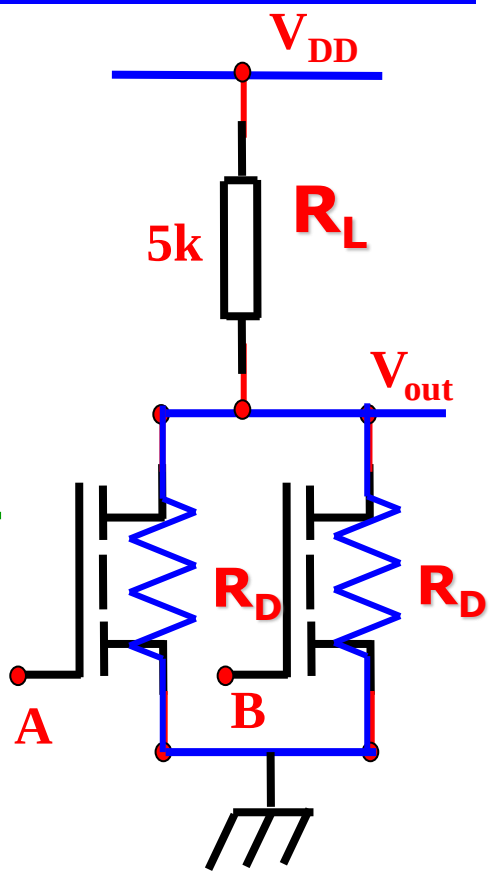
$0.5R_D/(0.5R_D+R_L)=V_{Out}/V_{DD}=0.1/5=0.02$

→ **$R_D \approx 200\Omega$**

$I_D= \beta[(V_G-V_T)V_D-V_D^2/2] \approx \beta[(V_G-V_T)V_D]$

$R_D=V_{Out}/I_D=\{\beta[(V_{DD}-V_T)]\}^{-1} =1/[\beta(5-0.3)]=200\Omega$

→ **$\beta \approx 10*10^{-4}$. Therefore, the aspect ratio, W/L, is 6**



Example: Design Exercise 2

Layout design of the nMOS IC shown in Fig.1

- It consists of an n channel NOR gate feeding an inverter.
- The transistors A and B are the termed driver MOSFETs.
- The process parameters are defined:
  - $2\lambda = 1\mu m$
  - $\beta_0 = 1.8 \times 10^{-4} AV^{-2}$
  - $V_T = 0.3V$
  - $V_{DD} = 5V$
  - $V_{in} = V_{DD}$
  - $R_S = 100\Omega/sq$

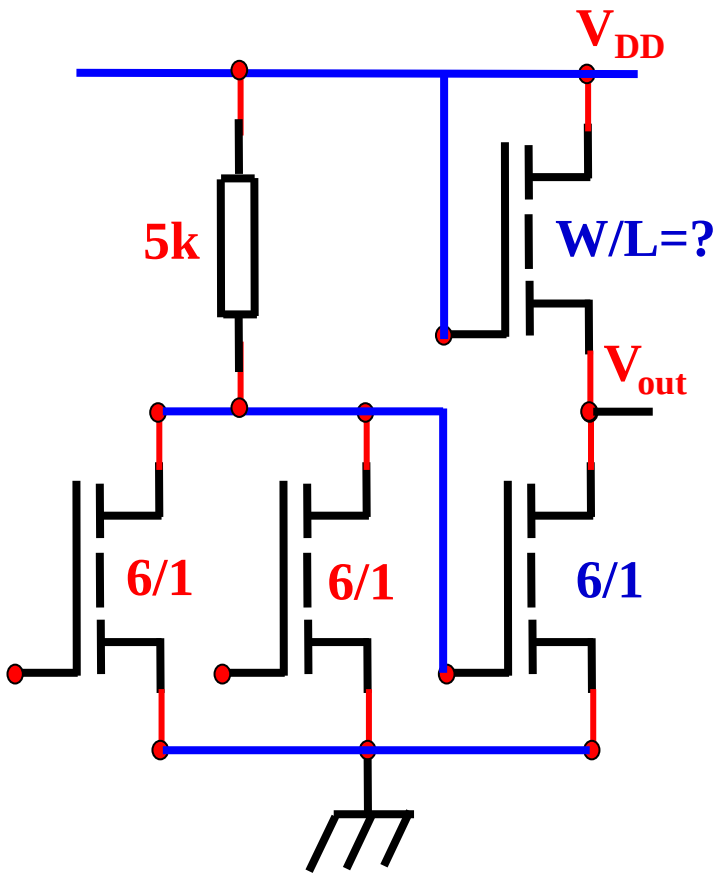


Fig.1

NMOS Logic (**Inverter**): **Example 5**

Calculate W/L of Load with the following specification:

1) The aspect ratios of D is **6**.
2) $\beta = \beta_0(W/L)$, and $\beta_0 = 1.8*10^{-4}AV^{-2}$.
3) $V_T = 0.3V$. 4) $V_{DD}=5V$.

Solution:

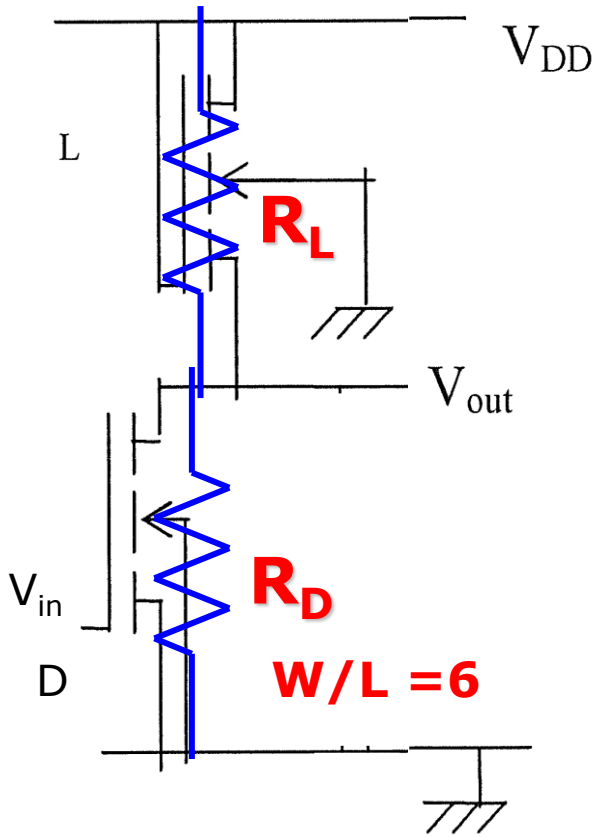
If $V_{in} = V_{DD}$, let $V_{Out} = 0.1V$:

$$I_D = \beta_D[(V_{in}-V_T)V_{Out}-V_{Out}^2/2]$$

$$\mathbf{R_D = V_{Out}/I_D = (6\beta_0[(V_{DD}-V_T)])^{-1} = 200\ \Omega}$$

$$[R_D/(R_D+R_L)]=V_{Out}/V_{DD}=0.1/5=0.02$$

$$\rightarrow \mathbf{R_L \approx 10k\Omega}$$



$$\mathbf{I_D = \beta_L(V_{DD}-V_T)^2/2}$$

$R_L = (V_{DD}-V_{out})/I_D = 4.9*2/[\beta_L(5-0.3)^2] = 10k\Omega$

$\rightarrow \beta_L = 4.4*10^{-5} \rightarrow$ aspect ratio of load = **0.25**

Example: Design Exercise 2

Layout design of the nMOS IC shown in Fig.1

- It consists of an n channel NOR gate feeding an inverter.
- The transistors A and B are the termed driver MOSFETs.
- The process parameters are defined:
  - $2\lambda = 1\mu m$
  - $\beta_0 = 1.8 \times 10^{-4} AV^{-2}$
  - $V_T = 0.3V$
  - $V_{DD} = 5V$
  - $V_{in} = V_{DD}$
  - $R_S = 100\Omega/sq$

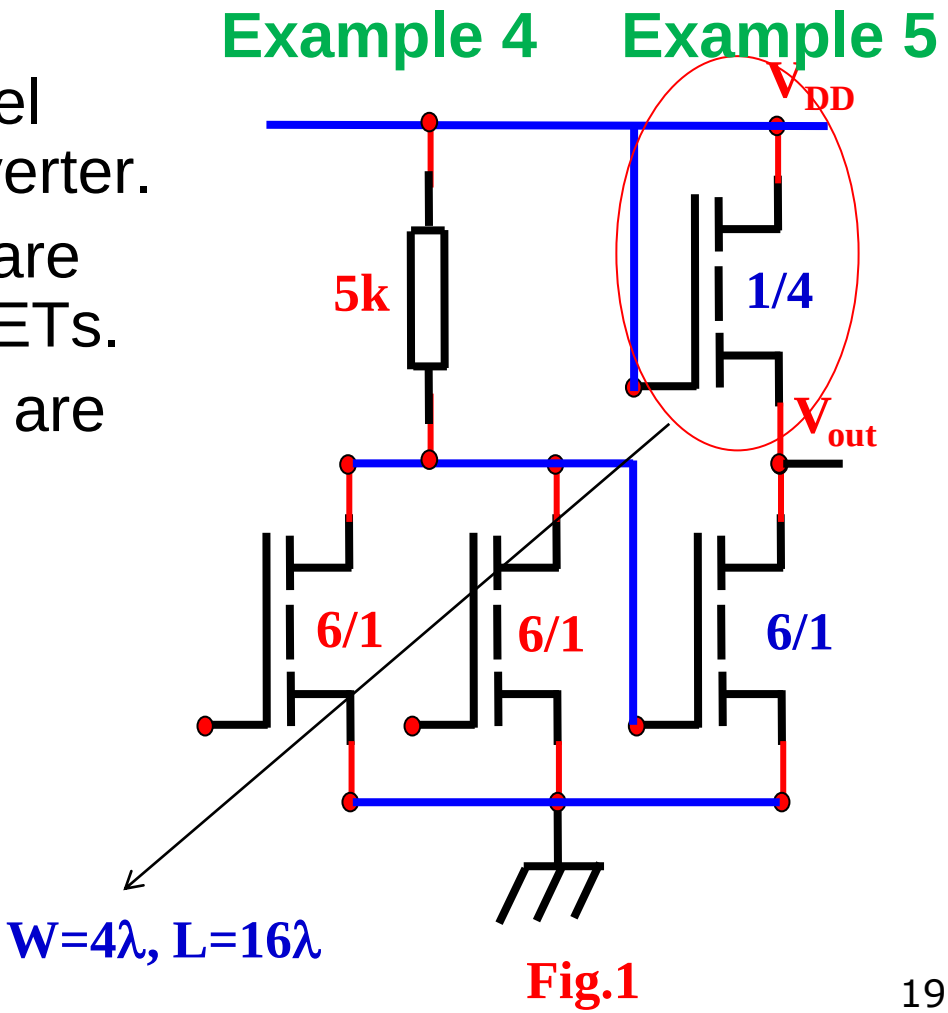
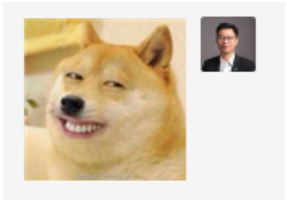


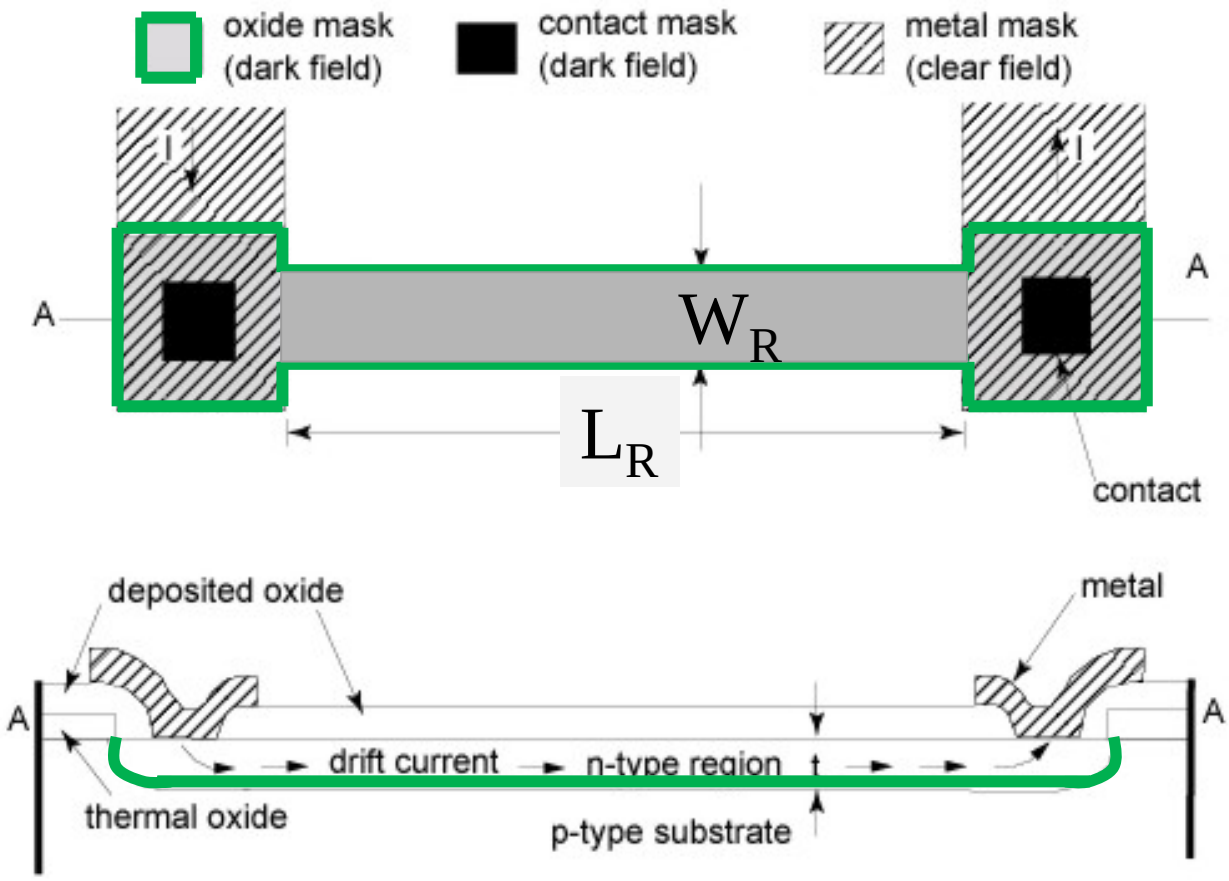
Fig.1

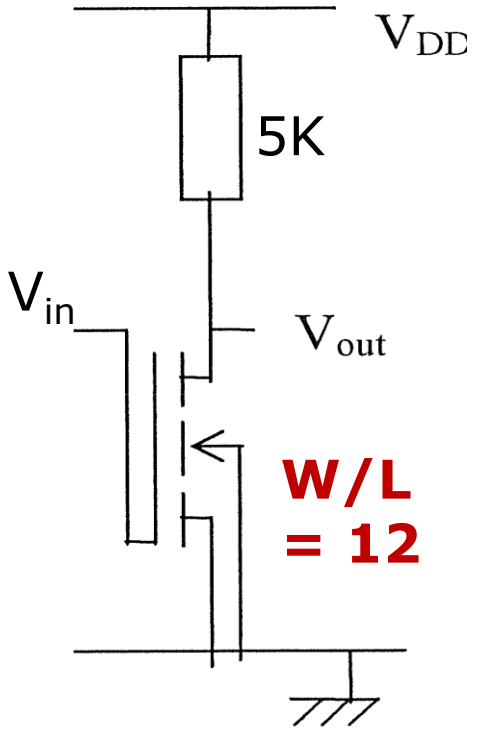
OUTLINE

- NMOS logic (examples)
  - Calculation
  - Layout
- Design Exercise

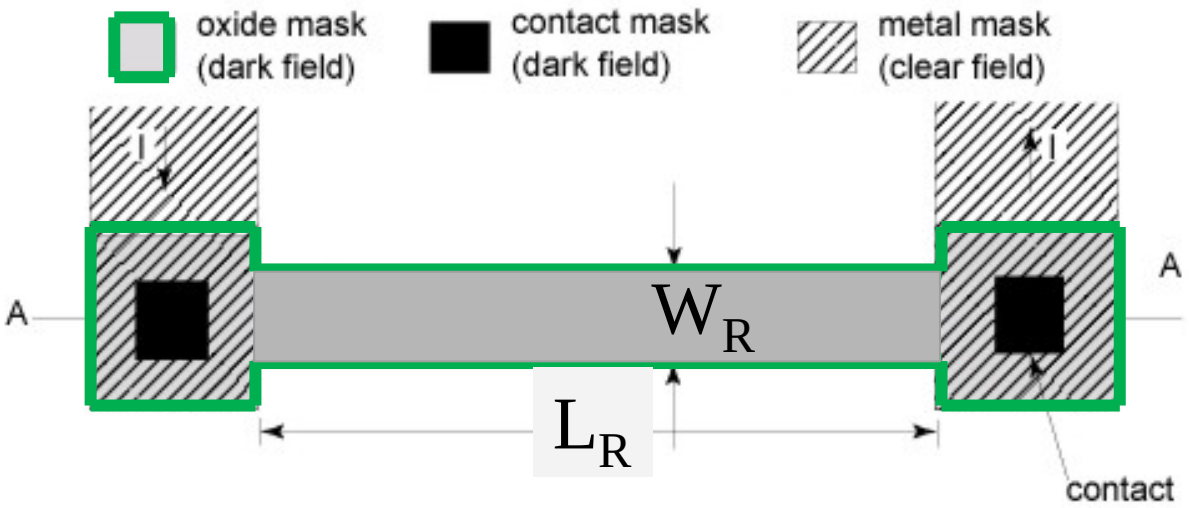


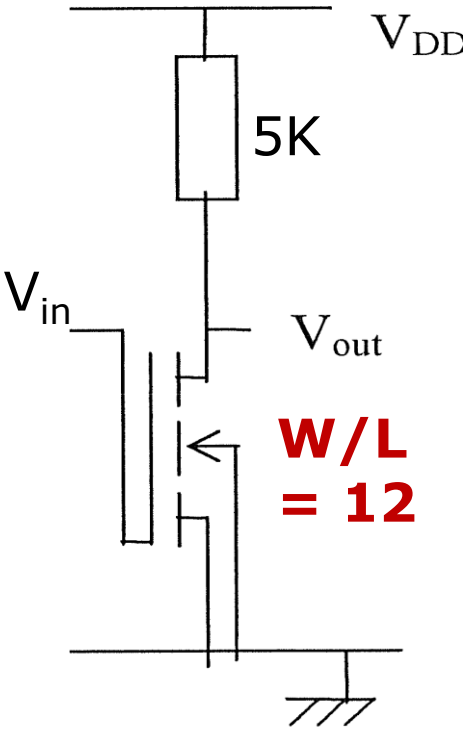
NMOS Logic (Inverter): Example 1



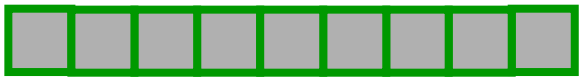


NMOS Logic (Inverter): Example 1

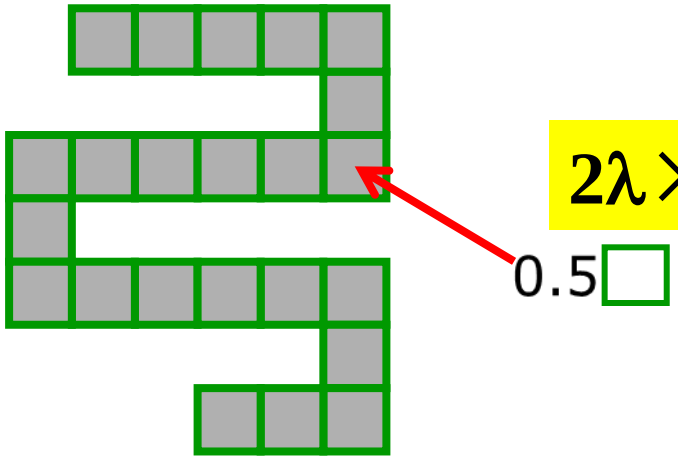




For small L_R/W_R:
(e.g. L_R/W_R=9)

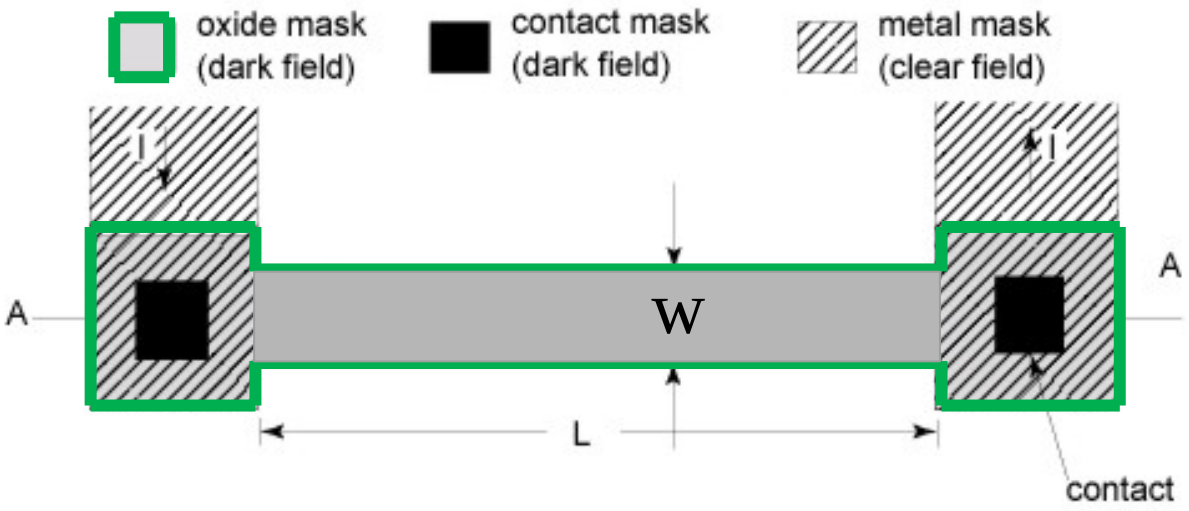


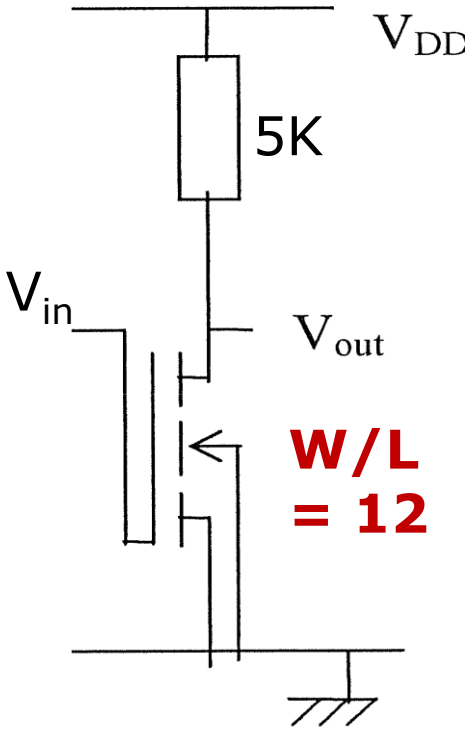
For large L_R/W_R:
(e.g. L_R/W_R=20)



Squares are used to calculate the length, L.

NMOS Logic (Inverter): Example 1



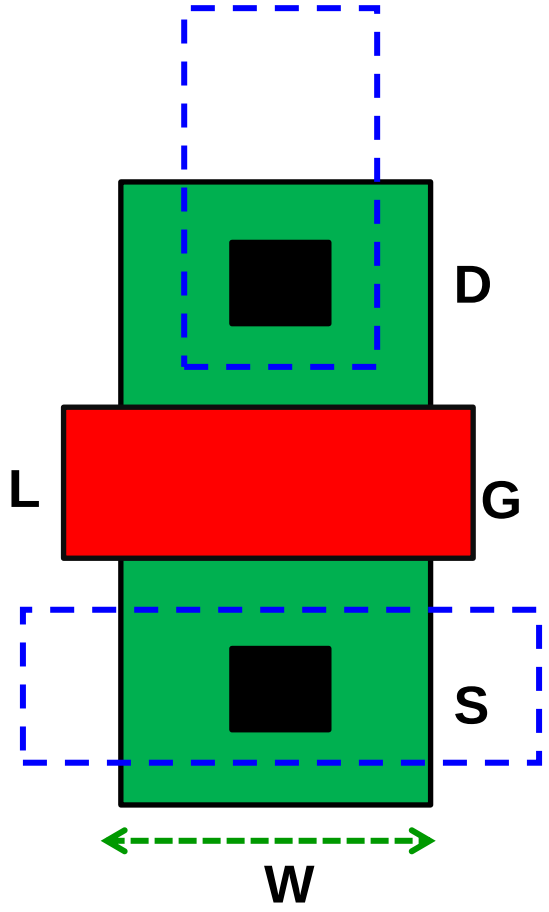


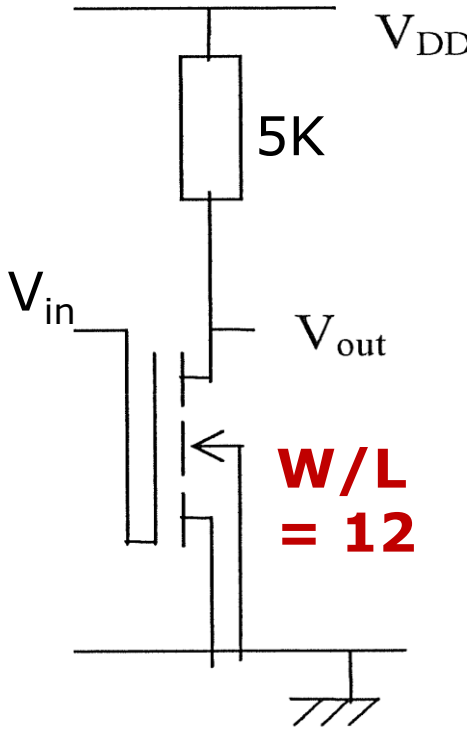
For small L_R/W_R:
(e.g. L_R/W_R=9)

For large L_R/W_R:
(e.g. L_R/W_R=20)

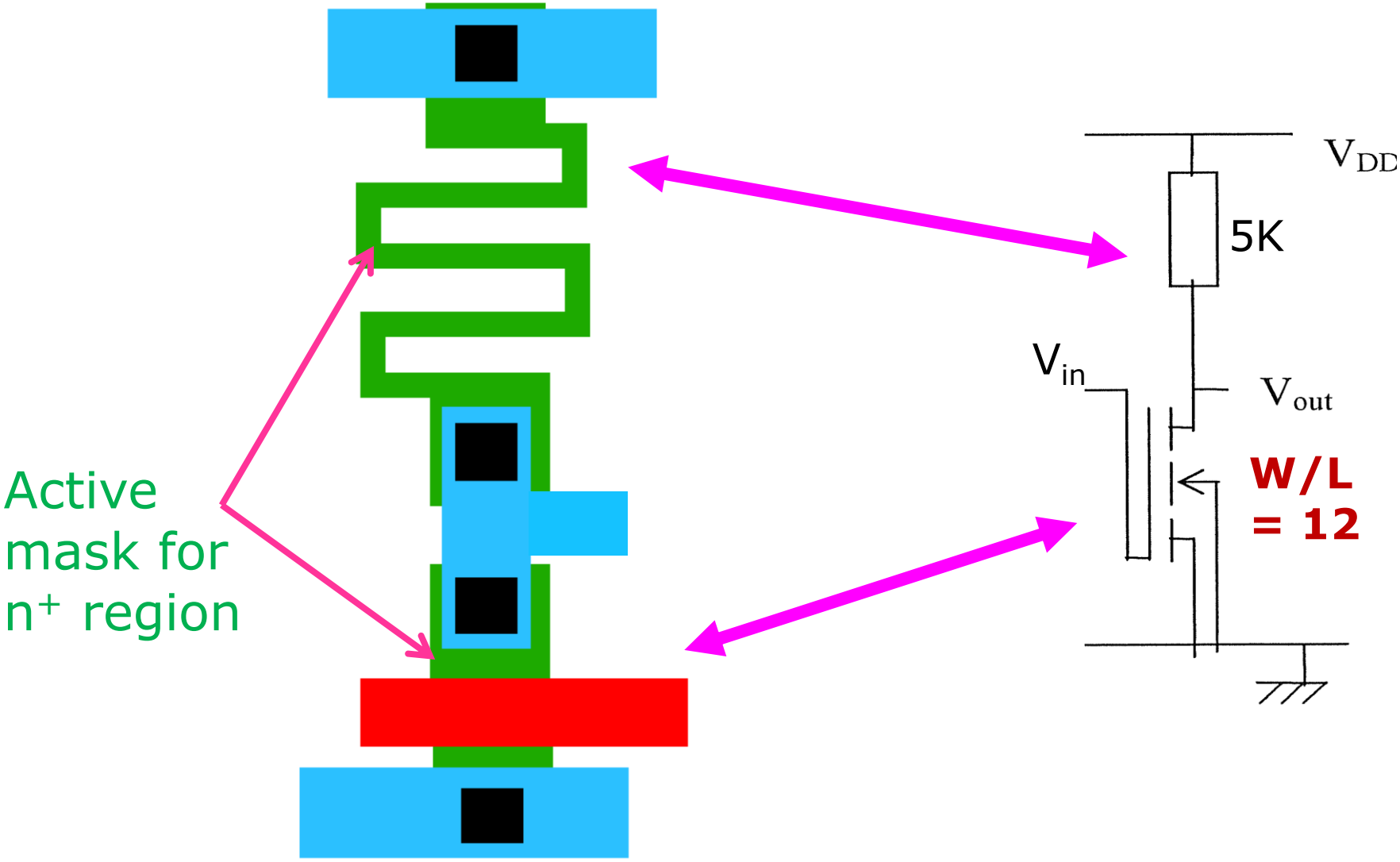
Every square must disappear when drawing your layout

NMOS Logic (Inverter): Example 1





NMOS Logic (**Inverter**): **Example 1**

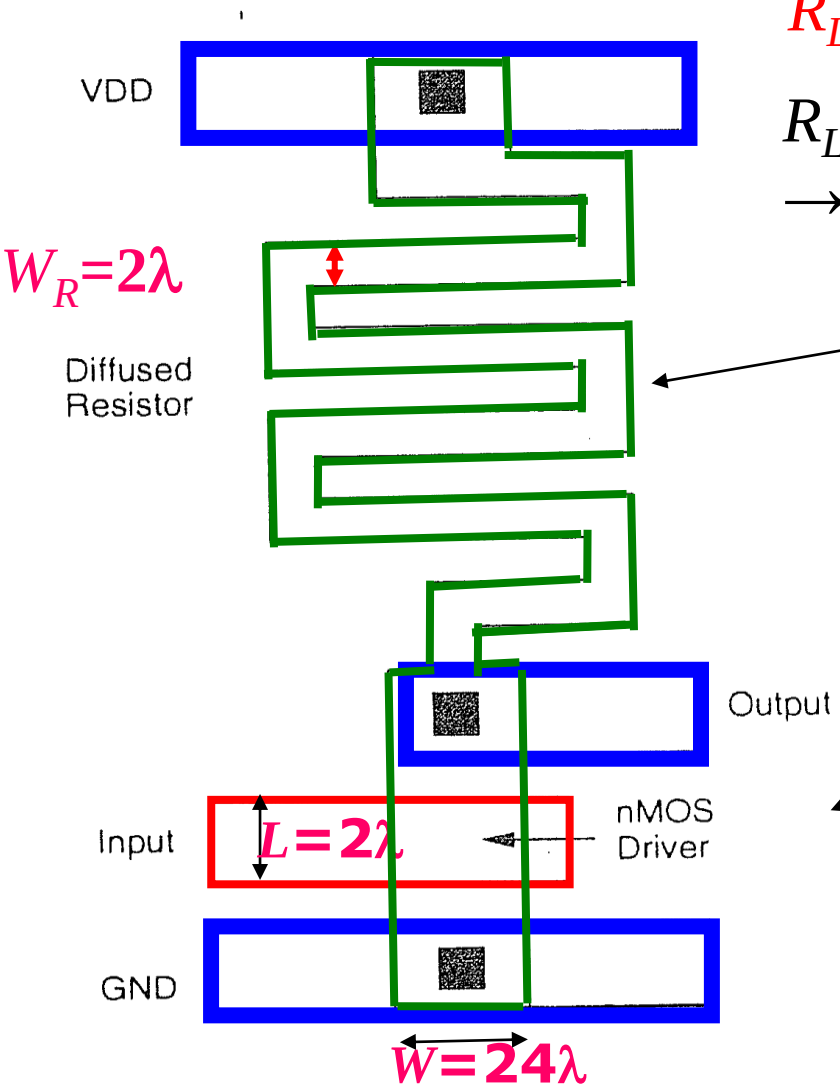


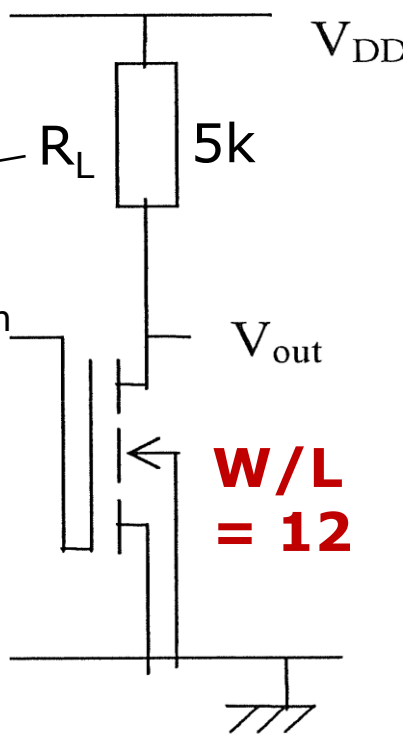
NMOS Logic (Inverter): Example 1

R_L=5k & R_s=100Ω/sq

$R_L=R_s(L_R/W_R)$

$\rightarrow L_R/W_R=50$



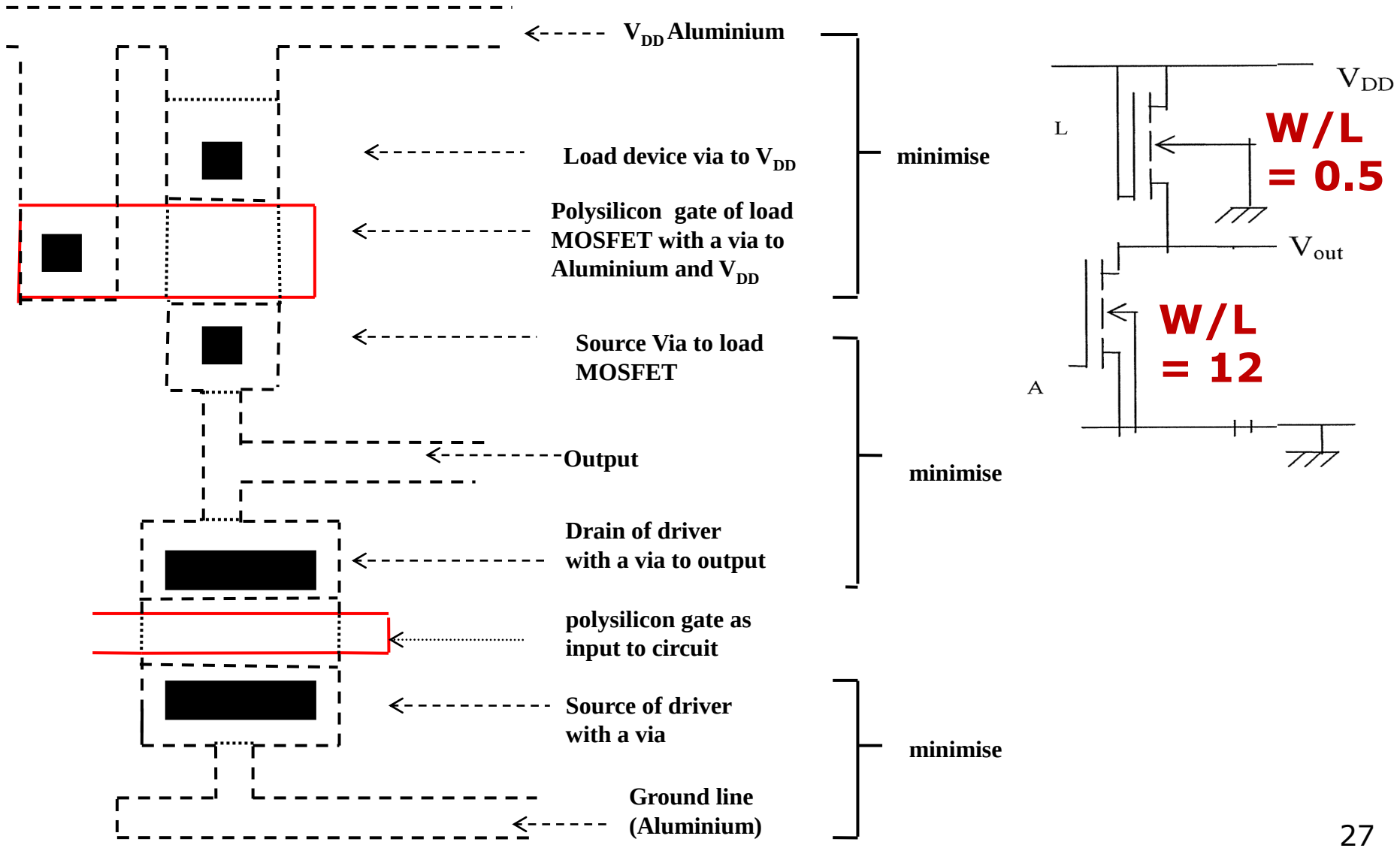


MOSFET

$\rightarrow W/L=12$

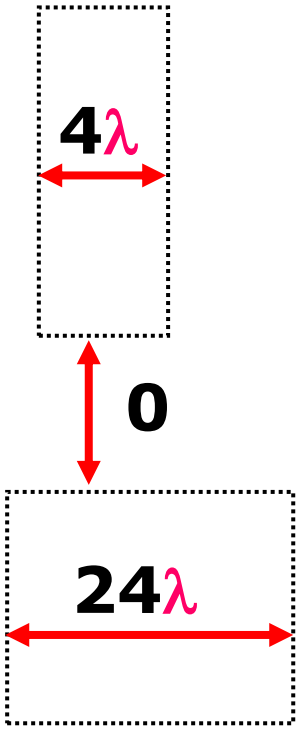
W/L = 12

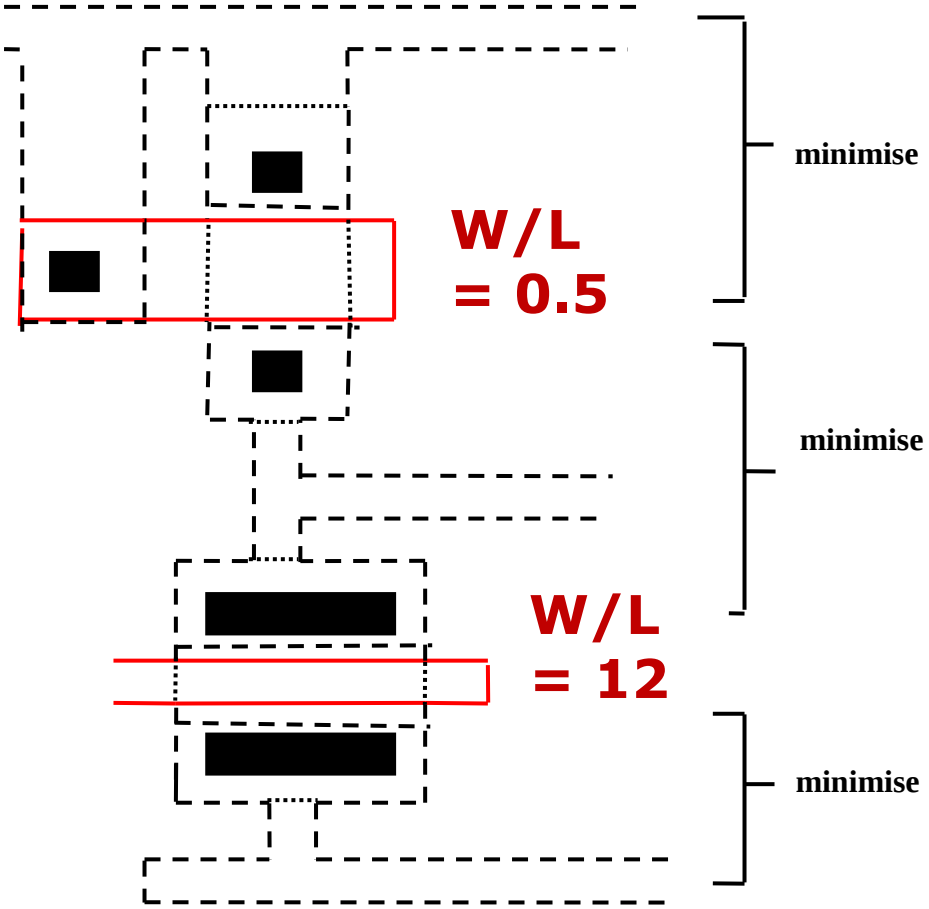
NMOS Logic (Inverter): Example 2



NMOS Logic (Inverter): Example 2

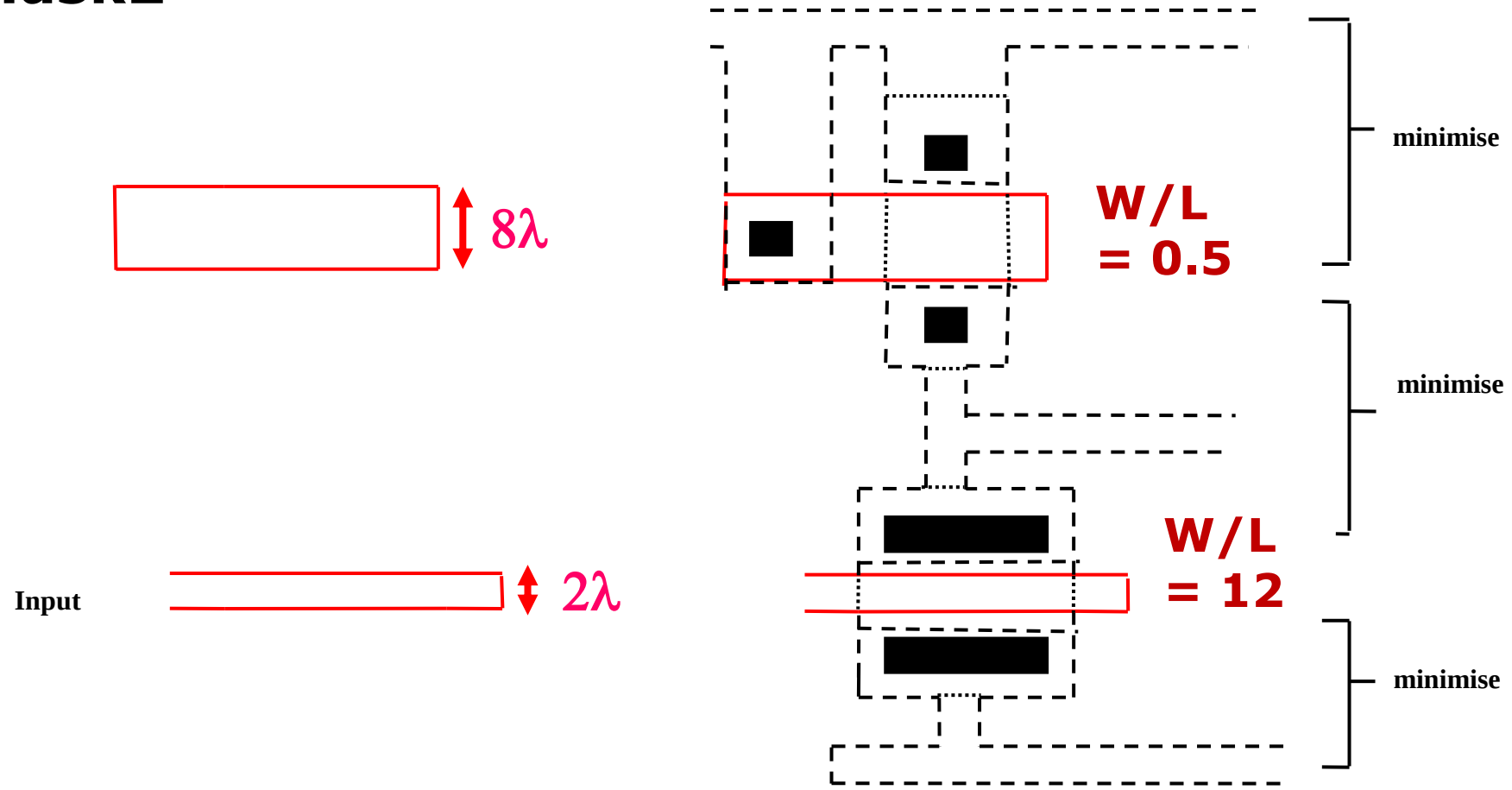
Mask1





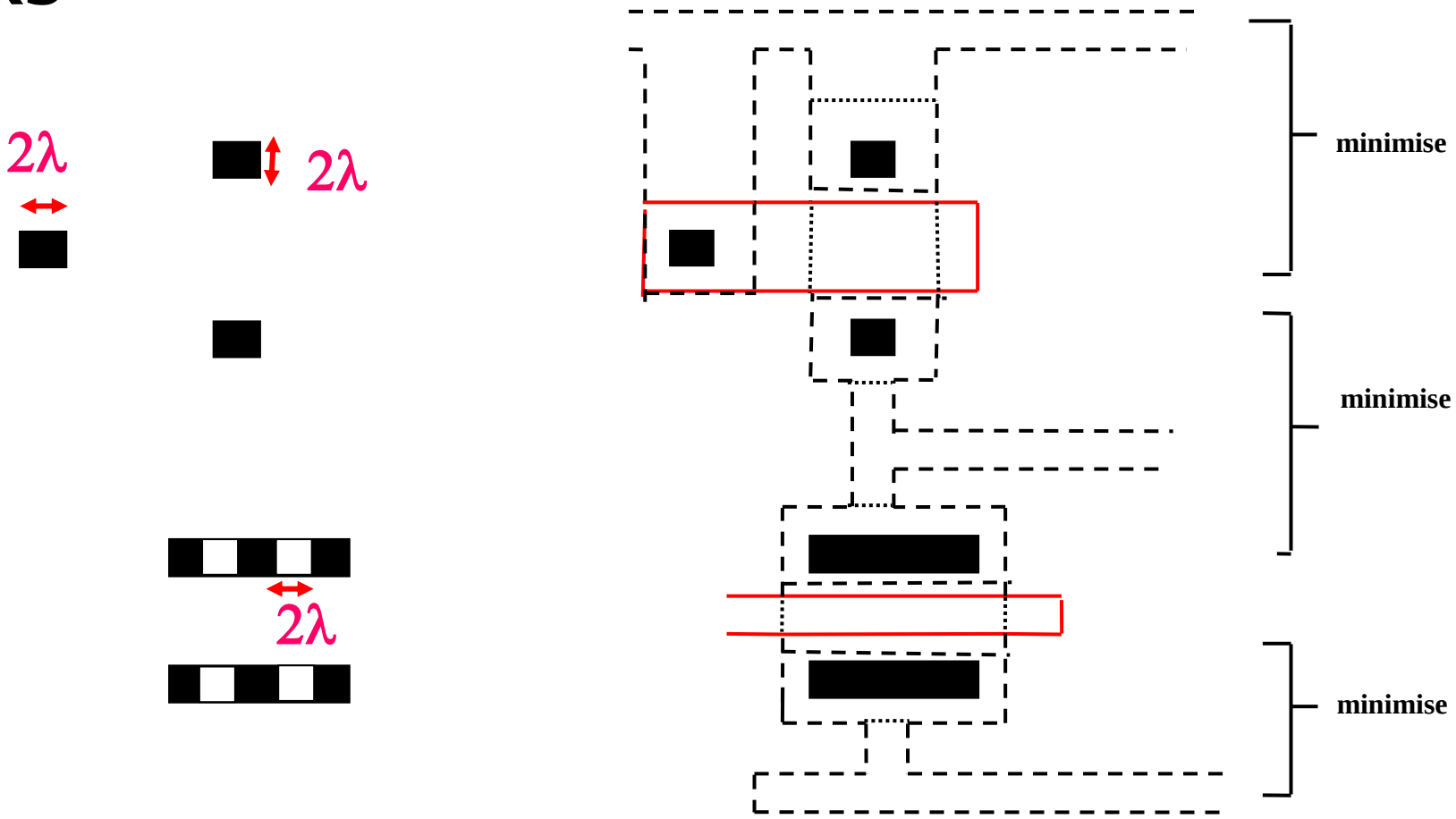
NMOS Logic (Inverter): Example 2

Mask2



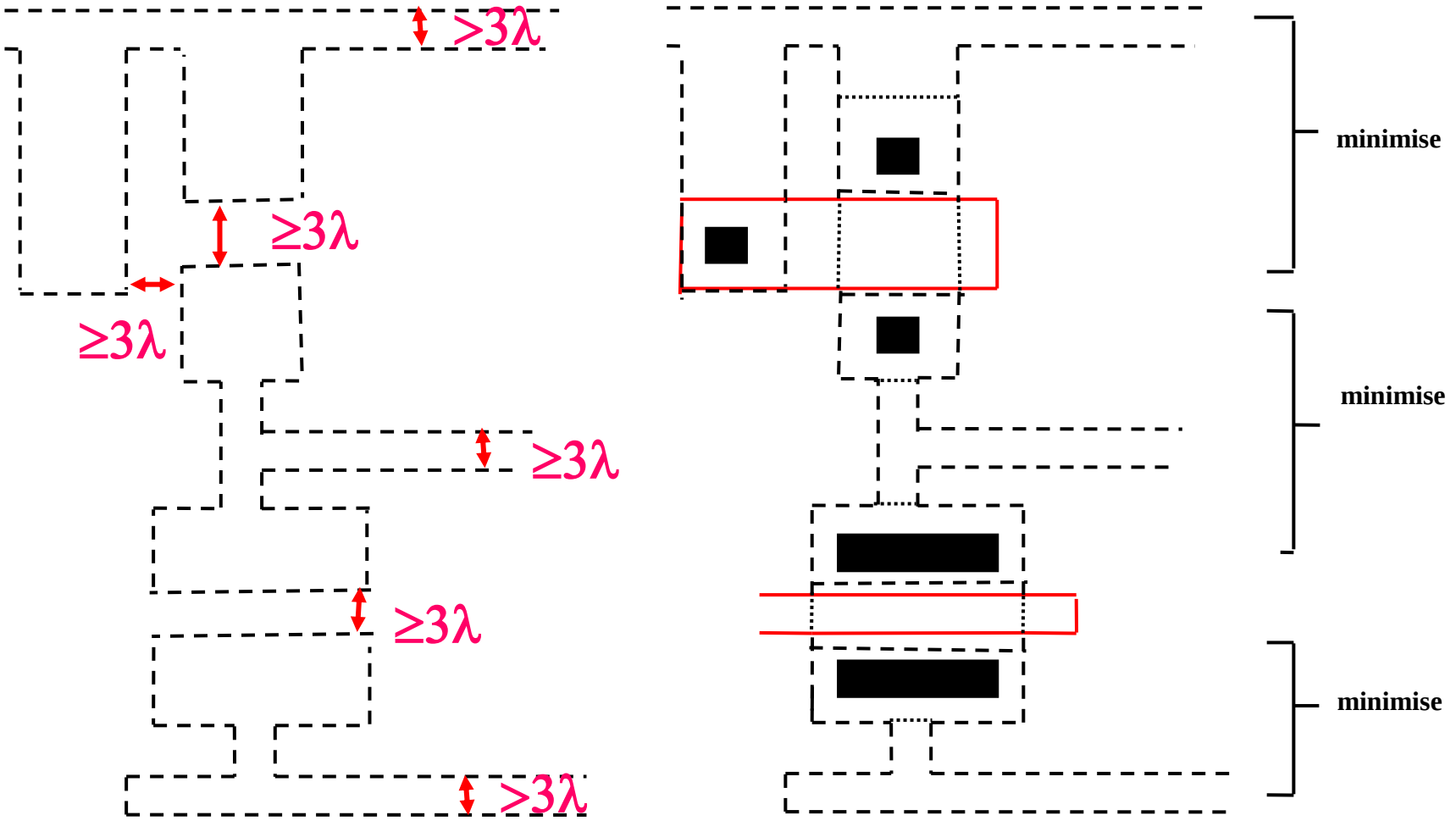
NMOS Logic (Inverter): Example 2

Mask3

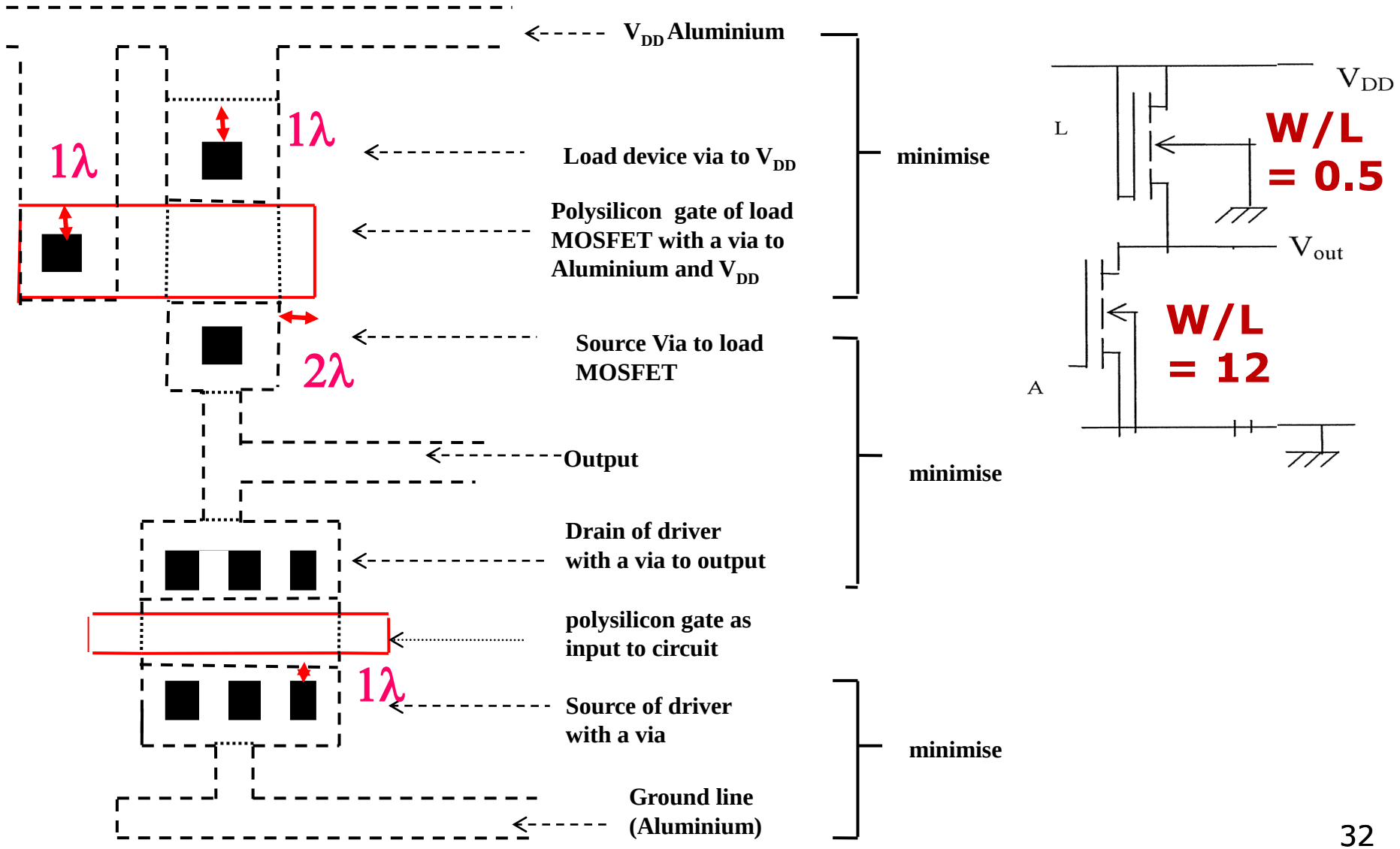


NMOS Logic (Inverter): Example 2

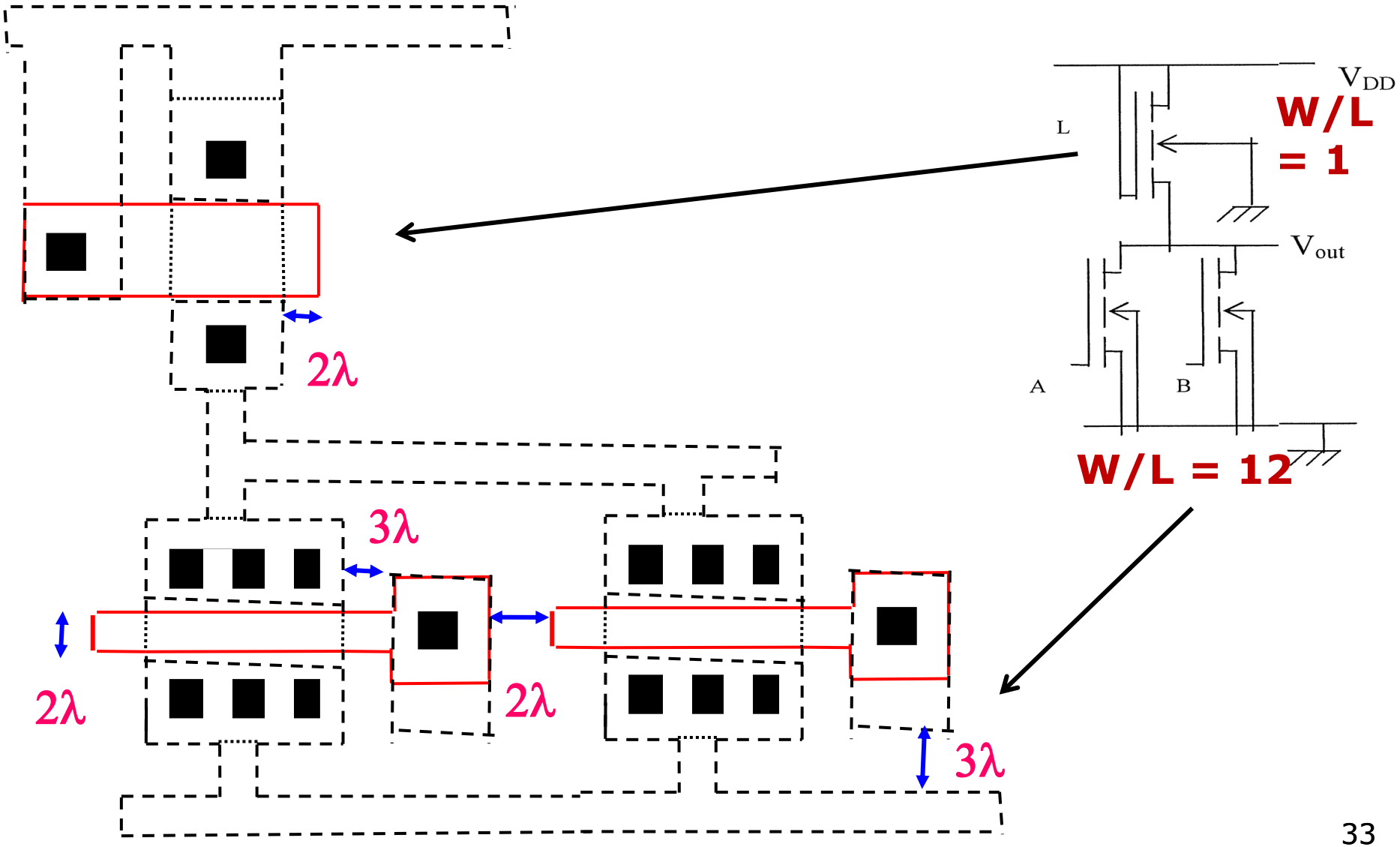
Mask4



NMOS Logic (Inverter): Example 2

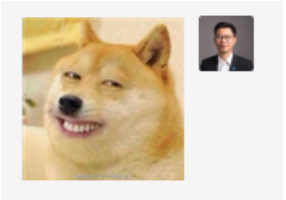


NMOS Logic (NOR): Example 3



OUTLINE

- NMOS logic (examples)
  - Calculation
  - Layout
- Design Exercise



Example: Design Exercise 2

Layout design of the nMOS IC shown in Fig.1

- It consists of an n channel NOR gate feeding an inverter.
- The transistors A and B are the termed driver MOSFETs.
- The process parameters are defined:
  - $2\lambda = 1\mu m$
  - $\beta_0 = 1.8 \times 10^{-4} AV^{-2}$
  - $V_T = 0.3V$
  - $V_{DD} = 5V$
  - $V_{in} = V_{DD}$
  - $R_S = 100\Omega/sq$

$$\mu C_{ox} = \beta_0$$

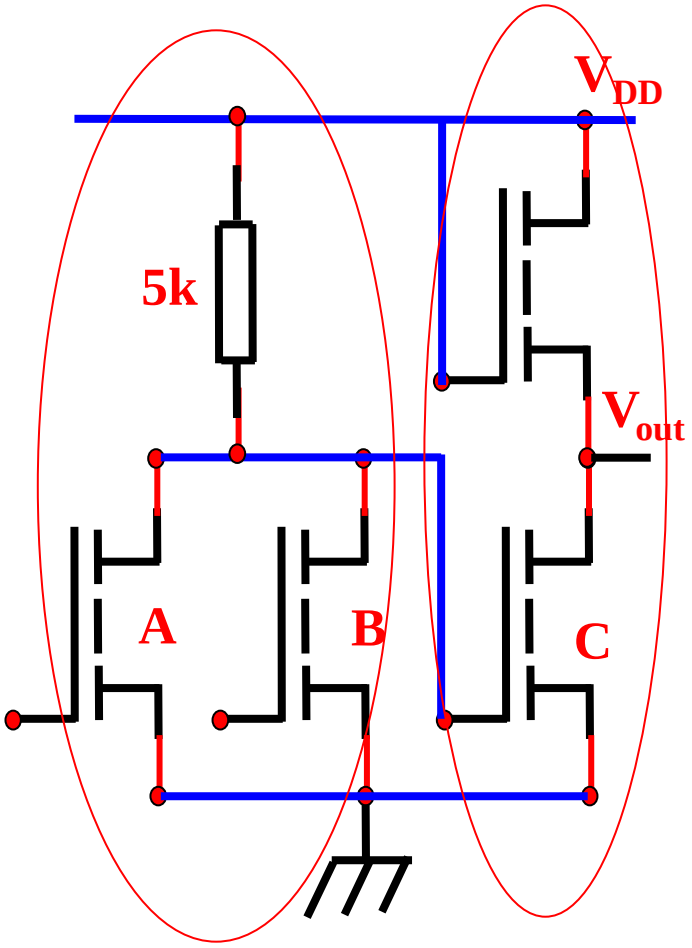
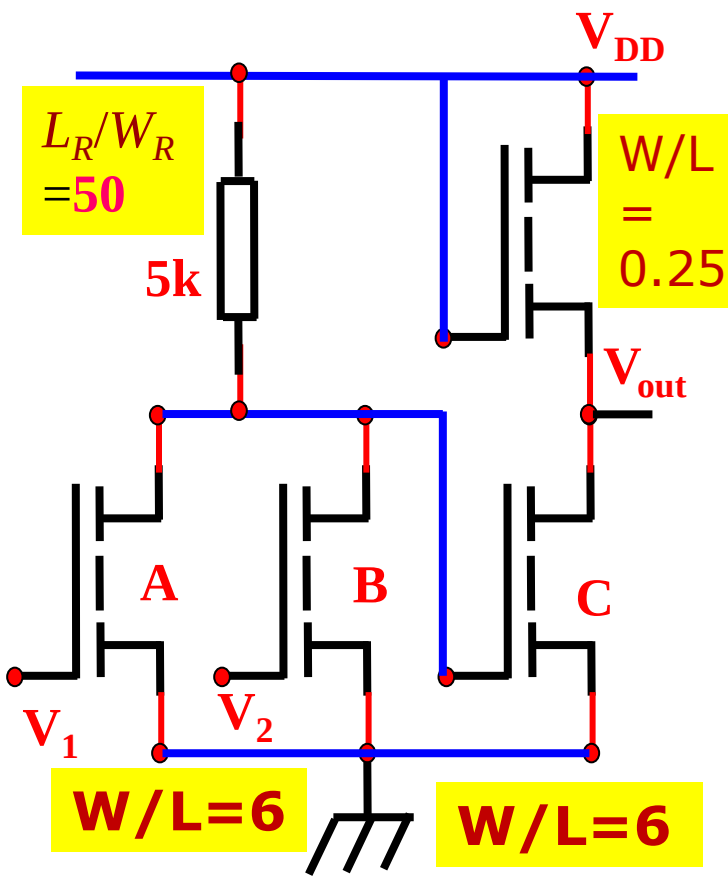


Fig.1

Example: Design Exercise 2

- Design rules:
- The driver transistors should have channel length L equal to the minimum feature size λ_m. The width of the drivers W, which must always be a whole number (n) of minimum feature sizes ($n\lambda_m$), and **the overall value of W must be chosen to give the required output voltage.** This must be significantly less than the threshold voltage of the third gate C if this transistor is to stay off.
- The layouts must take account of the alignment accuracy λ_a.
- $\lambda_m = 2\lambda_a$



Example: Design Exercise 2

1) The Design involves producing the patterns corresponding to each of the stages of the process already discussed.

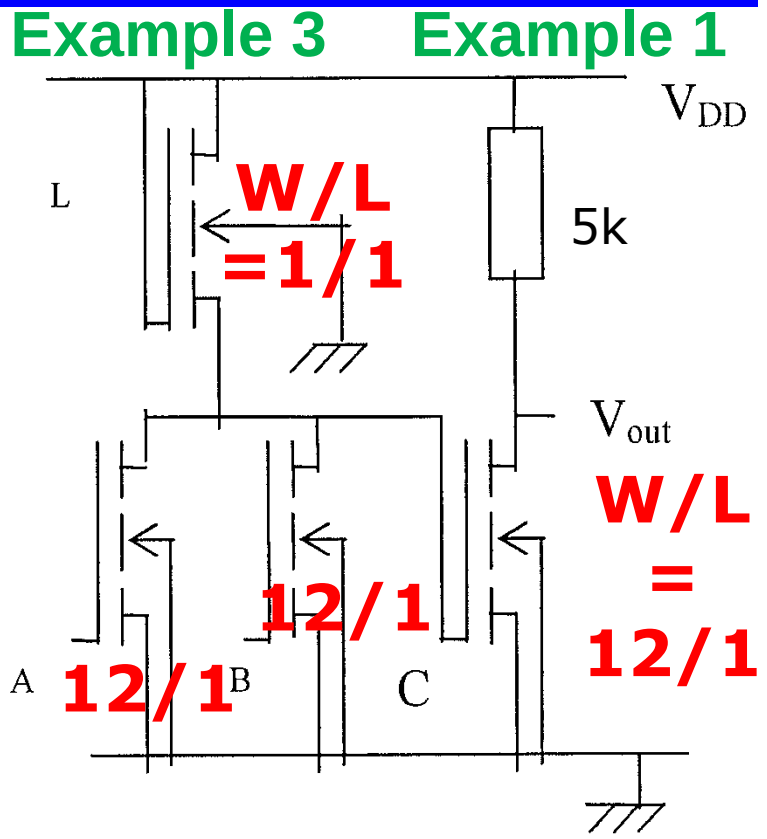
2) Each of the patterns should be drawn on graph paper with a stipulated scale. (e.g **1μm per cm**.)

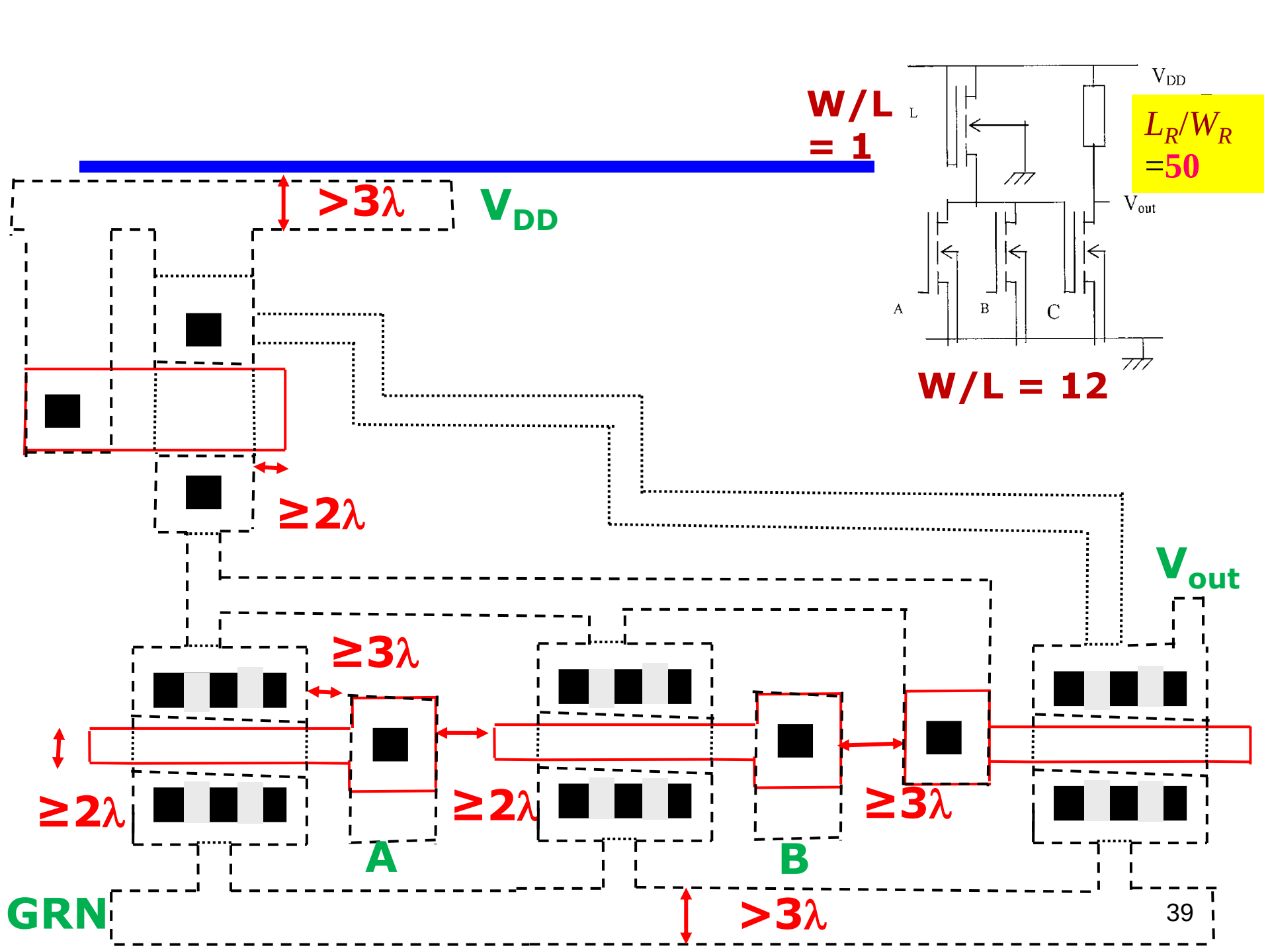
3) The patterns would be transferred at a later stage to glass masks, as opaque regions. There are 4 masks :

M1. define the device area (active)
M2. define the gate stripe (poly)
M3. define the contacts (contact)
M4. define the metal pattern (metal)

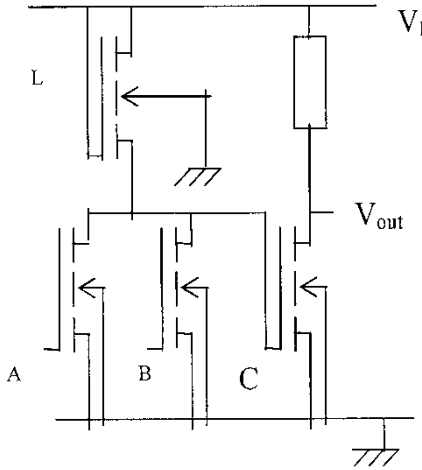
Example: Design Exercise 1

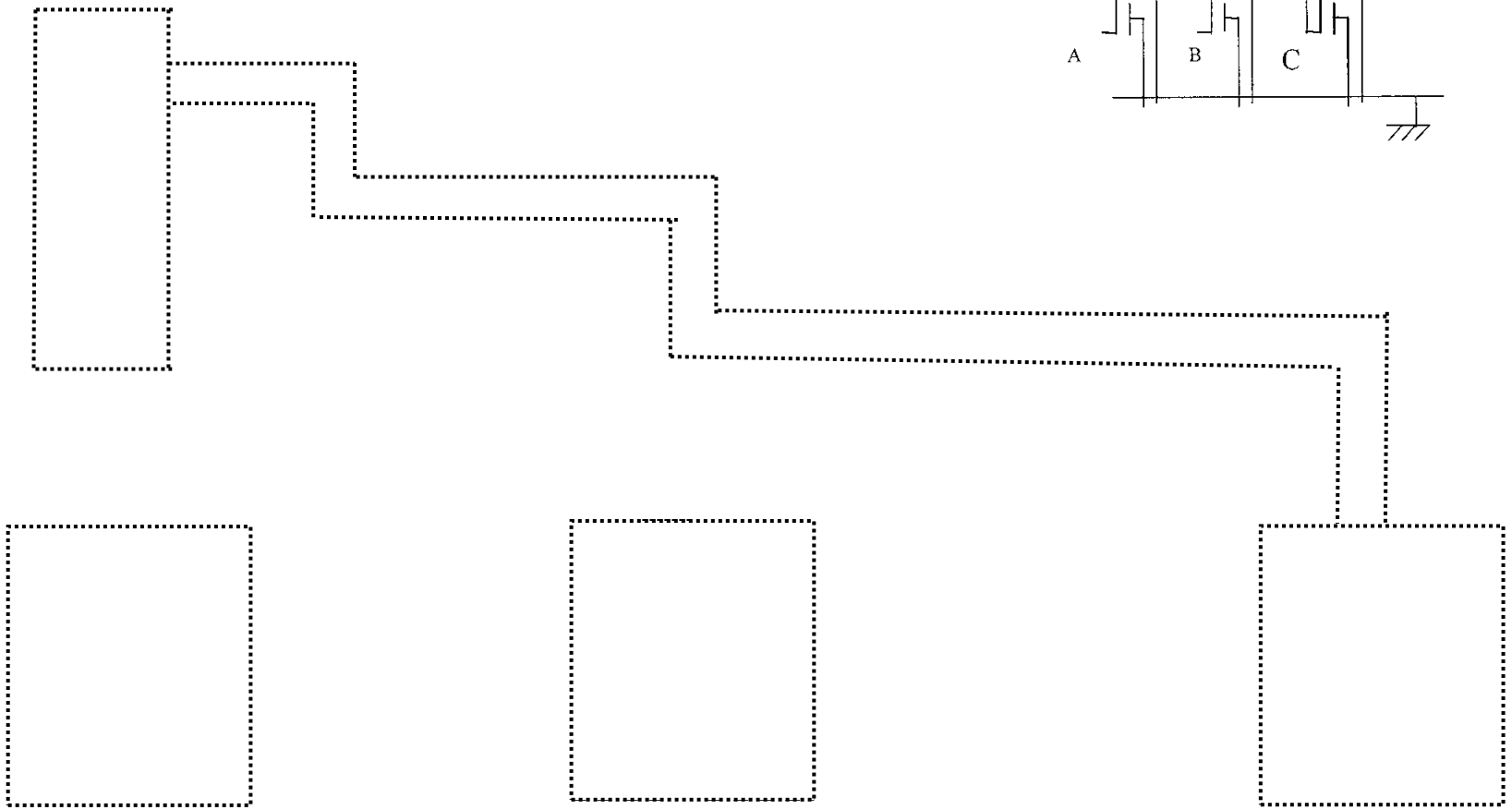
- It consists of an n channel NOR gate feeding an inverter.
- The transistors A and B are the termed driver MOSFETs.
- The process parameters are defined:
  - $2\lambda = 1\mu m$
  - $\beta_0 = 1.8 \times 10^{-4} AV^{-2}$
  - $V_T = 0.3V$
  - $V_{DD} = 5V$
  - $V_{in} = V_{DD}$
  - $R_S = 100\Omega/sq$
- HINTS: Liverpool notes.



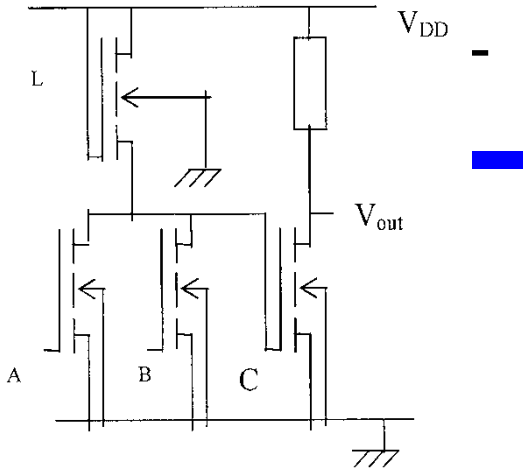

W/L
= 1
>3λ
V_DD
≥2λ
≥3λ
≥2λ
A
≥2λ
B
≥3λ
V_out
GRN
>3λ
V_DD
L
V_out
A
B
C
W/L = 12
L_R/W_R
=50

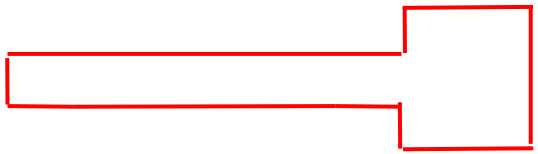
Mask1

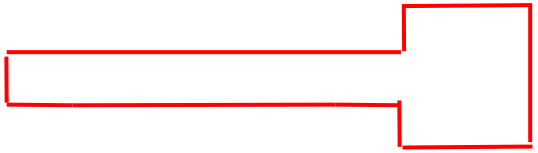


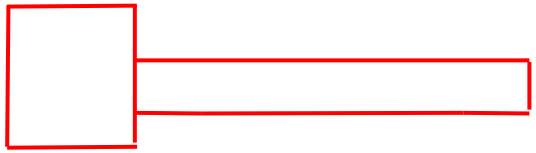


Mask2

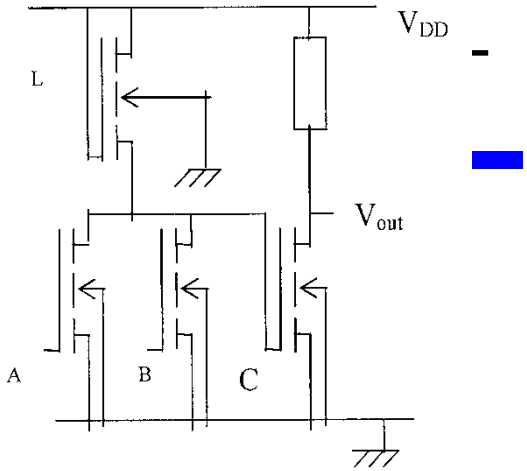


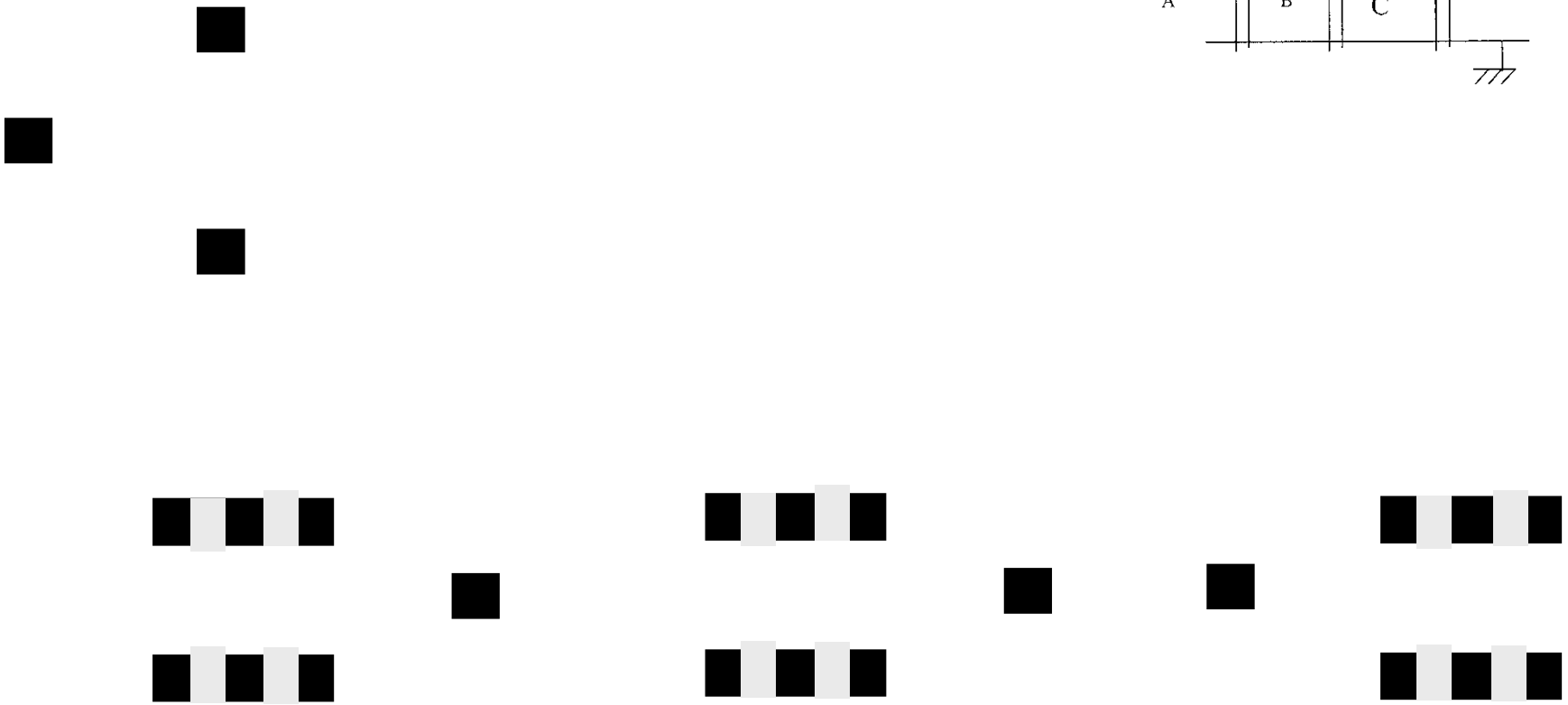






Mask3





Mask4