Lecture 9

of

EEE201

CMOS Digital Integrated Circuits

Department of Electrical & Electronic Engineering

Xi'an Jiaotong-Liverpool University (XJTLU)

Monday, 04th November 2024

❑ Drawing CMOS IC Layout

- ➢ CMOS inverter: schematic to device structure
- ➢ seven mask layers
- ➢ drawing each mask layer to give the layout

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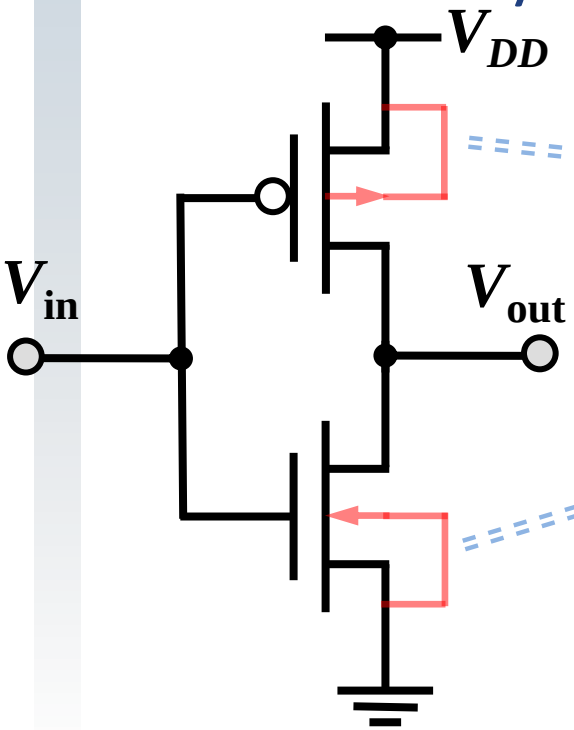
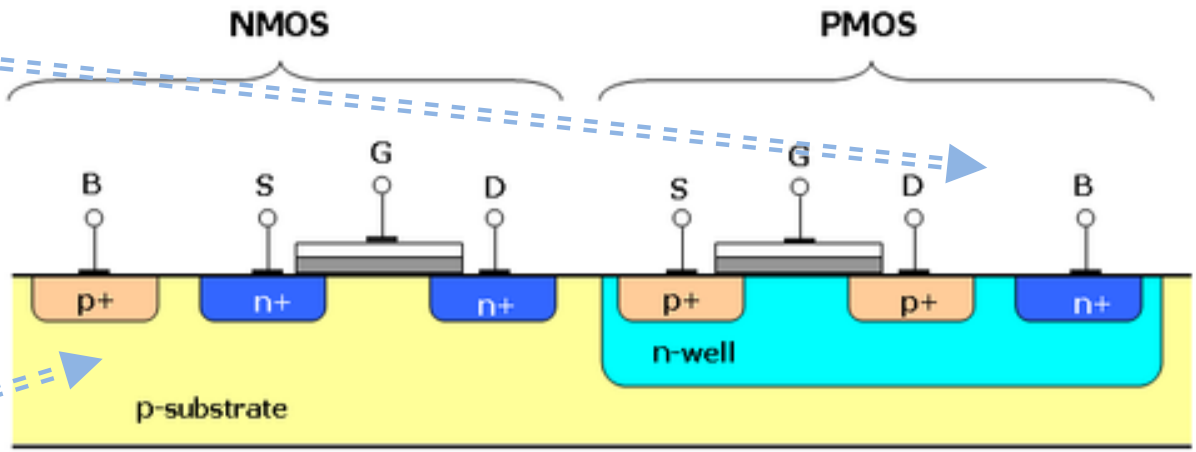
CMOS Inverter

(from schematic design to device structures on wafer)

- To make the CMOS inverter (and in general CMOS digital ICs), the ***p***MOSFET and ***n***MOSFET fabrication on a silicon wafer need to be well-defined by a set of mask layers in the IC layout.

Note the explicit substrate contacts in the structure.





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CMOS Inverter

(from schematic design to device structures on wafer)

- To fabricate NMOS transistors alone on a ***p***-type silicon wafer, at least four masks are needed.
  $\Rightarrow$ four mask layers in the IC layout for NMOS transistors
- To fabricate both NMOS and PMOS transistors on a ***p***-type silicon wafer, at least seven masks are needed: $\Rightarrow$ 7 mask layers in the IC layout for CMOS circuits

  Mask 1: ***n***-well; Mask 2: **active**; Mask 3: **polysilicon** (gate)

  Mask 4: ***p***-select (for defining the ***p***-type doping)

  Mask 5: *n*-select (for defining the ***n***-type doping)

  Mask 6: **contact** (to active & polysilicon)

  Mask 7: **metal** 1

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CMOS IC Layout

(schematic circuit to physical structures in fabrication)

- In drawing the IC layout, we need to be aware of what device structure will be fabricated from each mask layer.

  $\Rightarrow$ ***physical*** **layout design** in CMOS ICs (digital & analogue)

- In drawing the IC layout, it is a process of turning the schematic circuit into ***physical*** **design** in a planar representation (with very precise geometrical shapes & dimensions).
  - Electronic design automation (EDA) software (e.g. Cadence) is used nowadays to create the **layout design** for IC fabrication. Within Cadence, Virtuso is the IC layout editor.
  - Other examples of EDA for IC layout design: Synopsys, Tanner L-edit

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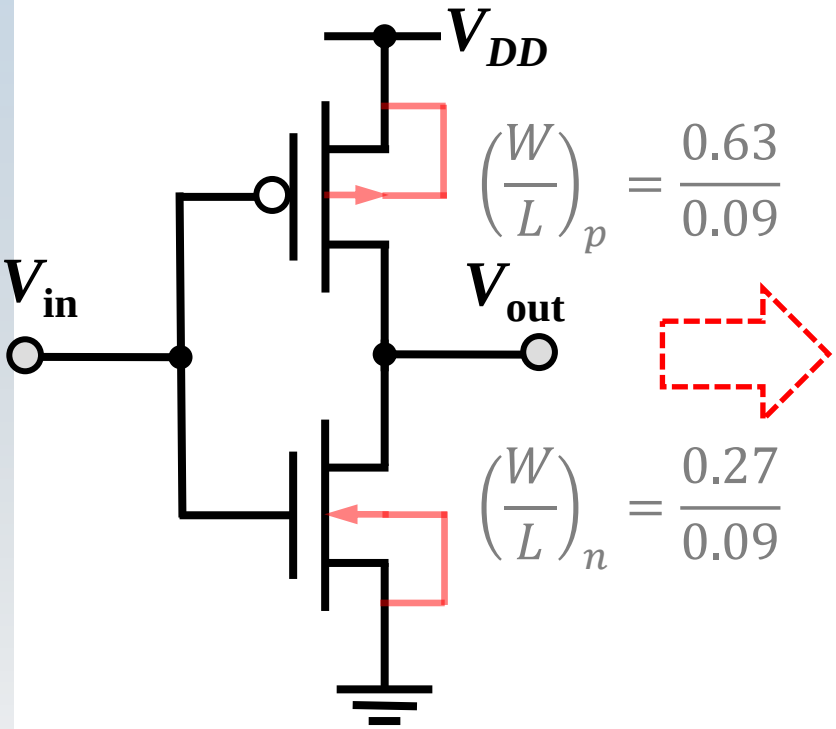
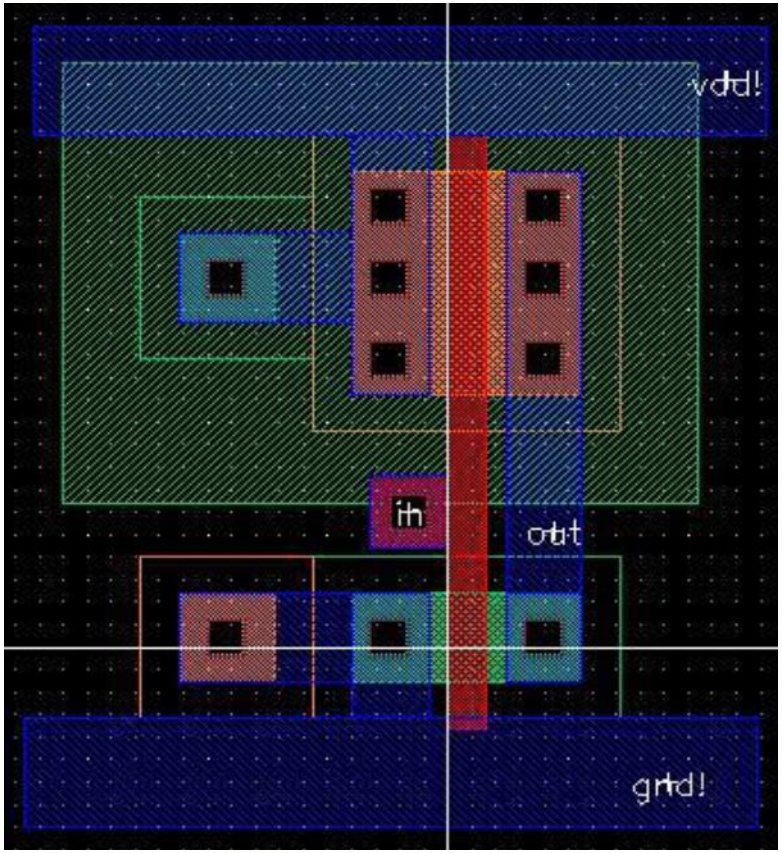
CMOS IC Layout

(schematic circuit to physical layout)





The mask number is the sequence in IC fabrication. But it doesn't matter in drawing which mask layers first & which later.

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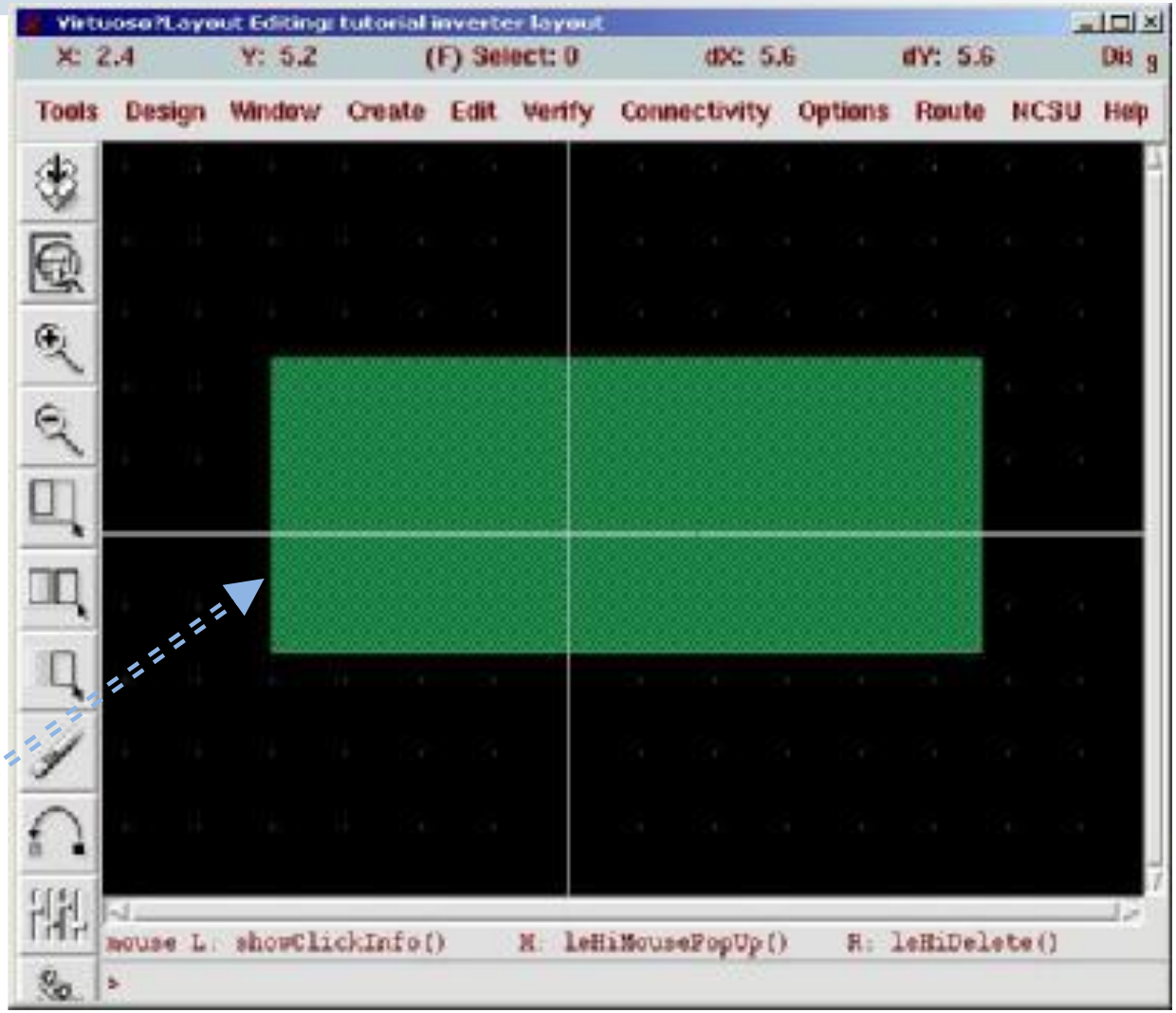
Drawing CMOS Layout with EDA

(start with the **active** mask layer for one MOSFET)

Mask 2: **active**

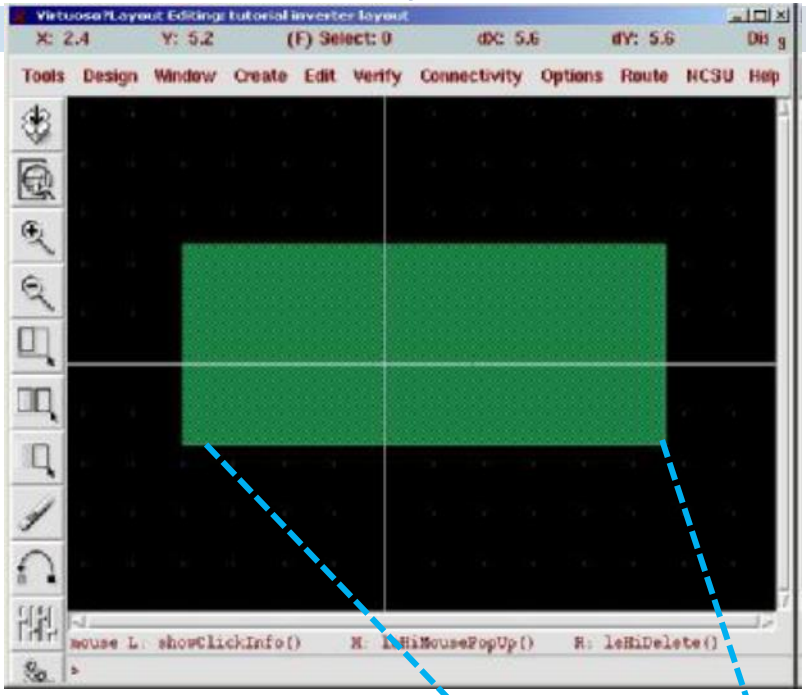
Start drawing NMOS transistor in this case.

Note that one dimension of the geometrical shape drawn for the **active** mask will define the channel width W of the MOSFET.

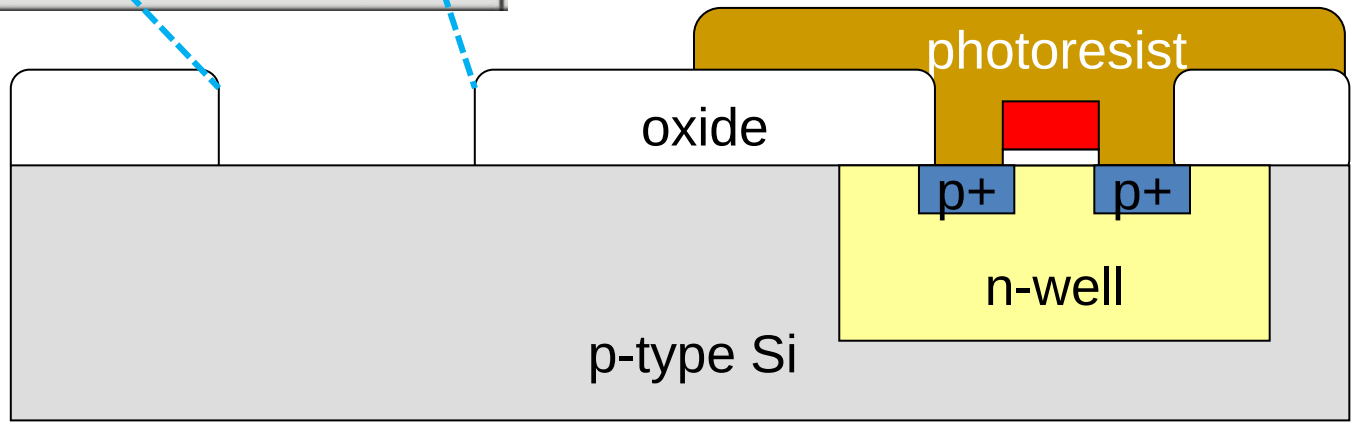


Drawing CMOS Layout with EDA

(**active** mask layer for MOS transistor)



- The **active** mask defines the regions where semiconductor **devices** (rather than e.g. inductors) will be located, hence without field oxide in the defined area.



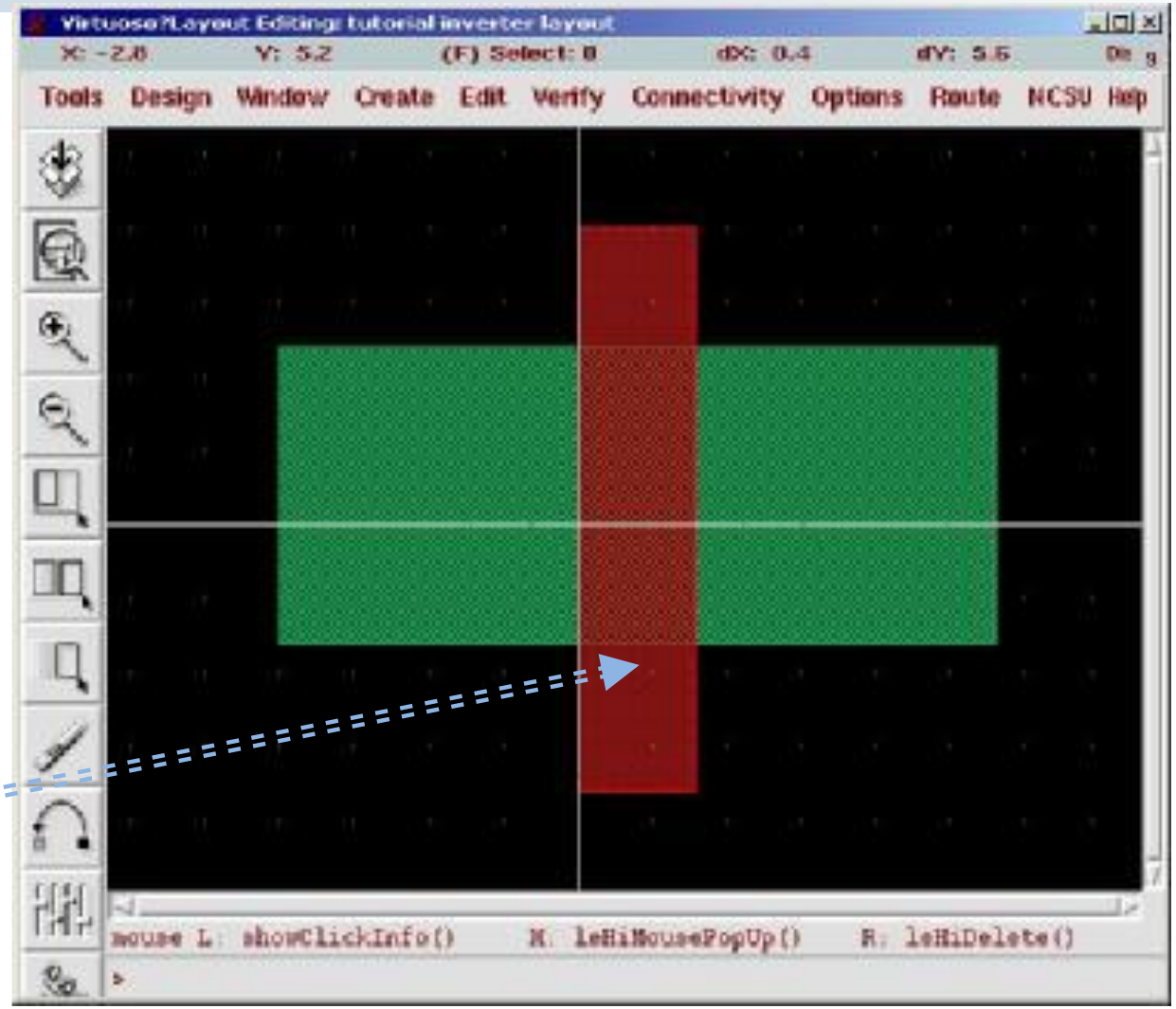
Drawing CMOS Layout with EDA

(**polysilicon** mask layer for MOS transistor)

Mask 3:

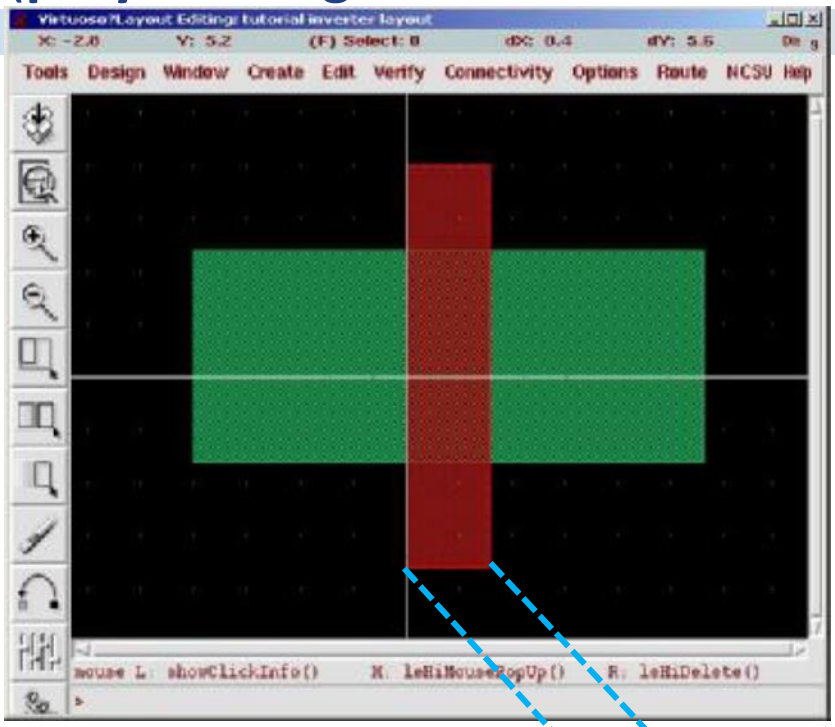
polysilicon

Note that the smaller size of the geometrical shape drawn for the **polysilicon** gate will define the channel length ***L*** of the MOSFET.

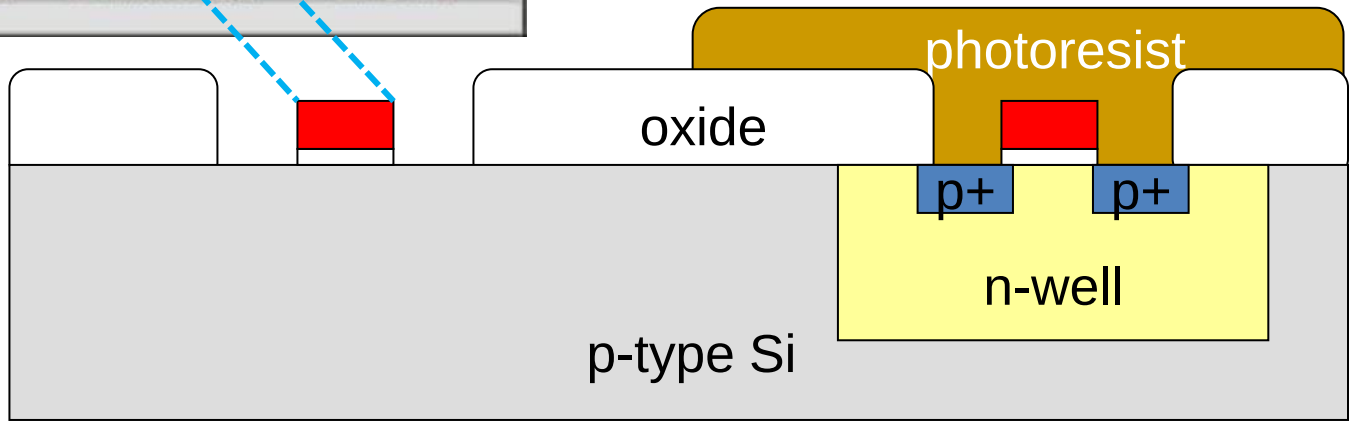


Drawing CMOS Layout with EDA

(**polysilicon** gate of the MOSFET)



- In the actual fabrication, the **polysilicon** gate is above a very thin gate oxide layer of the MOSFET.
  - In modern nano-CMOS technology, the gate is made of **copper**, not polysilicon.



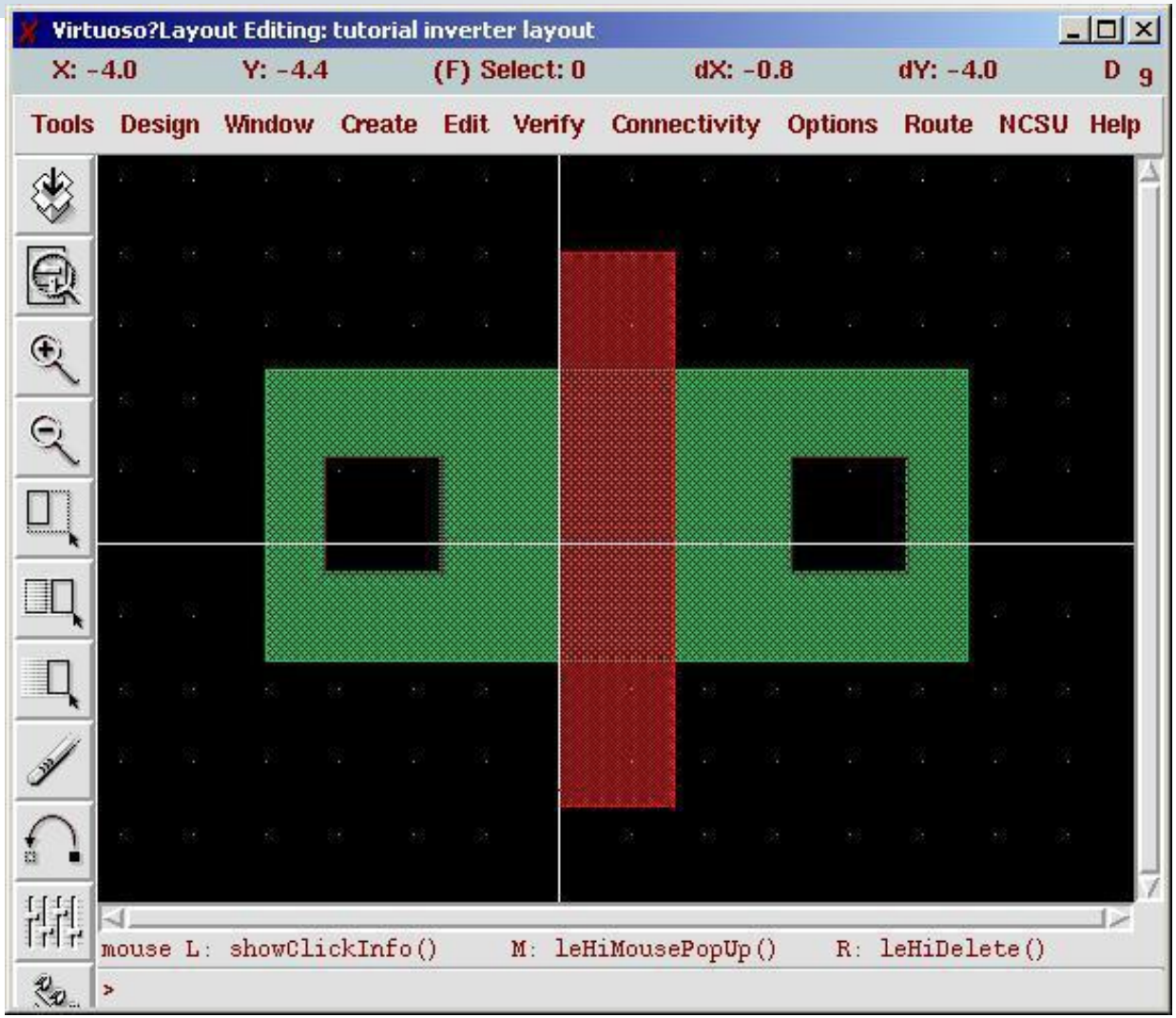
Drawing CMOS Layout with EDA

(one-sized square-shaped contact to active)

Mask 6:

contact

The **contacts** shown here connect the source/drain regions. It is the same **contact** mask layer for connecting to polysilicon.

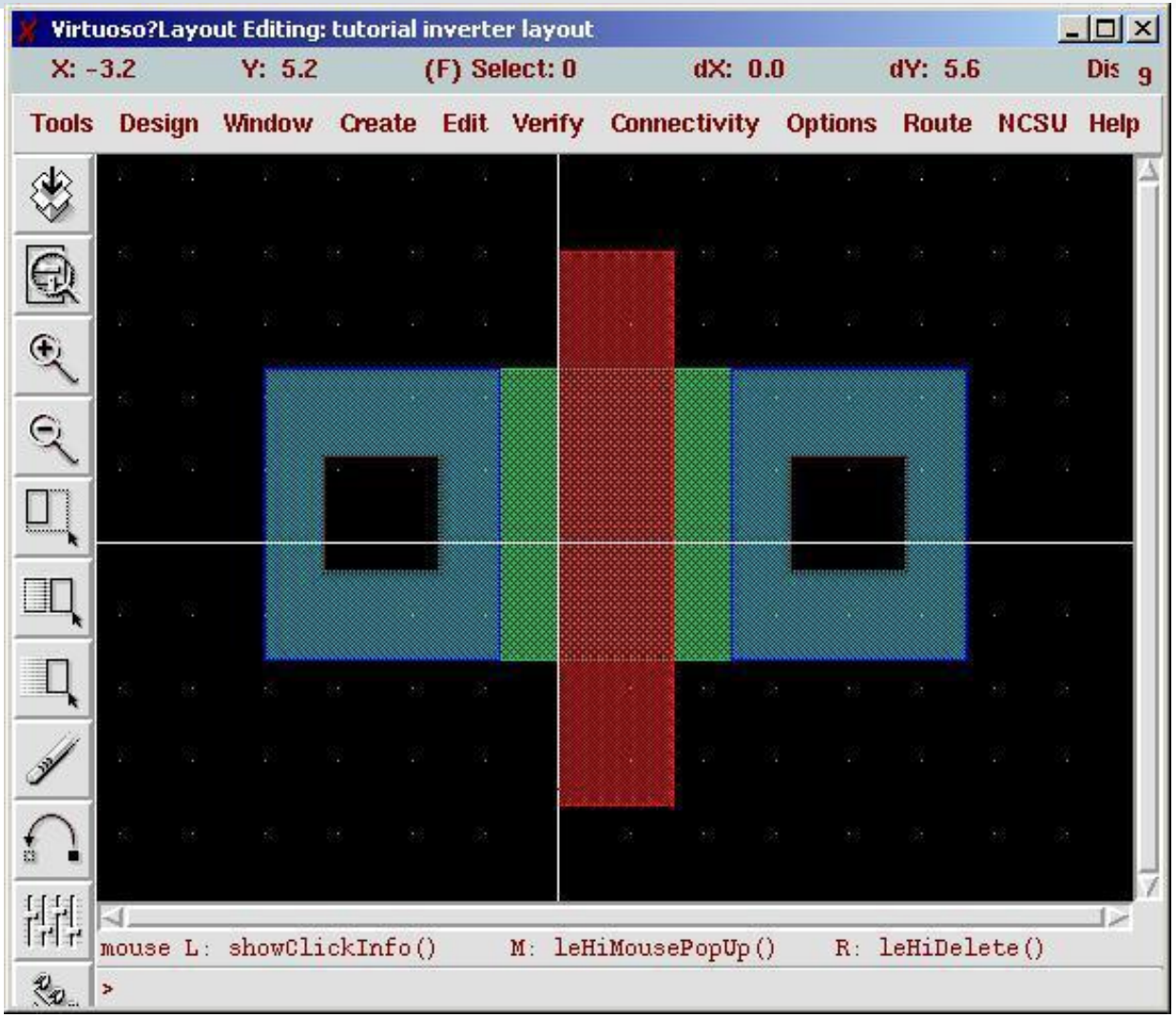


Drawing CMOS Layout with EDA

(covering **contact** with **metal**)

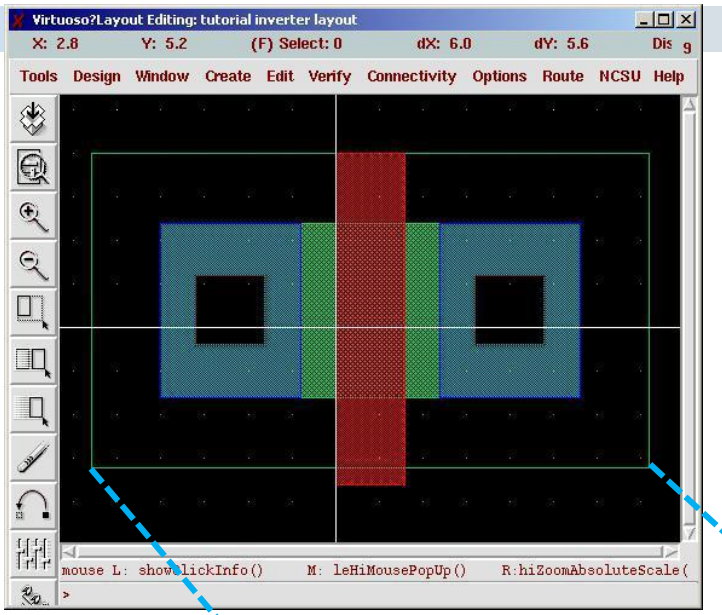
Mask 7: **metal**

The **contacts** must be covered with the **metal** mask layer, literally **metal 1**.

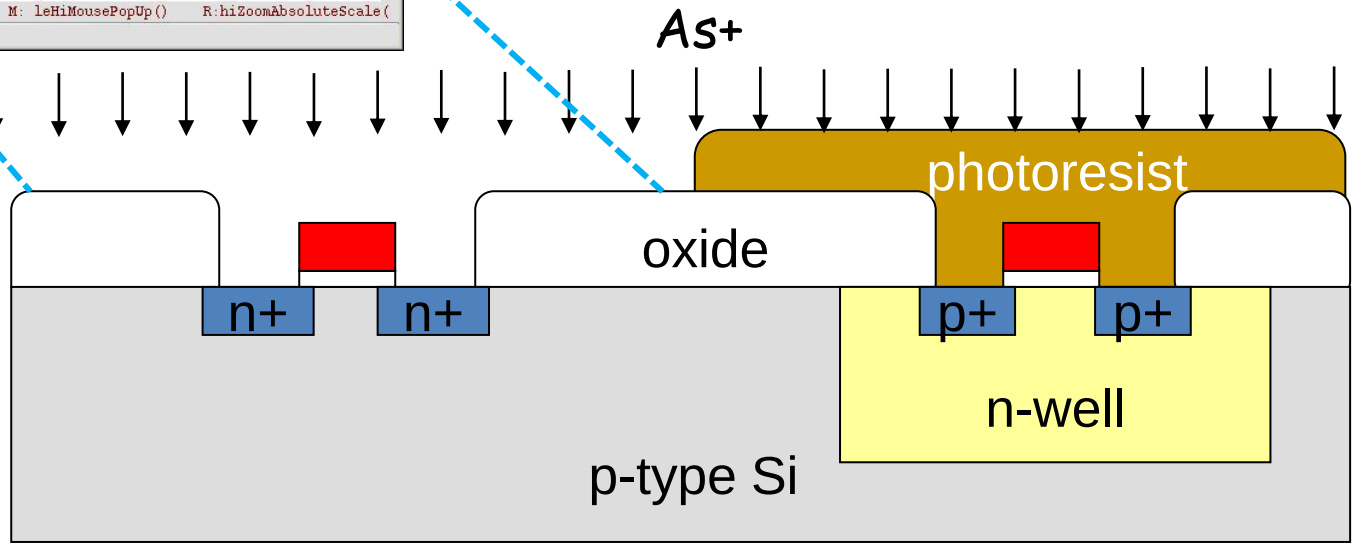


Drawing CMOS Layout with EDA

(***n***-select or called ***n***-diffusion implant)



- In the fabrication of both NMOS and PMOS transistors on the same wafer, the NMOS source/drain regions are selected for ***n***-type doping by the ***n***-select mask layer.

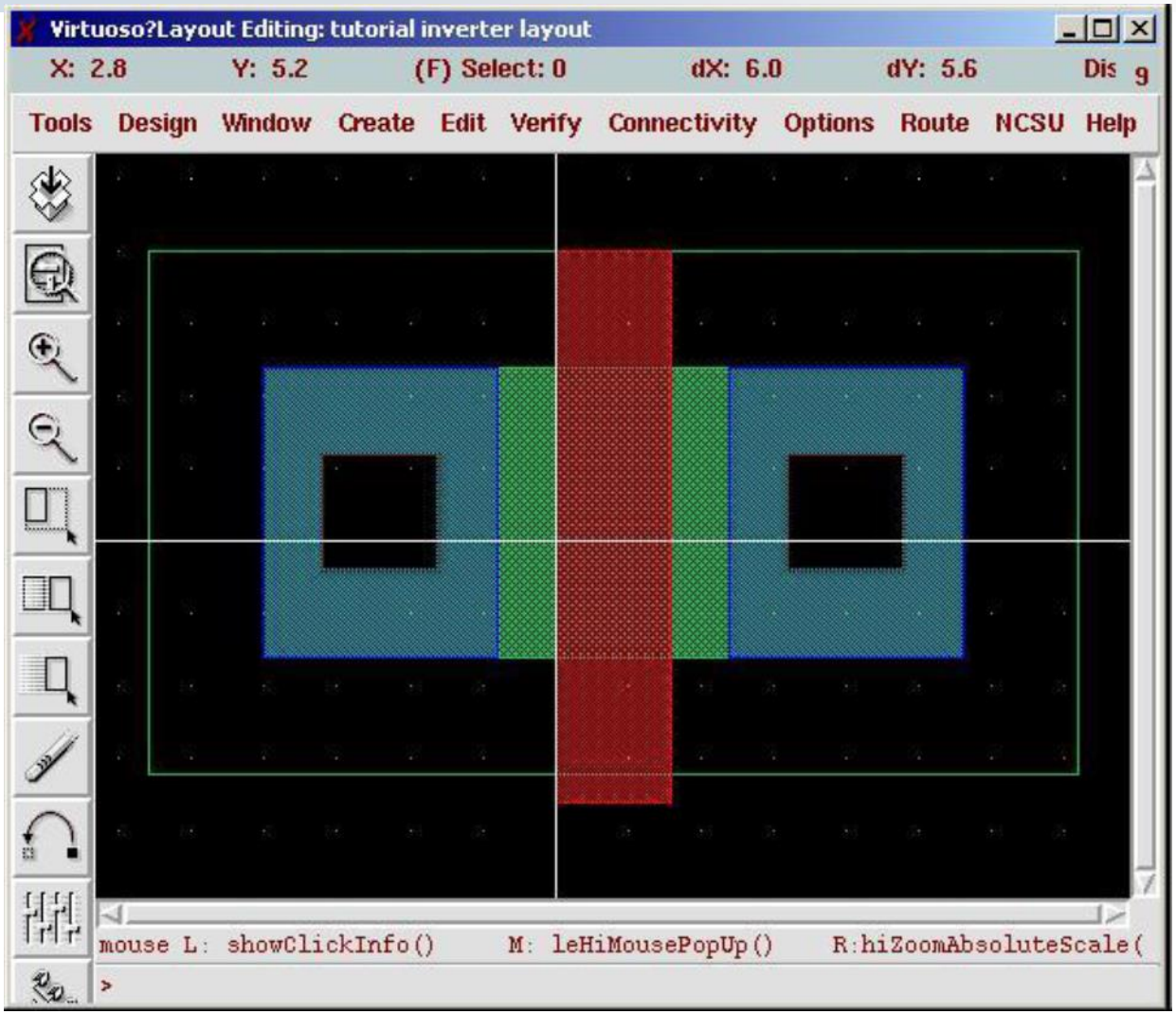


Drawing CMOS Layout with EDA

(***n***-select for regions to be doped ***n***-type)

Mask 5: ***n*-select**

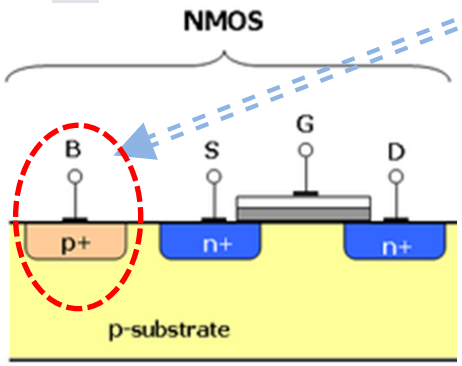
The ***n*-select** mask layer covers the **active** mask layer & the **polysilicon** mask layer in the NMOS transistor. ⇒ The polysilicon gate is heavily doped ⇒ more conducting

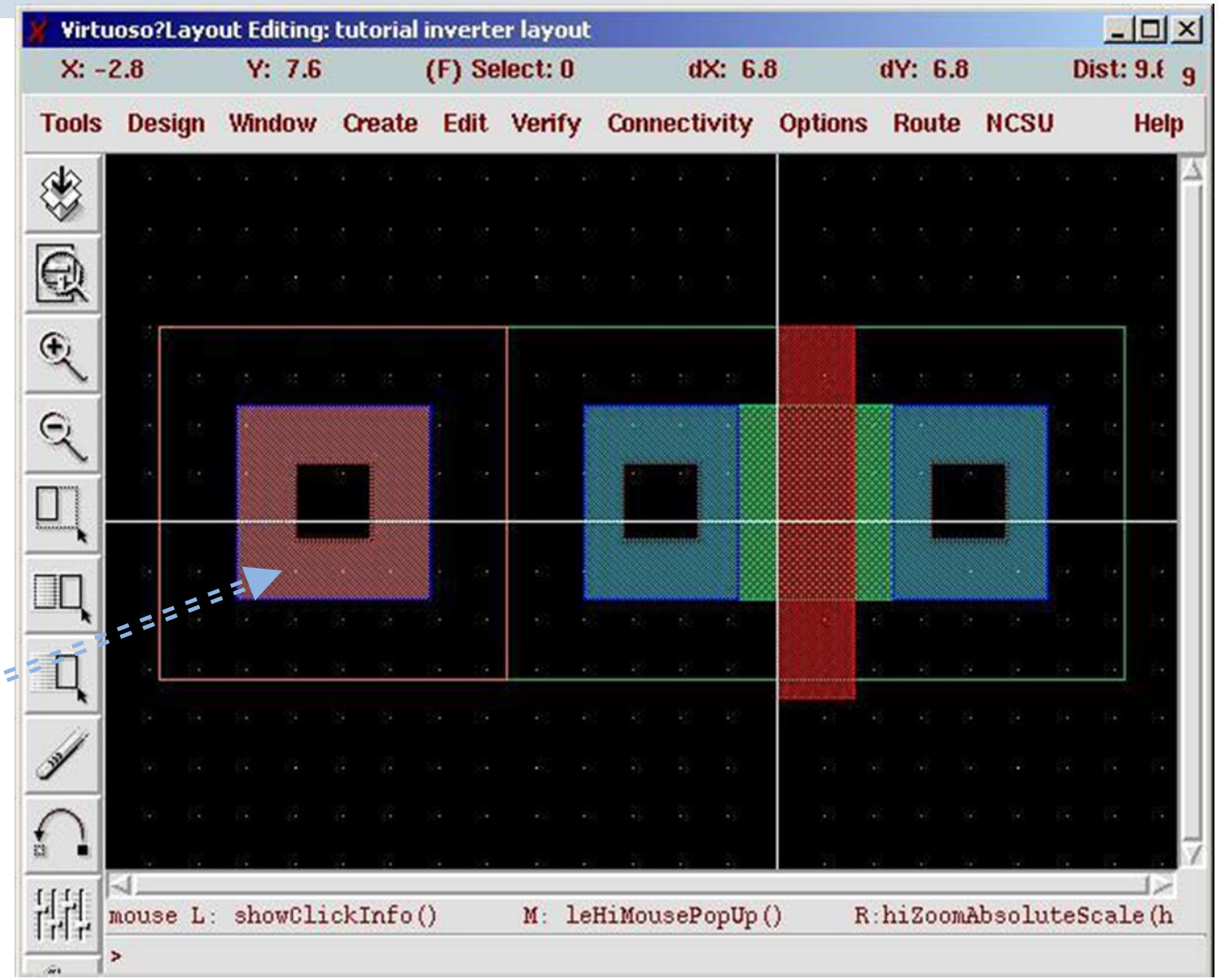


Drawing CMOS Layout with EDA

(substrate contact in NMOS transistor)

The substrate contact to the ***p***-type wafer can be explicitly created in ***n***MOSFET.



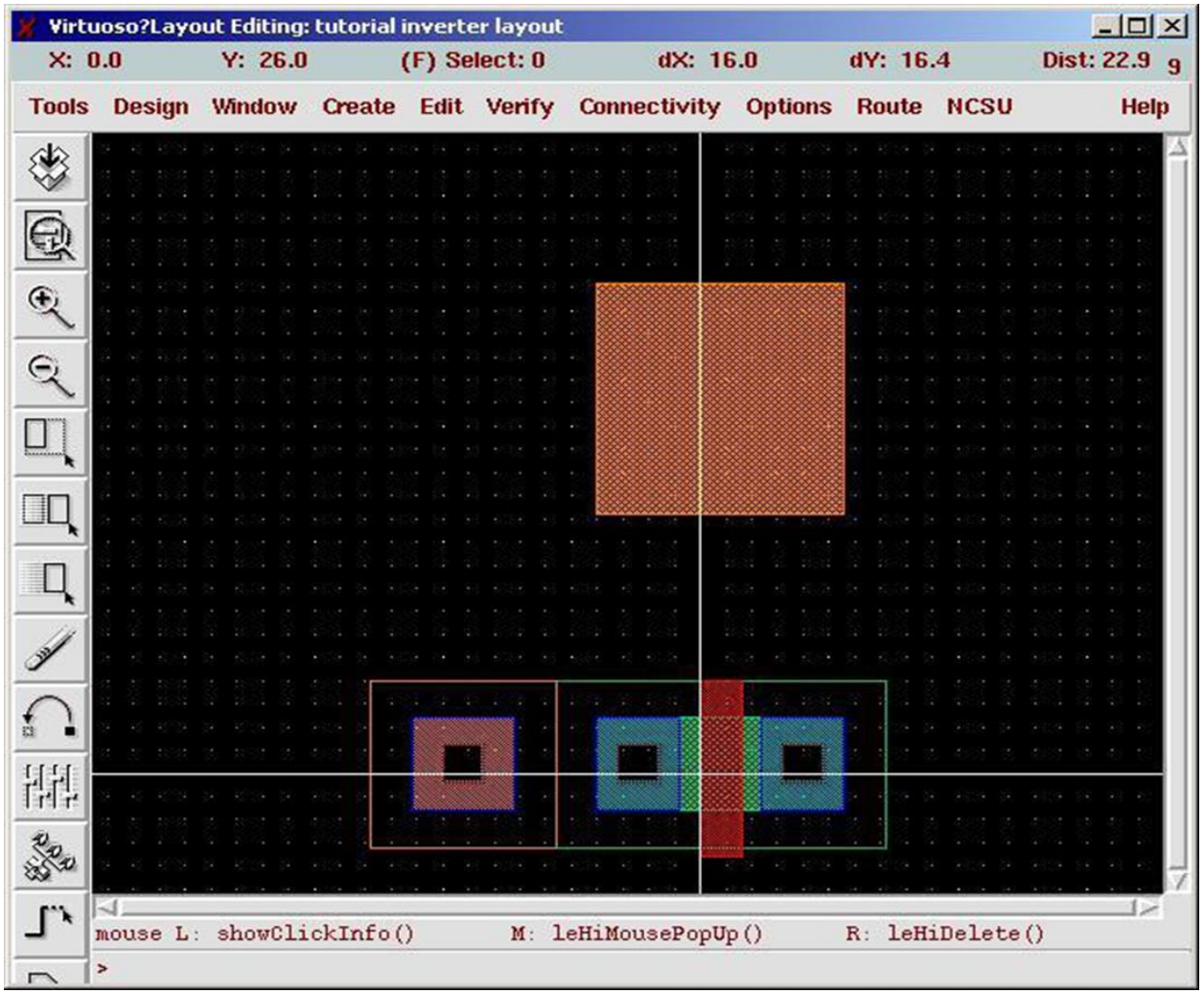


Drawing CMOS Layout with EDA

(same **active** mask layer for PMOS transistor)

Mask 2:
active

The PMOS transistor layout also starts with the **active** mask layer, which is essentially the same as that of the NMOS transistor.



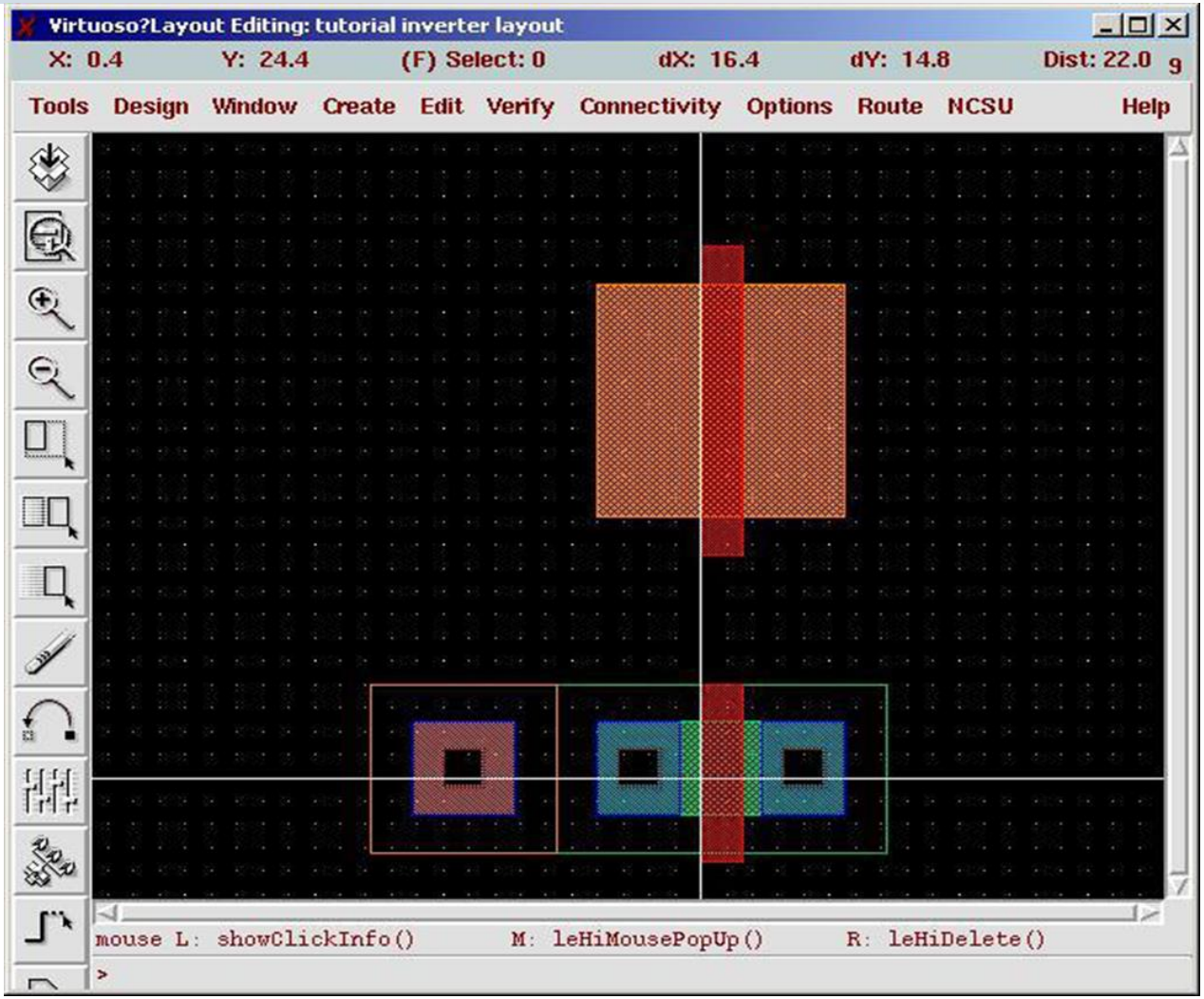
Drawing CMOS Layout with EDA

(same **polysilicon** mask layer for PMOS transistor)

Mask 3:

polysilicon

The PMOS transistor's gate electrode is defined by the same **polysilicon** mask layer of the NMOS transistor, in the same way.



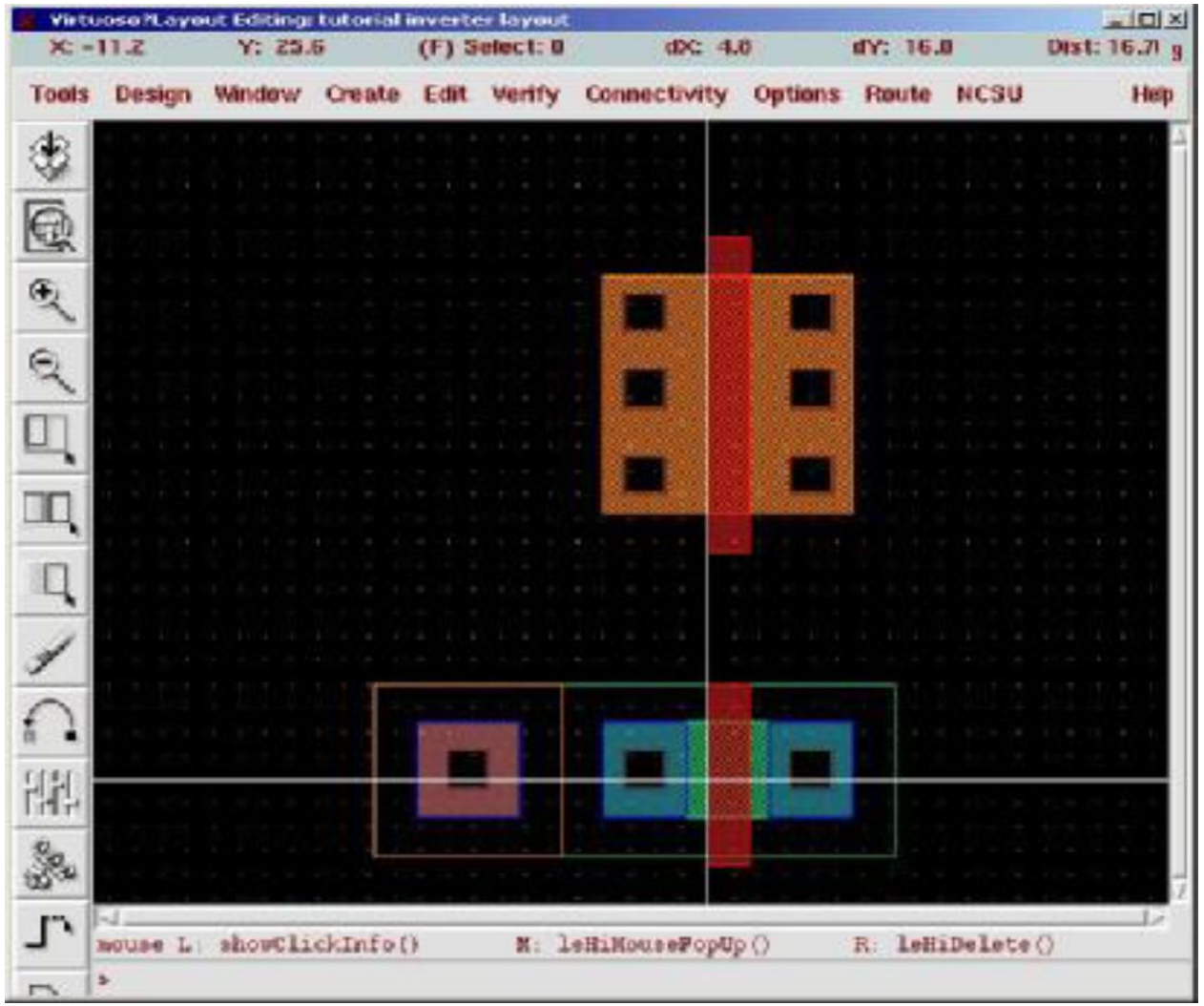
Drawing CMOS Layout with EDA

(**contact** to source/drain regions of PMOS transistor)

Mask 6:

contact

The same **contact** mask layer in the NMOS transistor applies to the PMOS transistor.

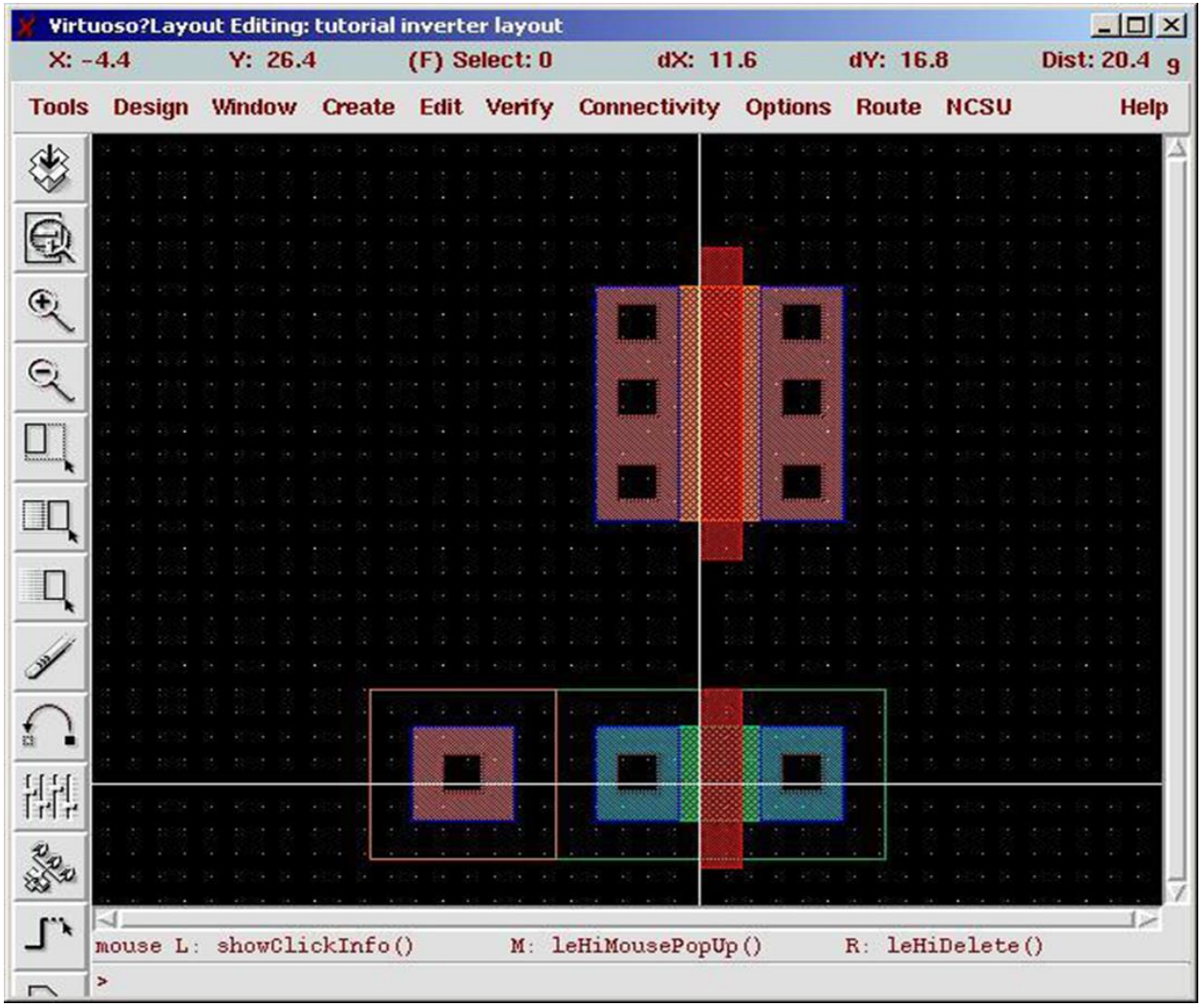


Drawing CMOS Layout with EDA

(same square **contact** covered with **metal**)

Mask 7:
metal

The same one-sized square **contacts** of the PMOS transistor must also be covered with the **metal** 1 mask layer.

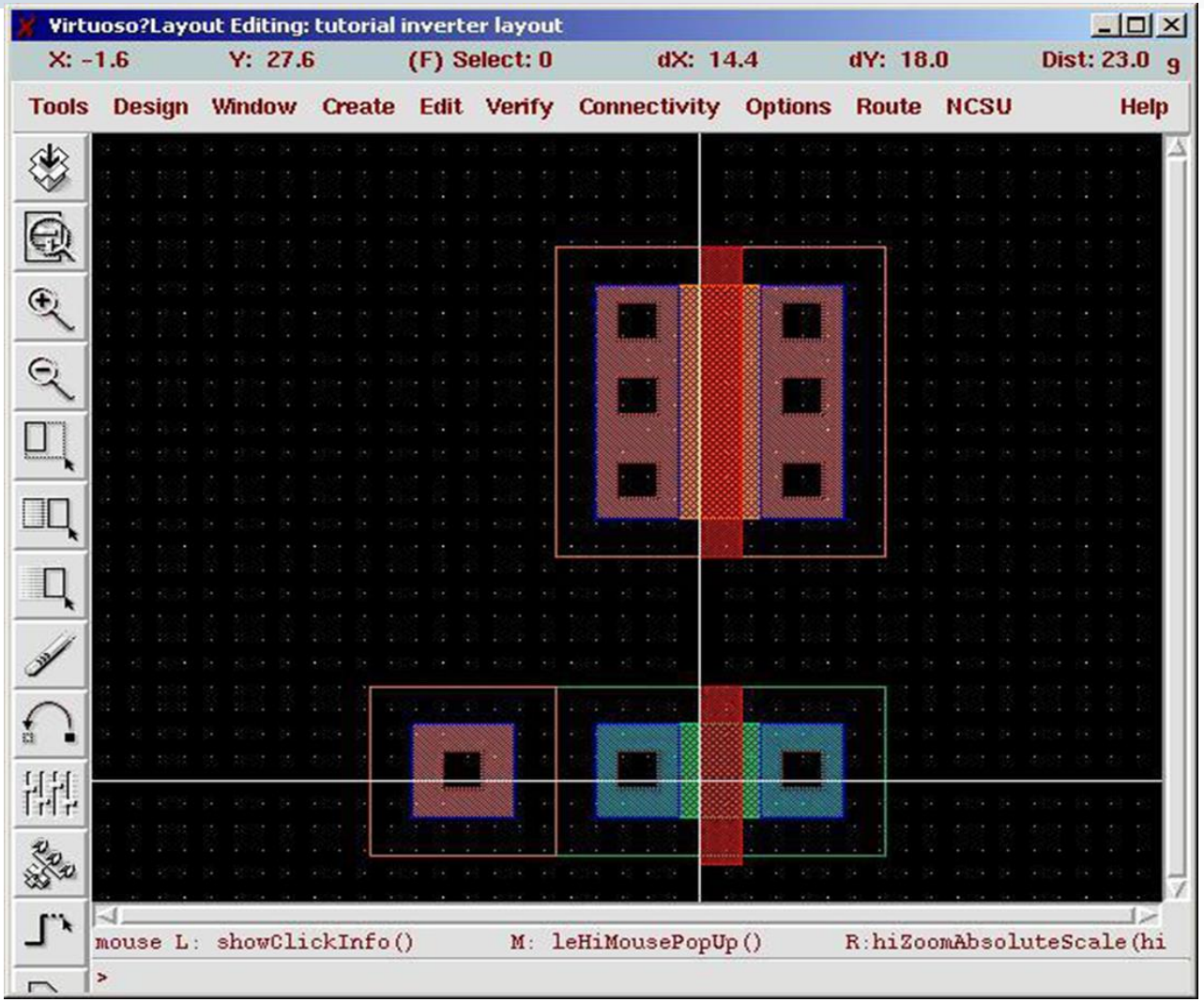


Drawing CMOS Layout with EDA

(***p*-select** for defining regions of ***p***-type doping)

Mask 6: ***p*-select**

In the PMOS transistor, the ***p*-select** mask layer defines the source/drain regions for ***p***-type doping.



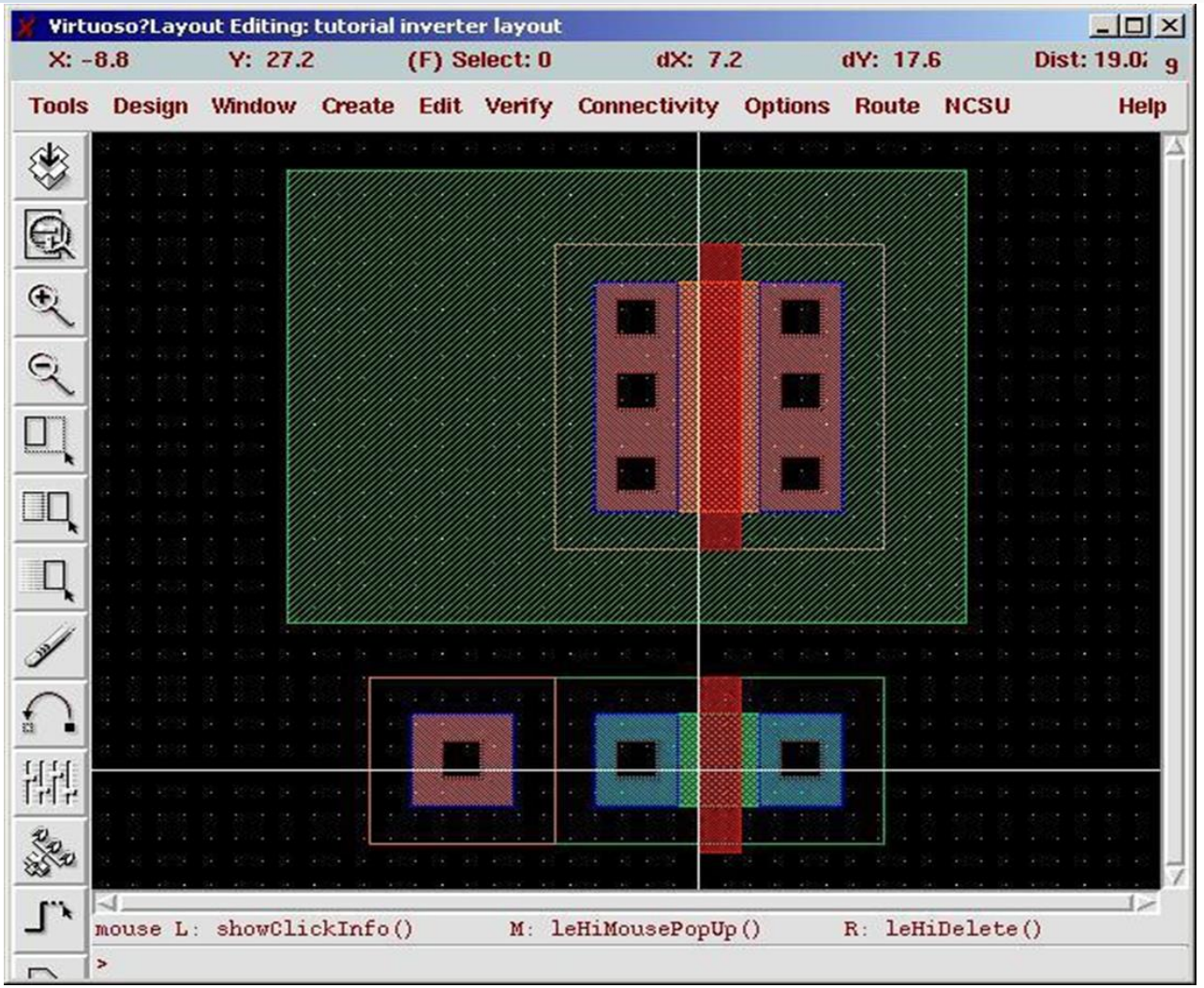
Drawing CMOS Layout with EDA

(***n*-well** mask layer for PMOS transistor)

Mask 1:

***n*-well**

To make PMOS transistors on a ***p***-type wafer, the ***n*-well** mask layer defines an ***n***-type region for the pMOSFET.

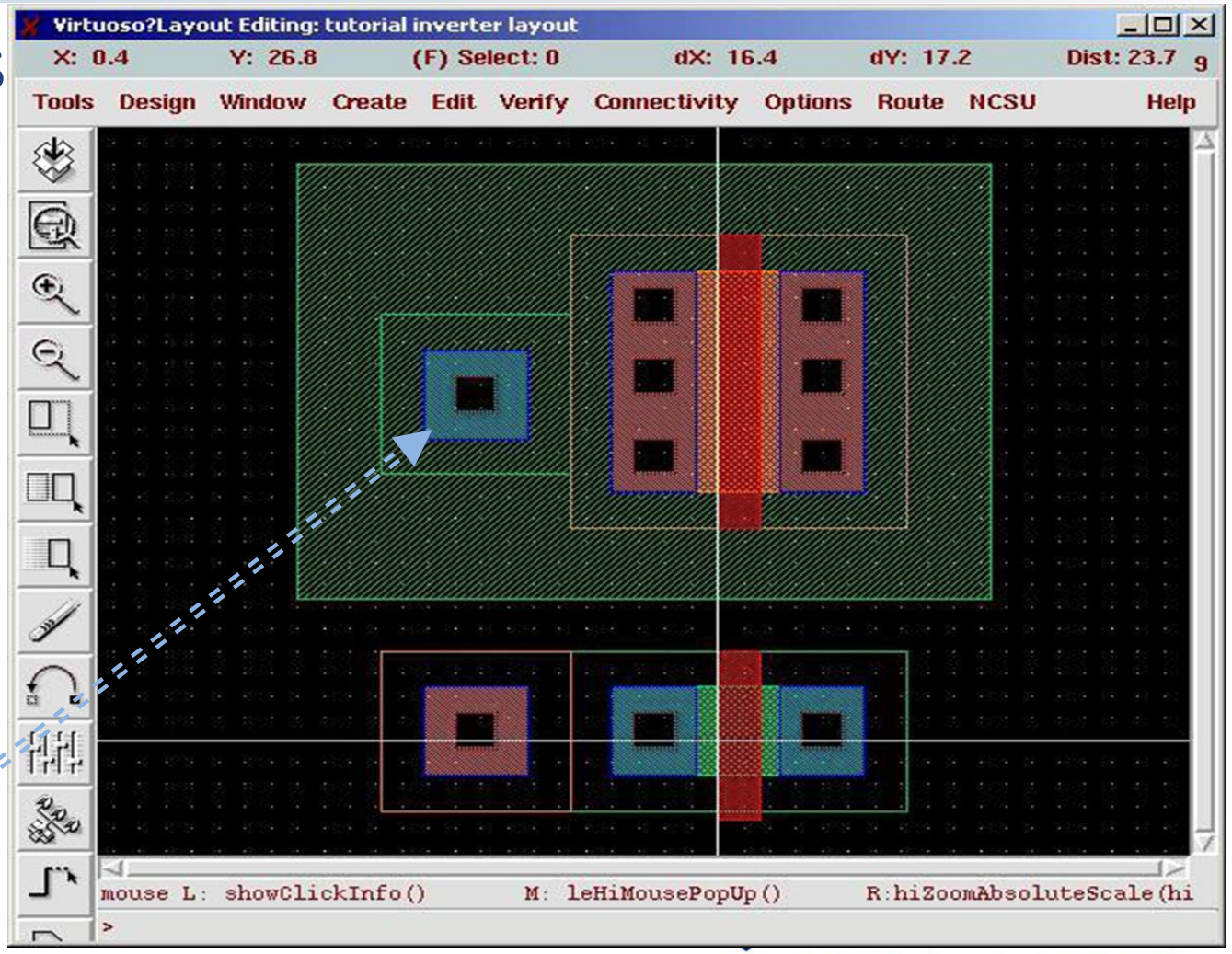


Drawing CMOS Layout with EDA

(**substrate contact** of PMOS transistor)

In the PMOS transistor, the **substrate contact** to the ***n*-well** is necessary.

Note 4 mask layers on ***n*-well**: **active**, **contact**, ***n*-select** & **metal**.

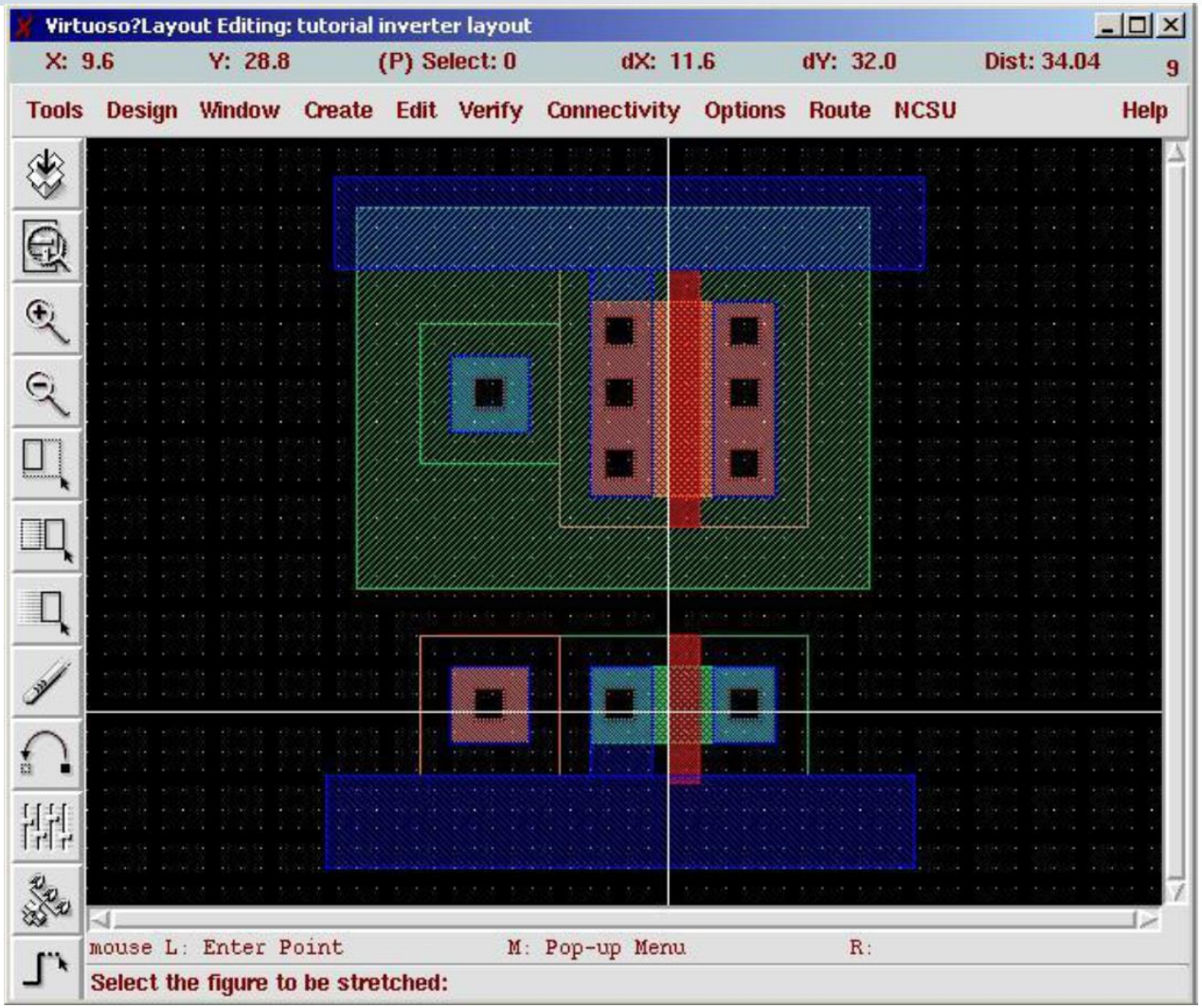


Drawing CMOS Layout with EDA

(use of **metal** mask layer for electrical wiring)

The **metal** mask layer is used to define the ***interconnect*** as **electrical wiring** of the circuit (e.g. connection to power supply & ground).

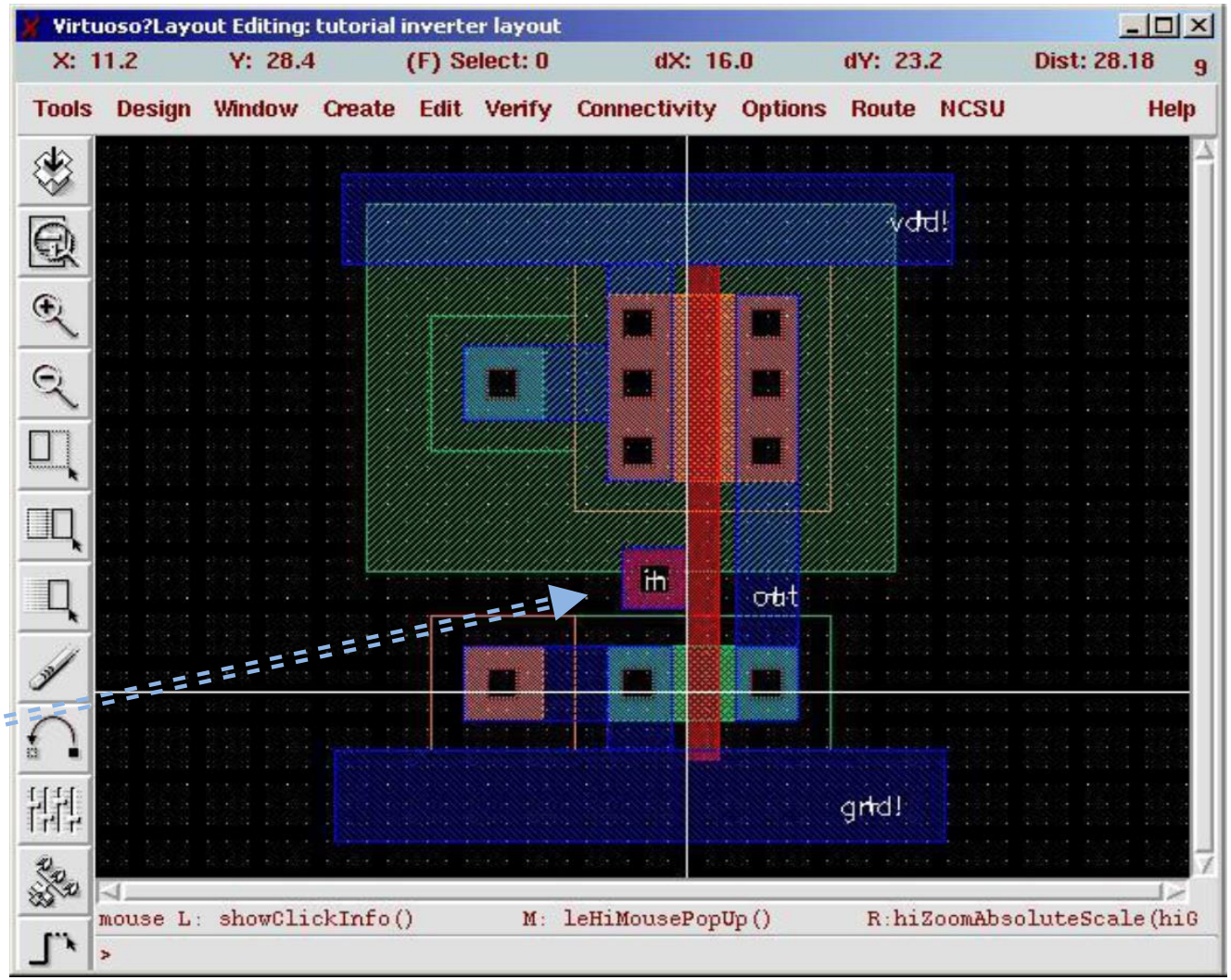
There can be metal 2, 3, …



Drawing CMOS Layout with EDA

(polysilicon gates connection)

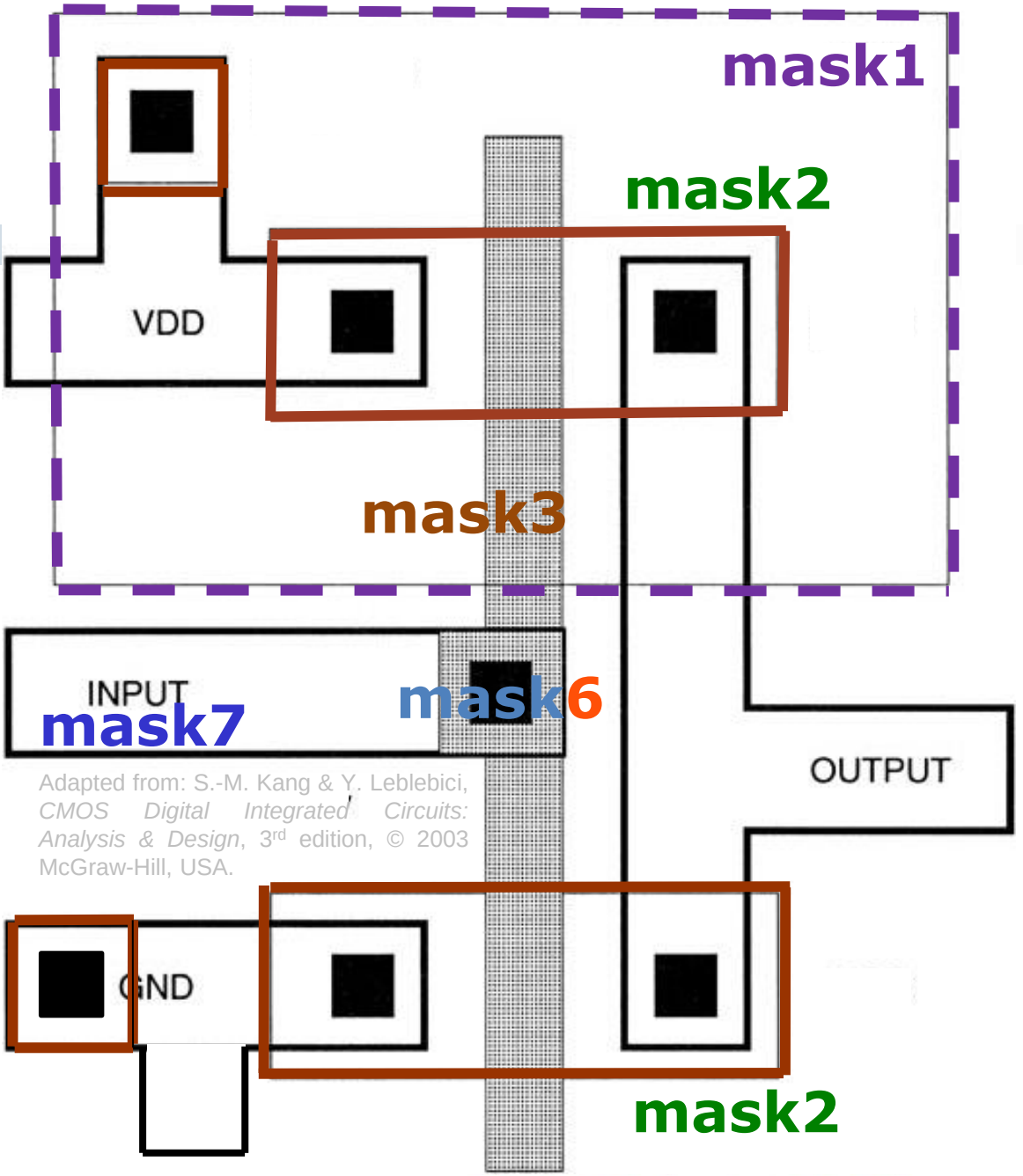
The **polysilicon** gates of the PMOS & NMOS transistors are connected together with a **contact** & **metal** to the input of the CMOS inverter.



IC Layout

(CMOS logic gate)

- When given a simple CMOS digital IC layout, can you recognise the **logic circuit**?
- Can you also identify the **mask layers** in the layout?
  - What mask layers missing?



Adapted from: S.-M. Kang & Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis & Design*, 3rd edition, © 2003 McGraw-Hill, USA.

IC Layout

(≥7 masks in CMOS)

Mask 1: ***n***-well

Mask 2: **active**

Mask 3: **polysilicon**

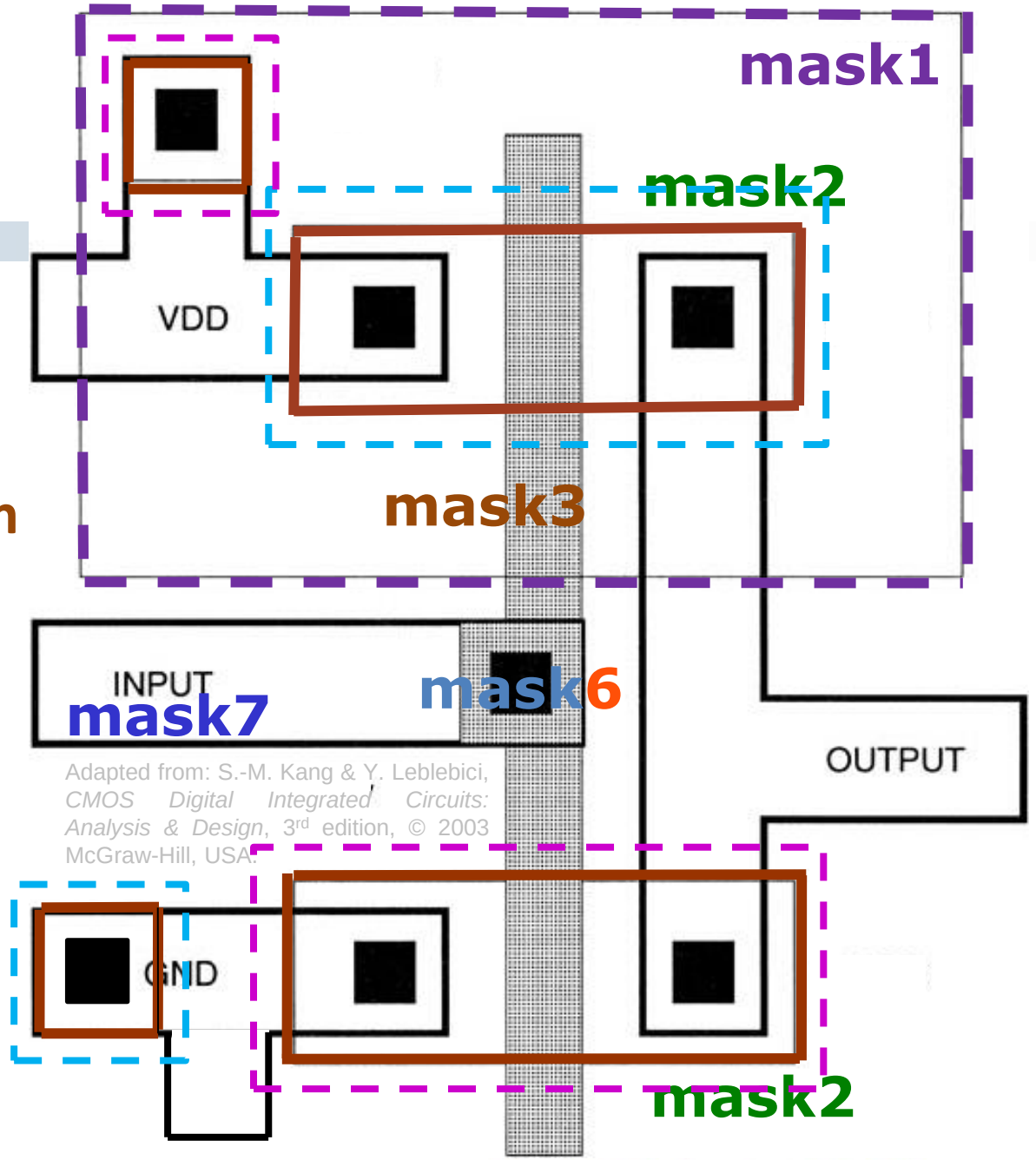
Mask 6: **contact**

Mask 7: **metal** 1

Two mask layers are missing on the previous slide:

Mask 4: ***p***-select

Mask 5: *n*-select



Adapted from: S.-M. Kang & Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis & Design*, 3rd edition, © 2003 McGraw-Hill, USA.