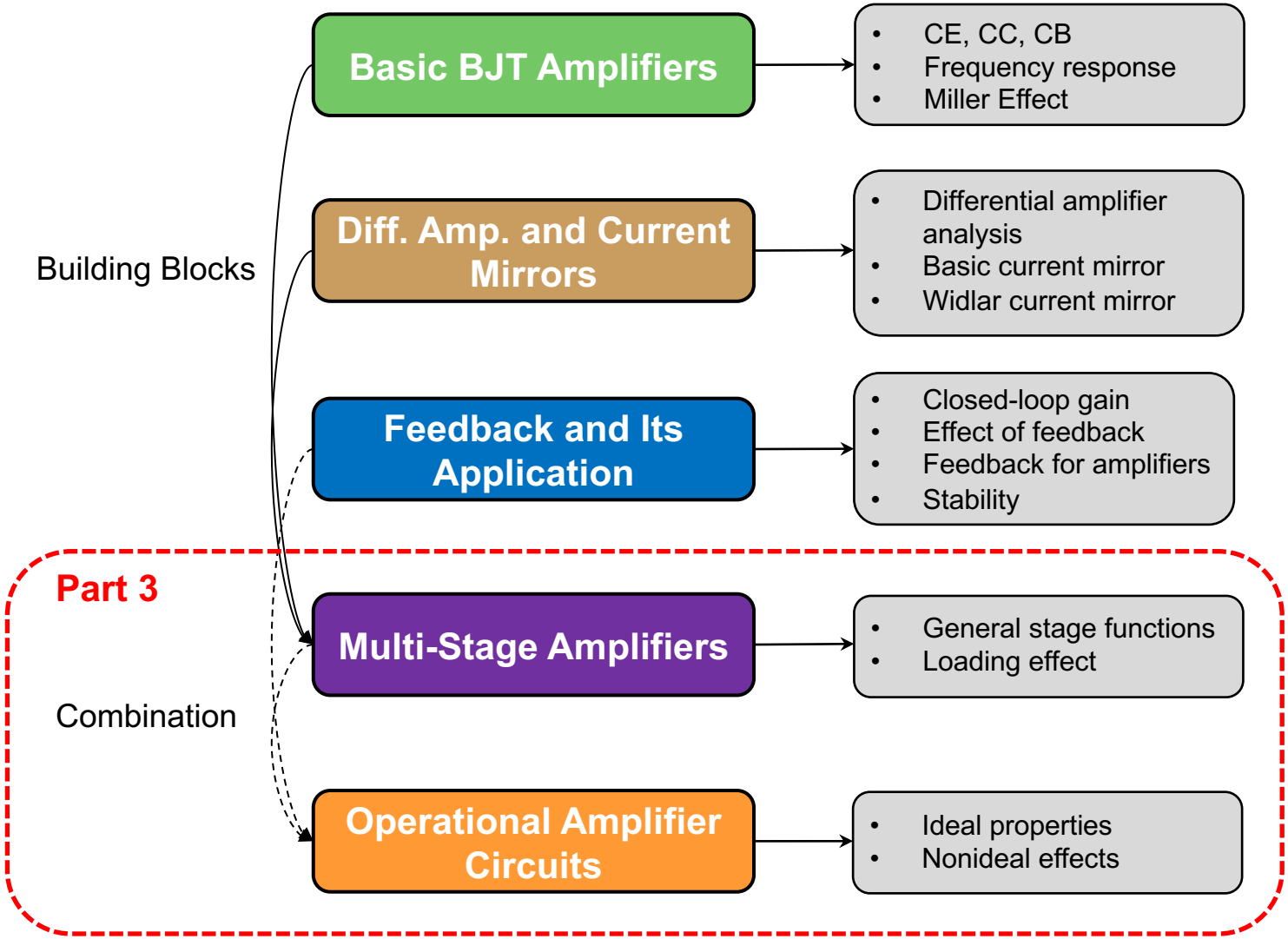
Revision – Part 3

Dr. Xiaoyang Chen

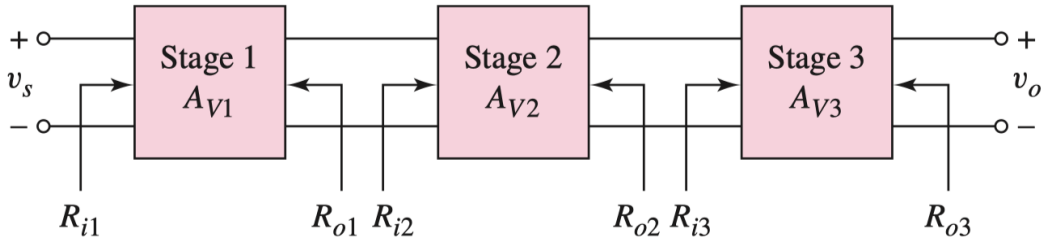
Dept. of Electrical & Electronic Engineering
XJTLU

A General Picture



Multi-Stage Amplifiers for Integrated Circuits

Main Principles



1. Perform the DC analysis of the circuit to determine the small-signal parameters of the transistors. In most cases the base currents can be neglected. This assumption will normally provide sufficient accuracy for a hand analysis.

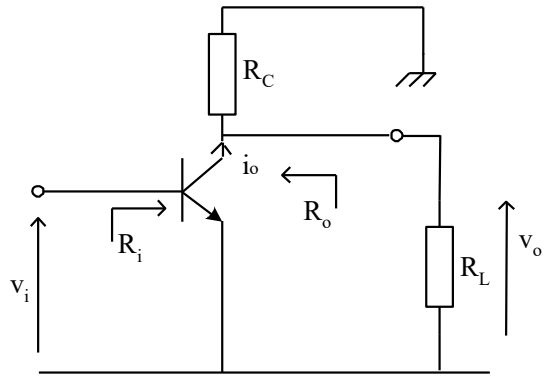
2. Perform the AC analysis on each stage of the circuit, taking into account the loading effect of the following stage.

   The properties of the previous stage (e.g., output resistance) can be a function of the input resistance (load) of the next stage, and vice versa.

3. The overall small-signal voltage gain is the product of the gains of each stage as long as the loading effect is taken into account.

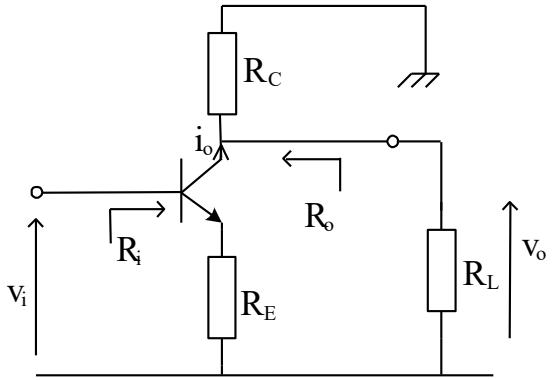
The Properties of Basic Amplifiers (Formula Sheet)

- **Common Emitter**



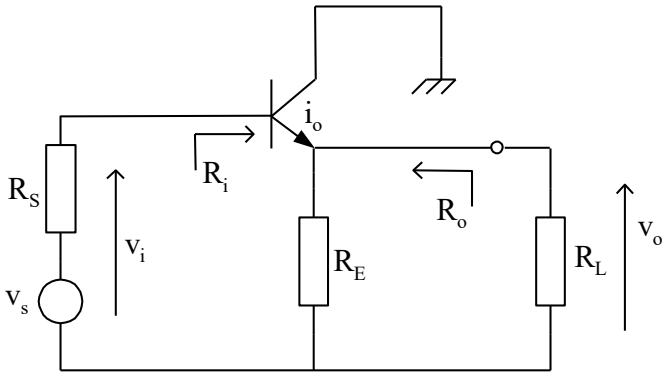
$$R_i = r_\pi$$
$$R_o = R_C||r_o \approx R_C$$
$$A_v = \frac{v_o}{v_i} = -g_m R_C||R_L$$

- **Common Emitter with Emitter Degradation**



$$R_i = r_\pi + (1+\beta)R_E$$
$$R_o = R_C||r_o \approx R_C$$
$$A_v = -\frac{g_m R_C||R_L}{1+g_m R_E}$$

- **Common Collector (Emitter Follower)**



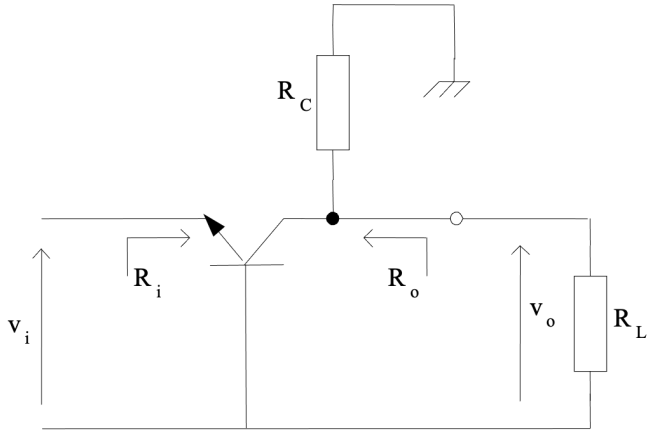
Why is CC a good buffer?

$$R_i = r_\pi + (1+\beta)R_E||R_L$$

$$R_o = \frac{r_\pi + R_S}{1+\beta}||R_E$$

$$A_v = \frac{g_m R_E||R_L}{1 + g_m R_E||R_L}$$

- **Common Base**



$$R_i = \frac{r_\pi}{1+\beta} \approx \frac{1}{g_m} = r_e$$

$$R_o = R_C$$

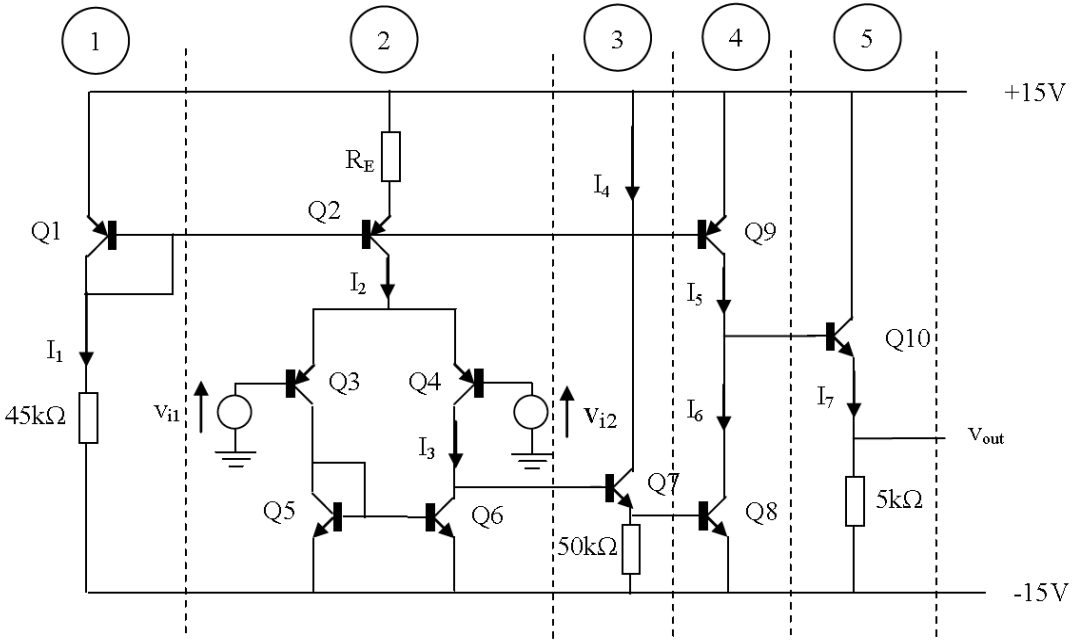
$$A_v = g_m R_C||R_L$$

Example

Consider the multi-stage voltage amplifier shown below (labelled by 5 stages):

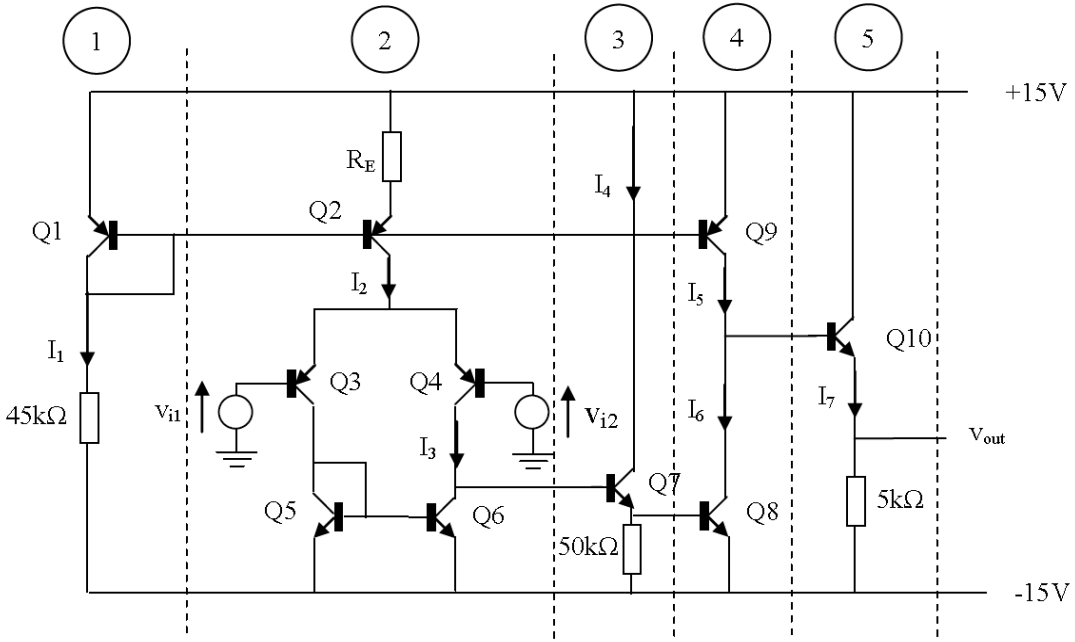
a) Briefly describe the function of each of the 5 stages

b) If $I_2 = 0.1$ mA, make reasonable approximations to estimate the total current drawn by the circuit from the ± 15 V DC voltage supply when the amplifier is biased so that the DC value of $V_{out} = 0$ V and the ac input signals are zero ($V_{BE}(on) = 0.6$ V).



c) Assuming $I_2 = 0.1$ mA, make reasonable approximations to estimate the overall small signal voltage gain of the circuit. Assume all transistors have a current gain $\beta = 100$ and Early voltage -100 V.

Solution a):



Stage 1 is the bias current section, which forms a Widlar current mirror with Q2 and a basic current mirror with Q9

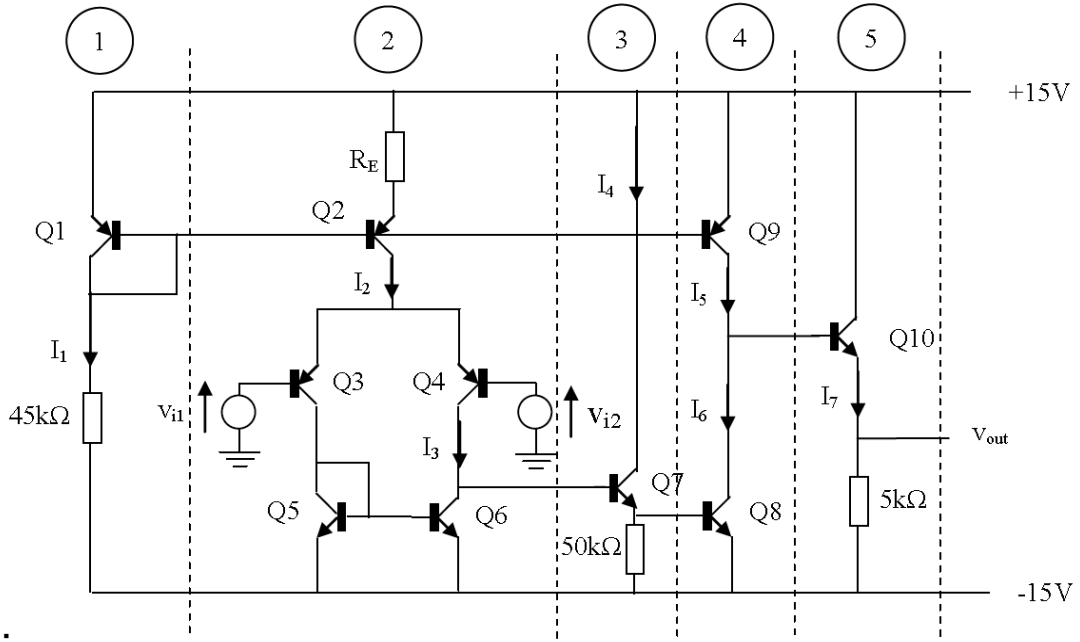
Stage 2 is a differential amplifier with active load. It forms the input of the circuit and provides the first voltage gain

Stage 3 is an emitter-follower (CC) circuit forming an impedance matching buffer between stages 2 and 4. It also reduces the loading effect.

Stage 4 is a CE amplifier with current mirror as active load that significantly contributes to the overall voltage gain.

Stage 5 is a CC circuit forming the output stage and reducing loading effect.

Solution b):



At stage 1, we have:

$$I_1 = \frac{V^+ - 0.6 - V^-}{45} = 0.653\ mA$$

From the current mirror, we have:

$$I_5 = I_1 = 0.653\ mA$$

$$I_4 = \frac{0.6}{50} = 0.012\ mA$$

Since we have $V_{out} = 0\ V$, we have:

$$I_7 = \frac{0 - (-15)}{5} = 3\ mA$$

Therefore, the total current drawn from the source is:

$$I_{total} = I_1 + I_2 + I_4 + I_5 + I_7 = 4.42\ mA$$

Solution c):

Stage 1:

Stage 1 is a bias reference, and will not contribute to the overall voltage gain

Stage 2:

For a differential amplifier with active loads, we have:

$$A_{v2} = g_{m4}(r_{o4}||r_{o6}||R_{L2})$$

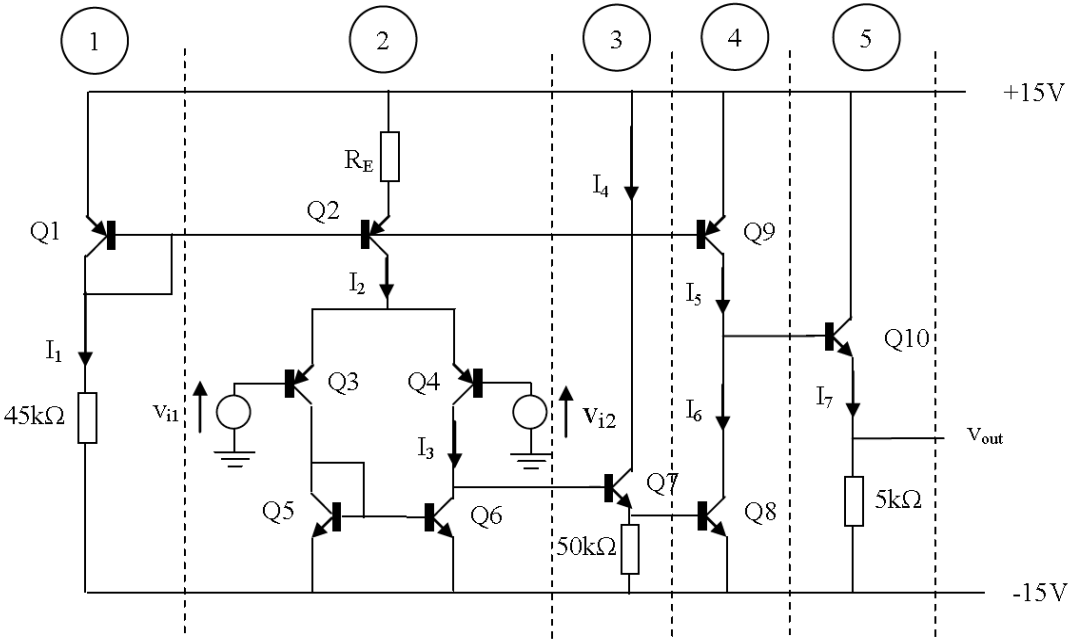
where

$$R_{L2} = R_{i3} = r_{\pi 7} + (1+\beta)50||R_{L3}$$

and $R_{L3} = R_{i4} = r_{\pi 8}$

Then we have:

$$g_{m4} = \frac{I_{CQ4}}{V_T} = \frac{I_2}{2V_T} = 2\ mA/V$$



$$r_{o4} = r_{o6} = \frac{100}{0.5I_2} = 2000\ k\Omega$$

$$r_{\pi 7} = \frac{\beta}{g_{m7}} = \frac{\beta}{40I_4} = 208\ k\Omega$$

At the base of Q10, we have:

$$I_6 = I_5 - \frac{I_7}{\beta} = 0.623\ mA$$

Therefore:

$$R_{L3} = r_{\pi 8} = \frac{\beta}{40I_6} \approx 4\ k\Omega$$

$$R_{L2} \approx 582\ k\Omega$$

and

$$\underline{A_{V2} \approx 736}$$

Solution c):

Stage 3:

Stage 3 is a CC circuit with $\underline{A_{V3} = 1}$

Stage 4:

For a CE amplifier, we have:

$A_{V4} = -g_{m8}(R_{L4}||r_{o8}||r_{o9})$

(Here $R_C = r_{o9}$)

where $R_{L4} = R_{i5}$

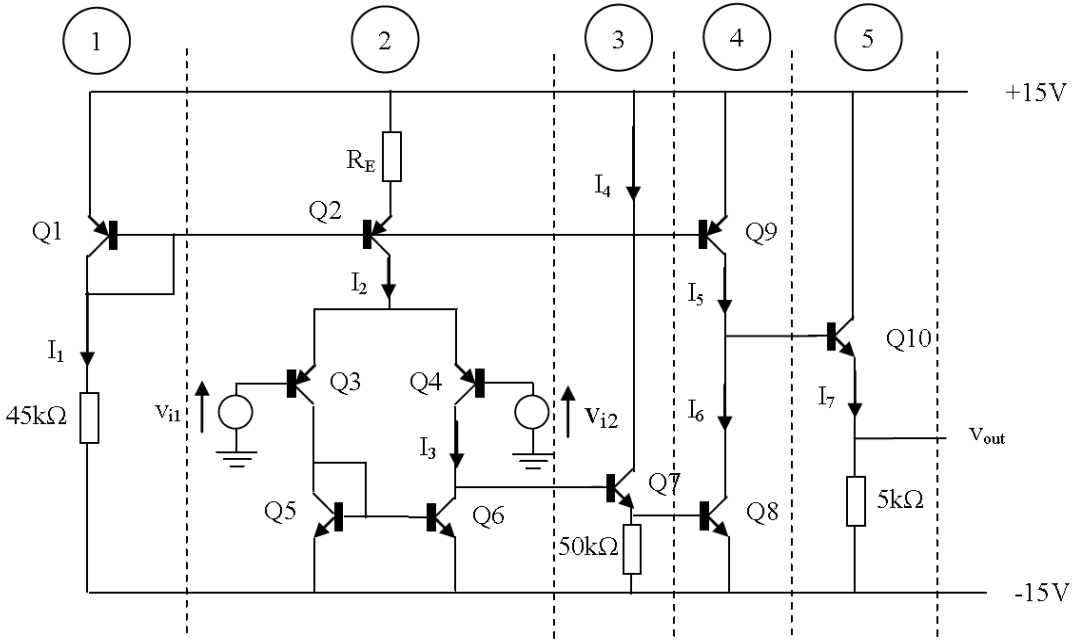
and $R_{i5} = r_{\pi 10} + (1+\beta)\cdot 5$ with $r_{\pi 10} = \dfrac{\beta}{40I_7} = 0.83\ k\Omega$

Hence $R_{i5} \approx 505\ k\Omega$

We have $r_{o8} \approx r_{o9} = \dfrac{100}{I_5} = 153\ k\Omega$

and $g_{m8} = 40I_6 = 25\ mA/V$

Then $\underline{A_{v4} = -25\times 153\ \|\ 153\ \|\ 505 \approx -1660}$



Stage 5:

Stage 5 is a CC circuit with $\underline{A_{V5} = 1}$

Finally we have:

$|A_v| = |A_{v2}\times A_{v3}\times A_{v4}\times A_{v5}| = 1.2\times 10^6$

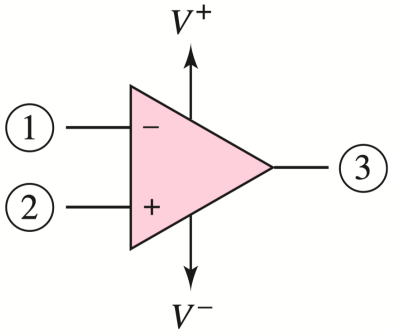
What about the input and output resistances?

Ideal Operational Amplifier Circuits

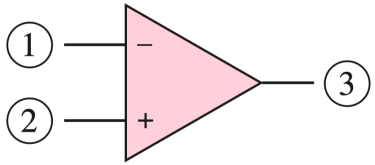
Circuit Representation

- An op-amp is normally made up from 20 to 30 transistors. However, as a typical IC op-amp has parameters that approach the ideal characteristics, **we can treat it as a simple compact device**.

- In most cases, an op-amp requires DC power, so that the internal transistors are biased in the active region.

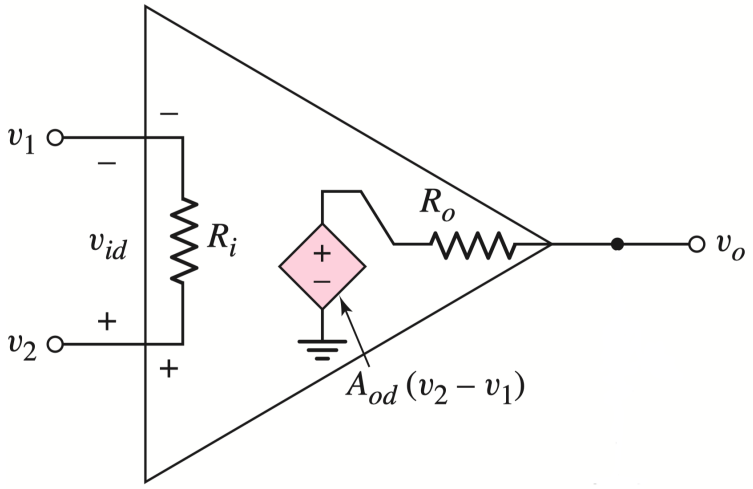


- From a signal point of view, the op-amp has two input terminals and one output terminal. Therefore, we often use a simplified symbol. But keep in mind that the op-amp does require DC input.



Equivalent Circuit

Omitting power supplies, the equivalent circuit for an op-amp is



- The output voltage source is controlled by the *differential* input voltage v_{id} so if there is no load, $v_o = A_{od} v_{id} \implies$ looks like a reasonable **voltage amplifier**

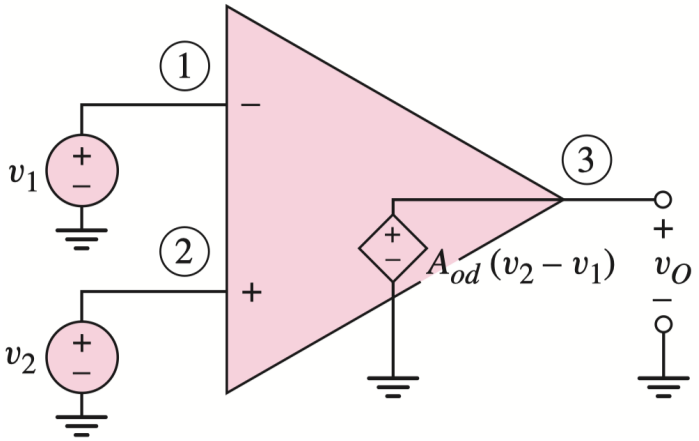
- An operational amplifier generally has **large** input impedance, **low** output impedance and **very high** voltage gain

Ideal Op-Amp Equivalent Circuit

① Inverting input:
$V_{out} = -A_{od}V_1$

② Non-inverting input:
$V_{out} = A_{od}V_2$

③ Output:
$V_{out} = A_{od}(V_2 - V_1)$

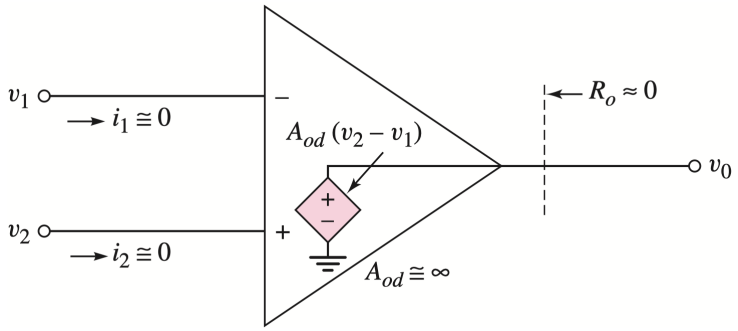


Ideal Parameters:

- the input resistance R_i between terminals 1 and 2 is infinite
- the output terminal of the op-amp acts as an ideal voltage source, i.e., R_o is zero
- the open loop gain A_{od} is very large and approaches infinity

Analysis Method – Virtual Short Principle

- An Op – amp has a very high gain, so for any reasonable output voltage, the input differential voltage $v_p - v_n$ will be **vanishingly small**
- So if the gain is very large then we can say that $v_p - v_n \approx 0$ or $v_p \approx v_n$
- This is a very useful approximation – a '***Golden Rule***' !! *(But remember – it only applies if the gain is **very** large)*; **We say that v_n tracks v_p**



- This leads to the concept of a **virtual short** – the circuit behaves as though there is a short across the inputs because the voltage difference between v_p and v_n is kept zero, *but it is not actually shorted* . Hence the name '**Virtual** Short'. It greatly simplifies the analysis of op-amp circuits
- To apply virtual short principle, the op-amp must be **ideal**.

Nonideal Effects in Operational Amplifiers

Non-ideal Effects – Slew Rate

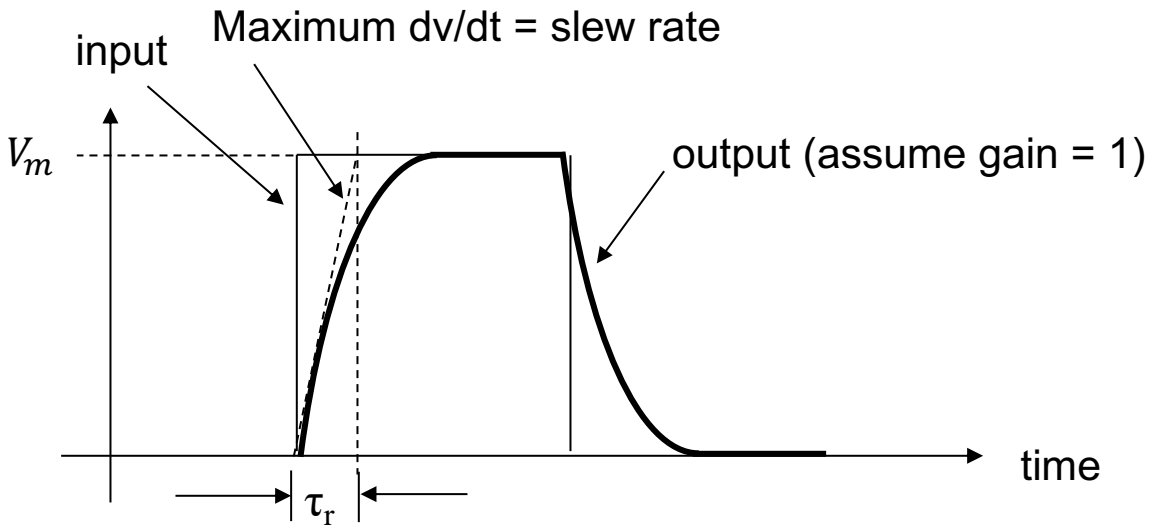
- In the ideal case, we assume the open-loop gain of an op-amp is infinite, hence it has no frequency dependence
- But in reality, the op-amp has a finite gain, and the frequency of the input signal affects the characteristics of the output signal in terms of dynamic response
- Due to the increased number of capacitances in an op-amp, the op-amp's output cannot respond instantaneously to a change in input
- In another word, op-amps have ***a limit on how rapidly the output voltage can change – Slew Rate***

$$SR = \frac{dV_o}{d_t}\Big|_{\max}$$

- The slew rate of the op-amp can limit the performance of a circuit and it can distort the output waveform if its limit is exceeded.
- The slew rate should be as high as possible to ensure the maximum undistorted output voltage

Slew Rate – Step Response

Note that for a step response, **only the rise time** of the output will become limited by the slew rate limit when maximum dv/dt = slew rate.



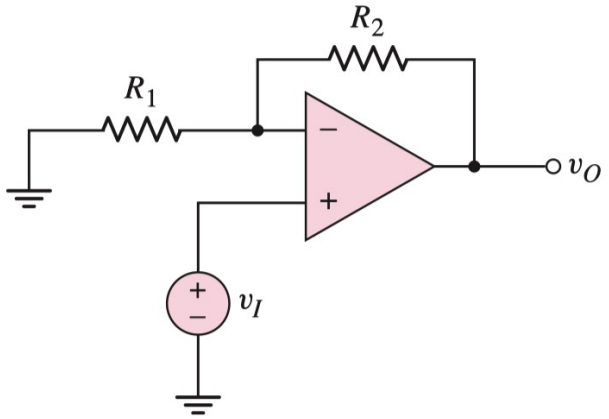
For a first order system, the maximum rate of change of voltage is given by:

$$V_0(t) = V_m\left(1 - e^{-t/\tau_r}\right) \quad \text{Hence} \quad SR = \frac{dV_O(t)}{d_t}\Big|_{\max} = \frac{V_m}{\tau_r} e^{-\frac{t}{\tau_r}}\Big|_{t=0} = \frac{V_m}{\tau_r}$$

So the output will become slew rate limited when $V_m = \tau_r \times \text{slew rate}$

Slew Rate - Sinusoidal Response

Now consider what happens when a sinusoidal input signal is applied. Consider the following non-inverting amplifier:



If $v_I = V_a \sin \omega t$, then we have

$$v_O(t) = V_a \left(1 + \frac{R_2}{R_1}\right) \sin \omega t = V_m \sin \omega t$$

where V_m is the ideal peak value of the sinusoidal output voltage

The rate at which the output voltage changes is:

$$\frac{dv_O(t)}{dt} = \omega V_m \cos \omega t$$

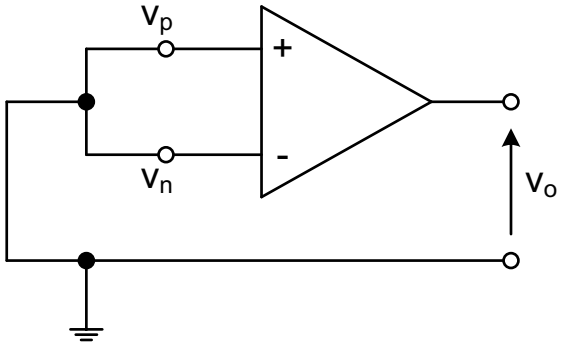
Therefore, the slew rate is: $\omega V_m \cos \omega t \,|_{max} = \omega V_m$

Non-ideal Effects – DC Imperfections

DC imperfections of operational amplifiers include ***offset voltage, bias current, and offset current*.** They result in non-zero output voltage even at zero input voltages. This effect is especially noticeable in high gain or precision DC amplifiers.

- **Offset Voltage**

Suppose an op-amp has both its inputs connected to ground:



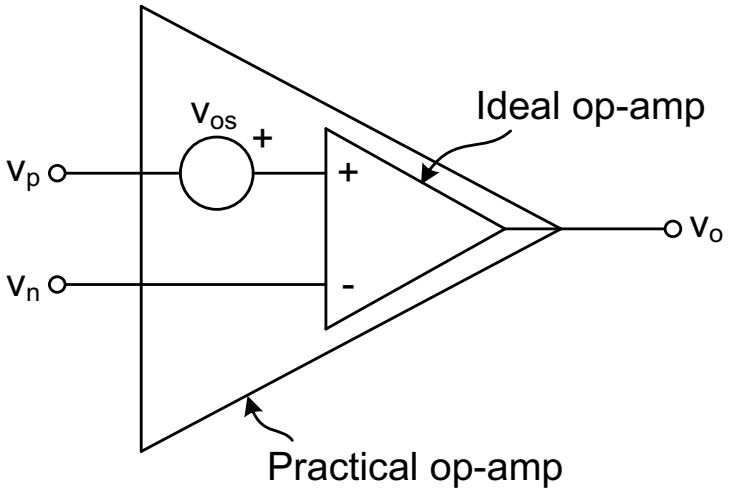
Here $V_p = V_n = 0$ (tied to ground) so **ideally** we expect $V_O = A_{OL}(V_p - V_n) = 0$

However, in **practice,** we usually find $V_O \neq 0$

We can therefore model this contribution to the output voltage in a *practical op-amp* by inserting a DC voltage V_{os} at the input of an *ideal op-amp* as shown:

The offset voltage V_{os} is the equivalent input voltage that would need to be applied (as shown) to make $V_O = 0$

N.B. V_{OS} is always (by convention) assumed connected to the *non-inverting (+) input*, with the polarity shown. (But note that it can be a positive or negative value!)



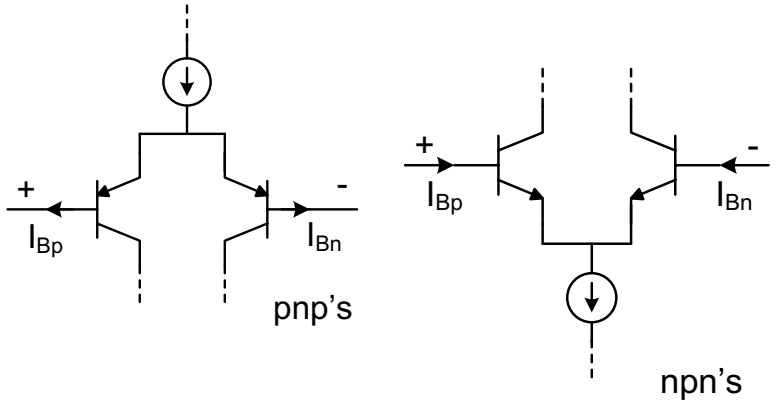
The manufacturer usually quotes the magnitude of V_{OS} – e.g., V_{OS} = 2mV typical, 6mV max.

This means ~50% of the tested op-amp have V_{OS} between -2mV to +2mV, but all have V_{OS} between -6mV and +6mV.

- **Bias Currents**

These are input currents I_{Bp} and I_{Bn} that MUST be provided for the operational amplifier to function properly.

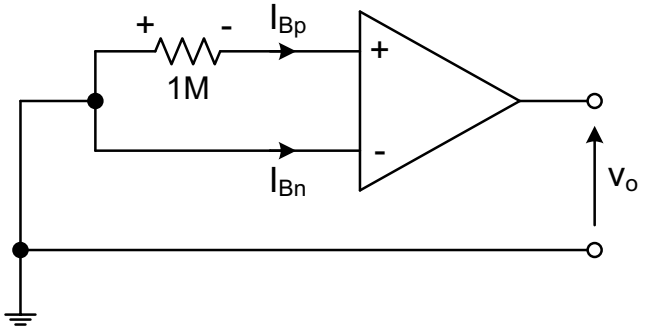
The input bias currents can flow *either in or out* of the op-amp depending on whether the input stage is constructed with npn or pnp transistors:



If pnp transistors are used, the current flows *out* of the input terminals.

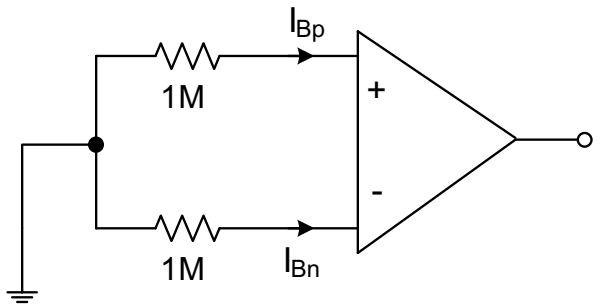
If npn transistors are used, the current flows *into* the input terminals.

If the circuit requires these currents to flow through resistances in the external input circuit, then a voltage will be generated that acts as an input voltage to the op-amp - so it is amplified to give a DC output V_O.



- **The Offset Current**

Even if the two bias currents are made to flow through equal resistances at the input, their effects will still not cancel exactly because the bias currents themselves are usually not quite equal in magnitude. The *difference* between the bias currents is called the ***offset current*** $I_{OS} = |I_{Bp} - I_{Bn}|$



$$V_O = A_V|I_{Bp} - I_{Bn}|\times 1\text{M}$$

These currents are particularly troublesome because they are sensitive to temperature

The manufacturer, after measuring a large number of samples, gives us the input bias current which is the average bias current

$$I_B = \frac{I_{Bp} + I_{Bn}}{2}$$

AND they give us the offset current which is the magnitude of the bias current *difference*

$$I_{OS} = |I_{Bp} - I_{Bn}|$$

For example:

For a 741C: $I_B = 80\ nA\ \ typical\ ,\ \ 500\ \ nA\ \ \max$

$I_{os} = 20\ nA\ \ typical\ ,\ \ 200\ \ nA\ \ \max$

In the WORST possible case, this means either $I_{Bp} = 600nA,\ I_{Bn} = 400nA$

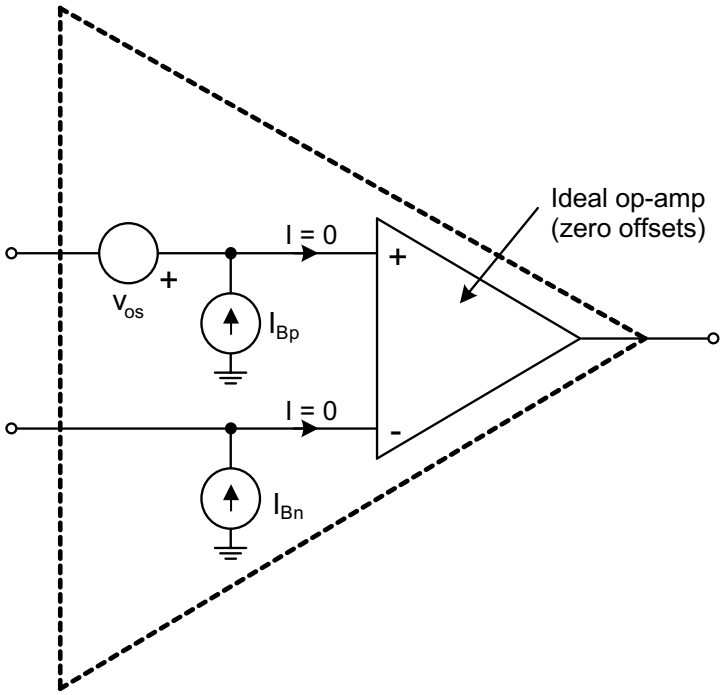
or $I_{Bp} = 400nA,\ I_{Bn} = 600nA$

Summarise this by saying that in all cases

$$I_B - \frac{I_{os}}{2} < [I_{Bp}, I_{Bn}] < I_B + \frac{I_{os}}{2}$$

So the complete model of the op-amp with both offset voltage and bias currents is:

We can use this model to determine the DC offset voltage that will occur in a given circuit.

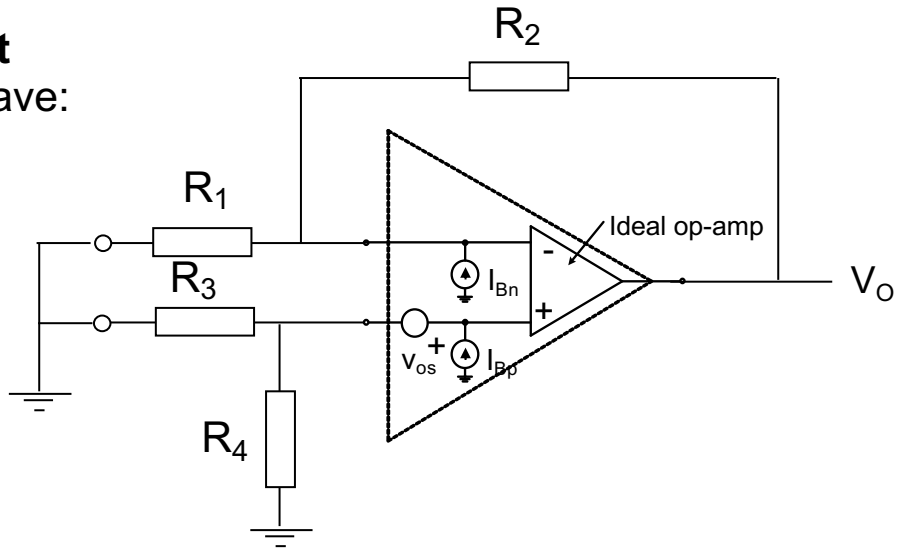


We can determine the contribution to the output voltage from each source individually using the 'principle of superposition'

To determine the contribution due to offset bias alone, assume no input signals are being applied so the two inputs are grounded.

To determine **the contribution from the offset voltage**, turn off the sources I_{Bn} and I_{Bp}, we have:

$$V_{O1} = \pm V_{OS}\left(\frac{R_1 + R_2}{R_1}\right)$$



To determine **the contribution from $\mathbf{I_{Bp}}$**, turn off the sources I_{Bn} and V_{OS}, we have:

$$V_{O2} = -I_{Bp}(R_3||R_4)\left(\frac{R_1 + R_2}{R_1}\right)$$

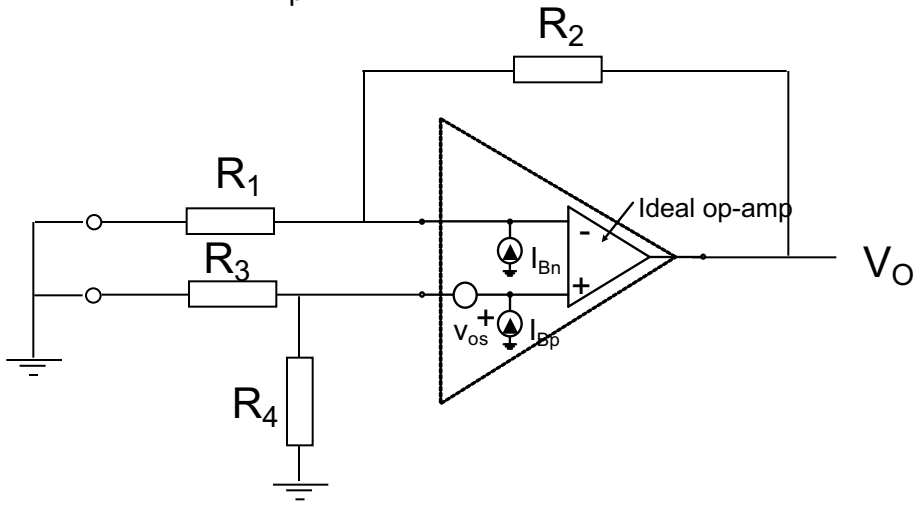
To determine **the contribution from $\mathbf{I_{Bn}}$**, turn off the sources I_{Bp} and V_{OS}, we have:

$$V_{O3} = I_{Bn}R_2$$

The total is:

$$V_O = V_{O1} + V_{O2} + V_{O3} = \pm V_{OS}\left(\frac{R_1 + R_2}{R_1}\right) - I_{Bp}\,(R_3||R_4)\left(\frac{R_1 + R_2}{R_1}\right) + I_{Bn}R_2$$

If we make the resistance 'seen' by I_{Bp} equal to that 'seen' by I_{Bn} , i.e. $R_1 \parallel R_2 = R_3 \parallel R_4$



Then for $V_O = \pm V_{OS}\left(\frac{R_1+R_2}{R_1}\right) - I_{Bp}\,(R_3||R_4)\left(\frac{R_1+R_2}{R_1}\right) + I_{Bn}R_2$

We find for the later part: $-I_{Bp}(R_3||R_4)\left(\frac{R_1+R_2}{R_1}\right) + I_{Bn}R_2 = R_2[-I_{Bp}(R_3||R_4)\left(\frac{R_1+R_2}{R_1R_2}\right) + I_{Bn}]$

$$= R_2\left[-I_{Bp}(R_3||R_4)\left(\frac{1}{(R_1||R_2)}\right) + I_{Bn}\right] = R_2(I_{Bn} - I_{Bp})$$

The only contribution from the bias currents will be due to the difference between them, i.e. the *offset* current.

Feedback on HW3

Q1 Consider the circuit shown in Figure 1.

(a) Determine the ideal output voltage v_O if $v_I = -0.40$ V.

(b) Assume the op-amp is ideal except it has a finite open-loop gain. Determine the actual output voltage if the open-loop gain of the op-amp is $A_{od} = 5\times10^3$.

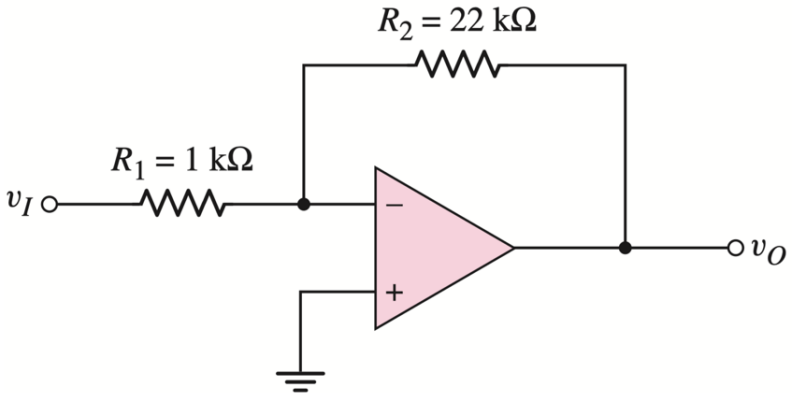


Figure 1

Q2 The op-amp in the circuit shown in Figure 2 is ideal except it has a finite open-loop gain.
(a) If $A_{od} = 10^4$ and $v_o = -2$ V, determine v_I.
(b) If $v_I = 2$ V and $v_o = 1$ V, determine A_{od}

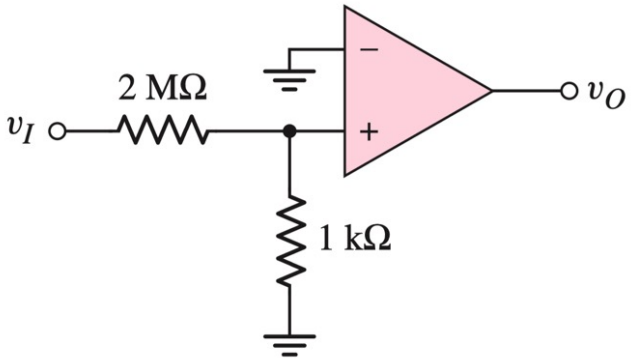


Figure 2

Q3 The parameters of the two inverting op-amp circuits connected in cascade shown in Figure 3 are $R_1 = 10$ kΩ, $R_2 = 80$ kΩ, $R_3 = 20$ kΩ, and $R_4 = 100$ kΩ. For $v_I = -0.15$ V, determine v_{O1}, v_O, i_1, i_2, i_3, and i_4.

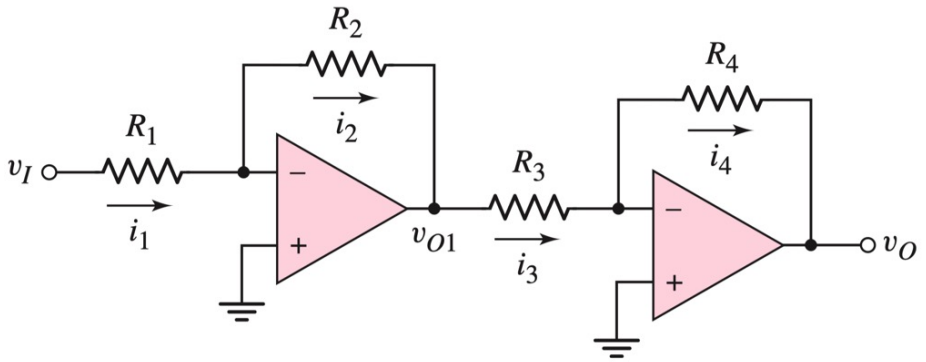


Figure 3

Q4 (a) If an op-amp has a slew-rate of 5 V/μs, find the upper corner frequency for a pulse output voltage of 5 V, 1.5 V, and 0.4 V.

(b) (b) An op-amp with a slew rate of 8 V/μs is driven by a 250 kHz sine wave. What is the maximum output amplitude at which slew-rate limiting is reached?

Q5 For the circuit shown in Figure 4, the input bias current is $I_B = 0.8$ μA and the input offset current is $I_{OS} = 0.2$ μA. Determine the output voltage due to the effect of the input offset current.

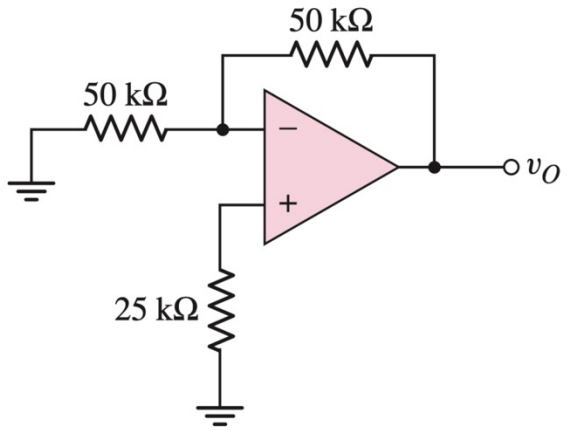


Figure 4

IMPORTANT
New Policies for Final Exams

New measures for the upcoming final exams

1.Bring two documents for admission携带双证参加考试:

a. XJTLU Student ID Card学生证

b. Official Identity Verification Document 官方身份证件

i.Mainland China: Resident Identity Card（居民身份证）;

ii.Hong Kong, Macau, Taiwan: Mainland Travel Permit （通行证）

iii.International: Passport (护照)

2.Use the washroom before admission check. No washroom breaks are allowed within the first two hours and last 15 minutes of each exam.

入场前如厕。考试开始后两小时内及考试结束前15分钟不得离场如厕。

3. (Students) Arrive at least 30 minutes early for admission and metal scanner check.

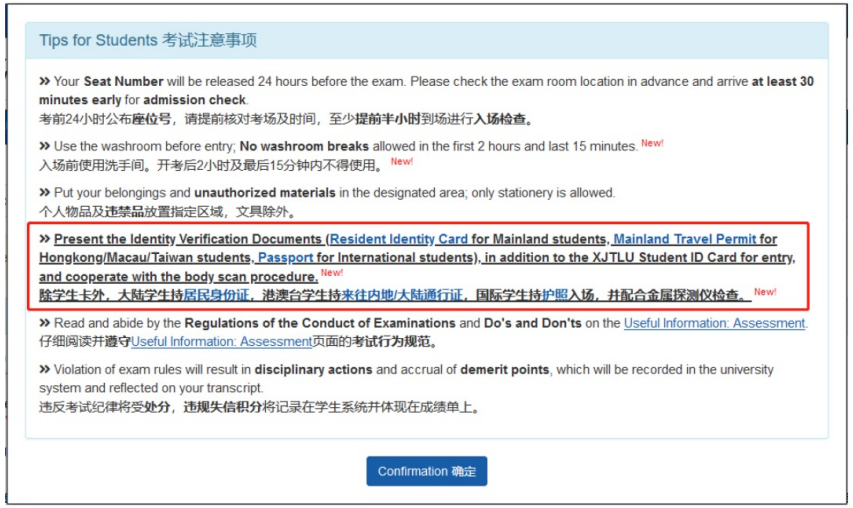
至少提前30分钟到达考场门口进行入场检查。

4.Any unauthorized materials or misbehaviors are strictly prohibited. Violation of exam rules will result in disciplinary actions and the imposition of demerit points on transcripts.

严禁携带任何考试违禁品及任何违纪行为。违反考试规则者将受到纪律处分，并在成绩单上记录违规积分。

Communication to students

- **Tips for students on Timetables page**



Tips for Students 考试注意事项

» Your **Seat Number** will be released 24 hours before the exam. Please check the exam room location in advance and arrive **at least 30 minutes early** for **admission check**.
考前24小时公布**座位号**，请提前核对考场及时间，至少**提前半小时**到场进行**入场检查**。

» Use the washroom before entry; **No washroom breaks** allowed in the first 2 hours and last 15 minutes. New!
入场前使用洗手间。开考后2小时及最后15分钟内不得使用。 New!

» Put your belongings and **unauthorized materials** in the designated area; only stationery is allowed.
个人物品及**违禁品**放置指定区域，文具除外。

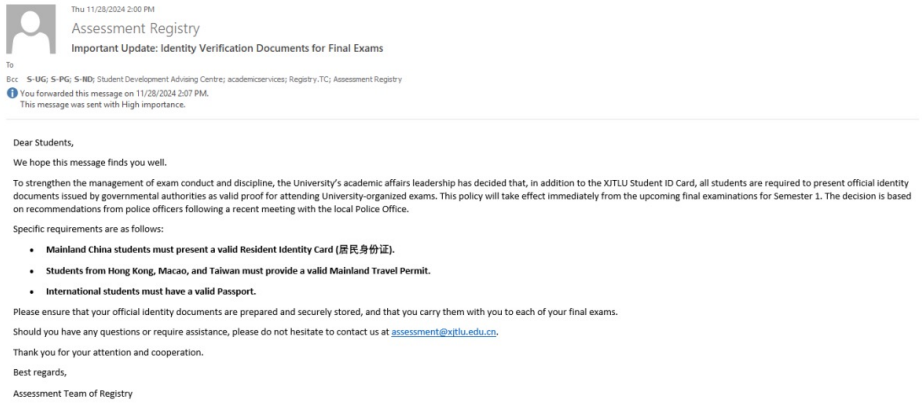
» **Present the Identity Verification Documents (Resident Identity Card for Mainland students, Mainland Travel Permit for Hongkong/Macau/Taiwan students, Passport for International students), in addition to the XJTLU Student ID Card for entry, and cooperate with the body scan procedure.** New!
除学生卡外，大陆学生持居民身份证，港澳台学生持来往内地/大陆通行证，国际学生持护照入场，并配合金属探测仪检查。 New!

» Read and abide by the **Regulations of the Conduct of Examinations** and **Do's and Don'ts** on the Useful Information: Assessment.
仔细阅读并**遵守**Useful Information: Assessment页面的**考试行为规范。**

» Violation of exam rules will result in **disciplinary actions** and accrual of **demerit points**, which will be recorded in the university system and reflected on your transcript.
违反考试纪律将受**处分**，**违规失信积分**将记录在学生系统并体现在成绩单上。

Confirmation 确定

- **E-mail notice to students from Assessment**



Thu 11/28/2024 2:00 PM
Assessment Registry
Important Update: Identity Verification Documents for Final Exams
To
Bcc: S-UG; S-PG; S-ND; Student Development Advising Centre; academicservices; Registry.TC; Assessment Registry
You forwarded this message on 11/28/2024 2:07 PM.
This message was sent with High importance.

Dear Students,

We hope this message finds you well.

To strengthen the management of exam conduct and discipline, the University's academic affairs leadership has decided that, in addition to the XJTLU Student ID Card, all students are required to present official identity documents issued by governmental authorities as valid proof for attending University-organized exams. This policy will take effect immediately from the upcoming final examinations for Semester 1. The decision is based on recommendations from police officers following a recent meeting with the local Police Office.

Specific requirements are as follows:

- **Mainland China students must present a valid Resident Identity Card (居民身份证).**
- **Students from Hong Kong, Macao, and Taiwan must provide a valid Mainland Travel Permit.**
- **International students must have a valid Passport.**

Please ensure that your official identity documents are prepared and securely stored, and that you carry them with you to each of your final exams.

Should you have any questions or require assistance, please do not hesitate to contact us at assessment@xjtlu.edu.cn.

Thank you for your attention and cooperation.

Best regards,

Assessment Team of Registry

- **Registry Wechat article**

See you in next semester...