# Integrated Electronics & Design

# IC Fabrication Techniques II

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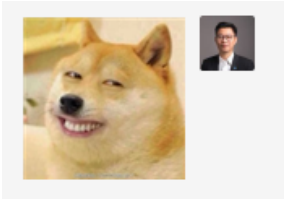
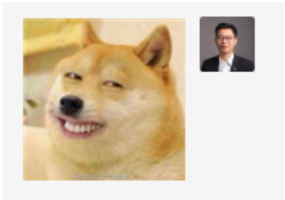
***May 2024***

https://www.xjtlu.edu.cn/en/departments/academic-departments/electrical-and-electronic-engineering/staff/chun-zhao

# IC Fab.Tech. OUTLINE

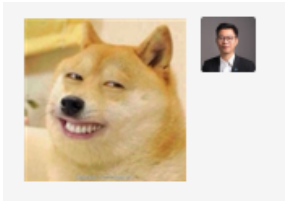
- Thin Film Formation
- Photolithography and Ecthing
- Doping
- **IC Resistor**
- **Sheet Resistance**
- **Diode**
- nMOSFET: Process Flow
- nMOSFET: Fab. and Layout
- nMOSFET: Layout Rules





# IC Fabrication Techniques

## OUTLINE

- **IC Resistor** 
- **Sheet Resistance**
- **Diode**

# Process Flow Example #1: Resistor

< 10μm x 1μm

($10^{-7}$ $cm^2$)

**Integrated R**

~1cm x 1mm

($10^{-1}$ $cm^{-2}$)

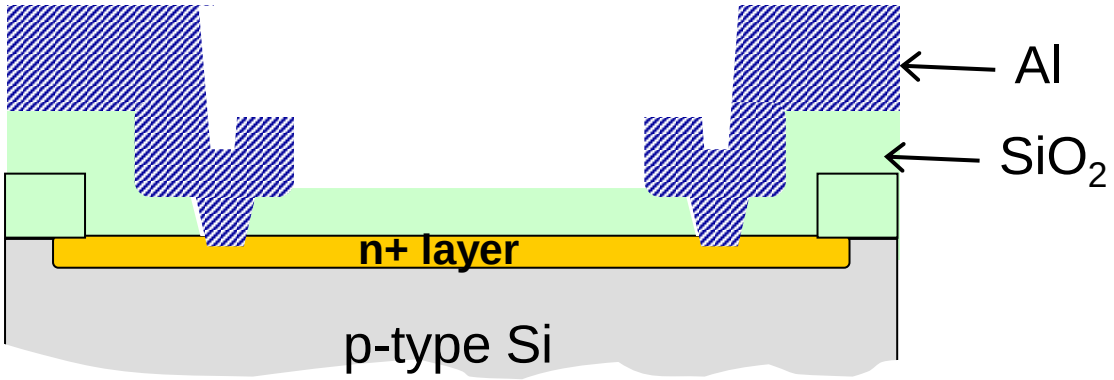
**Discrete R**

# Process Flow Example #1: Resistor

< 10μm x 1μm

($10^{-7}$ $cm^2$)

**Integrated R**




~1cm x 1mm

($10^{-1}$ $cm^{-2}$)

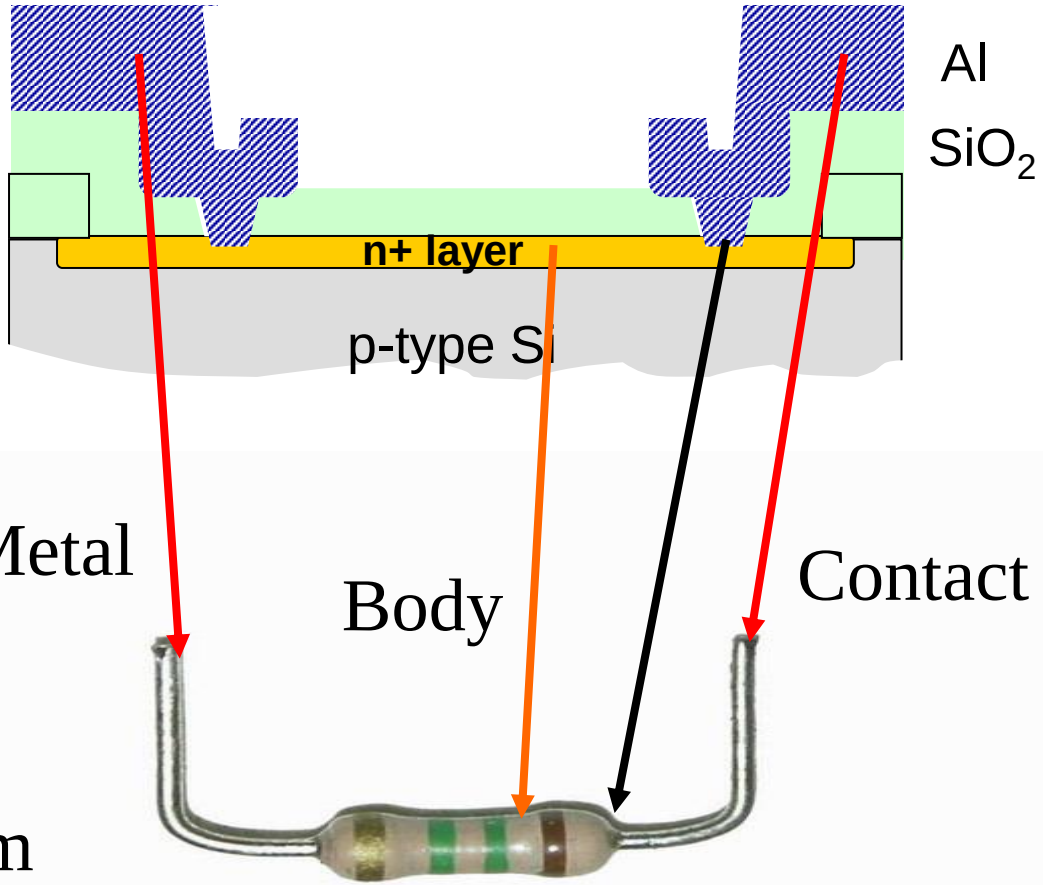
**Discrete R**

# Process Flow Example #1: Resistor

< 10μm x 1μm

($10^{-7}$ $cm^2$)

**Integrated R**

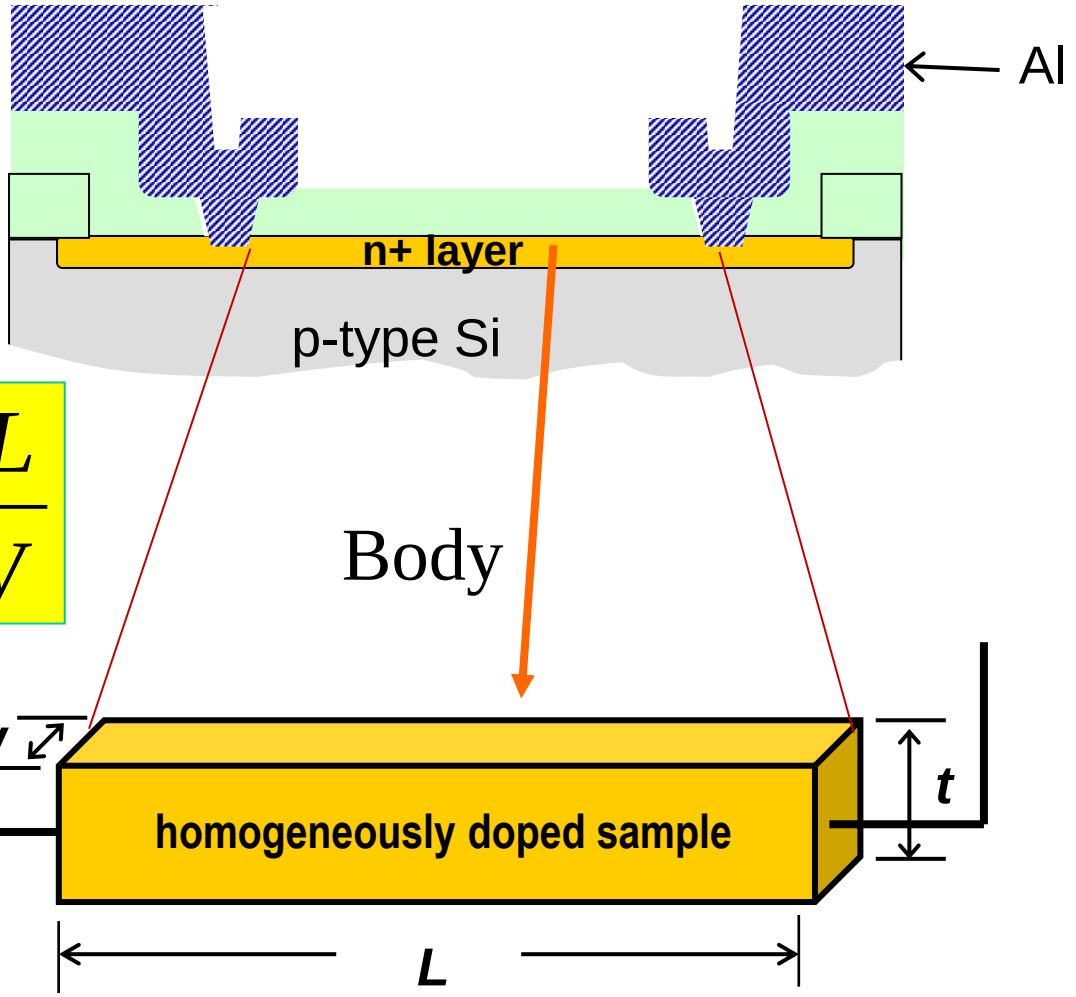



~1cm x 1mm

($10^{-1}$ $cm^{-2}$)

**Discrete R**

# Process Flow Example #1: Resistor




$$R \equiv \frac{\rho L}{A} = \frac{\rho L}{tW}$$

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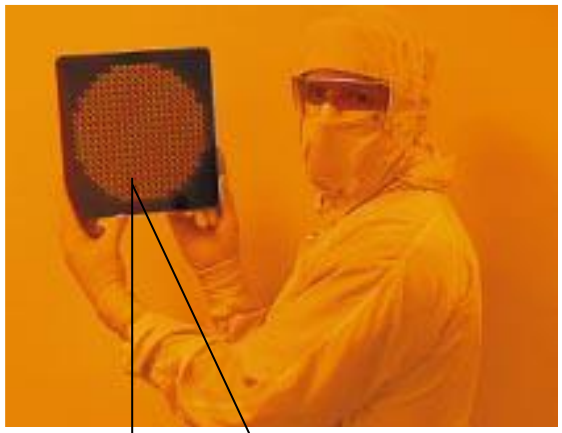
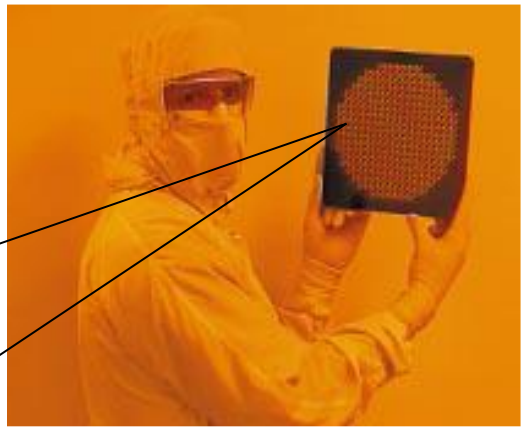
# Process Flow Example #1: Resistor



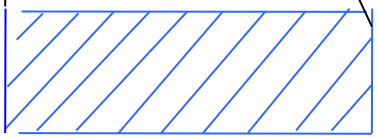
**3 Masks**

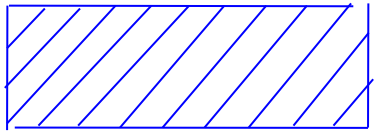


Mask 1 for "body"

Mask 3 for "metal"

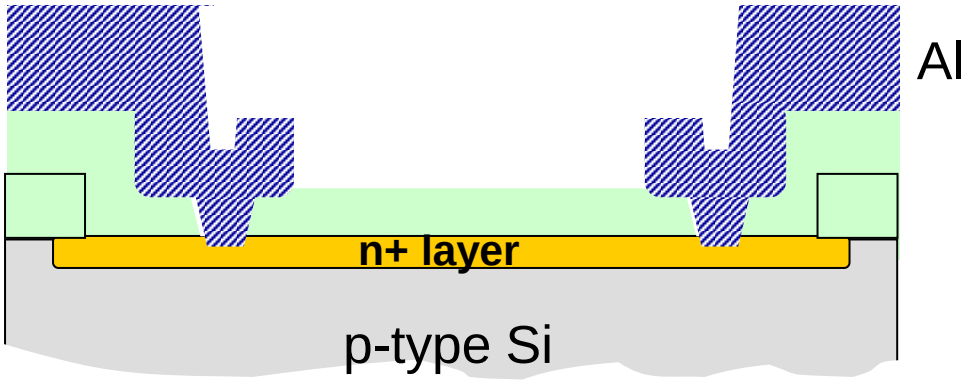
Mask 2 for "contact"





# Process Flow Example #1: Resistor

**A -- A**

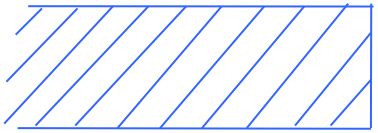


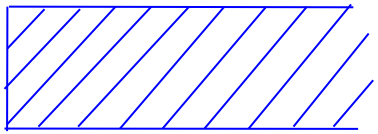

**Layout:**

negative resist

**Oxide mask (dark field)**
**or Active mask**

**Contact mask (dark field)**



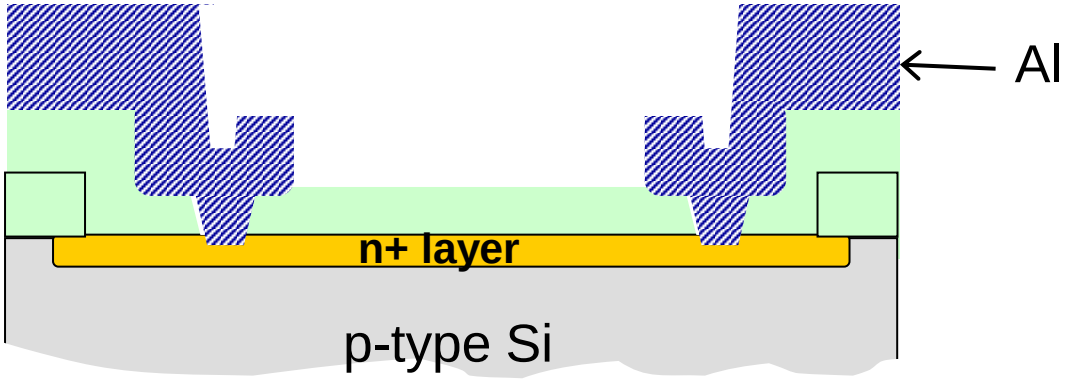


**Al mask (clear field)**

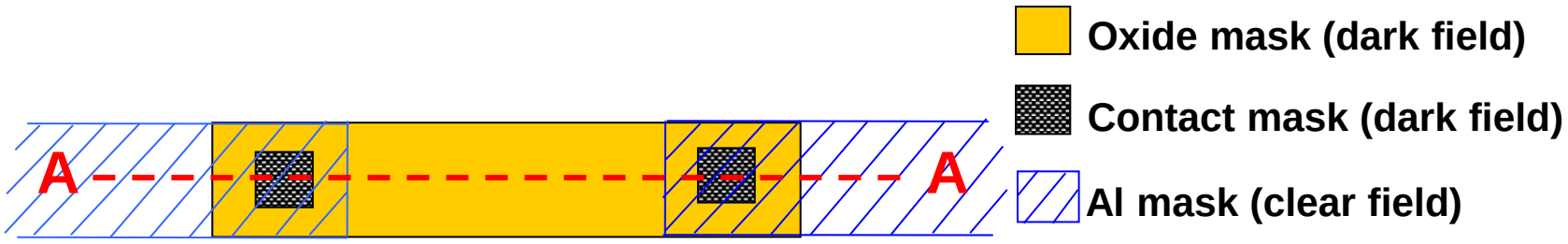
positive resist

# Process Flow Example #1: Resistor

A -- A




**Patterns transfer to wafer:**



# Process Flow Example #1: Resistor

**Three-mask process:**

**Starting material: p-type wafer with $N_A = 10^{16}$ cm$^{-3}$**

**Step 1:** grow 500 nm of $SiO_2$

**Step 2:** pattern oxide using the oxide mask (dark field)

**Step 3:** implant phosphorus and anneal to form an n-type layer with $N_D = 10^{20}$ cm$^{-3}$ and depth 100 nm

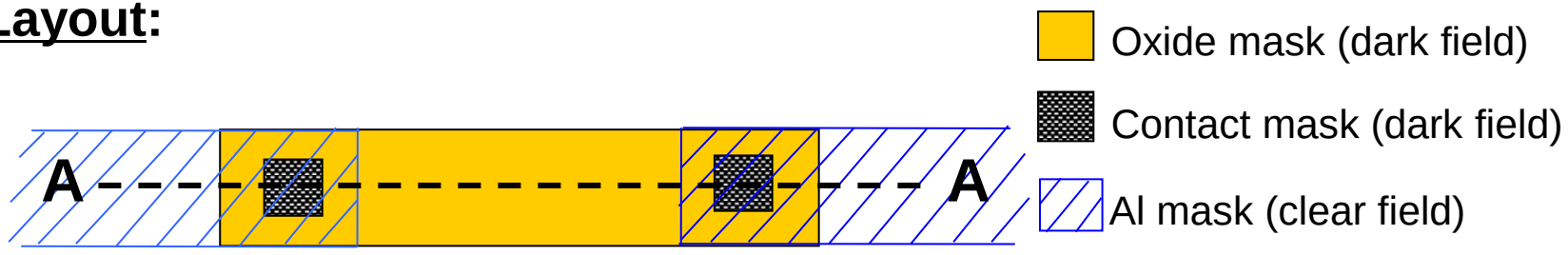
**Step 4:** deposit oxide to a thickness of 500 nm

**Step 5:** pattern deposited oxide using the contact mask (dark field)

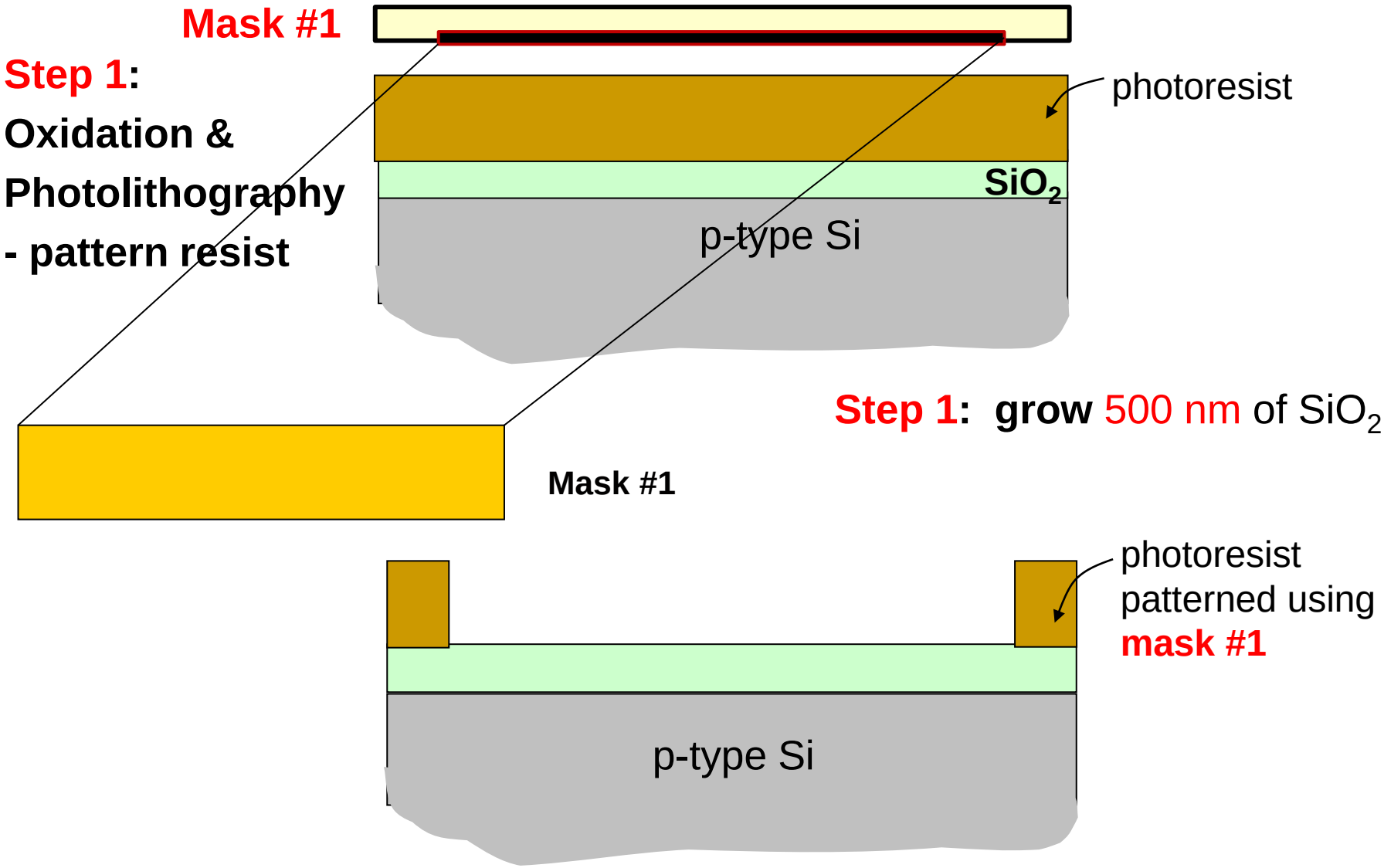
**Step 6:** deposit aluminum to a thickness of 1 μm

**Step 7:** pattern using the aluminum mask (clear field)

**Layout:**



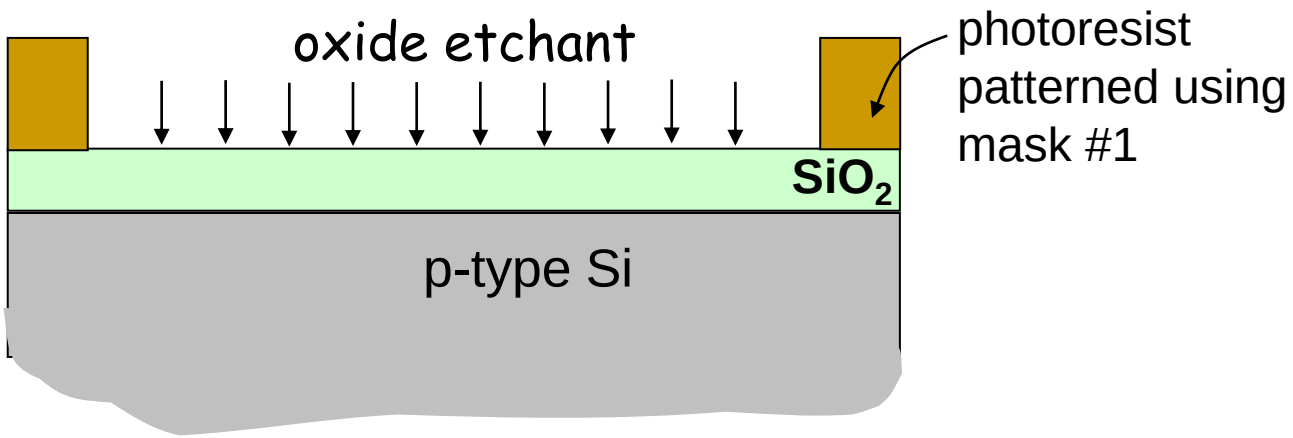
# A-A Cross-Section: oxidation, photolithography & etching



# A-A Cross-Section: oxidation, photolithography & etching

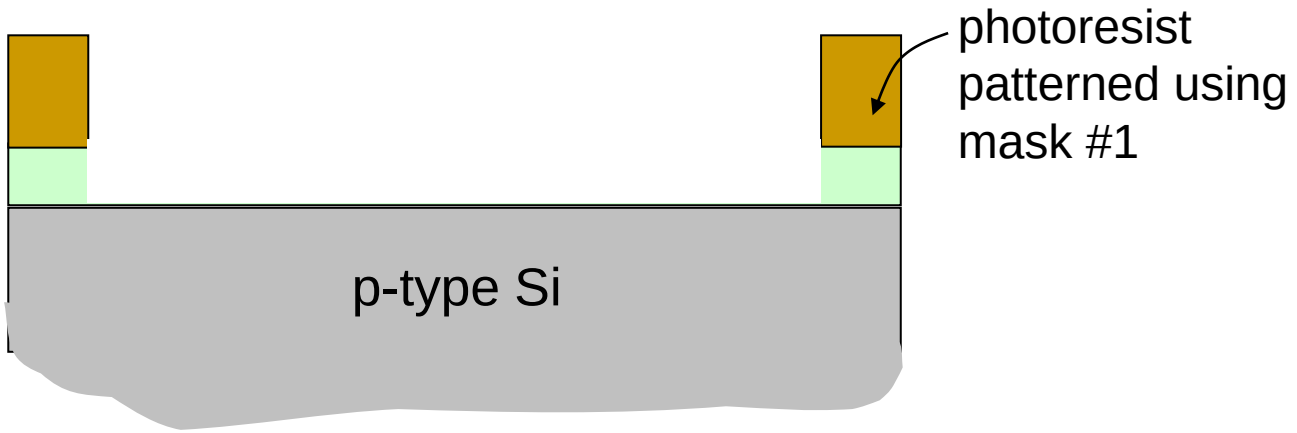
**Step 2:**

**Pattern oxide**

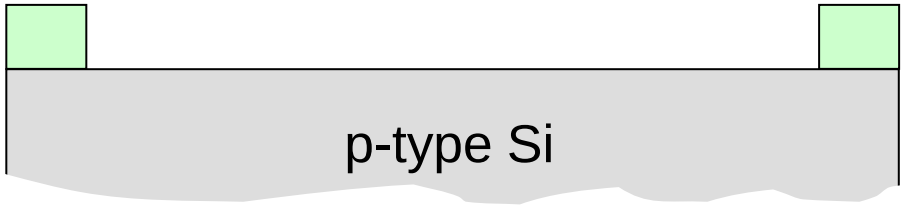



$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O$

**Step 2: pattern** oxide using the oxide mask (dark field)



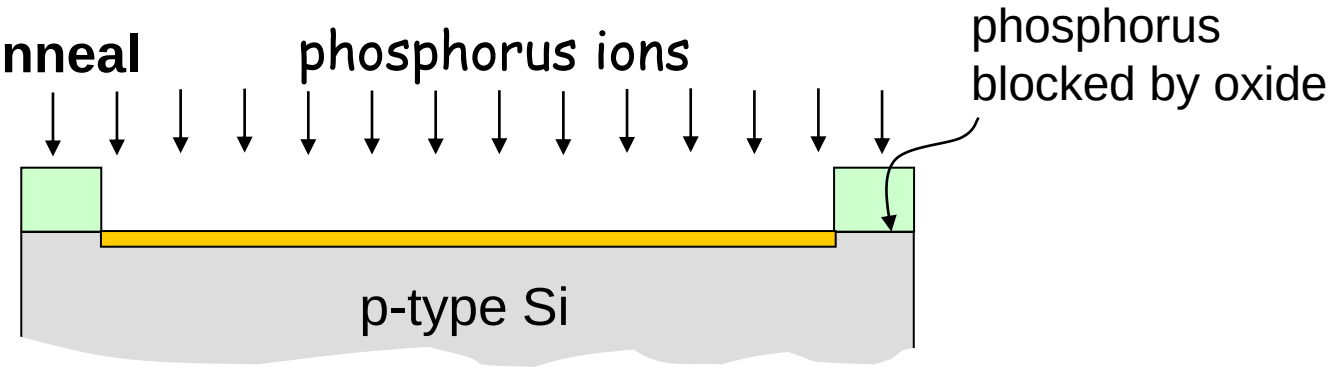
# A-A Cross-Section: doping & annealing



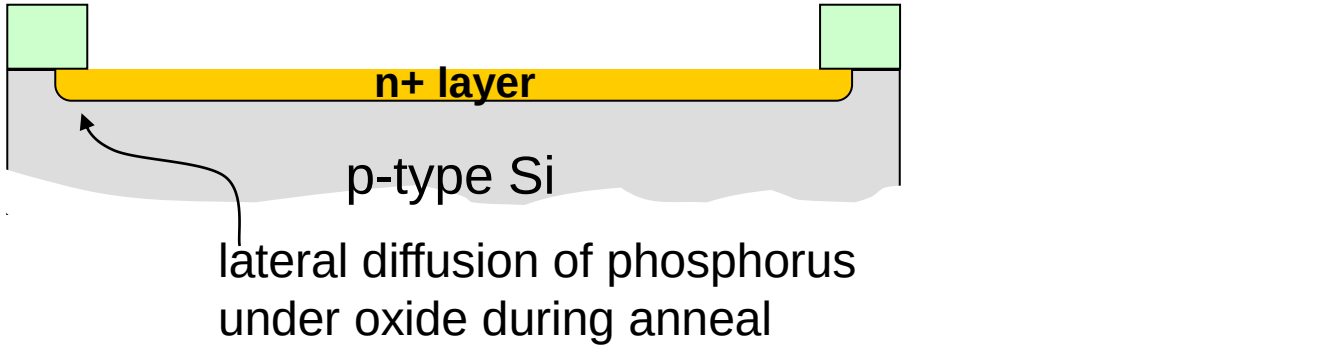

**Step 3: implant** phosphorus and **anneal** to form an n-type layer with $N_D = 10^{20}$ cm$^{-3}$ and depth 100 nm

**Step 3: Implant & Anneal**

phosphorus **implant**:

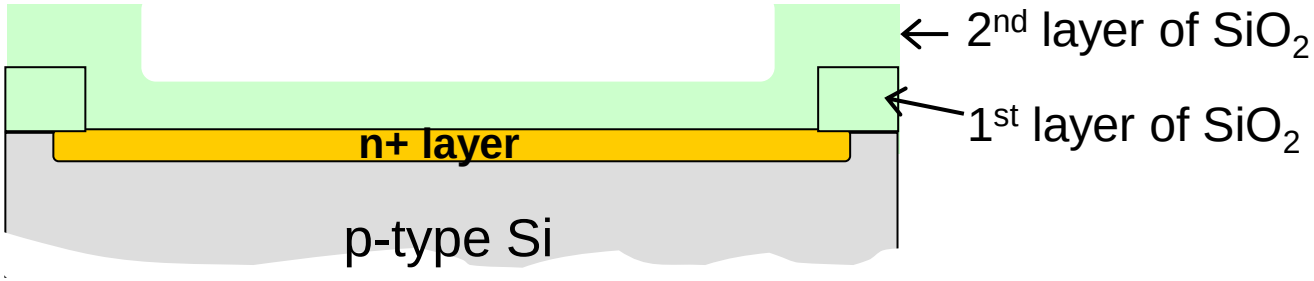



after **anneal** of phosphorus implant:



# A-A Cross-Section: Metal contact

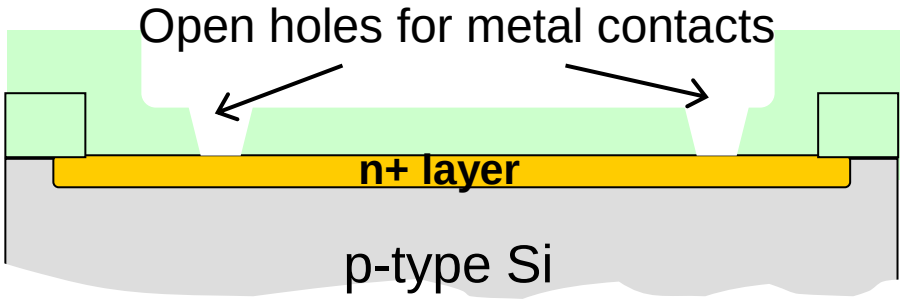
**Step 4: Deposit 500 nm oxide**




**Step 4: deposit** oxide to a thickness of 500 nm

**Mask #2**

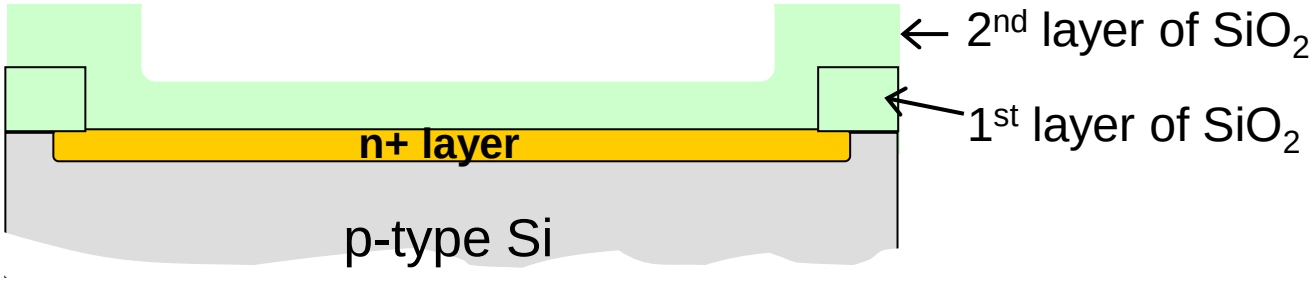
**Step 5: Pattern oxide**




**Step 5: pattern** deposited oxide using the **contact mask** (dark field)

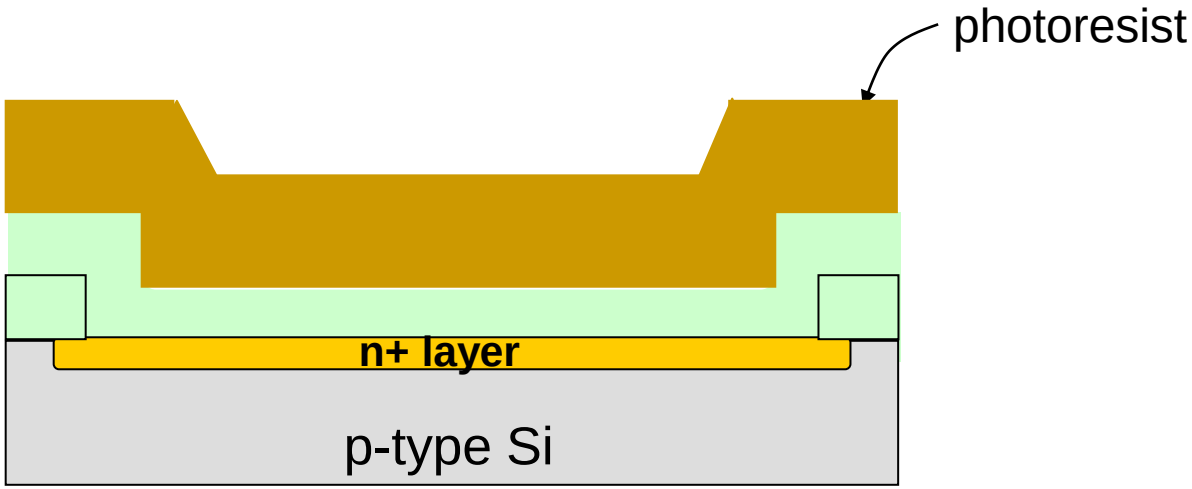
# A-A Cross-Section: Metal contact

**Step 4: Deposit 500 nm oxide**




**Step 5:**

**Pattern oxide**

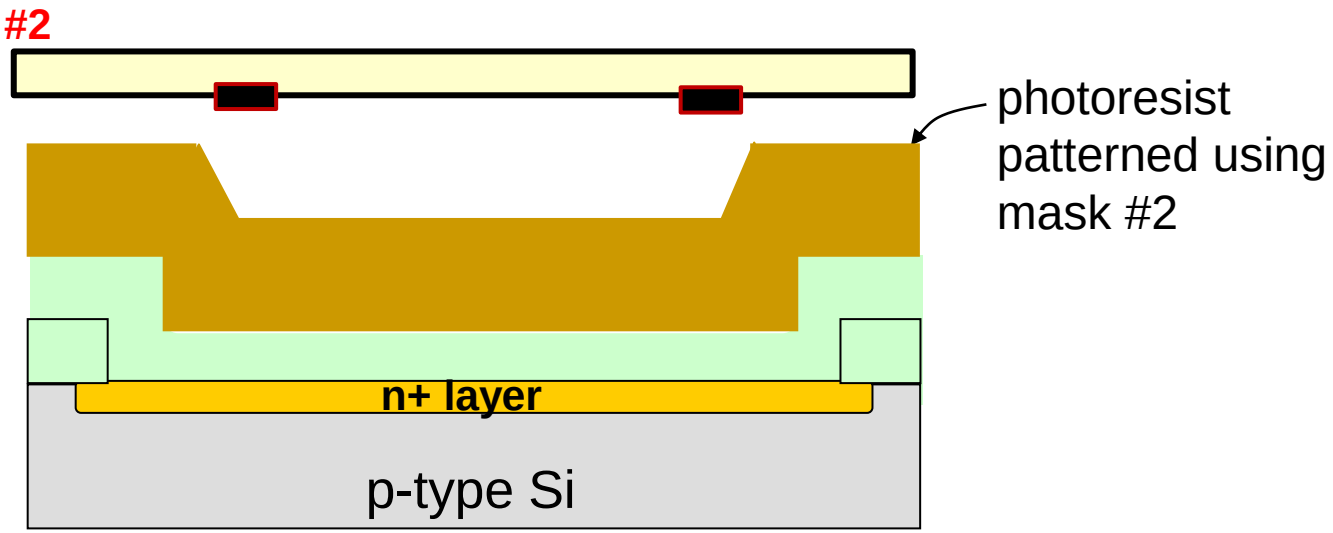



**Mask #2**

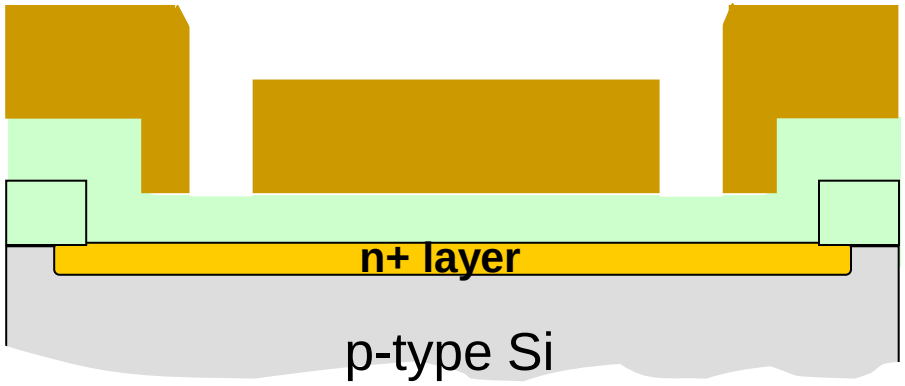
# A-A Cross-Section: Metal contact

**Step 5**:

**Pattern oxide**



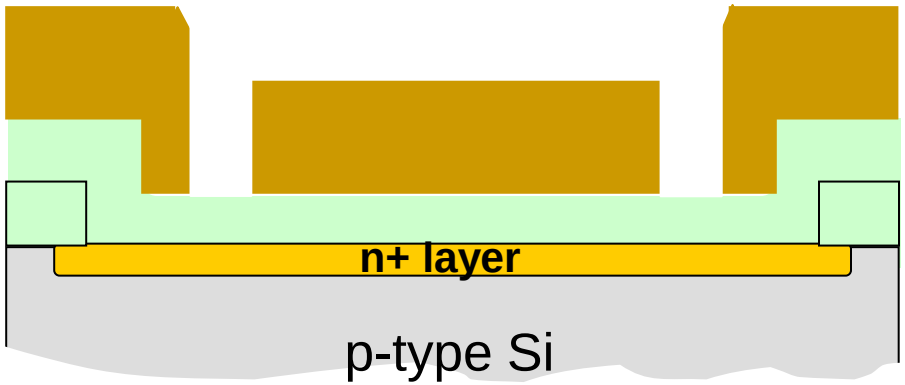


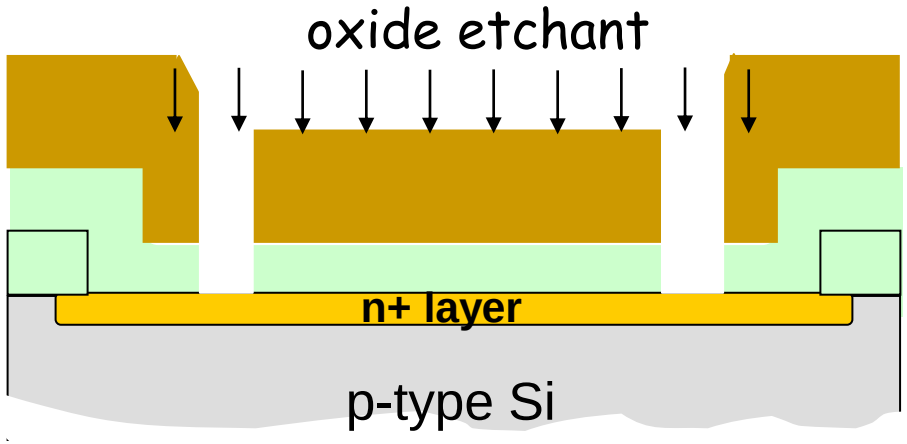


# A-A Cross-Section: Metal contact

**Step 5**:

**Pattern oxide**

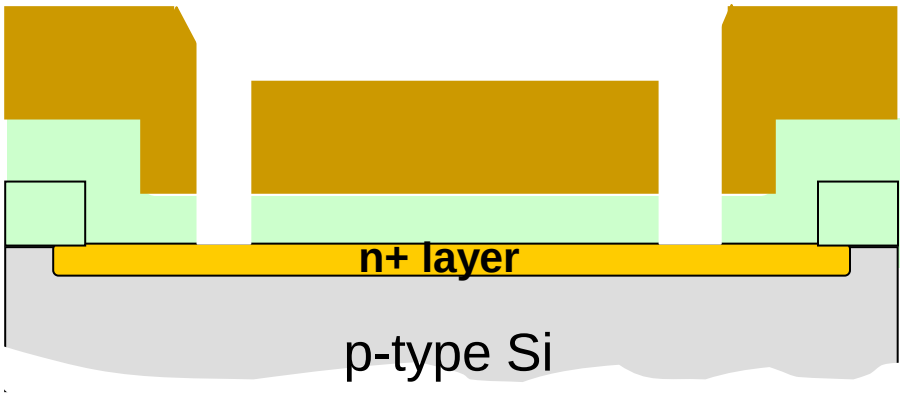


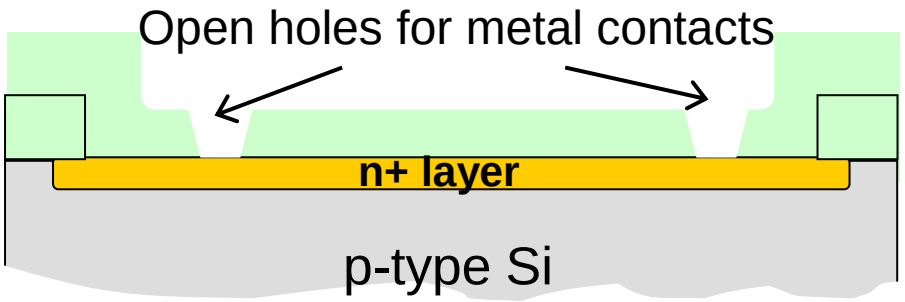



# A-A Cross-Section: Metal contact

**Step 5**:

**Pattern oxide**




**deposition, photolithography & etching**

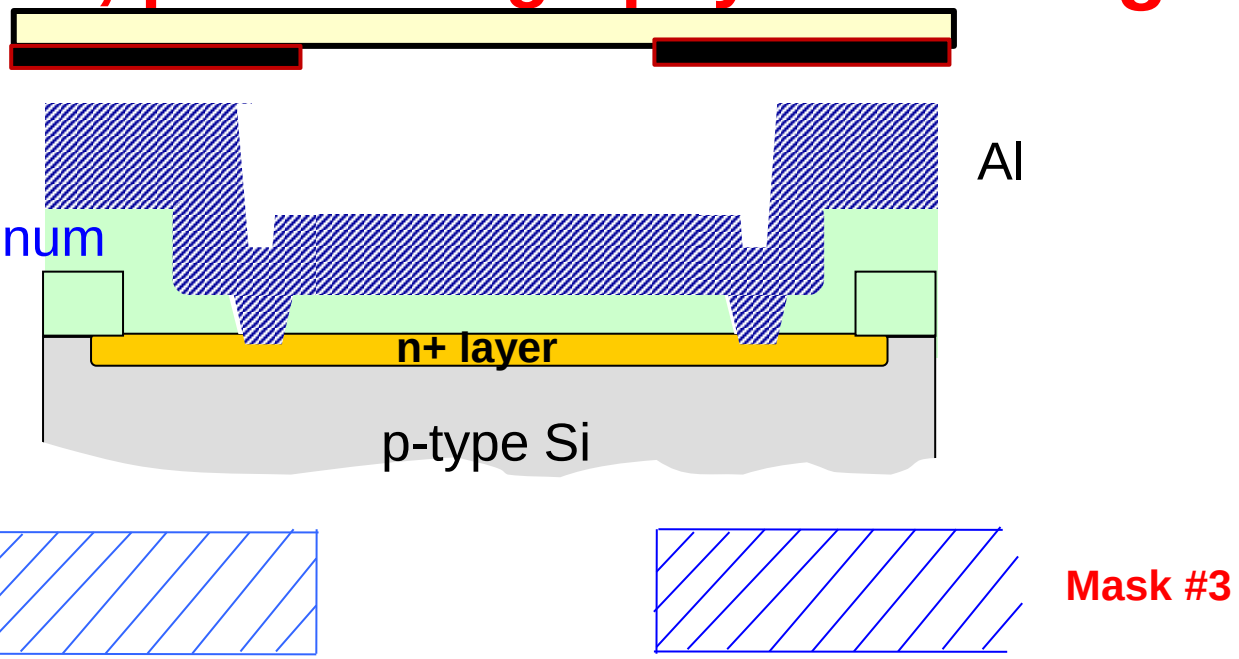
# A-A Cross-Section: metallization

## deposition, photolithography & etching

**Step 6:**

**Al deposition**

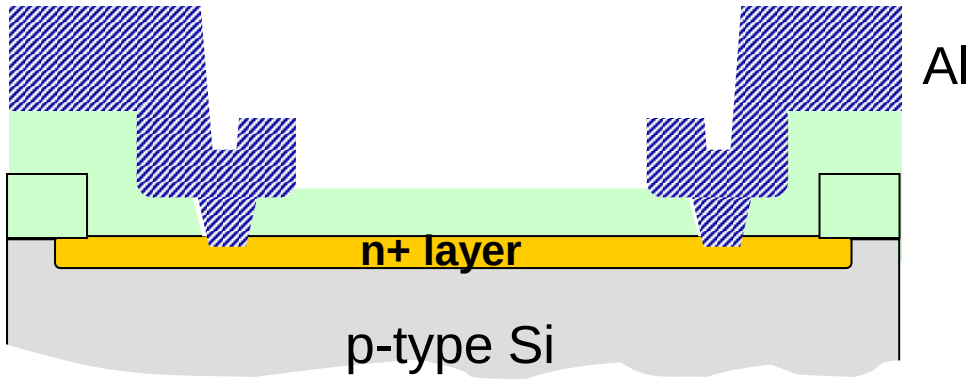
**Step 6: deposit** aluminum to a thickness of 1 μm



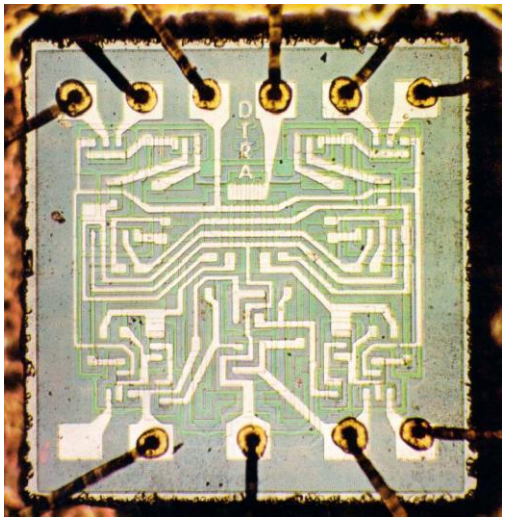

**Step 7:**

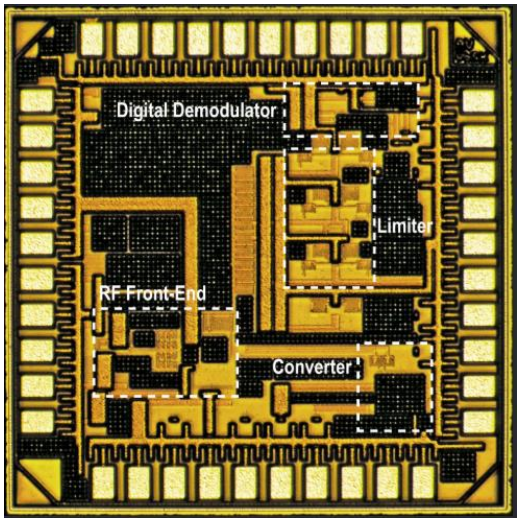
**Pattern metal**

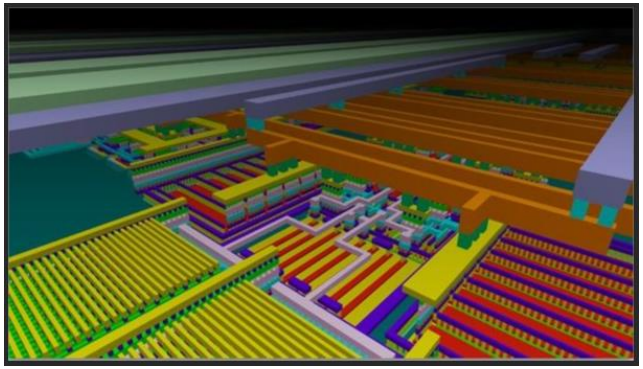
**Step 7: pattern** using aluminum mask (clear field)



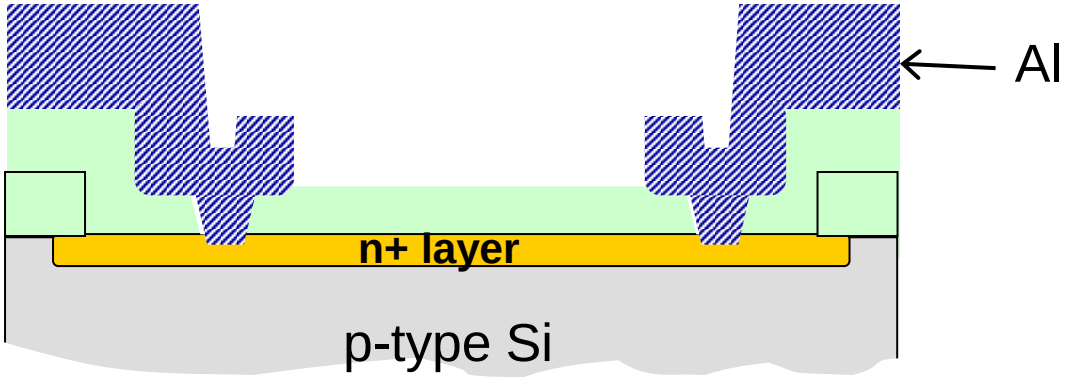
# Summary





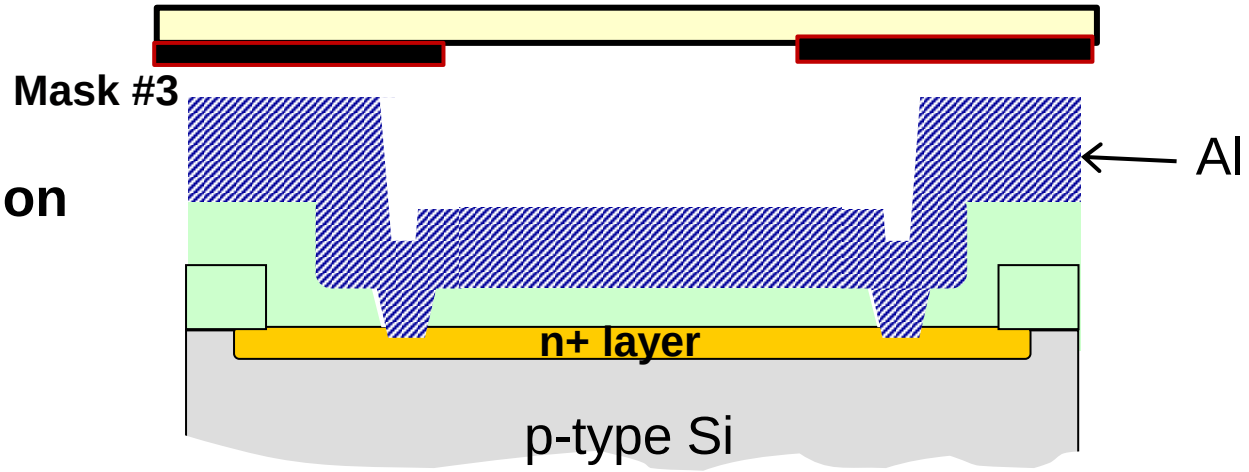
**After 7 steps**

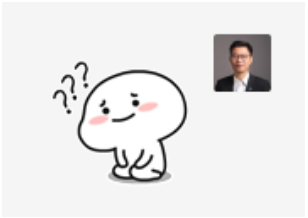


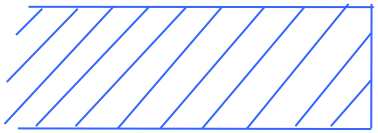
# Layer-to-Layer Alignment

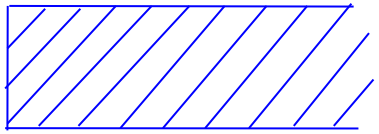
**Step 6:**

**Al deposition**



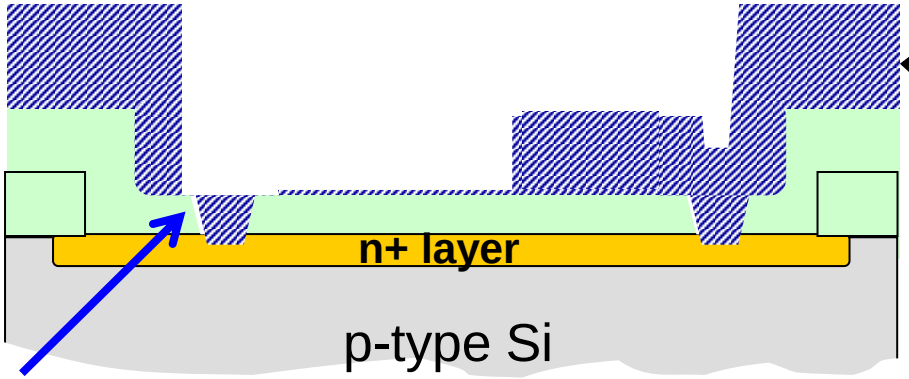








**Step 7:**

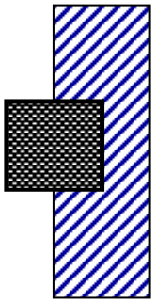
**Pattern metal**



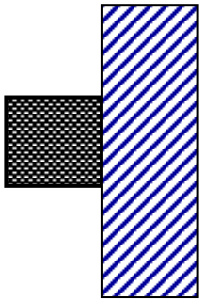

**Open circuit**

# Importance of Layer-to-Layer Alignment

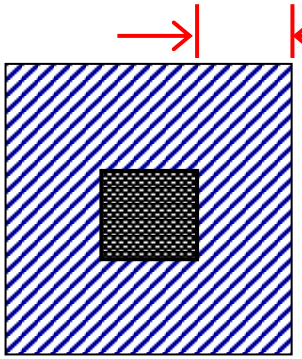
Example: metal line to contact hole



→ marginal contact



→ no contact!



safety margin to allow for misalignment

→ **Design Rules are needed:**

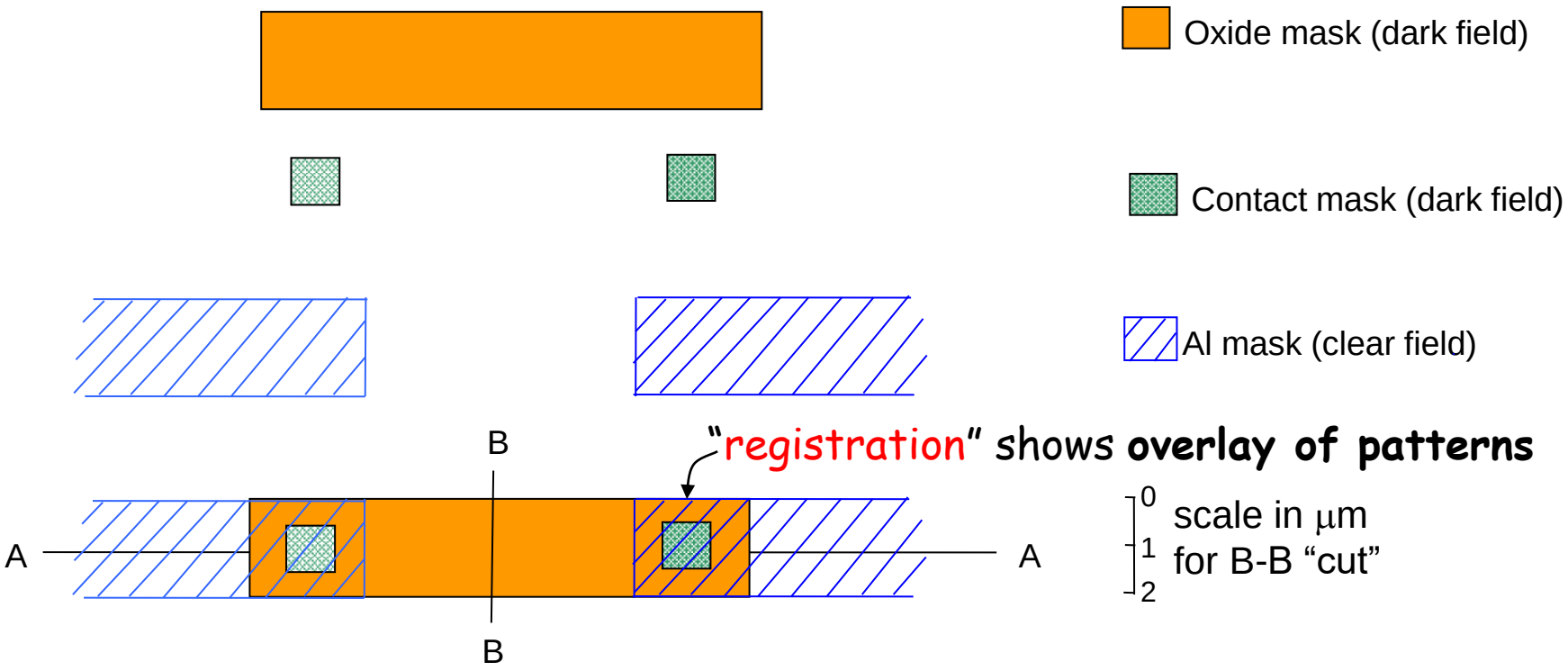
- Interface between designer & process engineer
- Guidelines for designing masks

**Example of Design Rule:**

If the minimum feature size is $2\lambda$, then the safety margin for overlay error is $\lambda$.

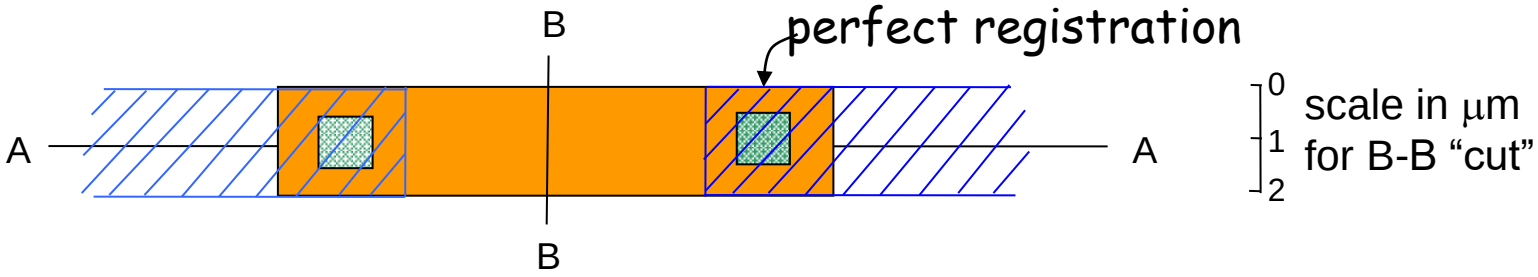
# Registration of Each Mask

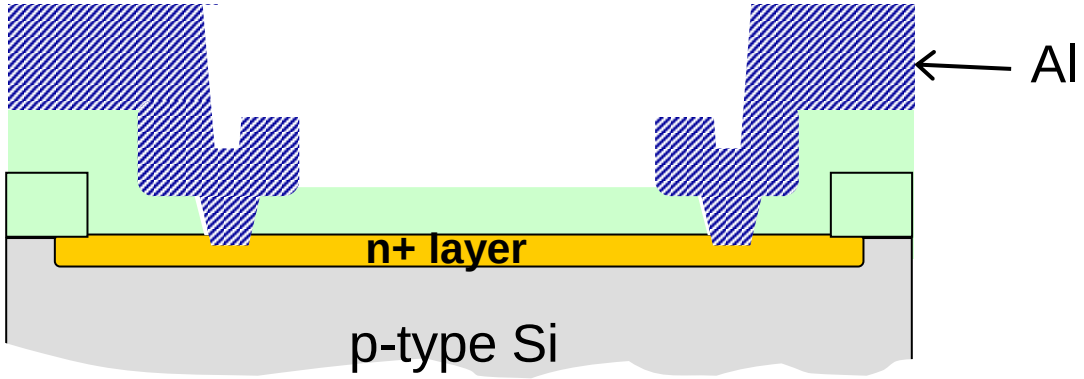
Registration of mask patterns is critical: show separate layouts to avoid ambiguity



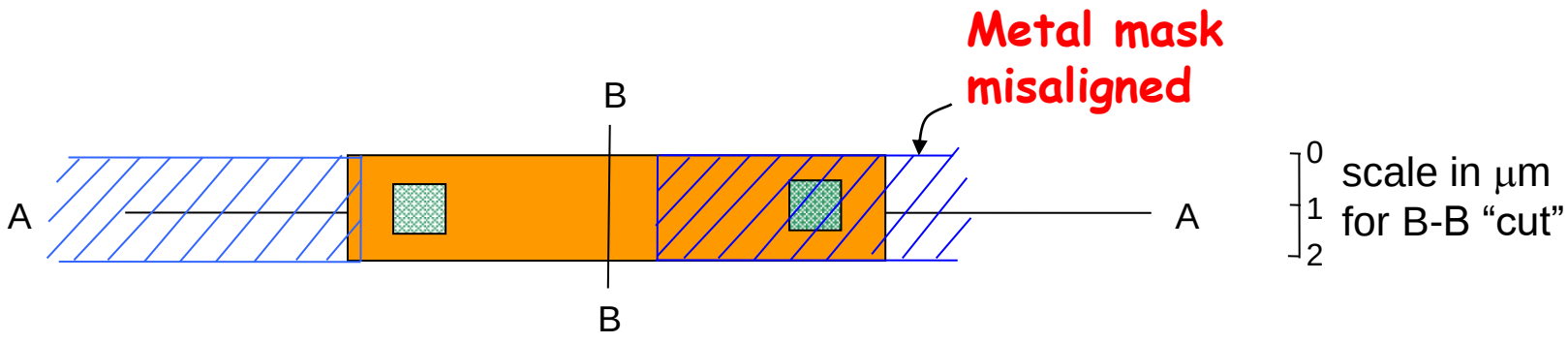

Registration of one mask to the next (also called "alignment" and "overlay") is a crucial aspect of lithography

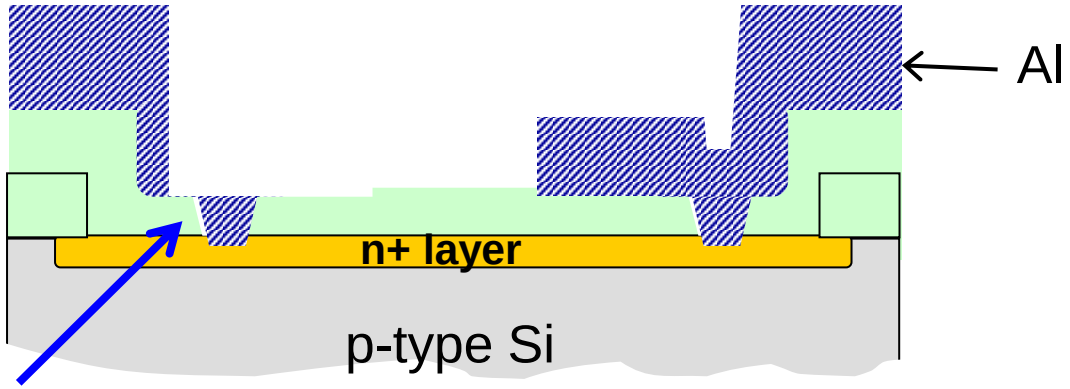
# Same Layout but with registration (alignment)



# Same Layout but with misregistration (misalignment)



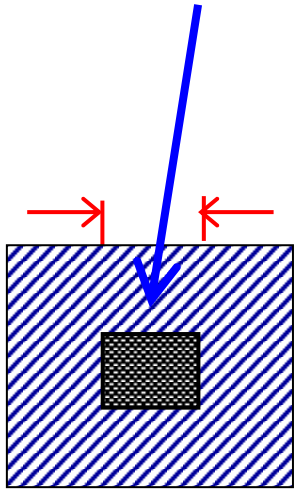




**Open circuit**

# Example of Design Rule: MOSIS

Implementation System

- **A minimum feature size is**



**Using 2λ to stand for the minimum feature size**

the smallest dimension that can be produced.

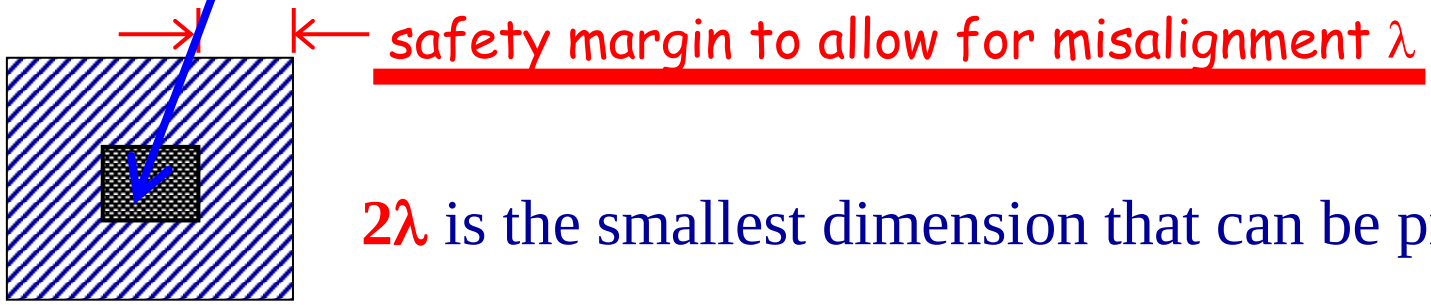
Intel & IBM: **2λ = 32nm → 22nm**

SMIC: **2λ = 14nm**

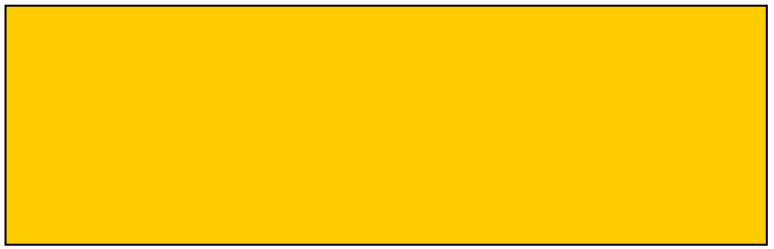
TSMC: **2λ = 7nm → 5nm**

# Example of Design Rule: MOSIS implementation

- If the **minimum feature size is 2λ**, then the minimum active area width is **3λ**, the minimum metal width is **3λ**, and the safety margin for overlay error is **λ**.

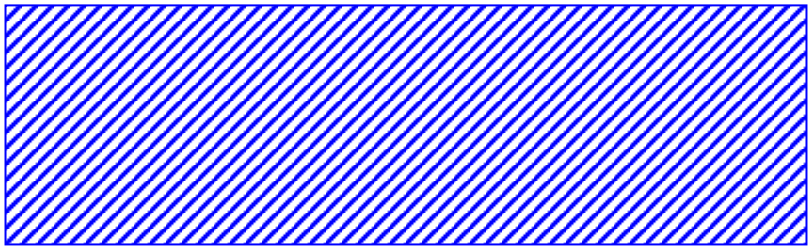



**2λ** is the smallest dimension that can be produced.



the minimum active area width is **3λ**.

**For IC resistors, the width can be 2λ.**



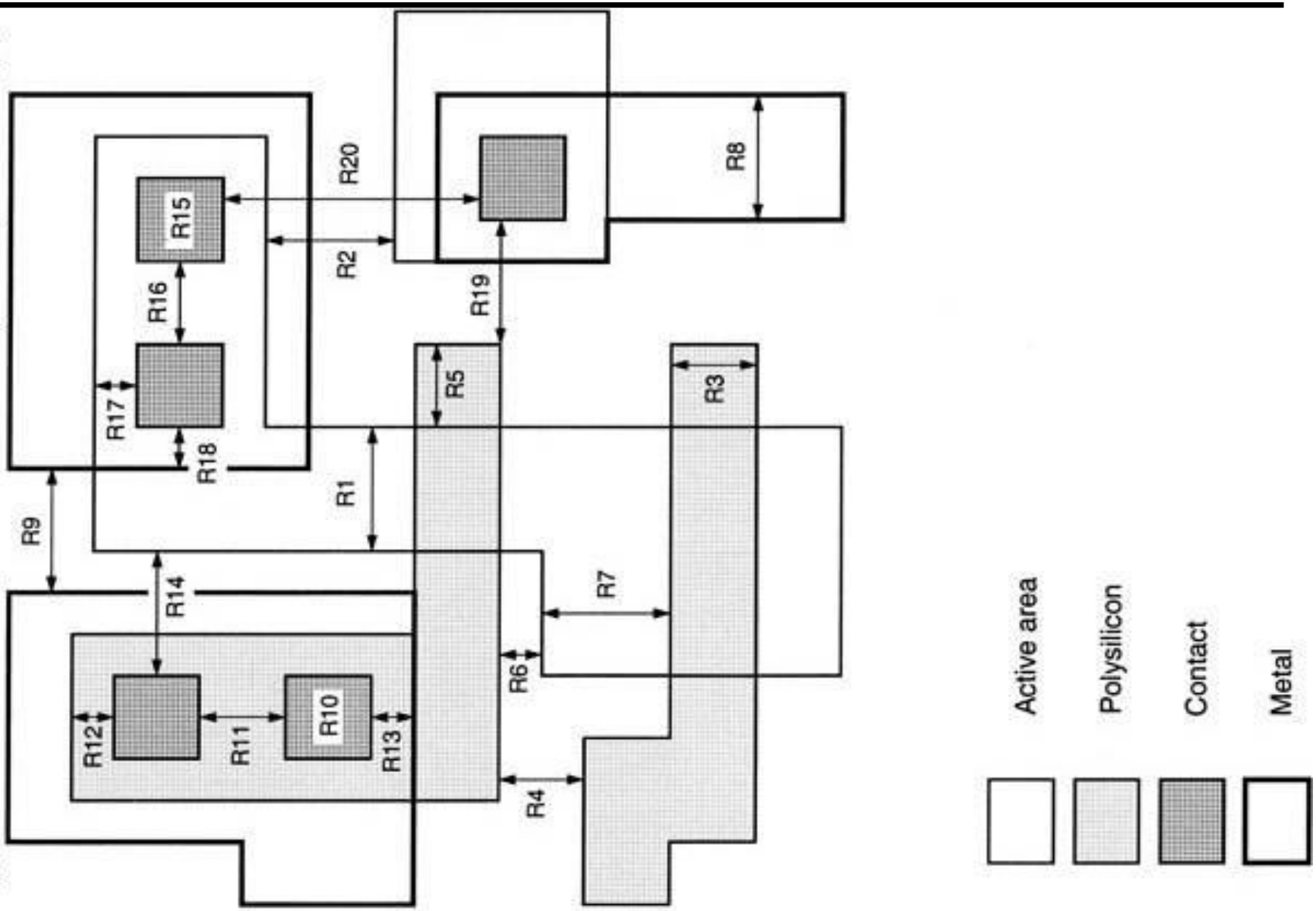
the minimum metal width is **3λ**.

## MOSIS Layout Design Rules (sample set)

| *Rule number* | *Description* | *λ-Rule* |
|---|---|---|
| | **Active area rules** | |
| R1 | Minimum active area width | 3λ |
| R2 | Minimum active area spacing | 3λ |
| | **Polysilicon rules** | |
| R3 | Minimum poly width | 2λ |
| R4 | Minimum poly spacing | 2λ |
| R5 | Minimum gate extension of poly over active | 2λ |
| R6 | Minimum poly-active edge spacing (poly outside active area) | 1λ |
| R7 | Minimum poly-active edge spacing (poly inside active area) | 3λ |
| | **Metal rules** | |
| R8 | Minimum metal width | 3λ |
| R9 | Minimum metal spacing | 3λ |
| | **Contact rules** | |
| R10 | Poly contact size | 2λ |
| R11 | Minimum poly contact spacing | 2λ |
| R12 | Minimum poly contact to poly edge spacing | 1λ |
| R13 | Minimum poly contact to metal edge spacing | 1λ |
| R14 | Minimum poly contact to active edge spacing | 3λ |
| R15 | Active contact size | 2λ |
| R16 | Minimum active contact spacing (on the same active region) | 2λ |
| R17 | Minimum active contact to active edge spacing | 1λ |
| R18 | Minimum active contact to metal edge spacing | 1λ |
| R19 | Minimum active contact to poly edge spacing | 3λ |
| R20 | Minimum active contact spacing (on different active regions) | 6λ |

MOSIS layout design rules

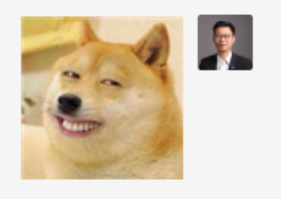
# **MOSIS** layout design rules



# IC Fabrication Techniques

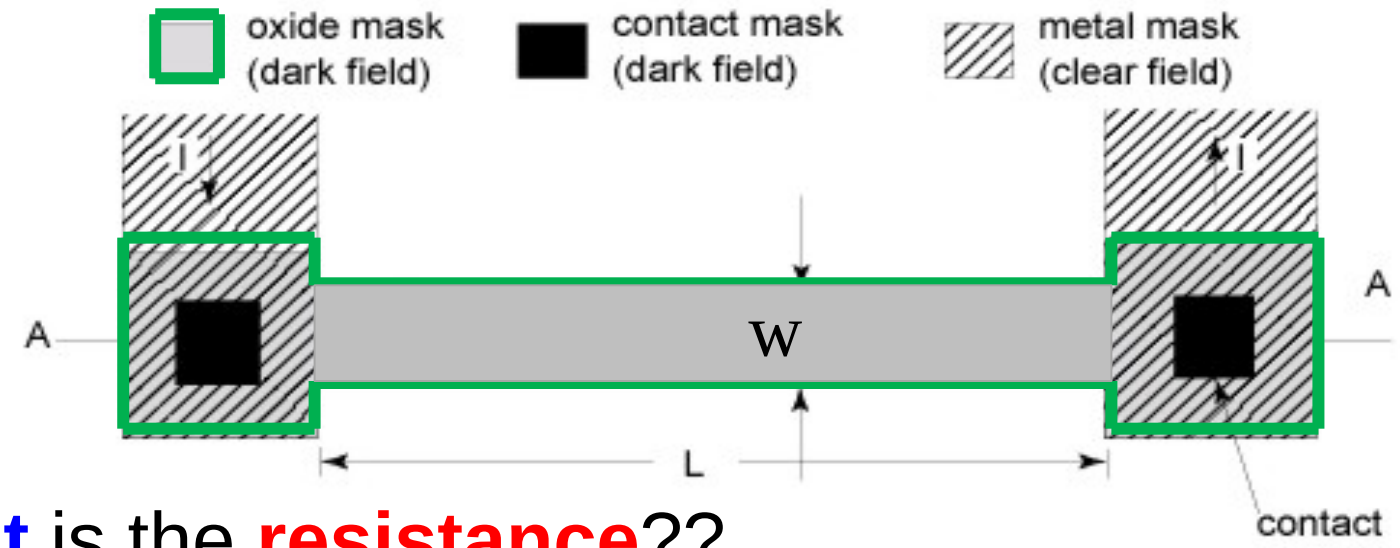
## OUTLINE

- IC Resistor
- **Sheet Resistance** ⟵
- Diode

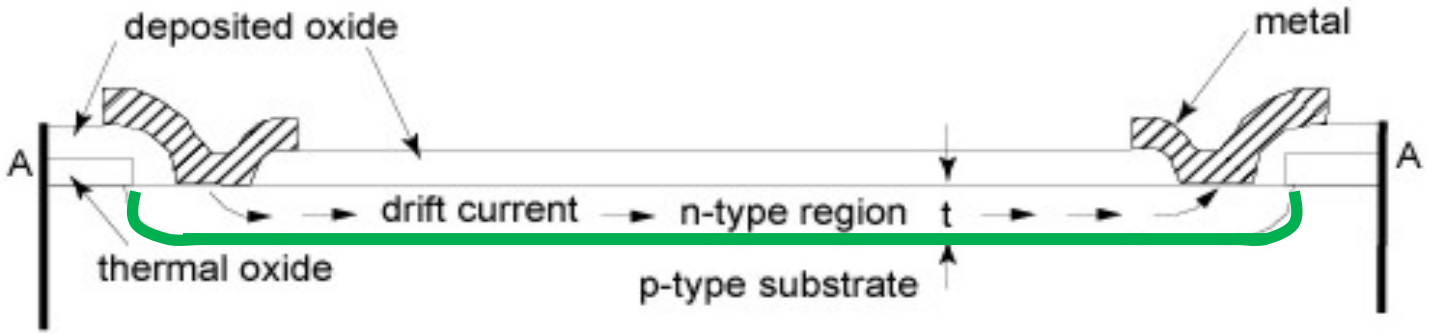


# Using Sheet Resistance (**Rs**)

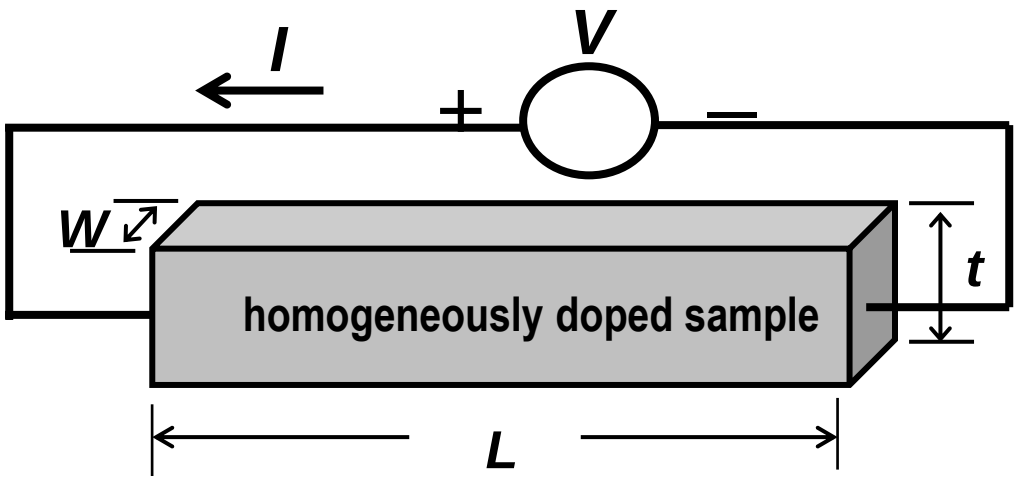
- **Ion-implanted (or "diffused") IC resistor**




**What** is the **resistance**??



# Electrical Resistance




Resistance $R \equiv \frac{V}{I} = \frac{\rho L}{A} = \frac{\rho L}{tW} = \left(\frac{\rho}{t}\right)\left(\frac{L}{W}\right)$ (Unit: ohms)

where $\rho$ is the resistivity **(Ω•cm)**

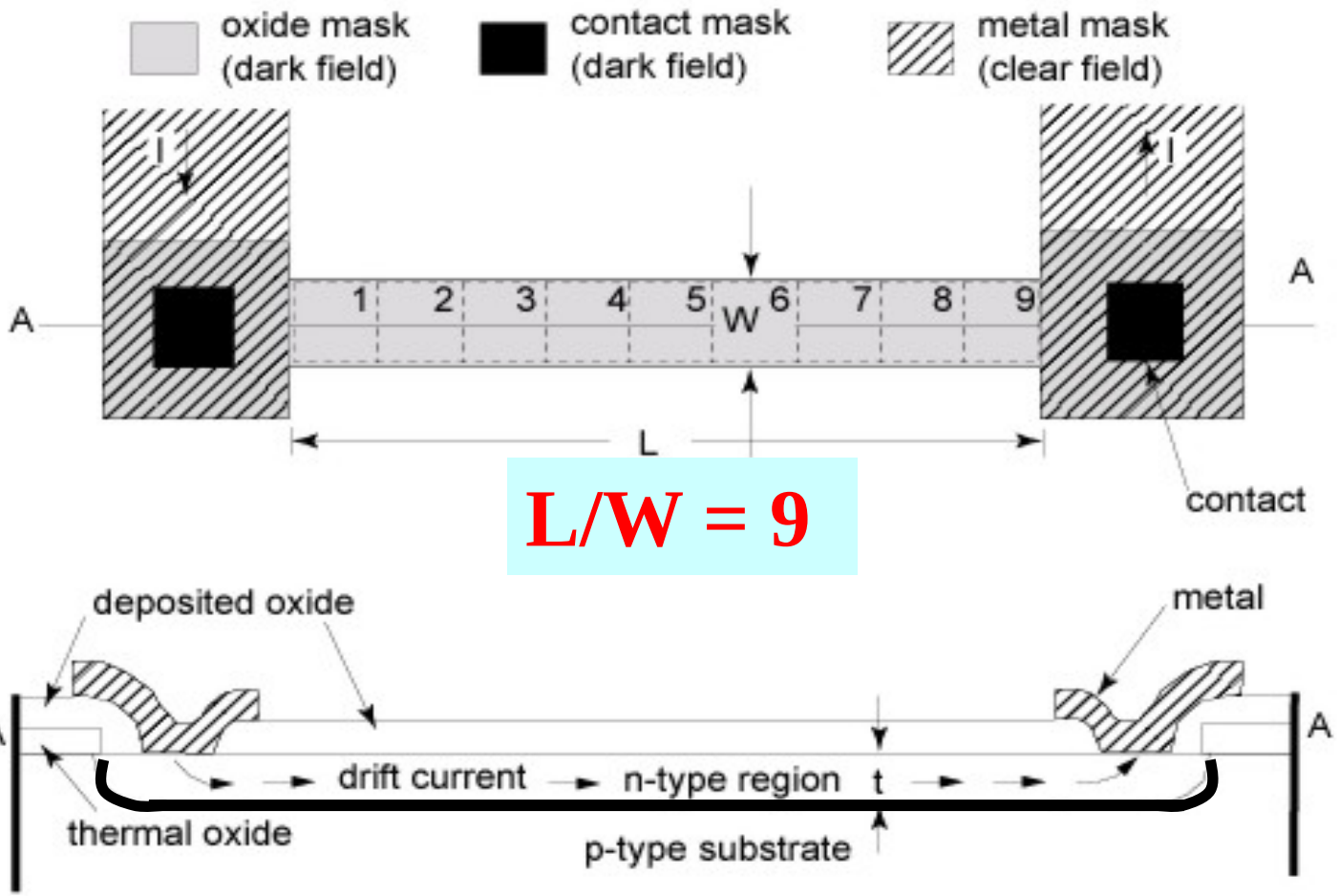
Process

Mask

**Sheet Resistivity** ($R_S$) Ω/sq
or **Sheet Resistance**

# Using Sheet Resistance (**Rs**)

- **Ion-implanted (or "diffused") IC resistor**



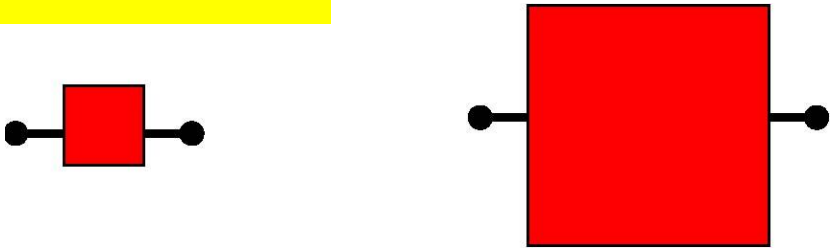
# Concept of Sheet Resistivity

$$R = \rho L/A = (\rho/t)\,(L/W)$$

**Sheet Resistivity** ($R_S$) Ω/sq
or **Sheet Resistance**

# of Squares

$$R = Rs\,(L/W)$$

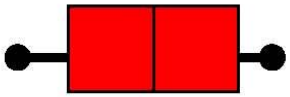


If L = W,

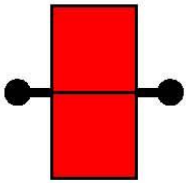
$R = R_s$

# Number of Squares

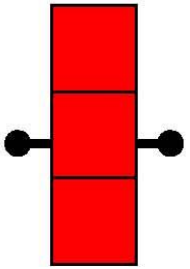
$R = R_S (L/W)$



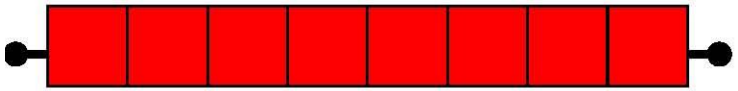
$R = 2R_S$



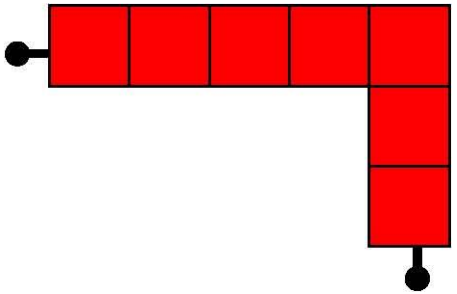
$R = R_S/2$



$R = R_S/3$

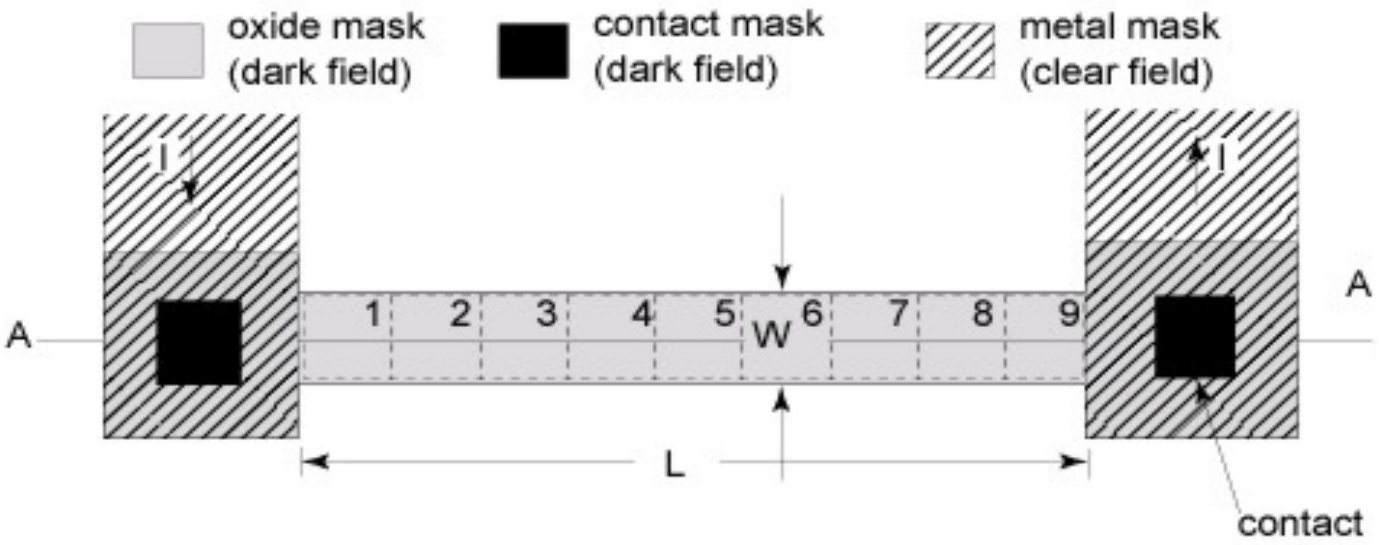


$R = 8R_S$



$R \approx 6.5R_S$

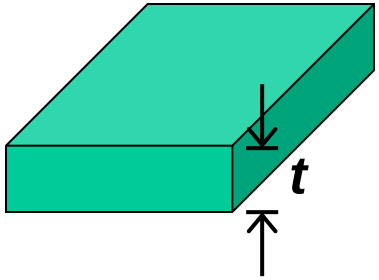
# Using Sheet Resistance (**Rs**)




$$R = \left(\frac{\rho}{t}\right)\left(\frac{L}{W}\right) = R_S \frac{L}{W} \approx 9R_S$$

# Integrated-Circuit Resistors

The resistivity $\rho$ and thickness ***t*** are fixed for each layer in a given manufacturing process




A circuit designer specifies the length ***L*** and width ***W***, to achieve a desired resistance ***R***

$$R = R_s\left(\frac{L}{W}\right)$$

fixed designable

Example: Suppose we want to design a 5 kΩ resistor using a layer of material with $R_s$ = 200 Ω/□

**Resistor layout (top view)**

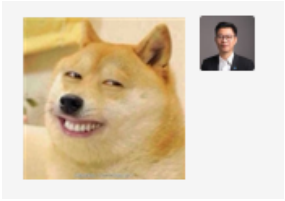
$W/L = 25$

**Space-efficient layout**

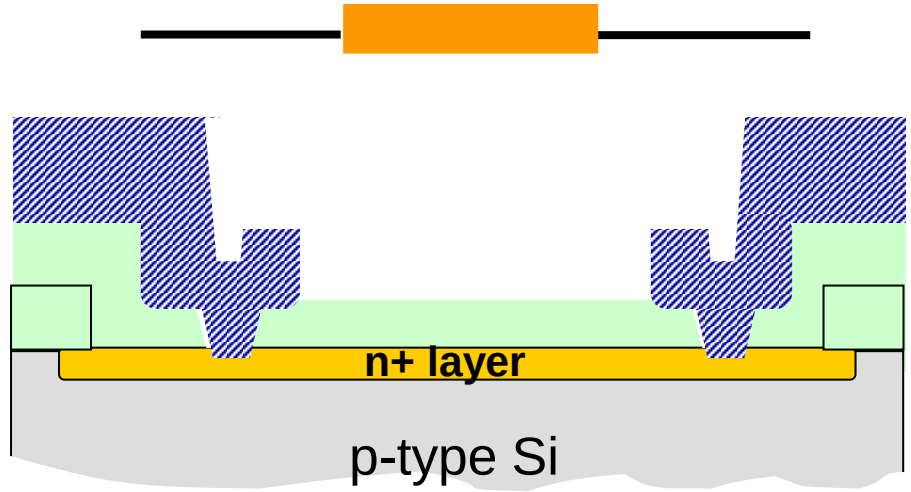
# IC Fabrication Techniques

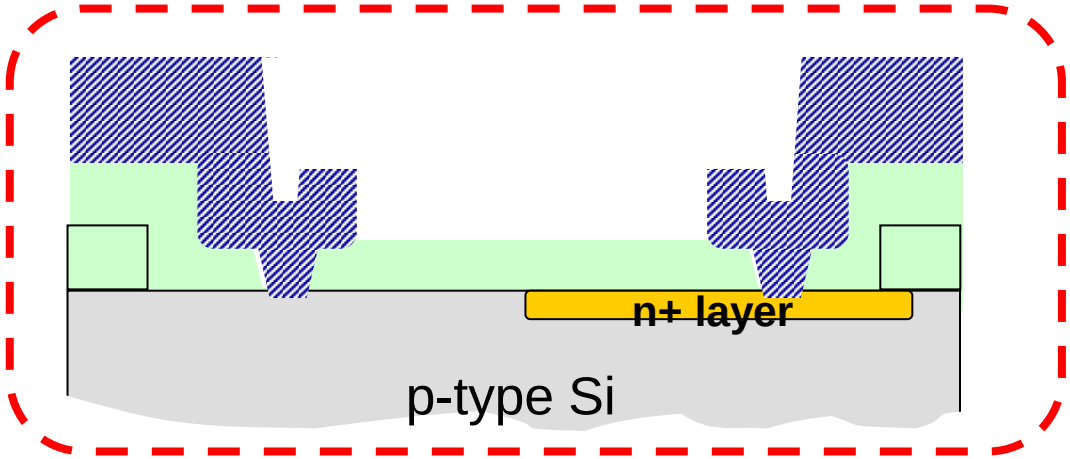
## OUTLINE

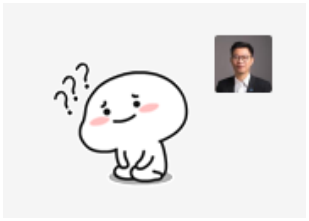
- IC Resistor
- Sheet Resistance
- **Diode** ⟵



# Process Flow Example #1: Resistor

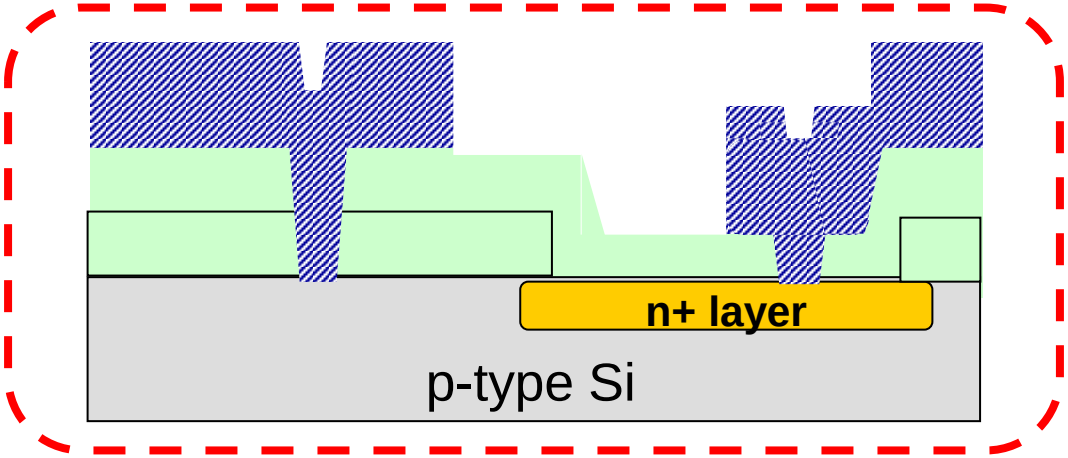


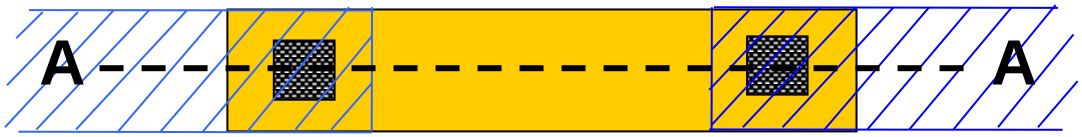



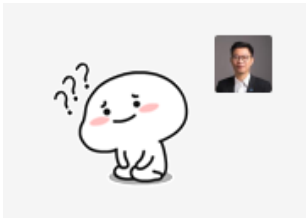



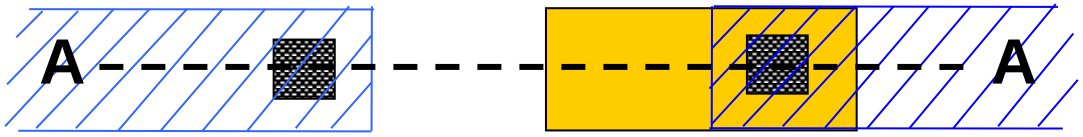
# Process Flow Example #2: diode

A -- A






Oxide mask (dark field)

Contact mask (dark field)

Al mask (clear field)

# Process Flow Example #1: Diode

**Three-mask process:**

**Starting material: p-type wafer with $N_A = 10^{16}$ cm$^{-3}$**

**Step 1:** grow 500 nm of $SiO_2$

**Step 2:** pattern oxide using the oxide mask (dark field)

**Step 3:** implant phosphorus and anneal to form an n-type layer with $N_D = 10^{20}$ cm$^{-3}$ and depth 100 nm

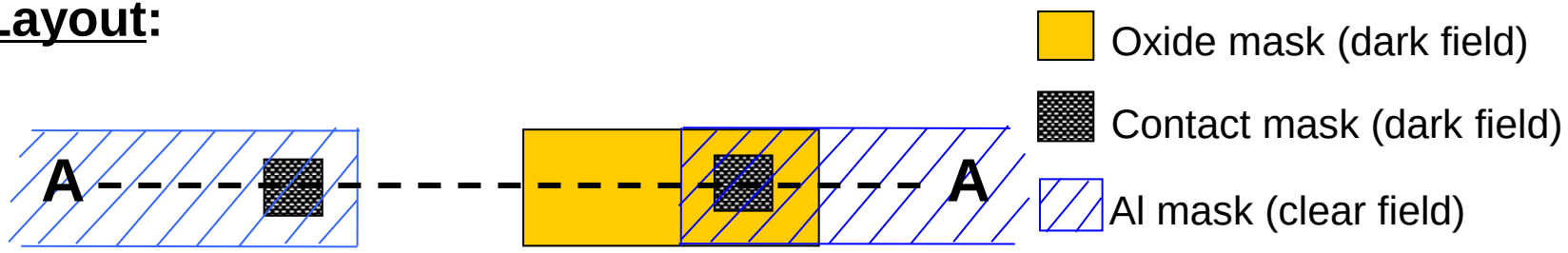
**Step 4:** deposit oxide to a thickness of 500 nm

**Step 5:** pattern deposited oxide using the contact mask (dark field)

**Step 6:** deposit aluminum to a thickness of 1 μm

**Step 7:** pattern using the aluminum mask (clear field)

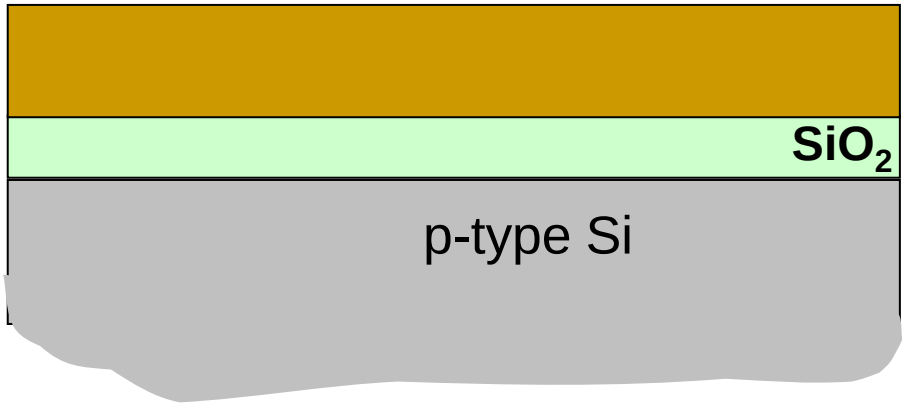
**Layout:**



# A-A Cross-Section: oxidation, photolithography & etching

**Step 1:**

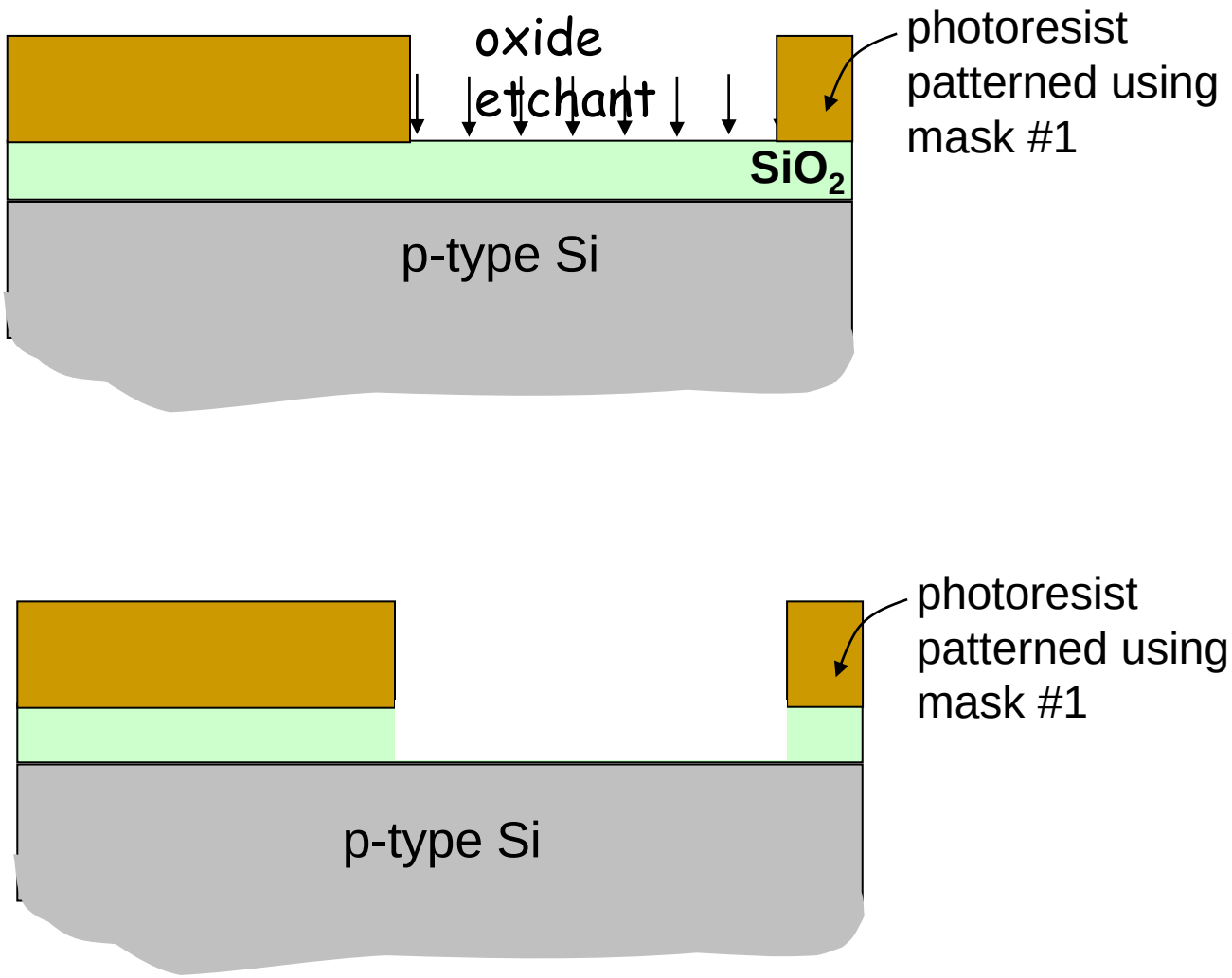
**Grow oxide**



# A-A Cross-Section: oxidation, photolithography & etching

**Step 2:**

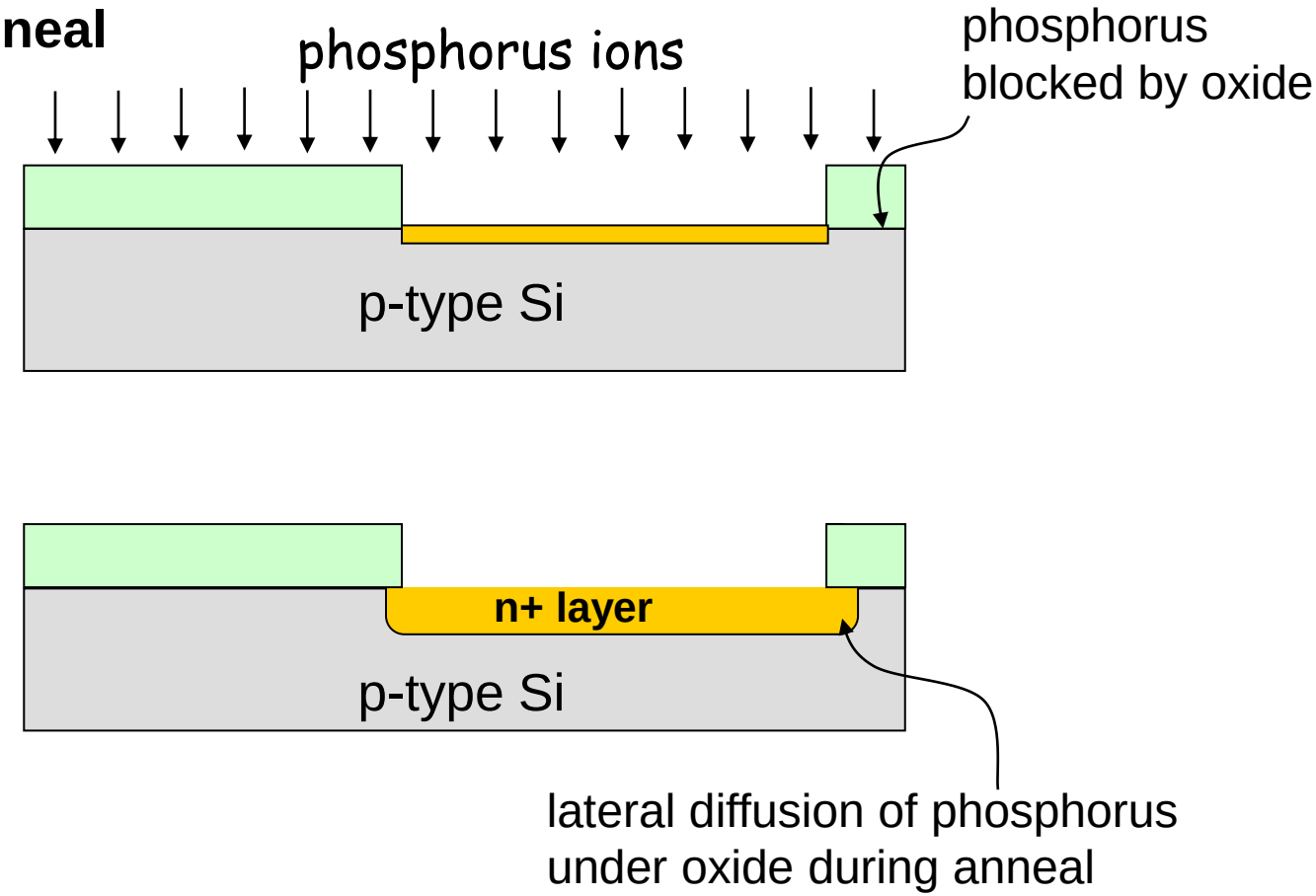
**Pattern oxide (active mask)**



# A-A Cross-Section: doping & annealing

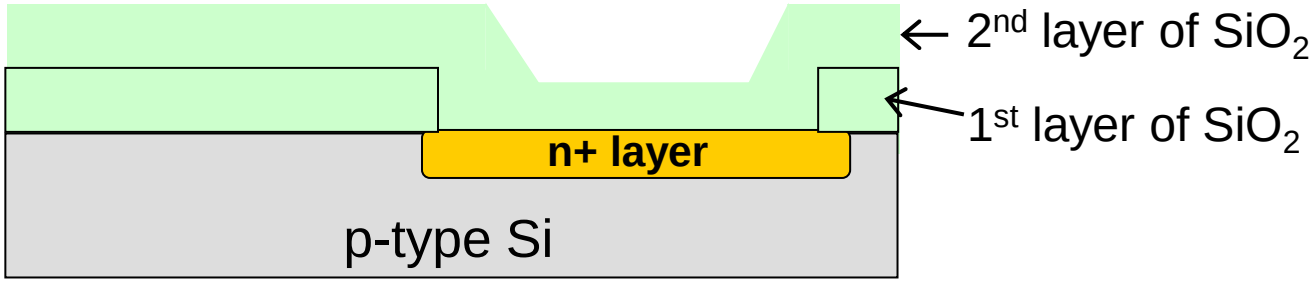
**Step 3: Implant & Anneal**

phosphorus implant:



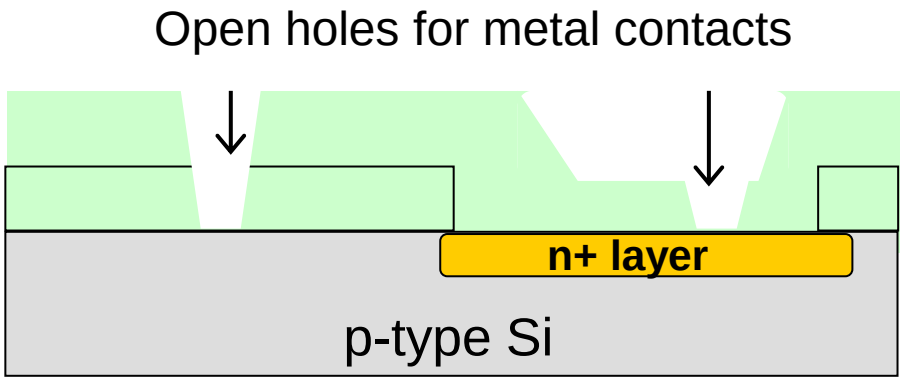
# A-A Cross-Section: Metal contact

**Step 4: Deposit 500 nm oxide**




**Step 5:**

**Pattern oxide (contact mask)**



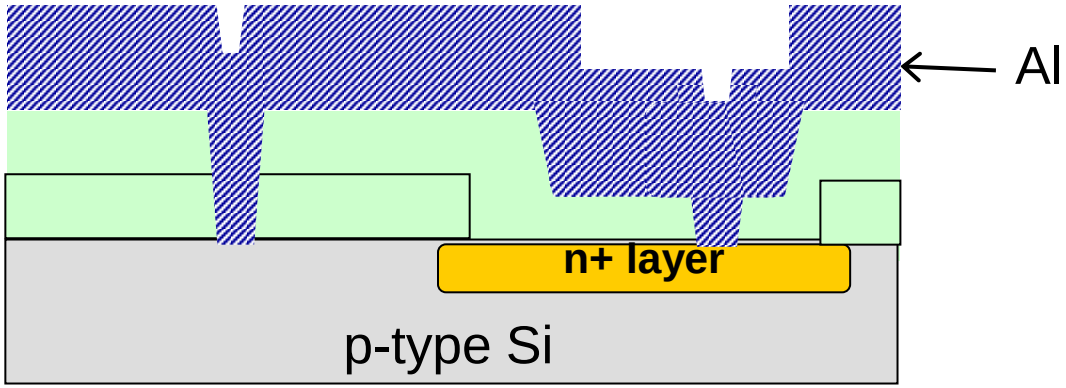

**deposition, photolithography & etching**

# A-A Cross-Section: metallization

## deposition, photolithography & etching

**Step 6:**

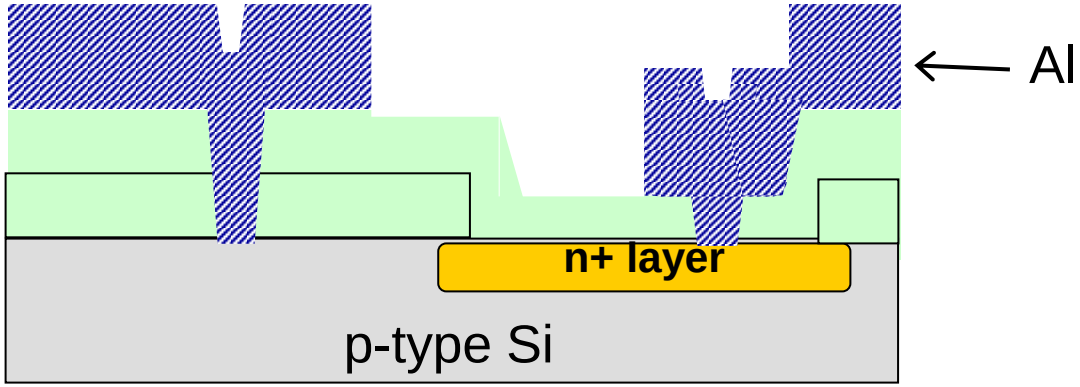
**Al deposition**




**Step 7:**

**Pattern metal**

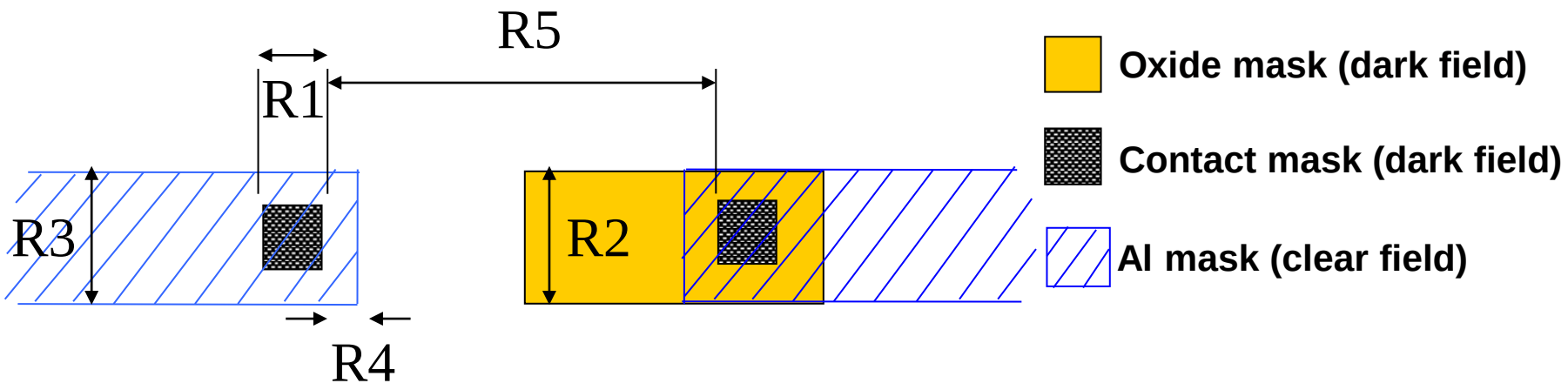
**(Metal mask)**



# Example of Design Rule: MOSIS

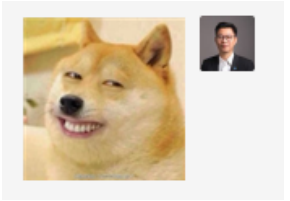
- R1: the minimum feature size is 2λ,
- R2: the minimum active area width is 3λ,
- R3: the minimum metal width is 3λ,
- R4: the safety margin for overlay error is λ,
- R5: the minimum active contact spacing on different active regions is 6λ.

**Layout:**

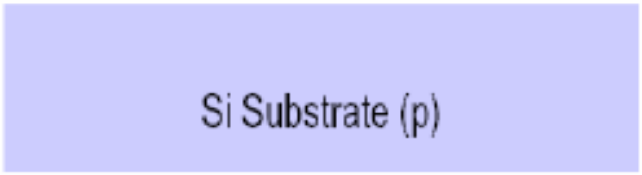


# IC Fabrication Techniques

- **nMOSFET: Process Flow**
- **nMOSFET: Layout Rule**

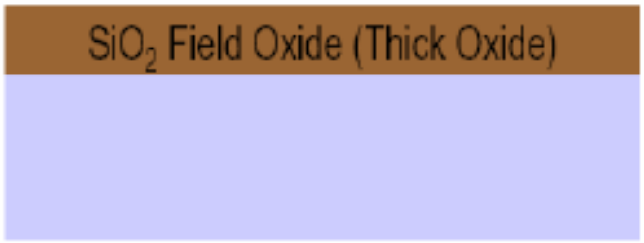


# Process Flow: nMOSFET

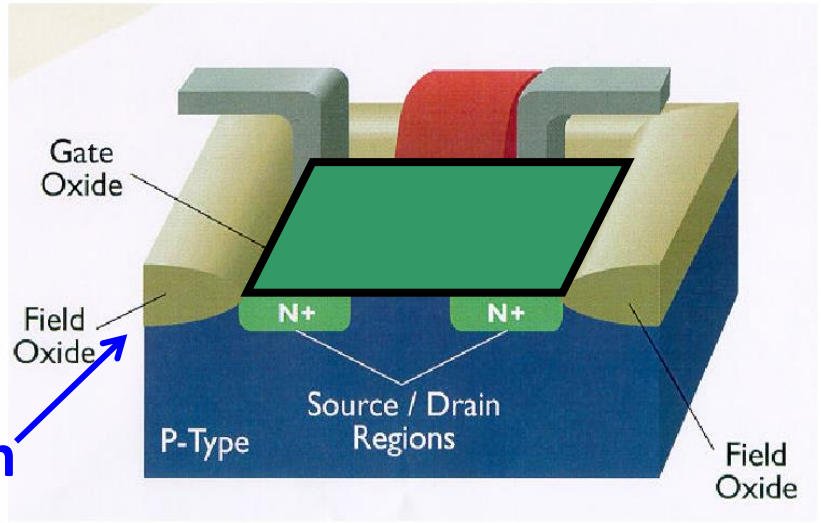



Oxidation (Layering)

**Oxide 1**




**~ 500nm**



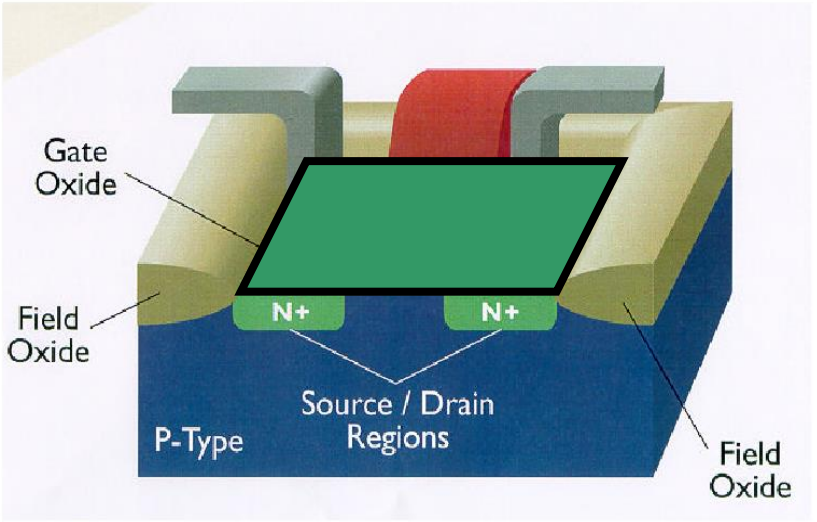

**Mask 1**

Oxide etching (Patterning)

**Mask 1: Active region**

# Process Flow: nMOSFET

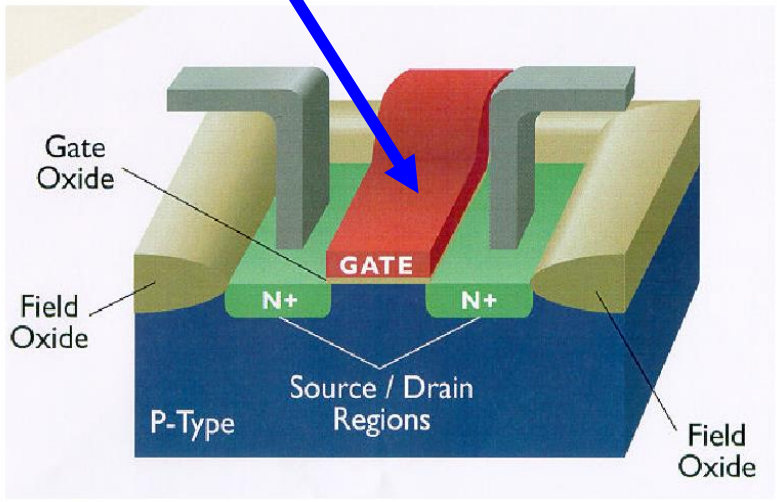
- The cleaned Si slice is **oxidized** (**oxide1**)
- A **window** is opened in the oxide (**mask1**).
- The sides of the mask 1 must be equal in size to a multiple of the minimum feature size (design rules).

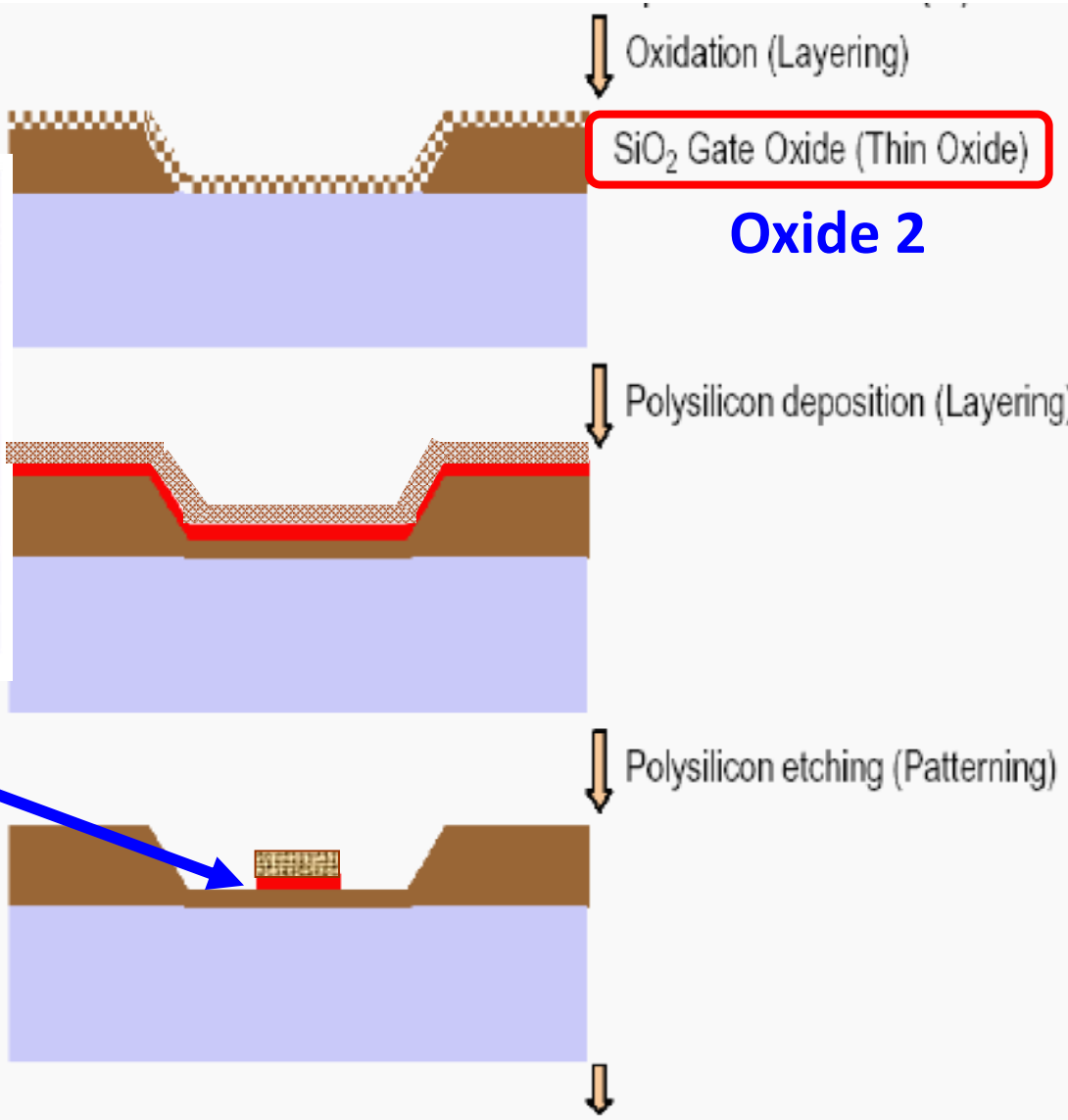



**Mask 1: Active region**

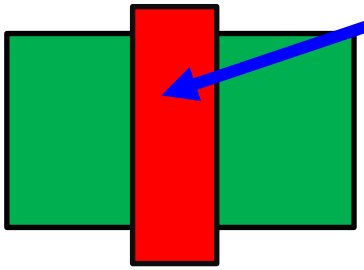
# Process Flow: nMOSFET

**Mask 2: Gate**

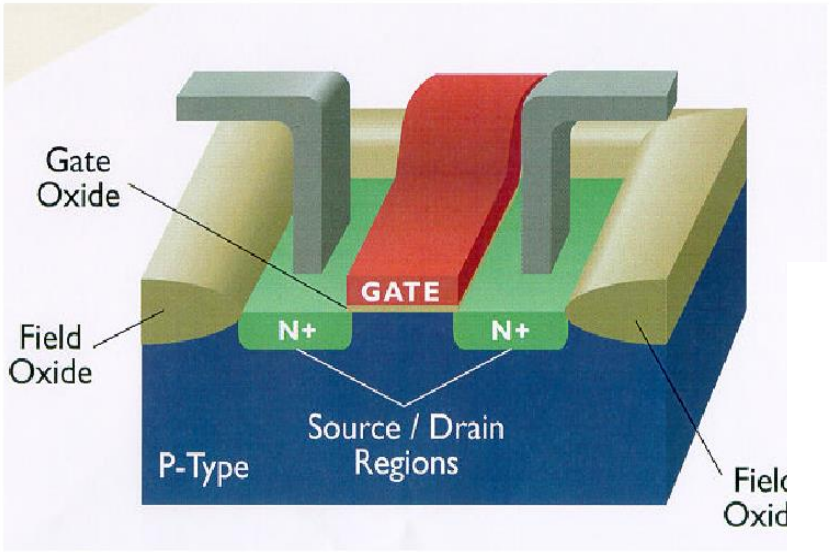


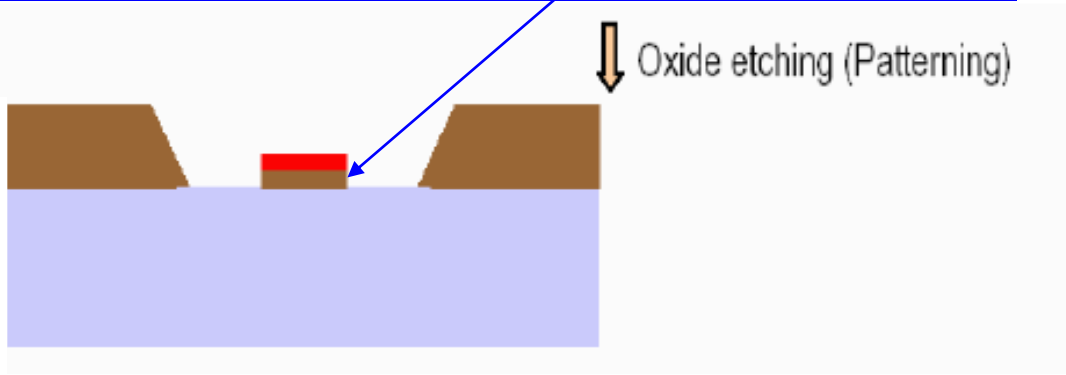

**Mask 2**



# Process Flow: nMOSFET

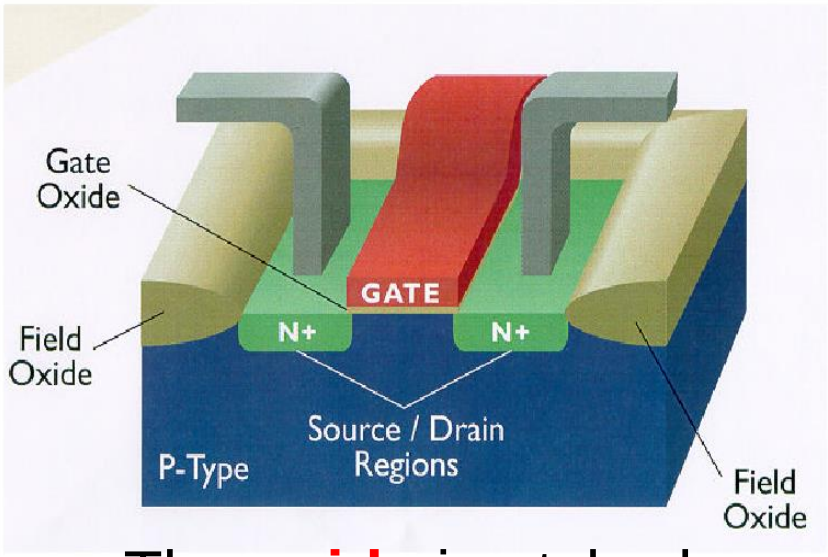



**Oxide** and **polysilicon** are **photoengraved** in the shape of the gate stripe after mask (**mask2**) for the **etching** of **polysilicon** gate electrode.

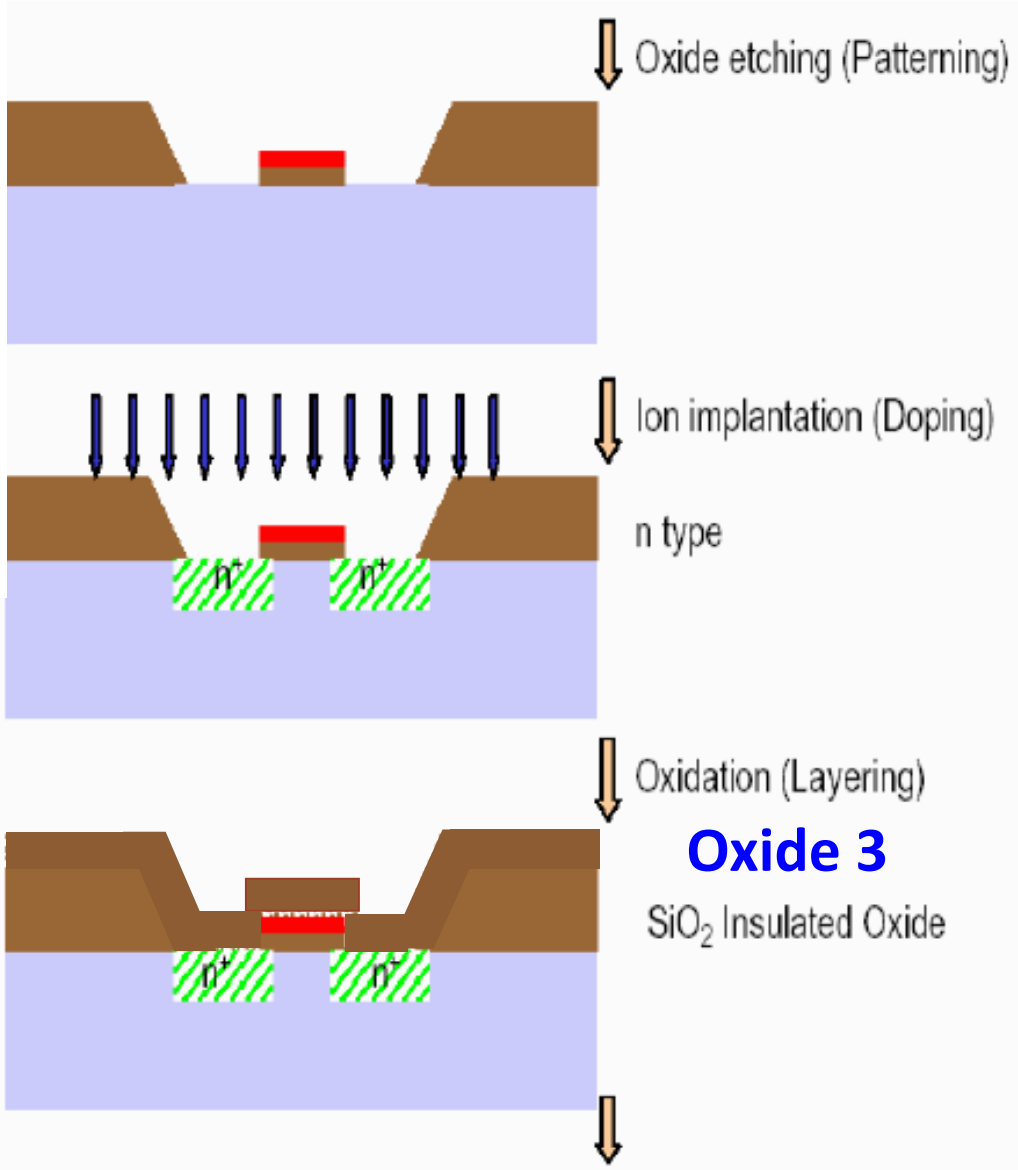



- The slice of silicon is **re-oxidized** (**oxide2**).
- It fills the window with **new thinner oxide**.
- **polysilicon** covers the entire surface.

# Process Flow: nMOSFET

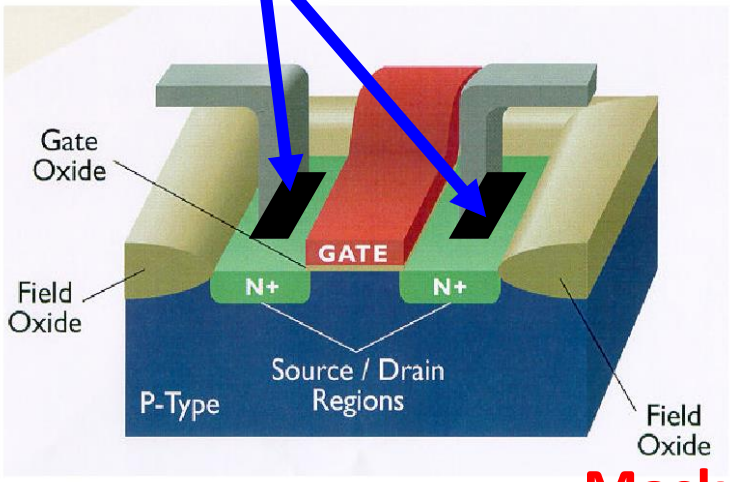


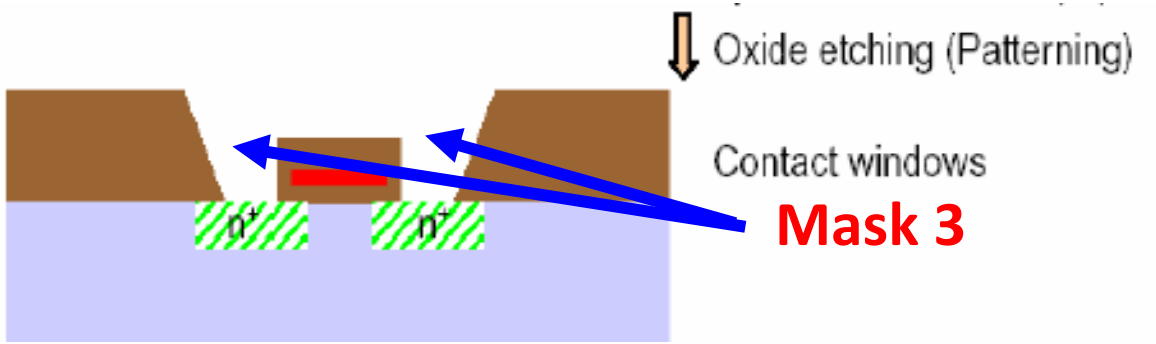

- The **oxide** is etched from the **source** and **drain** regions.
- The **implant** creates the **source** and **drain** regions and dopes the polysilicon to make it very conducting.



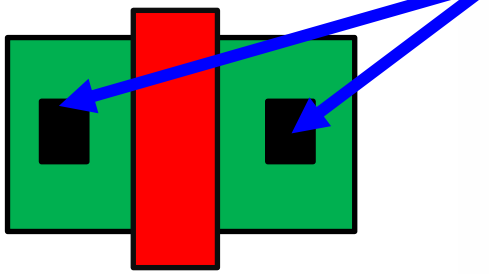
# Process Flow: nMOSFET

**Mask 3: contacts**



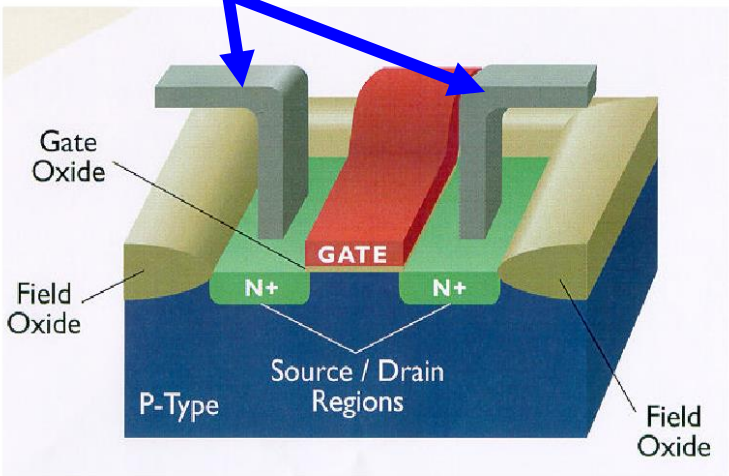

**Mask 3**



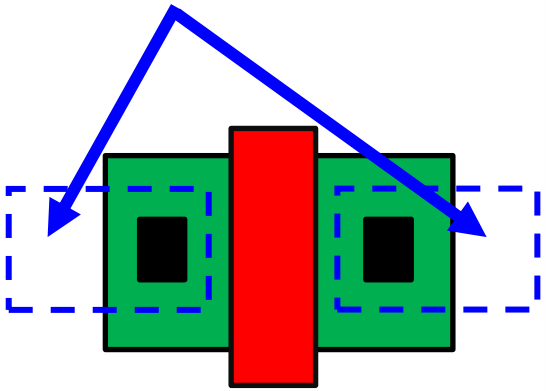
- **Oxide** is **deposited** on the surface (**oxide 3**)
- The **contact** or **via holes** are **opened** (**mask 3**).
- Each of these holes must have **dimensions** that are equal to the **minimum feature size**.

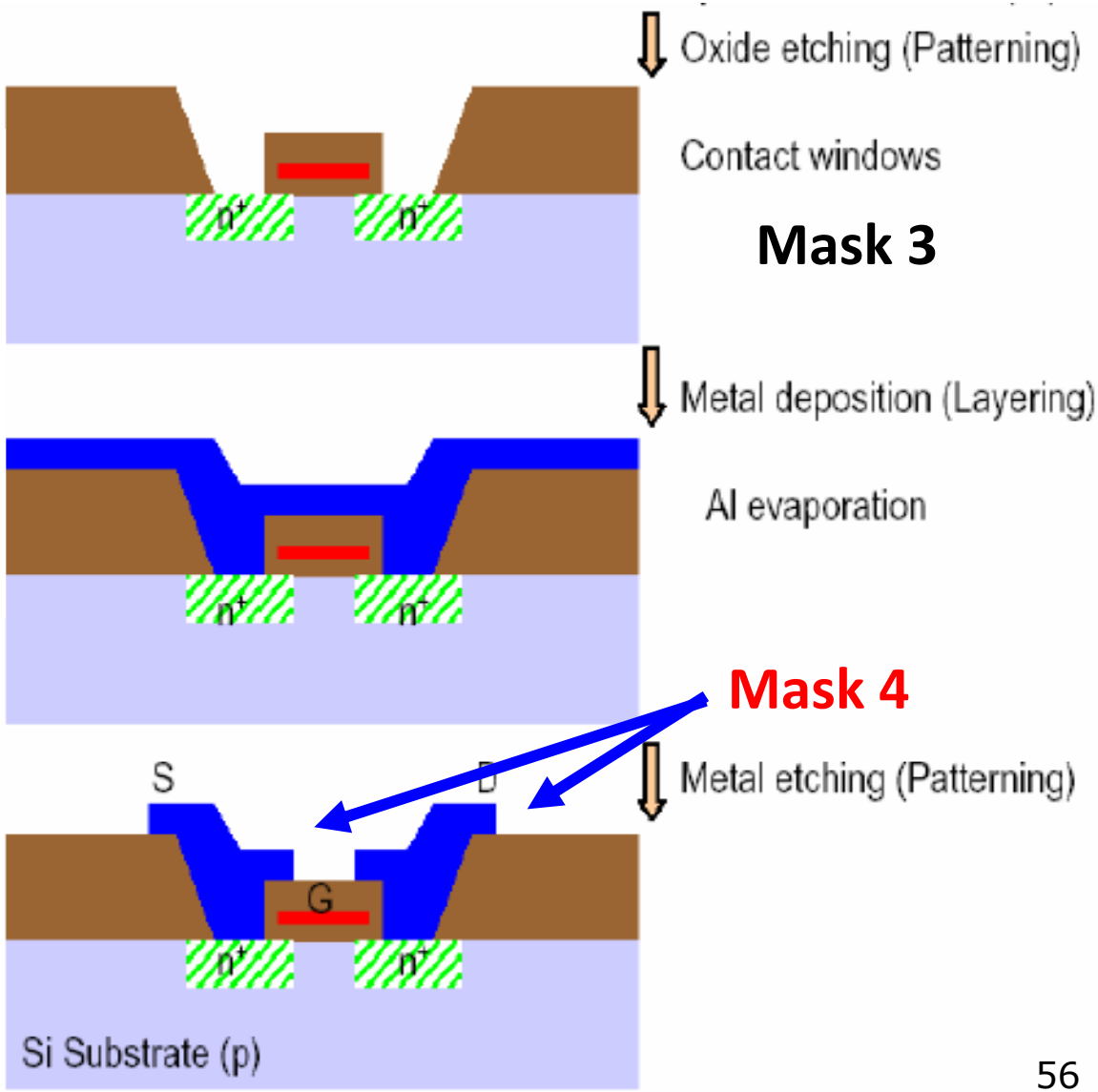
# Process Flow: nMOSFET

**Mask 4: metal**



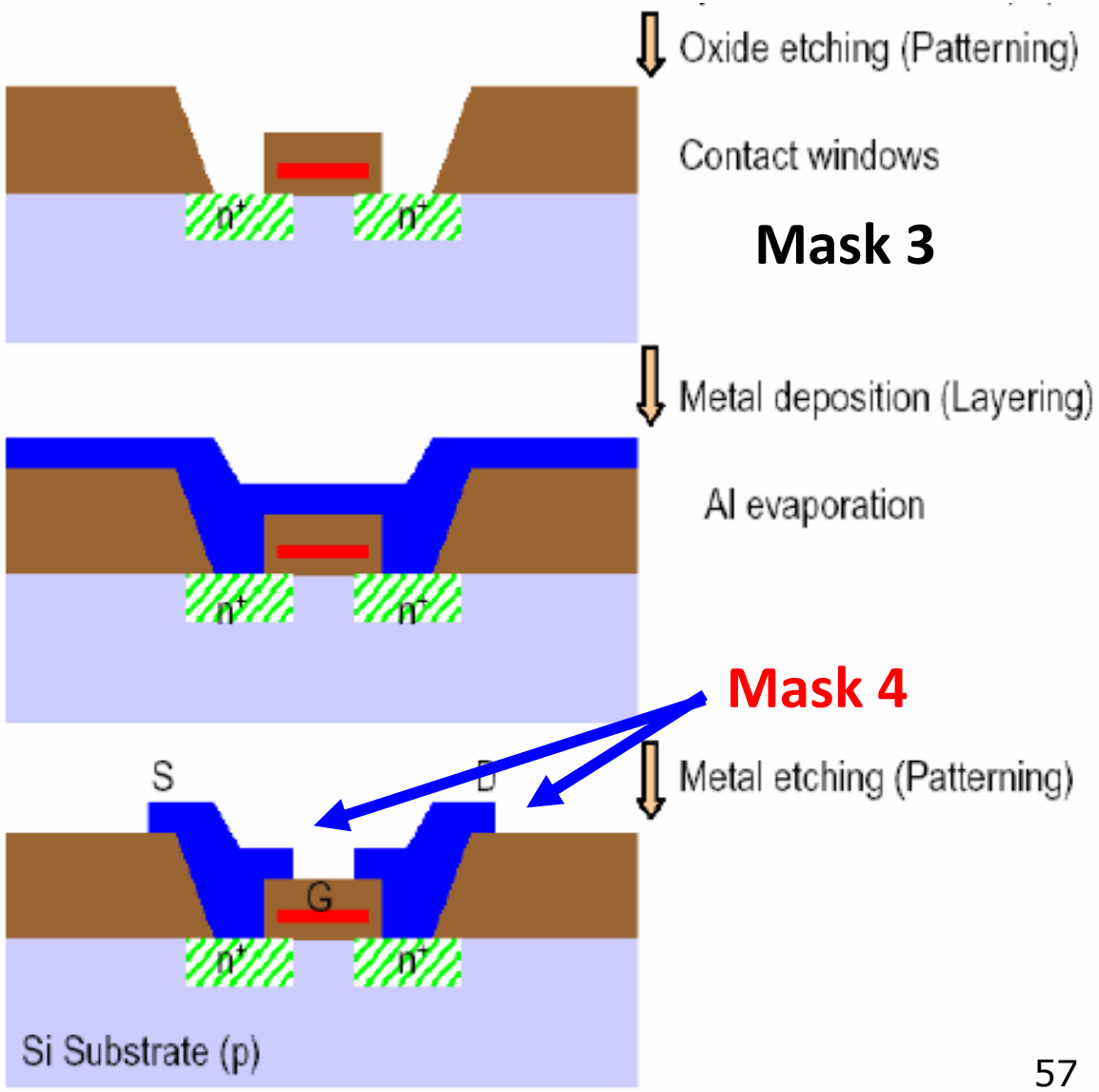

**Mask 4: metal**





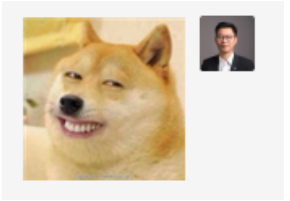
# Process Flow: nMOSFET

- **Al** is **evaporated** to cover the whole slice and is then covered with photoresist.
- **Al** is **patterned** into the shape of the conductor patterns across the chip (**mask 4**). It makes contact to the **source** and **drain** down the contact holes.
- The width of the **Al** stripes must **cover** the **contact holes** with an allowance on either side of an amount equal to the minimum alignment accuracy.

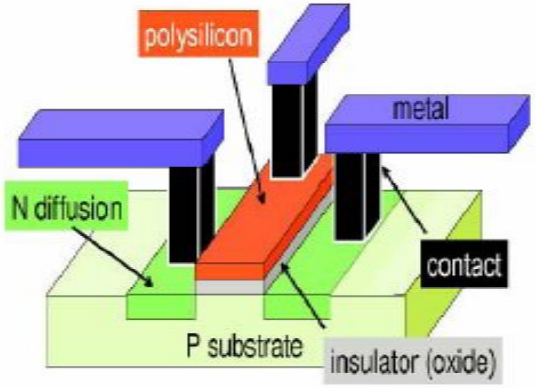


# IC Fabrication Techniques

- nMOSFET: Process Flow
- nMOSFET: Layout Rule

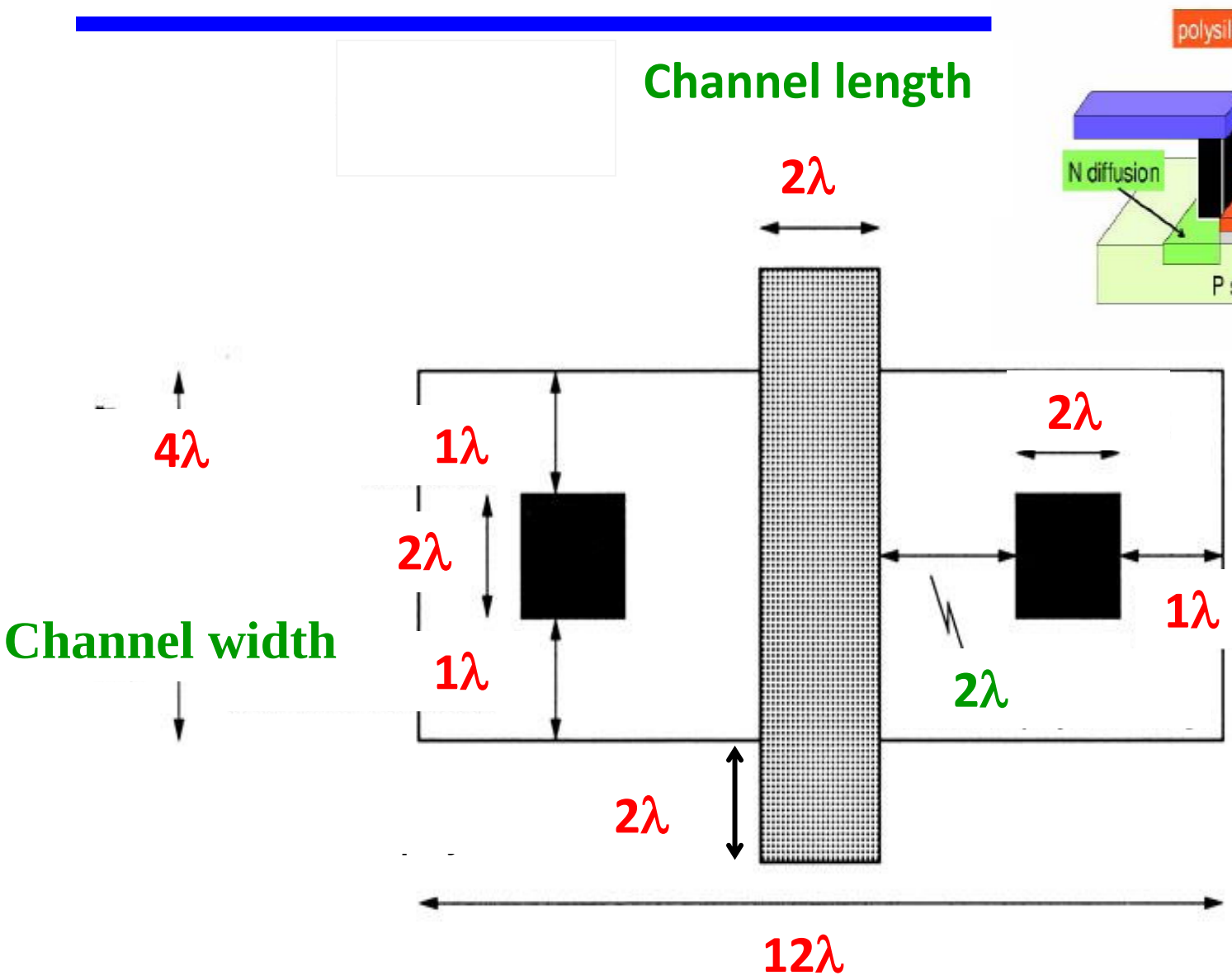


# Layout rules to minimise MOST size




Channel length

Channel width

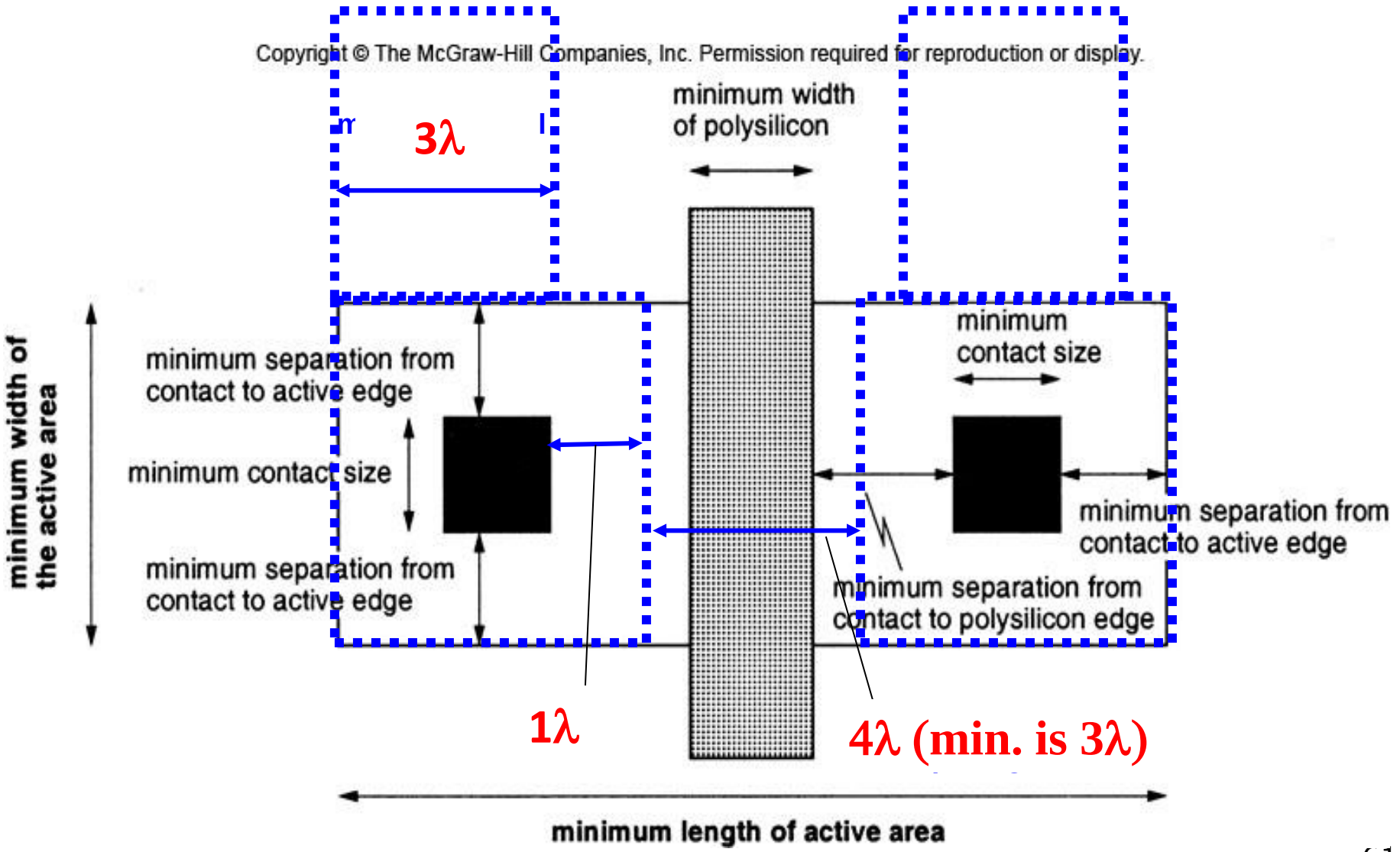


## MOSIS Layout Design Rules (sample set)

| *Rule number* | *Description* | *λ-Rule* |
|---|---|---|
| | **Active area rules** | |
| R1 | Minimum active area width | 3λ |
| R2 | Minimum active area spacing | 3λ |
| | **Polysilicon rules** | |
| R3 | Minimum poly width | 2λ |
| R4 | Minimum poly spacing | 2λ |
| R5 | Minimum gate extension of poly over active | 2λ |
| R6 | Minimum poly-active edge spacing (poly outside active area) | 1λ |
| R7 | Minimum poly-active edge spacing (poly inside active area) | 3λ |
| | **Metal rules** | |
| R8 | Minimum metal width | 3λ |
| R9 | Minimum metal spacing | 3λ |
| | **Contact rules** | |
| R10 | Poly contact size | 2λ |
| R11 | Minimum poly contact spacing | 2λ |
| R12 | Minimum poly contact to poly edge spacing | 1λ |
| R13 | Minimum poly contact to metal edge spacing | 1λ |
| R14 | Minimum poly contact to active edge spacing | 3λ |
| R15 | Active contact size | 2λ |
| R16 | Minimum active contact spacing (on the same active region) | 2λ |
| R17 | Minimum active contact to active edge spacing | 1λ |
| R18 | Minimum active contact to metal edge spacing | 1λ |
| R19 | Minimum active contact to poly edge spacing | 3λ |
| R20 | Minimum active contact spacing (on different active regions) | 6λ |

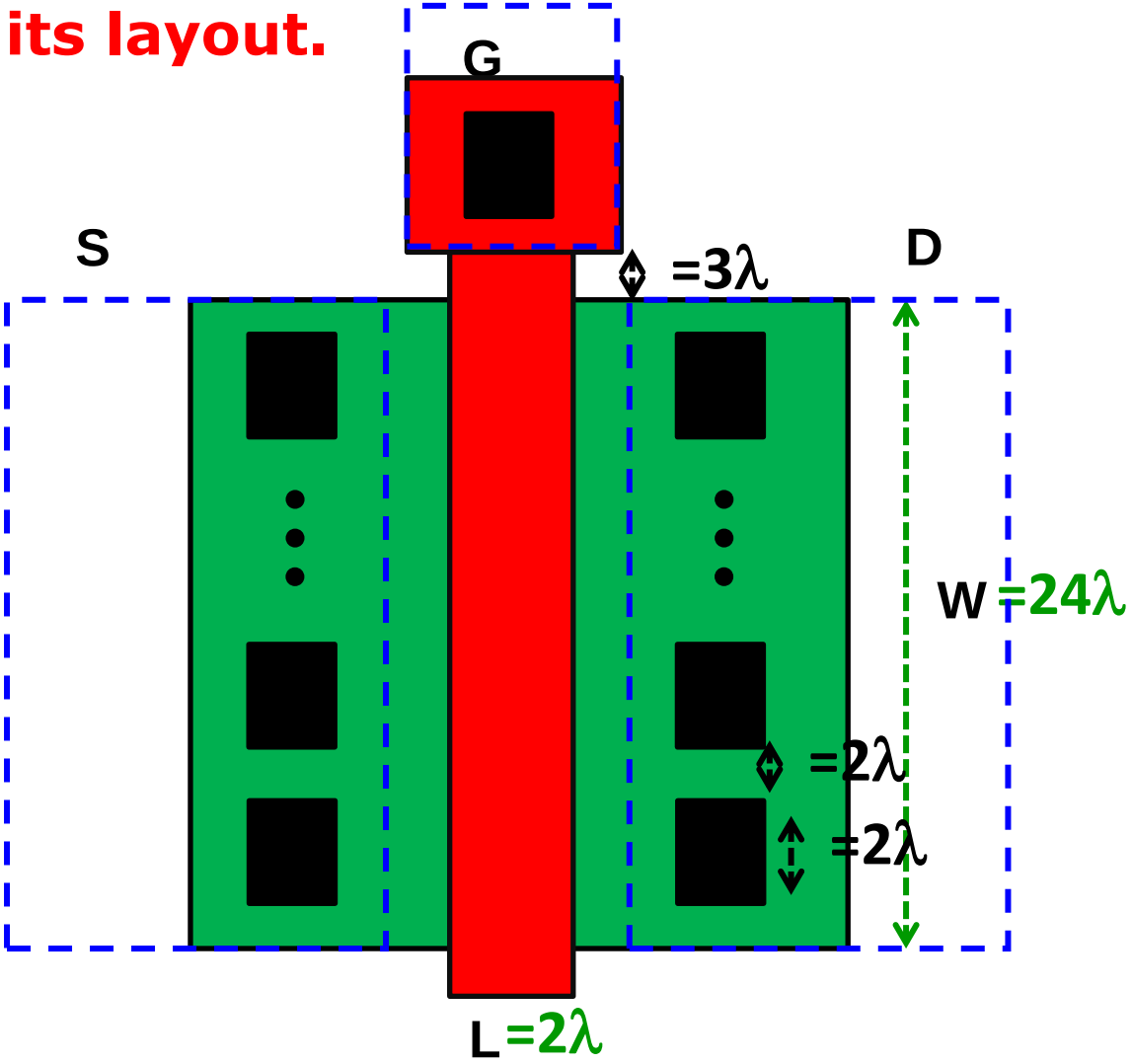
MOSIS layout design rules

# Layout rules to minimise MOST size



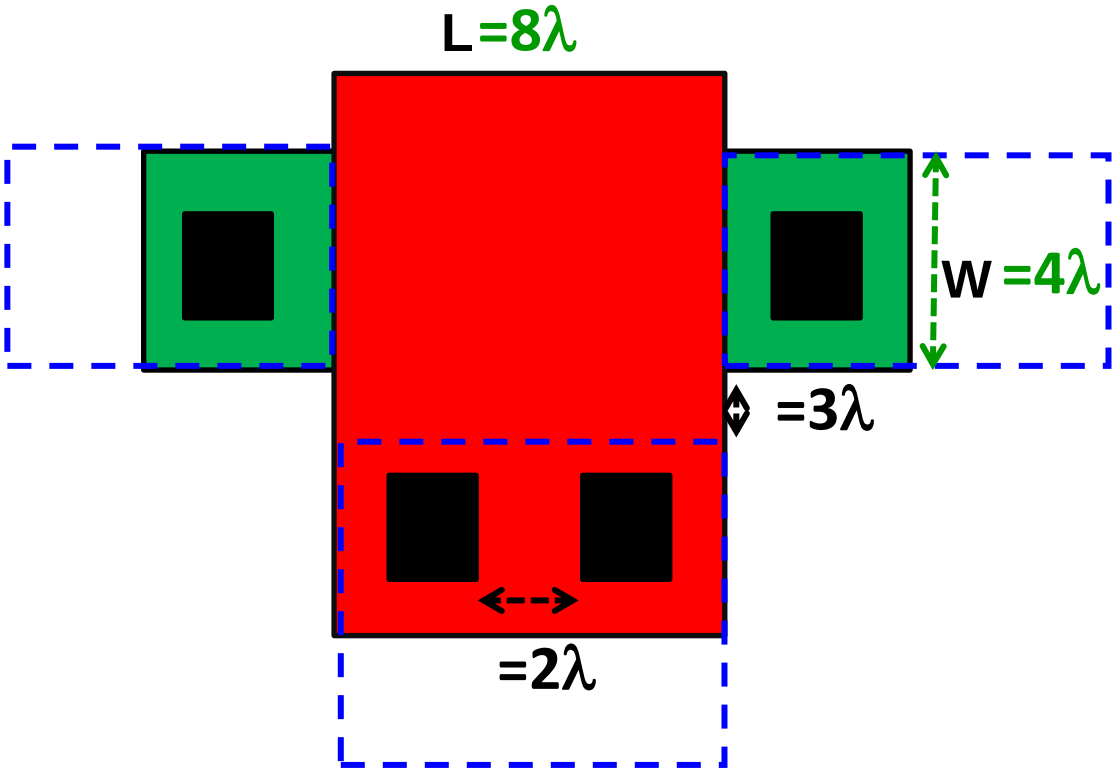
# The Design of a MOSFET

**Example: if we need a MOSFET with W/L = 12, design its layout.**

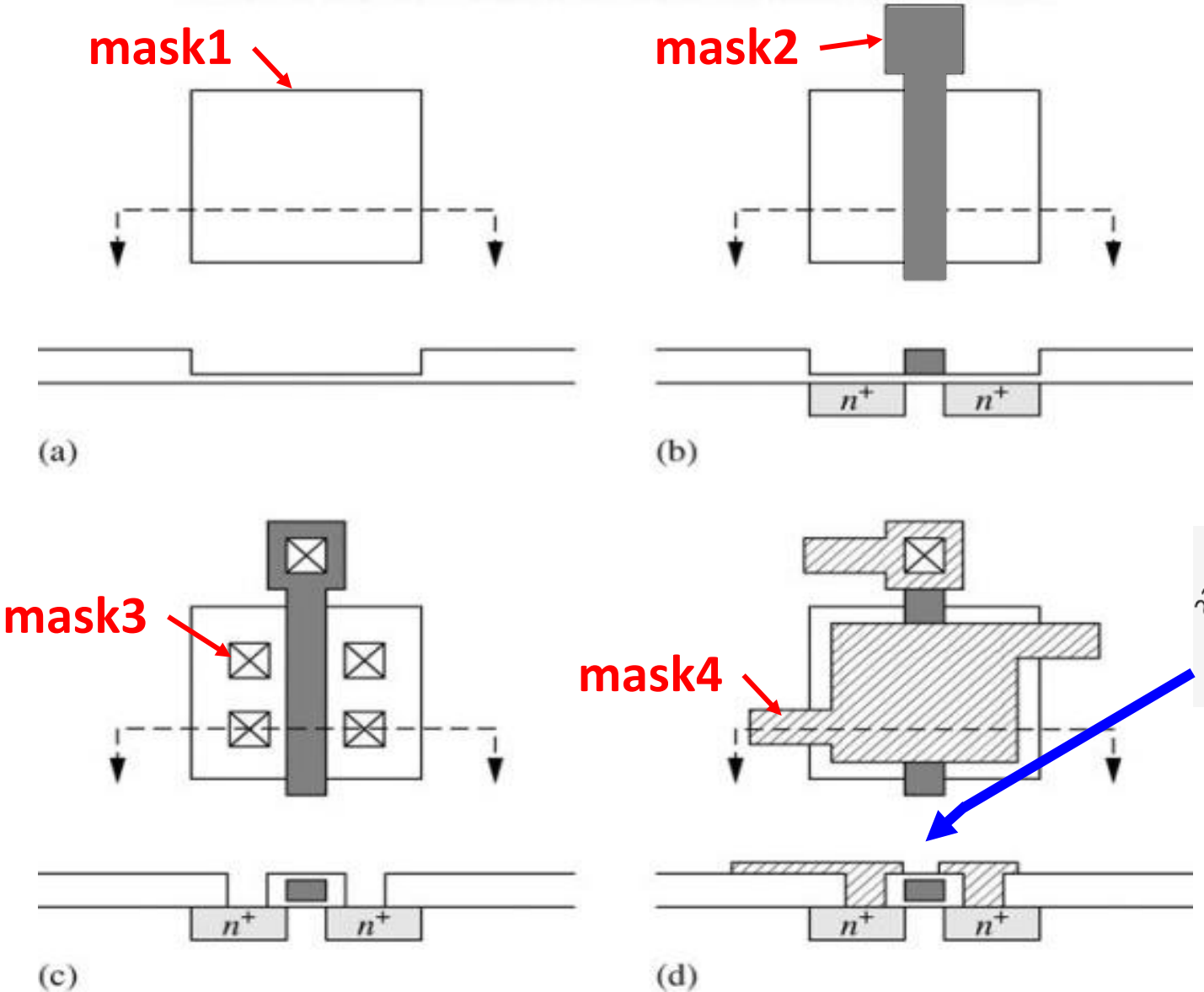


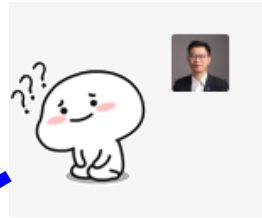
# The Design of a MOSFET

**Example: if we need a MOSFET with W/L = 0.5, design its layout.**

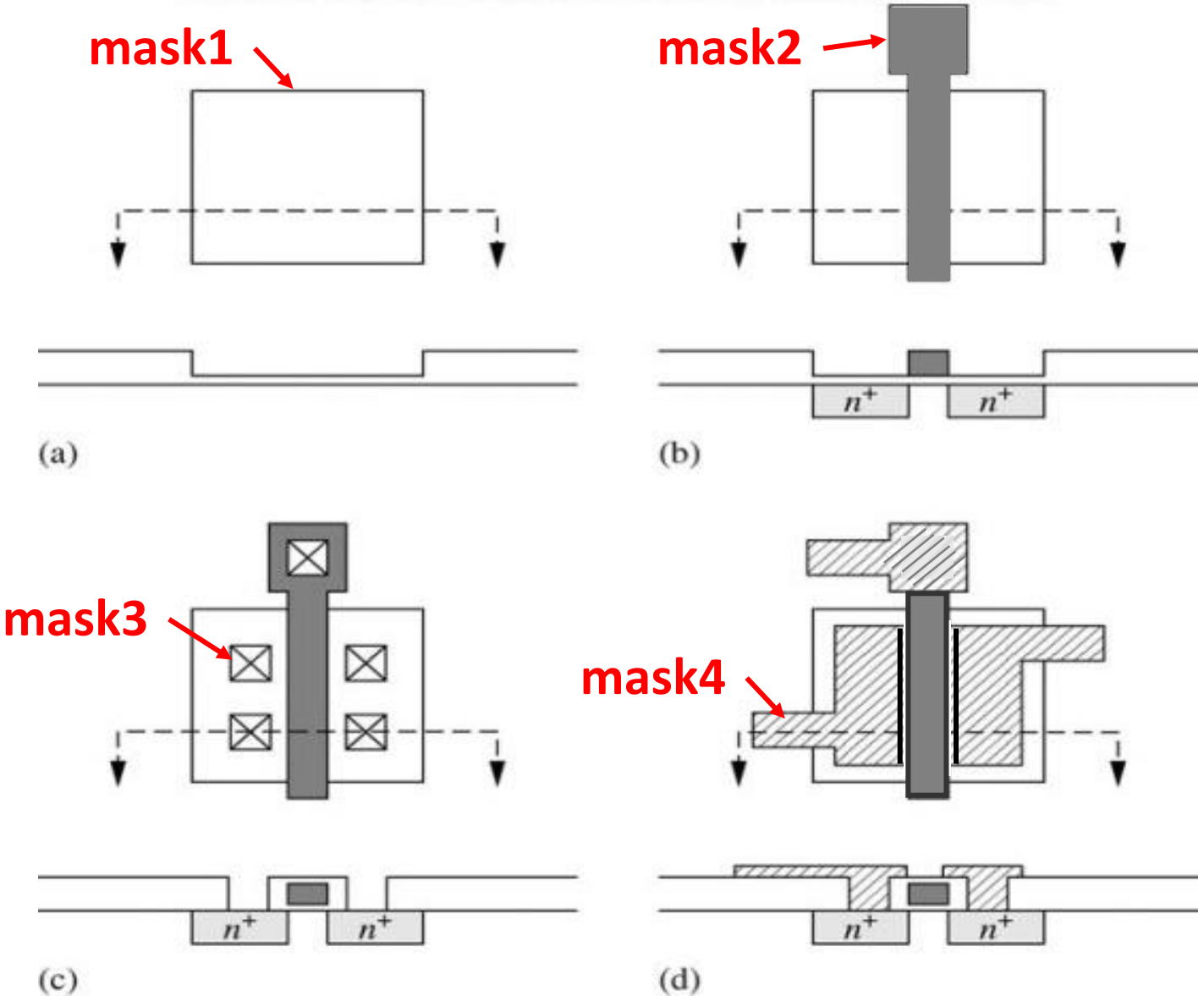


# Mask Sequence for a Polysilicon-Gate Transistor

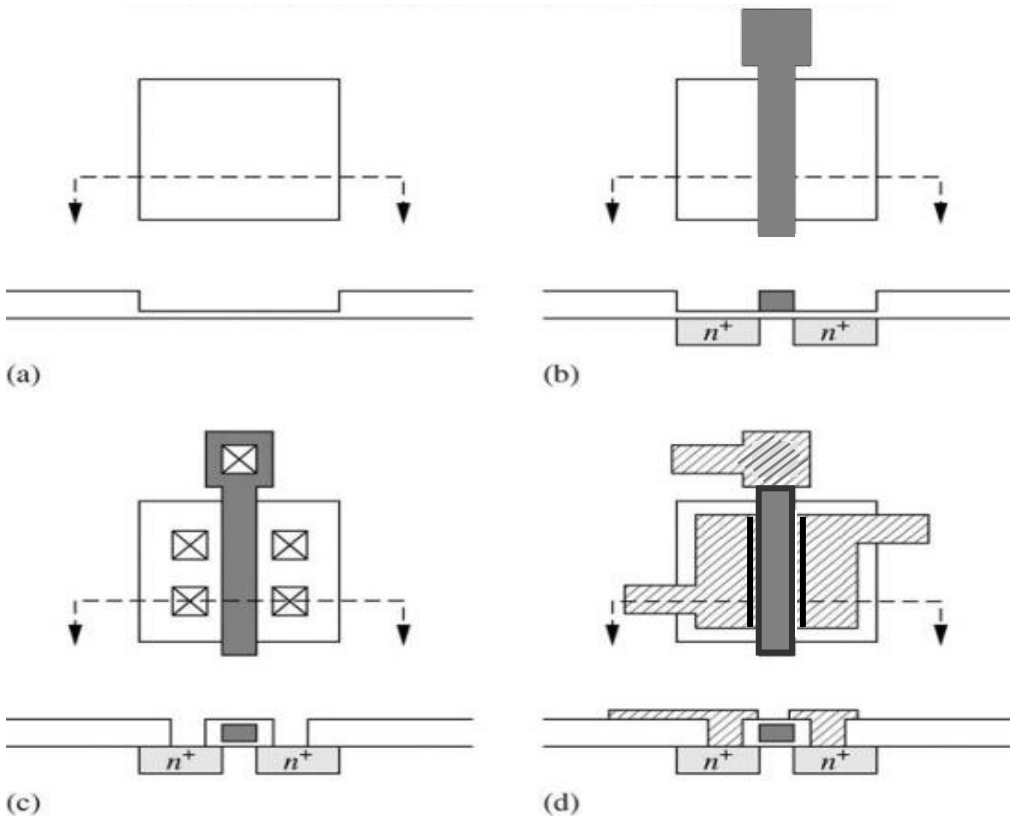


# Mask Sequence for a Polysilicon-Gate Transistor



# Mask Sequence for a Polysilicon-Gate Transistor




- **Mask 1**: Defines **active area** or thin oxide region of transistor
- **Mask 2**: Defines **polysilicon gate** of transistor, **aligns to mask 1**
- **Mask 3**: Delineates the **contact window**, **aligns to mask 2 & 1.**
- **Mask 4**: Delineates the **metal pattern**, **aligns to mask 3.**

Channel region of transistor formed by intersection of first two mask layers. Source and Drain regions formed wherever mask 1 is not covered by mask 2