Xi'an Jiaotong-Liverpool University
西交利物浦大学

EEE109: The Field-Effect Transistor

Chapter 3

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- Study and understand the structure and operation of the various types of MOSFETs.
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  - P-channel MOSFET
- Understand the DC analysis and design techniques of MOSFET circuits.
  - Put the MOSFET into a specific DC circuit and calculate the electrical parameter

MOS FIELD-EFFECT TRANSISTOR

Understand the operation and characteristics of the various types of metal-oxide semiconductor field-effect transistors (MOSFETs).

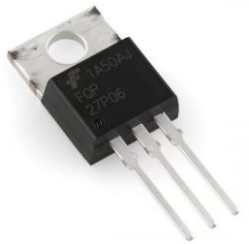
MOSFET

- **M**etal-**O**xide-**S**emiconductor **F**ield-**E**ffect-**T**ransistor (MOSFET,金属氧化物半导体场效应晶体管)

- Compare to another transistor (BJT in Chapter 4), MOSFET can be made very small. MOSFET is widely used in integrated circuit (IC).

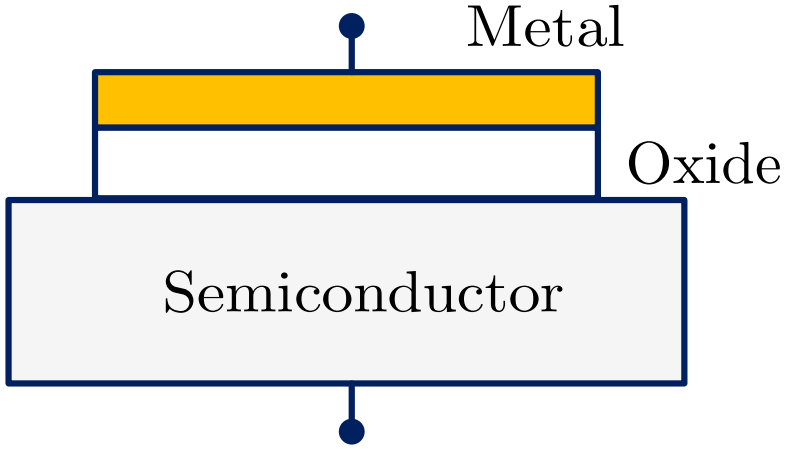
- In the MOSFET, the current is controlled by an electric field applied perpendicular to both the semiconductor surface and to the direction of current. This phenomenon is called 「**Field-Effect**」.

MOSFET ⇒ Voltage controlled device (电压控制型器件)



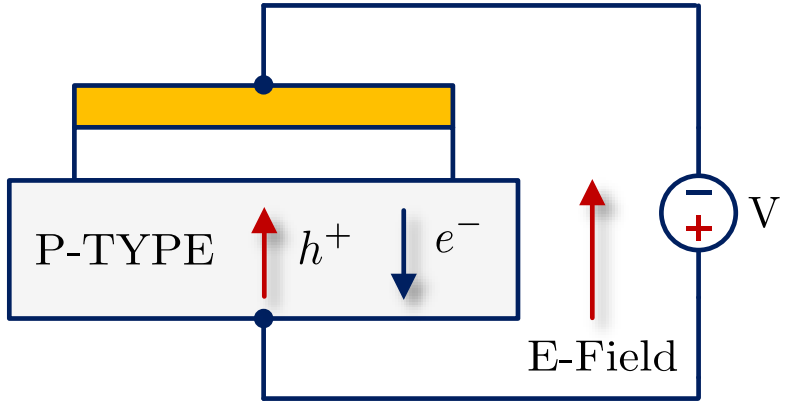
Two-Terminals MOS Structure

- The heart of the MOSFET is the metal-oxide-semiconductor capacitor. It is a classic sandwich or hamburger structure.
- Metal could be aluminum or some other type of metal
- Oxide (氧化物) is a very good type of insulator
- Semiconductor, including P-type and N-type

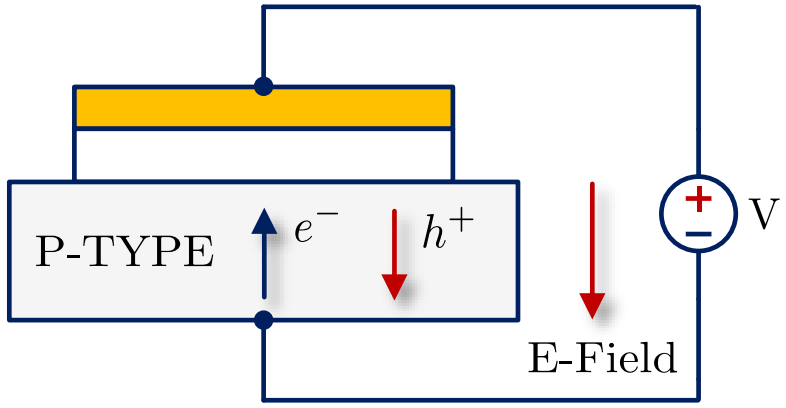


Two-Terminals MOS (P-Type)

- E-field direction: point from bottom to the top
- Hole is moving toward the top interface, and electron is moving toward the bottom



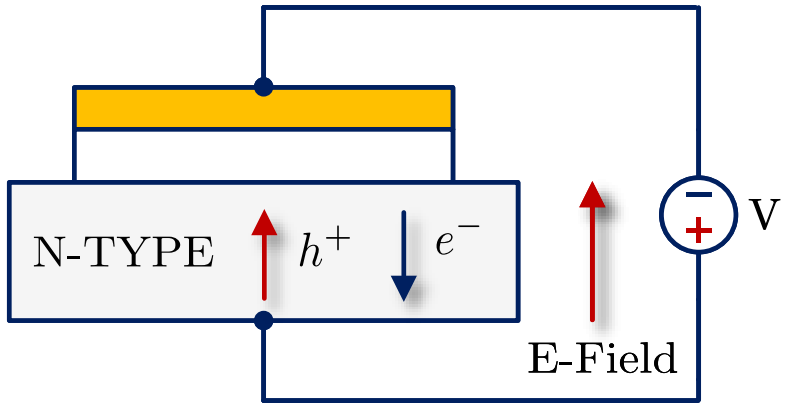
- E-field direction: point from top to the bottom
- Hole is moving toward the bottom, and electron is moving toward the top interface



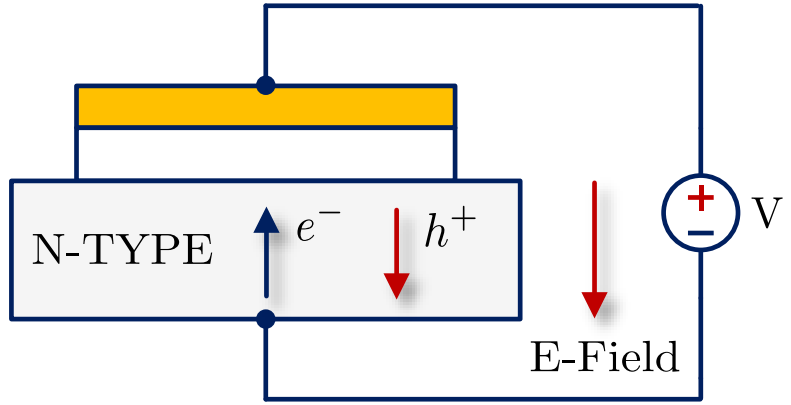
- An 「**Electron Inversion Layer**」 is created at the interface

Two-Terminals MOS (N-Type)

- E-field direction: point from bottom to the top
- Hole is moving toward the top interface, and electron is moving toward the bottom
- An 「**Hole Inversion Layer**」 is created at the interface



- E-field direction: point from top to the bottom
- Hole is moving toward the bottom, and electron is moving toward the top interface



Inversion Layer (反形层)

- What is inversion layer? Why do we have electron inversion layer at the interface in P-type MOS structure, not the hole inversion layer?
- **inversion layer**: is a layer in semiconductor material where the type of the majority carriers changes to it 「opposite」 under certain conditions.
- **For example**: In P-type semiconductor, the majority carriers are holes. However, an external voltage creates a region on surface where there are no holes but only electrons. In that region, minority electrons jump to the majority. The layer is called inversion layer.

P-MOS ⇨ Electron inversion layer

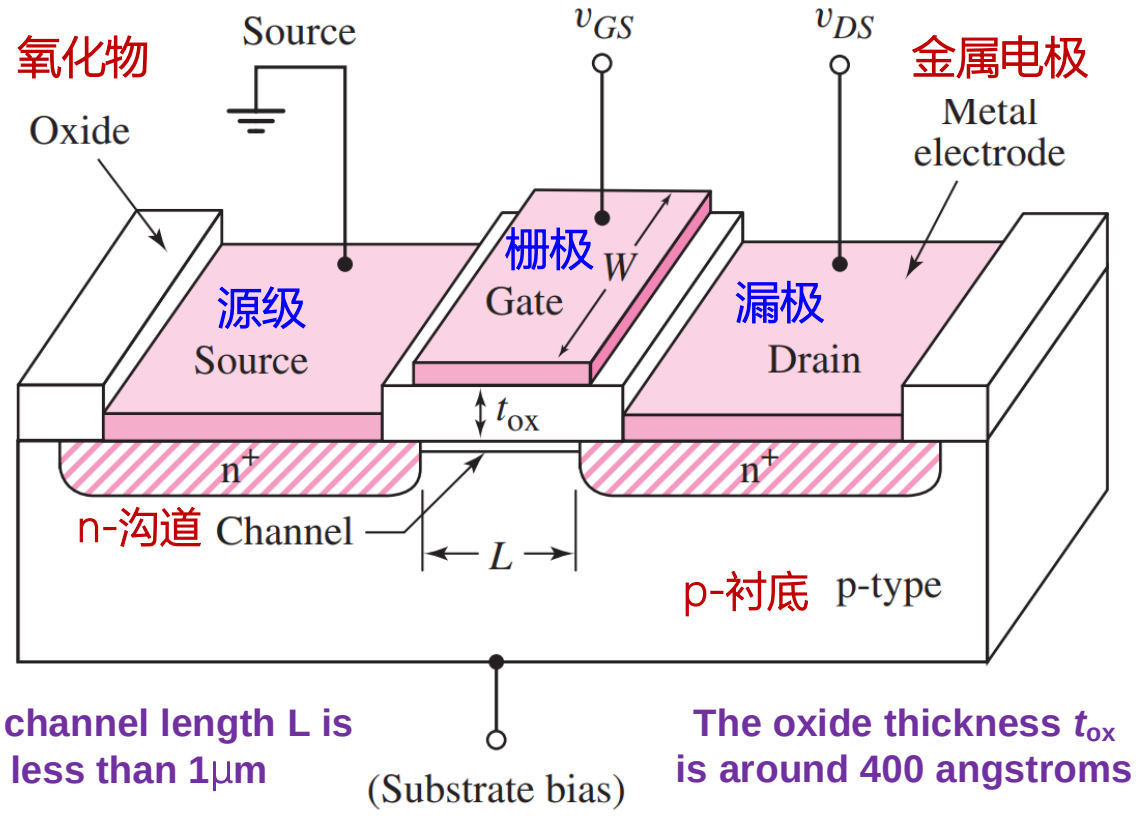
N-MOS ⇨ Hole inversion layer

N-channel MOSFET

- Now, we apply the concept of an inversion layer charge in a MOS capacitor to a transistor

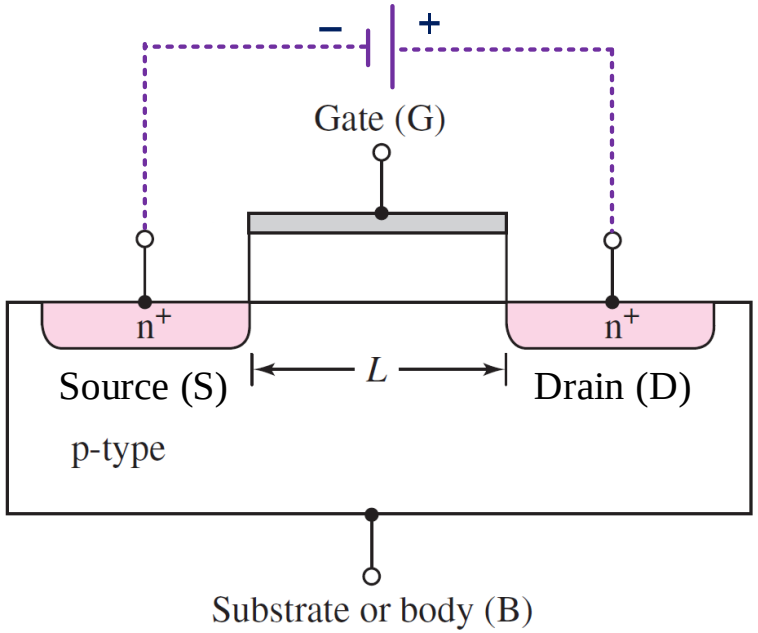
- The gate, oxide and p-type substrate are the same as those of a MOS capacitor.

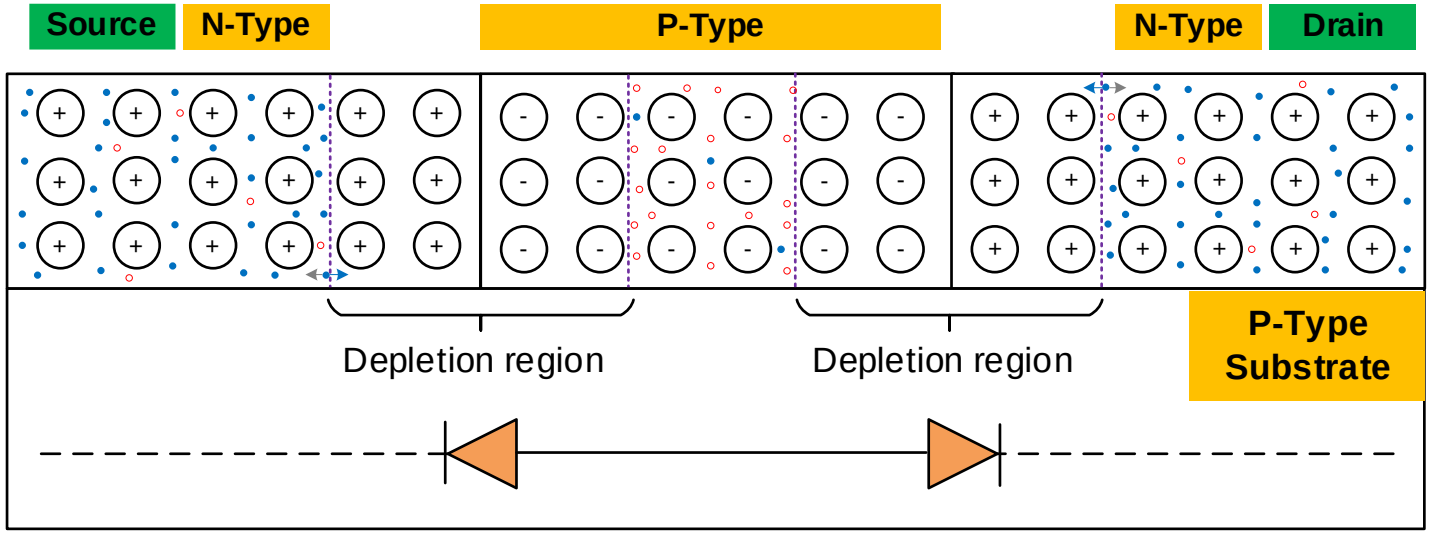
- However, we add two n-regions
  - Source terminal
  - Drain terminal



N-channel MOSFET

- Let simplify the structure of the NMOS to a 2D structure
- If there is no external voltage on this MOSFET, the source and drain terminal are separated by the p-region (substrate). The current in this case is zero

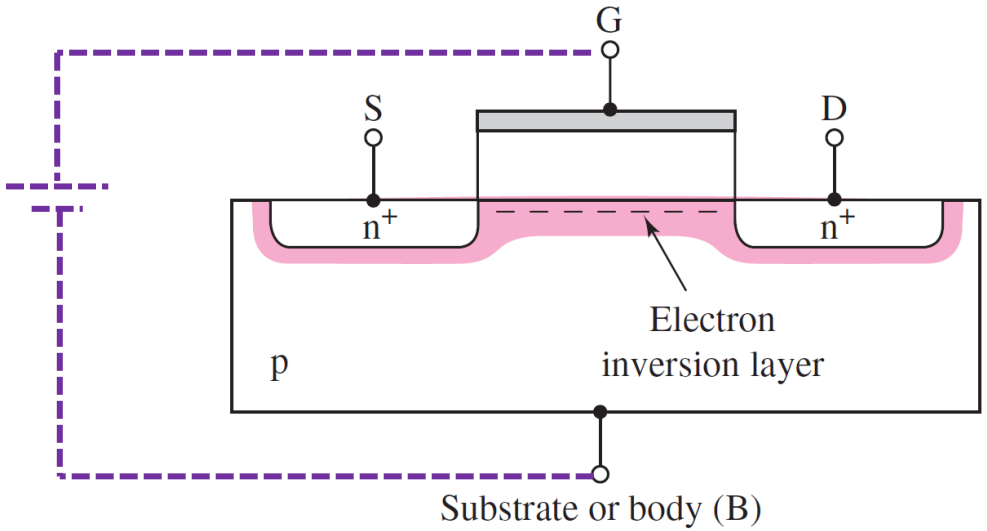




N-channel MOSFET

- If we add an external voltage on **Gate-to-Source**

- The electron inversion layer is created at the interface to connects the source and drain.

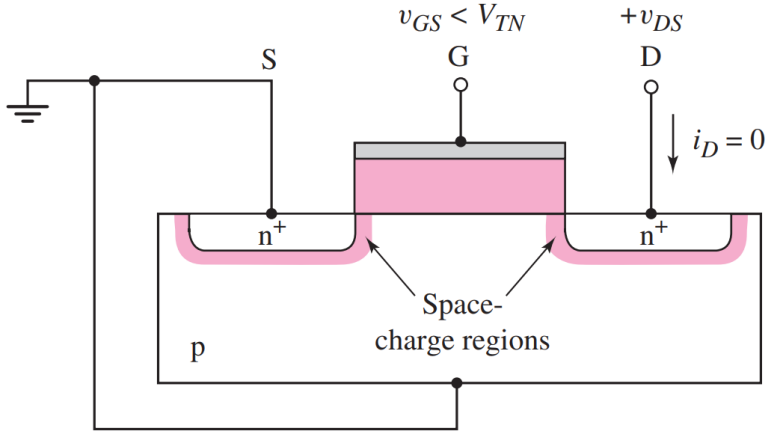


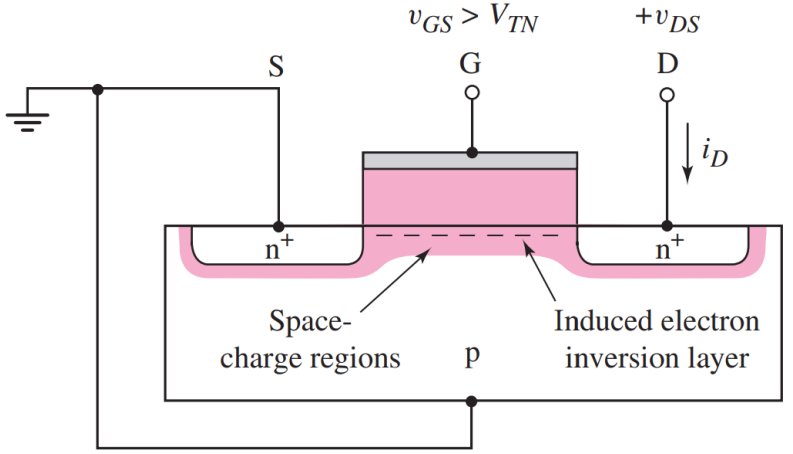
- **Definition**:
  - Since a external voltage must be applied to the gate to create the inversion layer, this transistor is called **enhancement-mode** MOSFET.
  - Since carrier in the inversion layer are electrons, it calls n-channel MOSFET (NMOS).

Characteristic curve of ideal NMOS

- 「**Threshold Voltage**」(阈值电压) V_{TN} is the voltage to "turn on" the transistor.

- For n-channel MOSFET, the threshold voltage is positive voltage is required to create the inversion layer.
  - When $V_{GS} < V_{TN}$, MOSFET turns OFF, drain current is zero
  - When $V_{GS} \geq V_{TN}$, MOSFET turns ON, current flows through the channel region

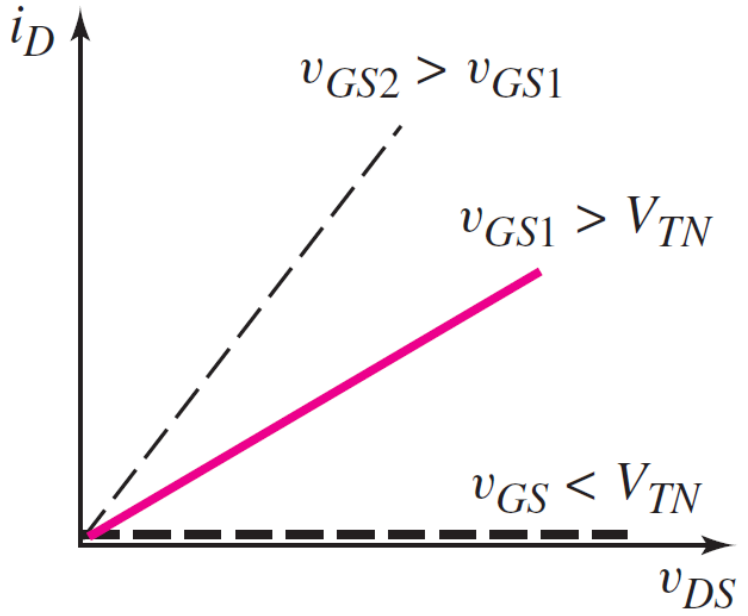




Characteristic curve of ideal NMOS

- The magnitude of current is a function of [amount of charge in the inversion layer] + [Gate voltage]

- When $V_{GS} < V_{TN}$, MOSFET turns OFF, drain current is zero



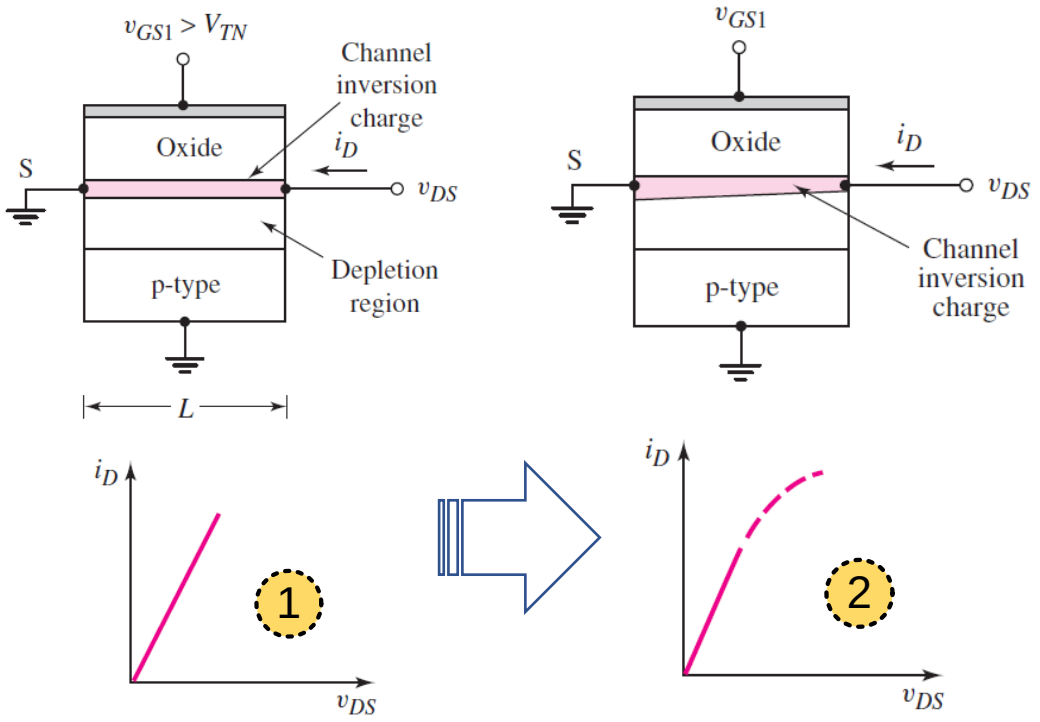
- When $V_{GS1} > V_{TN}$
  - Channel inversion charge is formed
  - Drian current increases with V_{DS}

- With a larger gate voltage V_{GS2}
  - Larger inversion charge density
  - Drain current is greater for a given value of V_{DS}

I-V Characteristic curve-Nonsaturation

1. At the beginning, applied V_{DS} is small, a relative constant thickness inversion layer

2. If V_{DS} is increasing, with a bigger value
   - The voltage drop across the oxide near the drain terminal decreases
   - The induced inversion charge density decreases
   - The incremental conductance is decreasing



I-V Characteristic curve-Saturation

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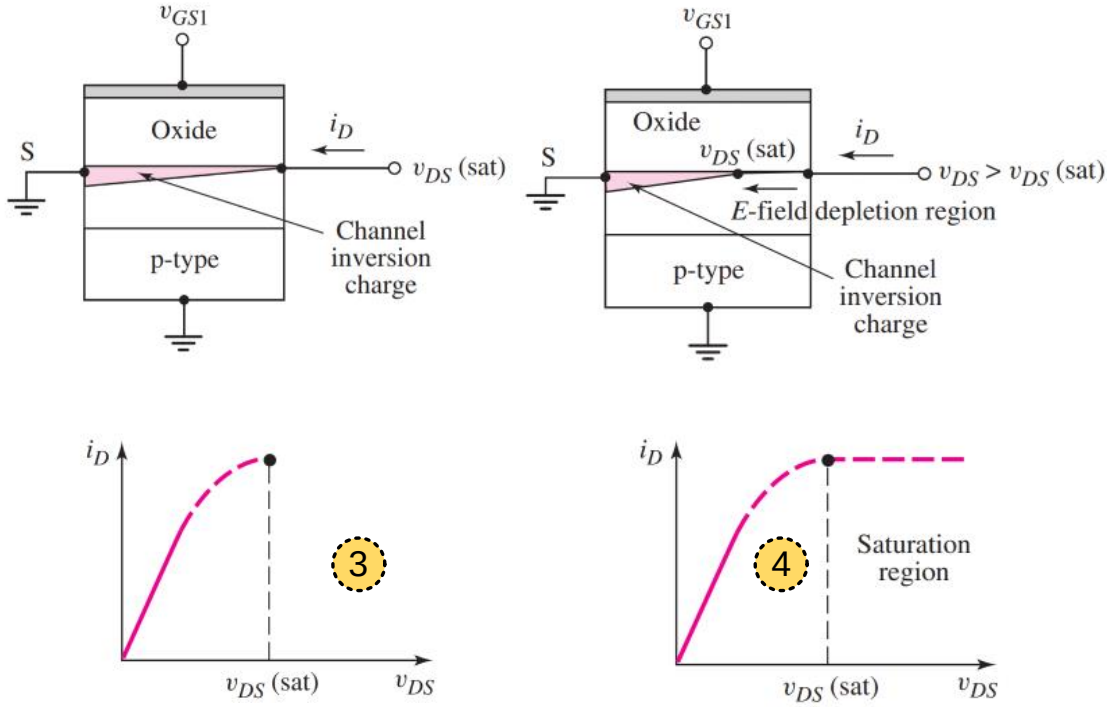
3. If $V_{DS} = V_{GS} - V_{TN}$
   - The inversion charge density at the drain terminal is zero (Similar to the case when $V_{GS} = V_{TN}$)
   - The incremental conductance equal to zero

$$V_{\mathrm{DS}}\,(\mathrm{sat}) = V_{\mathrm{GS}} - V_{\mathrm{TN}}$$



4. If $V_{DS} > V_{DS}(sat)$
   - Drain current i_D is constant
   - This MOSFET is in 「**saturation region**」

I-V Characteristic curve-NMOS

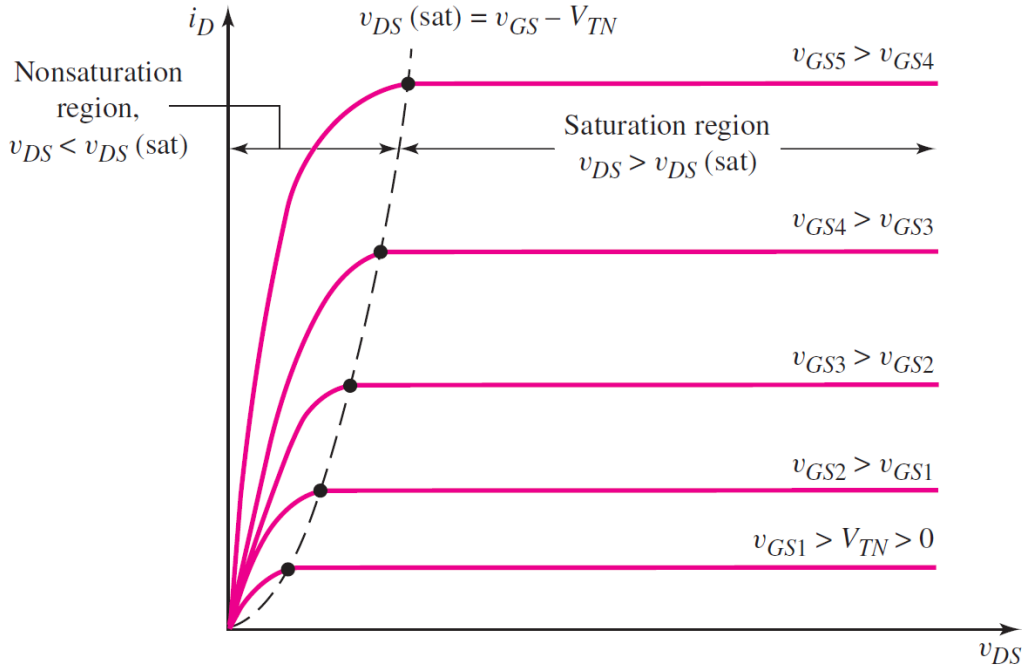
- Nonsaturation region:

$$V_{\mathrm{DS}} < V_{\mathrm{DS}}\,(\mathrm{sat})$$

$$i_D = K_n\left[2\left(V_{GS} - V_{TN}\right)V_{DS} - V_{DS}^2\right]$$

- Saturation point:

$$V_{DS}\,(\mathrm{sat}) = V_{GS} - V_{TN}$$



- Saturation region: $V_{\mathrm{DS}} \geq V_{\mathrm{DS}}\,(\mathrm{sat})$

$$i_D = K_n(V_{GS} - V_{TN})^2$$

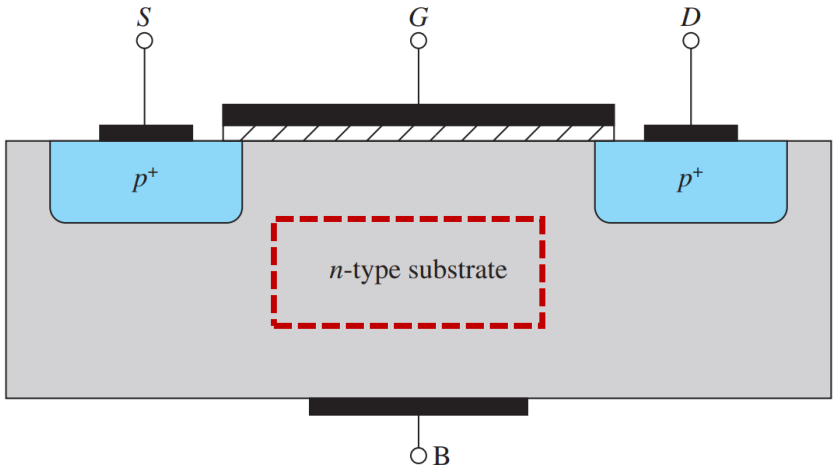
K_n is the conduction parameter, constant

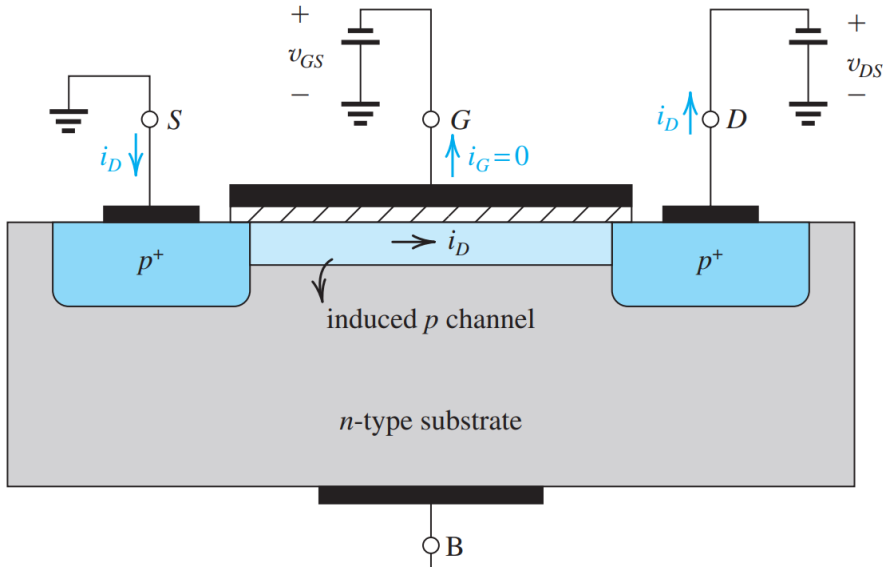
I_D is independent of V_{DS}

P-channel MOSFET (PMOS)

- The substrate is n-type semiconductor. The source and drain areas are p-type semiconductor. Current is out of the drain terminal.

- The channel length, width, and oxide thickness parameter definitions of PMOS are the same as those for the NMOS.

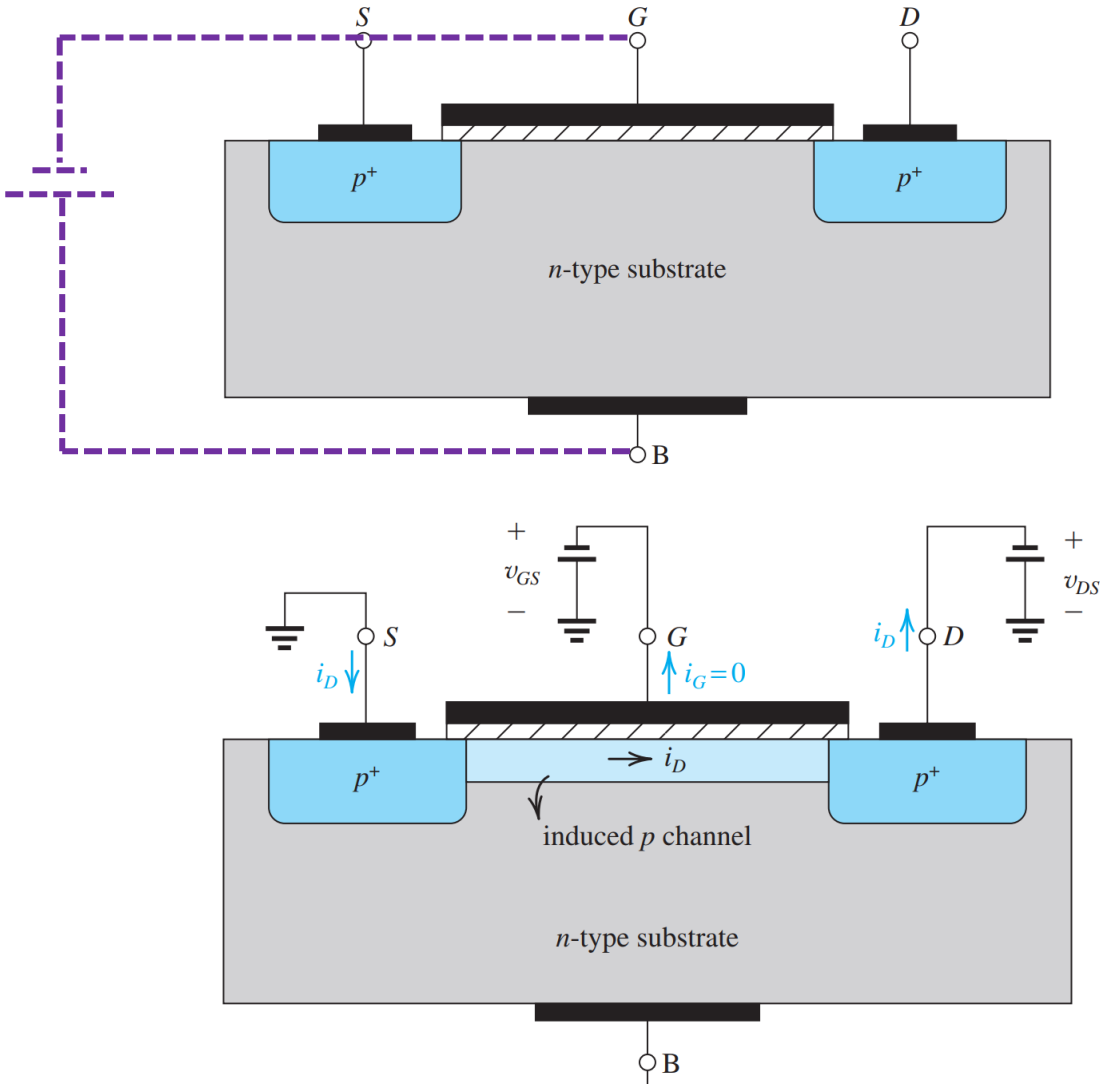




P-channel MOSFET (PMOS)

- In PMOS, holes are the carrier
- A negative gate bias voltage is required to induce inversion layers. Therefore, the threshold voltage is negative $V_{TP} < 0$
- For generating of current flow, we should ensure $V_{GS} \leq V_{TP}$

$$|V_{SG}| \geq |V_{TP}|$$



P-channel MOSFET (PMOS)

- V_{DS} is replaced by V_{SD} in PMOS
- Nonsaturation region:

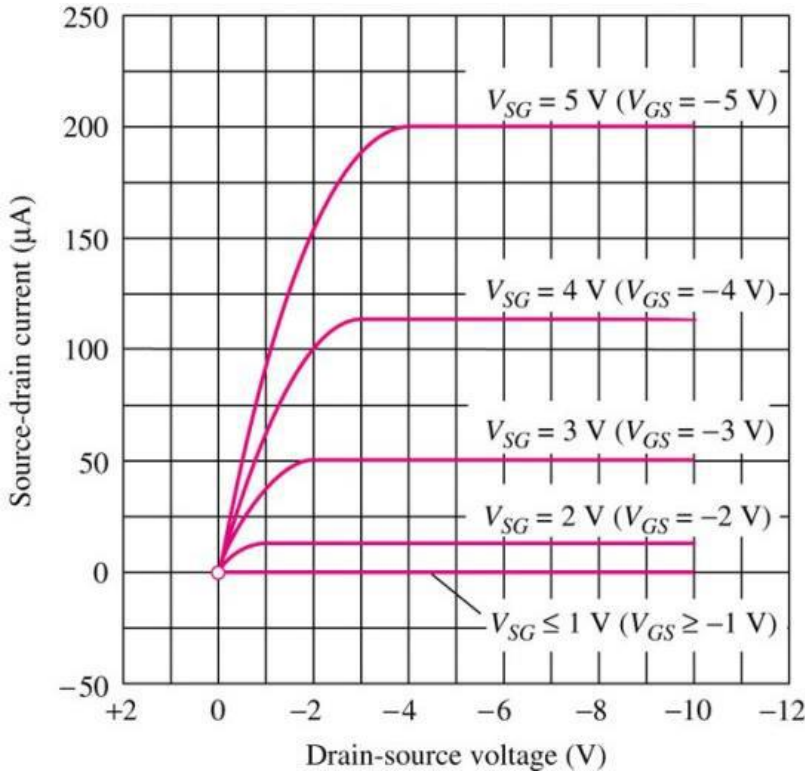
$$i_D = K_n \left[2\left(V_{SG} + V_{TP}\right) V_{SD} - V_{SD}^2\right]$$

- Saturation point:

$$V_{SD}\,(\text{sat}) = V_{SG} + V_{TP}$$

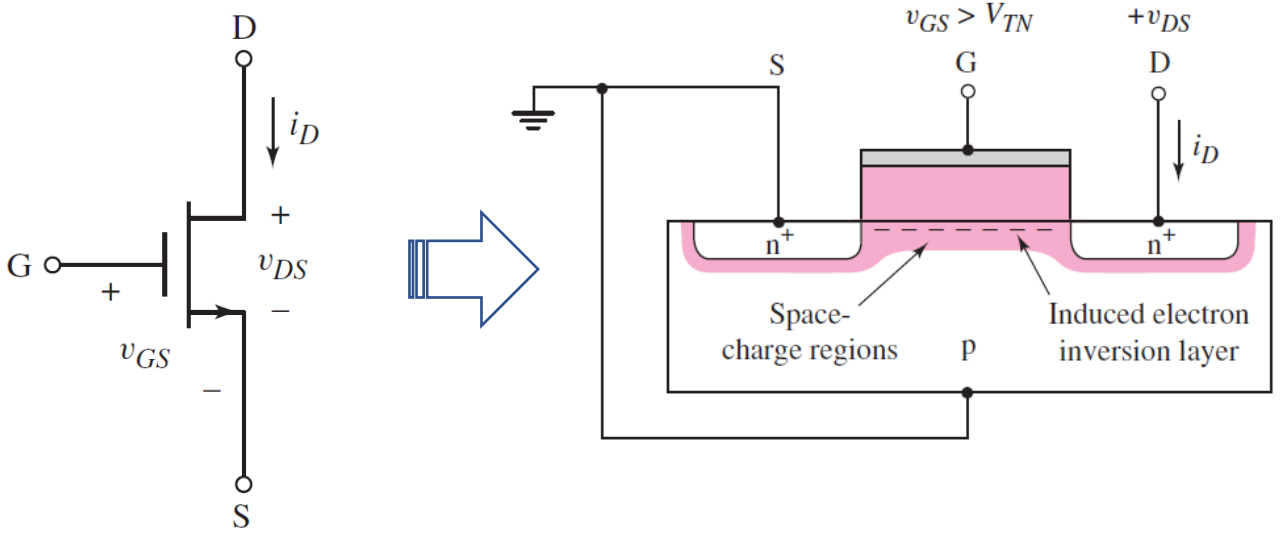
- Saturation region:

$$i_D = K_p (V_{SG} + V_{TP})^2$$

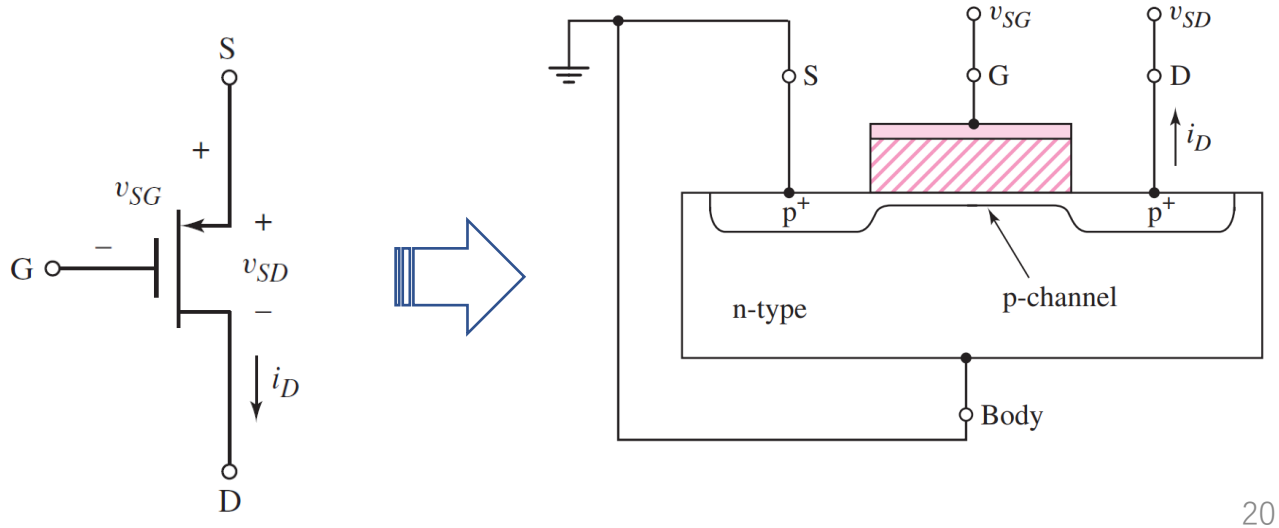


Circuit Symbol

- For NMOS
- The "TOP" terminal is the Drain
- The "Bottom" terminal is the Source



- For PMOS
- The "Top" terminal is the Source
- The "Bottom" terminal is the Drain



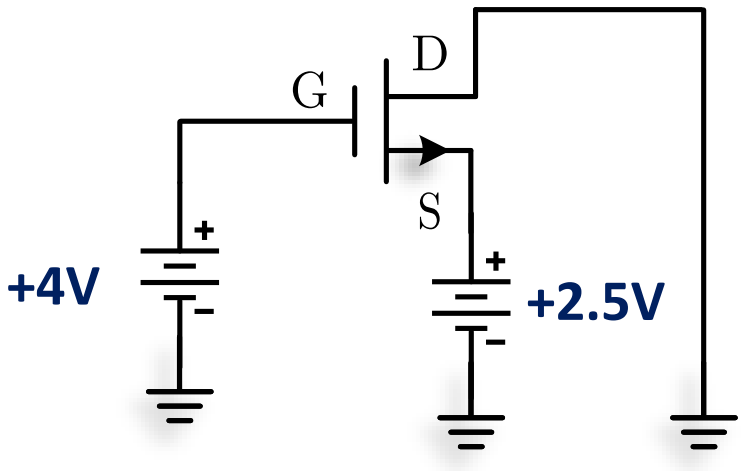
Summary of Transistor Operation

	NMOS	PMOS
Saturation	$v_{DS} \geq v_{DS}\,(sat)$ $i_D = k_n(v_{GS} - v_{TN})^2$	$v_{SD} \geq v_{SD}\,(sat)$ $i_D = k_n(v_{SG} + v_{TP})^2$
Nonsaturation	$v_{DS} < v_{DS}(sat)$ $i_D = k_n\left[2\left(v_{GS} - v_{TN}\right)v_{DS} - v_{DS}^2\right]$	$v_{SD} < v_{SD}(sat)$ $i_D = k_n\left[2\left(v_{SG} + v_{TP}\right)v_{SD} - v_{SD}^2\right]$
Transition point	$v_{DS}\,(sat) = v_{GS} - v_{TN}$	$v_{SD}\,(sat) = v_{SG} + v_{TP}$
Enhancement mode	$v_{TN} > 0$	$v_{TP} < 0$

Reinforce Your Learning (Exercise)

1. Consider an NMOS transistor having V_{TN} = 2V. What is the bias region if we have:
   - (a) V_{GS} = 10V, V_{DS} = 1;
   - (b) V_{GS} = 5V, V_{DS} = 5V;
   - (c) V_{GS} = 1V, V_{DS} = 10V

2. Consider an NMOS transistor having V_{TN} = 2V. In such a circuit (right figure). What is the bias region of the NMOS?

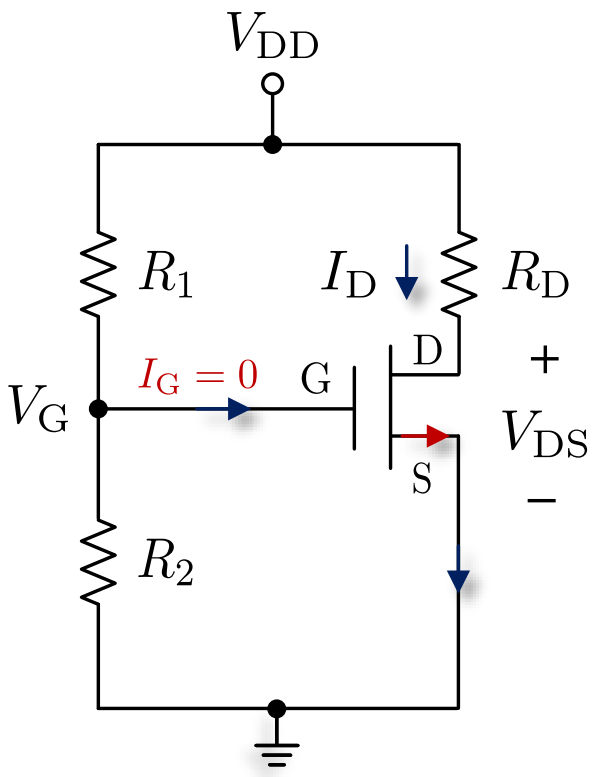


MOSFET DC Circuit Analysis

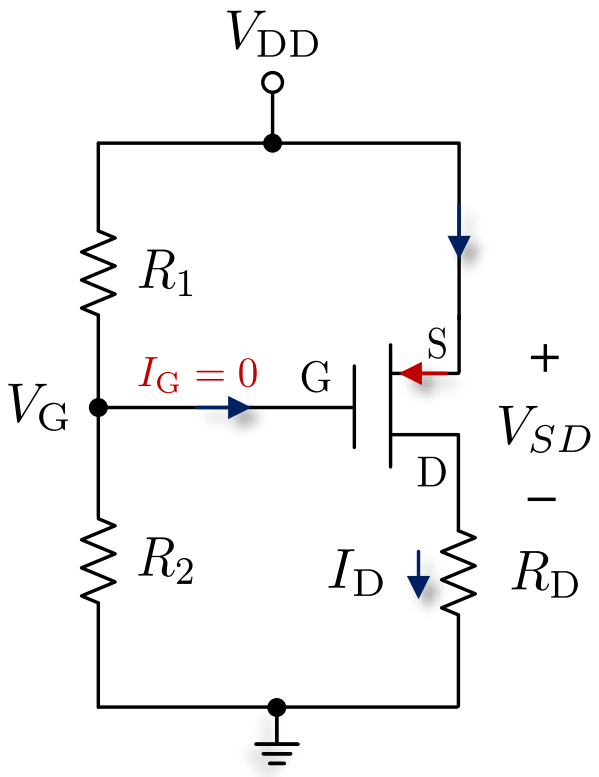
Understand and become familiar with the DC analysis and design techniques of MOSFET circuits.

MOSFET Common Source Circuit

- Put a MOSFET into a DC circuit to analyze the Drain to Source voltage, drain current and power consumption.



NMOS DC CIRCUIT



PMOS DC CIRCUIT

- 「Cut-off region」
- 「Non-saturation region」
- 「Saturation region」

Problem-Solving Tips: DC Analysis

- To analyze MOSFET circuit with DC sources, we must follow these **Four steps (AACM)**:

1. **ASSUME** an operation model (saturation firstly)

2. **ANALYZE** the circuit with the assumed condition

$$i_D = K_n(V_{GS} - V_{TN})^2 \quad V_{DS} = V_{DD} - I_D R_D \quad V_{DS}\,(\text{sat}) = V_{GS} - V_{TN}$$

3. **CHECK** the results of the mode for matching with original assumption. If consistent, the analysis is complete; If inconsistent, go to step 4

4. **MODIFY** your original assumption and repeat all steps.

NMOS Common Source Circuit

- The gate current into the transistor is zero, don't forget the oxide (insulator) between metal and substrate

$$V_{GS} = V_G - V_S \qquad V_S = 0 \rightarrow V_{GS} = V_G = \frac{R_2}{R_1 + R_2} V_{DD}$$

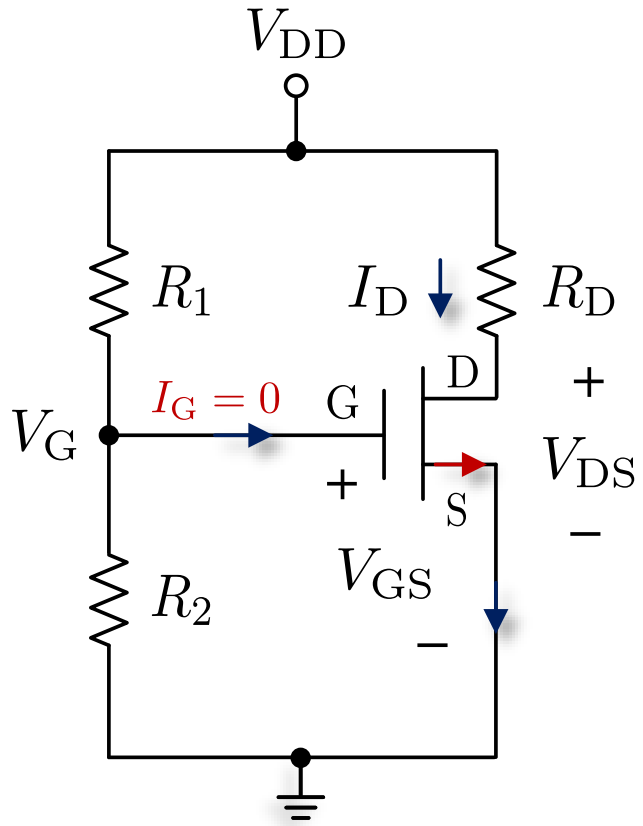
- Then we can calculate the saturation voltage

$$V_{DS}\,(\text{sat}) = V_{GS} - V_{TN}$$

- Assume $V_{DS} \geq V_{DS(sat)}$ and the transistor bias in saturation

$$i_D = K_n (V_{GS} - V_{TN})^2 \Rightarrow V_{DS} = V_{DD} - I_D R_D$$

- Finally, we should verify our assumption $\Rightarrow V_{DS} \geq V_{DS}\,(\text{sat})$ Yes?



NMOS DC CIRCUIT

PMOS Common Source Circuit

- The gate current into the transistor is zero

$$V_{SG} = \frac{R_1}{R_1 + R_2} V_{DD}$$

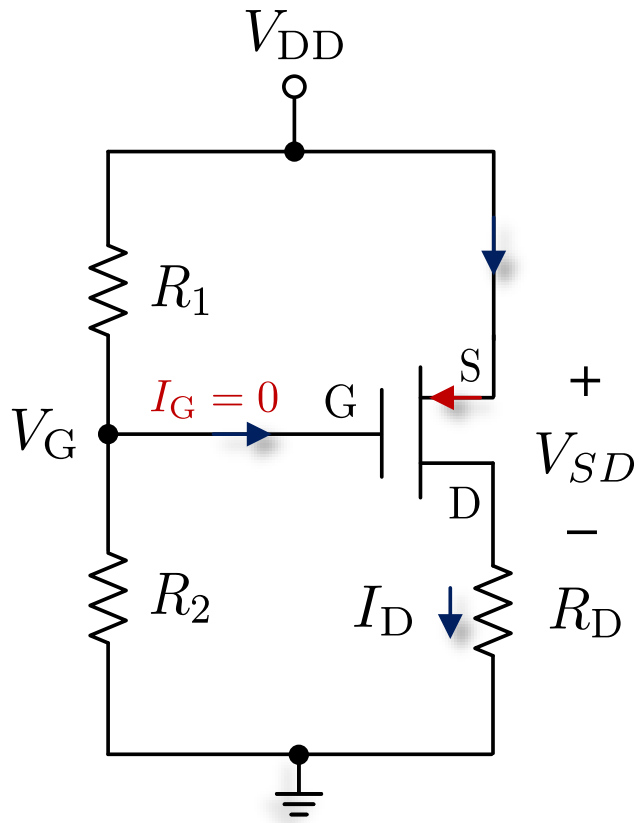
- Then we can calculate the saturation voltage

$$V_{SD}\,(\text{sat}) = V_{SG} + V_{TP}$$

- Assume $V_{SD} \geq V_{SD(sat)}$ and the transistor bias in saturation

$$i_D = K_n (V_{SG} + V_{TP})^2 \quad \Rightarrow \quad V_{SD} = V_{DD} - I_D R_D$$

- Finally, we should verify our assumption $\Rightarrow$ $V_{SD} \geq V_{SD}\,(\text{sat})$ Yes?

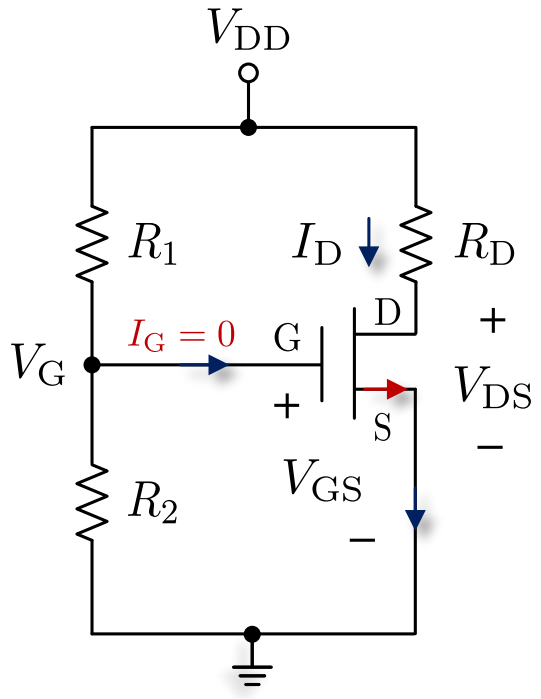


PMOS DC CIRCUIT

Reinforce Your Learning (Exercise)

- Calculate the drain current and drain-to-source voltage of a common-source circuit with an n-channel enhancement-mode MOSFET. Find the power dissipated in the transistor. Assume R_1 = 30kΩ, R_2 = 20kΩ, R_D = 20kΩ, V_{DD} = 5V, V_{TN} = 1V and K_n = 0.1mA/V^2

- Solution



NMOS DC CIRCUIT

BASIC MOSFET APPLICATION

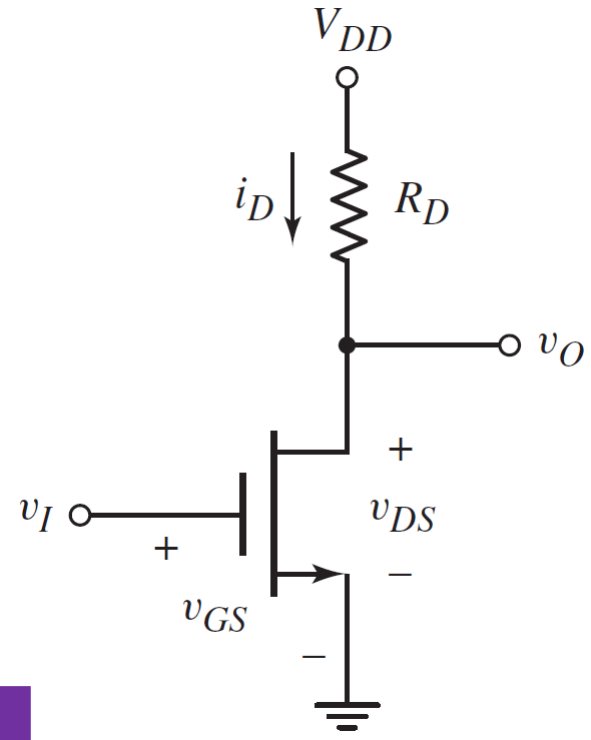
Examine three applications of MOSFET circuits: a MOS Inverter, digital logic circuit, and an amplifier circuit.

Switch circuit-NMOS Inverter

- The transistor switch considered in this section is also called an MOS inverter. The working mode is that value of input signal control the output signal. But, the potentials are reversed.

- If the input signal is Low-level, and $V_I < V_{TN}$
  - Transistor is cutoff, and $I_D = 0$. No power is dissipated in the transistor
  - Output voltage $V_o = V_{DD}$, which is high-level

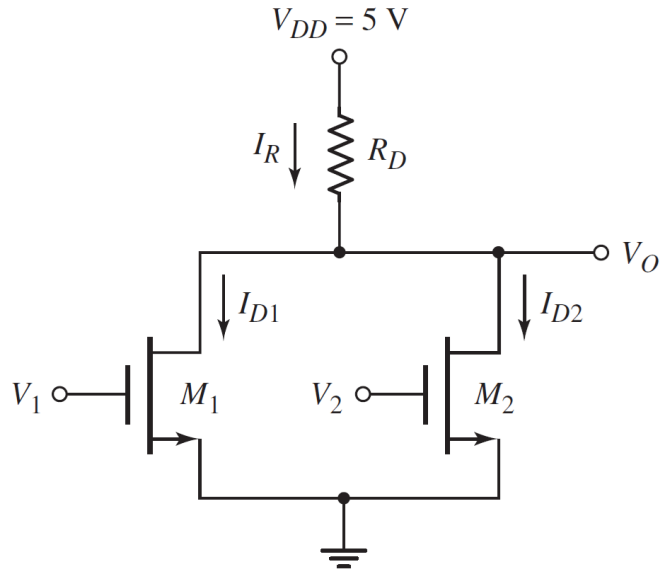
- If the input signal is High-level, and $V_I > V_{TN}$
  - Transistor is on, and whole circuit goes on.
  - Output voltage $V_o = V_{DD}$-$i_D R_D$, which is Low-level



V_I Low ⇨ V_o High V_I High ⇨ V_o Low

Digital Logic Gate (NOR Gate)

- Two NMOS Transistors are connected in parallel
- If $V_1 = V_2 = 0$ (M_1 and M_2 are cutoff. $V_o = V_{DD}$, high-level)
- If V_1 = 5V V_2 = 0V or V_1 = 0V V_2 = 5V
  - M_1 is turn on, M_2 is cut off. Or, M_1 is cut off, M_2 is turn on
  - $V_o = V_{DD}$-$I_R R_D$ which is a low-level
- If $V_1 = V_2$ = 5V
  - M_1 and M_2 are turn on
  - V_o is at low-level



NMOS NOR logic circuit response		
V_1(V)	V_2(V)	V_O(V)
0	0	**High**
5	0	Low
0	5	Low
5	5	Low

MOSFET Amplifier

- An amplifier is an electrical device, used to enhance the amplitude of the input signal. It is an essential part of audio sources like a record player or CD player and also other devices

- At present, MOSFET amplifiers are a design choice in 99% of the microchips around the world.

- We will learn such circuit in CHAPTER 5.