EEE201-HW1

- **Q1:**

In the MOS transistors of a digital integrated circuits (ICs), the drain diffusion region has an ***n***-type doping of 10^{18} cm^{-3} on a silicon substrate with the ***p***-type doping of 10^{16} cm^{-3}.

a) **Question:**

What is the approximate intrinsic carrier concentration in silicon at room temperature (T = 300 K)? Hence or otherwise, calculate the built-in potential V_{bi} of the *p*-*n* junction between the *p*-type substrate and the *n*-type drain region at room temperature.

Answer:

From the given information,

$$ND = 10^{18}cm^{-3} \ and \ NA = 10^{16}cm^{-3}$$

Because it is a n-type MOSFET under room temperature, therefore, we can approximate the intrinsic carrier concentration:

$$n_i = 10^{10}cm^{-3}$$

According to the formula,

$$V_{bi} = \frac{kT}{q} * \ln\left(\frac{\mathrm{NA} * \mathrm{ND}}{n_i^2}\right)$$

Where

Boltzmann constant $k = 1.38 * 10^{-23}J/k$

Electron charge $q = 1.602 * 10^{-19}c$

Thus, the built-in potential,

$$V_{bi} = 0.84V$$

b) **Question:**

Using the result in (a) or otherwise, calculate the depletion width of the *p*-*n* junction when both the drain and the substrate are not connected to any voltage (i.e. zero-biased).

Answer:

If the junction is under zero-biased condition, the depletion width can be represented as:

$$W_{dep} = \sqrt{\frac{2\varepsilon_{si}}{q}\left(\frac{\mathrm{NA} + \mathrm{ND}}{NA * ND}\right)V_{bi}}$$

Where

Permittivity of Si $\varepsilon_{si} = 1.05 * 10^{-12}F/cm$

Electron charge $q = 1.602 * 10^{-19}c$

Donor concentration $NA = 10^{18}cm^{-3}$

Acceptor concentration $ND = 10^{16}cm^{-3}$

Built-in potential $V_{bi} = 0.84V$
Hence, depletion width (zero-biased) is

$$W_{dep} = 0.33\mu m$$

c) **Question:**
Using Matlab or Excel, plot a graph of the depletion width when the substrate is connected to ground and the drain voltage VDS increases from 0 V to +3.0 V.

Answer:
If we apply drain voltage VDS, then the depletion width can be rewrite as:

$$W_{dep} = \sqrt{\frac{2\varepsilon_{si}}{q}\left(\frac{\mathrm{NA} + \mathrm{ND}}{NA * ND}\right)(V_{bi} + VDS)}$$

From (a) and (b), we have calculated the parameters, and then we write a code to plot the diagram shown in Fig 1 (*See codes in Appendix*).

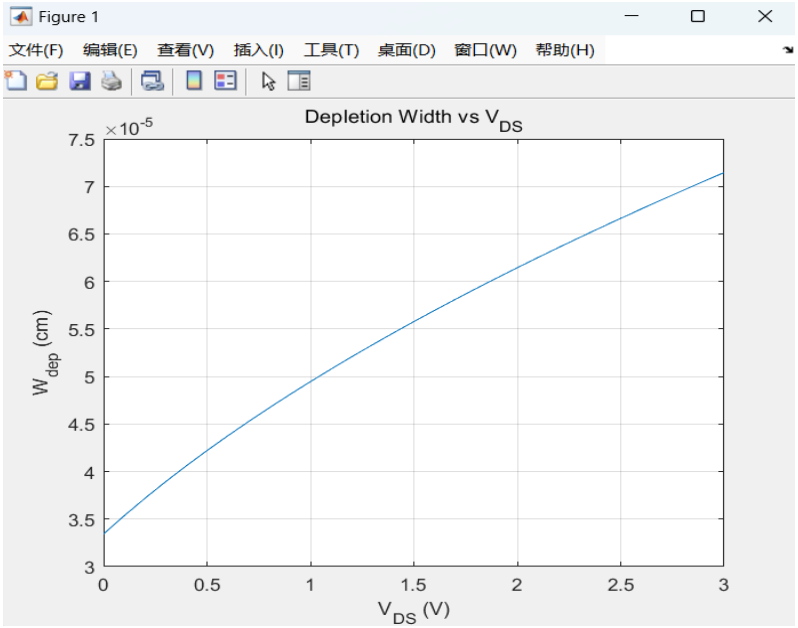

Fig 1. Depletion Width grows with VDS

d) **Question:**
If the drain region of the MOSFET has a total area of 40 μm × 0.6 μm, using the result in (b) or otherwise, calculate the depletion capacitance of the drain terminal in the open-circuit condition. Assume the sidewall contribution to the depletion capacitance negligible.

Answer:
The general form of junction capacitance is:

$$Cj0 = Cjoa * AREA + Cjosw * PERIMETER$$

This question only requires us to the former part, and assign this capacitance as $Cj1$, and we can derive the relationship:

$$Cj1 = Cjoa * AREA$$

The unit capacitance $Cjoa$ is

$$Cjoa = \frac{\varepsilon_{si} * AREA}{W_{dep}} * \frac{1}{AREA} = \frac{\varepsilon_{si}}{W_{dep}}$$

Thus, the we can simplify the $Cj1$ to:

$$Cj1 = \frac{\varepsilon_{si} * AREA}{W_{dep}}$$

Where

Permittivity of Si $\varepsilon_{si} = 1.05 * 10^{-10} F/m$

Depletion Width W_{dep} $W_{dep} = 0.33\mu m$

Total Area AREA $AREA = 40\mu m * 0.6\mu m = 2.4 * 10^{-15} m^2$

In summary, this capacitance can be calculated as

$$Cj1 = 7.64 * 10^{-15} F$$

e) **Question:**

If the depth of the drain region is 0.15 μm, calculate the sidewall contribution to the depletion capacitance in the open-circuit condition (i.e. zero-biased) (Hint: What is the perimeter of the drain region?).

Answer:

From (d), we can assume that $W = 40\mu m$ and $Ls = 0.6\mu m$.

The general form of junction capacitance is:

$$Cj0 = Cjoa * AREA + Cjosw * PERIMETER$$

This question only requires us to the latter part, and assign this capacitance as $Cj2$, and we can derive the relationship:

$$Cj2 = Cjosw * PERIMETER$$

Additionally, the sidewall capacitance of MOSFET under zero-bias condition should include all four surrounding sidewalls, since there is no formed channel under zero-bias condition.

The unit capacitance $Cjosw$ is

$$Cjosw = \frac{\varepsilon_{si} * h * PERIMETER}{W_{dep}} * \frac{1}{PERIMETER} = \frac{\varepsilon_{si} * h}{W_{dep}}$$

Thus, the we can simplify the $Cj2$ to:

$$Cj2 = \frac{\varepsilon_{si} * h * PERIMETER}{W_{dep}}$$

Where

Permittivity of Si $\varepsilon_{si} = 1.05 * 10^{-10} F/m$

Depletion Width W_{dep} $W_{dep} = 0.33\mu m$

Total perimeter PERIMETER $PERIMETER = 2 * (Ls + W) = 8.12 * 10^{-5} m$

Depth h $h = 0.15\mu m$

In summary, this capacitance can be calculated as

$$Cj2 = 3.88 * 10^{-15} F$$

f) **Question:**

Using Matlab or Excel, plot a graph of the total depletion capacitance (with the sidewall contribution included) when the substrate is connected to ground and the drain voltage VDS increases from 0 V to +3.0 V.

Answer:

From (d) and (e), we have calculated the separated part of capacitance contributed to the area and sidewall of the junction. To find the total capacitance, we just need to add them together, and treat this unity as a constant, which is

$$Cj0 = Cj1 + Cj2 = (7.64 + 3.88) * 10^{-15} = 11.52 * 10^{-15} F$$

Based on the relationship between total junction capacitance and VDS,

$$Cj = \frac{Cj0}{\sqrt{1 + \frac{VDS}{Vbi}}}$$

Where

Built-in potential $V_{bi} = 0.84V$

Therefore, the graph is shown in following Fig 2 (*See codes in Appendix*).

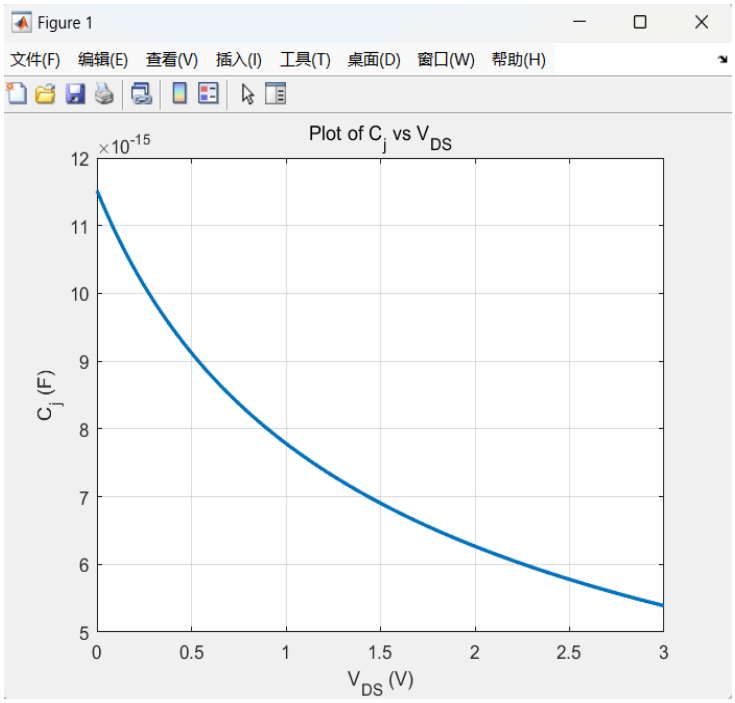

Fig 2. Junction Capacitance decreases with VDS

➢ **Q2:**

The MOS transistors of the same digital integrated circuits (ICs) described in Question 1 has a gate oxide thickness t_{ox} of 30 Å (i.e. 3.0 nm) and an effective channel length L = 0.15 μm.

a) **Question:**

Calculate the *normalized* gate oxide capacitance C_{ox} of the MOS transistors. Assume the gate oxide is made of high-quality silicon dioxide (SiO_2).

Answer:

Since we need to find the normalized capacitance of gate oxide, we are able to neglect the fringing effect, and the formula is

$$Cgate = \frac{\varepsilon_{ox}}{t_{ox}}$$

Where

Permittivity of Sio2 $\varepsilon_{ox} = 3.9 * 8{,}85 * 10^{-12} F/m$

From the given information, $t_{ox} = 3nm$

Therefore, the gate oxide capacitance can be calculated as

$$Cox = Cgate = 11.51\ mF$$

b) **Question:**

Determine the gate-to-source capacitance C_{GS} of the MOS transistor operating in the saturation region. Note that the MOSFET has W = 40 μm and L = 0.15 μm.

Answer:

Since the MOSFET is biased in the linear mode, hence CGS will become

$$CGS = Cox * W * Leff * 2/3$$

Where

Capacitance of gate oxide $Cox = 11.51 * 10^{-3} F$

Width $W = 40\mu m$

Effective Length $Leff = 0.15\mu m$

Hence, gate-to-source capacitance CGS is

$$CGS = 4.60 * 10^{-14} F$$

c) **Question:**

Determine the gate-to-drain capacitance C_{GD} of the MOS transistor if it operates in the linear mode. How does the value of C_{GD} compare with the depletion capacitance of the drain-to-substrate junction?

Answer:

Since the MOSFET is biased in the linear mode, hence CGD will become

$$CGD = Cox * W * Leff * 1/2$$

Where

Capacitance of gate oxide $Cox = 11.51 * 10^{-3} F$

Width $W = 40\mu m$

Effective Length $Leff = 0.15\mu m$

Hence, gate-to-drain capacitance CGD is

$$CGD = 3.45 * 10^{-14} F$$

From Q1, we know that $Cj0 = 11.52 * 10^{-15} F < CGD = 3.45 * 10^{-14} F$

Therefore, CGD is greater than the depletion capacitance of the drain-to-substrate junction $Cj0$.

d) **Question:**

It is given the electron mobility for the MOS transistors is 370 cm_2/Vs and the threshold voltage V_T of the *n*-channel MOS transistors is 0.45 V. Assuming the long-channel approximation, using *Matlab* or *Excel*, plot a graph of the output characteristics (i.e. I_{DS} vs. V_{DS}) of a MOS transistor with a channel width W = 40 μm and L = 0.15 μm for V_{GS} = 0.7 V, 1.0 V, 1.5 V and 2.0 V while V_{DS} varies from 0 V to 2.5 V.

Answer:

We know that the output characteristics of MOSFET is the curve with y-axis ID and x-axis VDS, and ID has different equations under various regions.
If MOSFET is biased in the linear region (VGS>VT & VDS<VGS-VT), then ID will equal to,

$$ID = \mu n * Cox * \frac{W}{L} * [(VGS - VT) * VDS - 0.5 * VDS^2]$$

And if MOSFET is biased in the saturation region (VGS>VT & VDS>VGS-VT), then ID will equal to,

$$ID = 0.5 * \mu n * Cox * \frac{W}{L} * (VGS - VT)^2$$

All the parameters we have known as below,
Electron mobility for the MOS transistors μn $\mu n = 370\ cm^2/\text{Vs}$
Capacitance of gate oxide Cox $Cox = 11.51 * 10^{-3} F$
Width W $W = 40\mu m$
Effective Length L $L = Leff = 0.15\mu m$
Threshold Voltage VT $VT = 0.45V$
Then, we need to set conditions for different biases and write the MATLAB code (*because all these VGS are greater than VT, hence I don't set VGS>VT as a condition*), and observe the plot as shown in Fig 3 (*See codes in Appendix*).

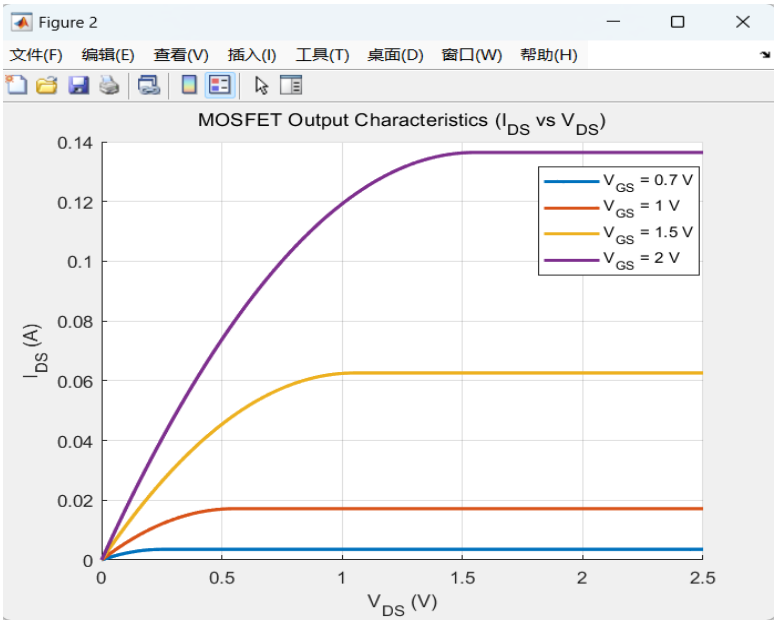

Fig 3. MOSFET Output Characteristics Curve

e) **Question:**

With the same parameters and the long-channel approximation, using *Matlab* or *Excel*, plot a graph of the transfer characteristics (i.e. I_{DS} vs. V_{GS}) of a MOS transistor of the same size W/L = 40 µm/0.15 µm for V_{DS} = 0.2 V, 1.0 V, 2.0 V while V_{GS} varies from 0 V to 2.0 V. Assume the current is zero when V_{GS} is below the threshold voltage V_T.

Answer:

We know that the transfer characteristics of MOSFET is the curve with y-axis IDS and x-axis VGS, and ID has different equations under various regions.
If MOSFET is biased in the linear region (VGS>VT & VDS<VGS-VT), then ID will equal to,

$$ID = \mu n * Cox * \frac{W}{L} * [(VGS - VT) * VDS - 0.5 * VDS^2]$$

And if MOSFET is biased in the saturation region (VGS>VT & VDS>VGS-VT), then ID will equal to,

$$ID = 0.5 * \mu n * Cox * \frac{W}{L} * (VGS - VT)^2$$

All the parameters we have known as below,
Electron mobility for the MOS transistors μn $\mu n = 370\ cm^2/Vs$
Capacitance of gate oxide Cox $Cox = 11.51 * 10^{-3} F$
Width W $W = 40\mu m$
Effective Length L $L = Leff = 0.15\mu m$
Threshold Voltage VT $VT = 0.45V$
Then, we need to set conditions for different biases and write the MATLAB code, and observe the plot as shown in Fig 4 (*See codes in Appendix*).

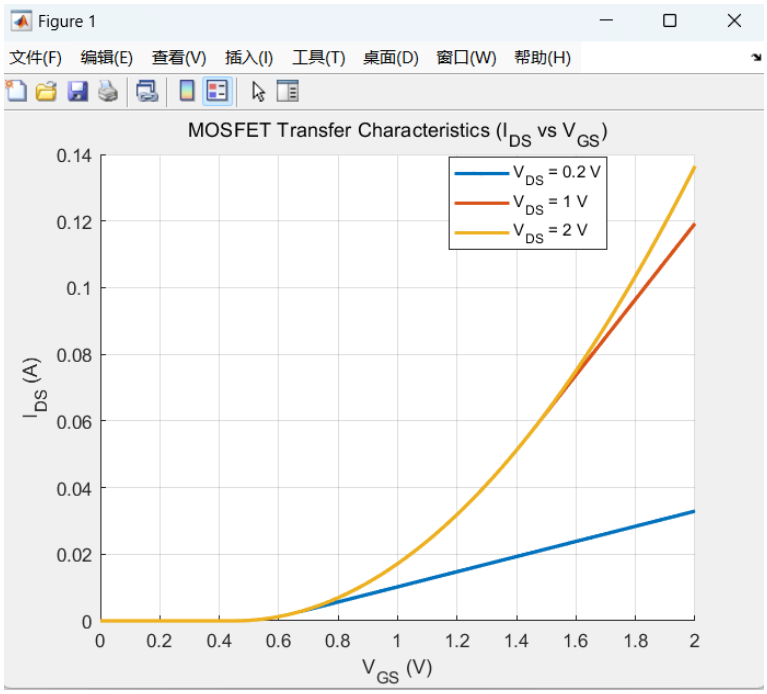

Fig 4. MOSFET Transfer Characteristics

f) **Question:**

If hafnium oxide (HfO_2) with a dielectric constant of 25 is used to replace the silicon dioxide (SiO_2) as the gate dielectric, what would be the gate oxide thickness t_{HfO} to keep same the normalized gate oxide capacitance C_{ox} as that obtained in Q2(a)?

Answer:

We have known the formula of gate oxide capacitance,

$$Cox = Cgate = \frac{\varepsilon_{ox}}{t_{ox}}$$

If we would like to maintain the same capacitance but with different materials, then we should satisfy:

$$\frac{\varepsilon_{ox}}{t_{ox}} = \frac{\varepsilon_{Hfo2}}{t_{Hfo2}}$$

So, it simplifies to

$$t_{Hfo2} = \frac{\varepsilon_{r-Hfo2}}{\varepsilon_{r-sio2}} t_{ox}$$

With

$$\frac{\varepsilon_{r-Hfo2}}{\varepsilon_{r-sio2}} = \frac{25}{3.9} \; and \; t_{ox} = 3nm$$

Therefore,

$$t_{Hfo2} = 19.23nm$$

➢ Appendix

✧ Q1(c)

```
% Constants
epsilon_0 = 8.85e-14; % F/cm
epsilon_s = 11.9 * epsilon_0; % Permittivity of silicon
q = 1.6e-19; % Electron charge
NA = 1e16; % P-type doping concentration
ND = 1e18; % N-type doping concentration
Vbi = 0.84; % Built-in potential V
Vds = 0:0.1:3; % Voltage range from 0V to 3V

% Calculate depletion width
Wdep = sqrt(2 * epsilon_s * (Vbi + Vds) / q * (NA + ND) / (NA * ND));

% Plot graph
plot(Vds, Wdep);
xlabel('V_{DS} (V)');
ylabel('W_{dep} (cm)');
title('Depletion Width vs V_{DS}');
grid on;
```

✧ Q1(f)

```
% Define known parameters
Cj0 = 11.52e-15;  % Updated Cj0 value
Vbi = 0.84;       % Vbi value

% Define VDS range from 0 to 3V
VDS = linspace(0, 3, 100);

% Calculate Cj values
Cj = Cj0 ./ sqrt(1 + VDS / Vbi);

% Plot graph
figure;
plot(VDS, Cj, 'LineWidth', 2);
xlabel('V_{DS} (V)');
ylabel('C_j (F)');
title('Plot of C_j vs V_{DS}');
grid on;
```

✧ Q2(d)

```
% Define known parameters
mu_n = 0.037;  % Electron mobility, in m^2/Vs
Cox = 11.51e-3;  % Gate oxide capacitance, in F/m^2
```

```
W = 40e-6;  % Channel width, in meters
L = 0.15e-6;  % Channel length, in meters
V_T = 0.45;  % Threshold voltage, in V

% Define VDS range
VDS = linspace(0, 2.5, 100);

% Define different VGS values
VGS_values = [0.7, 1.0, 1.5, 2.0];

% Calculate IDS for each VGS value
figure;
hold on;
for VGS = VGS_values
    IDS = zeros(size(VDS));  % Initialize ID array
    for i = 1:length(VDS)
        if VDS(i) < VGS - V_T
            % Linear region equation
            IDS(i) = mu_n * Cox * (W/L) * ((VGS - V_T) * VDS(i) - 0.5 *
VDS(i)^2);
        else
            % Saturation region equation
            IDS(i) = 0.5 * mu_n * Cox * (W/L) * (VGS - V_T)^2;
        end
    end
    % Plot curve
    plot(VDS, IDS, 'LineWidth', 2, 'DisplayName', ['V_{GS} = '
num2str(VGS) ' V']);
end

% Set plot attributes
xlabel('V_{DS} (V)');
ylabel('I_{DS} (A)');
title('MOSFET Output Characteristics (I_{DS} vs V_{DS})');
legend('show');
grid on;
hold off;
```

✧ Q2(e)

```
% Define known parameters
mu_n = 0.037;  % Electron mobility, in m^2/Vs
Cox = 11.51e-3;  % Gate oxide capacitance, in F/m^2
W = 40e-6;  % Channel width, in meters
L = 0.15e-6;  % Channel length, in meters
```

```
V_T = 0.45;  % Threshold voltage, in V

% Define VGS range
VGS = linspace(0, 2, 100);

% Define different VDS values
VDS_values = [0.2, 1.0, 2.0];

% Calculate IDS for each VDS value
figure;
hold on;
for VDS = VDS_values
    IDS = zeros(size(VGS));  % Initialize ID array
    for i = 1:length(VGS)
        if VGS(i) > V_T
            % Linear region: VDS < VGS - VT
            if VDS < VGS(i) - V_T
                IDS(i) = mu_n * Cox * (W/L) * ((VGS(i) - V_T) * VDS -
0.5 * VDS^2);
            % Saturation region: VDS >= VGS - VT
            else
                IDS(i) = 0.5 * mu_n * Cox * (W/L) * (VGS(i) - V_T)^2;
            end
        else
            % When VGS <= VT, ID = 0
            IDS(i) = 0;
        end
    end
    % Plot curve
    plot(VGS, IDS, 'LineWidth', 2, 'DisplayName', ['V_{DS} = '
num2str(VDS) ' V']);
end

% Set plot attributes
xlabel('V_{GS} (V)');
ylabel('I_{DS} (A)');
title('MOSFET Transfer Characteristics (I_{DS} vs V_{GS})');
legend('show');
grid on;
hold off;
```