Integrated Electronics & Design

In-Class Test 2 (19th May 2017)
(2.5%)

Print Name:

ID No:

Signature:

Q1. The unit of the sheet resistance is:

(a) Ω

(b) Ω cm

(c) $cm^2/(V\ s)$

(d) Ω/

Q2. Resistance can be calculated: $R \equiv \rho \frac{L}{Wt} = \frac{\rho}{t} \frac{L}{W}$

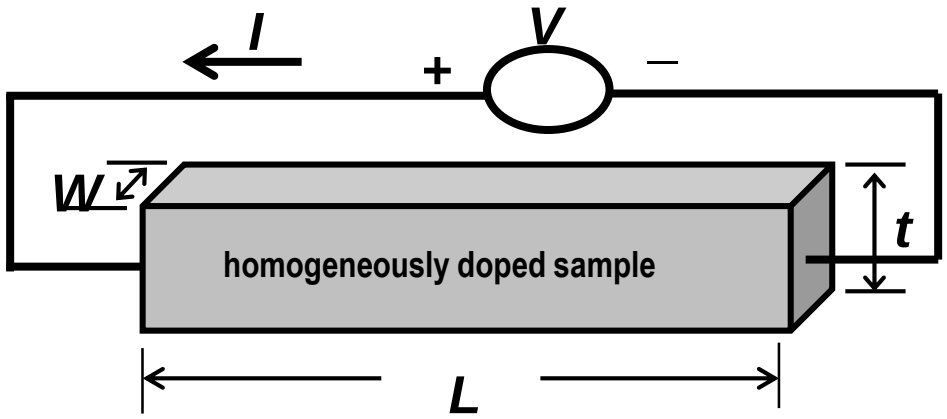
The sheet resistance is:

(a) *R*

(b) ρ

(c) ρ/t

(d) L/W



Q3. With respect to thermal oxidation (dry or wet), which statement or reaction below is NOT correct:

(a) SiO_2 formed by thermal oxidation is amorphous.

(b) $Si + O_2 \rightarrow SiO_2$ (900-1200°C)

(c) $Si + H_2O \rightarrow SiO_2 + 2H_2$ (900-1200°C)

(d) $SiH_4 + O_2 \rightarrow SiO_2 + 2H_2$ (300-600°C)

Q4. The drain current of an nMOSFET in the <u>saturation region</u> can be expressed as:

(a) $I_D(lin) = \frac{\mu_n C_{ox}}{2}\frac{W}{L}[2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$, $V_{GS} \geq V_T$ and $V_{DS} < V_{GS} - V_T$

(b) $I_D(sat) = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_T)^2$, $V_{GS} \geq V_T$ and $V_{DS} \geq V_{GS} - V_T$

(c) $I_D(sat) = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_T)^2$, $V_{GS} \geq V_T$ and $V_{DS} < V_{GS} - V_T$

(d) $I_D(lin) = \frac{\mu_n C_{ox}}{2}\frac{W}{L}[2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$, $V_{GS} \geq V_T$ and $V_{DS} \geq V_{GS} - V_T$

Q5. With respect to thermal oxidation, which statement below is NOT correct:

(a) Thermal SiO_2 is amorphous.

(b) Thermal SiO_2 is a good diffusion mask for common dopants.

(c) There is a very good etching selectivity between Si and thermal SiO_2.

(d) Thermal SiO_2 does not react with hydrofluoric (HF) acid.

Q6. The drain current of an nMOSFET in the <u>linear region</u> can be expressed as:

(a) $I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}[2(V_{GS}-V_T)V_{DS}-V_{DS}^2],\ \ V_{GS} \geq V_T$ and $V_{DS} < V_{GS}-V_T$

(b) $I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS}-V_T)^2,\qquad V_{GS} \geq V_T$ and $V_{DS} \geq V_{GS}-V_T$

(c) $I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS}-V_T)^2,\qquad V_{GS} \geq V_T$ and $V_{DS} < V_{GS}-V_T$

(d) $I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}[2(V_{GS}-V_T)V_{DS}-V_{DS}^2],\ \ V_{GS} \geq V_T$ and $V_{DS} \geq V_{GS}-V_T$

Q7. With respect to chemical vapor deposition (CVD), which statement below is NOT correct:

(a) CVD can be performed at atmospheric pressure or at low pressure.

(b) There is no chemical reaction involved in CVD.

(c) Thin film formation from vapor phase reactants is called CVD.

(d) CVD is an essential process step in the manufacturing of microelectronic devices.

Q8. With respect to physical vapor deposition (PVD), which statement below is NOT correct:

(a) The common techniques for PVD are evaporation and ion beam sputtering.

(b) Only physical reaction is involved in PVD.

(c) Thin film formation from vapor phase reactants is called PVD.

(d) PVD is an essential process step in the manufacturing of microelectronic devices.

Q9. With respect to glass photomasks, which statement below is NOT correct:

(a) A glass photomask includes opaque regions and translucent regions.
(b) The material of the opaque regions is chromium.
(c) Projected ultraviolet (UV) light can go through the opaque regions of the glass mask.
(d) Project ultraviolet (UV) light can go through the translucent regions of the glass mask.

Q10. With respect to photoresists, which statement below is NOT correct:

(a) There are two kinds of photoresists: positive resist and negative resist.
(b) Spin coating is a process to apply a photoresist on a wafer.
(c) For a negative resist, the regions exposed to ultraviolet light are insoluble to an organic solvent in the development step.
(d) For a negative resist, the regions exposed to ultraviolet light are soluble to an organic solvent in the development step.

Q11. With respect to photolithography, which statement below is NOT correct:

(a) The photolithographic process is a process of using ultraviolet (UV) light to transfer patterns from a glass mask onto the surface of a wafer.

(b) The typical photolithographic process steps are: (1) applying photoresist on a wafer, (2) placing a glass mask in close proximity of the wafer, (3) UV light exposure, and (4) development.

(c) Development is a process to dissolve the unexposed negative resist.

(d) Development is a process to dissolve the exposed negative resist.

Q12. With respect to etching, which statement below is NOT correct:

(a) Etching is a process to remove a thin film unprotected by photoresist away from semiconductor substrate by using chemical or physical method.

(b) There are three commonly used thin films: dielectric thin films (SiO_2, Si_3N_4), metal thin films (Al, Cu), and conductor thin films (poly-Si).

(c) The SiO_2 thin film can be etched away in hydrofluoric (HF) acid.

(d) The poly-Si thin film can be etched away in hydrofluoric (HF) acid.

Q13. With respect to doping, which statement below is NOT correct:

(a) There are two commonly used doping techniques: thermal diffusion and ion implantation.

(b) There are two steps to thermal diffusion: predeposition and drive-in.

(c) To activate implanted ions and to restore crystal damages during ion implantation, the semiconductor must be annealed

(d) Only gas sources, such as AsH_3, PH_3 and B_2H_6, can be used for thermal diffusion. Solid sources and liquid sources cannot be used for thermal diffusion.

Q14. According to the MOSIS (metal oxide semiconductor implementation system) layout design rules, which statement on metal rules below is NOT correct:

(a) Minimum metal width is 3λ.

(b) Minimum metal spacing is 3λ.

(c) Minimum metal spacing is 1λ.

(d) Minimum separation from active contact to metal edge is 1λ.

Q15. According to the MOSIS (metal oxide semiconductor implementation system) layout design rules, which statement on polysilicon rules below is NOT correct:

(a) Minimum polysilicon width is 2λ.

(b) Minimum polysilicon spacing is 2λ.

(c) Minimum separation from active contact to poly edge is 1λ.

(d) Minimum gate extension of poly over active area is 2λ.

Q16. According to the MOSIS (metal oxide semiconductor implementation system) layout design rules, which statement on active area rules below is NOT correct:

(a) Minimum active area width is 3λ.

(b) Minimum active area width is 4λ.

(c) Minimum active area spacing is 3λ.

(d) Minimum separation from active contact to active area edge is 1λ.

Q17. According to the MOSIS (metal oxide semiconductor implementation system) layout design rules, which statement on active contact rules below is NOT correct:

(a) Minimum active contact size is 2λ.

(b) Minimum active contact spacing on the same active region is 2λ.

(c) Minimum separation from active contact to active area edge is 1λ.

(d) Minimum separation from active contact to metal edge is 6λ.

Q18. According to the MOSIS (metal oxide semiconductor implementation system) layout design rules, which statement on poly contact rules below is NOT correct:

(a) Minimum poly contact size is 2λ.

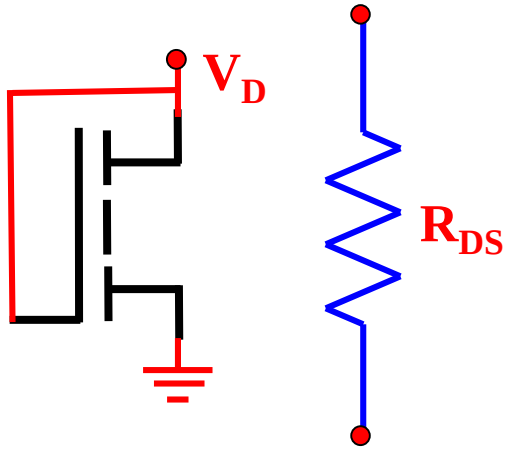
(b) Minimum poly contact spacing is 2λ.

(c) Minimum separation from poly contact to poly edge is 1λ.

(d) Minimum separation from poly contact to metal edge is 6λ.

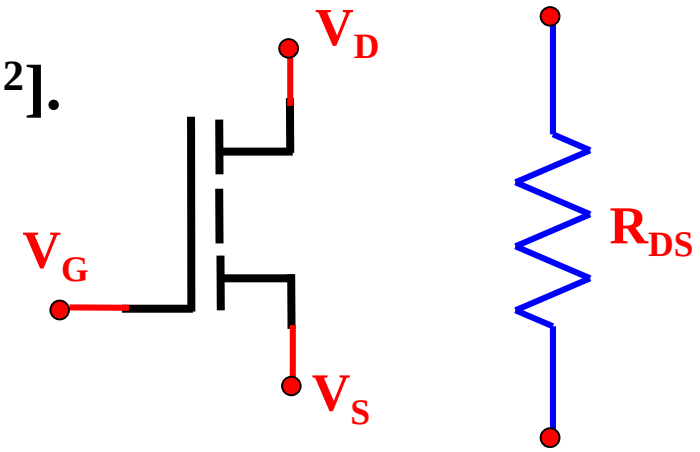
Q19. The resistance of the load MOSFET is:

(a) ∞.
(b) 0.
(c) $R_{DS} = 2V_D / [\mu(W/L) C_{ox} (V_D - V_T)^2]$.
(d) $R_{DS} = 1 / [\mu(W/L) C_{ox} (V_{GS} - V_T)]$.



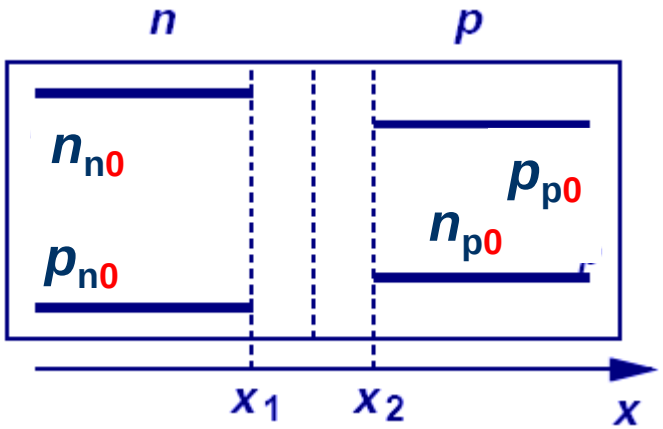
Q20. For small V_{DS} ($V_{DS} << V_{GS} - V_T$), the resistance of the load MOSFET is:

(a) ∞.
(b) 0.
(c) $R_{DS} = 2V_D / [\mu(W/L) C_{ox} (V_D - V_T)^2]$.
(d) $R_{DS} = 1 / [\mu(W/L) C_{ox} (V_{GS} - V_T)]$.

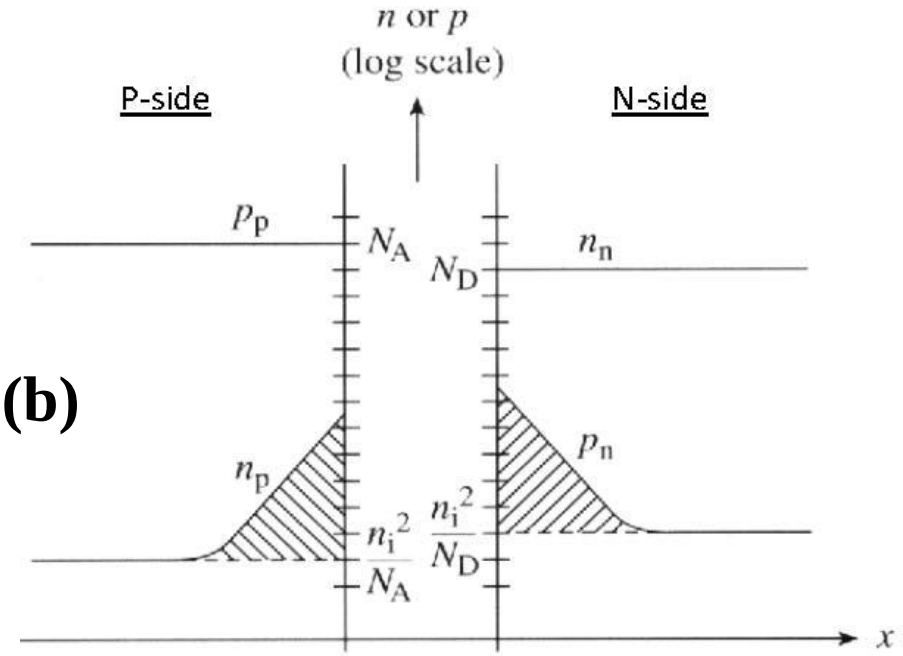


Q21. Carrier concentration profiles of a PN junction diode are shown in below, which one is under reverse bias:

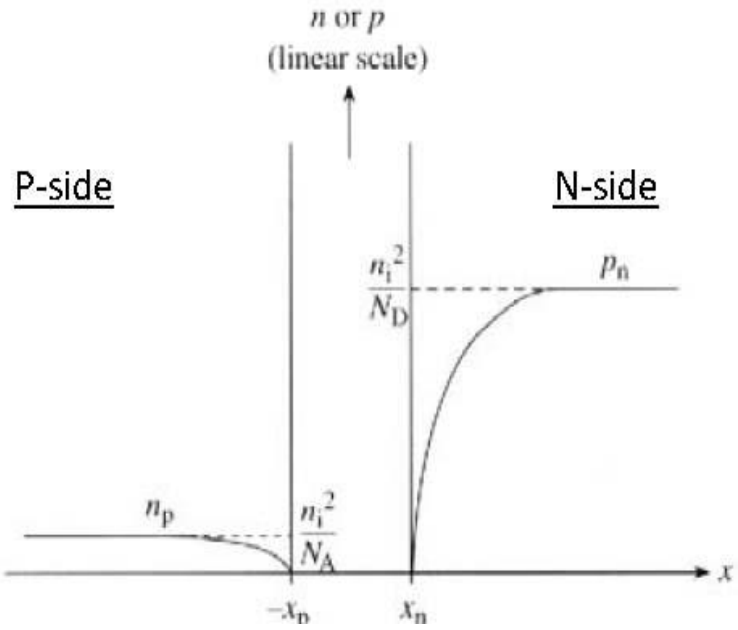
(a)



(b)

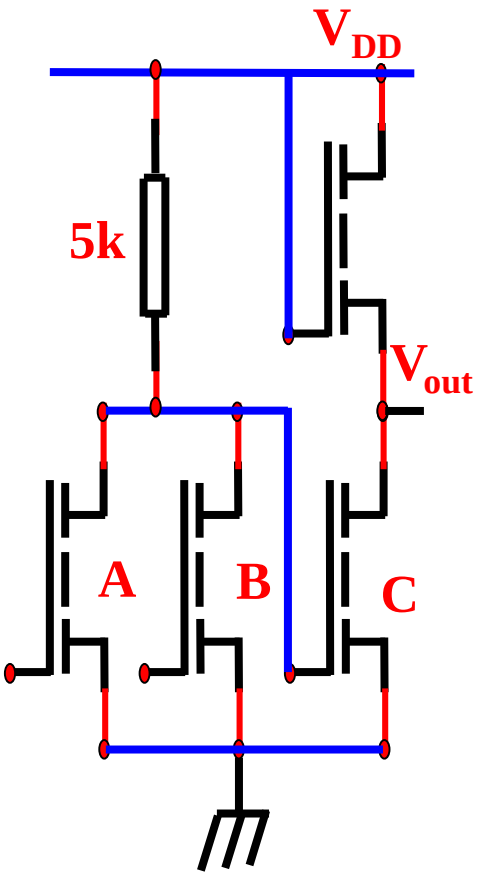


(c)

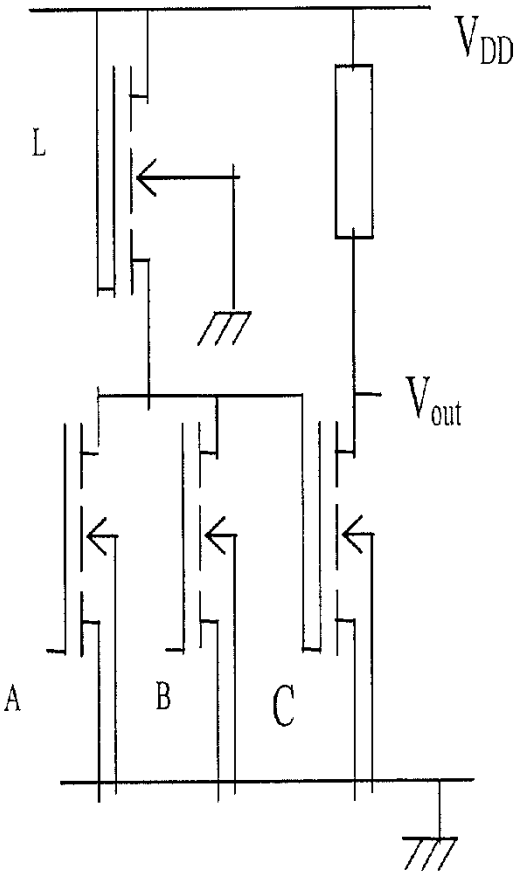


Q22. Four logic circuits are shown in below, which one is the inverter?

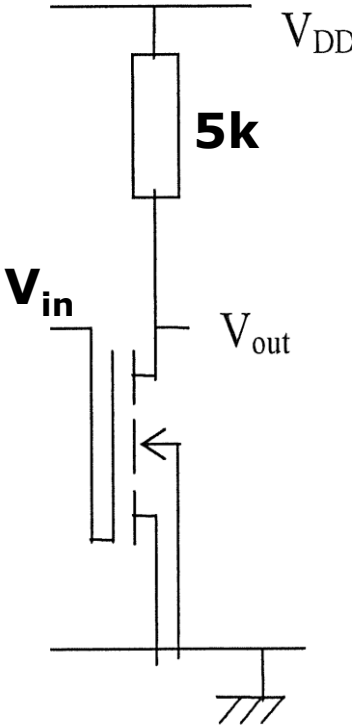
(a)



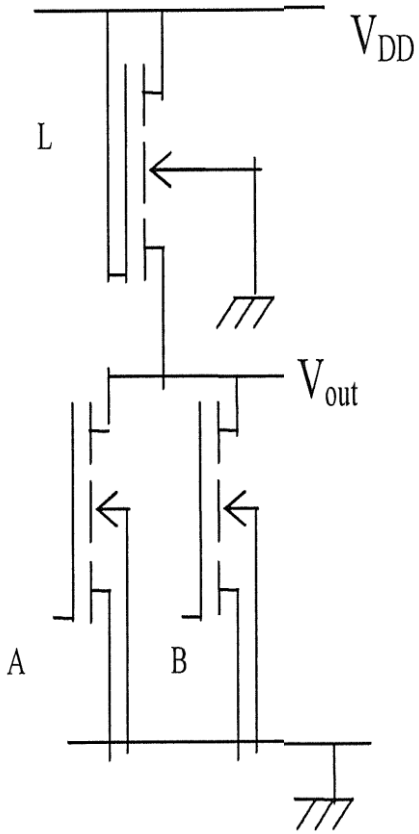
(b)



(c)

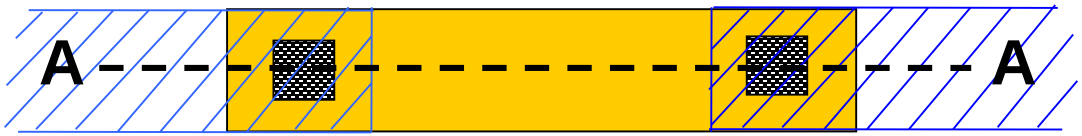


(d)

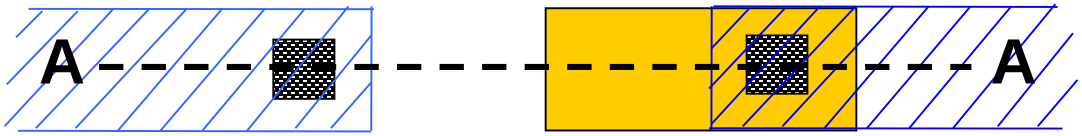


Q23. The layout of a pn junction diode is:

(a)



(b)

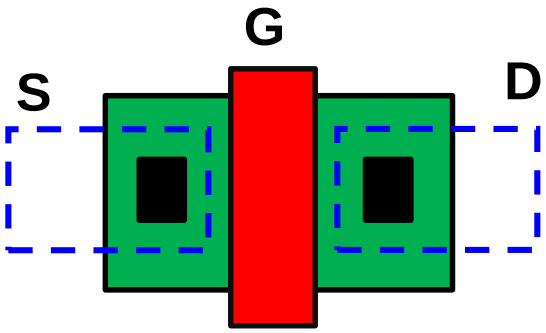


Oxide mask (dark field)

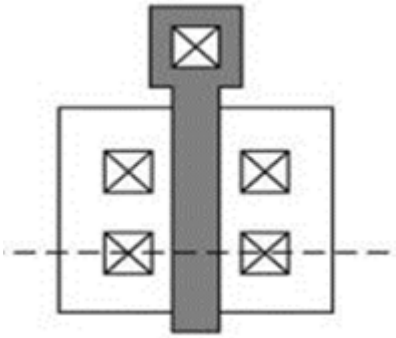
Contact mask (dark field)

Al mask (clear field)

(c)

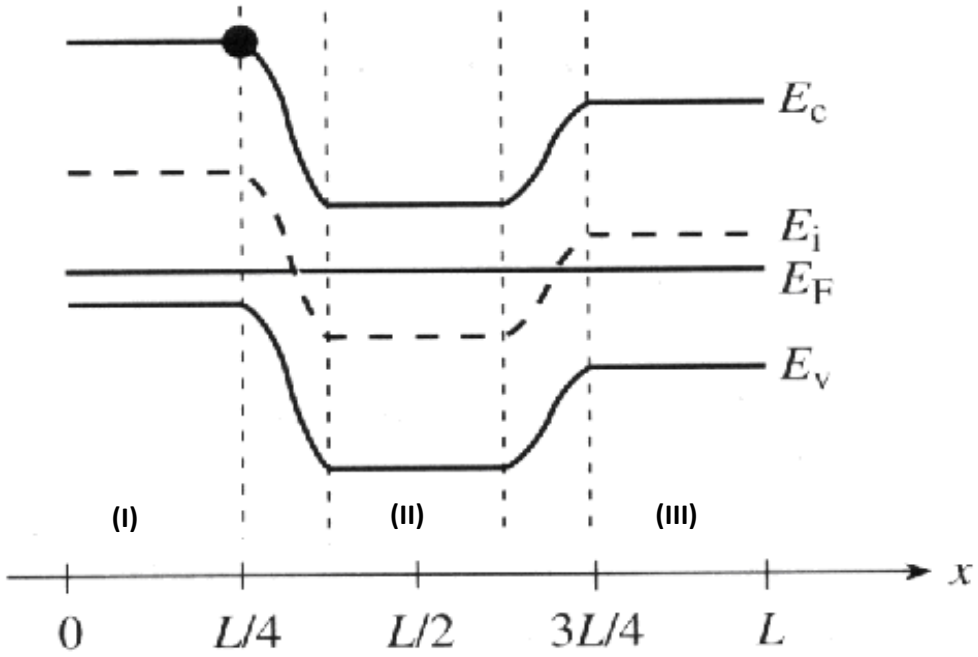


(d)



Q24. A silicon sample maintained at T=300K is characterized by the energy band diagram below. Is the sample in equilibrium conditions? Is it a pnp or npn structure?

(a) Yes. It's a pnp structure.
(b) No. It's a pnp structure.
(c) Yes. It's a npn structure.
(d) No. It's a npn structure.



Q25. The drain current of an nMOSFET can be expressed as:

(a) $I_D(lin) = \frac{\mu_n C_{ox}}{2}\frac{W}{L}[2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$, $V_{GS} \geq V_T$ and $V_{DS} < V_{GS} - V_T$

$I_D(sat) = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_T)^2$, $V_{GS} \geq V_T$ and $V_{DS} \geq V_{GS} - V_T$

(b) $I_D(lin) = \frac{\mu_n C_{ox}}{2}\frac{W}{L}[2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$, $V_{GS} < V_T$ and $V_{DS} < V_{GS} - V_T$

$I_D(sat) = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_T)^2$, $V_{GS} < V_T$ and $V_{DS} \geq V_{GS} - V_T$

(c) $I_D(lin) = \frac{\mu_n C_{ox}}{2}\frac{W}{L}[2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$, $V_{GS} \geq V_T$ and $V_{DS} \geq V_{GS} - V_T$

$I_D(sat) = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_T)^2$, $V_{GS} \geq V_T$ and $V_{DS} < V_{GS} - V_T$

(d) $I_D(lin) = \frac{\mu_n C_{ox}}{2}\frac{W}{L}[2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$, $V_{GS} < V_T$ and $V_{DS} < V_{GS} - V_T$

$I_D(sat) = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_T)^2$, $V_{GS} \geq V_T$ and $V_{DS} \geq V_{GS} - V_T$