Plan for the following weeks

W9: Multi-stage Amplifiers for Integrated Circuits

W10: Ideal Operational Amplifier Circuits ← HW3 release

W11: Nonideal Effects in Operational Amplifiers + Feedback on HW2 ← HW3 deadline

W12: Revision1 ← HW3 cut-off

W13: Revision2+Feedback on HW3 (Lab 2)

Office: SC429

Office Hours: Thursday, 2-4 pm

Email: Xiaoyang.Chen02@xjtlu.edu.cn

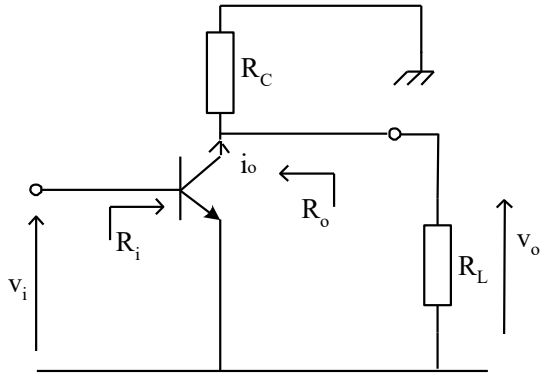
Multi-Stage Amplifiers for Integrated Circuits

Dr. Xiaoyang Chen

Part 1: Basic Building Blocks in Multi-Stage Circuits

1. Basic Amplifiers (with Load Resistor)

- **Common Emitter**



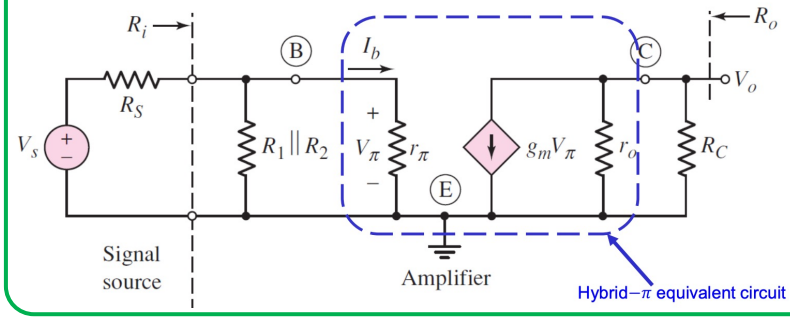
$$R_i = r_\pi$$

$$R_o = R_C||r_o \approx R_C$$

$$A_v = \frac{v_o}{v_i} = -g_m R_C||R_L||r_o \approx -g_m R_C||R_L$$

Usage: Gain stage

W3 P7

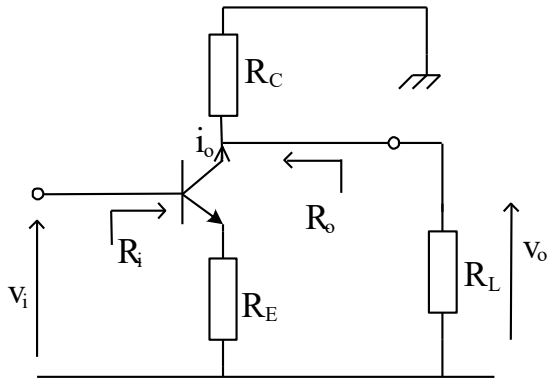


The output voltage can be written as, $V_o = -g_m V_\pi (r_o||R_C)$

The control voltage V_π is found to be, $V_\pi = \frac{R_1||R_2||r_\pi}{R_1||R_2||r_\pi + R_S} \times V_s$

Thus, the small-signal voltage gain is, $A_v = \frac{V_o}{V_s} = -g_m(r_o||R_C)\frac{R_1||R_2||r_\pi}{R_1||R_2||r_\pi + R_S}$

- **Common Emitter with Emitter Resistor (Degradation)**



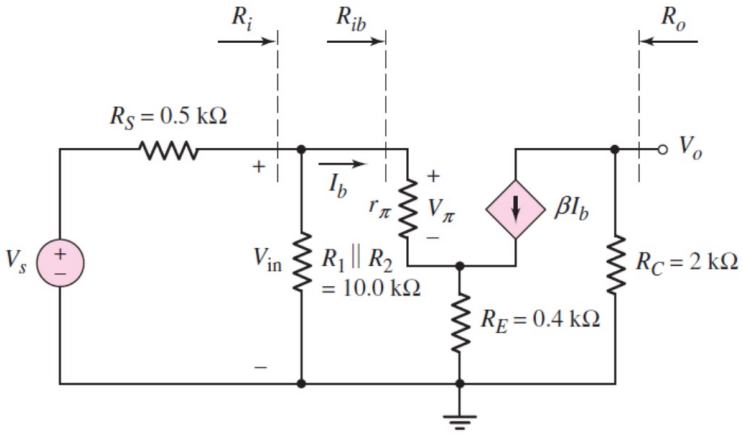
$$R_i = r_\pi + (1+\beta)R_E$$

$$R_o = R_C || r_o \approx R_C$$

$$A_v = -\frac{g_m R_C || R_L}{1 + g_m R_E}$$

Usage: R_E gives increased stability; Gain stage

W3 P9



Voltage gain A_v:

The output voltage is, $V_o = -(\beta I_b)\, R_C$

The input resistance to the amplifier, $R_i = R_1 || R_2 || R_{ib}$

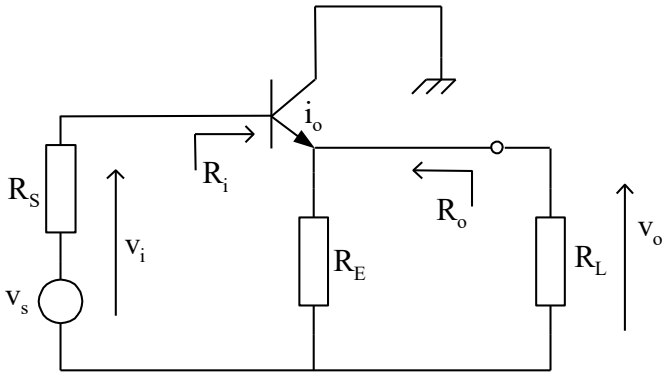
Moreover, $V_{in} = \left(\frac{R_i}{R_i + R_S}\right) V_s$

Therefore, $A_v = \frac{V_o}{V_s} = \frac{-(\beta I_b)\, R_C}{V_s} = -\beta R_C \left(\frac{V_{in}}{R_{ib}}\right)\left(\frac{1}{V_s}\right) = \frac{-\beta R_C}{r_\pi + (1+\beta)R_E}\left(\frac{R_i}{R_i + R_S}\right)$

Input resistance R_{ib}: It is the input resistance looking into the base

Use KVL for the loop, $V_{in} = I_b r_\pi + (I_b + \beta I_b) R_E \rightarrow R_{ib} = \frac{V_{in}}{I_b} = r_\pi + (1+\beta)R_E$

- **Common Collector (Emitter Follower)**



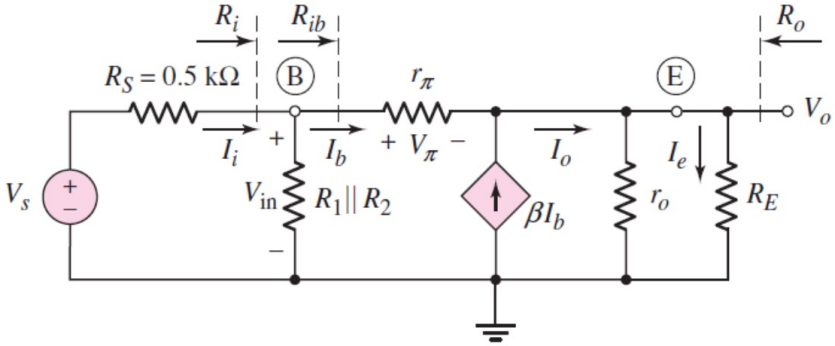
$$R_i = r_\pi + (1+\beta)R_E||R_L \quad \text{High}$$

$$R_o = \frac{r_\pi + R_S}{1+\beta}||R_E \quad \text{Low}$$

$$A_v = \frac{g_m R_E||R_L}{1+g_m R_E||R_L} \quad \text{Low}$$

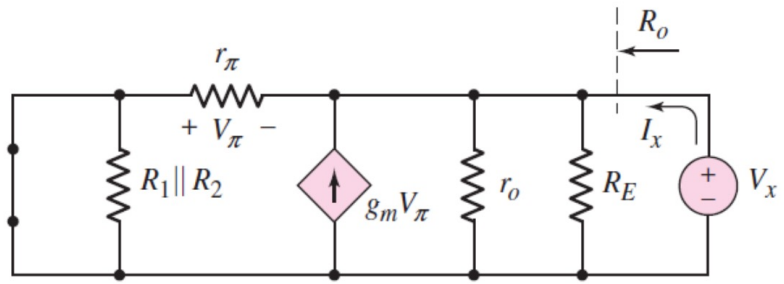
Usage: Impedance matching; Buffer ★

W3 P15-17



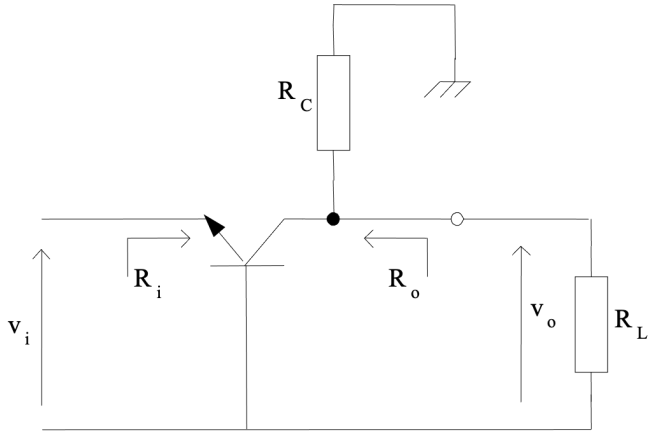
$$R_{ib} = \frac{V_{in}}{I_b} = r_\pi + (1+\beta)(r_o||R_E)$$

$$A_v = \frac{V_o}{V_s} = \frac{(1+\beta)(r_o||R_E)}{r_\pi+(1+\beta)(r_o||R_E)}\left(\frac{R_i}{R_i+R_S}\right)$$



$$R_o = \frac{V_x}{I_x} = \frac{1}{g_m}||R_E||r_o||r_\pi$$

- **Common Base**



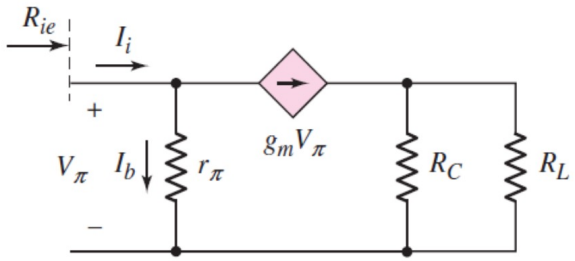
$$R_i = \frac{r_\pi}{1+\beta} \approx \frac{1}{g_m} = r_e \quad \text{Low}$$

$$R_o = R_C \quad \text{High}$$

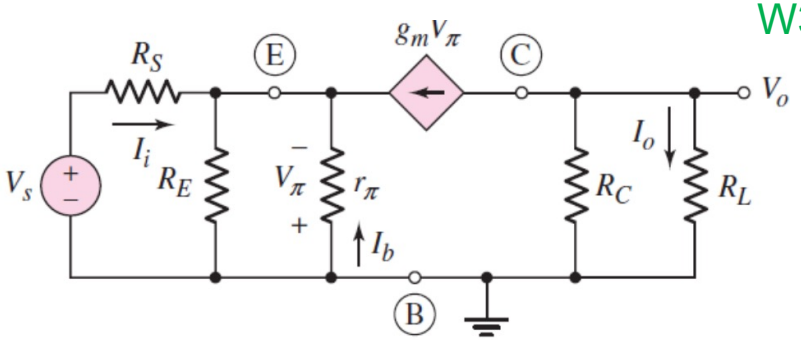
$$A_v = g_m R_C || R_L \quad \text{High}$$

Usage: Impedance matching

W3 P21-23

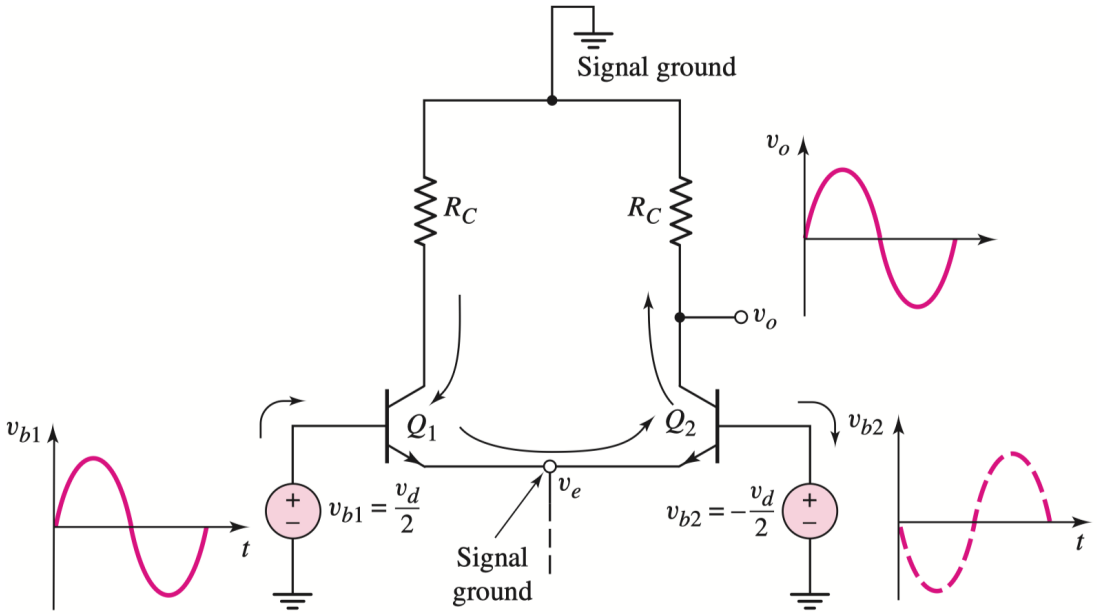


$$R_{ie} = \frac{V_\pi}{I_i} = \frac{r_\pi}{1+\beta} \equiv r_e$$



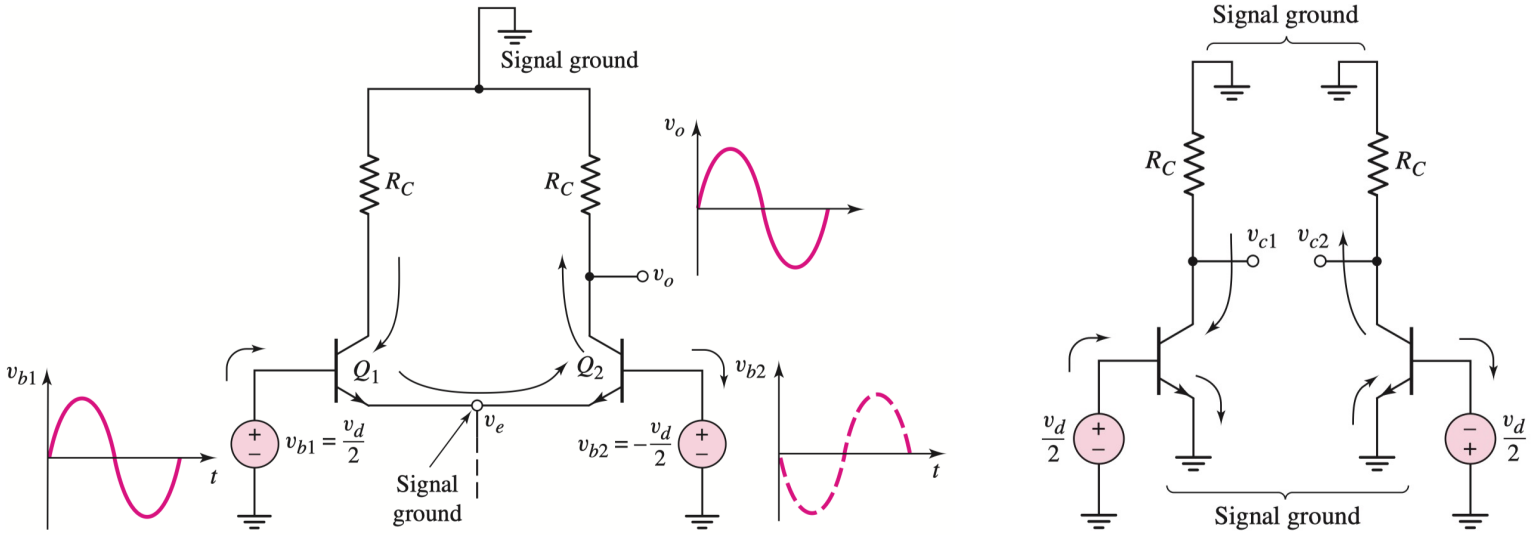
$$A_v = \frac{V_o}{V_s} = g_m \left(\frac{R_C || R_L}{R_S}\right) \left[\left(\frac{r_\pi}{1+\beta}\right) || R_E || R_S\right]$$

2. Differential Amplifier



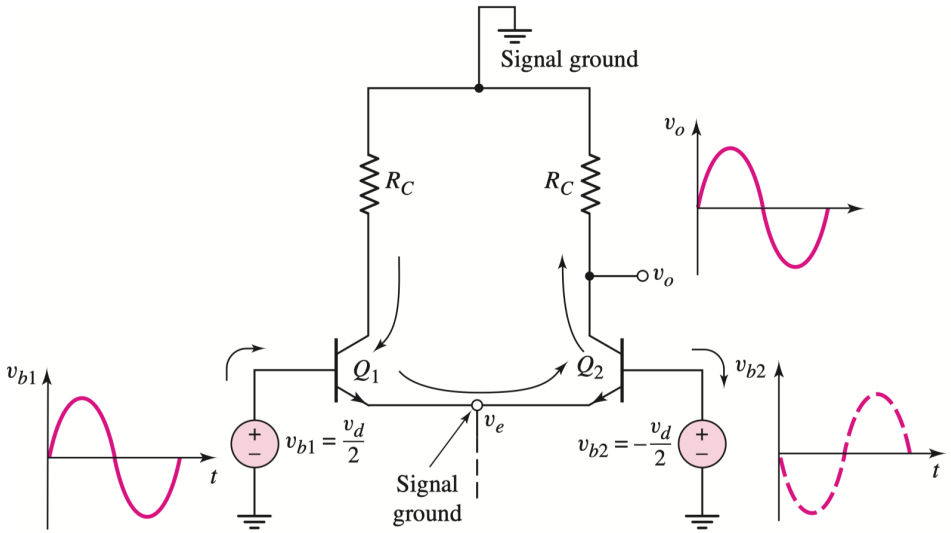
- Although the diff-amp contains two transistors, it is considered as an individual module in IC design.
- A diff-amp has characteristics very similar to a CE amplifier
- Usage: Input stage to virtually all multi-stage amplifiers and integrated circuits

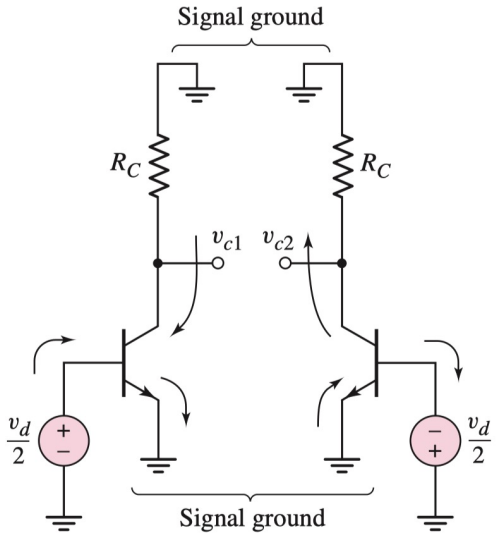
AC equivalent circuit for differential-mode input signal



- With differential-mode input, we have $v_e = 0$, so the emitters of Q1 and Q2 remain at signal ground
- Since v_e is always at ground potential, we can treat each half of the diff-amp as a CE circuit
- The differential-mode characteristics of the diff-amp can be determined by analyzing the half circuit

Properties (Differential Mode)





$$R_i = \frac{v_d}{i_b} = 2 \cdot \frac{\frac{v_d}{2}}{i_b} = 2r_\pi$$

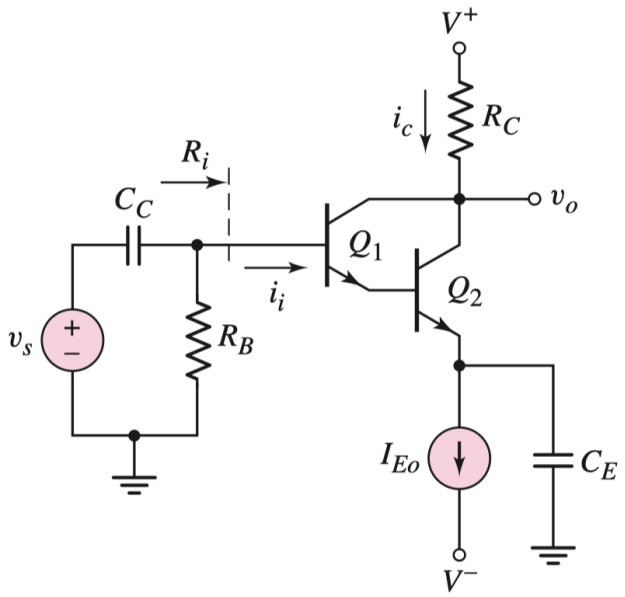
W4 P23

$$R_o = \frac{v_o}{i_o} = R_C || r_o$$

$$A_v = \frac{v_o}{v_i} = \frac{v_o}{v_d} = -\frac{1}{2} \cdot \frac{v_o}{-\frac{v_d}{2}} = -\frac{1}{2} \cdot A_v(CE) \approx \frac{g_m R_C}{2}$$

Must Remember!

3. Darlington Pair Configuration



- It's a multi-transistor configuration. In ICs, we consider the Darlington Pair as an individual building block
- Usage: Gain stage

Small signal equivalent circuit W3 P32

We see that $V_{\pi 1} = I_i r_{\pi 1}$, hence

$$g_{m1} V_{\pi 1} = g_{m1} r_{\pi 1} I_i = \beta_1 I_i$$

Then, $V_{\pi 2} = (I_i + \beta_1 I_i) r_{\pi 2}$, and we can write:

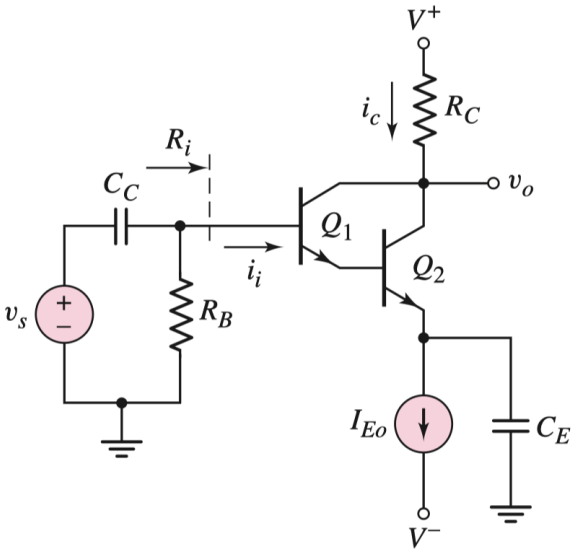
$$V_i = V_{\pi 1} + V_{\pi 2} = I_i r_{\pi 1} + I_i (1 + \beta_1) r_{\pi 2}$$

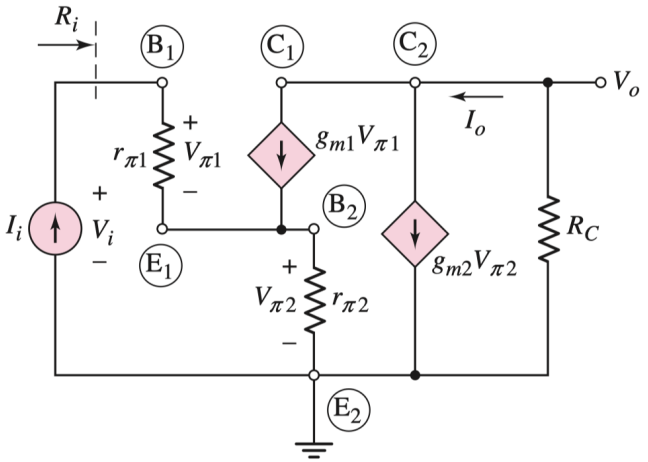
so that the input resistance is:

$$R_i = \frac{V_i}{I_i} = r_{\pi 1} + (1 + \beta_1) r_{\pi 2}$$

The output resistance can be easily found by:

$$R_o = \frac{V_o}{I_o} = R_C || r_o \approx R_C$$





Small signal equivalent circuit

For a Darlington Pair, the current gain is:

$$A_i = \frac{I_o}{I_i} \approx \beta_1\beta_2$$

Hence we have $I_o = I_i \cdot \beta_1\beta_2$

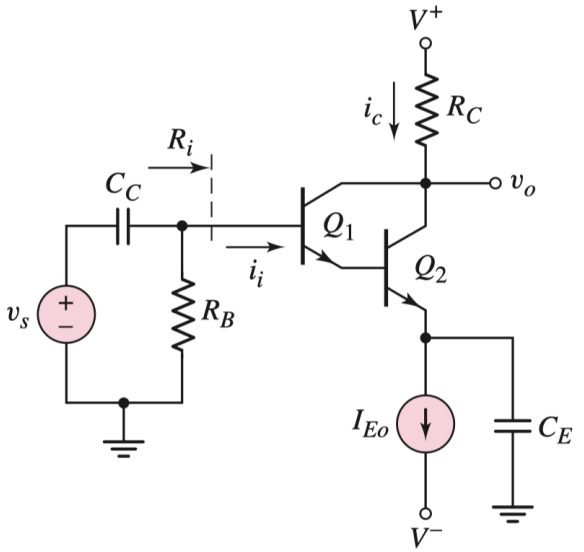
The voltage gain then can be found by:

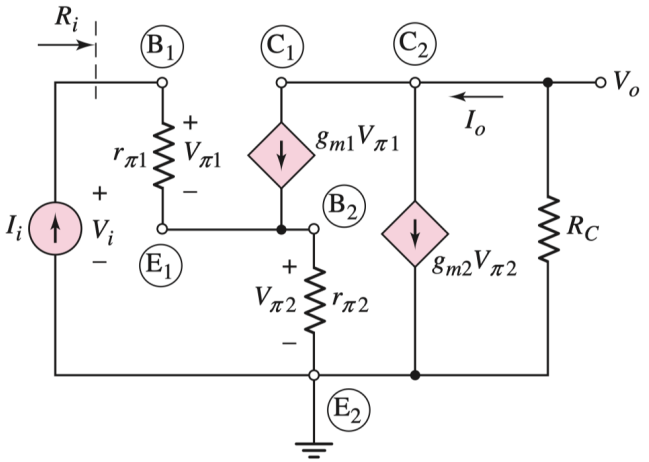
$$A_v = \frac{V_o}{V_i} = \frac{I_o R_o}{I_i R_i} = \frac{I_i \cdot \beta_1\beta_2 \cdot R_C}{I_i(r_{\pi1} + (1+\beta_1)r_{\pi2})}$$

$$= \frac{\beta_1\beta_2 \cdot R_C}{r_{\pi1} + (1+\beta_1)r_{\pi2}} \approx \frac{\beta_1\beta_2 \cdot R_C}{r_{\pi1} + \beta_1 r_{\pi2}}$$

If we have two identical transistors, then

$$A_v = \frac{\beta_1\beta_2 \cdot R_C}{r_{\pi1} + \beta_1 r_{\pi2}} = \frac{\beta^2 R_C}{r_{\pi1} + \beta r_{\pi2}}$$



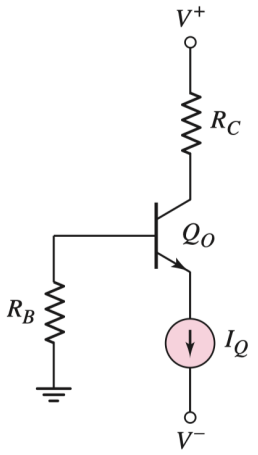


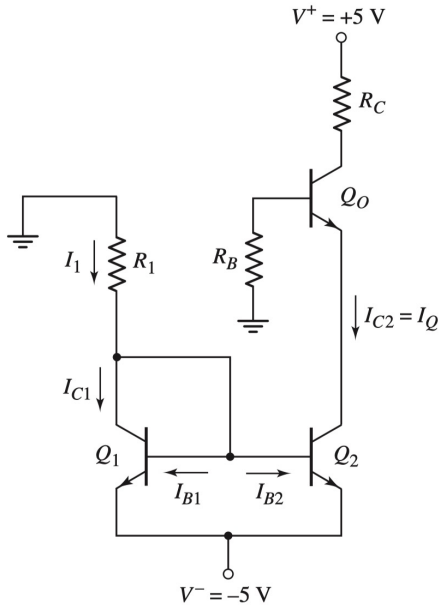
4. Active Loads

- When a bipolar transistor is used as a linear amplifying device, it must be biased in the forward-active mode.
- In discrete circuits, biasing are basically achieved with resistor biasing.
- In integrated circuits, we would like to eliminate as many resistors as possible because they require larger surface area than transistors.
- A bipolar transistor can be biased by using a constant-current source I_Q.

Advantages:

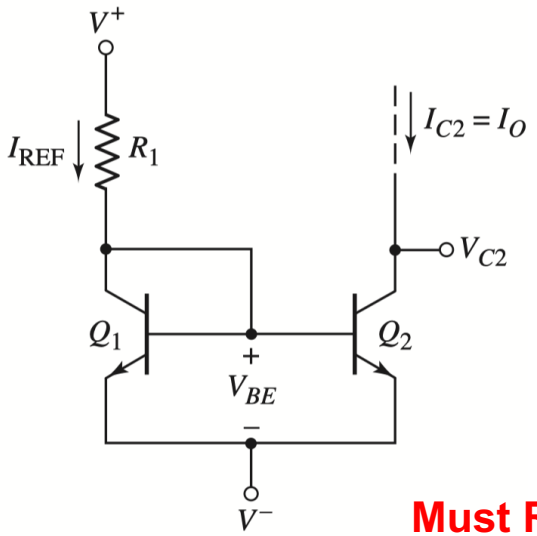
- The emitter current is independent of β and R_B
- The collector current are essentially independent of β
- The value of R_B can be increased, thus increasing the input resistance at the base, without disturbing the bias stability





Current mirror circuits

Basic two transistor current source



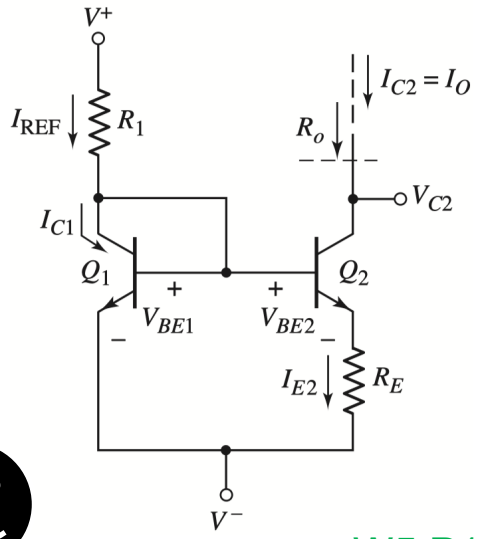
W5 P7, 10

$$I_{C2} = I_o = \frac{I_{REF}}{1 + \frac{2}{\beta}} \approx I_{REF}$$

$$R_o = r_{o2}$$

Must Remember!

Widlar current source

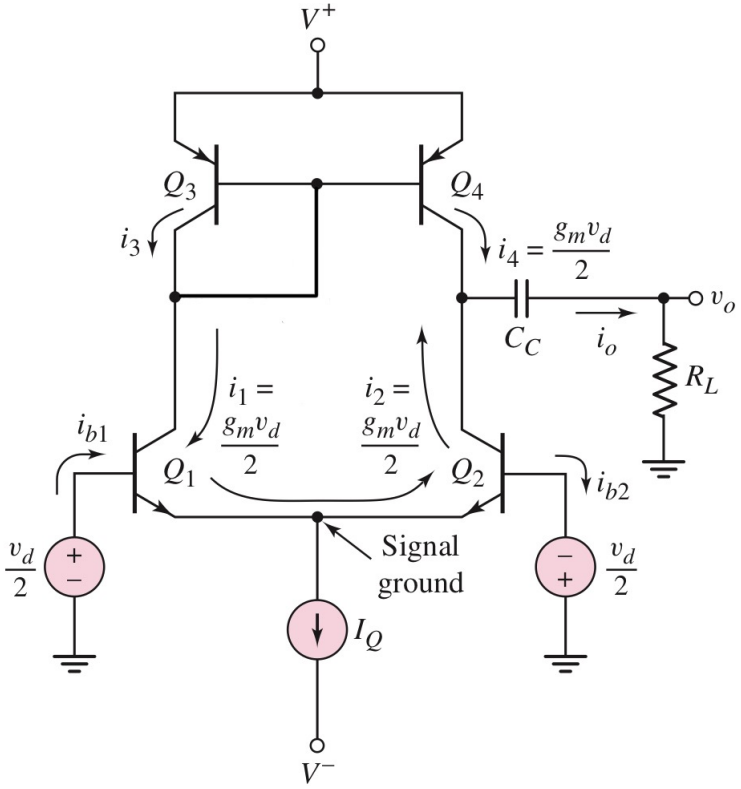


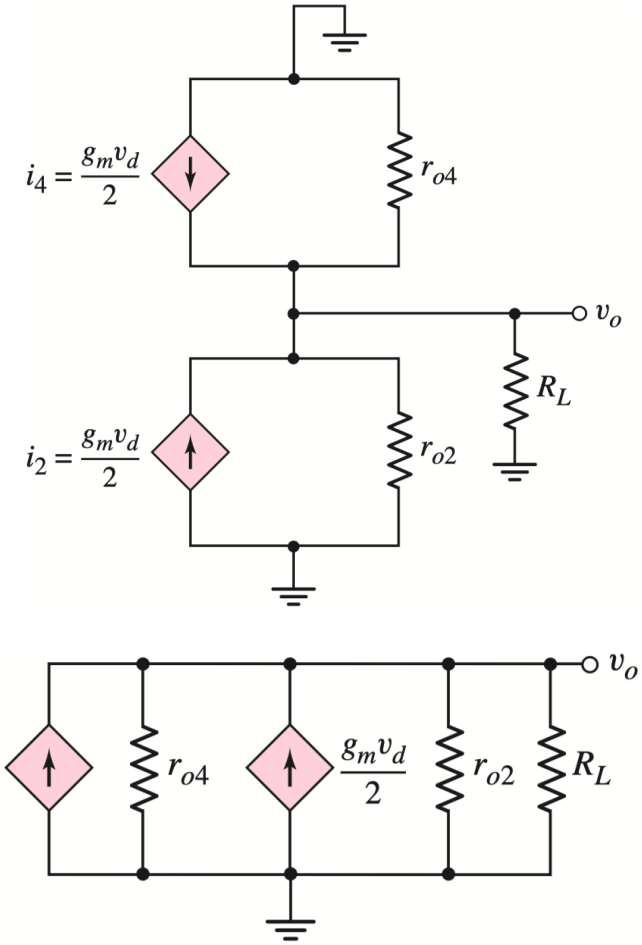
W5 P18, 21

$$I_o R_E = V_T \ln\left(\frac{I_{REF}}{I_o}\right)$$

$$R_o \approx r_{o2}(1 + g_{m2} R_E)$$

Differential amplifier with active load





$$A_v = g_m(r_{o2} \parallel r_{o4} \parallel R_L)$$

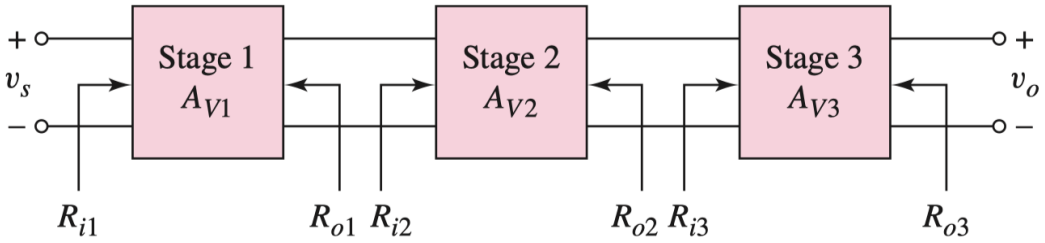
$$R_o = r_{o2} \parallel r_{o4} \parallel R_L$$

W5 P27

Must Remember!

Part 2: Multi-Stage Amplifier Circuits Analysis

Main Principles



1. Perform the DC analysis of the circuit to determine the small-signal parameters of the transistors. In most cases the base currents can be neglected. This assumption will normally provide sufficient accuracy for a hand analysis.

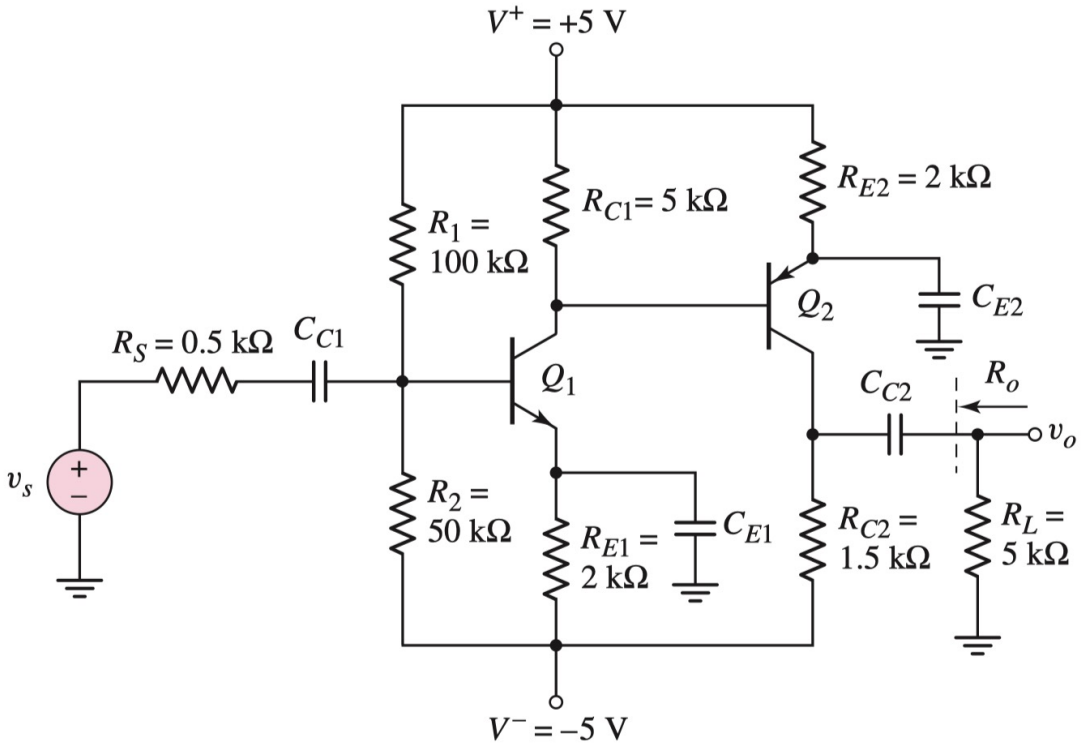
2. Perform the AC analysis on each stage of the circuit, taking into account the loading effect of the following stage.

   The properties of the previous stage (e.g., output resistance) can be a function of the input resistance (load) of the next stage, and vice versa.

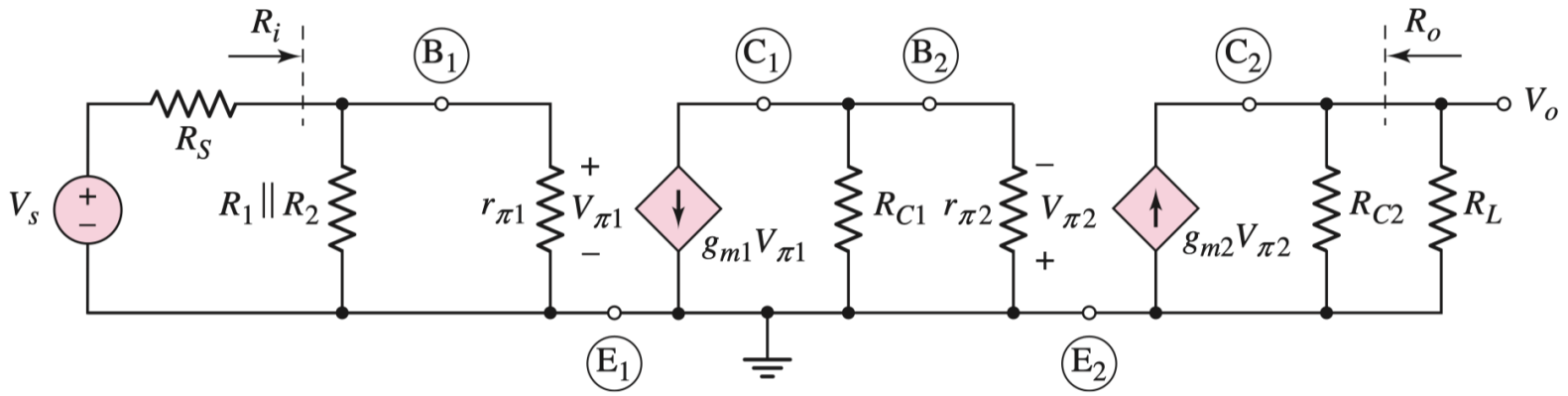
3. The overall small-signal voltage gain is the product of the gains of each stage as long as the loading effect is taken into account.

Example 1 (Revisit)

Find the mathematical expression of the overall voltage gain for the amplifier shown below ($V_A = \infty$).



Solution (traditional small-signal equivalent circuit approach):



According to the two-stage small-signal equivalent circuit, we have:

$$A_V = \frac{V_o}{V_s} = \frac{V_o}{V_{\pi 2}} \times \frac{V_{\pi 2}}{V_{\pi 1}} \times \frac{V_{\pi 1}}{V_s} \quad \text{(Chain rule)}$$

$$\frac{V_{\pi 1}}{V_s} = \frac{R_i}{R_S + R_i}$$

and

$$g_{m2}V_{\pi 2}R_{C2}||R_L = V_o \Longrightarrow \frac{V_o}{V_{\pi 2}} = g_{m2}R_{C2}||R_L$$

$$g_{m1}V_{\pi 1}R_{C1}||r_{\pi 2} = V_{\pi 2} \Longrightarrow \frac{V_{\pi 2}}{V_{\pi 1}} = g_{m1}R_{C1}||r_{\pi 2}$$

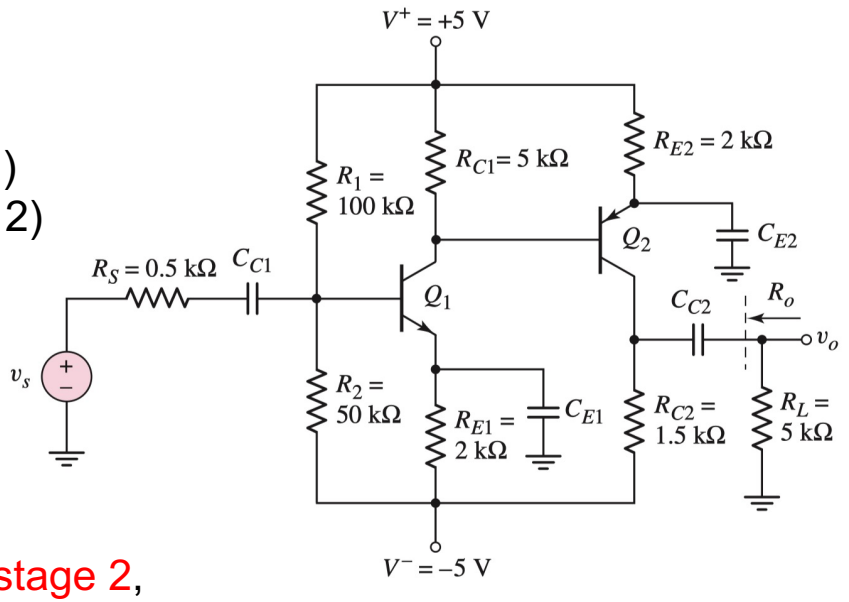
Therefore:

$$A_V = g_{m1}g_{m2}(R_{C1}||r_{\pi 2})(R_{C2}||R_L)\left(\frac{R_i}{R_i + R_S}\right)$$

where $R_i = R_1||R_2||r_{\pi 1}$

Solution (applying loading effect):

This amplifier is composed of two stages
- A CE amplifier at the input with Q1 (stage 1)
- A CE amplifier at the output with Q2 (stage 2)



Stage 1:

According to the formula sheet, we have:

$$A_{v1} = -g_{m1}R_{C1}||R_{L1}$$

In this case, R_{L1} is just the input resistance of stage 2, then we have:

$$R_{L1} = R_{i2} = r_{\pi 2}$$

Hence: $A_{v1} = -g_{m1}R_{C1}||r_{\pi 2}$

Stage 2:

$$A_{v2} = -g_{m2}R_{C2}||R_L$$

Therefore, the overall voltage gain can be found as:

$$A_V = \frac{v_o}{v_s} = g_{m1}g_{m2}(R_{C1}||r_{\pi 2})(R_{C2}||R_L)\left(\frac{R_i}{R_i + R_S}\right)$$

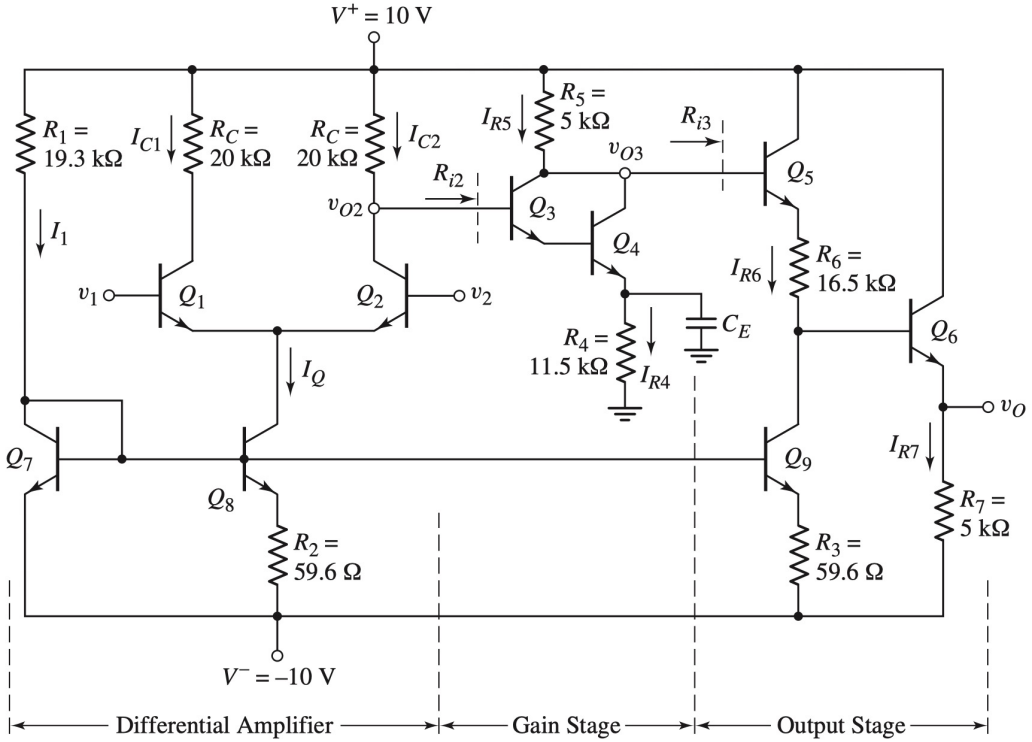
where $R_i = R_1||R_2||r_{\pi 1}$

Example 2

Consider the circuit shown below. Assume $V_{BE}(on) = 0.7\ V$ for all transistors.

a) Perform DC analysis and find the currents: $I_1, I_Q, I_{C1}, I_{C2}, I_{R4}, I_{R5}, I_{R6}$, and I_{R7} (Neglect base currents)

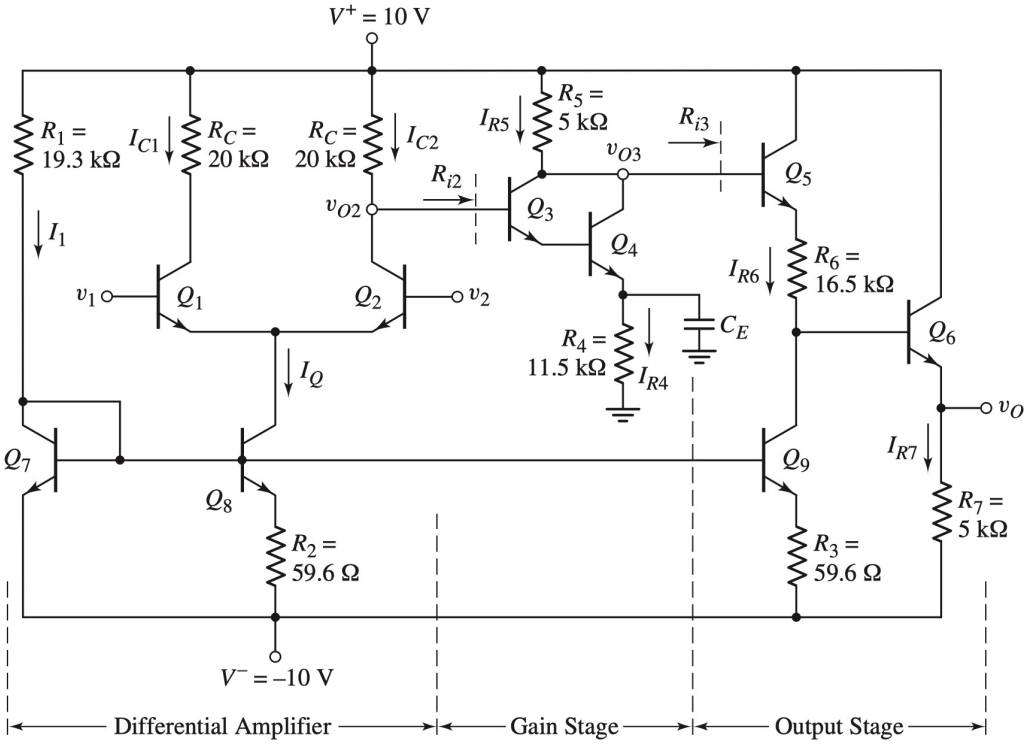
b) Determine the small signal voltage gain of the circuit, assuming $\beta = 100$ and $V_A = \infty$



Solution a):

The circuit is composed of three stages

- A differential amplifier biased by a Widlar current source (stage 1)
- A gain stage with a Darlington pair (stage 2)
- An output circuit with CC (stage 3)



The reference current I_1 is:

$$I_1 = \frac{V^+ - 0.7 - V^-}{R_1} = 1\,mA$$

The bias current I_Q is found by:

$$I_Q R_2 = V_T \ln\left(\frac{I_1}{I_Q}\right) \longrightarrow I_Q = 0.4\,mA$$

The collector currents are then:

$$I_{C1} = I_{C2} = \frac{1}{2} I_Q = 0.2\,mA$$

The DC voltage at the collector of Q2 is:

$$V_{O2} = V^+ - I_{C2} R_C = 6\,V$$

The current I_{R4} is then determined to be:

$$I_{R4} = \frac{V_{O2} - 2V_{BE}(on)}{R_4} = 0.4\,mA$$

Solution a):

Since base currents are negligible, we have: $I_{R5} \approx I_{R4} = 0.4\,mA$

The DC voltage at the collectors of Q3 and Q4 is then:

$$V_{O3} = V^+ - I_{R5}R_5 = 8\,V$$

Since $R_2 = R_3$, we have:

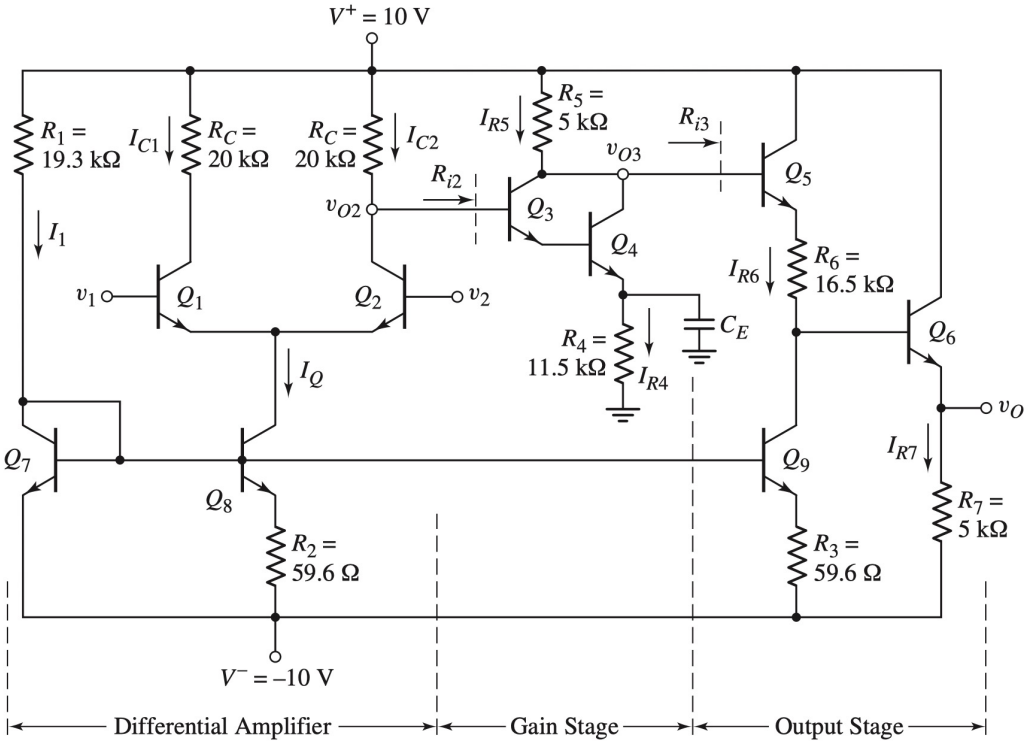
$$I_{R6} = I_Q = 0.4\,mA$$

The DC voltage at the base of Q6 is found to be:

$$V_{B6} = V_{O3} - V_{BE}(on) - I_{R6}R_6 = 0.7\,V$$

Finally, current I_{R7} is:

$$I_{R7} = \frac{V_O - V^-}{R_7} = \frac{0 - (-10)}{5} = 2\,mA$$



This produces $V_O = 0\,V$. This is desired as a zero differential-mode voltage is now applied (DC analysis)

Solution b):

Taking the loading resistance into account, the overall small-signal gain is the product of the individual stage gains: $A_V = A_{V1} \cdot A_{V2} \cdot A_{V3}$

Stage 1:

The differential-mode voltage gain is:

$$A_{V1} = \frac{g_m(R_C||R_{L1})}{2}$$

In this case,

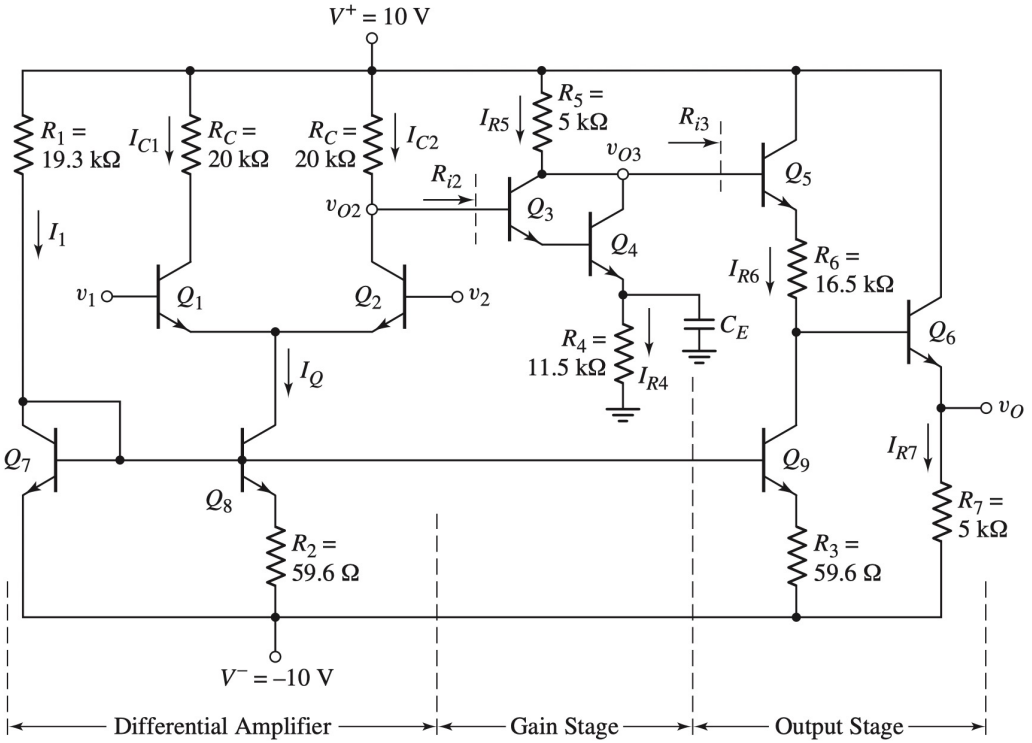
$$R_{L1} = R_{i2} = r_{\pi 3} + (1+\beta)r_{\pi 4}$$

where $r_{\pi 4} = \frac{\beta V_T}{I_{R4}} = 6.5\ k\Omega$

and $r_{\pi 3} \approx \frac{\beta^2 V_T}{I_{R4}} = 650\ k\Omega$

Therefore, $R_{i2} = 1307\ k\Omega$

The transconductance is $g_m = \frac{I_Q}{2V_T} = 7.7\ mA/V$



The gain of stage 1 is therefore:

$$A_{V1} = \left(\frac{7.7}{2}\right)(20||1307) = 75.8$$

Solution b):

Stage 2:

For the Darlington pair, the voltage gain is:

$$A_{V2} = \frac{\beta^2(R_5||R_{L2})}{r_{\pi 3} + \beta r_{\pi 4}}$$

In this case,

$$R_{L2} = R_{i3} = r_{\pi 5} + (1+\beta)(R_6 + R_{iQ6})$$

and $R_{iQ6} = r_{\pi 6} + (1+\beta)R_7$

We find that

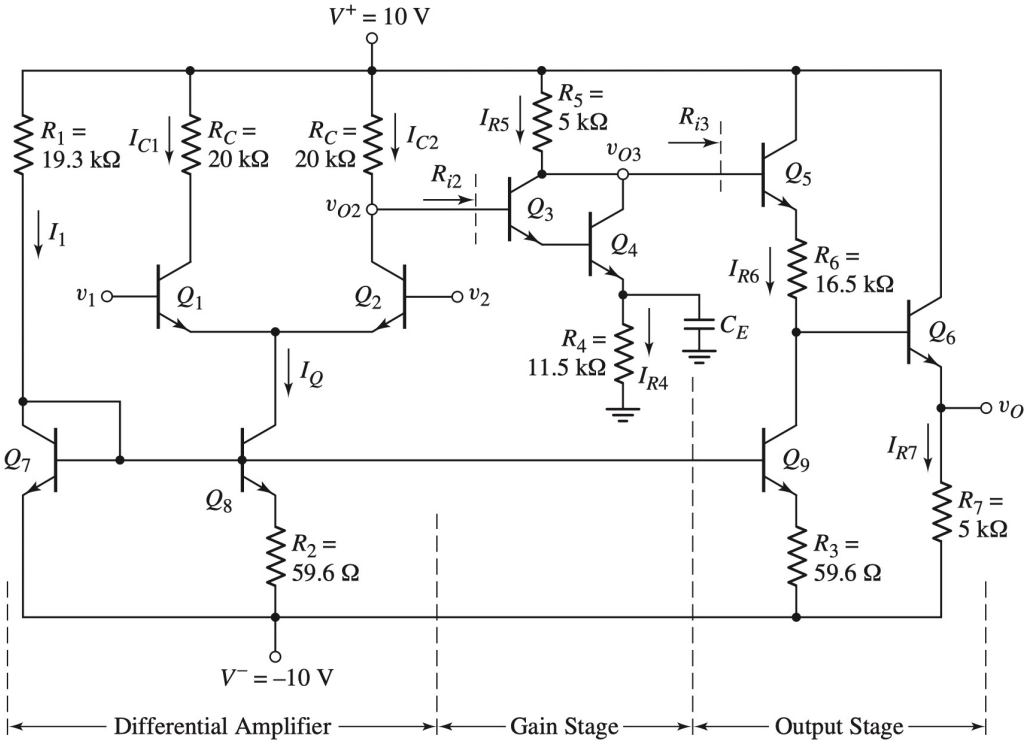
$$r_{\pi 5} = \frac{\beta V_T}{I_{R6}} = 6.5\ k\Omega \text{ and } r_{\pi 6} = \frac{\beta V_T}{I_{R7}} = 1.3\ k\Omega$$

Therefore, $R_{i3} = 52.8\ M\Omega$

The input resistance of CC is very large, so the loading effect can be ignored

Hence,

$$A_{V2} = 38.5$$



Solution b):

Stage 3:

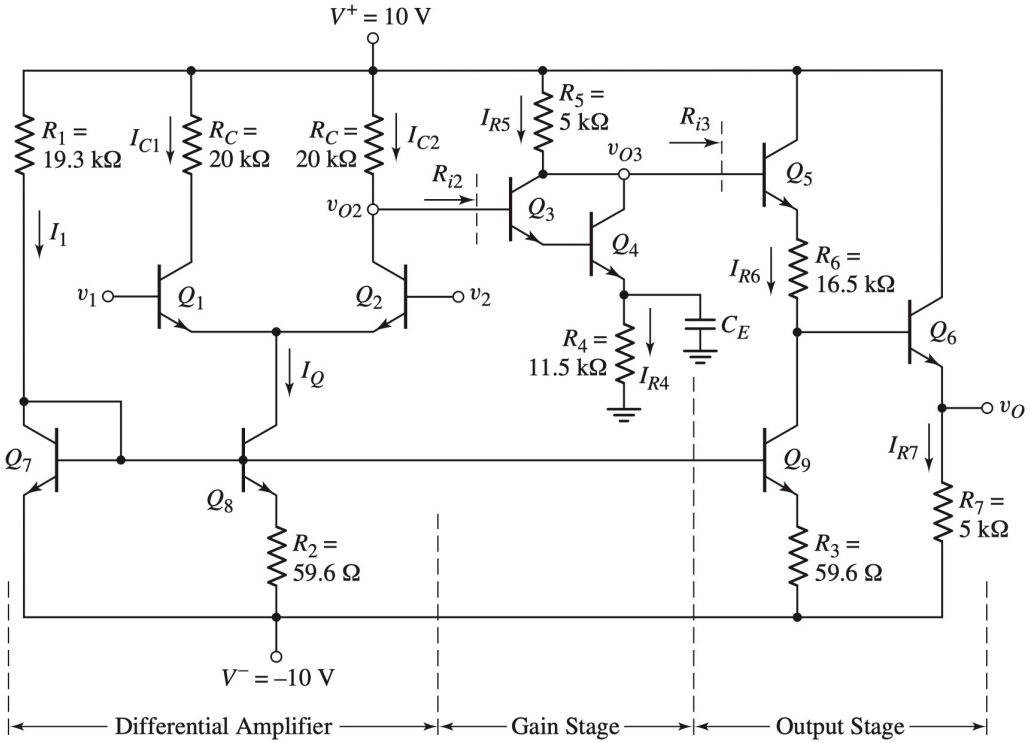
The output stage is a CC formed by Q5 and Q6, whose gain is:

$A_{V3} \approx 1$

CC acts like a good buffer to isolate two stages

The overall small-signal voltage gain is therefore:

$$A_V = A_{V1} \cdot A_{V2} \cdot A_{V3} = 2918$$

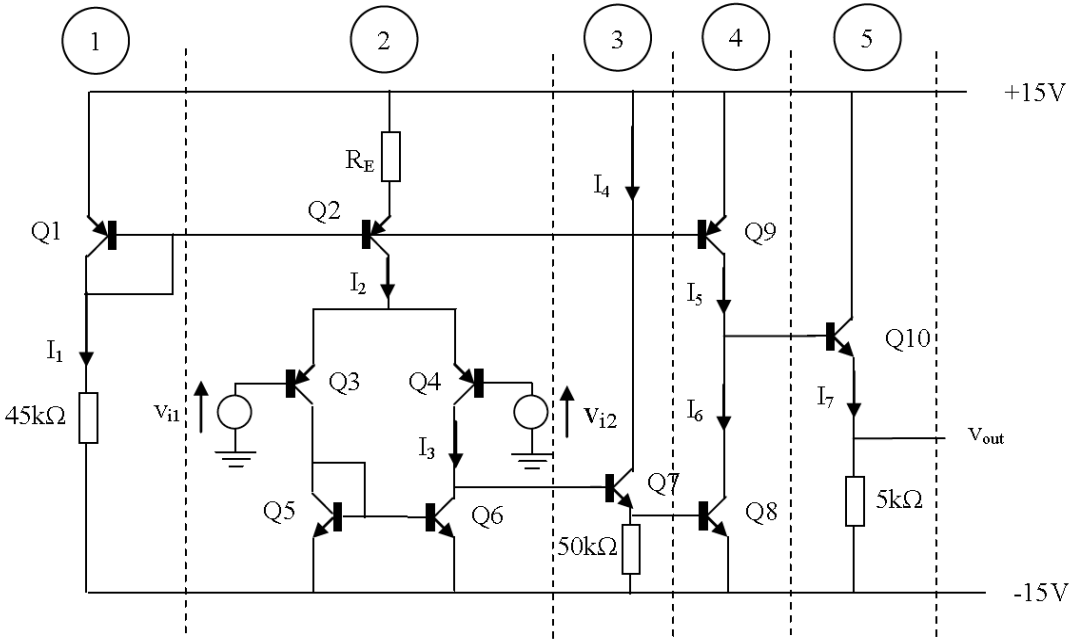


Example 3

Consider the multi-stage voltage amplifier shown below (labelled by 5 stages):

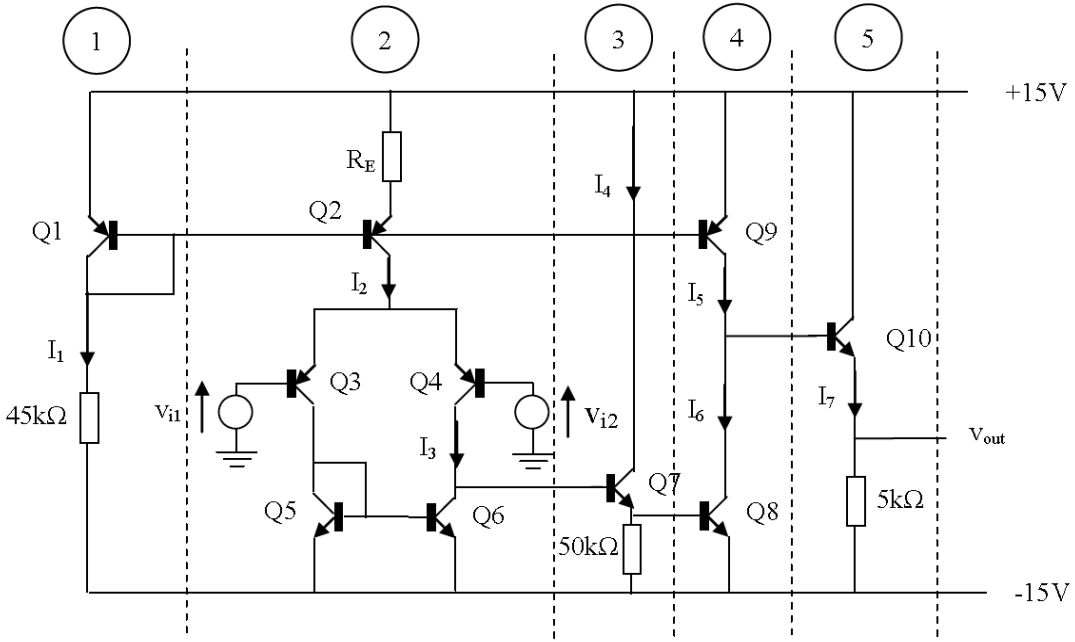
a) Briefly describe the function of each of the 5 stages

b) If $I_2 = 0.1$ mA, make reasonable approximations to estimate the total current drawn by the circuit from the ± 15 V DC voltage supply when the amplifier is biased so that the DC value of $V_{out} = 0$ V and the ac input signals are zero ($V_{BE}(on) = 0.6$ V).



c) Assuming $I_2 = 0.1$ mA, make reasonable approximations to estimate the overall small signal voltage gain of the circuit. Assume all transistors have a current gain $\beta = 100$ and Early voltage -100 V.

Solution a):



Stage 1 is the bias current section, which forms a Widlar current mirror with Q2 and a basic current mirror with Q9

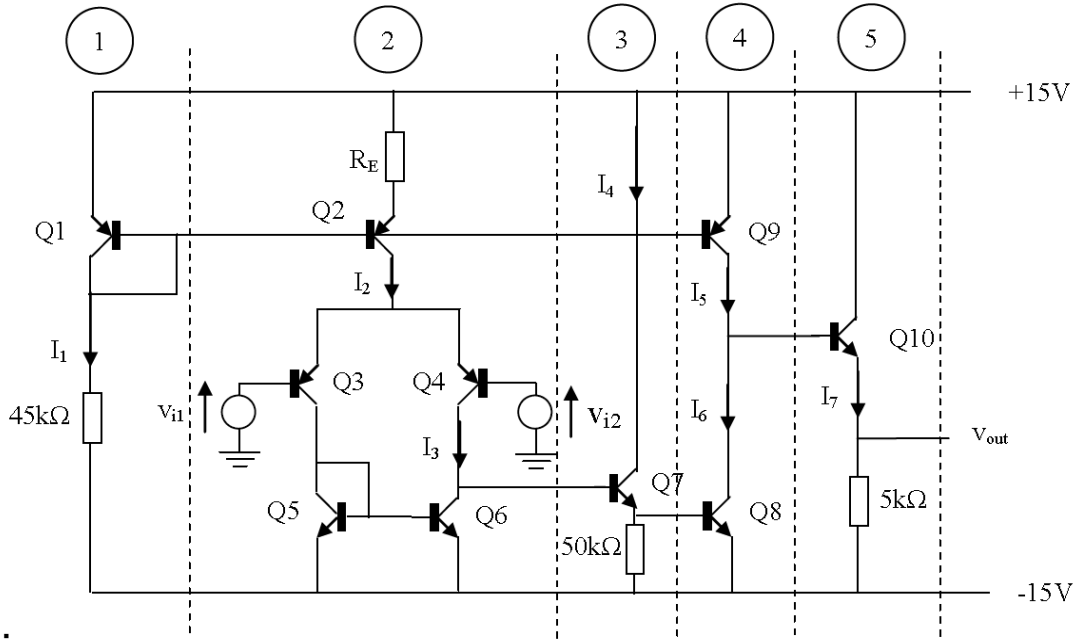
Stage 2 is a differential amplifier with active load. It forms the input of the circuit and provides the first voltage gain

Stage 3 is an emitter-follower (CC) circuit forming an impedance matching buffer between stages 2 and 4. It also reduces the loading effect.

Stage 4 is a CE amplifier with current mirror as active load that significantly contributes to the overall voltage gain.

Stage 5 is a CC circuit forming the output stage and reducing loading effect.

Solution b):



At stage 1, we have:

$$I_1 = \frac{V^+ - 0.6 - V^-}{45} = 0.653\ mA$$

From the current mirror, we have:

$$I_5 = I_1 = 0.653\ mA$$

$$I_4 = \frac{0.6}{50} = 0.012\ mA$$

Since we have $V_{out} = 0\ V$, we have:

$$I_7 = \frac{0 - (-15)}{5} = 3\ mA$$

Therefore, the total current drawn from the source is:

$$I_{total} = I_1 + I_2 + I_4 + I_5 + I_7 = 4.42\ mA$$

Solution c):

Stage 1:

Stage 1 is a bias reference, and <u>will not</u> contribute to the overall voltage gain

Stage 2:

For a differential amplifier with active loads, we have:

$$A_{v2} = g_{m4}(r_{o4}||r_{o6}||R_{L2})$$

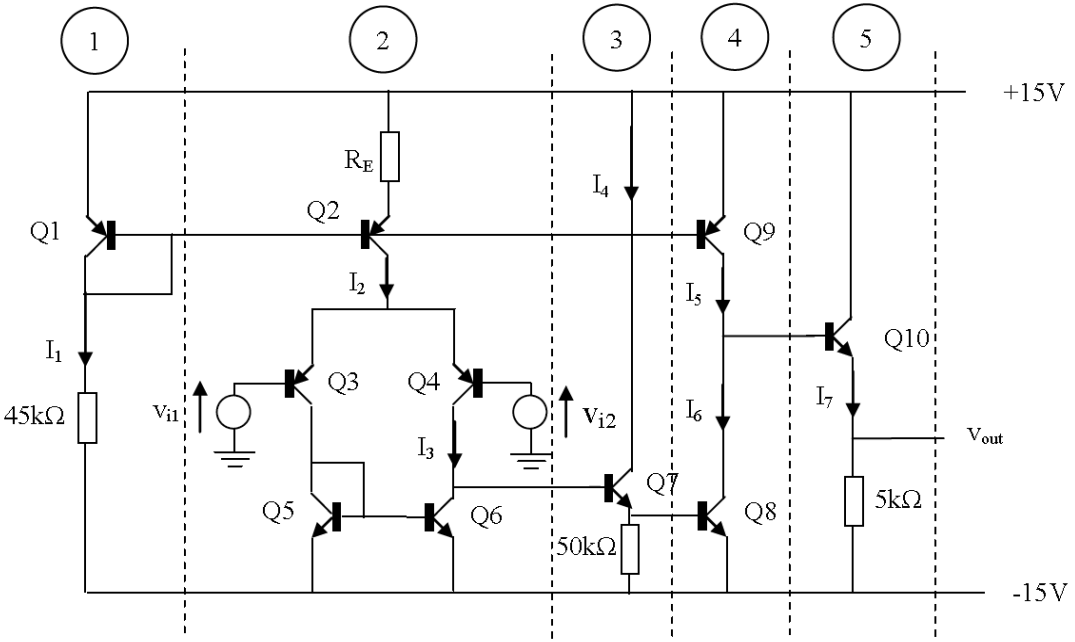
where

$$R_{L2} = R_{i3} = r_{\pi 7} + (1+\beta)50||R_{L3}$$

and $R_{L3} = R_{i4} = r_{\pi 8}$

Then we have:

$$g_{m4} = \frac{I_{CQ4}}{V_T} = \frac{I_2}{2V_T} = 2\ mA/V$$



$$r_{o4} = r_{o6} = \frac{100}{0.5I_2} = 2000\ k\Omega$$

$$r_{\pi 7} = \frac{\beta}{g_{m7}} = \frac{\beta}{40I_4} = 208\ k\Omega$$

At the base of Q10, we have:

$$I_6 = I_5 - \frac{I_7}{\beta} = 0.623\ mA$$

Therefore:

$$R_{L3} = r_{\pi 8} = \frac{\beta}{40I_6} \approx 4\ k\Omega$$

$$R_{L2} \approx 582\ k\Omega$$

and

$$\underline{A_{V2} \approx 736}$$

Solution c):

Stage 3:

Stage 3 is a CC circuit with $\underline{A_{V3} = 1}$

Stage 4:

For a CE amplifier, we have:

$A_{V4} = -g_{m8}(R_{L4}||r_{o8}||r_{o9})$

(Here $R_C = r_{o9}$)

where $R_{L4} = R_{i5}$

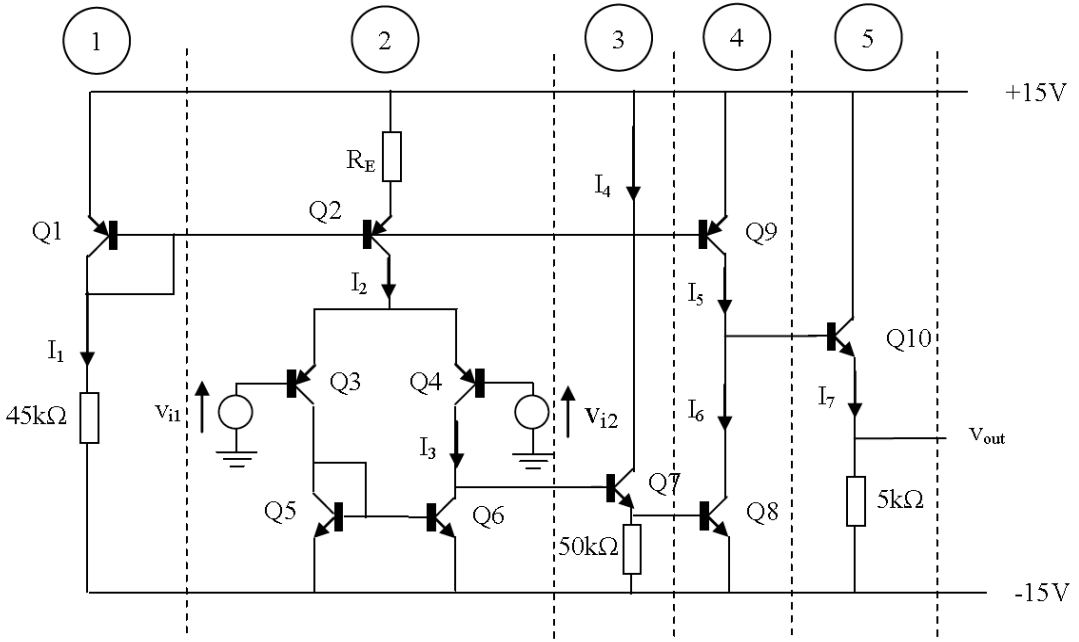
and $R_{i5} = r_{\pi 10} + (1+\beta)\cdot 5$ with $r_{\pi 10} = \dfrac{\beta}{40I_7} = 0.83\ k\Omega$

Hence $R_{i5} \approx 505\ k\Omega$

We have $r_{o8} \approx r_{o9} = \dfrac{100}{I_5} = 153\ k\Omega$

and $g_{m8} = 40I_6 = 25\ mA/V$

Then $\underline{A_{v4} = -25\times 153\ \|\ 153\ \|\ 505 \approx -1660}$



Stage 5:

Stage 5 is a CC circuit with $\underline{A_{V5} = 1}$

Finally we have:

$|A_v| = |A_{v2}\times A_{v3}\times A_{v4}\times A_{v5}| = 1.2\times 10^6$

See you in the next lecture...