EEE104 – Digital Electronics (I)

Lecture 18

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In This Session

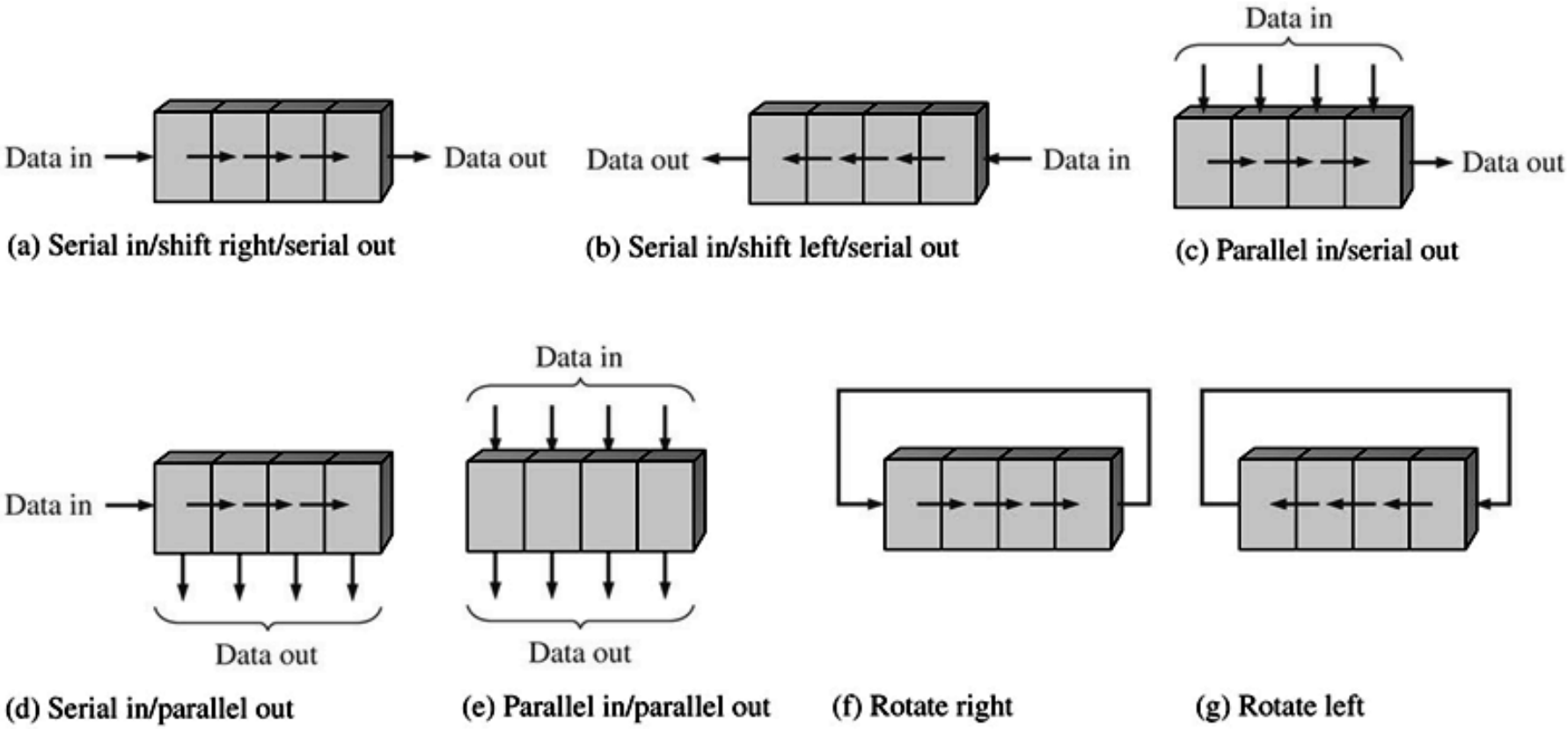
- Shift Registers

Shift Registers

- A **shift register** is made up of a set of cascaded flip-flops which store and move data.
- Each flip-flop (a stage) stores one bit of the data.
- The data moves from stage to stage at the triggering edges of a clock signal.

Shift Registers

- Types of shift registers



Shift Registers

Applications of shift registers

1. To convert serial data to parallel data

A computer system commonly requires incoming data to be in parallel format. But frequently, these systems must communicate with external devices that send or receive serial data.

Shift Registers

Applications of shift registers

2. To produce time delay

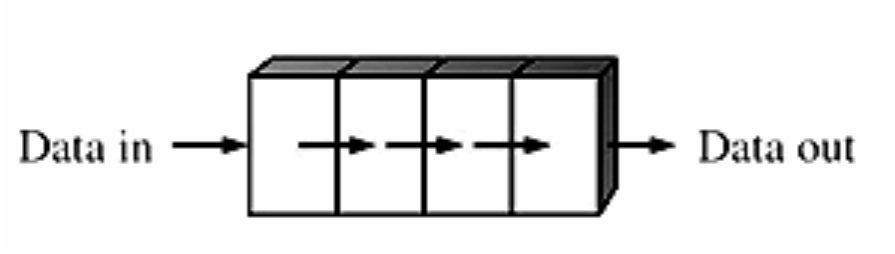
The SI/SO shift register can be used as a time delay device. The amount of delay can be controlled by the number of registers and the clock frequency.

3. Hardware Division or Multiplication by Two

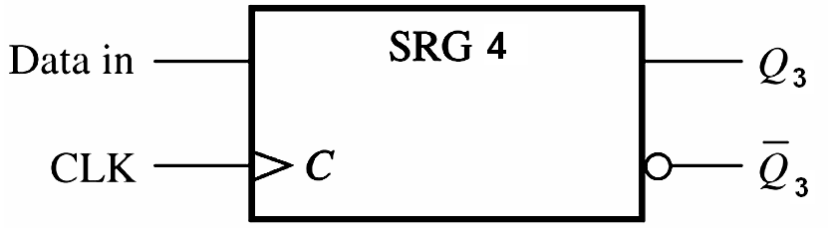
Many computers and microprocessors support instructions 'shift right' and 'shift left' for the data in a register, efficiently dividing or multiplying the data by two.

0000 1100 (12)
0000 0110 (6)
0000 0011 (3)

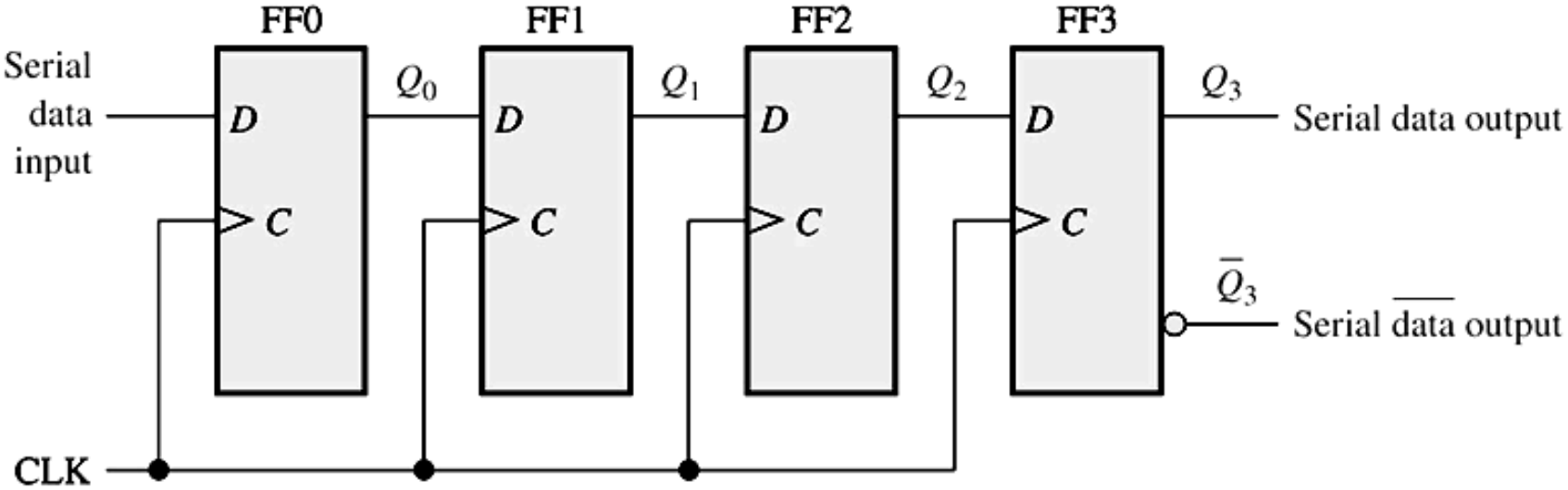
Serial In/Serial Out Shift Registers



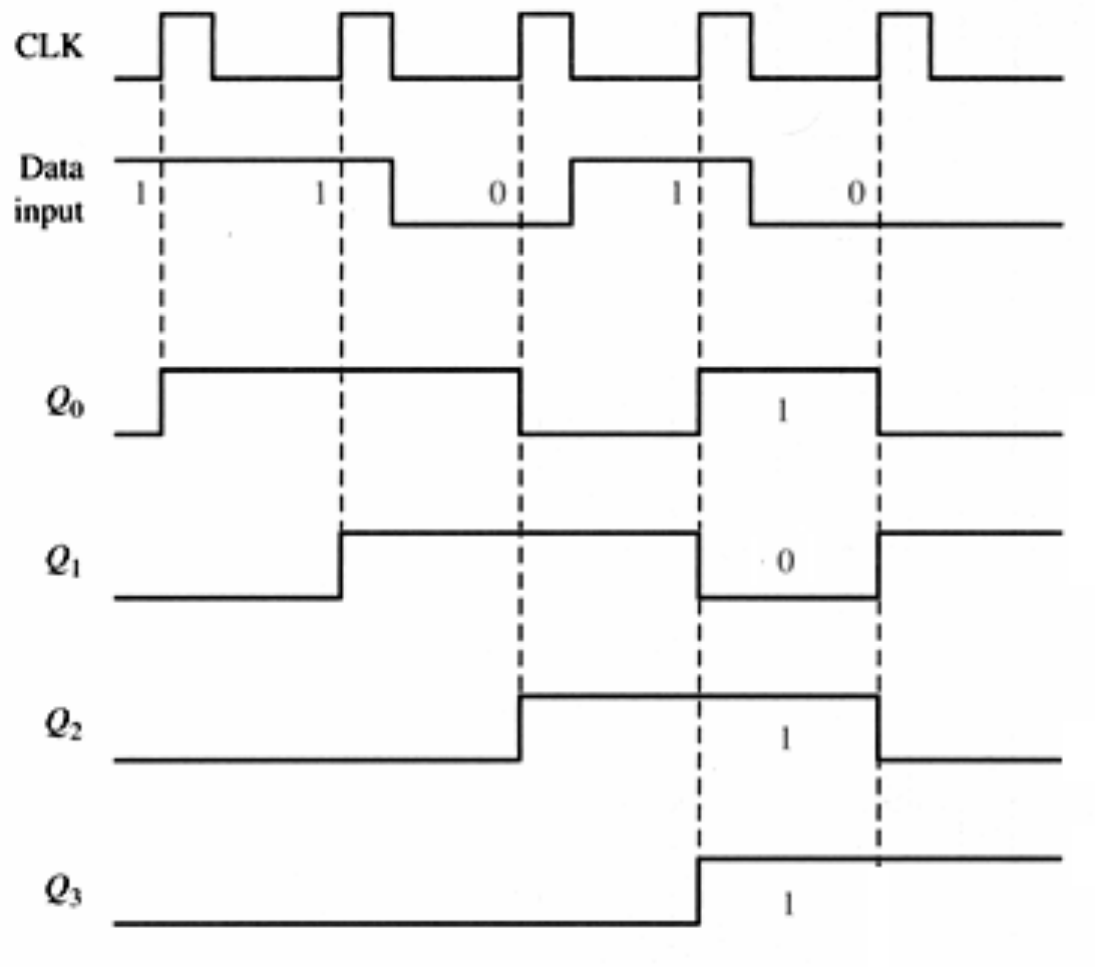
data movement



logic symbol

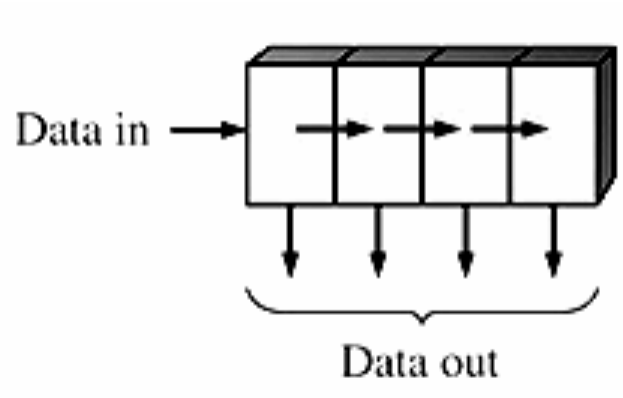


Serial In/Serial Out Shift Registers

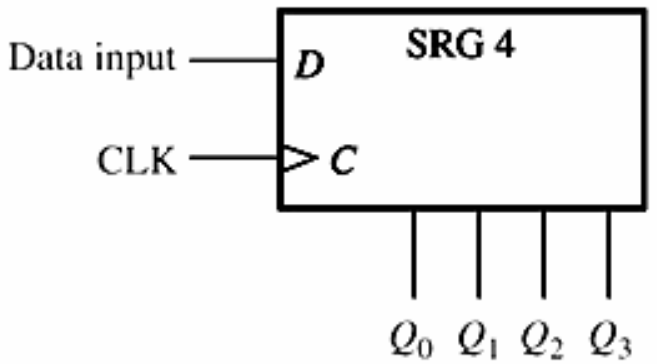


- Note the role of propagation delay.
- Data bits 1101 are stored after 4 clock cycles.

Serial In/Parallel Out Shift Registers



data movement



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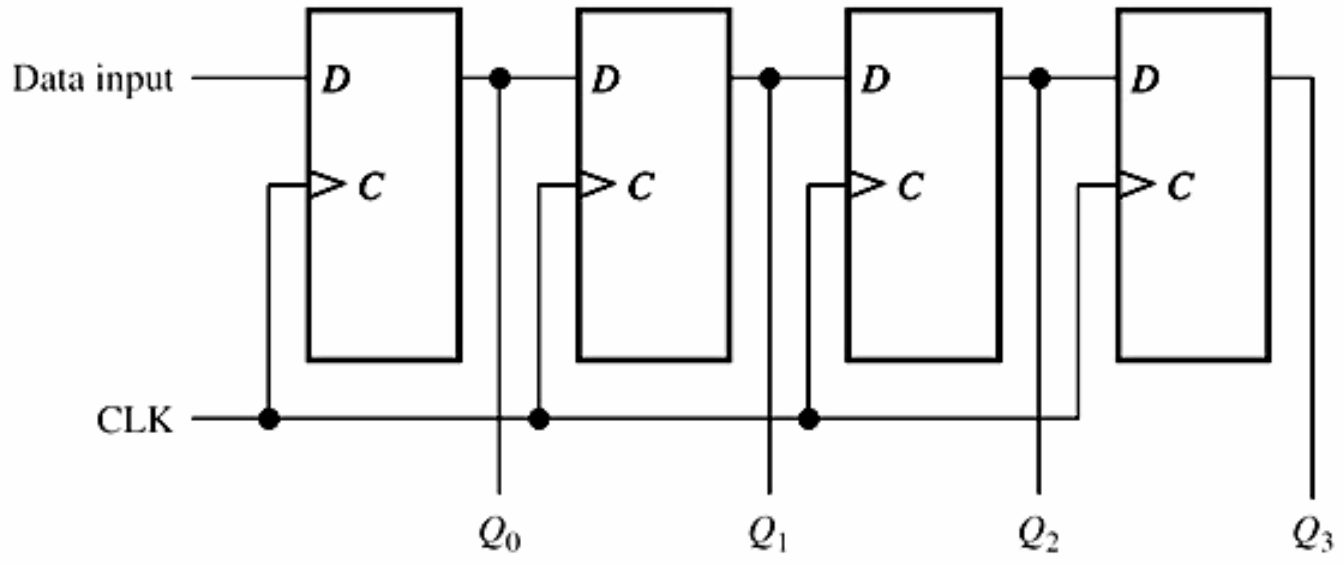
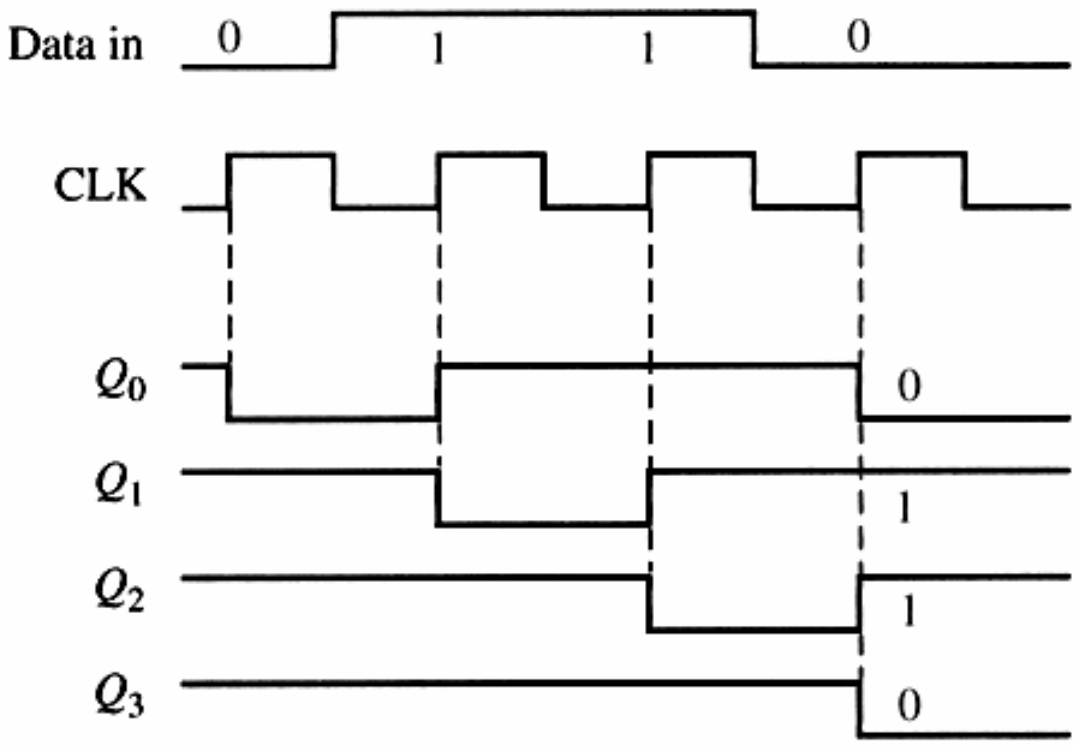
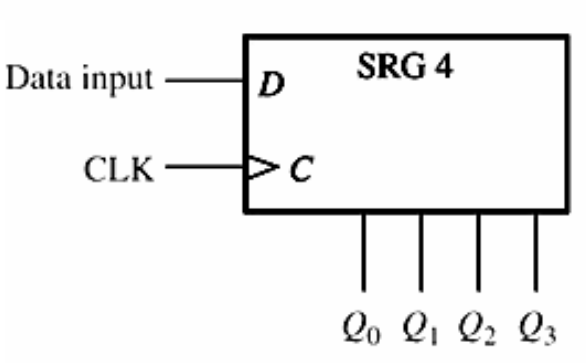


Serial In/Parallel Out Shift Registers

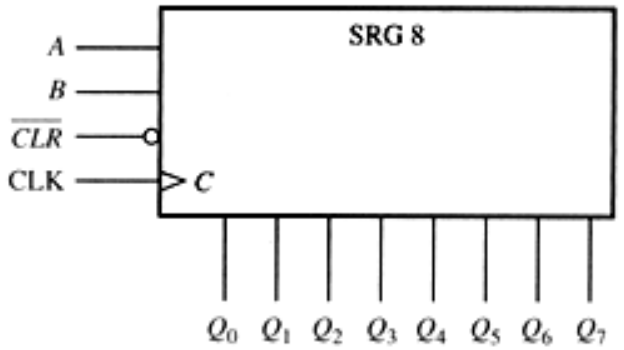


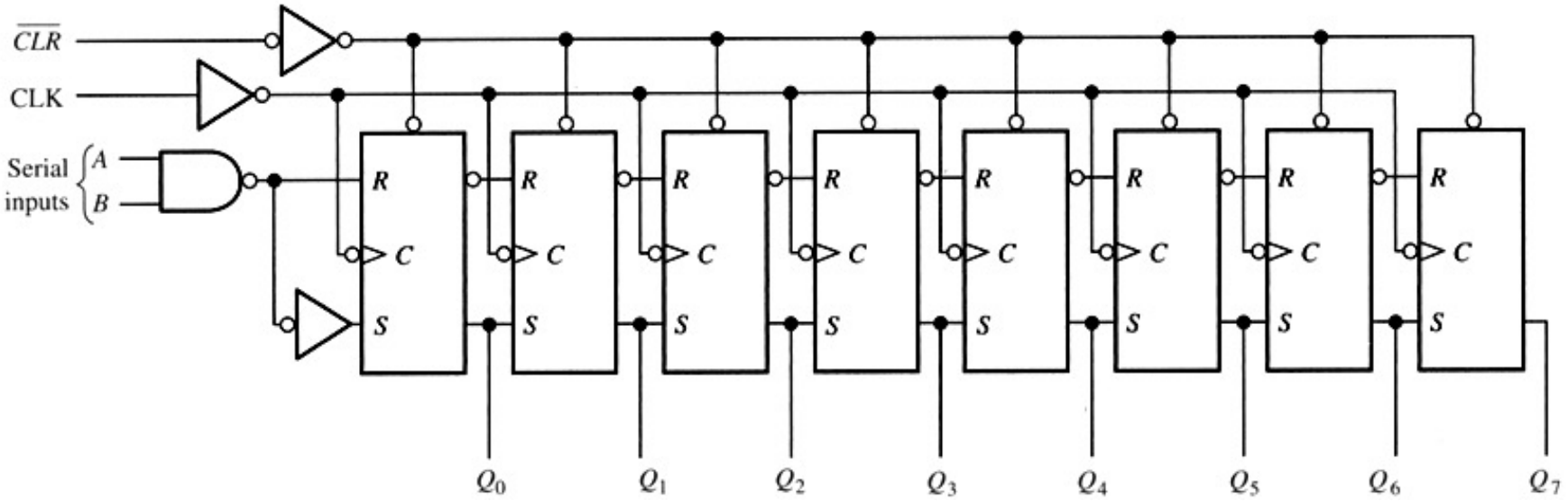


- The circuit is the same with SI/SO ones, except the output of each stage is available.

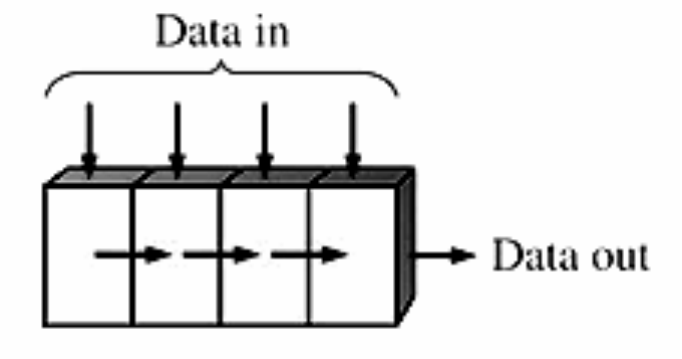
Serial In/Parallel Out Shift Registers

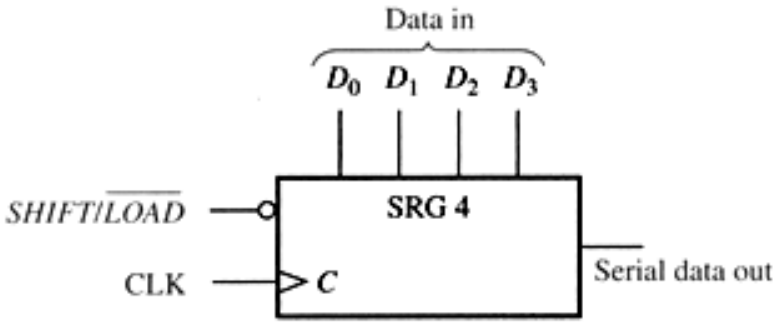
- 74HC164: an IC with 8-bit output.
- When inputs A and B are HIGH, the first FF is set; otherwise, it is reset.

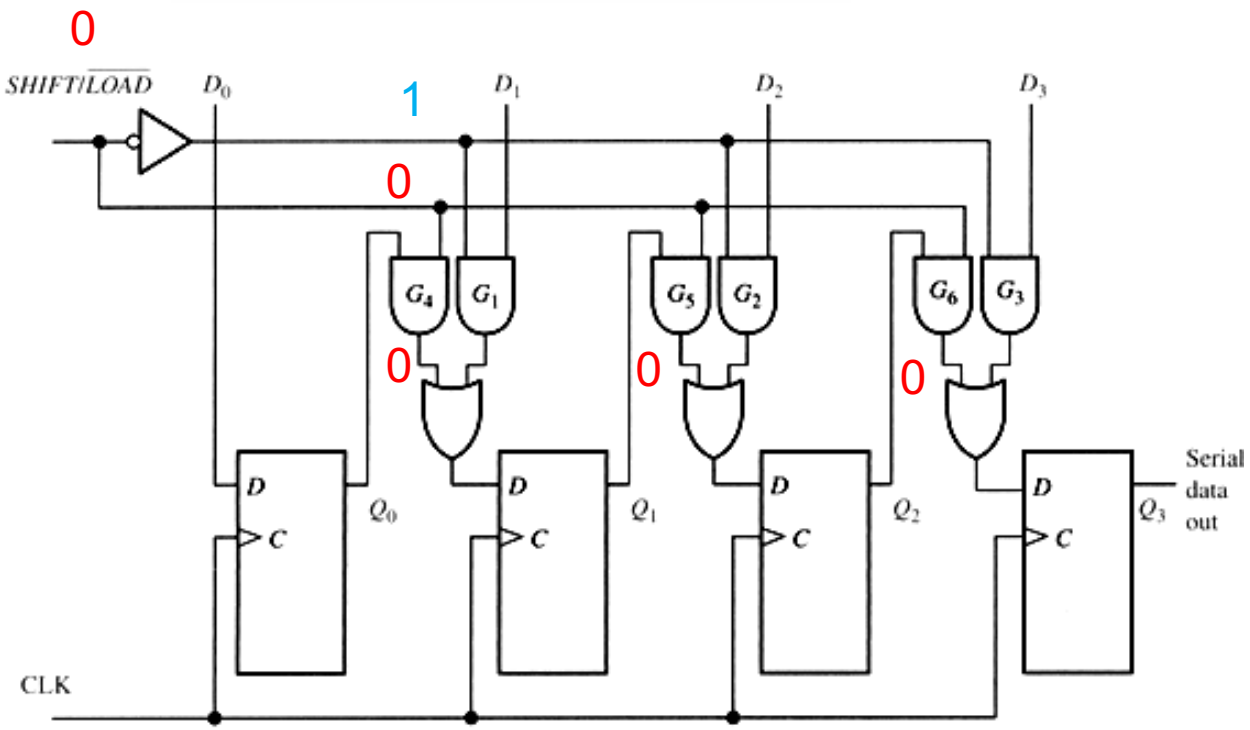




Parallel In/Serial Out Shift Registers

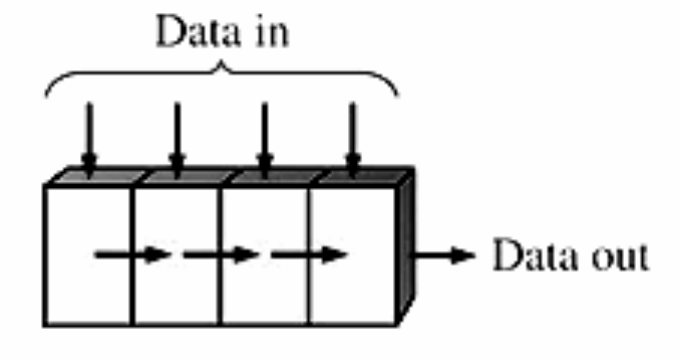


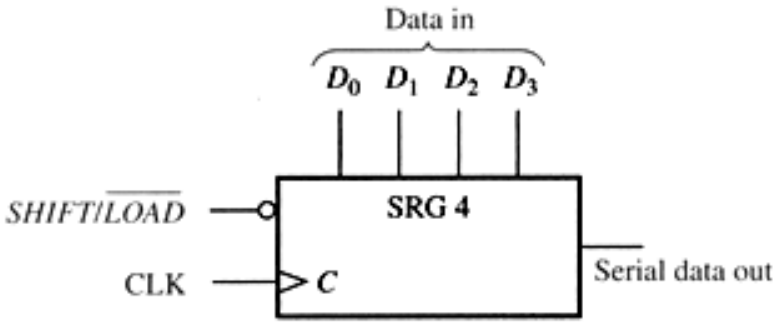


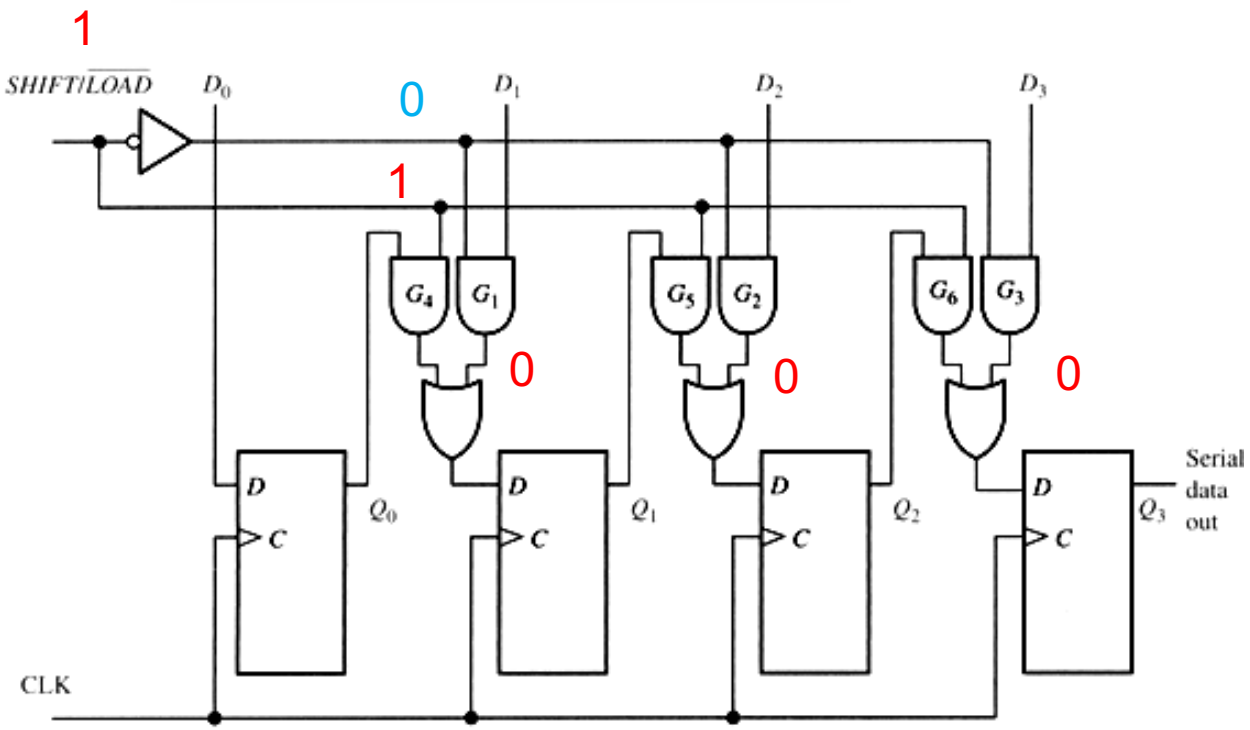


1. A LOW on S/L will enable G_1 to G_3 – load data.
2. A High on S/L will enable G_4 to G_6 – shift data.

Parallel In/Serial Out Shift Registers







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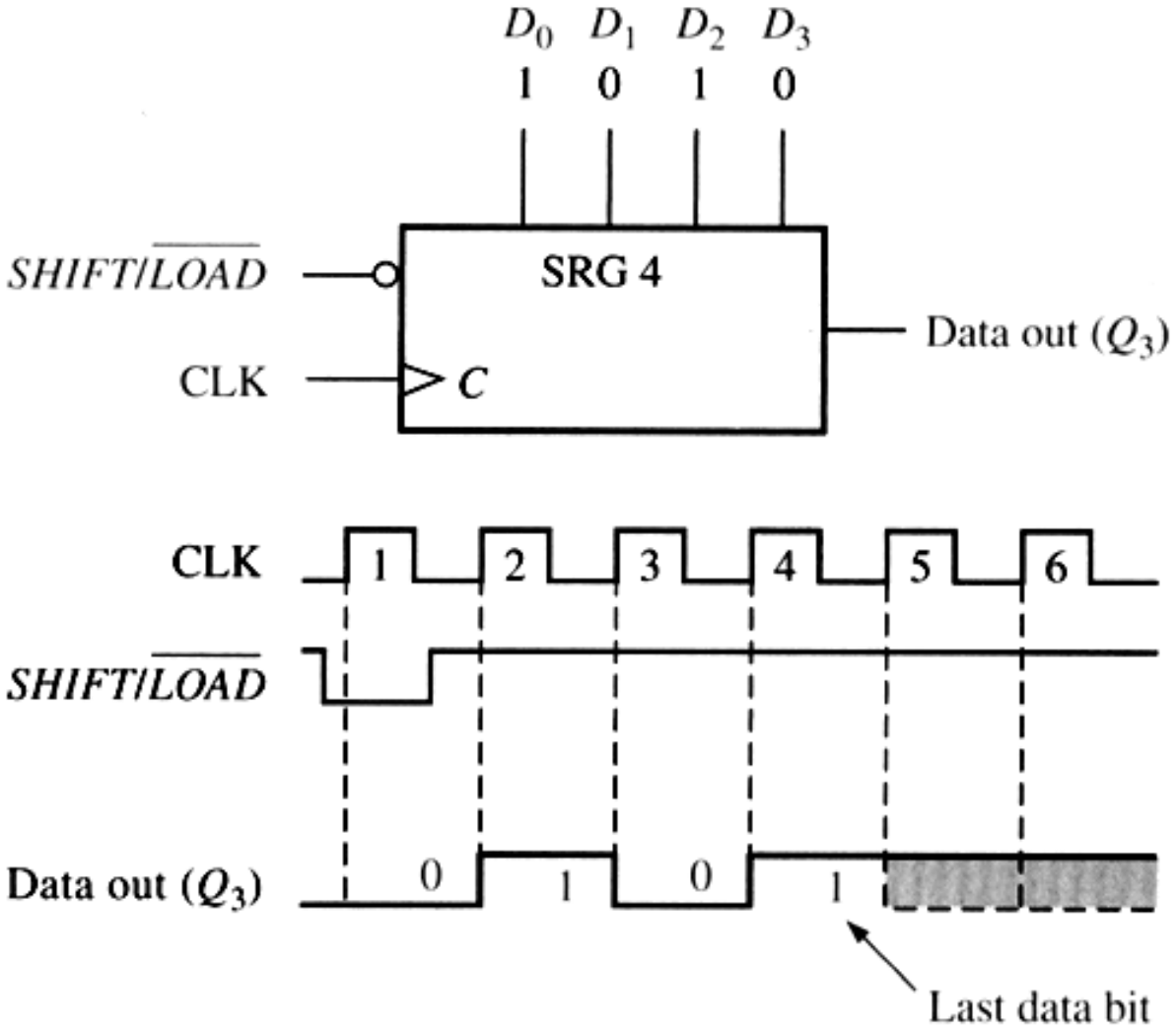

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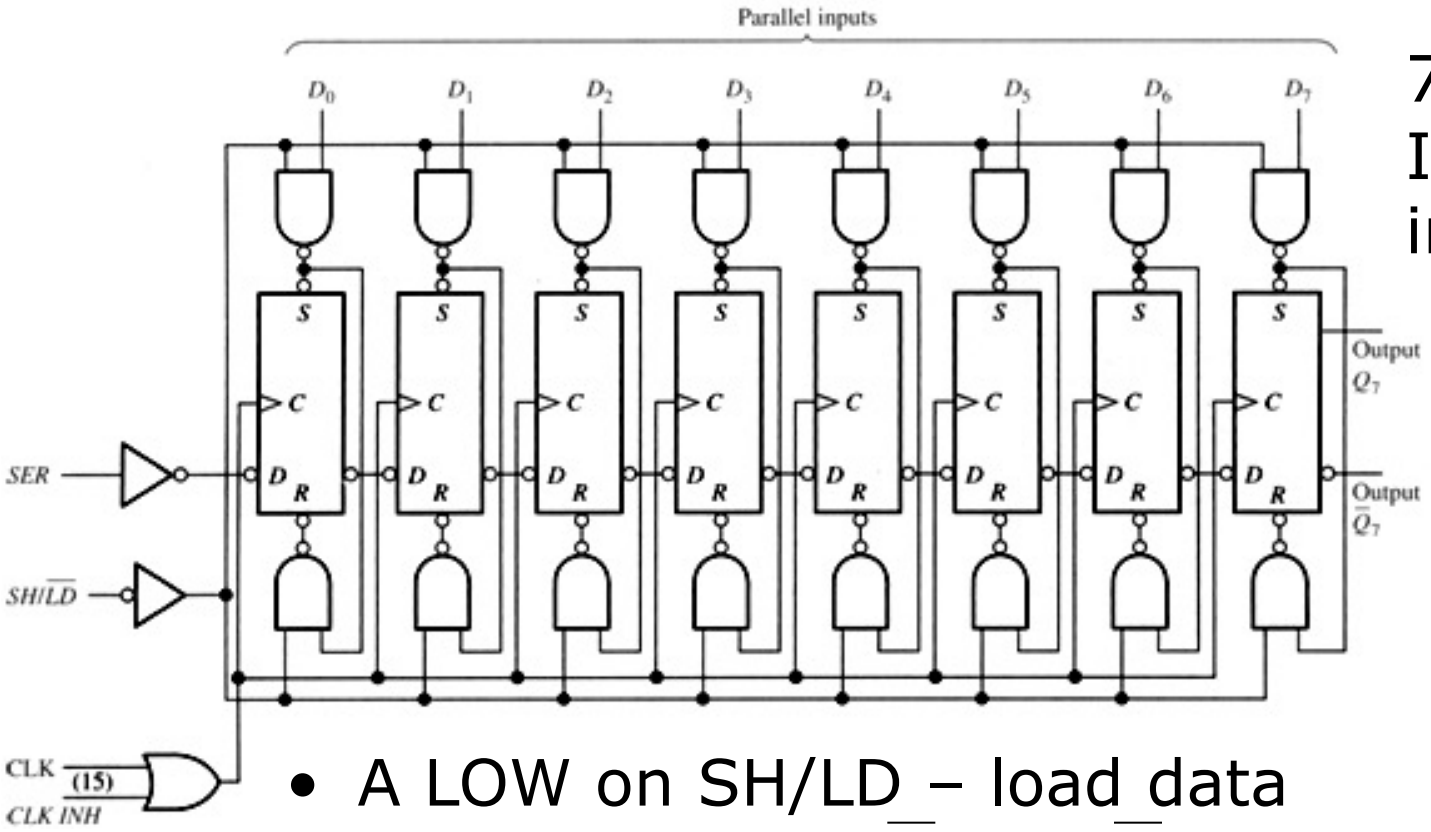
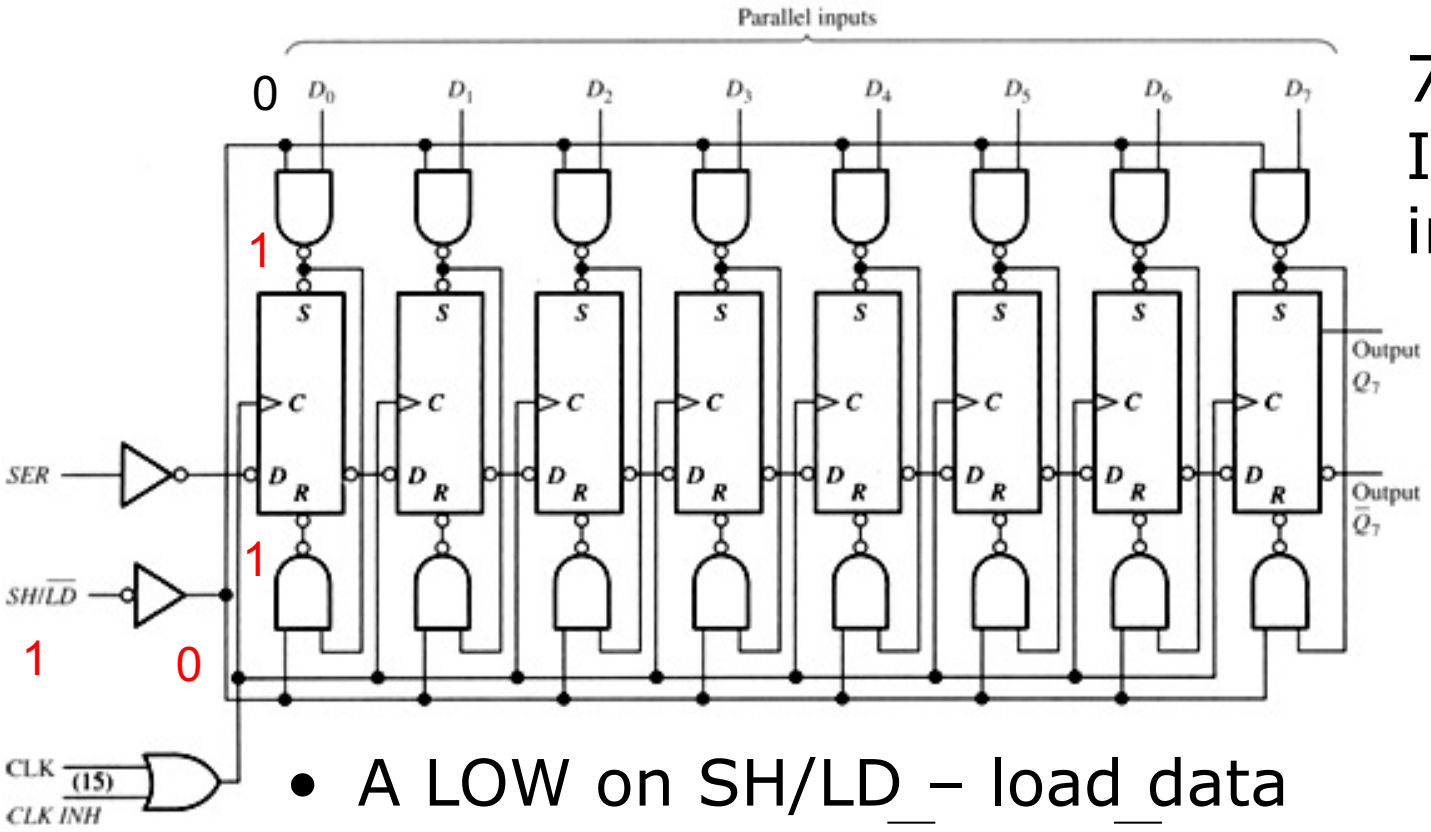


74HC165: an IC with 8-bit input

- A LOW on SH/$\overline{LD}$ – load data
  - When D = 0, $\overline{S}$ = 1, $\overline{R}$ = 0, so Q = 0.
  - When D = 1, $\overline{S}$ = 0, $\overline{R}$ = 1, so Q = 1.
- A HIGH on SH/$\overline{LD}$ makes $\overline{S}$ and $\overline{R}$ HIGH – shift data

Parallel In/Serial Out Shift Registers



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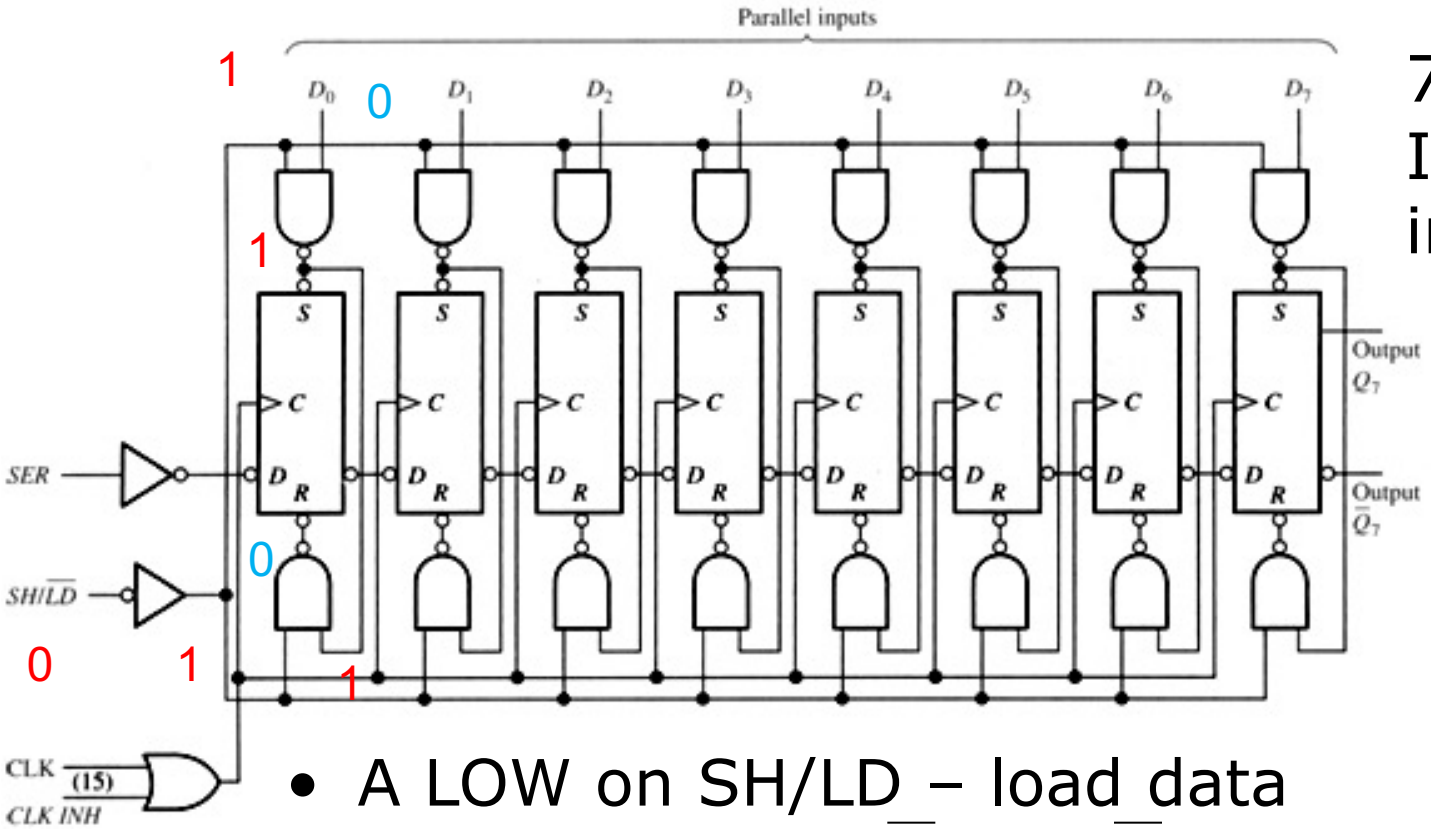

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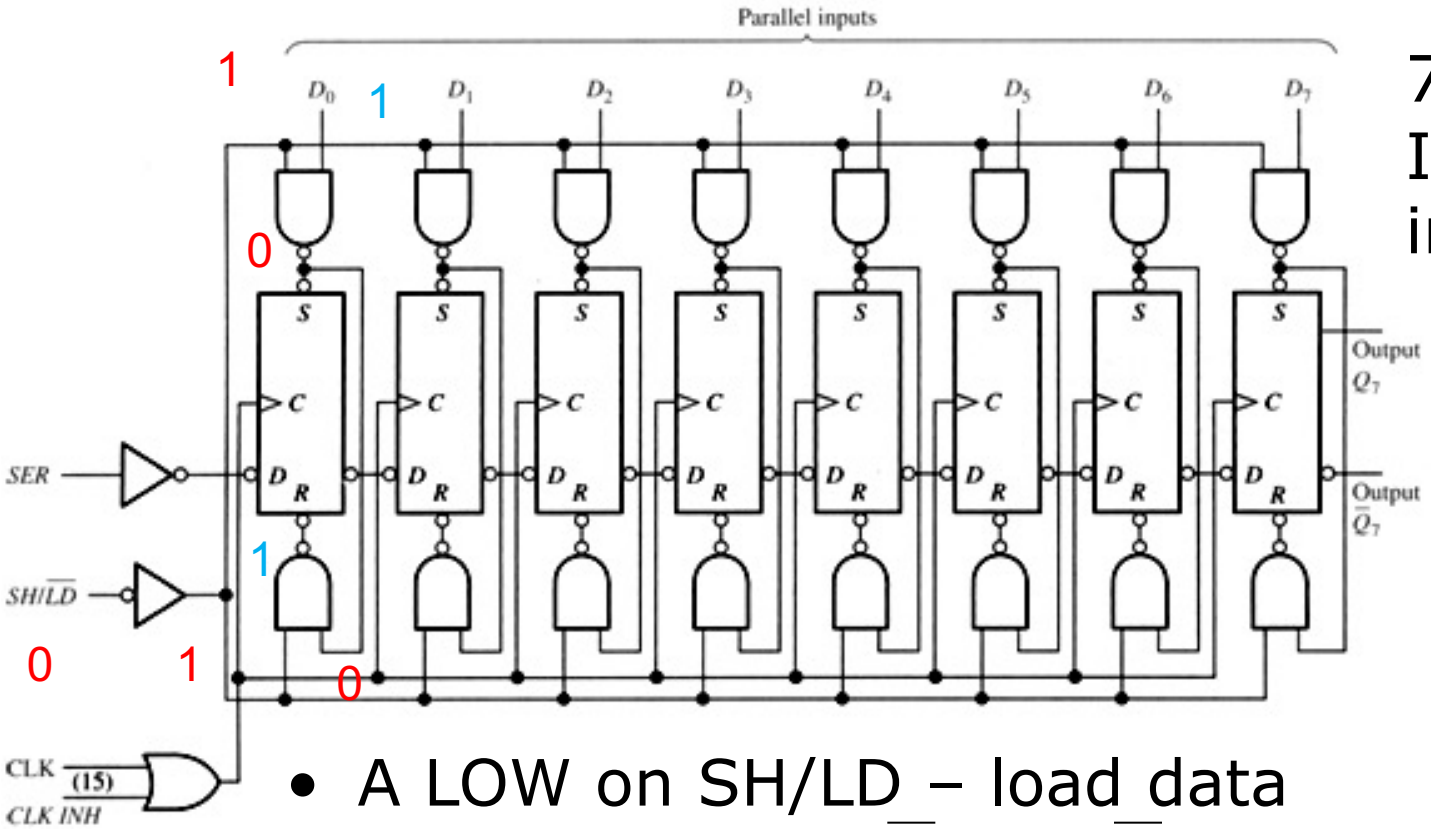

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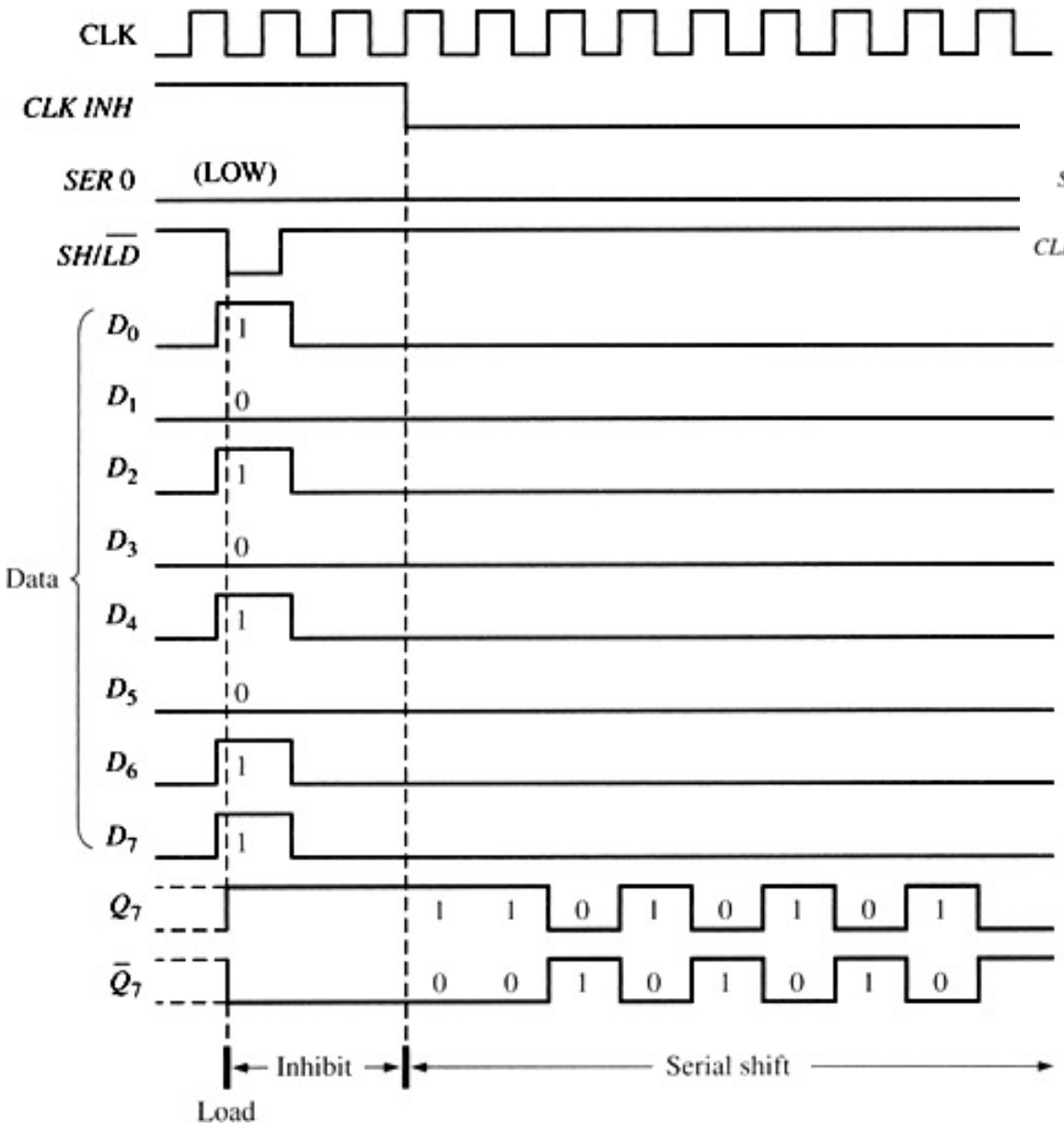

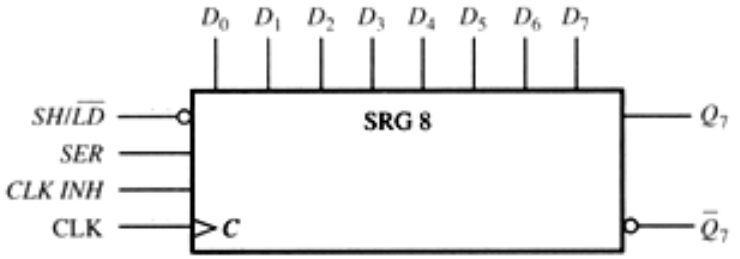

CLK INH: clock inhibit

SER: serial data in

SH/LD: shift/load

Parallel In/Parallel Out Shift Registers