Nonideal Effects in Operational Amplifiers

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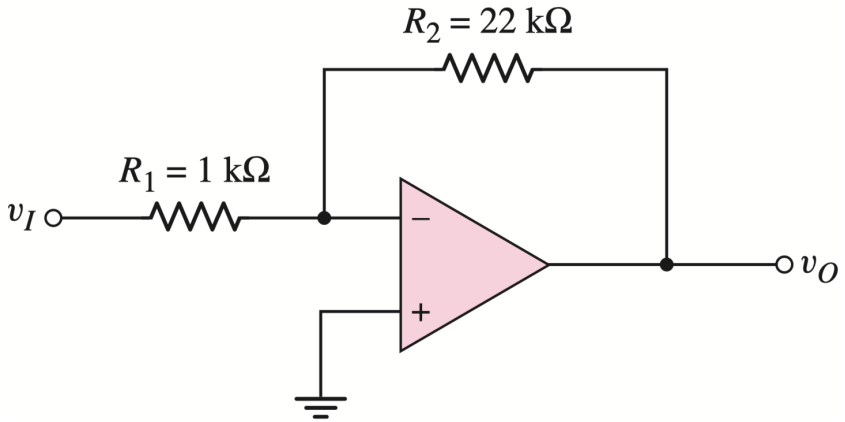
Part 1: Finite Open-Loop Gain, Input and Output Resistances

Finite Open-Loop Gain

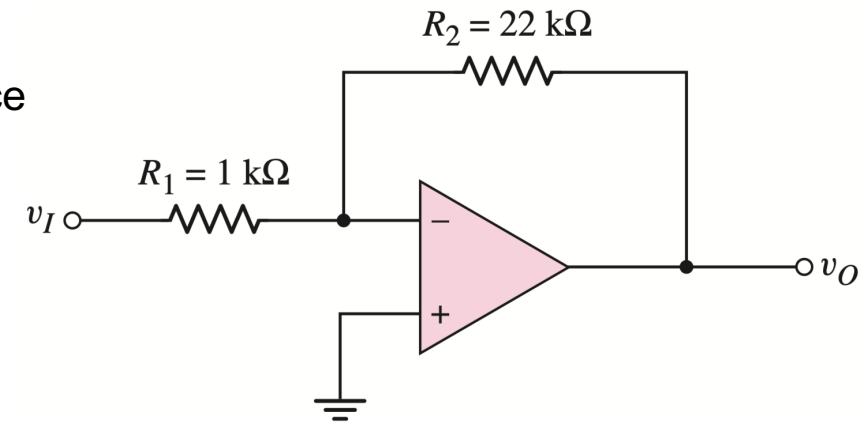
Exercise

Consider the circuit shown below. (a) Determine the ideal output voltage v_O if $v_I = -0.40$ V. (b) Assume the op-amp is ideal except it has a finite open-loop gain. Determine the actual output voltage if the open-loop gain of the op-amp is $A_{od} = 5\times10^3$.



Solution:

(a) For an ideal Op-Amp, the input resistance and open-loop gain are *infinite*.



From Virtual Short Principle, we have

$$v_O = -\frac{R_2}{R_1} \cdot v_I = 8.8\ \text{V}$$

(b) For an actual Op-Amp with finite open-loop gain (*no virtual short*), we have

$$\frac{v_I - v_1}{R_1} = \frac{v_1 - v_O}{R_2}$$

Since $v_2 = 0$, the output voltage is

$$v_O = -A_{OL} v_1$$

We find

$$\frac{v_I}{R_1} = v_1 \left(\frac{1}{R_1} + \frac{1}{R_2}\right) - \frac{v_O}{R_2}$$

The closed-loop gain is then

$$A_{CL} = \frac{v_O}{v_I} = \frac{-\frac{R_2}{R_1}}{1 + \frac{1}{A_{OL}}(1 + \frac{R_2}{R_1})} = -21.8993$$

$$v_O = (-21.8993) \times (-0.4) = 8.7597\ \text{V}$$

Closed-Loop Input Resistance

1. Inverting Amplifier

Consider the finite open-loop gain A_{OL}, finite open-loop input resistance R_i, and nonzero output resistance R_o, a KCL at the output node yields

$$\frac{v_O}{R_L}+\frac{v_O-(-A_{OL}v_1)}{R_o}+\frac{v_O-v_1}{R_2}=0$$

Solving for the output voltage, we have

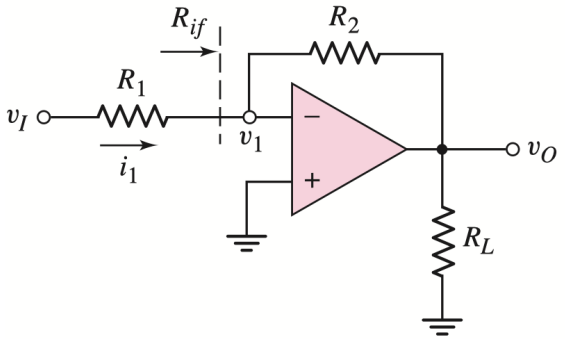
$$v_O=\frac{-v_1\left(\frac{A_{OL}}{R_o}-\frac{1}{R_2}\right)}{\frac{1}{R_L}+\frac{1}{R_O}+\frac{1}{R_2}}$$

A KCL equation at the input node yields

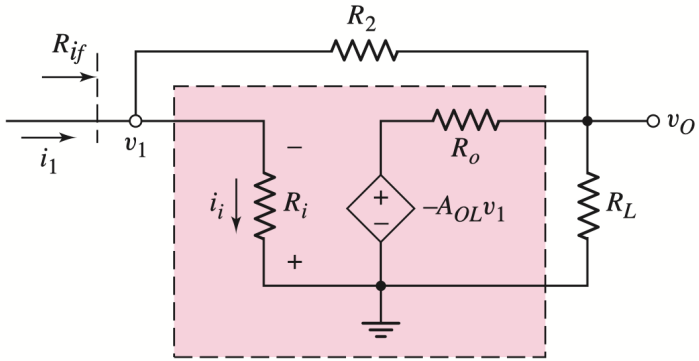
$$i_1=\frac{v_1}{R_i}+\frac{v_1-v_O}{R_2}$$

Combining the equations produces

$$R_{if}=\frac{v_1}{i_1}=\frac{1}{\frac{1}{R_i}+\frac{1}{R_2}\left(\frac{1+A_{OL}+\frac{R_o}{R_L}}{1+\frac{R_o}{R_L}+\frac{R_o}{R_2}}\right)}$$



(a)



(b)

In the limit as $A_{OL}\to\infty$, we see that $R_{if}\to 0$, which means that $v_1\to 0$, it becomes **virtual ground** then.

2. Noninverting Amplifier

Writing a KCL at the output node yields

$$\frac{v_O}{R_L} + \frac{v_O - A_{OL}v_d}{R_o} + \frac{v_O - v_1}{R_2} = 0$$

Solving for the output voltage, we have

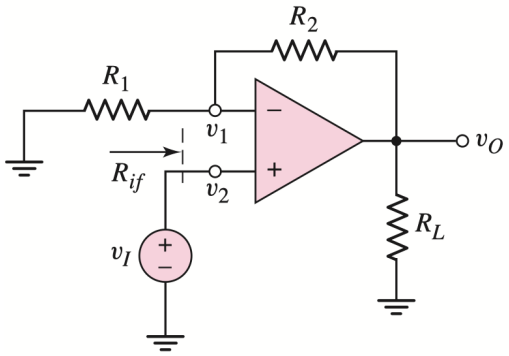
$$v_O = \frac{\frac{v_1}{R_2} + \frac{A_{OL}v_d}{R_o}}{\frac{1}{R_L} + \frac{1}{R_O} + \frac{1}{R_2}}$$

A KCL equation at the v_1 node yields

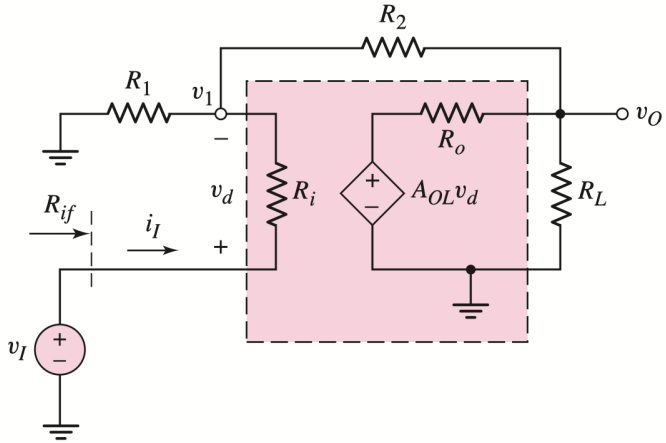
$$i_I = \frac{v_1}{R_1} + \frac{v_I - v_O}{R_2}$$

Combining the equations, noting $v_d = i_I R_i$, $v_1 = v_I - v_d$, and setting $R_o = 0$, produce

$$R_{if} = \frac{v_I}{i_I} = \frac{R_i(1 + A_{OL}) + R_2\left(1 + \frac{R_i}{R_1}\right)}{1 + \frac{R_2}{R_1}}$$



(a)

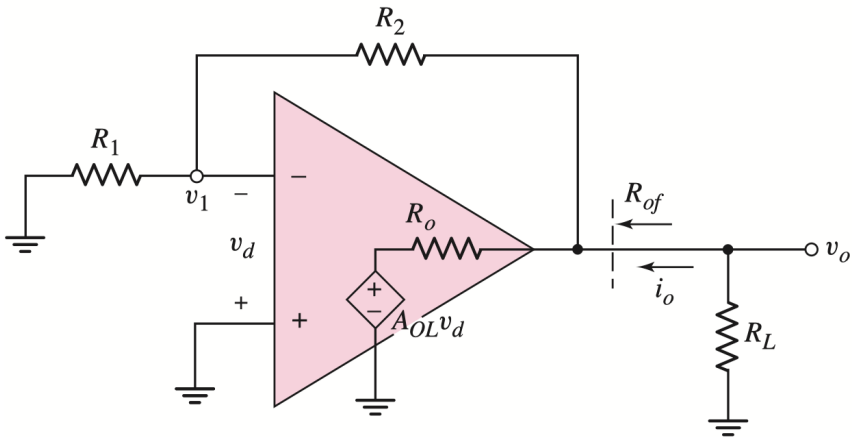


(b)

In the limit as $A_{OL} \to \infty$, we see that $R_{if} \to \infty$, which is the property of the ideal noninverting amplifier.

Nonzero Output Resistance

Consider a general equivalent circuit of both an inverting and noninverting amplifier, to determine the output resistance, we set the independent input voltages equal to zero (assuming input resistance is very large).



A KCL at the output node yields

$$i_o = \frac{v_o - A_{OL}v_d}{R_o} + \frac{v_o}{R_1 + R_2}$$

The differential input voltage is $v_d = -v_1$, where

$$v_1 = \left(\frac{R_1}{R_1 + R_2}\right) v_o$$

Combining the equation, we have

$$i_o = \frac{v_o}{R_o} - \frac{A_{OL}}{R_o}\left[-\left(\frac{R_1}{R_1 + R_2}\right) v_o\right] + \frac{v_o}{R_1 + R_2}$$

or

$$\frac{i_o}{v_o} = \frac{1}{R_{of}} = \frac{1}{R_o}\left[1 + \frac{A_{OL}}{1 + \frac{R_2}{R_1}}\right] + \frac{1}{R_1 + R_2}$$

Since R_o is normally small and A_{OL} is normally large, the equation, to a good approximation, is as follows

$$\frac{1}{R_{of}} \cong \frac{1}{R_o}\left(\frac{A_{OL}}{1 + \frac{R_2}{R_1}}\right)$$

In most op-amp, the open-loop output resistance R_o is on the order of 100 Ω. Since A_{OL} is normally much larger than $1 + R_1/R_2$, the closed–loop output resistance can be very small.

Part 2: Slew Rate

What is Slew Rate?

- In the ideal case, we assume the open-loop gain of an op-amp is infinite, hence it has no frequency dependence
- But in reality, the op-amp has a finite gain, and the frequency of the input signal affects the characteristics of the output signal in terms of dynamic response
- Due to the increased number of capacitances in an op-amp, the op-amp's output cannot respond instantaneously to a change in input
- In another word, op-amps have ***a limit on how rapidly the output voltage can change – Slew Rate***

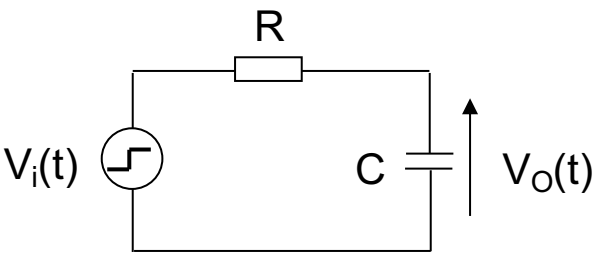
$$SR = \frac{dV_o}{d_t}\Big|_{\max}$$

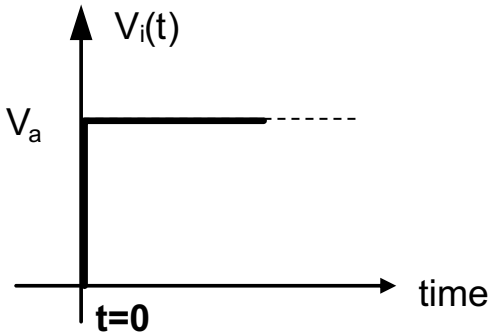
- The slew rate of the op-amp can limit the performance of a circuit and it can distort the output waveform if its limit is exceeded.
- The slew rate should be as high as possible to ensure the maximum undistorted output voltage

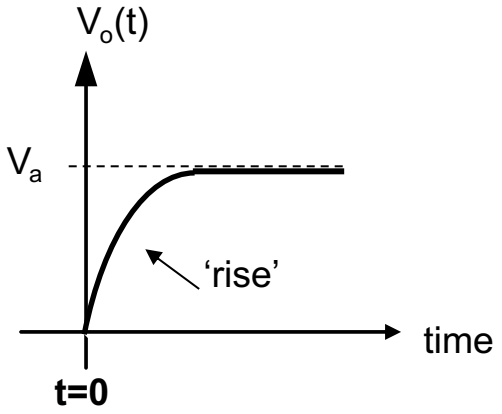
Effect of the Slew Rate Limit on Amplifier Response

1. Step Response

First we consider a low-pass RC circuit with a *step input*:







According to the complete response equation: $f(t) = f(\infty) + [f(0)^+ - f(\infty)]e^{-\frac{t}{\tau}}$

We have:

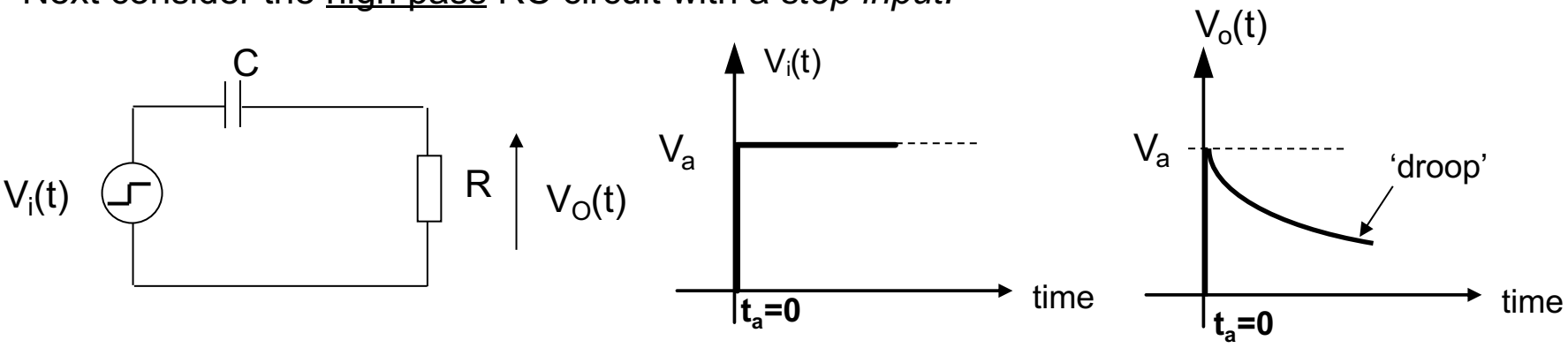
$V_o(t) = V_a(1 - e^{-t/\tau_r})$ where $\tau_r = RC$ is called the rise time constant of the circuit

Recall for the low-pass RC circuit, the rise time constant is related to the upper corner frequency of the frequency response by:

$$f_H = \frac{1}{2\pi\tau_r}$$

We can deduce the rise time constant of step response from the upper corner frequency and 'vice versa'

Next consider the high pass RC circuit with a *step input:*



Solution of the circuit equation: $V_i(t) = iR + V_c(t)$ with $V_o(t) = iR$

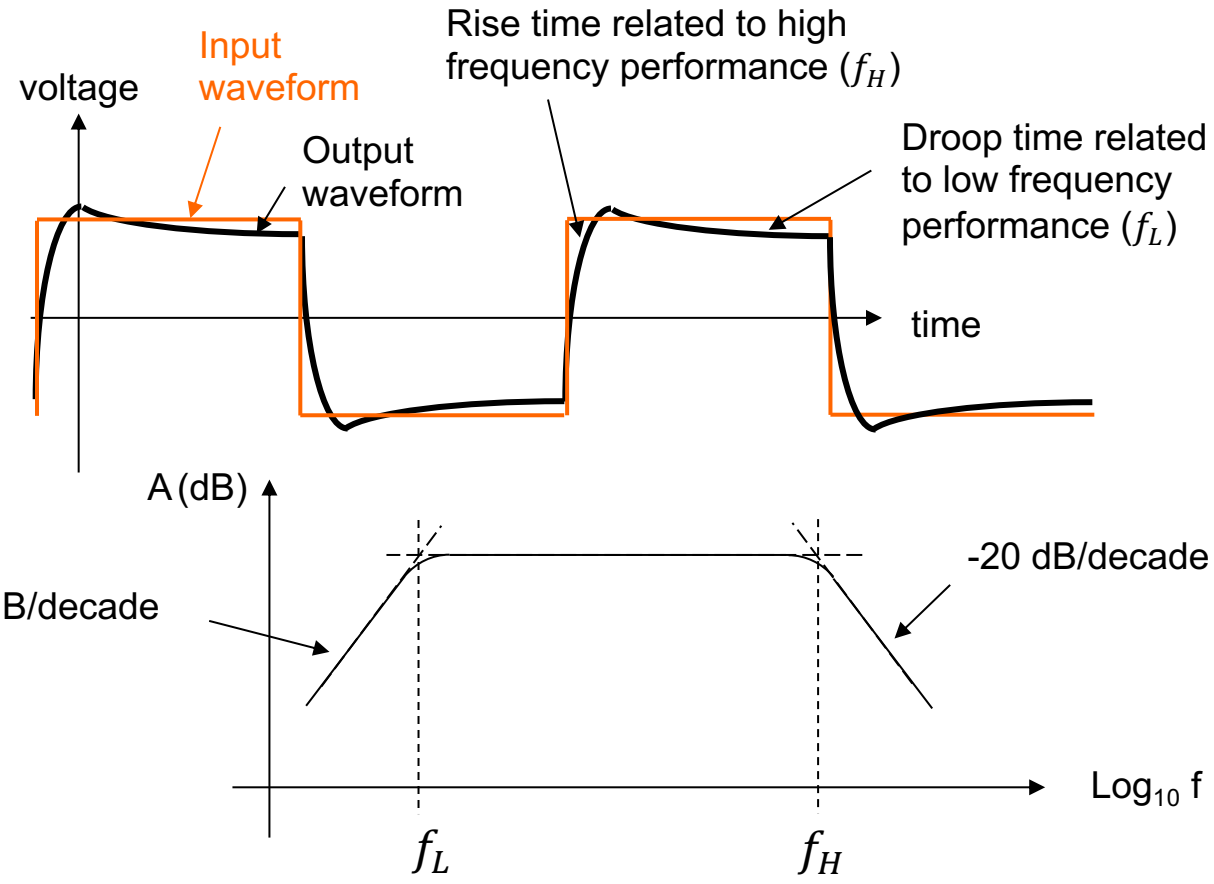
Then $V_0(t) = V_a e^{-t/\tau_d}$ where $\tau_d = RC$ is the droop time constant

For the high-pass RC circuit, the droop time constant of the step response is related to the lower corner frequency:

$$f_L = \frac{1}{2\pi\tau_d}$$

We can deduce the droop time constant of step response from the lower corner frequency and 'vice versa'

Bring together, the step response of an amplifier circuit would look like:

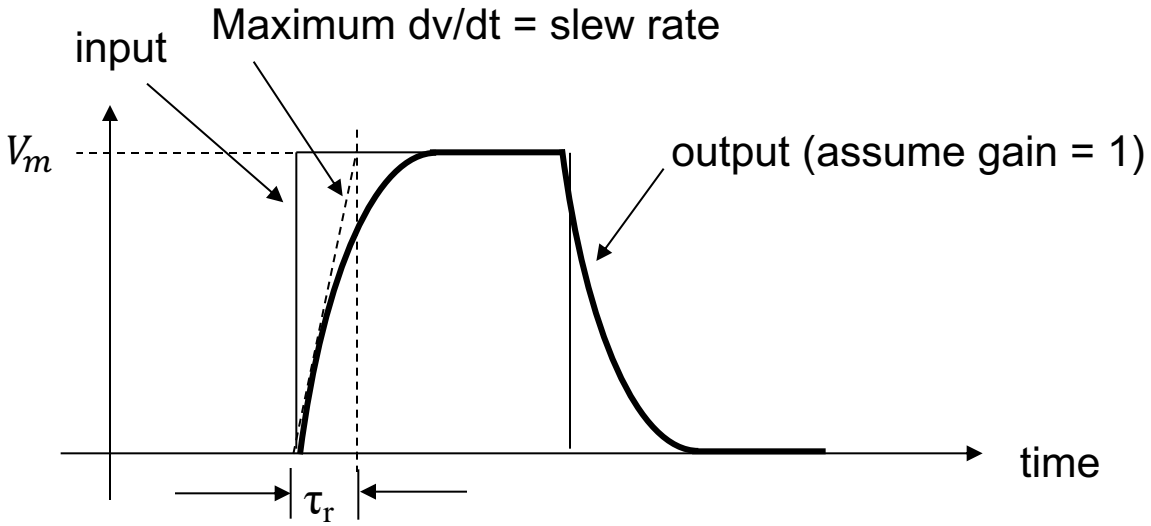


$$f_H = \frac{1}{2\pi\tau_r}$$

$$f_L = \frac{1}{2\pi\tau_d}$$

The step response can be determined from the upper and lower corner frequencies of the system and 'vice versa'.

Note that for a step response, **only the rise time** of the output will become limited by the slew rate limit when maximum dv/dt = slew rate.



For a first order system, the maximum rate of change of voltage is given by:

$$V_0(t) = V_m\left(1 - e^{-t/\tau_r}\right) \quad \text{Hence} \quad SR = \frac{dV_O(t)}{d_t}\Big|_{\max} = \frac{V_m}{\tau_r} e^{-\frac{t}{\tau_r}}\Big|_{t=0} = \frac{V_m}{\tau_r}$$

So the output will become slew rate limited when $V_m = \tau_r \times \text{slew rate}$

Example:

Determine the pulse output voltage for which a circuit with bandwidth 10MHz that uses a 741 op-amp becomes slew rate limited.

(slew rate limit for 741 op-amp = 1V/μS),

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Solution:

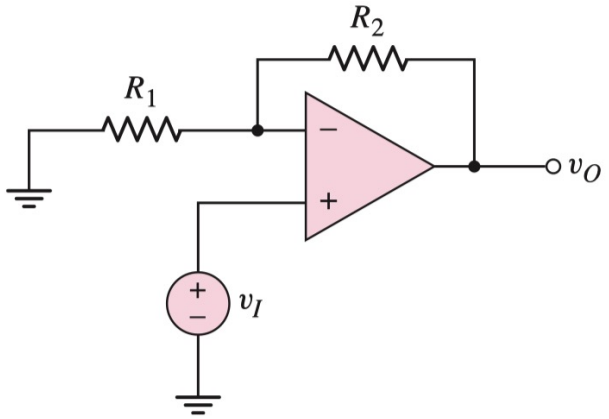
The rise time constant can be found by: $\tau_r = \frac{1}{2\pi f_H} = \frac{1}{2\pi \times 10^7} = 16 \ \ n\text{S}$

Therefore the rising edge will become slew rate limited when

$$V_O = \tau_r \times SR = 16 \times 10^{-9} \times 10^6 = 16 \, mV$$

2. Sinusoidal Response

Now consider what happens when a sinusoidal input signal is applied. Consider the following non-inverting amplifier:



If $v_I = V_a \sin \omega t$, then we have

$$v_O(t) = V_a \left(1 + \frac{R_2}{R_1}\right) \sin \omega t = V_m \sin \omega t$$

where V_m is the ideal peak value of the sinusoidal output voltage

The rate at which the output voltage changes is:

$$\frac{dv_O(t)}{dt} = \omega V_m \cos \omega t$$

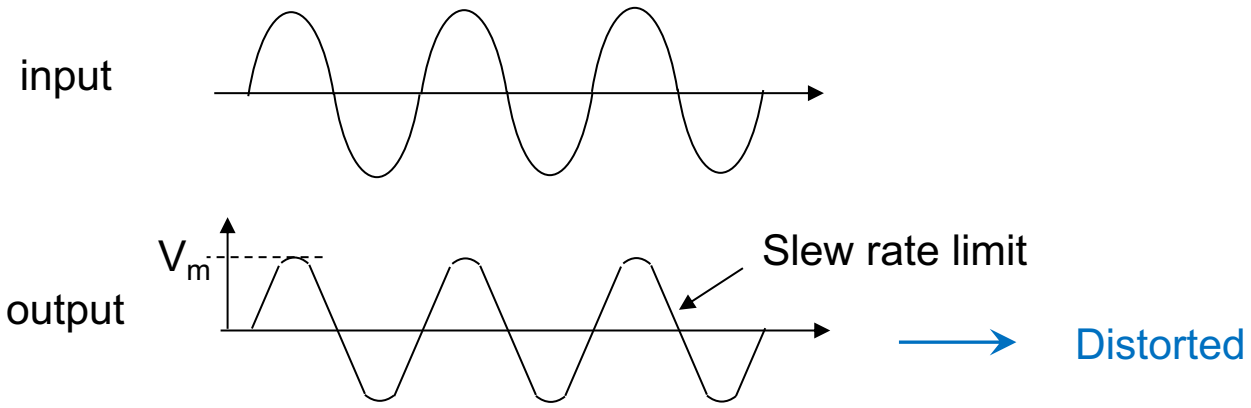
Therefore, the slew rate is: $\omega V_m \cos \omega t \,|_{max} = \omega V_m$

If the input signal is sinusoidal, the slew rate limit is reached when

$$\text{slew rate} = \frac{dV_O}{dt}(\max) = \left.\frac{d(V_m \sin \omega t)}{dt}\right|_{\max} = V_m \omega$$

The frequency at which the slew rate limit is reached depends on the amplitude of the output signal as well as it's frequency.

A slew rate limited output will be apparent from the shape of the output waveform:



Example:

What is the maximum frequency at which an undistorted output signal of 10V amplitude sinusoidal can be obtained using a 741 op-amp? (SR = 1V/μsec)

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What is the maximum frequency at which an undistorted output signal of 10V amplitude sinusoidal can be obtained using a 741 op-amp? (SR = 1V/μsec)

Solution:

For sinusoidal response, we have: $SR = V_m\omega$

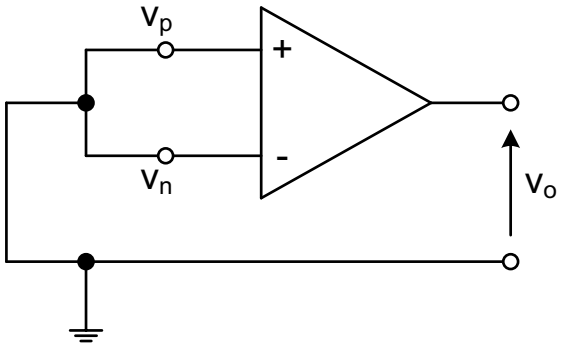
Hence, $f_{max} = \frac{SR}{V_m \cdot 2\pi} = \frac{10^6}{20\pi} \approx 16\ kHz$ *Higher frequency signals will be distorted.*

Part 3: DC Imperfections of Operational Amplifiers

DC imperfections of operational amplifiers include ***offset voltage, bias current, and offset current*.** They result in non-zero output voltage even at zero input voltages. This effect is especially noticeable in high gain or precision DC amplifiers.

1. Offset Voltage

Suppose an op-amp has both its inputs connected to ground:



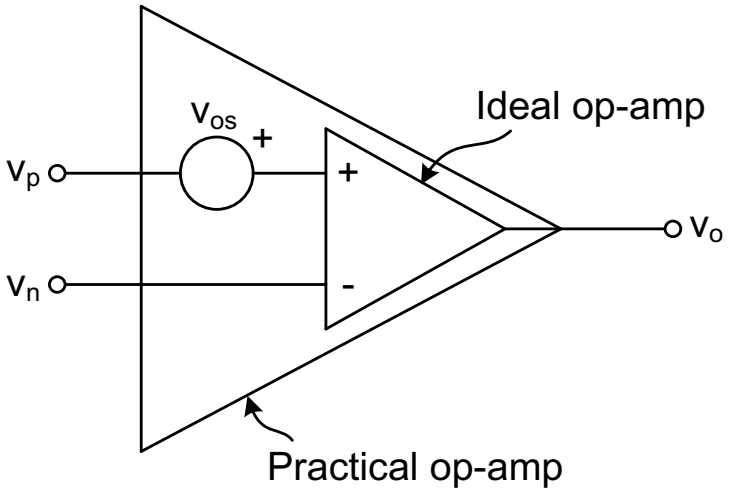
Here $V_p = V_n = 0$ (tied to ground) so **ideally** we expect $V_O = A_{OL}(V_p - V_n) = 0$

However, in **practice,** we usually find $V_O \neq 0$

We can therefore model this contribution to the output voltage in a *practical op-amp* by inserting a DC voltage V_{os} at the input of an *ideal op-amp* as shown:

The offset voltage V_{os} is the equivalent input voltage that would need to be applied (as shown) to make $V_O = 0$

N.B. V_{OS} is always (by convention) assumed connected to the *non-inverting (+) input*, with the polarity shown. (But note that it can be a positive or negative value!)



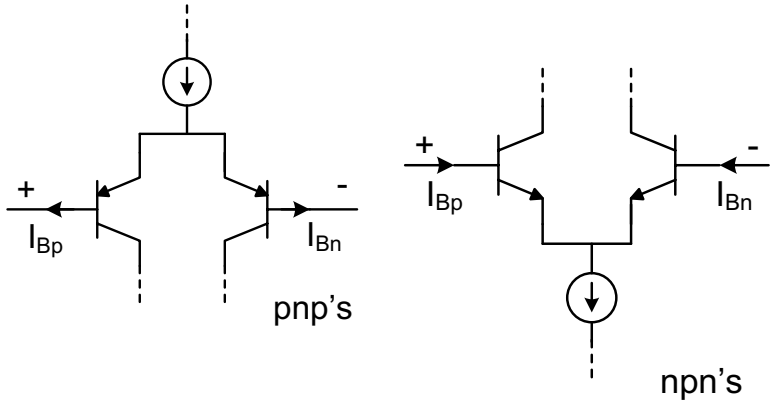
The manufacturer usually quotes the magnitude of V_{OS} – e.g., V_{OS} = 2mV typical, 6mV max.

This means ~50% of the tested op-amp have V_{OS} between -2mV to +2mV, but all have V_{OS} between -6mV and +6mV.

2. Bias Currents

These are input currents I_{Bp} and I_{Bn} that MUST be provided for the operational amplifier to function properly.

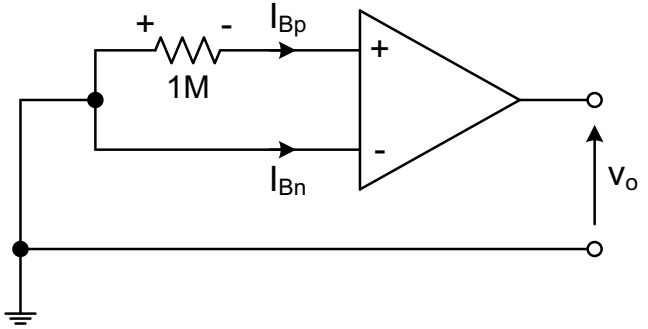
The input bias currents can flow *either in or out* of the op-amp depending on whether the input stage is constructed with npn or pnp transistors:



If pnp transistors are used, the current flows *out* of the input terminals.

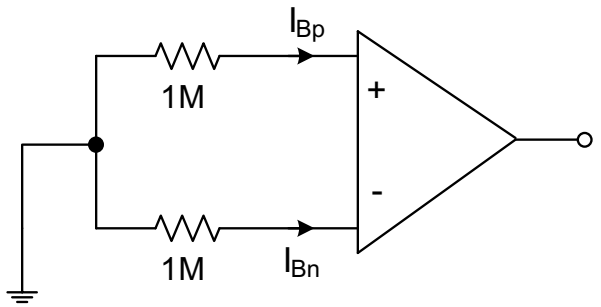
If npn transistors are used, the current flows *into* the input terminals.

If the circuit requires these currents to flow through resistances in the external input circuit, then a voltage will be generated that acts as an input voltage to the op-amp - so it is amplified to give a DC output V_O.



3. The Offset Current

Even if the two bias currents are made to flow through equal resistances at the input, their effects will still not cancel exactly because the bias currents themselves are usually not quite equal in magnitude. The *difference* between the bias currents is called the ***offset current*** $I_{OS} = |I_{Bp} - I_{Bn}|$



$$V_O = A_V|I_{Bp} - I_{Bn}|\times 1\text{M}$$

These currents are particularly troublesome because they are sensitive to temperature

The manufacturer, after measuring a large number of samples, gives us the input bias current which is the average bias current

$$I_B = \frac{I_{Bp} + I_{Bn}}{2}$$

AND they give us the offset current which is the magnitude of the bias current *difference*

$$I_{OS} = |I_{Bp} - I_{Bn}|$$

For example:

For a 741C: $I_B = 80\ nA\ \ typical\ ,\ \ 500\ \ nA\ \ \max$

$I_{os} = 20\ nA\ \ typical\ ,\ \ 200\ \ nA\ \ \max$

In the WORST possible case, this means either $I_{Bp} = 600nA,\ I_{Bn} = 400nA$

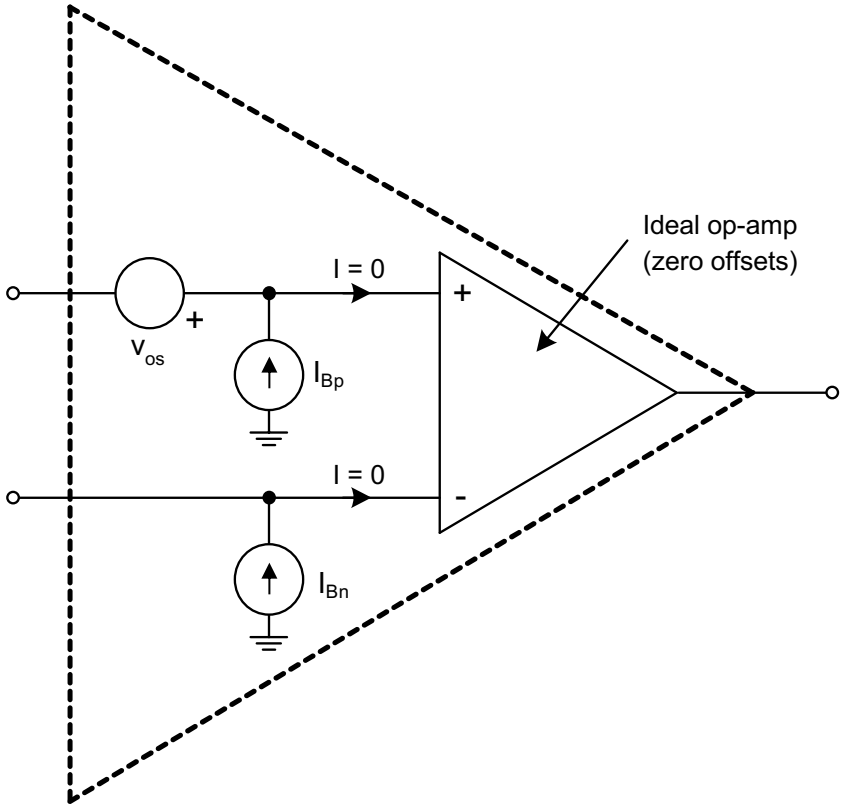
or $I_{Bp} = 400nA,\ I_{Bn} = 600nA$

Summarise this by saying that in all cases

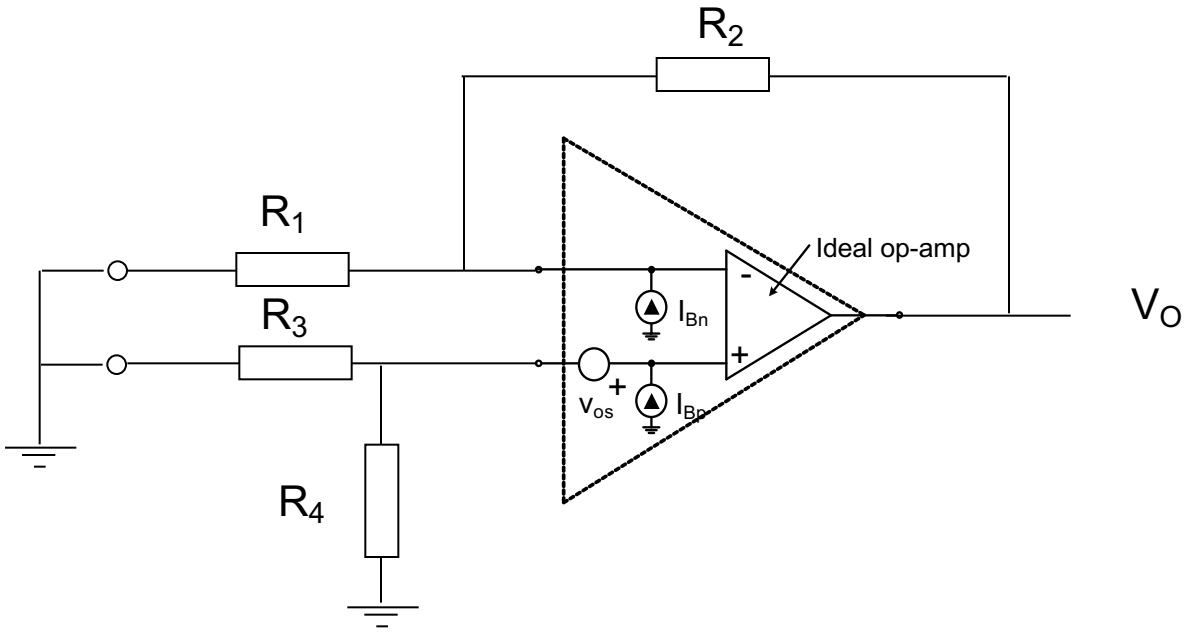
$$I_B - \frac{I_{os}}{2} < [I_{Bp}, I_{Bn}] < I_B + \frac{I_{os}}{2}$$

So the complete model of the op-amp with both offset voltage and bias currents is:

We can use this model to determine the DC offset voltage that will occur in a given circuit.



For example, the differential amplifier circuit gives:

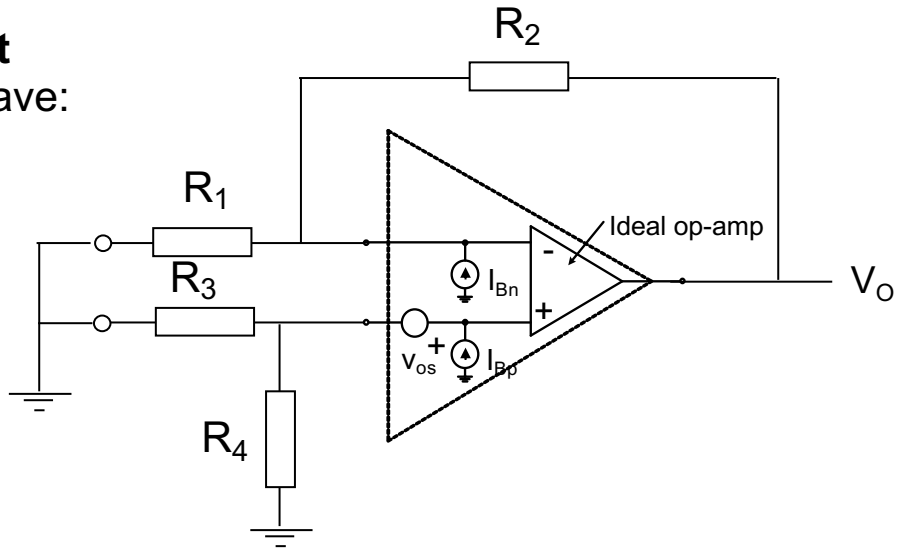


We can determine the contribution to V_o from each source individually using the '**principle of superposition**'

To determine the contribution due to offset bias alone, assume no input signals are being applied so the two inputs are grounded.

To determine **the contribution from the offset voltage**, turn off the sources I_{Bn} and I_{Bp}, we have:

$$V_{O1} = \pm V_{OS}\left(\frac{R_1 + R_2}{R_1}\right)$$



To determine **the contribution from $\mathbf{I_{Bp}}$**, turn off the sources I_{Bn} and V_{OS}, we have:

$$V_{O2} = -I_{Bp}(R_3||R_4)\left(\frac{R_1 + R_2}{R_1}\right)$$

To determine **the contribution from $\mathbf{I_{Bn}}$**, turn off the sources I_{Bp} and V_{OS}, we have:

$$V_{O3} = I_{Bn}R_2$$

The total is:

$$V_O = V_{O1} + V_{O2} + V_{O3} = \pm V_{OS}\left(\frac{R_1 + R_2}{R_1}\right) - I_{Bp}\,(R_3||R_4)\left(\frac{R_1 + R_2}{R_1}\right) + I_{Bn}R_2$$

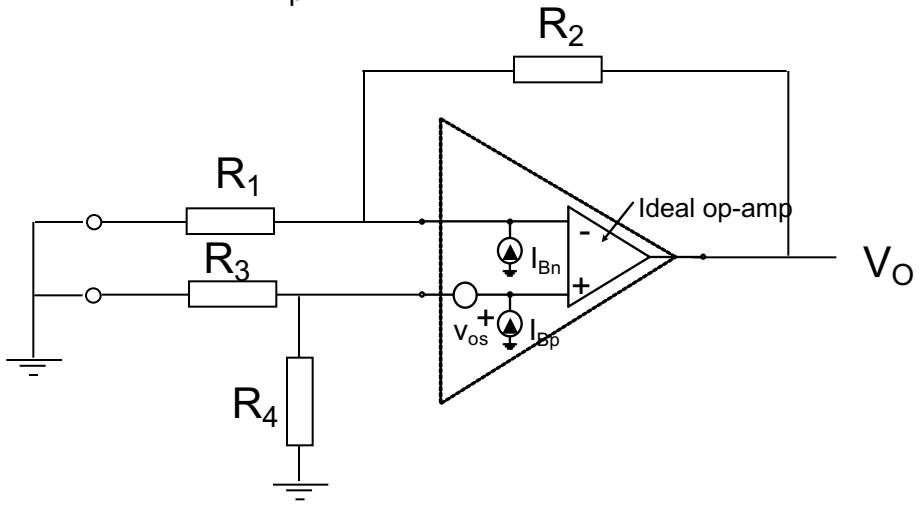
$$V_O = V_{O1} + V_{O2} + V_{O3} = \pm V_{OS}\left(\frac{R_1 + R_2}{R_1}\right) - I_{Bp}\,(R_3||R_4)\left(\frac{R_1 + R_2}{R_1}\right) + I_{Bn}R_2$$

Note that to find the maximum and minimum possible value of V_o we need to consider carefully the appropriate values to use for the sign of V_{os} and the values of I_{Bp} and I_{Bn}

The maximum possible value of V_o will be given by the maximum *positive* value of V_{os}, the *minimum* value of I_{Bp} and the *maximum* value of I_{Bn}

The minimum possible value (i.e. the most negative value) of V_o will be given by the maximum *negative* value of V_{os}, the *maximum* value of I_{Bp} and the *minimum* value of I_{Bn}

If we make the resistance 'seen' by I_{Bp} equal to that 'seen' by I_{Bn} , i.e. $R_1 \parallel R_2 = R_3 \parallel R_4$



Then for $V_O = \pm V_{OS}\left(\frac{R_1+R_2}{R_1}\right) - I_{Bp}\,(R_3||R_4)\left(\frac{R_1+R_2}{R_1}\right) + I_{Bn}R_2$

We find for the later part: $-I_{Bp}(R_3||R_4)\left(\frac{R_1+R_2}{R_1}\right) + I_{Bn}R_2 = R_2[-I_{Bp}(R_3||R_4)\left(\frac{R_1+R_2}{R_1R_2}\right) + I_{Bn}]$

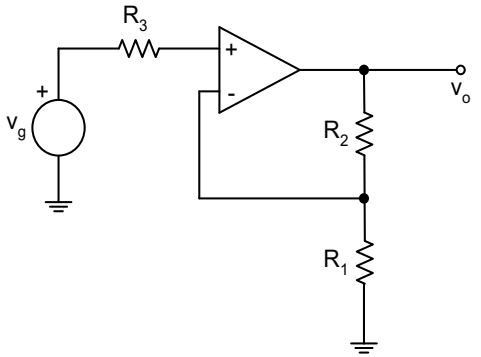
$$= R_2\left[-I_{Bp}(R_3||R_4)\left(\frac{1}{(R_1||R_2)}\right) + I_{Bn}\right] = R_2(I_{Bn} - I_{Bp})$$

The only contribution from the bias currents will be due to the difference between them, i.e. the *offset* current.

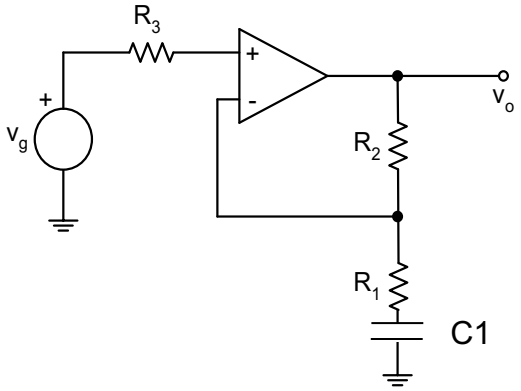
N.B.

It is important to remember that we are dealing here with DC quantities for V_{OS} and I_{Bp} and I_{Bp}. ***The analysis must consider only DC paths***. If capacitors are present then the analysis must treat them as OPEN CIRCUIT because they block DC.

So in this circuit we make $R_3 = R_1//R_2$ so that the only contribution from the bias currents will be due to the difference between them



But in this circuit we make $R_3 = R_2$ because the capacitor blocks the DC path through R_1



Welcome Timur to give you the feedback of HW2!

Week 12 will be the first revision class delivered by Suneel and Timur

See you in Week 13