New lecturer:

My name: Dr Timur Saifutdinov

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Office Hours: 12:00 – 14:00 Wednesday,

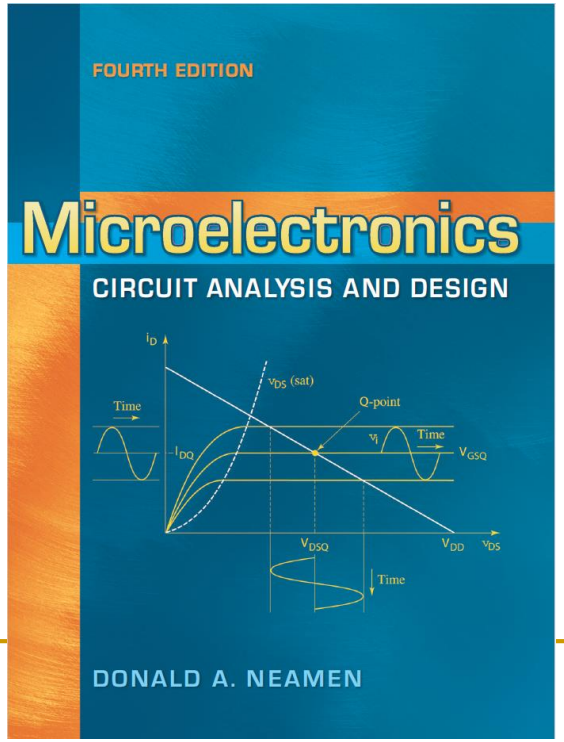
Address: SIP, North Campus, SC465

Main textbook (very useful!!!):

Title: Microelectronics: Circuit Analysis and Design 4th ed. (3rd ed. should work)

Author: Donald A. Neamen

Where to find: XJTLU Library and …



Plan for the next five weeks

W4 (Tutorial session): Lecture on Differential Amplifiers

W5: Lecture on Current Mirror and Active Load circuits

W6: Feedback on HW1 (Dr Suneel Kommuri) + Lecture on Introduction to Feedback

W7: Lecture on Feedback Amplifiers ← HW2 Assignment release

W8: Reading week (Not a holiday!) ← HW2 Submission deadline

W9: Frequency Response and Stability Analysis of Amplifier Circuits with Feedback ← HW2 Submission cut-off

W9+ (Tutorial session): Dr. Xiaoyang Chen will take over the module

W10 or 11: I will return to give Feedback on HW2

Differential Amplifiers

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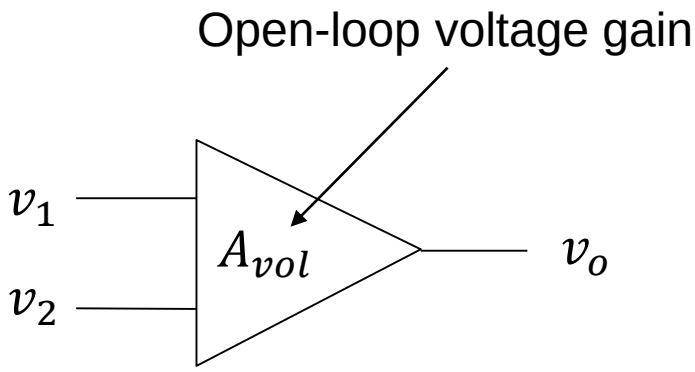
Outline

- Part 1: Introduction to Differential Amplifiers
  - Describe the characteristics and terminology of the ideal differential amplifier.
- Part 2: Basic BJT Differential Pair
  - Operational principle and analysis of the basic bipolar differential amplifier.
- Part 3: Exercises
  - Practice differential amplifier analysis skills (necessary for the assessment)

Part 1: Introduction to Differential Amplifiers

The Differential Amplifier

- is an amplifier designed to produce an output voltage v_o that represents an amplified version of the difference between two input signals v_1 and v_2. The difference between v_1 and v_2 is called 'differential-mode' signal:



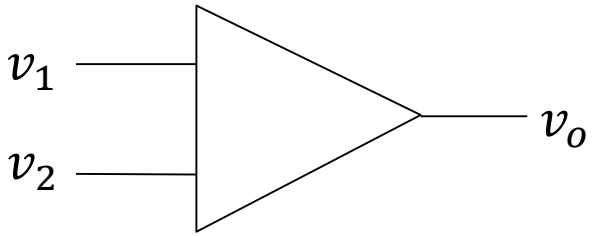
$$v_o^{ideal} = A_{vol}(v_1 - v_2)$$

In an ideal differential amplifier, if the same signal voltage is applied to both inputs at the same time , then $v_1 = v_2$ and v_o should be zero. A signal that appears on both inputs at the same time in this way is called a 'common-mode' signal.

Unfortunately, in practice it is found that a small output voltage will be produced in response to a common mode signal. However, a good differential amplifier would have a high gain for the differential signal but a low gain for the common mode signal. This figure of merit is expressed as the 'Common Mode Rejection Ratio' of the amplifier (CMMR)

Input modes

Suppose the input signals to a differential amplifier v_1 and v_2 consist of a common-mode voltage v_{cm} applied to both inputs and a difference voltage v_d shared between them, then



$$v_1 = v_{cm} + \frac{v_d}{2} \qquad v_2 = v_{cm} - \frac{v_d}{2}$$

so $v_d = v_1 - v_2$

Note *that the differential-mode signal is simply equal to the difference between the values of* v_1 *and* v_2

and $v_{cm} = \dfrac{v_1 + v_2}{2}$

but the common-mode signal is equal to the average value of v_1 *and* v_2

For example, if $v_1 = 50$ μV and $v_2 = -50$ μV then $v_d = 100$ μV and $v_{cm} = 0$ μV

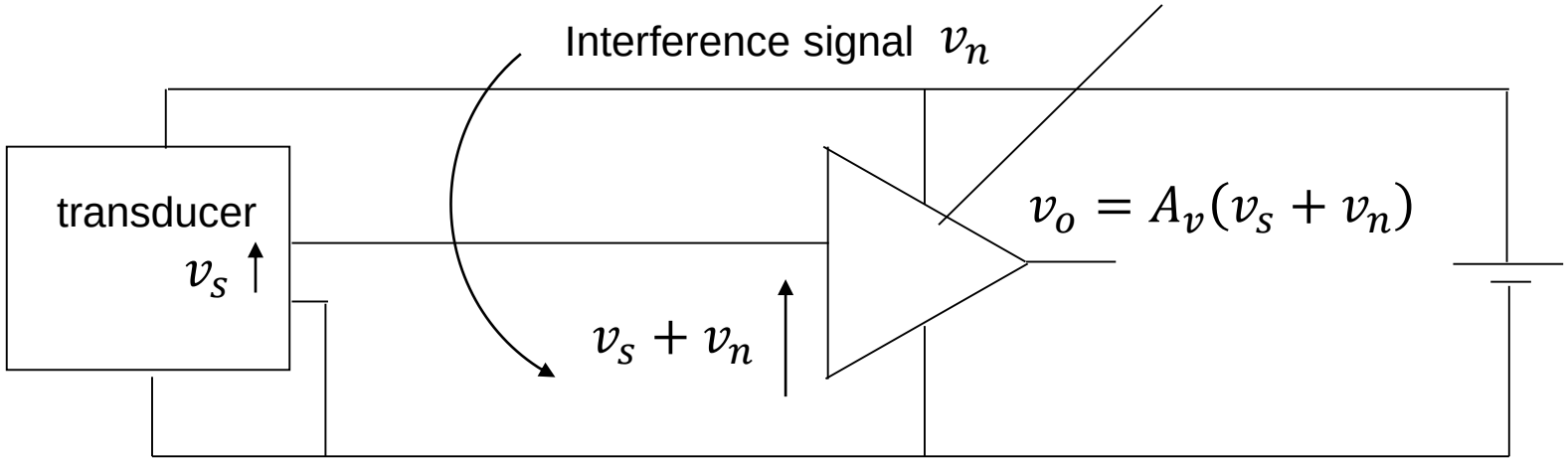
Or, if $v_1 = 100$ μV and $v_2 = 0$ μV, then $v_d = 100$ μV and $v_{cm} = 50$ μV

Now, the actual output is found as: $v_o = A_d v_d + A_{cm} v_{cm}$

Common-mode signal

What is this 'common-mode' signal?

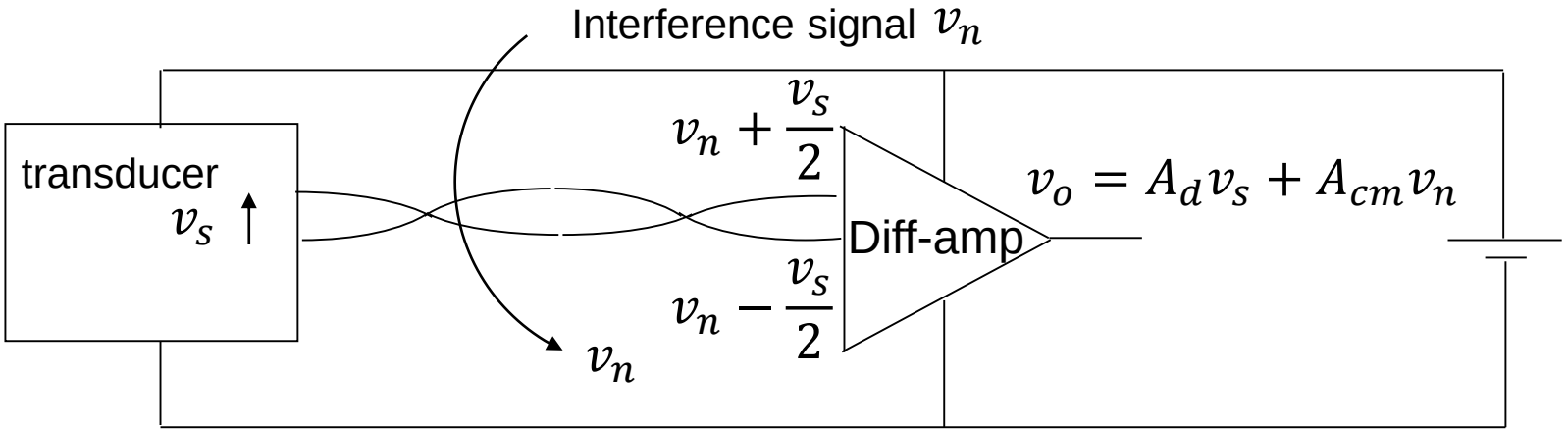
Ordinary single input amp



In practice, it is often required to amplify very small electrical signals and unwanted interference signals ('noise') can be 'picked up'. Often the noise signal can completely obscure the required signal and an ordinary amplifier would not improve the situation, because it will amplify both the noise and the required signal by the same amount.

Common-mode signal

The interference signal can be reduced considerably if a differential amplifier is used and the wires are twisted together so that the area of the pickup loop is minimised.



Only a 'common-mode' signal is now picked up and this should not be amplified by the differential amplifier.

A good differential amplifier will not amplify the **common-mode signal (the noise)** but will amplify the **differential-mode signal (the required signal)**. In this way the signal/noise ratio is greatly improved.

Common mode rejection ratio, CMRR

This is an important figure of merit for a differential amplifier that tells us how good it is at rejecting the unwanted common mode signal (CM) relative to the differential signal that we want to amplify (DM). We clearly want a high differential gain and a low common mode gain.

As a measure of this, we define $$CMRR = \left|\frac{A_d}{A_{cm}}\right|$$

Usually, it is measured in decibel (dB): $$CMRR\Big|_{dB} = 20\log_{10}\left|\frac{A_d}{A_{cm}}\right|$$

The aim is to have CMRR as large as possible.

Commercial op-amps offer:

741 $CMRR|_{dB}$ = 70 – 90 dB

OP07 $CMRR|_{dB}$ = 94 – 106 dB

How big is the actual ratio?

741 $CMRR =$

OP07 $CMRR =$

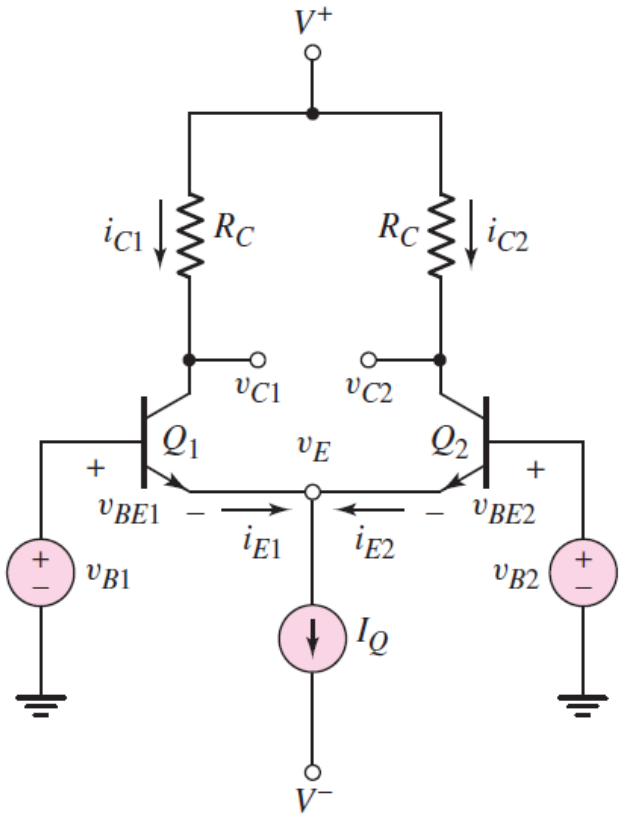
The differential signals are amplified several thousand times more than the common mode signals.

Part 2:

Basic BJT Differential Pair and Its DC&AC Analysis

The basic BJT differential pair

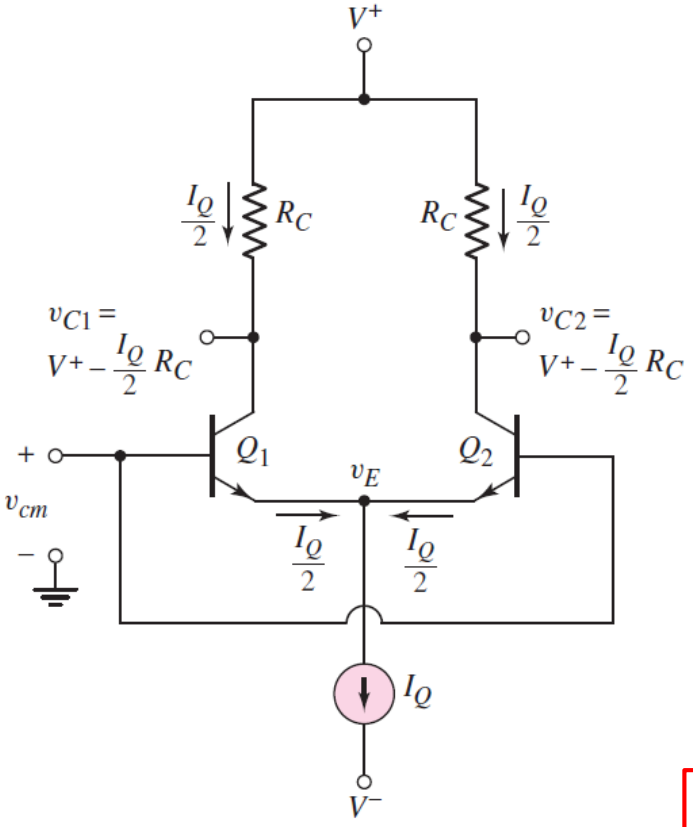
The basic BJT differential-pair configuration:



- Two identical or matched transistors Q1 and Q2 (common emitter connection);
- Positive and negative voltage supply V^+ and V^-;
- Constant current source I_Q to bias transistors;
- Two identical resistors R_C;
- Two ideal voltage sources v_{B1} and v_{B2} as inputs;
- Two terminals v_{C1} and v_{C2} as output.

By design, transistors *Q*1 and *Q*2 are to remain biased in the forward-active region.

Qualitative analysis: common-mode input voltage



Common emitter voltage: $v_E = v_{cm} - V_{BE}(on)$

Emitter currents: $i_{E1} = i_{E2} = \frac{I_Q}{2}$

If base currents negligible: $i_{C1} \cong i_{E1}$

and $i_{C2} \cong i_{E2}$

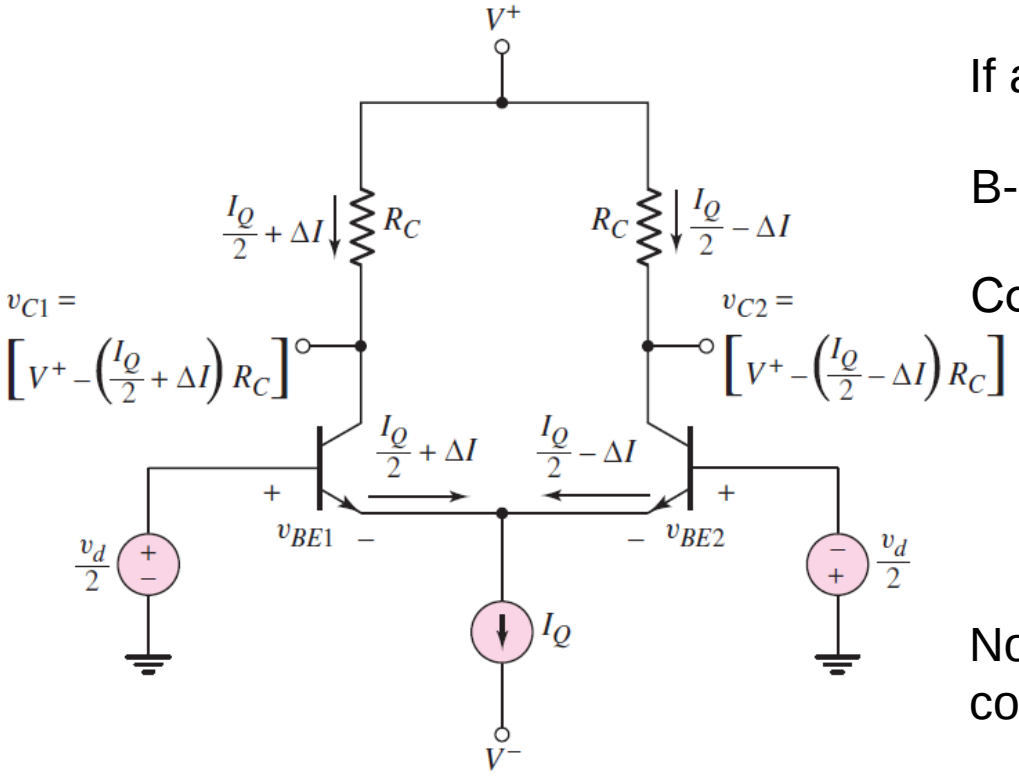
The current going through collectors/emitters in common-mode is called **Quiescent current**

Collector voltages identical: $v_{C1} = V^+ - \frac{I_Q}{2} R_C = v_{C2}$

For an applied common-mode voltage, I_Q splits evenly between *Q*1 and *Q*2 and the difference between v_{C1} and v_{C2} is zero

– common-mode output

Qualitative analysis: differential-mode input voltage



If a diff-mode input voltage v_d is applied

B-E voltages of Q1 and Q2: $v_{BE1} > v_{BE2}$

Collectors' currents change by $\pm\Delta I$:

$$i_{C1} = \frac{I_Q}{2} + \Delta I$$

and $$i_{C2} = \frac{I_Q}{2} - \Delta I$$

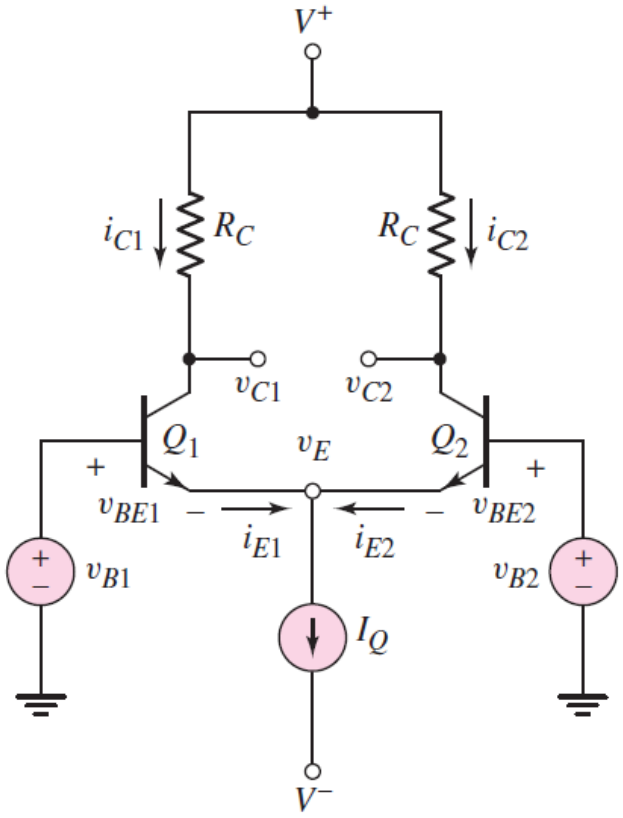
Now, the voltage difference between collectors appears:

$$v_{C2} - v_{C1} = \left[V^+ - \left(\frac{I_Q}{2} - \Delta I\right)R_C\right] - \left[V^+ - \left(\frac{I_Q}{2} + \Delta I\right)R_C\right] = 2 \cdot \Delta I \cdot R_C$$

A voltage difference is created between v_{C2} and v_{C1} when a differential-mode input voltage is applied **– differential-mode output**

Example:

Task: Determine the quiescent collector current and collector-emitter voltage in a diff-amp for common-mode input signals v_{cm} =0 V; -5 V; and +5 V.



Circuit parameters:
$V^+ = 10$ V;
$V^- = -10$ V;
$I_Q = 1$ mA;
$R_C = 10$ kOhm.

Transistor parameters:
$\beta = \infty$,
$V_A = \infty$,
$V_{BE}(on) = 0.7$ V

Solution:

1. We know that collector currents: $i_{C1} = i_{C2} = \frac{I_Q}{2} = 0.5$ mA;

2. Therefore, collector voltages are found as:

$$v_{C1} = v_{C2} = V^+ - i_{C1}R_C = 10 - (0.5)(10) = 5 \text{ V};$$

3. For $v_{cm} = 0$: $v_E = -V_{BE}(on) = -0.7$ V

and $v_{CE1} = v_{C1} - v_E = 5 - (-0.7) = 5.7$ V;

4. For $v_{cm} = -5$ V and $v_{cm} = +5$ V: *practice on your own!*

As the common-mode input voltage varies, the collector-emitter voltage varies, which means that the *Q*-point changes.

DC transfer characteristics of the basic diff-amp

From previous lectures you know: $i_{C1} = I_S \exp\left(\frac{v_{BE1}}{V_T}\right)$ and $i_{C2} = I_S \exp\left(\frac{v_{BE2}}{V_T}\right)$

From previous analysis you know: $I_Q = i_{C1} + i_{C2}$ or $I_Q = I_S\left[\exp\left(\frac{v_{BE1}}{V_T}\right) + \exp\left(\frac{v_{BE2}}{V_T}\right)\right]$

Normalizing i_{C1} and i_{C2} wrt I_Q gives: $\frac{i_{C1}}{I_Q} = \frac{1}{1 + \exp\left(\frac{v_{BE2} - v_{BE1}}{V_T}\right)}$

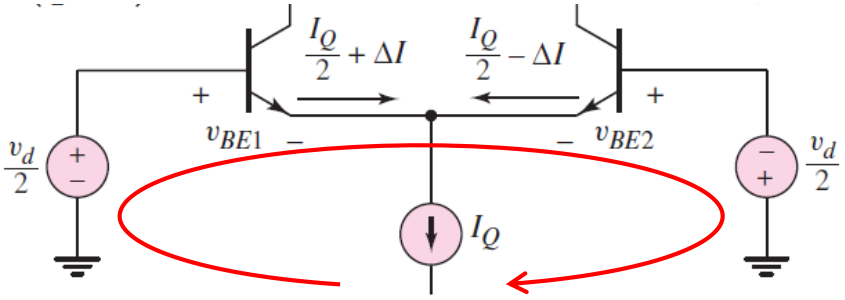
and $\frac{i_{C2}}{I_Q} = \frac{1}{1 + \exp\left(\frac{-(v_{BE2} - v_{BE1})}{V_T}\right)}$

Recognizing that $v_{BE1} - v_{BE2} \equiv v_d$, collector currents are:

$$i_{C1} = \frac{I_Q}{1 + \exp\left(\frac{-v_d}{V_T}\right)}$$

and

$$i_{C2} = \frac{I_Q}{1 + \exp\left(\frac{+v_d}{V_T}\right)}$$



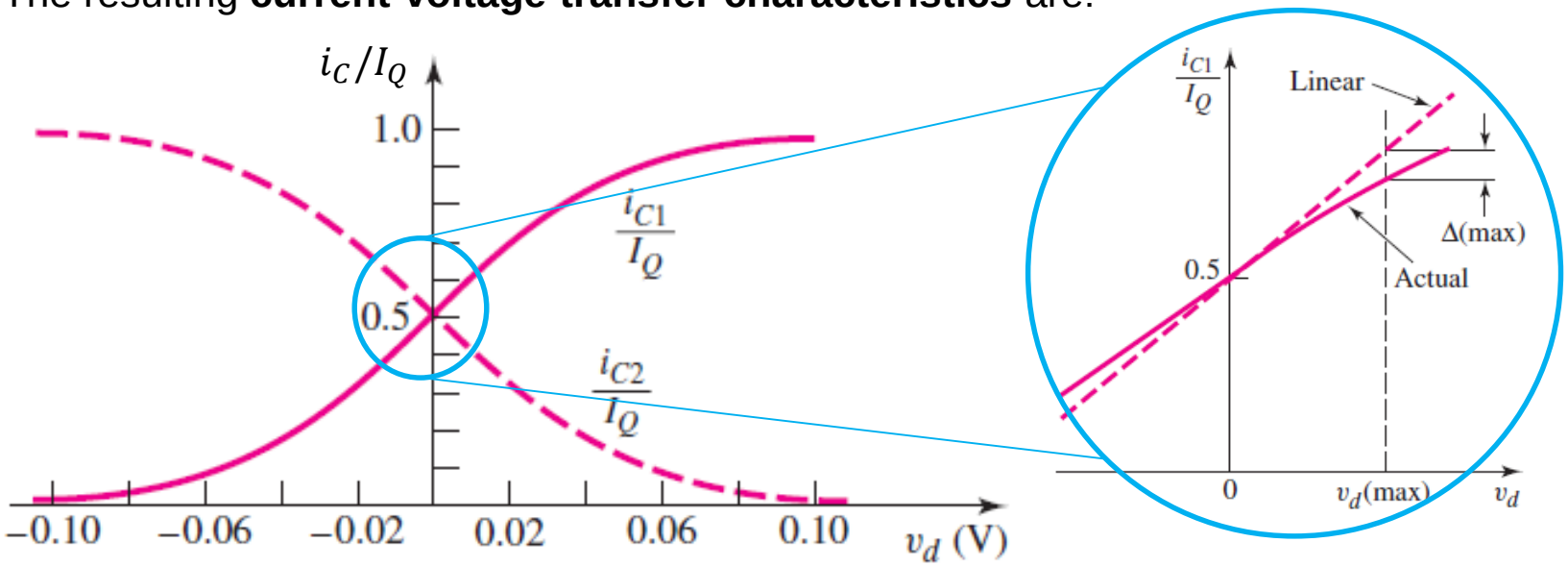
KVL: $\frac{v_d}{2} - v_{BE1} + v_{BE2} + \frac{v_d}{2} = 0 \quad \Rightarrow v_{BE1} - v_{BE2} = v_d$

Basic **current-voltage characteristics** of the diff-amp

DC transfer characteristics of the basic diff-amp

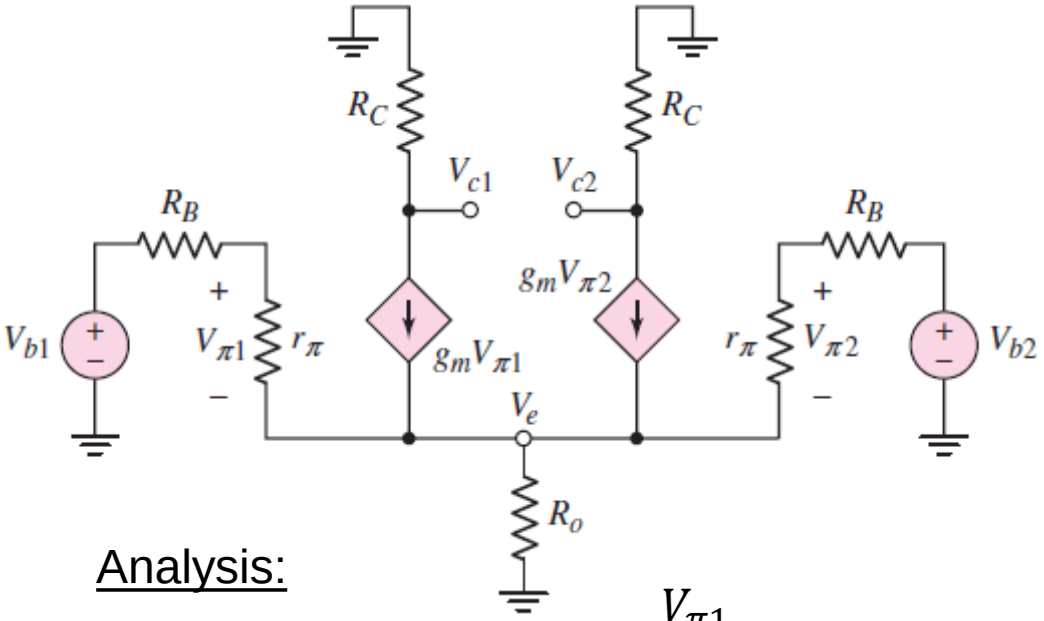
Normalizing i_{C1} and i_{C2} wrt I_Q will give: $\frac{i_{C1}}{I_Q} = \frac{1}{1+\exp\left(\frac{-v_d}{V_T}\right)}$ and $\frac{i_{C2}}{I_Q} = \frac{1}{1+\exp\left(\frac{+v_d}{V_T}\right)}$

The resulting **current-voltage transfer characteristics** are:



- The gain of the diff-amp is nonlinear for wide range of diff-mode inputs – v_d must be kept small to maintain a linear operation;
- As the magnitude of v_d becomes sufficiently large, the second transistor effectively turns off – this characteristic is used in the emitter-coupled logic (ECL) family of digital logic circuits

Small-signal equivalent circuit analysis – output voltage



Our assumptions:

- Constant current source is never ideal – represented by R_0;
- Input voltage source resistance is non-zero – represented by R_B;
- Both transistors are biased at the same quiescent current, so that:

$r_{\pi 1} = r_{\pi 2} \equiv r_\pi$ and $g_{m1} = g_{m2} \equiv g_m$

Analysis:

1. KCL equation at node V_e: $\dfrac{V_{\pi 1}}{r_\pi} + g_m V_{\pi 1} + g_m V_{\pi 2} + \dfrac{V_{\pi 2}}{r_\pi} = \dfrac{V_e}{R_o}$

2. Representing $g_m = \beta / r_\pi$: $V_{\pi 1}\left(\dfrac{1+\beta}{r_\pi}\right) + V_{\pi 2}\left(\dfrac{1+\beta}{r_\pi}\right) = \dfrac{V_e}{R_o}$

3. From the circuit we see that: $\dfrac{V_{\pi 1}}{r_\pi} = \dfrac{V_{b1} - V_e}{r_\pi + R_B}$ and $\dfrac{V_{\pi 2}}{r_\pi} = \dfrac{V_{b2} - V_e}{r_\pi + R_B}$

4. Solving (3.) for $V_{\pi 1}$ and $V_{\pi 2}$ and substituting into (2.): $(V_{b1} + V_{b2} - 2V_e)\left(\dfrac{1+\beta}{r_\pi + R_B}\right) = \dfrac{V_e}{R_o}$

Small-signal equivalent circuit analysis – output voltage

5. Solving (4.) for V_e will give: $V_e = \dfrac{V_{b1} + V_{b2}}{2 + \dfrac{r_\pi + R_B}{(1+\beta)R_o}}$

6. One-sided output at the collector of Q2: $V_o = V_{c2} = -(g_m V_{\pi 2})R_C = -\dfrac{\beta R_C (V_{b2} - V_e)}{r_\pi + R_B}$

Why? Recall: $g_m = \beta / r_\pi$ and $\dfrac{V_{\pi 2}}{r_\pi} = \dfrac{V_{b2} - V_e}{r_\pi + R_B}$

7. Substituting (5.) into (6.) will give: $V_o = \dfrac{-\beta R_C}{r_\pi + R_B} \left\{ \dfrac{V_{b2}\left[1 + \dfrac{r_\pi + R_B}{(1+\beta)R_o}\right] - V_{b1}}{2 + \dfrac{r_\pi + R_B}{(1+\beta)R_o}} \right\}$

8. Considering that $V_{b1} = V_{cm} + \dfrac{V_d}{2}$ and $V_{b2} = V_{cm} - \dfrac{V_d}{2}$, (7.) can be transformed to:

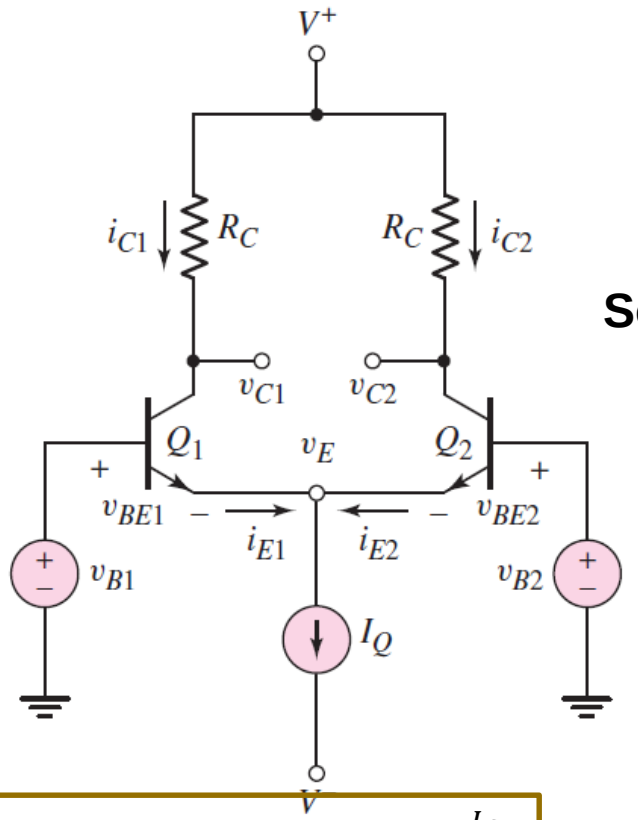
$$V_o = A_d V_d + A_{cm} V_{cm}$$

9. The voltage output will be: $V_o = \dfrac{\beta R_C}{2(r_\pi + R_B)} \cdot V_d - \dfrac{\beta R_C}{r_\pi + R_B + 2(1+\beta)R_o} \cdot V_{cm}$

Finally we can see the reason behind non-zero common-mode output. What is it?

Example:

Task: Determine the differential- and common-mode gains and the common-mode rejection ratio of a diff-amp in dB.



Hint: $\beta = r_\pi g_m$ and $g_m = \frac{I_C}{V_T}$

Circuit parameters:
$V^+ = 10$ V;
$V^- = -10$ V;
$I_Q = 0.8$ mA;
$R_C = 12$ kOhm.

Transistor parameters:
$\beta = 100$;
$V_A = \infty$;
$R_0 = 25$ kOhm;
$R_B = 0$ Ohm.

Solution (for one-sided output v_{C2}):

1. From the previous slide:

$$A_d = \frac{\beta R_C}{2(r_\pi + R_B)} = \frac{g_m R_C}{2} = \frac{i_{C2} R_C}{2V_T} = \frac{I_Q R_C}{4V_T} =$$

$$A_{cm} = \frac{-\beta R_C}{r_\pi + R_B + 2(1+\beta)R_0} = \frac{-\beta R_C}{\frac{2\beta V_T}{I_Q} + 2(1+\beta)R_0} =$$

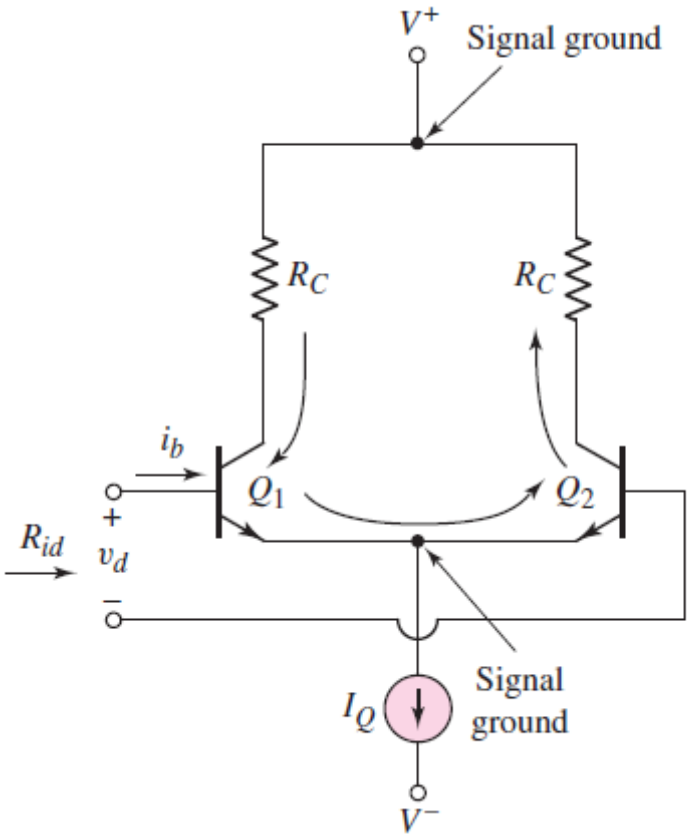
2. To find CMRR: $CMRR = \left|\frac{A_d}{A_{cm}}\right| =$

3. CMRR in dB: $CMRR|_{dB} = 20 \log_{10} CMRR =$

In practice, $CMRR|_{dB} > 80$ dB is a design goal for a diff-amp. Then, the aim is to design a better diff-amp than considered in this example. How can we achieve this?

Input impedance of the basic diff-amp

The input resistance (or impedance) determines the loading of the circuit on the signal source – the higher the better.



There are:

- **Differential-mode input resistance** – the effective resistance between the two input base terminals when a differential-mode signal is applied:

  For the voltage source current: $i_s = i_b = v_d/2r_\pi$

  Therefore, the internal resistance of the diff-amp in **differential-mode**: $R_{id} = \frac{v_d}{i_s} = 2r_\pi$

  Obviously, the higher the impedance the better. How do you think we can increase it? Options:

  1. Since $r_\pi = \frac{2\beta V_T}{I_Q}$: $R_{id} = \frac{4\beta V_T}{I_Q}$

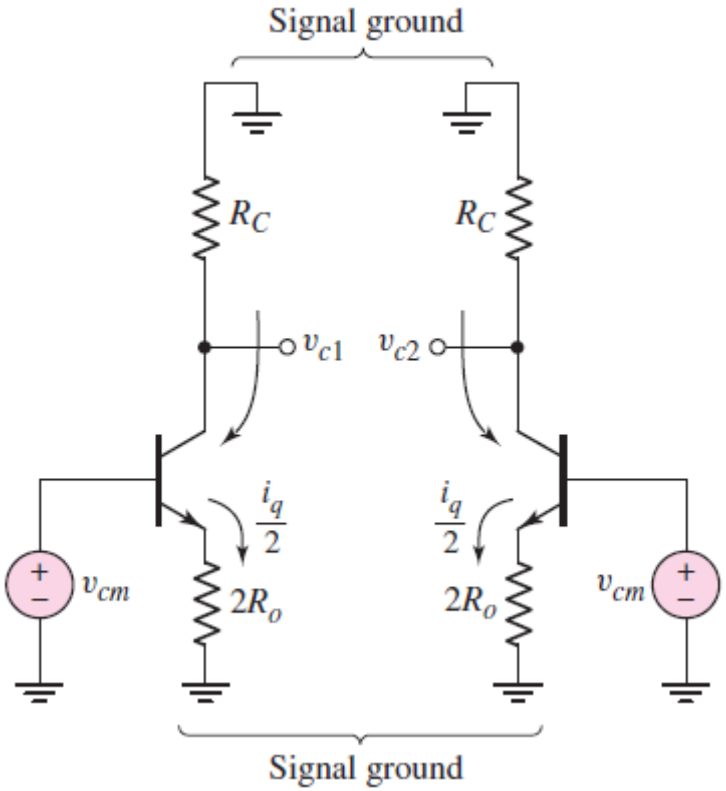
  Therefore, we can choose small I_Q but this will decrease the diff-mode gain.

  2. Use emitter resistors. In this case, internal resistance become: $R_{id} = 2[r_\pi + (1+\beta)R_E]$

The diff-mode input resistance increases significantly when emitter resistors are included. Additionally, a larger diff-mode voltage range (>20 mV) may be applied to the diff-amp.

Input impedance of the basic diff-amp

The input resistance (or impedance) determines the loading of the circuit on the signal source – the higher the better.



There are:

- **Common-mode input resistance** – the effective resistance between the two input base terminals when a common-mode signal is applied:

  For the voltage source current: $i_s = i_{b1} + i_{b2} = 2i_{b1}$

  Therefore, the internal resistance of the diff-amp in common-mode:

$$R_{icm} = \frac{v_{cm}}{i_s} = \frac{i_{b1}r_\pi + i_{b1}(\beta+1)2R_0}{2i_{b1}} = \frac{r_\pi}{2} + (\beta+1)R_0$$

Task: Calculate the diff- and comm-mode input resistances for the diff-amp from the previous example (slide 20):

$$R_{id} =$$

$$R_{icm} =$$

Common-mode input resistance is essentially very large in the basic BJT diff-amp configuration

Summary – basic BJT differential pair

Differential mode

Input resistance

$$R_{id} = 2r_\pi = \frac{4\beta V_T}{I_Q}$$

Voltage gain

$$A_d = \frac{\beta R_C}{2(r_\pi + R_B)}$$

Common mode

Input resistance

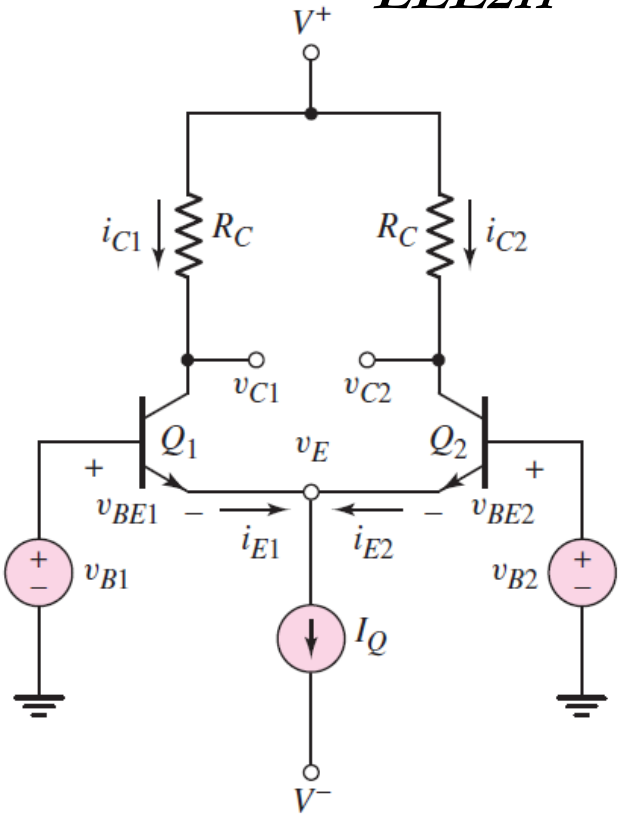
$$R_{icm} = \frac{r_\pi}{2} + (\beta + 1)R_0 \approx \beta R_0$$

Voltage gain

$$\mathrm{A_{cm}} = \frac{-\beta R_C}{r_\pi + R_B + 2(1+\beta)R_0} \approx -\frac{R_C}{2R_0}$$

Common Mode Rejection Ratio

$$CMRR = \left|\frac{A_d}{A_{cm}}\right| \approx \frac{(1+\beta)R_0}{r_\pi + R_B}$$



Questions to reflect:

- How to reduce comm-mode gain?
- How to increase diff-mode gain?
- How to increase input resistances?
- How to improve CMRR?
- Is there any conflict?

Part 3:

Exercises

Exercise 1 – Design for purpose

Task: Determine the required value of the constant current source resistance for the diff-amp to produce common-mode rejection ration of $80\ dB$.

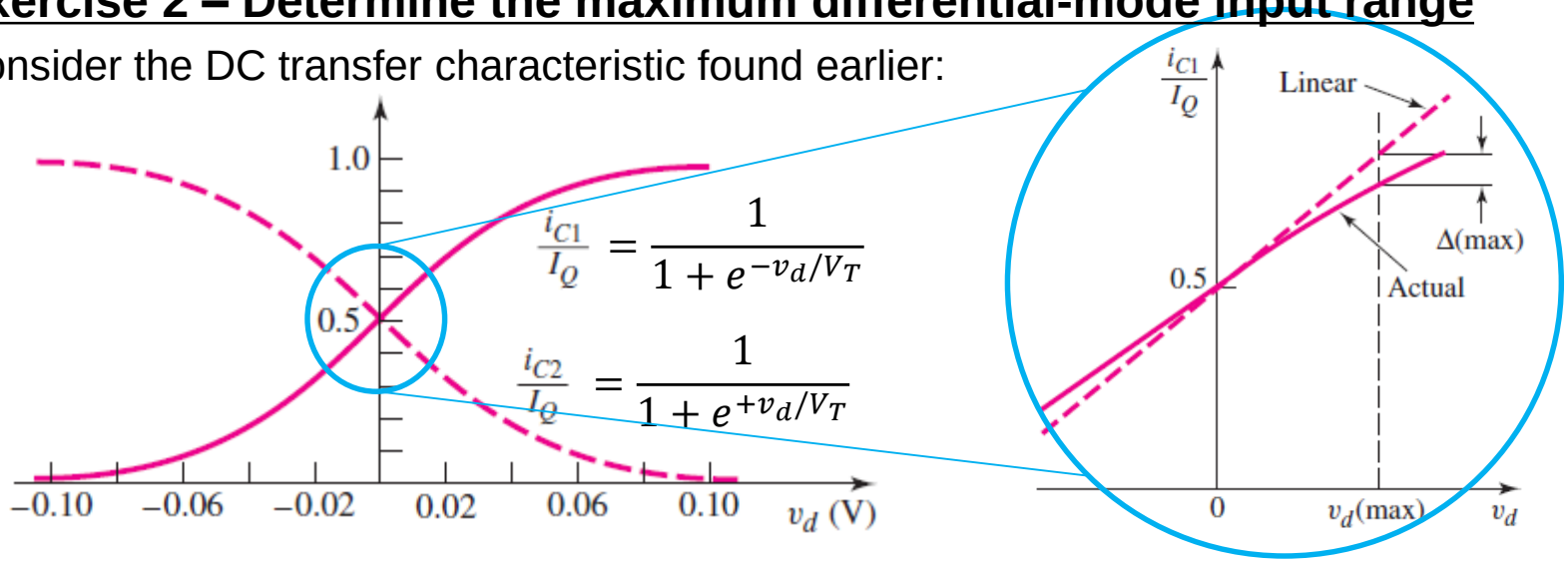
Circuit parameters:
$V^+ = 10$ V;
$V^- = -10$ V;
$I_Q = 0.8$ mA;
$R_C = 12$ kOhm.

Transistor parameters:
$\beta = 100$;
$V_A = \infty$;
$R_B = 0$ Ohm.

Solution:

Exercise 2 – Determine the maximum differential-mode input range

Consider the DC transfer characteristic found earlier:



Task: Determine the value of v_d^{max} such that the difference between the linear approximation and the actual curve is 1 percent.

Solution:

Exercise 2 – Determine the maximum differential-mode input range

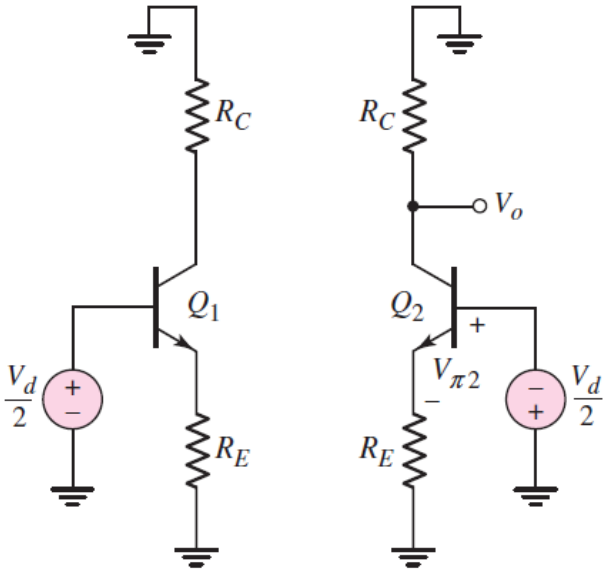
Solution (continue):

Look at the task again and think – what is particularly interesting about the result?

Exercise 3 – Diff-mode voltage gain and input resistance with emitter resistors

Task: Determine the one-sided differential-mode voltage gain and internal resistance of the basic diff-amp with and without emitter resistance.

Hint – consider differential-mode half circuits below:



Transistor parameters:
$\beta = 100.$

Circuit parameters:
$I_Q = 0.5$ mA;
$R_C = 10$ kOhm;
$R_E = 500$ Ohm.

Solution:

In this lecture we have:

- Introduced the concept of a differential amplifier
- Identified ‘common mode’ and ‘differential’ voltage gains
- Introduced the common mode rejection ratio (CMRR)
- Analysed the basic BJT differential pair amplifier circuit to determine its D.C. biasing condition
- Analysed the basic BJT differential pair amplifier circuit to determine its common mode and differential input impedances and common mode and differential voltage gains.
- Exercised to practice diff-amp analysis skills

Announcements:

- Next lecture:
  - Group 1: 15-OCT, Week 5, Tuesday @ 9:00 in EB138;
  - Group 2: 16-OCT, Week 5, Wednesday @ 17:00 in EB138.

- For more practice on numerical problems:
  - Refer to: The textbook (details in slide 1)
  - Exercises: Chapter 11:
    - Ex 11.1; Ex 11.2; Ex 11.3; Ex 11.5; Ex 11.6.

Thank you for your attention…..

The End