EEE104 – Digital Electronics (I)

Lecture 16

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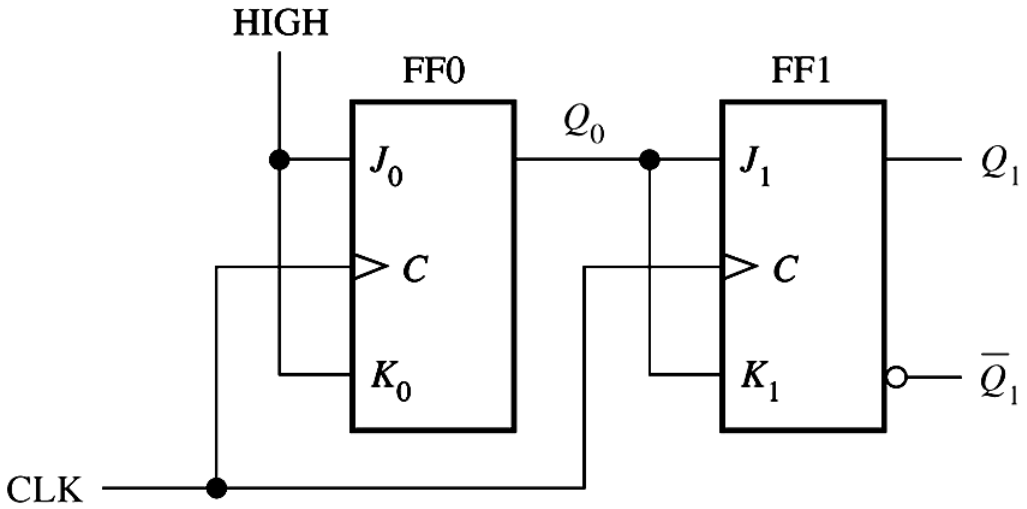
XJTLU

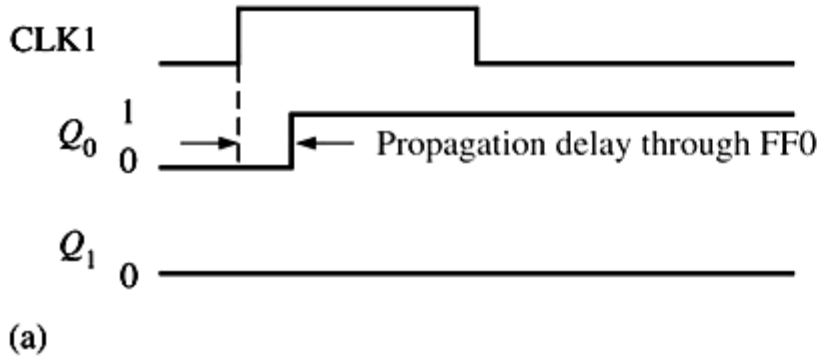
In This Session

- Synchronous Counters

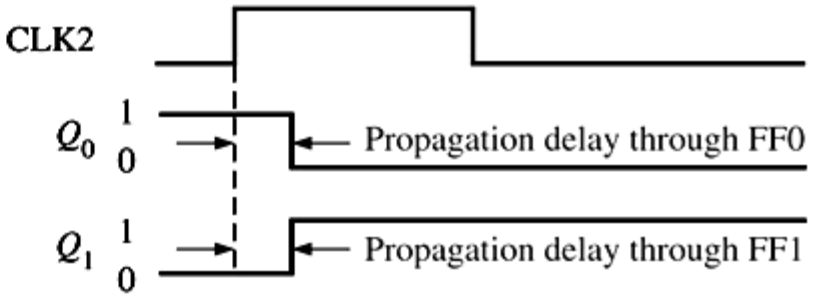
2-Bit Synchronous Binary Counters



- All the flip-flops are clocked by CLK.
- J and K of FF1 are connected to Q_0 output of FF0.

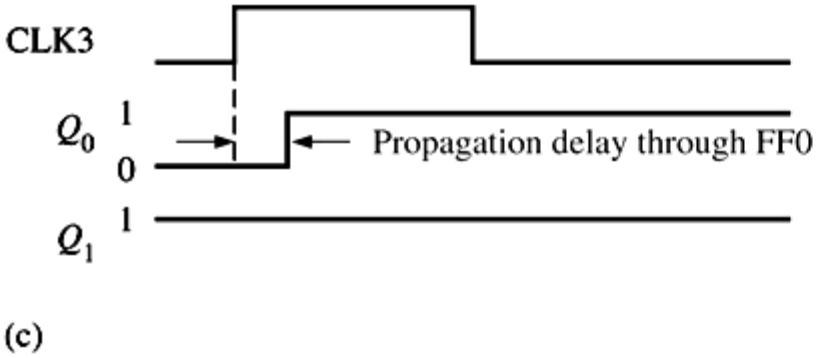


(a)

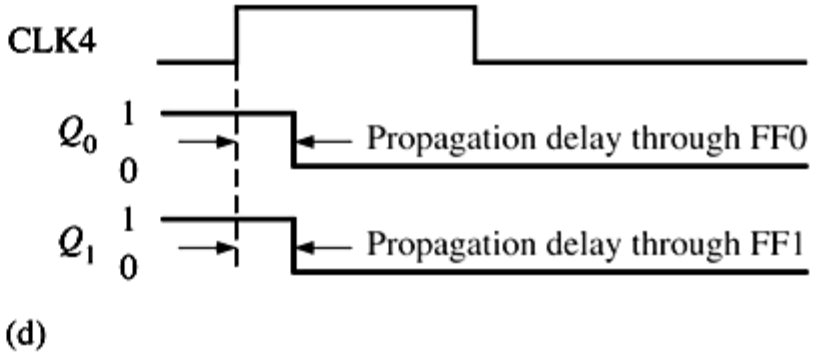


(b)

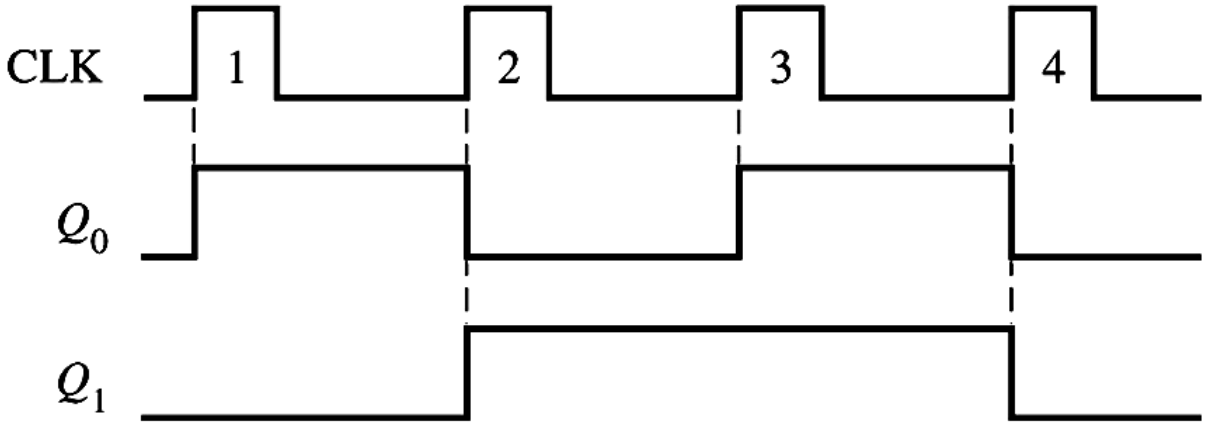
2-Bit Synchronous Binary Counters



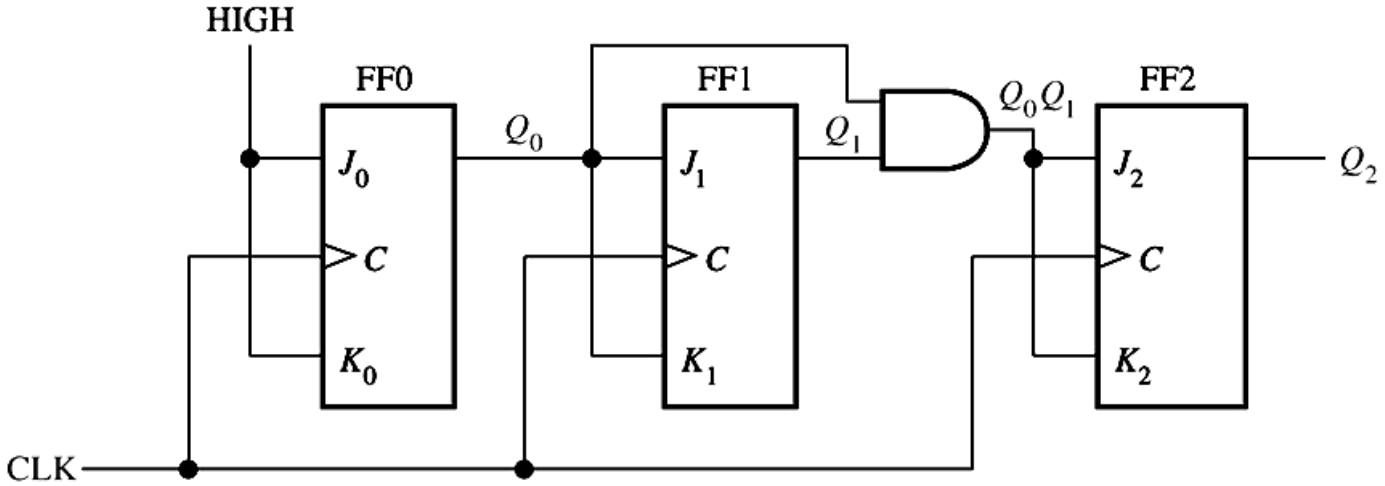
(c)

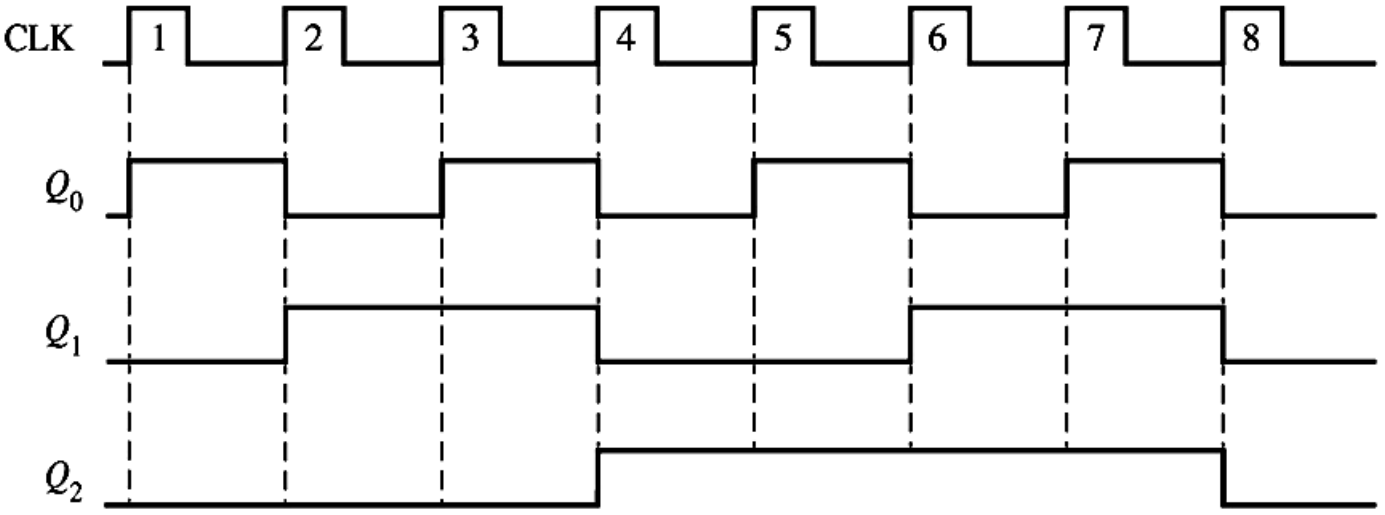


(d)



3-Bit Synchronous Binary Counters

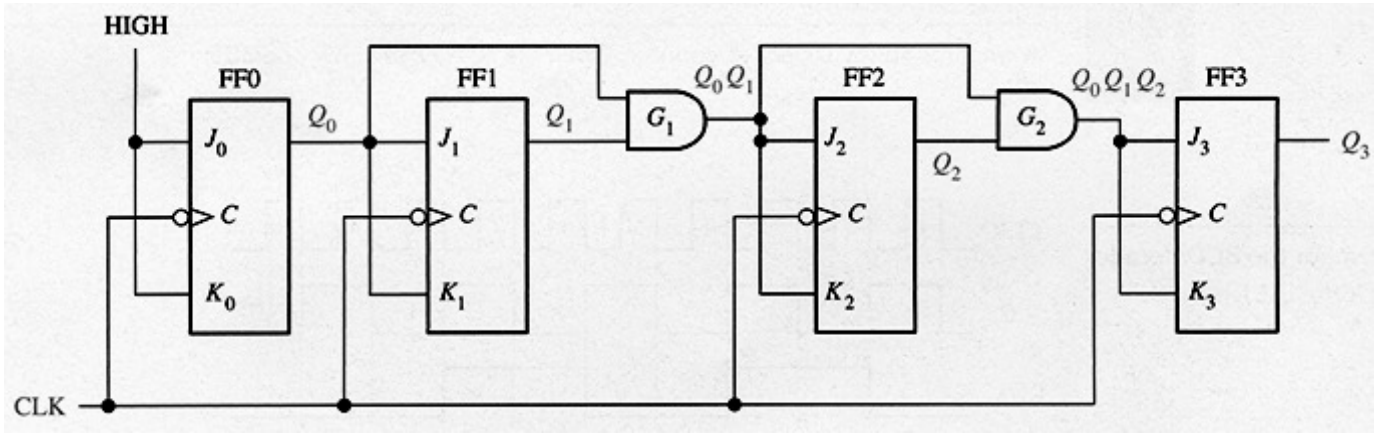




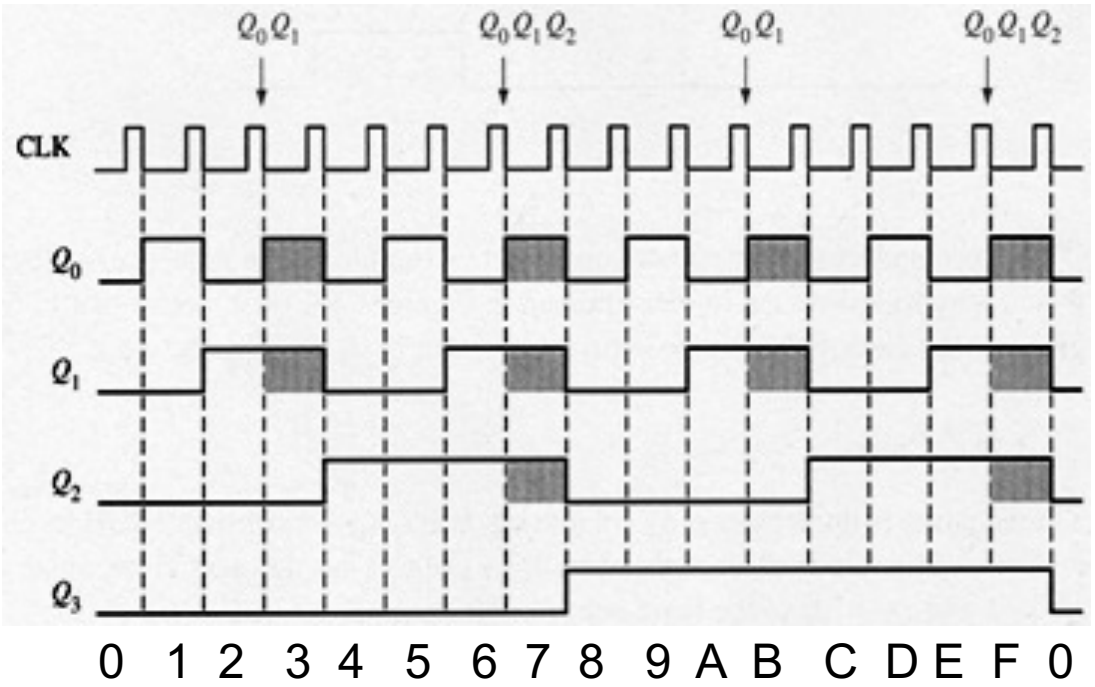
Q2	Q1	Q0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

Q_2 is toggled at states 011 and 111. So $J_2=K_2=Q_0Q_1$

4-Bit Synchronous Binary Counters



Q3	Q2	Q1	Q0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1



Q_3 is toggled at states 0111 and 1111. So $J_3=K_3=Q_0Q_1Q_2$

4-Bit Synchronous Decade Counters

Q3	Q2	Q1	Q0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1

- Q_0 is always toggled.
- Q_1 is toggled at states 0001, 0011, 0101, 0111.
- Q_2 is toggled at states 0011, 0111.
- Q_3 is toggled at states 0111, 1001.

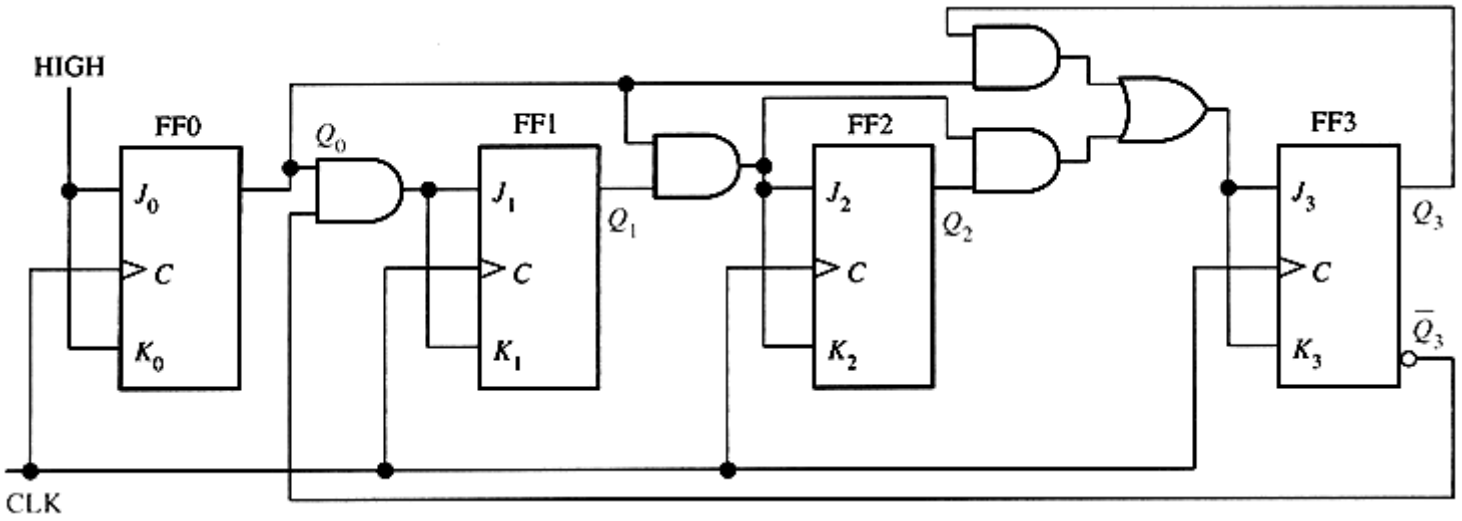
$$J_0 = K_0 = 1$$

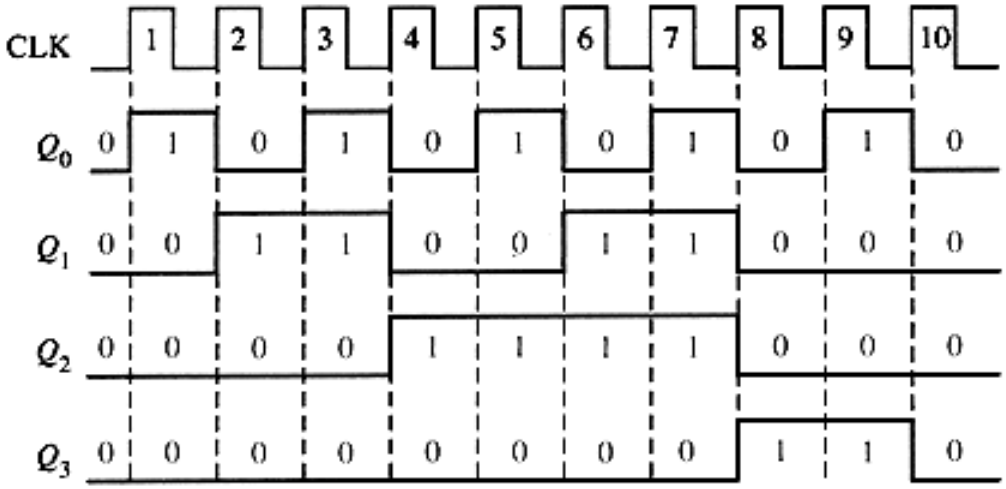
$$J_1 = K_1 = Q_0\bar{Q}_3$$

$$J_2 = K_2 = Q_0Q_1$$

$$J_3 = K_3 = Q_0Q_1Q_2 + Q_0Q_3$$

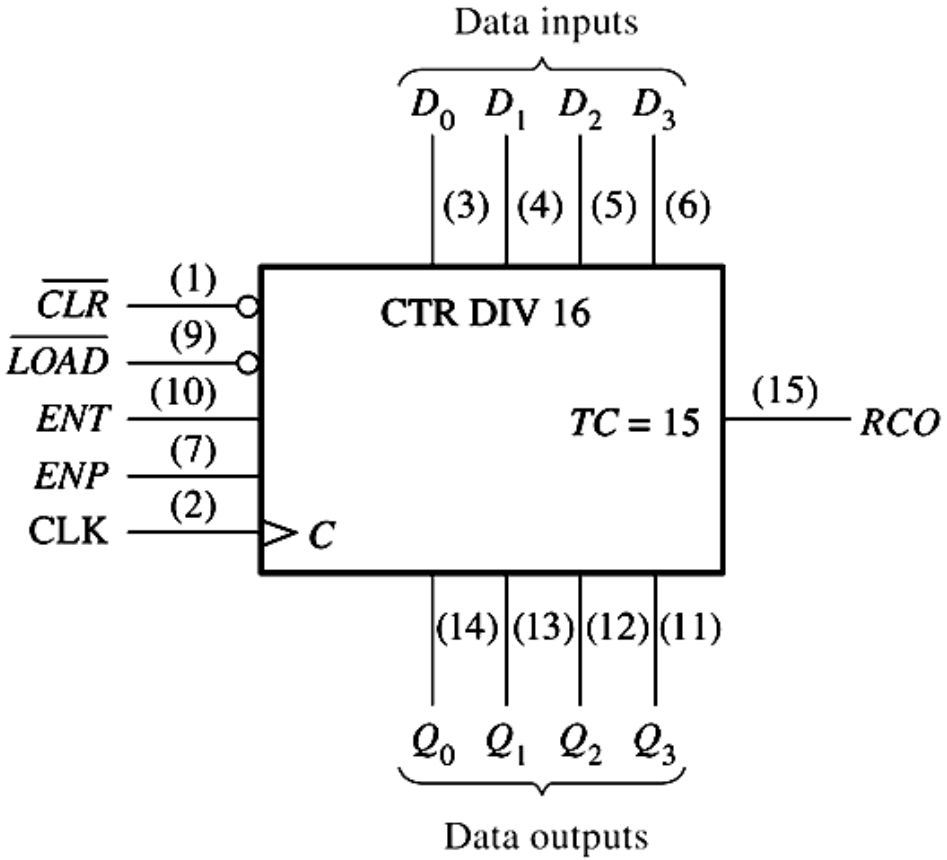
4-Bit Synchronous Decade Counters





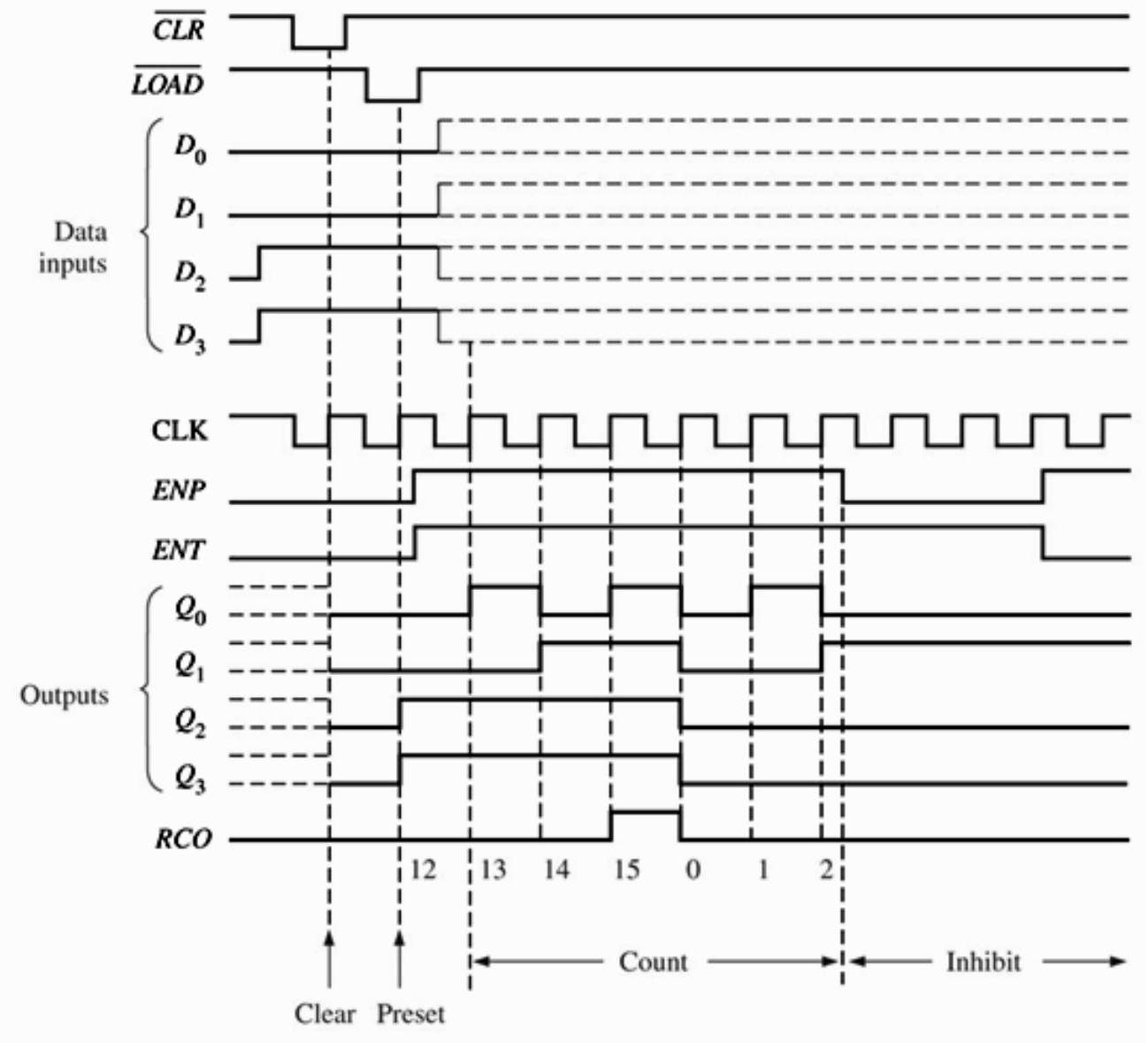
IC Synchronous Counters

74HC163 — a 4-bit synchronous binary counter



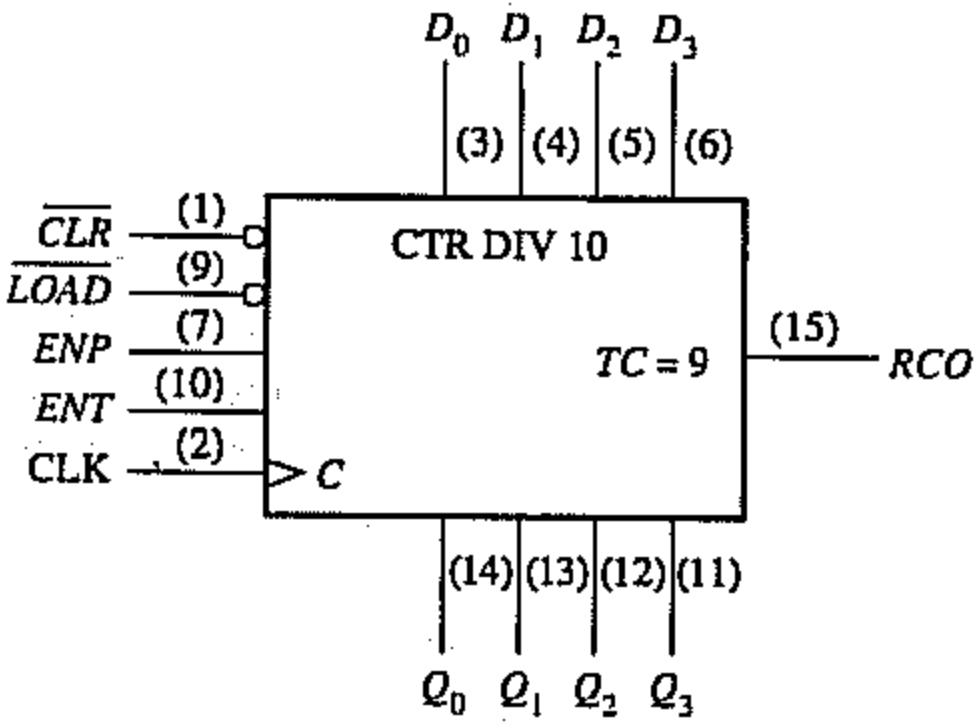
- $\overline{CLR}$: synchronous clear
- $\overline{LOAD}$: synchronous preset
- *ENT, ENP*: enable
- *RCO*: ripple clock output, which goes to 1 at count 15

IC Synchronous Counters



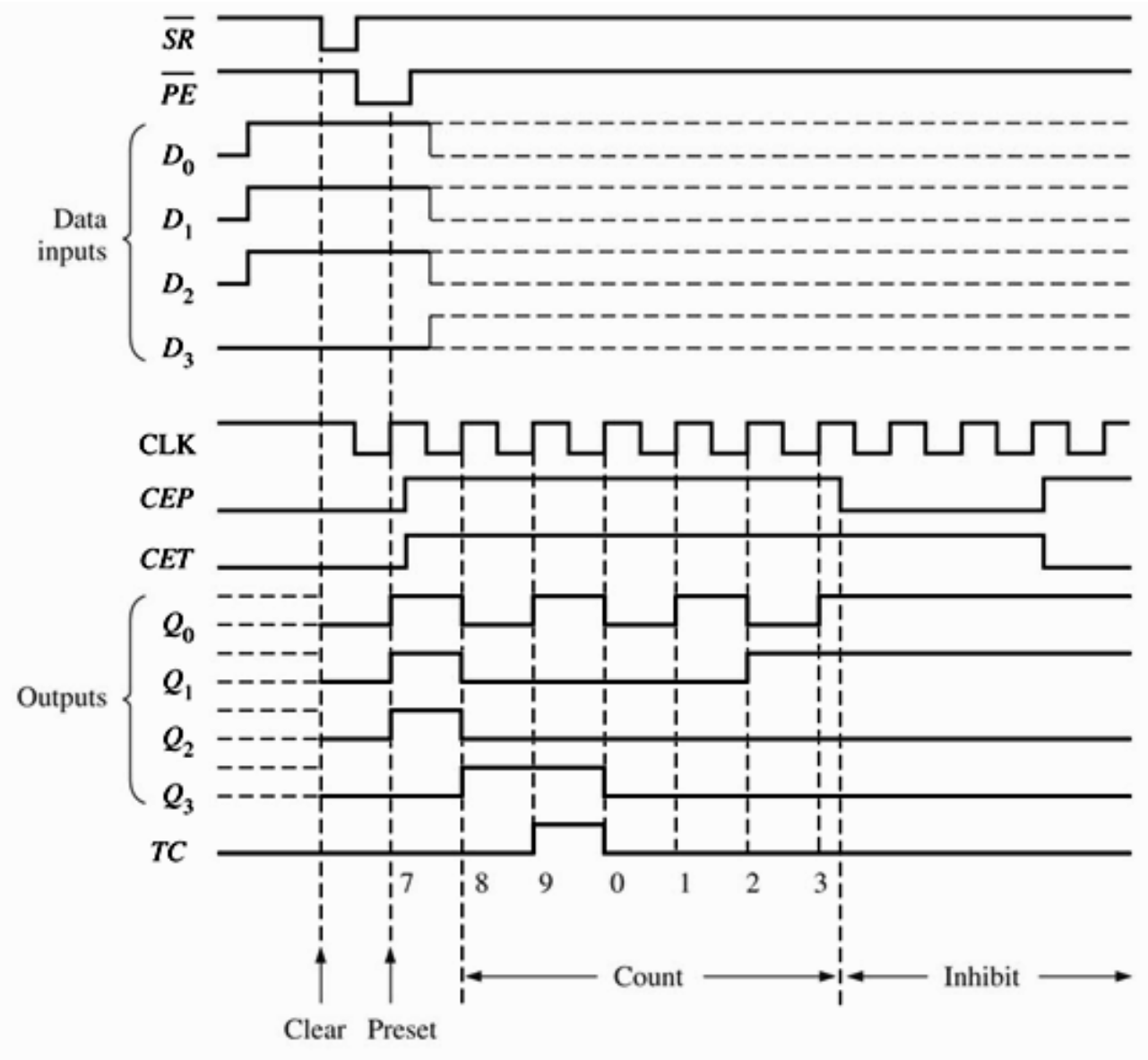
IC Synchronous Counters

74HC160 — a 4-bit synchronous decade counter



- $\overline{CLR}$: asynchronous clear
- $\overline{LOAD}$: synchronous preset
- *ENT, ENP*: enable
- *RCO*: ripple clock output, which goes to 1 at count 9

IC Synchronous Counters



Up/Down Synchronous Counters

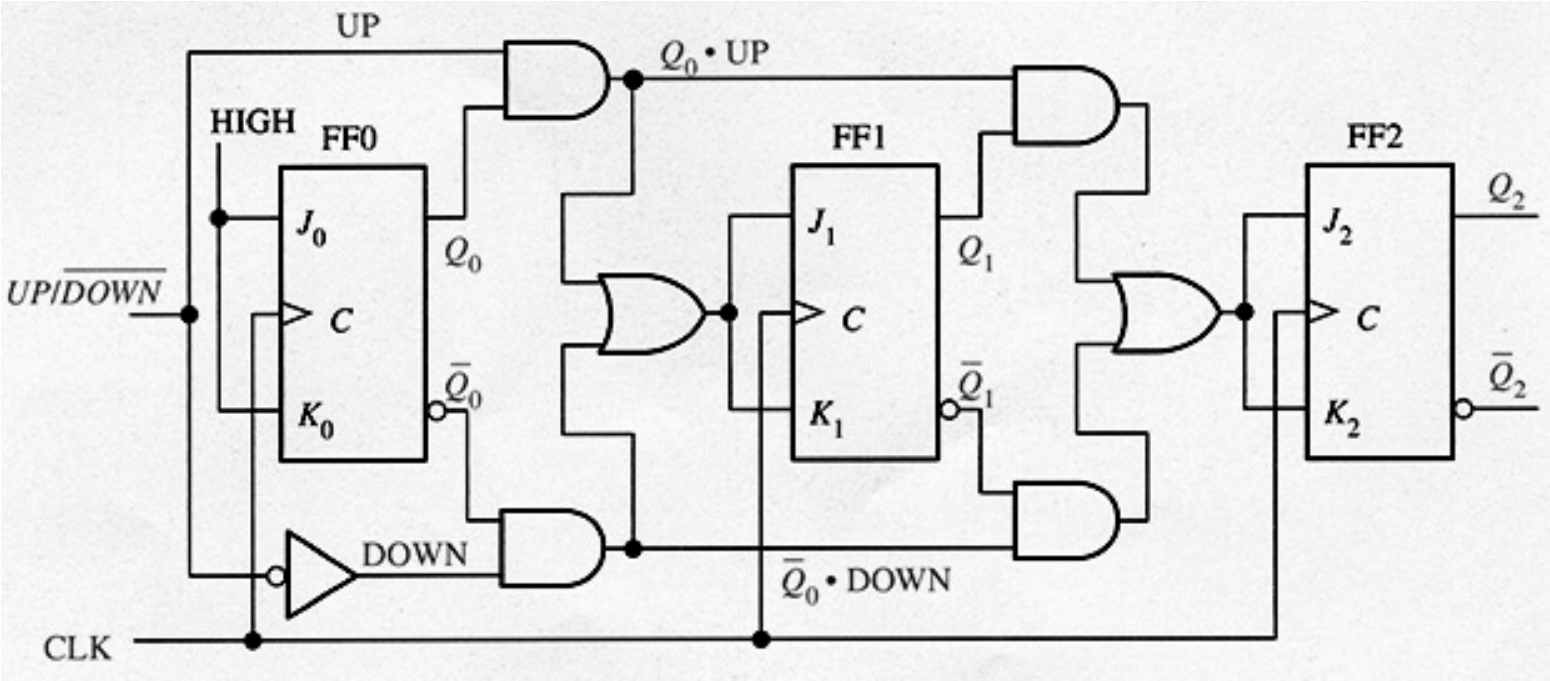
An **up/down counter** is one that is capable of progressing in either direction through a sequence.

CLOCK PULSE	UP	Q_2	Q_1	Q_0	DOWN
0		0	0	0	
1		0	0	1	
2		0	1	0	
3		0	1	1	
4		1	0	0	
5		1	0	1	
6		1	1	0	
7		1	1	1	

In count-down mode:

- Q_0 is always toggled.
- Q_1 is toggled at states 110, 100, 010, 000. So $J_1 = K_1 = /Q_0$.
- Q_2 is toggled at states 100, 000. So $J_2 = K_2 = /Q_0 /Q_1$

Up/Down Synchronous Counters

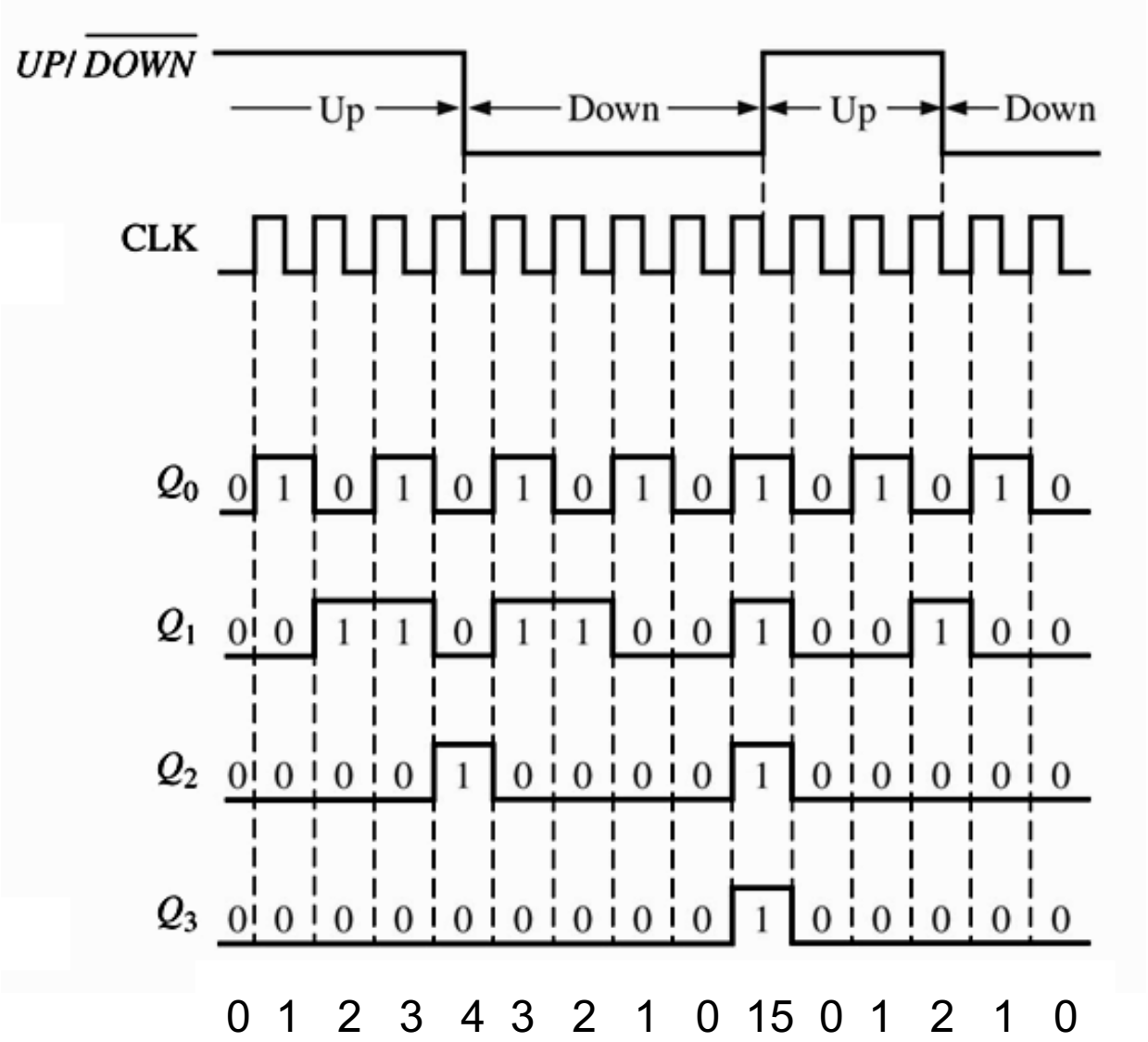


$$J_0 = K_0 = 1$$

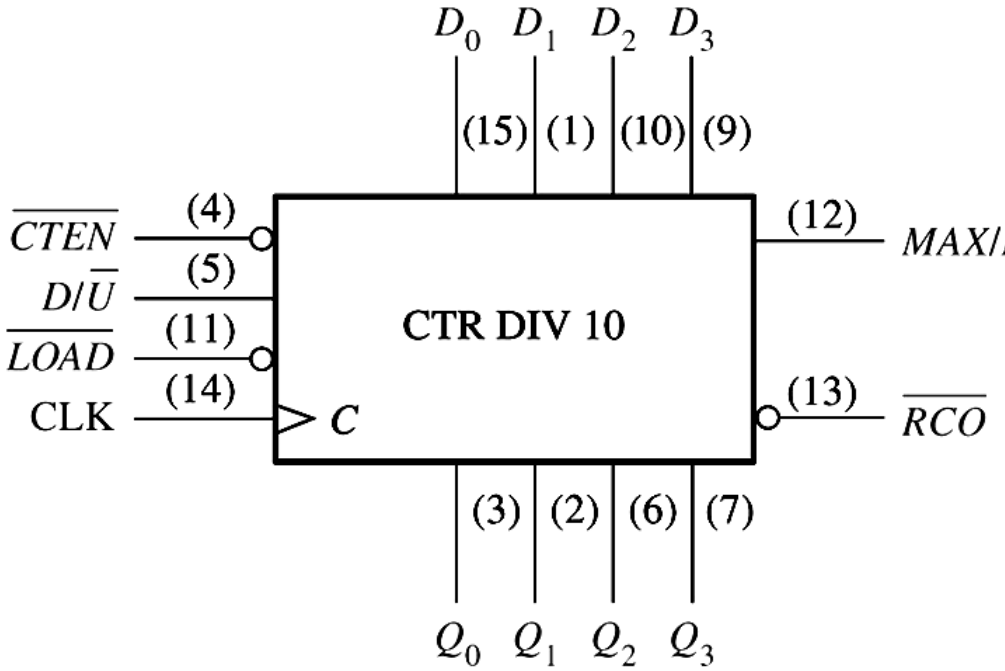
$$J_1 = K_1 = (Q_0 \cdot \text{UP}) + (\overline{Q}_0 \cdot \text{DOWN})$$

$$J_2 = K_2 = (Q_0 \cdot Q_1 \cdot \text{UP}) + (\overline{Q}_0 \cdot \overline{Q}_1 \cdot \text{DOWN})$$

Up/Down Synchronous Counters



An IC Up/Down Decade Counter



74LS190

- *CTEN*: enable
- *D/U*: down/up
- *LOAD*: synchronous preset
- *MAX/MIN*: HIGH when 1001 or 0000 is reached.
- *RCO*: ripple clock output, which is 0 at count 9