

# EEE104 – Digital Electronics (I)

## Lecture 13

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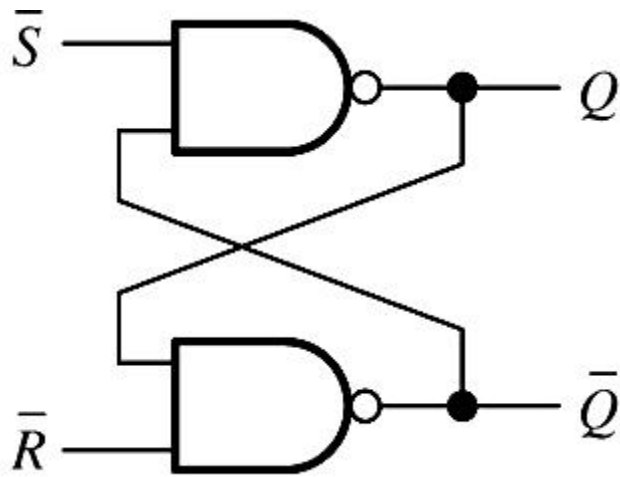
XJTLU

# In This Session

## Flip-Flops and Related Devices

- Latches
- Edge-Triggered Flip-Flops
- Flip-Flop Applications

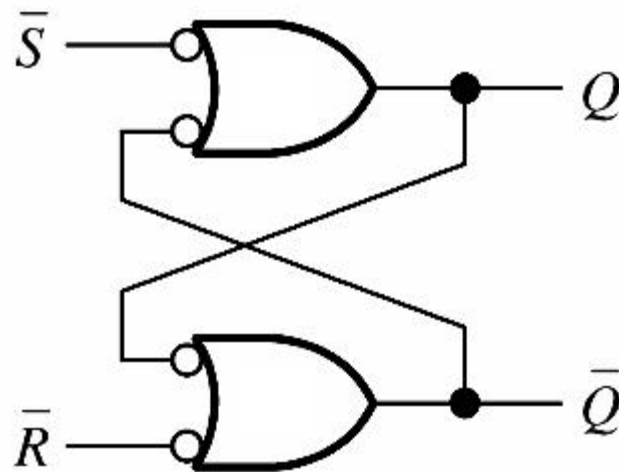
# Latches – The S-R Latch



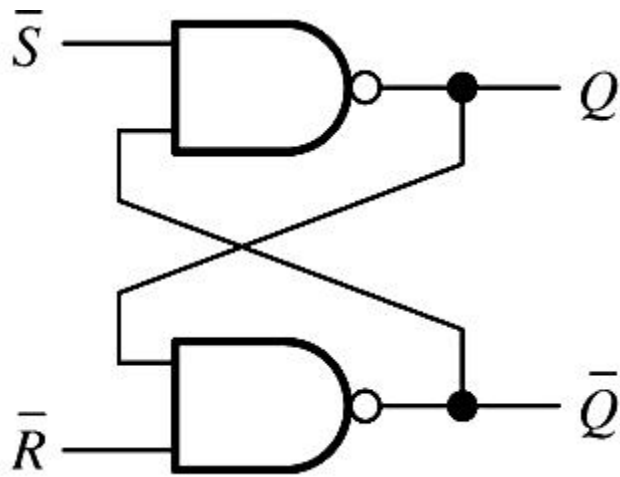
- A latch is a bistable digital circuit used for storing a bit.
- An S-R latch with active –LOW inputs is formed with two NAND gates.
- The output of one gate is fed back to the input of the other.

# Latches – The S-R Latch

- A NAND gate is equivalent to a negative-OR gate.
- Hence the S-R Latch equivalent implementation.
- It will be used extensively later.



# Latches – The S-R Latch

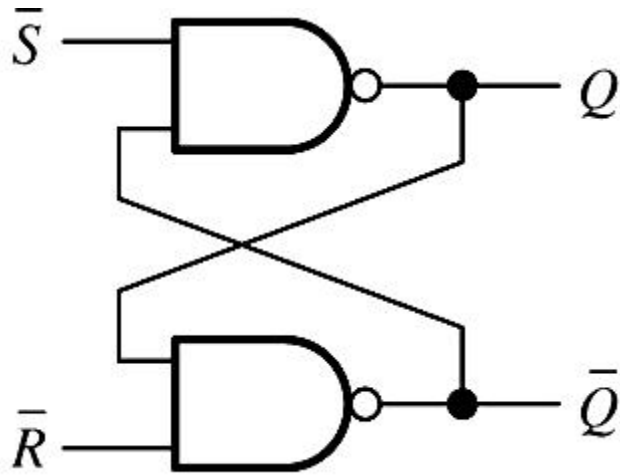


How does it work?

1. Suppose that  $/S$  and  $/R$  are both 1 originally.
2. When a negative pulse appears at  $/S$ , i.e.  $/S = 0$ , then  $Q = 1$ ,  $/Q = 0$ .
3. When the pulse finishes, i.e.  $/S = 1$ ,  $Q$  is still 1 and  $/Q$  is still 0.

So the low-level pulse at  $/S$  **sets** the output  $Q$  to 1.

# Latches – The S-R Latch

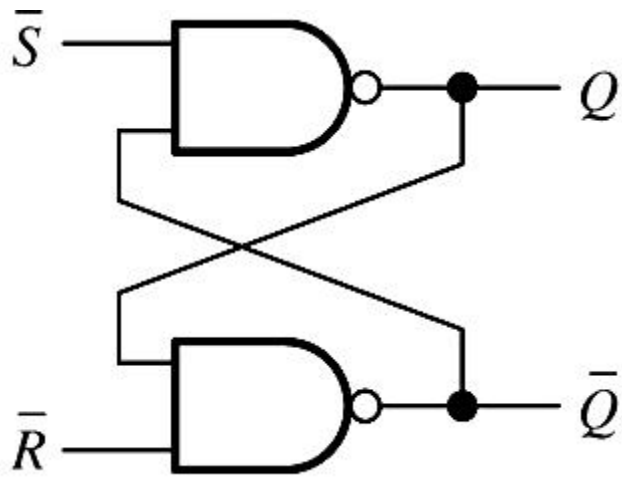


How does it work?

1. Suppose that  $\bar{S}$  and  $\bar{R}$  are both 1 originally.
2. When a negative pulse appears at  $\bar{R}$ , i.e.  $\bar{R} = 0$ , then  $\bar{Q} = 1$  and  $Q = 0$ .
3. When the pulse finishes, i.e.  $\bar{R} = 1$ ,  $Q$  is still 0 and  $\bar{Q}$  is still 1.

So the low-level pulse at  $\bar{R}$  **resets** the output  $Q$  to 0.

# Latches – The S-R Latch



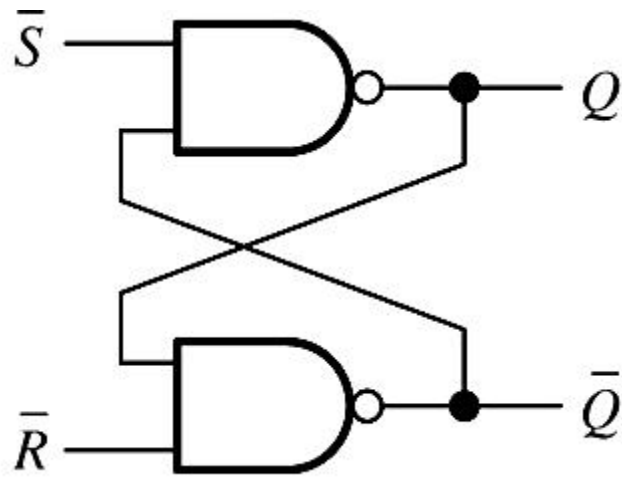
How does it work?

When both  $\bar{S}$  and  $\bar{R}$  are 1, the outputs will not be changed.

$$Q = \overline{1 \cdot \bar{Q}} = \bar{\bar{Q}} = Q$$

$$\bar{Q} = \overline{1 \cdot Q} = \bar{Q}$$

# Latches – The S-R Latch



How does it work?

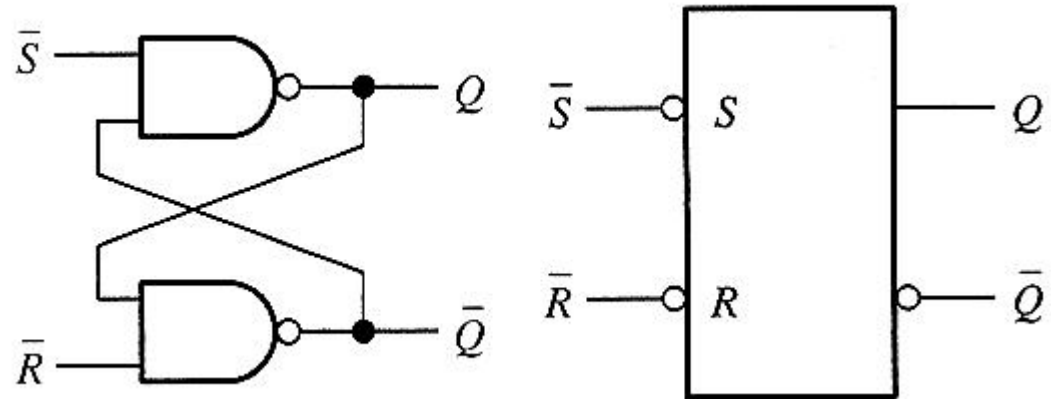
What will happen when both  $\bar{S}$  and  $\bar{R}$  are 0?

- Both  $Q$  and  $\bar{Q}$  will become 1.
- When  $\bar{S}$  and  $\bar{R}$  become HIGH simultaneously, the outputs are ideally LOW but uncertain due to the competition in gate speed.



# Latches – The S-R Latch

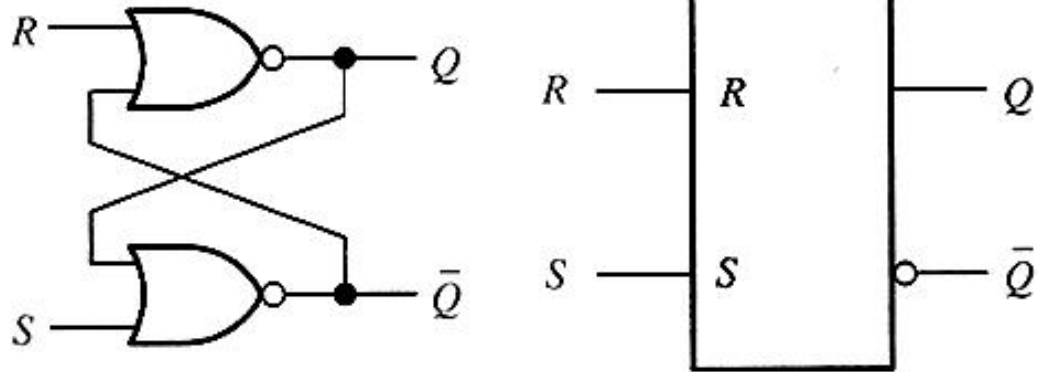
An S-R latch with active-LOW inputs is formed using NAND gates.



INPUTS		OUTPUTS		COMMENTS
$\bar{S}$	$\bar{R}$	$Q$	$\bar{Q}$	
1	1	NC	NC	No change. Latch remains in present state.
0	1	1	0	Latch SET.
1	0	0	1	Latch RESET.
0	0	1	1	Invalid condition

# Latches – The S-R Latch

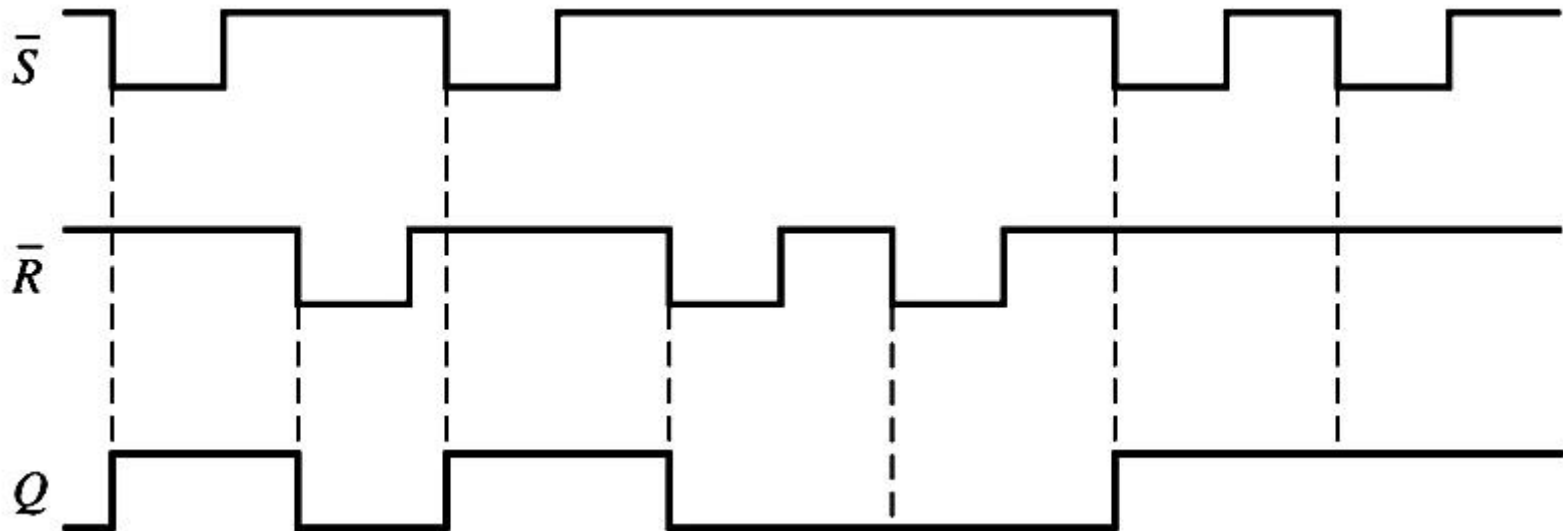
An S-R latch with active-HIGH inputs is formed using NOR gates.



INPUTS		OUTPUTS		COMMENTS
$S$	$R$	$Q$	$\bar{Q}$	
0	0	NC	NC	No change. Latch remains in present state.
0	1	0	1	Latch RESET.
1	0	1	0	Latch SET.
1	1	0	0	Invalid condition

# Latches – The S-R Latch

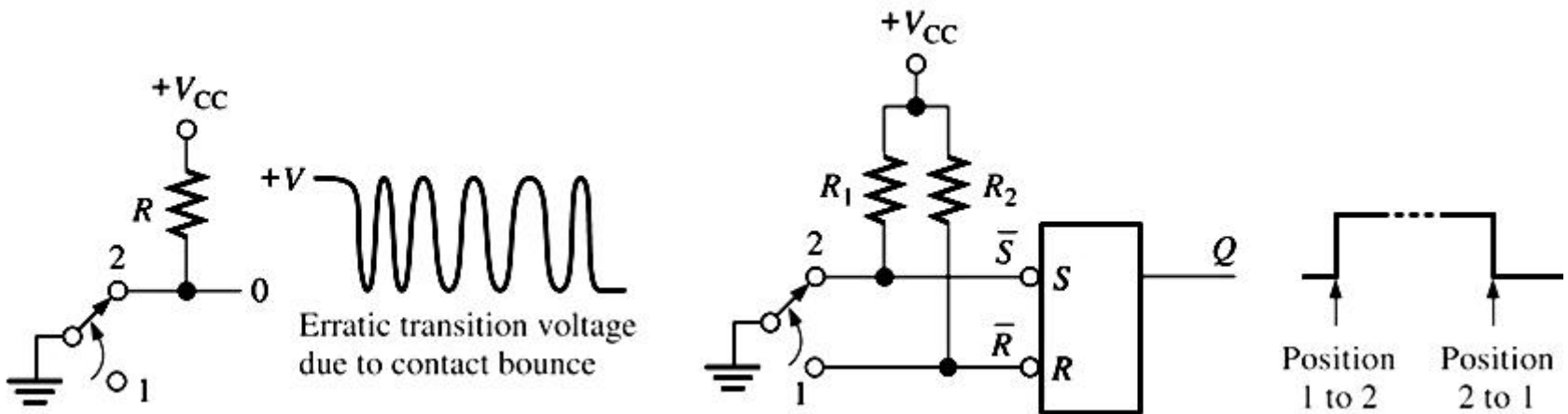
An Example: For a latch with active-LOW inputs



# Latches – The S-R Latch

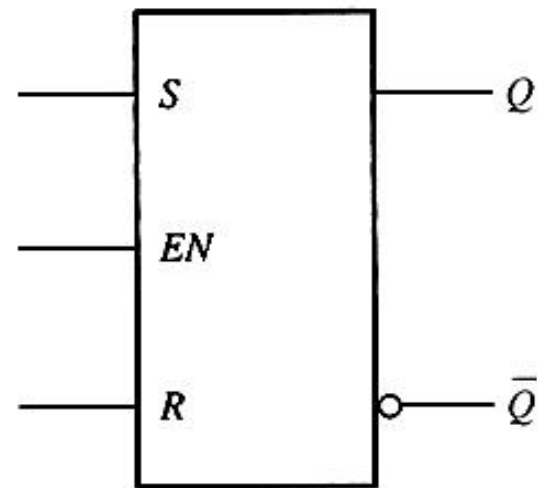
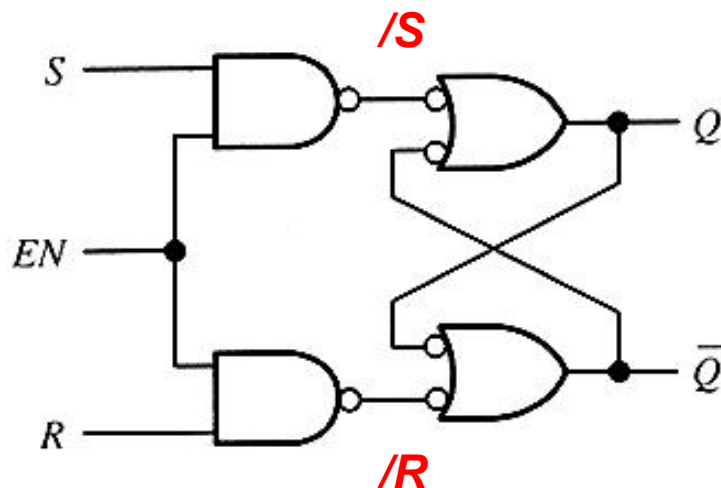
## Application Example

The latch as a contact-bounce eliminator



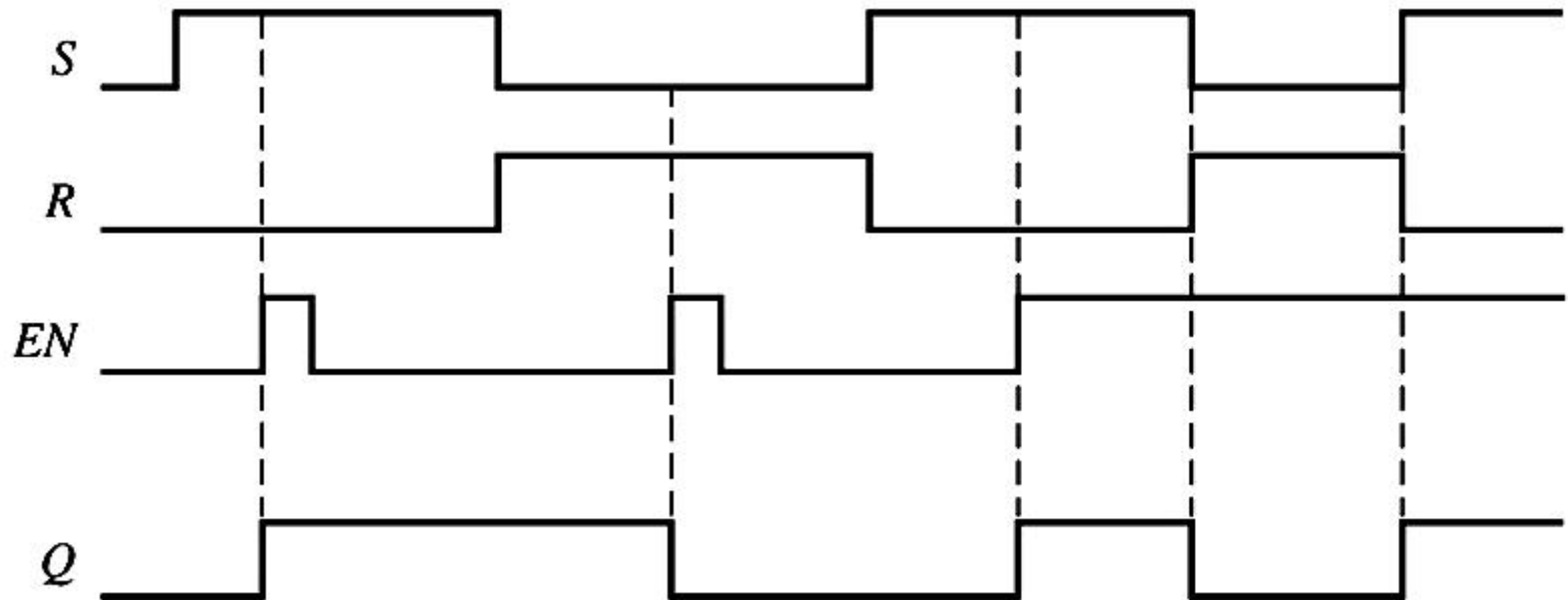
# Latches – The Gated S-R Latch

- A gated latch is a latch with an enable input  $EN$ .
- The latch will not change until  $EN$  is HIGH. Otherwise it is like an S-R latch with active-LOW inputs  $/S = 1$  and  $/R = 1$ .



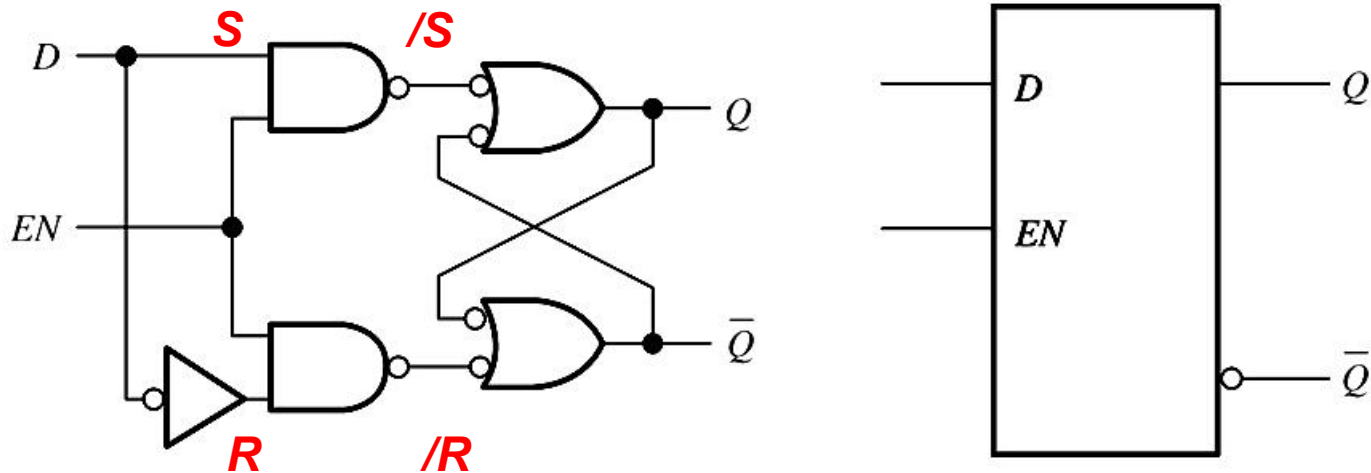
# Latches – The Gated S-R Latch

An Example: For a latch with active-HIGH inputs



# Latches – The Gated D Latch

- It has only one input in addition to EN.
- When  $D = 1$  and  $EN = 1$ ,  $Q = 1$ .
- When  $D = 0$  and  $EN = 1$ ,  $Q = 0$ .
- Output  $Q$  follows the input  $D$  when  $EN$  is HIGH.



# Latches – The Gated D Latch

An Example:

