

**Homework 1 on Electronic Devices in Silicon CMOS ICs**

in the module

**EEE201 CMOS Digital Integrated Circuits**

1. In the MOS transistors of a digital integrated circuits (ICs), the drain diffusion region has an ***n***-type doping of  $10^{18} \text{ cm}^{-3}$  on a silicon substrate with the ***p***-type doping of  $10^{16} \text{ cm}^{-3}$ .

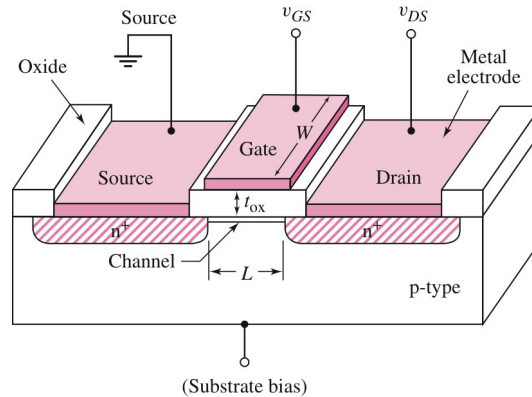


Image from: Donald A. Neamen, Microelectronics: Circuit Analysis & Design, 4th edition, © 2010 McGraw-Hill, USA.

- What is the approximate intrinsic carrier concentration in silicon at room temperature ( $T = 300 \text{ K}$ )? Hence or otherwise, calculate the **built-in potential**  $V_{bi}$  of the ***p-n* junction** between the ***p***-type substrate and the ***n***-type drain region at room temperature.
- Using the result in (a) or otherwise, calculate the **depletion width** of the ***p-n* junction** when both the drain and the substrate are not connected to any voltage (i.e. zero-biased).
- Using *Matlab* or *Excel*, plot a graph of the **depletion width** when the substrate is connected to ground and the drain voltage  $V_{DS}$  increases from  $0 \text{ V}$  to  $+3.0 \text{ V}$ .
- If the drain region of the MOSFET has a total area of  $40 \mu\text{m} \times 0.6 \mu\text{m}$ , using the result in (b) or otherwise, calculate the **depletion capacitance** of the drain terminal in the open-circuit condition. Assume the sidewall contribution to the depletion capacitance negligible.
- If the depth of the drain region is  $0.15 \mu\text{m}$ , calculate the sidewall contribution to the **depletion capacitance** in the open-circuit condition (i.e. zero-biased) (Hint: What is the perimeter of the drain region?).
- Using *Matlab* or *Excel*, plot a graph of the total **depletion capacitance** (with the sidewall contribution included) when the substrate is connected to ground and the drain voltage  $V_{DS}$  increases from  $0 \text{ V}$  to  $+3.0 \text{ V}$ .

Assume an abrupt junction (i.e. abrupt metallurgical boundary in the ***p-n* junction**) in all the calculations. Please find out the physical constants (e.g. Boltzmann's constant  $k_B$ ) from textbooks or reliable websites on the internet.

2. The MOS transistors of the same digital integrated circuits (ICs) described in Question 1 has a gate oxide thickness  $t_{ox}$  of  $30 \text{ \AA}$  (i.e.  $3.0 \text{ nm}$ ) and an effective channel length  $L = 0.15 \mu\text{m}$ .

- Calculate the **normalised gate oxide capacitance**  $C_{ox}$  of the MOS transistors. Assume the gate oxide is made of high quality silicon dioxide ( $\text{SiO}_2$ ).

- (b). Determine the gate-to-source capacitance  $C_{GS}$  of the MOS transistor operating in the saturation region. Note that the MOSFET has  $W = 40\text{ }\mu\text{m}$  and  $L = 0.15\text{ }\mu\text{m}$ .
- (c). Determine the gate-to-drain capacitance  $C_{GD}$  of the MOS transistor if it operates in the linear mode. How does the value of  $C_{GD}$  compare with the **depletion capacitance** of the drain-to-substrate junction?
- (d). It is given the electron mobility for the MOS transistors is  $370\text{ cm}^2/\text{Vs}$  and the **threshold voltage**  $V_T$  of the **n**-channel MOS transistors is  $0.45\text{ V}$ . Assuming the long-channel approximation, using *Matlab* or *Excel*, plot a graph of the output characteristics (i.e.  $I_{DS}$  vs.  $V_{DS}$ ) of a MOS transistor with a channel width  $W = 40\text{ }\mu\text{m}$  and  $L = 0.15\text{ }\mu\text{m}$  for  $V_{GS} = 0.7\text{ V}$ ,  $1.0\text{ V}$ ,  $1.5\text{ V}$  and  $2.0\text{ V}$  while  $V_{DS}$  varies from  $0\text{ V}$  to  $2.5\text{ V}$ .
- (e). With the same parameters and the long-channel approximation, using *Matlab* or *Excel*, plot a graph of the **transfer characteristics** (i.e.  $I_{DS}$  vs.  $V_{GS}$ ) of a MOS transistor of the same size  $W/L = 40\text{ }\mu\text{m}/0.15\text{ }\mu\text{m}$  for  $V_{DS} = 0.2\text{ V}$ ,  $1.0\text{ V}$ ,  $2.0\text{ V}$  while  $V_{GS}$  varies from  $0\text{ V}$  to  $2.0\text{ V}$ . Assume the current is zero when  $V_{GS}$  is below the **threshold voltage**  $V_T$ .
- (f). If hafnium oxide ( $\text{HfO}_2$ ) with a dielectric constant of 25 is used to replace the silicon dioxide ( $\text{SiO}_2$ ) as the gate dielectric, what would be the gate oxide thickness  $t_{\text{HfO}}$  to keep same the normalised **gate oxide capacitance**  $C_{ox}$  as that obtained in Q2(a)?

Note: In all the calculations, please show your steps clearly. When you find the values of some material parameters or physical constants (not provided in the questions), please cite the source(s) explicitly as a footnote or include a section of references at the end.