Lecture 13

of

EEE201

CMOS Digital Integrated Circuits

Department of Electrical & Electronic Engineering

Xi'an Jiaotong-Liverpool University (XJTLU)

Monday, 9th December 2024

- **Ratioed Logic**
  - pull-up network replaced by a load
  - pseudo-NMOS
- **Dynamic Logic & Domino Logic**
  - precharge & evaluation phases

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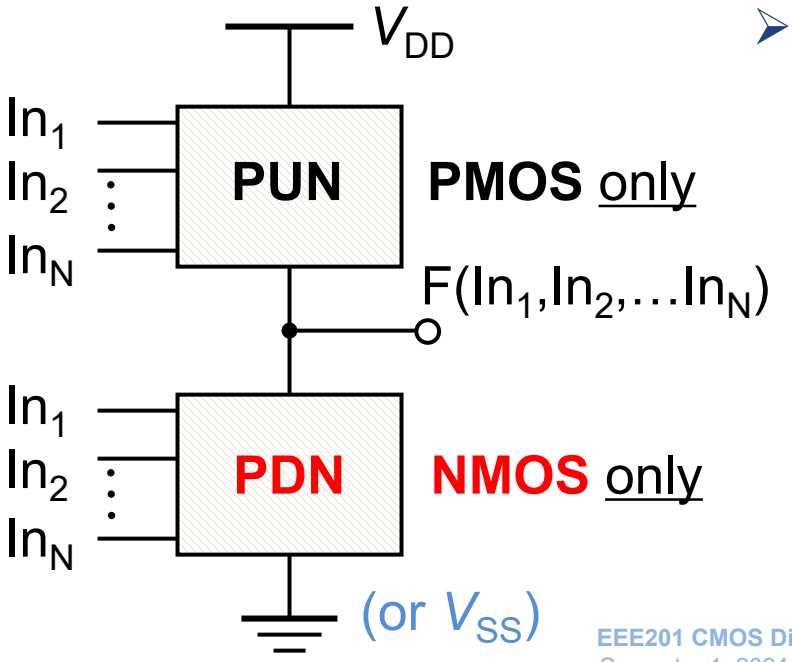
Combinational Logic Circuits

(pull-up & pull-down networks)

- In CMOS technology, a **combinational logic circuit** consists of basically a **pull-up network** (**PUN**) and a **pull-down network** (**PDN**).
  - The **PUN** consists of only **PMOS transistors** while **PDN** only **NMOS transistors**.



- In the *steady* state, either the PUN provides a low-resistance path to connect the output (F) to V_{DD} or the PDN make a low-resistance connection between the output and ground (or V_{SS}), hence ***pulling up*** or ***down*** the output voltage.

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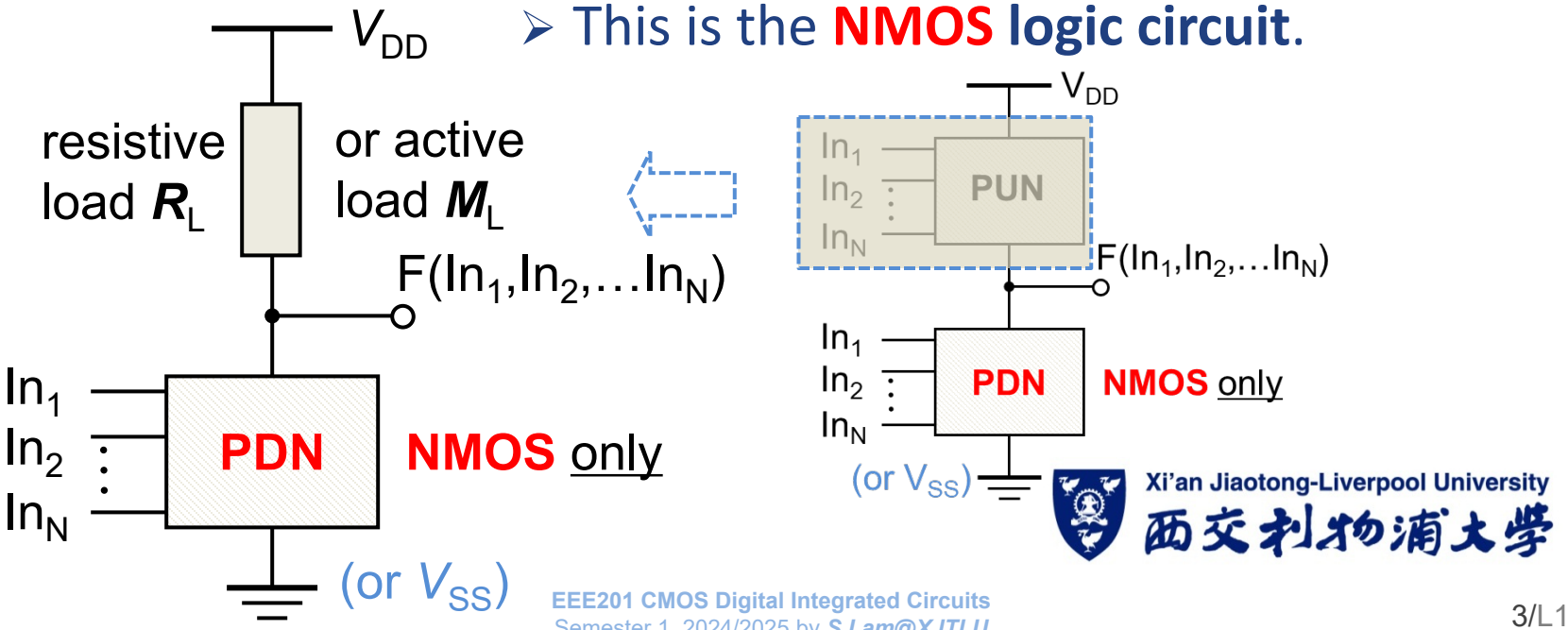
NMOS Combinational Logic Circuits

(pull-up network replaced with a load device)

- Before CMOS technology became mature, only one type of MOS transistors was available for implementation of digital integrated circuits. The **pull-down network** (**PDN**) consists of only **NMOS transistors** but the **PUN** is *replaced* by either a *resistive* **load** or an NMOS transistor as an active load.
  - This is the **NMOS logic circuit**.



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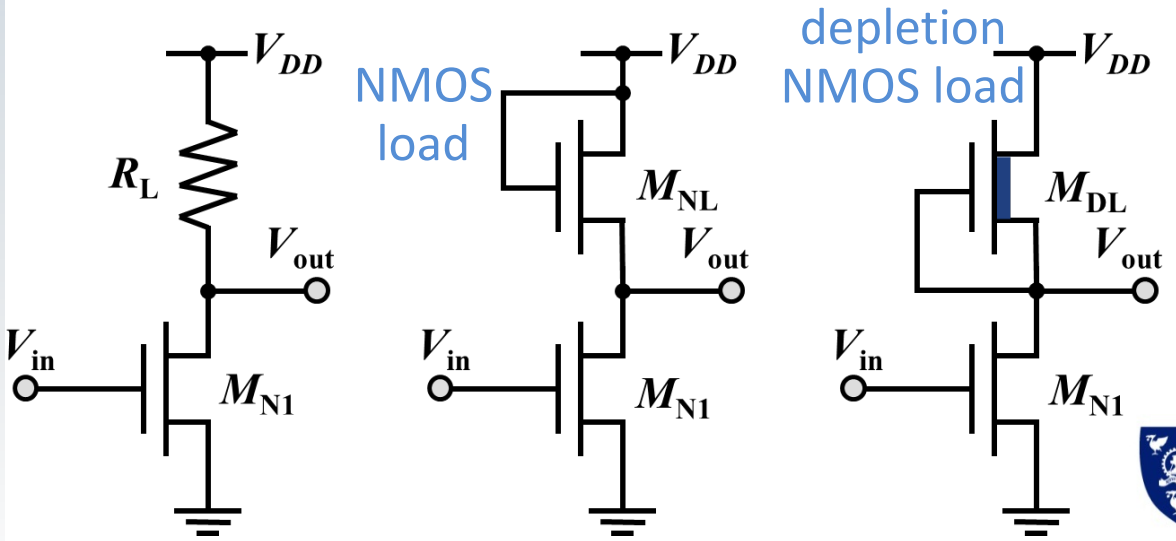
NMOS Combinational Logic Circuits

(pull-down network fights with load device)

- In the **NMOS logic circuits**, when the **pull-down network** turns on, it "fights" with the resistive or active load to pull down the output voltage.
  - The ***equivalent*** **load resistance** should be high enough so that the NMOS **pull-down network** can pull down the output to an acceptably low logic "0" voltage $\boldsymbol{V}_{OL}$.



  - This can be understood with the VTC of the simple NMOS inverter.

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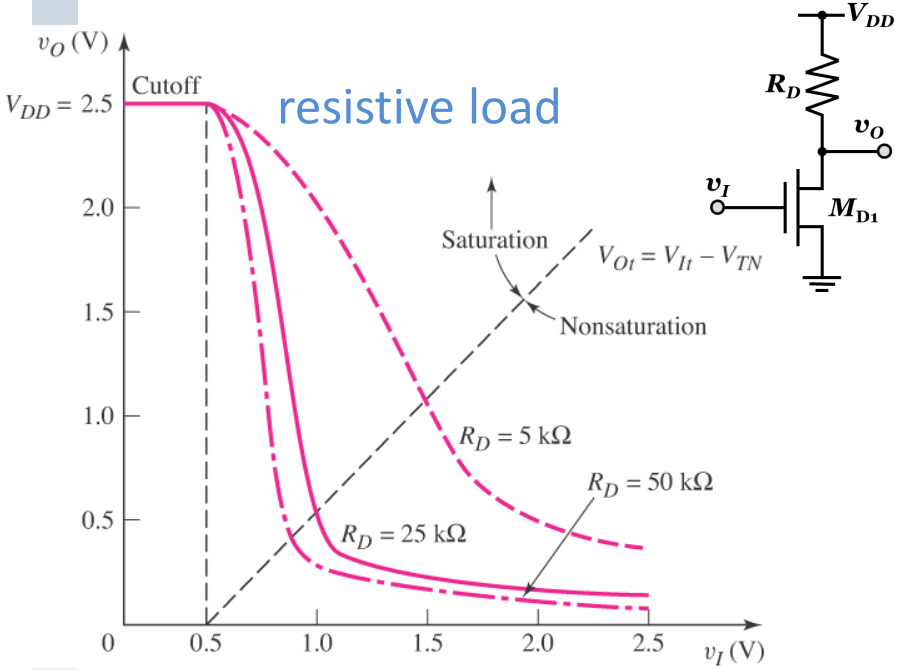
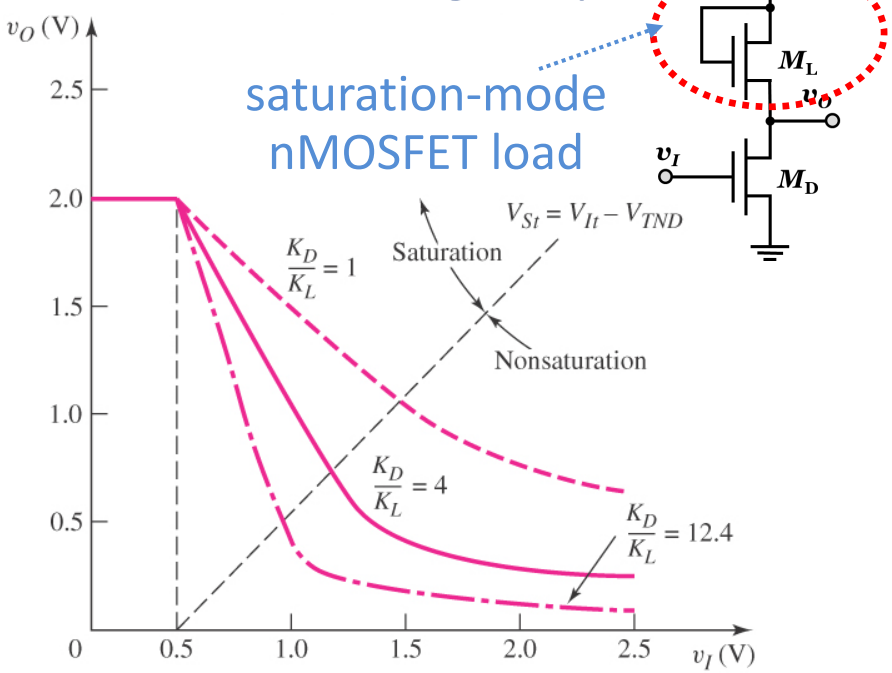
VTC of NMOS Inverters

(pull-down NMOS transistors fights with load device)

- A lower ***equivalent*** **load resistance** gives higher V_{OL} and hence degrading the **noise margin** NM_L (also *static* **power consumption**) though it produces faster rising output.





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VTC of NMOS Inverters

(depletion load with negative V_{TN})

- In the case of using a depletion-mode nMOSFET as the load device, VTC are better for certain gain factor (K_D, K_L) ratios.

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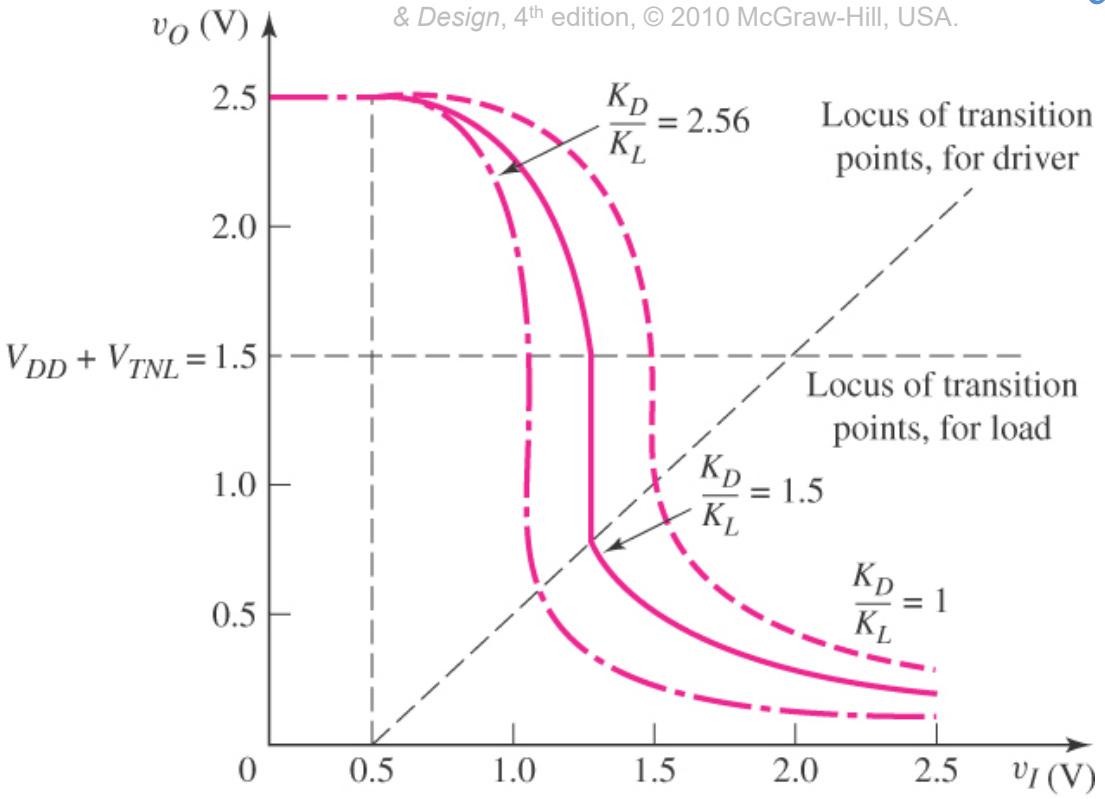
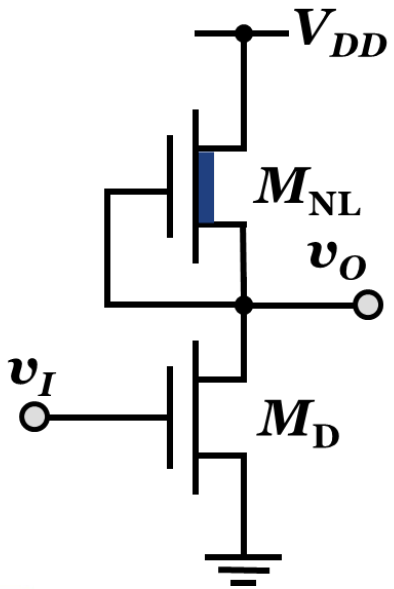


depletion load with negative threshold voltage V_{TNL}



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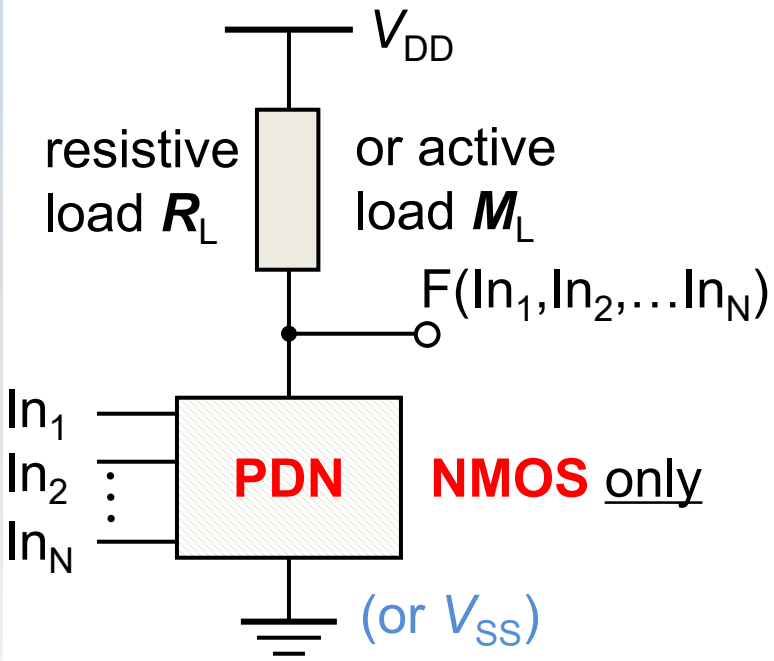
Ratioed Logic Circuits

(ratioed load resistance or transistor size)

- With the ***static*** **load**, the proper operation of the **NMOS logic circuits** depends on the appropriate **load resistance R_L** or **transistor size** (i.e. ***W/L***).



- Typically, the ***static*** **load** is a MOSFET. Its size and that of those NMOS transistors in the pull-down network (PDN) have a **ratio constraint**.
- Such logic circuits are called ***ratioed*** **logic**, with the logic function performed solely by the PDN.

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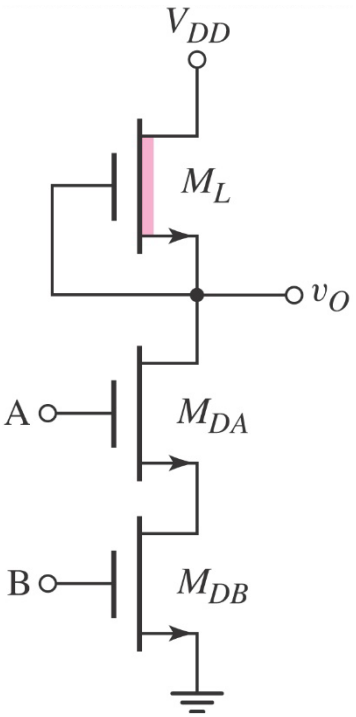
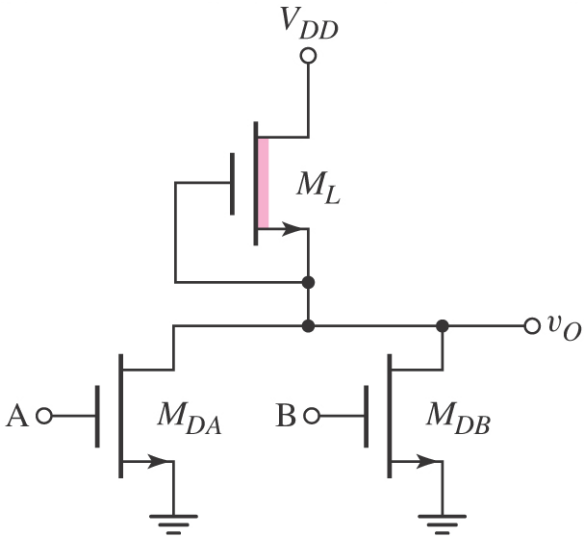
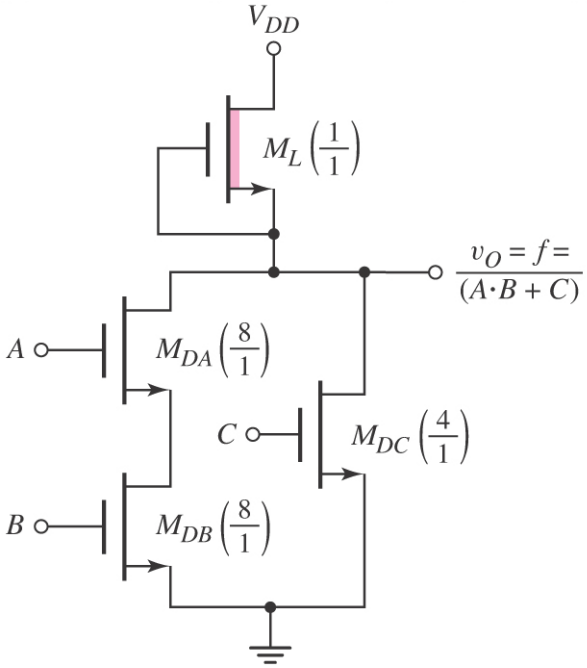
Ratioed Logic Circuits

(examples other than inverter)

- Examples of ratioed logic have more than one NMOS transistors in the pull-down network (instead of one nMOSFET in the inverter).







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Ratioed Logic Circuits

(disadvantages compared with CMOS)

- Ratioed logic is generally not as good as CMOS logic circuits:
  - It is less ***robust*** (in terms of fabrication variation from the components' nominal values and circuit operation), with a simple load device replacing the PUN which provides a conditional path between V_{DD} and the output when the PDN is turned off.
  - **Static power dissipation** in **ratioed logic** may not be acceptable when the number of logic gates increases; (think about 10 mA static current in each logic gate and there are 10k logic gates).
  - $\boldsymbol{V}_{OL} > 0$ (hence $\boldsymbol{NM}_L = \boldsymbol{V}_{IL} - \boldsymbol{V}_{OL}$ decreases) in **ratioed logic** circuit while CMOS has $\boldsymbol{V}_{OL} = 0$.

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Ratioed Logic Circuits

(less transistors & input capacitance)

- Despite the disadvantages compared with CMOS logic, **ratioed logic** is used in some special applications.
- **Ratioed logic** can be used to achieve certain purposes:
  - It reduces the number of transistors required to implement a given logic function.
    - If there are ***N*** inputs in a logic circuit, ratioed logic requires only ***N***+1 MOSFETs but CMOS requires 2***N***.
  - It reduces the input capacitances of the logic gates as pMOSFETs typically have much larger transistor size than nMOSFETs in CMOS logic and hence contributing much to the input capacitance. As a result, ratioed logic circuits can have a faster switching speed.

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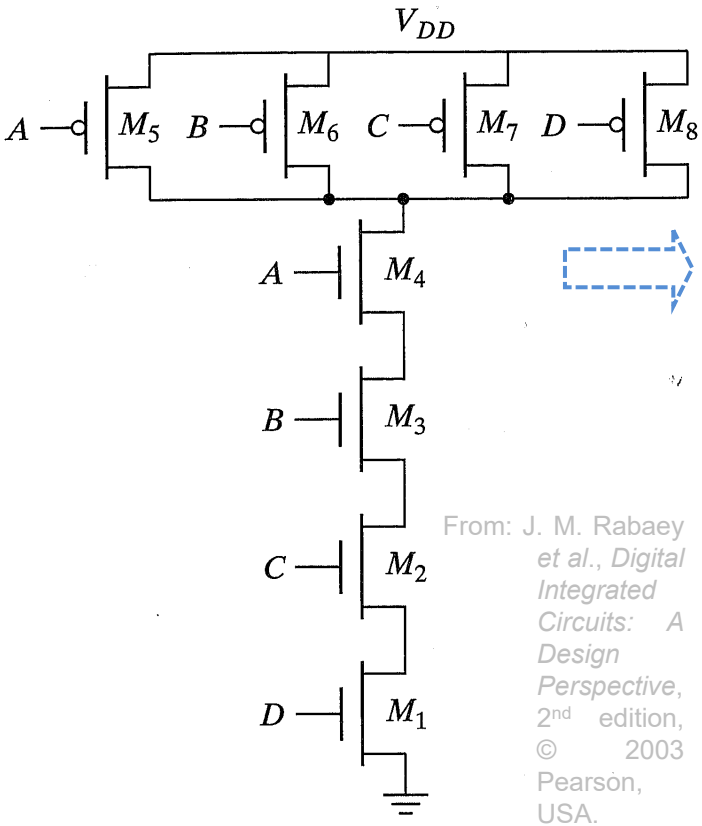
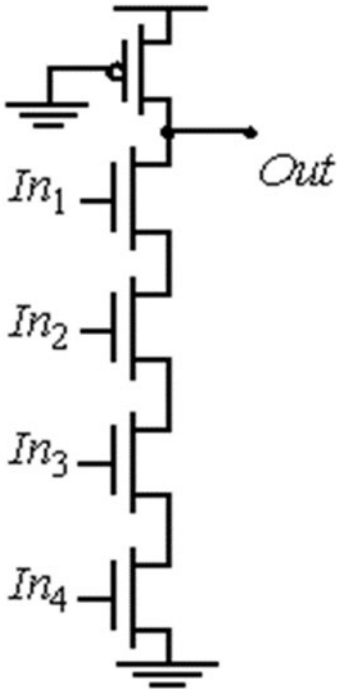
Ratioed Logic Circuits

(4-input NAND gate example)

- The reduced number of MOSFETs can be seen in an example of a four-input NAND gate.





From: J. M. Rabaey *et al.*, *Digital Integrated Circuits: A Design Perspective*, 2nd edition, © 2003 Pearson, USA.

- 4 inputs require only 5 MOSFETs in ratioed logic but 8 in CMOS.
- Imagine the layout of the 4-input NAND gate and the chip area saved in replacing the 4-transistor PUN with one pMOSFET.

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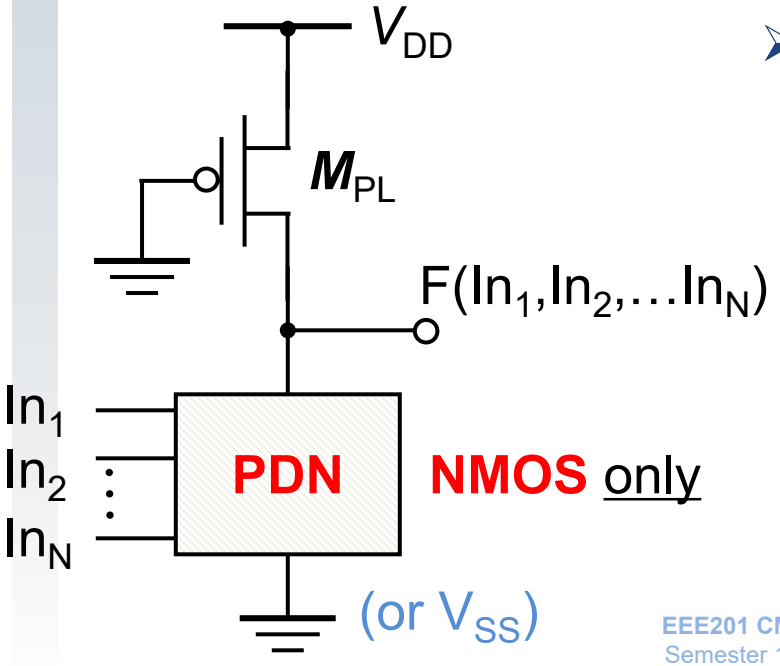
Ratioed Logic: pseudo-NMOS

(implemented in CMOS technology)

- **Ratioed logic** can be implemented in CMOS technology with a pMOSFET as the load device replacing the PUN.
  - The gate of pMOSFET as the load device is grounded (or connected to the negative power supply V_{SS}).
- Such **ratioed logic** is referred to as **pseudo-NMOS** logic.



- As expected in **ratioed logic**, the size of the pMOSFET relative to that of the nMOSFETs in the PDN can be used to *trade off* parameters such as **noise margin**, **propagation delay**, and **power dissipation**.

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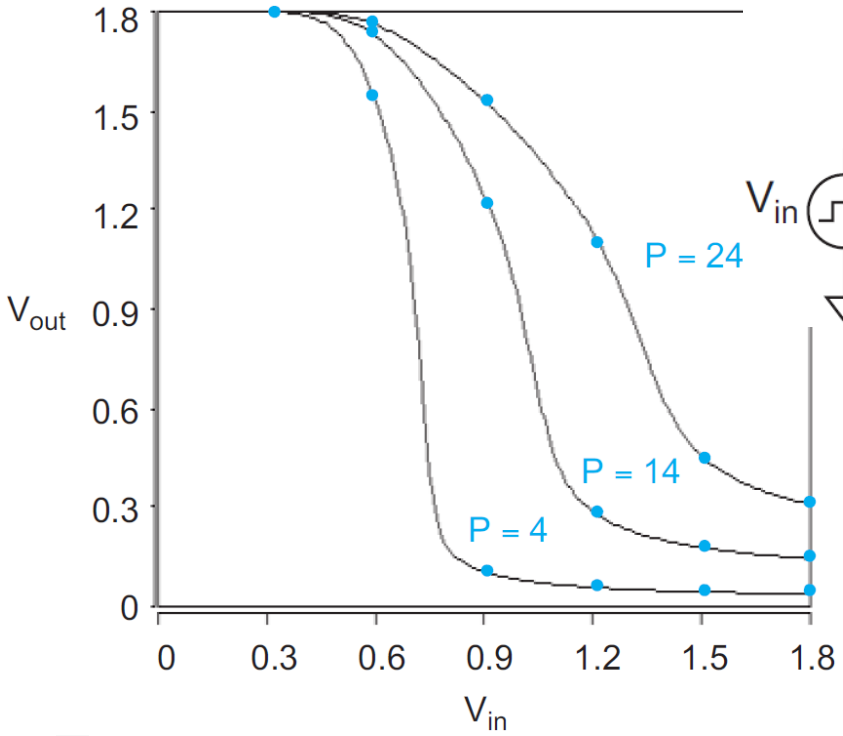
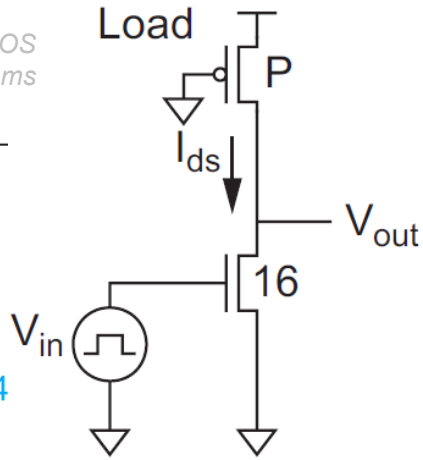
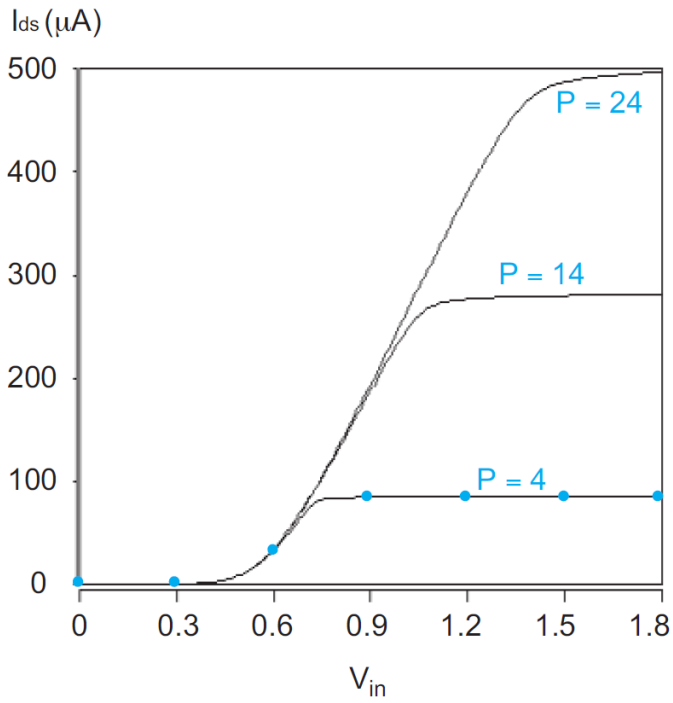
Ratioed Logic: pseudo-NMOS

(pseudo NMOS inverter)

- The performance trade-off in the **pseudo-NMOS** logic can be seen in the simple case of a pseudo-NMOS inverter.







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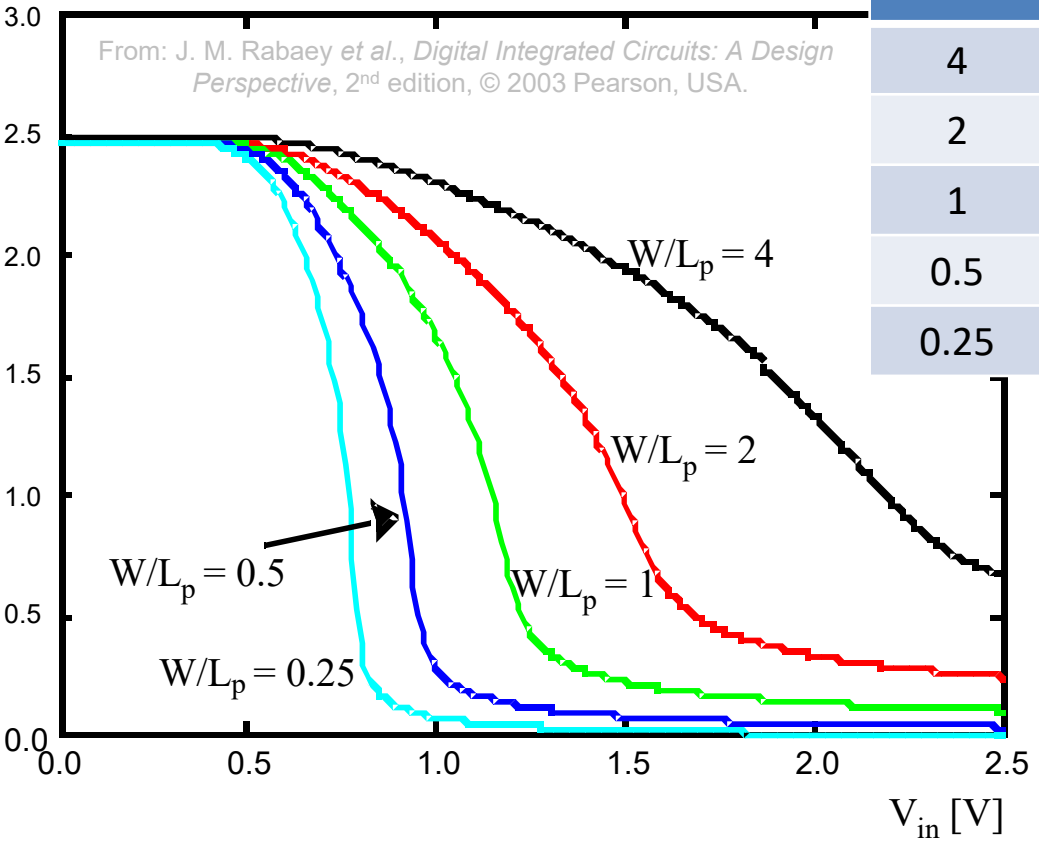
Ratioed Logic: pseudo-NMOS

(pseudo NMOS inverter)

- In a pseudo-NMOS inverter, the size of nMOSFET is 0.5μm/0.25μm.

$(W/L)_p$	V_{OL} (V)	Static Power Dissipation (μW)	t_{pLH} (ps)
4	0.693	564	14
2	0.273	298	56
1	0.133	160	123
0.5	0.064	80	268
0.25	0.031	41	569



- **trade-off** between power dissipation & propagation delay (hence speed)

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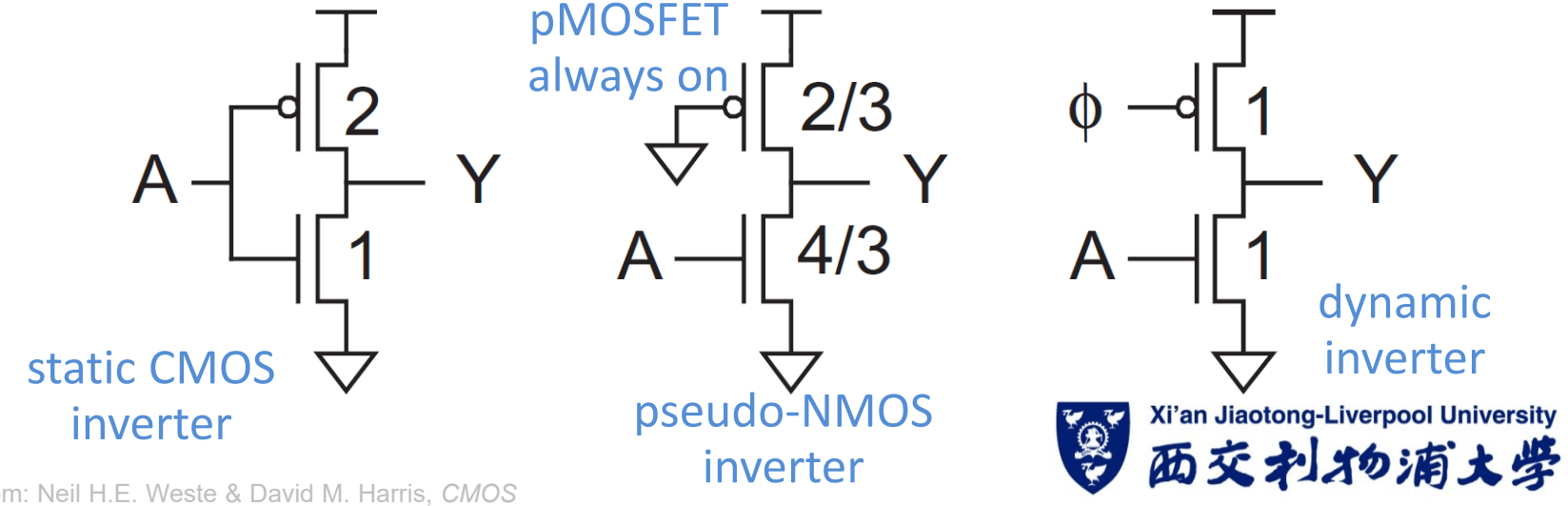
Pseudo-NMOS to Dynamic Logic

(overcoming static power dissipation)

- The drawbacks (especially the *static* power dissipation) of **pseudo-NMOS** can be overcome by using a ***clocked*** **pull-up transistor** rather than a pMOSFET that is always on.
  - Logic circuits with a *clocked* pull-up device are referred to as **dynamic logic**.
  - The idea can be illustrated using the inverter case.



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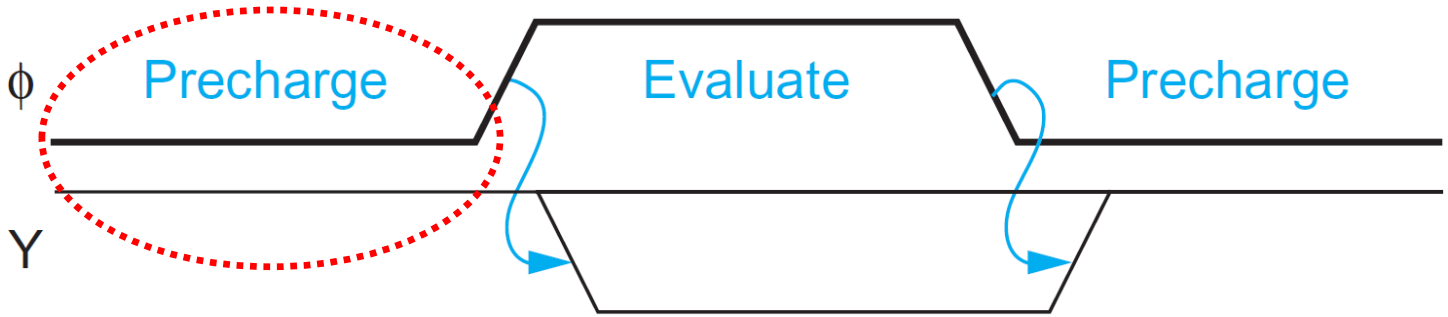
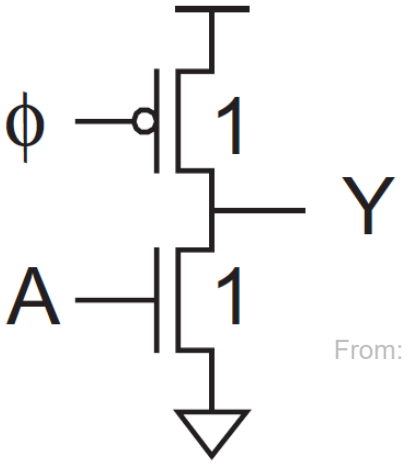
From: Neil H.E. Weste & David M. Harris, *CMOS VLSI Design: A Circuits & Systems Perspective*, 4e © 2011 Pearson , USA.

Dynamic Logic – precharge mode

(precharge & evaluation modes)

- The operation of the ***dynamic*** **inverter** is divided into two modes (or phases): **precharge** and **evaluation**, in sequence.
  - The operation mode is determined by the clock input ϕ.





- During the **precharge** mode (i.e. when the clock ϕ is "0"), the clocked pMOSFET turns on and the output Y is ***precharged*** to V_{DD}.

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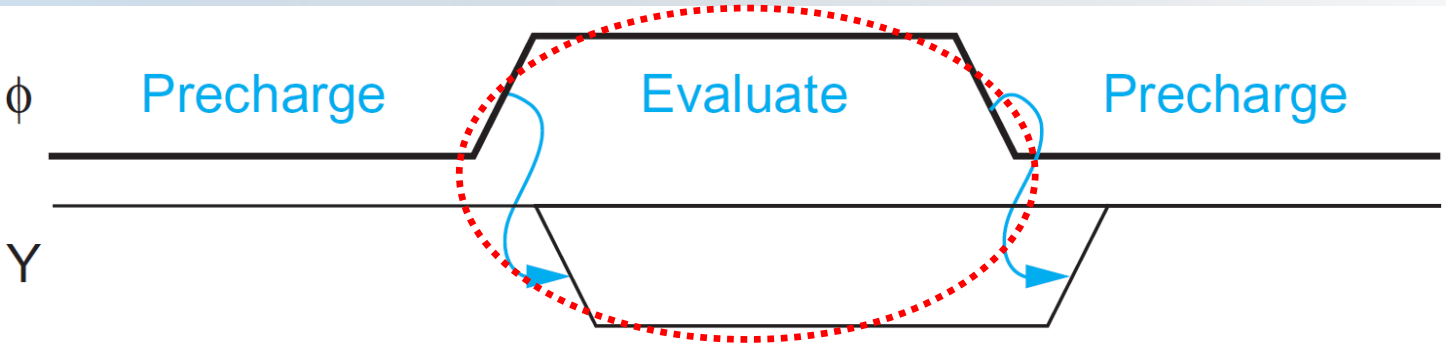
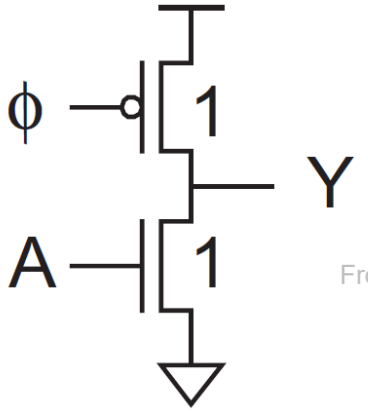
Dynamic Logic – evaluation mode

(no static power dissipation in evaluation mode)



- During the **evaluation** mode (i.e. when the clock ϕ is "1"), the clocked pMOSFET turns off and the output Y may remain at $\boldsymbol{V}_{DD}$ or may be discharged to "0" through the pull-down network (an nMOSFET in the inverter case).
  - As the clocked pMOSFET turns off during the **evaluation** mode, there is no *static* power dissipation in this mode whatever the input A is.



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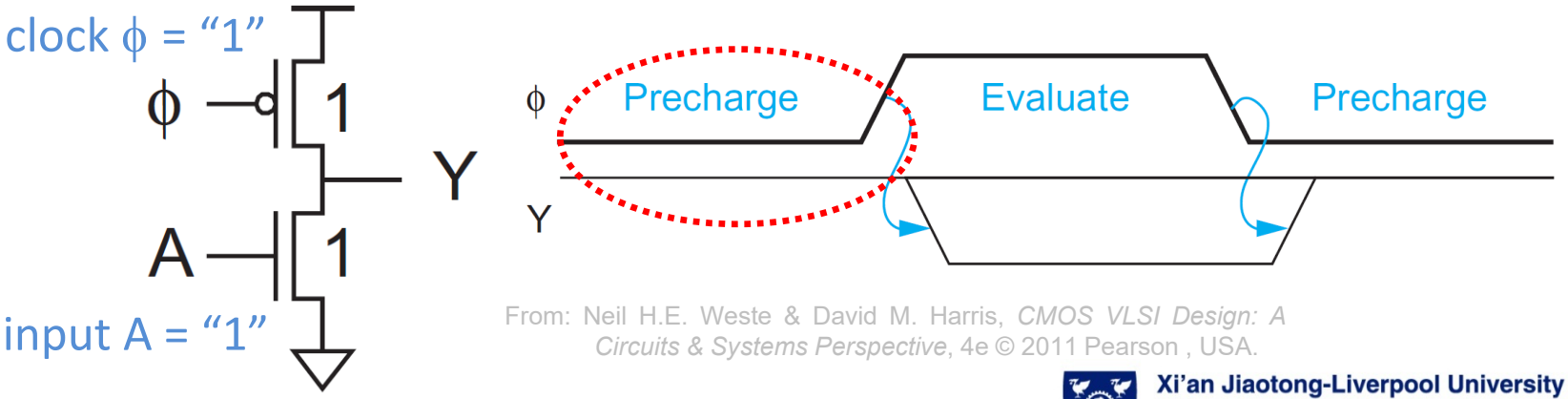
Dynamic Logic – precharge mode

(contention in pulling up & down)

- With only the pull-up pMOSFET clocked, there can be problems during the **precharge** mode:
  - if the input A is "1" hence the pull-down nMOSFET turns on, both the pMOSFET and nMOSFET are on and contention will take place between them (i.e. the two MOSFETs fight to pull up or down the output voltage).



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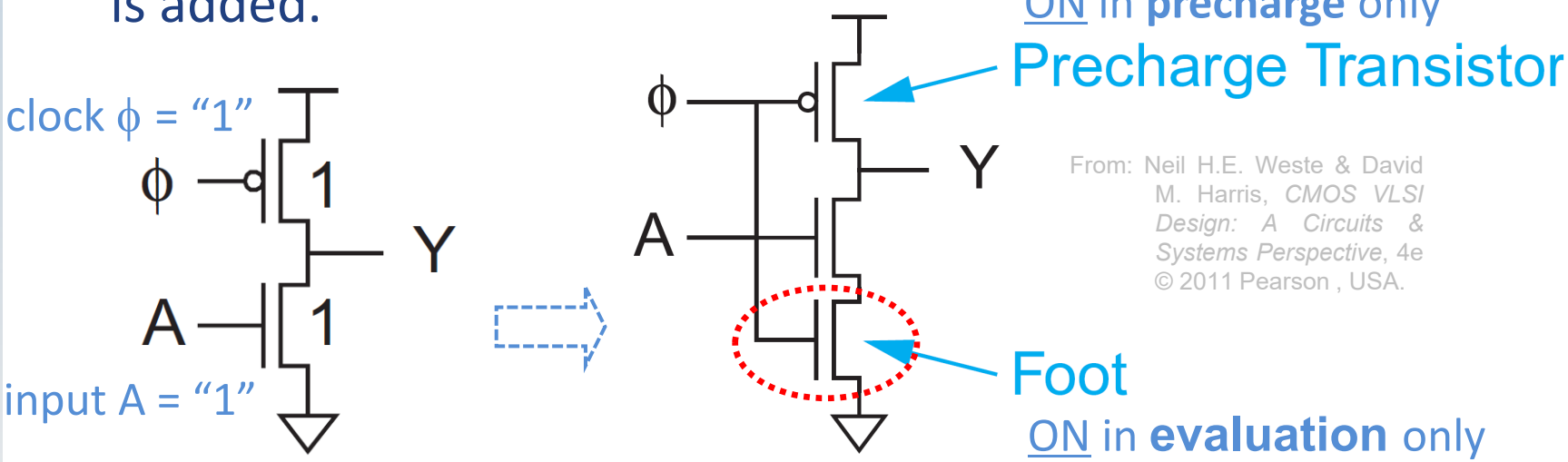
Dynamic Logic – precharge mode

(extra clocked evaluation transistor)

- To avoid such a contention situation that both pull-up and pull-down MOSFETs turn on, an extra ***evaluation*** transistor is added.



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  - The extra ***clocked*** transistor is an nMOSFET stacked under the pull-down network (one nMOSFET in the inverter case). It is sometimes called a **foot**.

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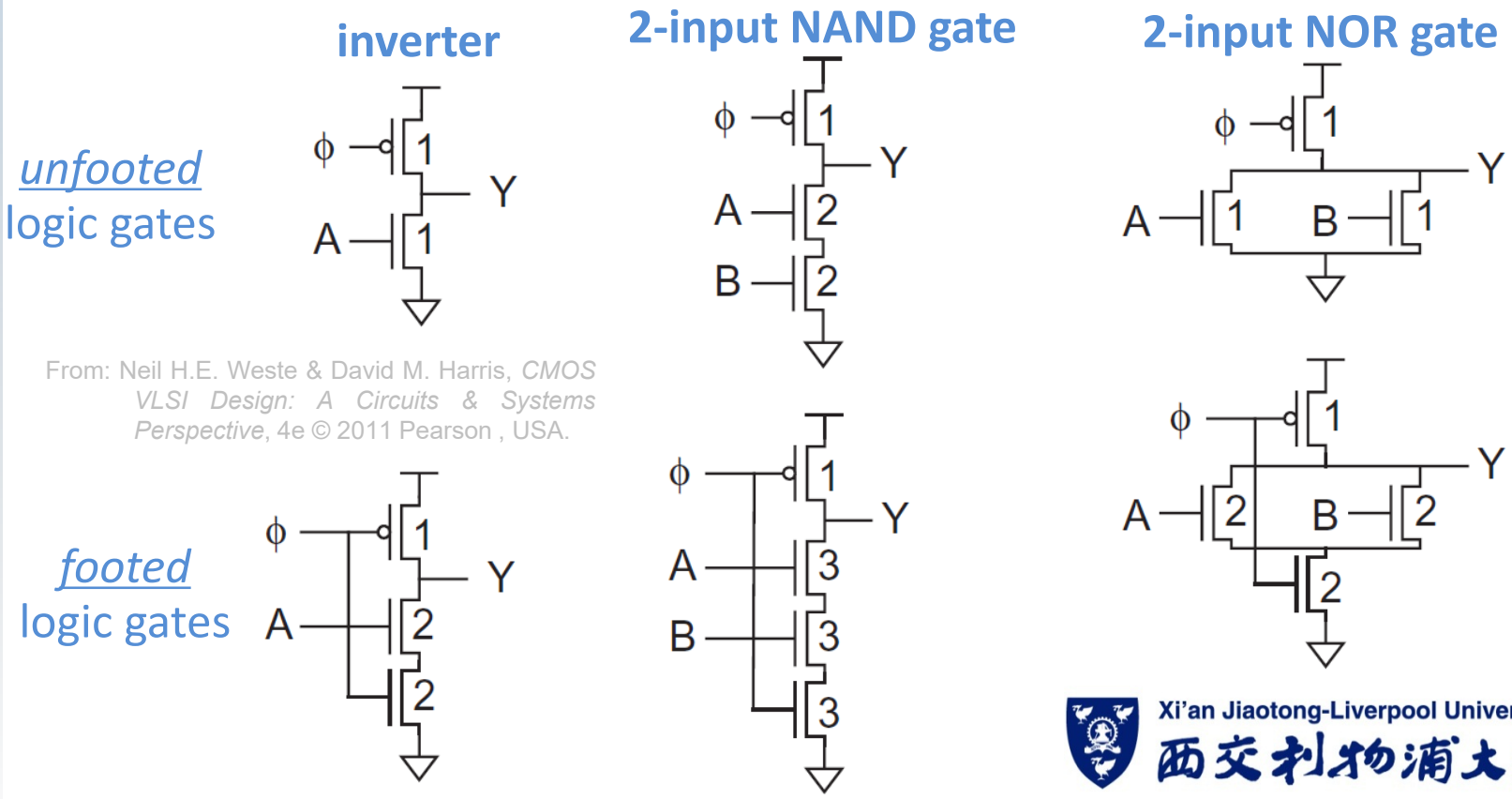
Dynamic Logic

(footed & unfooted logic gates)

- Examples of dynamic logic gates with the extra clocked MOSFET is shown below:



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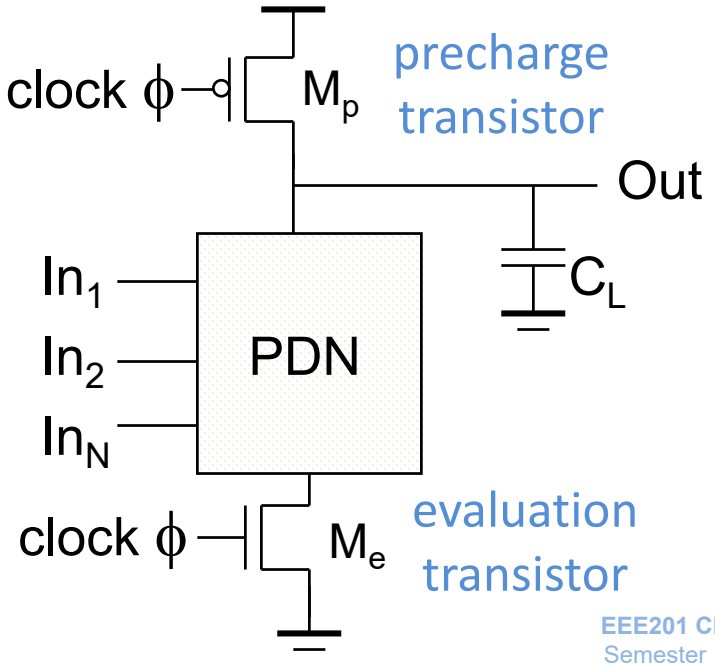
Dynamic Logic
(footed & unfooted logic gates)

- In general, a **dynamic logic** circuit consists of three parts stacked on one another:
  - a ***clocked* pMOSFET** (called a precharge transistor);
  - a **pull-down network** (PDN) of nMOSFETs for performing logic function; it is exactly the same as that in CMOS logic;
  - a ***clocked* nMOSFET** (called a foot or evaluation transistor).
  - The number of MOSFETs required for implementing a logic circuit of *N* inputs is *N*+2 which is generally smaller than 2*N* in CMOS logic.



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Dynamic Logic
(important properties)

- Several important properties can be derived for the **dynamic logic**:
  - It is non-*ratioed*: the size of the precharge pMOSFET is not important for the correct operation of the logic gates; the size of the pMOSFET can be made large to improve the low-to-high transition time (but at a cost to the high-to-low transition time).
  - It consumes only ***dynamic*** **power**. Ideally, there is no static current path exists between V_{DD} and the ground.
  - The logic gates have faster **switching speed**, due to the reduced input capacitance of the logic gates (with less MOSFETs per gate).
  - $\boldsymbol{V}_{OL}$ is ground (or V_{SS}) & $\boldsymbol{V}_{OH} = V_{DD}$.

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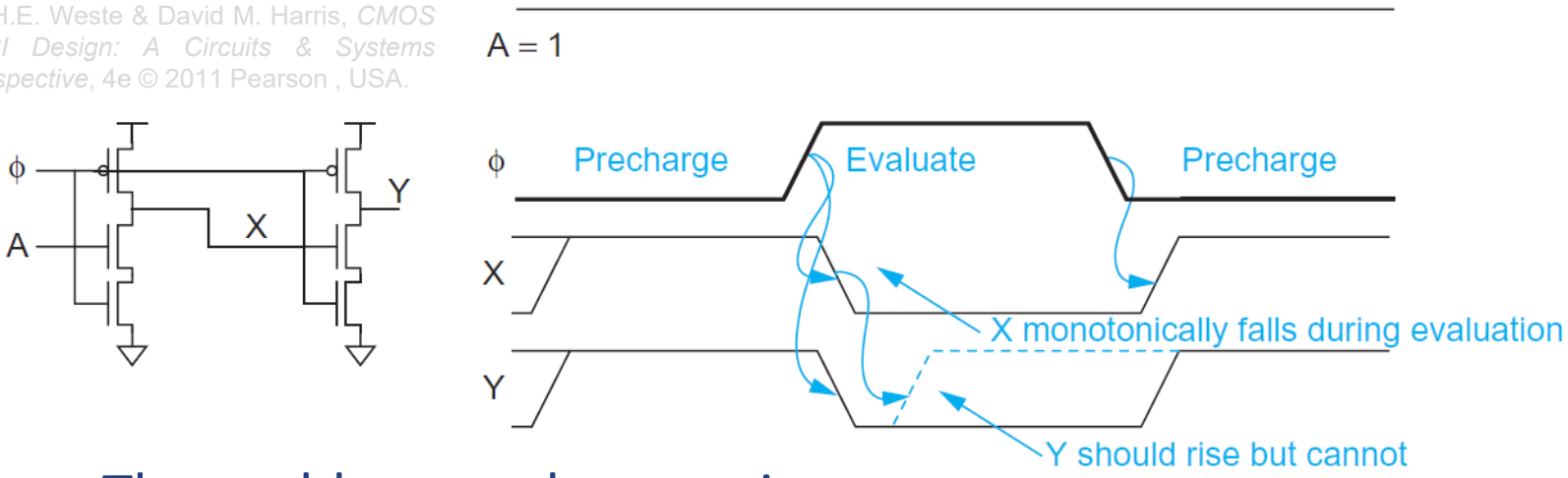
Dynamic Logic
(monotonicity problem)

- Despite the apparent advantages (especially the faster switching speed and zero static power dissipation) of the **dynamic logic**, it suffers from monotonicity problem:
  - During evaluation, the inputs must be monotonically rising; they cannot start "1" and fall to "0".



  - The problem can be seen in cascaded dynamic logic gates.

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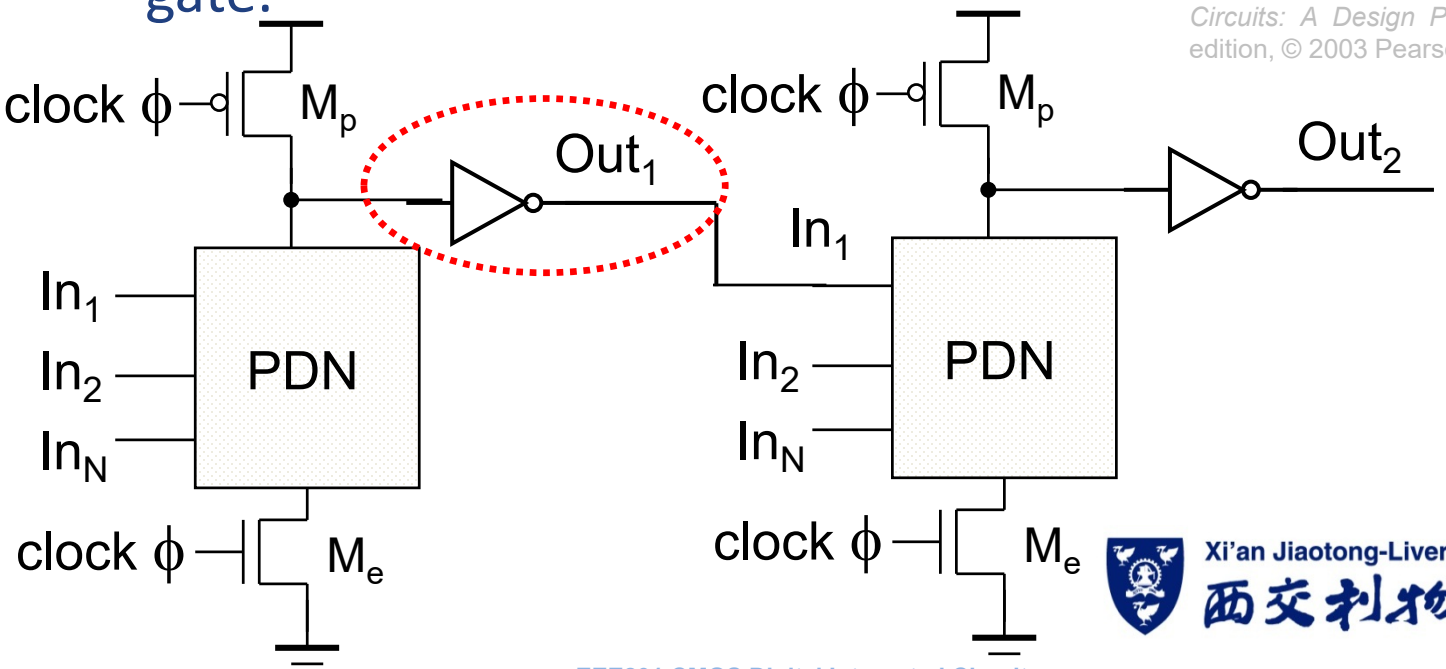
Domino CMOS Logic

(monotonicity problem)

- The monotonicity problem in the **dynamic logic** can be resolved by placing a static CMOS inverter between the dynamic logic gates.
  - The **dynamic-static pair** together is called a **domino logic** gate.



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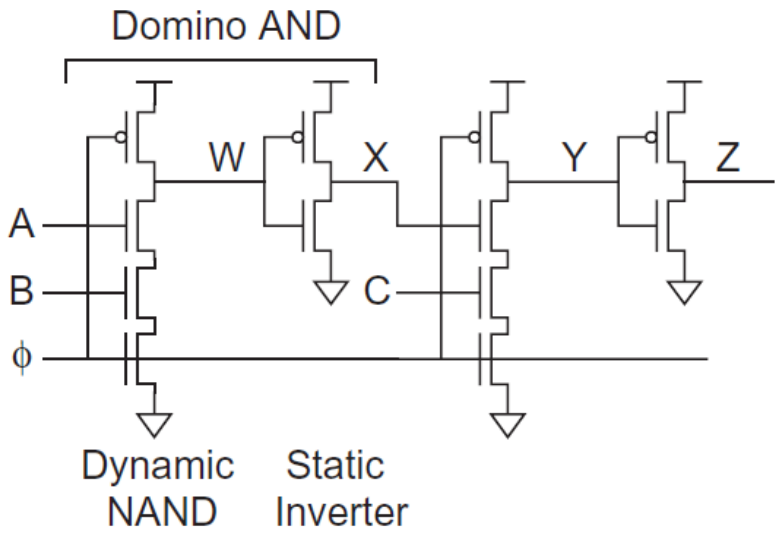
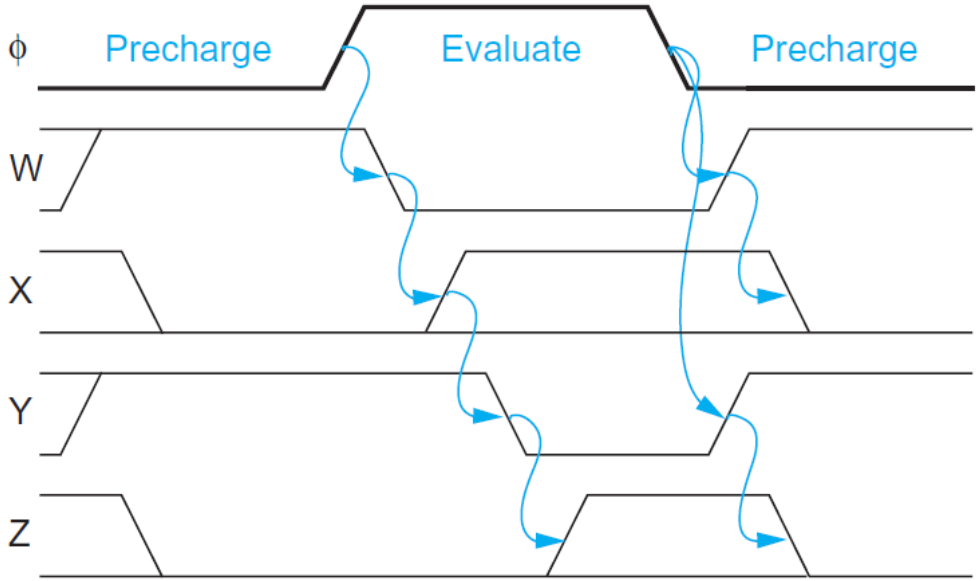
Domino CMOS Logic

(like dominos tipping over)

- The name domino logic derives from the fact that precharge resembles setting up a chain of dominos and evaluation causes the logic gates to fire like dominos tipping over, each triggering the next.





- This can be illustrated using a two cascading domino AND gates.

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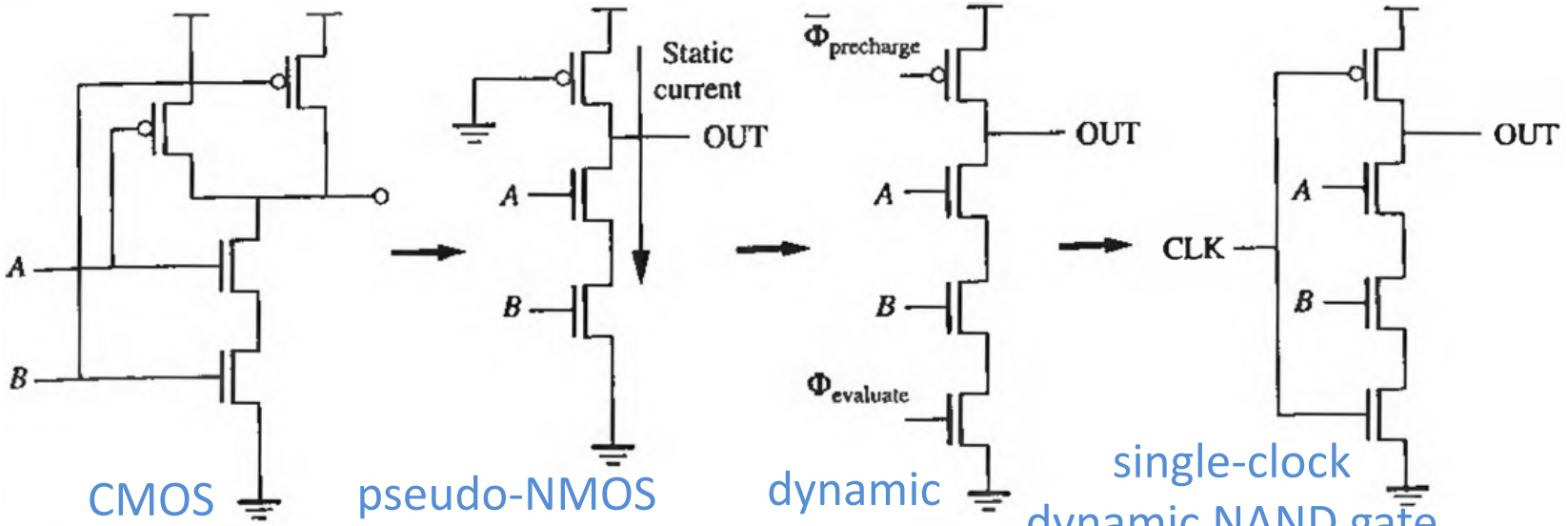
Pseudo-NMOS to Dynamic Logic

(comparisons with CMOS logic)

- The **domino logic** is developed from **dynamic logic** which is in turn from pseudo-NMOS (which is ratioed logic and has static power dissipation problems).
  - Their comparisons can be seen using a 2-input NAND gate.



CMOS NAND gate

pseudo-NMOS NAND gate

dynamic NAND gate

single-clock dynamic NAND gate

From: D.A. Hodges *et al.*, *Analysis and Design of Digital Integrated Circuits: In Deep Submicron Technology*, 3rd edition, © 2003 McGraw Hill, USA.

Xi'an Jiaotong-Liverpool University 西交利物浦大學