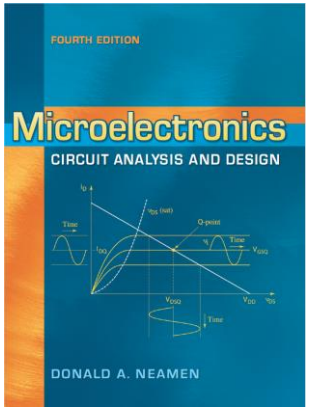
Announcements:

- Provide your feedback on Practical Lectures:
  - Please tap here to proceed…

- Reading material and Practice exercises:
  - **Microelectronics: Circuit Analysis and Design** by Donald A. Neamen
  - Reading/Examples to learn, **Exercises to practice**
  - **Can help you a lot for exam preparation!**



- My office hours:
  - Regular time: every Thursday in SC465 16:00-18:00

- Module Questionnaire (MQ):
  - Please tap here to proceed…

Revision session

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Outline

- Part 1: Differential amplifiers
- Part 2: Current Mirror Circuits
- Part 3: Introduction to Feedback
- Part 4: Frequency Response and Stability of Amplifier Circuits with Feedback

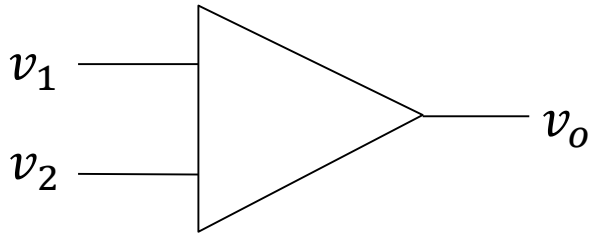
Part 1:

Differential amplifiers

- Reading material:
  - Microelectronics: Circuit Analysis and Design:
    - Chapter 11: Sec. 11.2 – Basic BJT Differential Pair
- Practice exercises:
  - Microelectronics: Circuit Analysis and Design, Chapter 11
    - Chapter 11: Ex. 11.1-3; 11.5-6

Diff-amp: Block diagram and Input modes

Suppose the input signals to a differential amplifier v_1 and v_2 consist of a common-mode voltage v_{cm} applied to both inputs and a difference voltage v_d shared between them, then



$$v_1 = v_{cm} + \frac{v_d}{2} \qquad v_2 = v_{cm} - \frac{v_d}{2}$$

so $v_d = v_1 - v_2$

Note *that the differential-mode signal is simply equal to the difference between the values of* v_1 *and* v_2

and $v_{cm} = \frac{v_1 + v_2}{2}$

but the common-mode signal is equal to the average value of v_1 *and* v_2

Now, the actual output is found as: $v_o = A_d v_d + A_{cm} v_{cm}$

Diff-amp: Common mode rejection ratio, CMRR

This is an important figure of merit for a differential amplifier that tells us how good it is at rejecting the unwanted common mode signal (CM) relative to the differential signal that we want to amplify (DM). We clearly want a high differential gain and a low common mode gain.

As a measure of this, we define $$CMRR = \left|\frac{A_d}{A_{cm}}\right|$$

Usually, it is measured in decibel (dB): $$CMRR\Big|_{dB} = 20\log_{10}\left|\frac{A_d}{A_{cm}}\right|$$

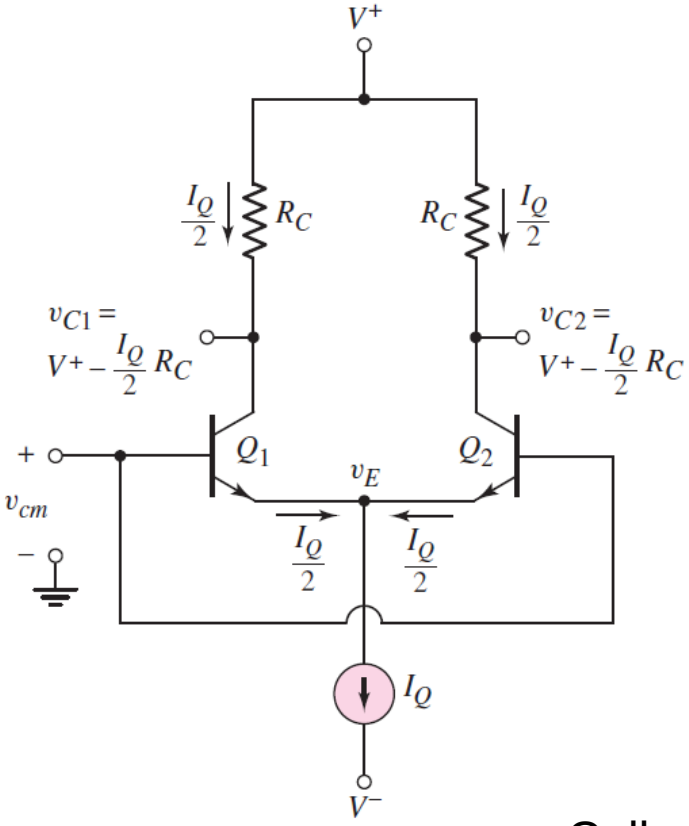
The aim is to have CMRR as large as possible.

Commercial op-amps offer:
741 $CMRR|_{dB}$ = 70 – 90 dB
OP07 $CMRR|_{dB}$ = 94 – 106 dB

How big is the actual ratio?
741 $CMRR =$
OP07 $CMRR =$

The differential signals are amplified several thousand times more than the common mode signals.

Qualitative analysis: common-mode input voltage



Common emitter voltage: $v_E = v_{cm} - V_{BE}(on)$

Emitter currents: $i_{E1} = i_{E2} = \frac{I_Q}{2}$

If base currents negligible: $i_{CQ1} \cong i_{E1}$

and $i_{CQ2} \cong i_{E2}$

The current going through collectors/emitters in common-mode is called **Quiescent current. It establishes small-signal transistor characteristics:**

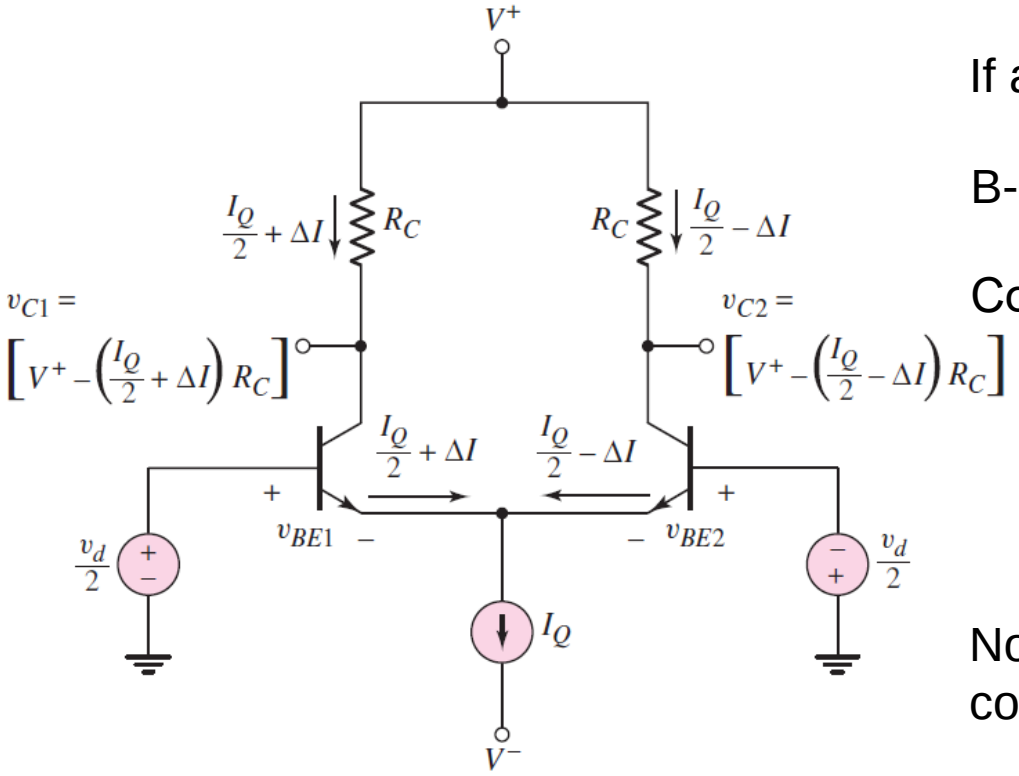
Must remember: $g_m = \frac{i_{CQ}}{V_T}$ and $r_\pi = \frac{\beta}{g_m}$

Collector voltages identical: $v_{C1} = V^+ - \frac{I_Q}{2}R_C = v_{C2}$

For an applied common-mode voltage, I_Q splits evenly between *Q*1 and *Q*2 and the difference between v_{C1} and v_{C2} is zero

– common-mode output

Qualitative analysis: differential-mode input voltage



If a diff-mode input voltage v_d is applied

B-E voltages of Q1 and Q2: $v_{BE1} > v_{BE2}$

Collectors' currents change by $\pm\Delta I$:

$$i_{C1} = \frac{I_Q}{2} + \Delta I$$

and $$i_{C2} = \frac{I_Q}{2} - \Delta I$$

Now, the voltage difference between collectors appears:

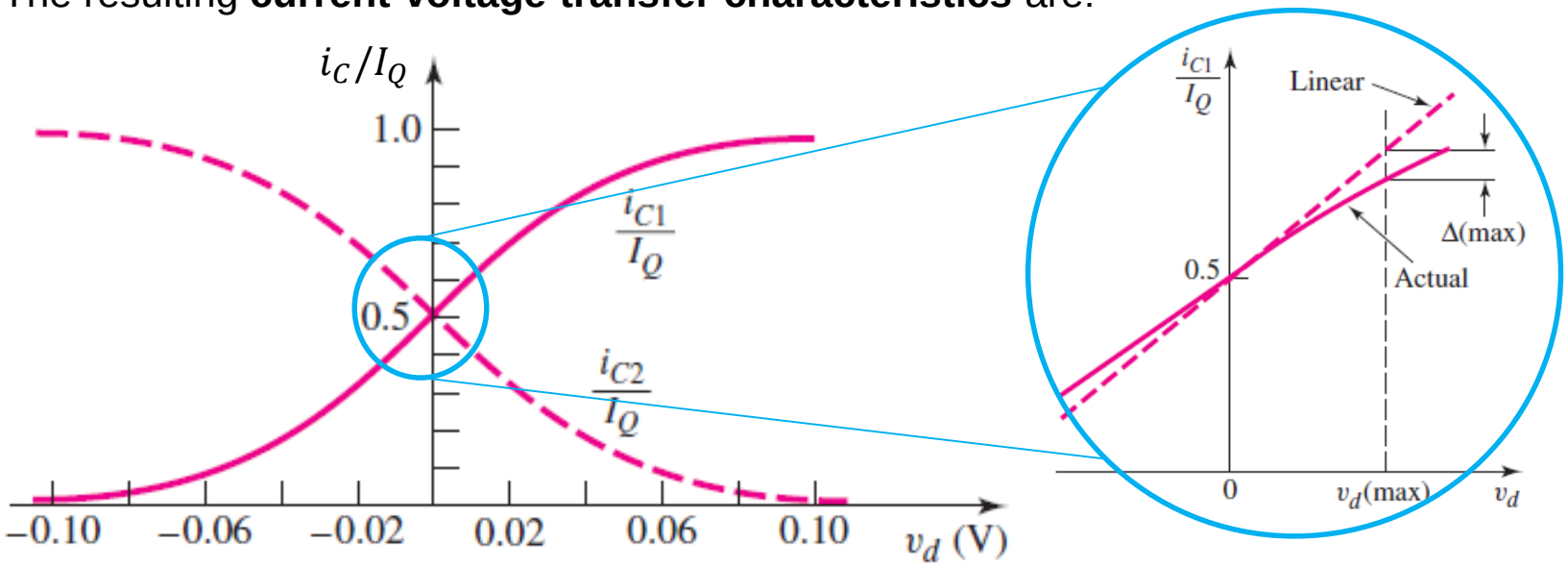
$$v_{C2} - v_{C1} = \left[V^+ - \left(\frac{I_Q}{2} - \Delta I\right)R_C\right] - \left[V^+ - \left(\frac{I_Q}{2} + \Delta I\right)R_C\right] = 2 \cdot \Delta I \cdot R_C$$

A voltage difference is created between v_{C2} and v_{C1} when a differential-mode input voltage is applied **– differential-mode output**

DC transfer characteristics of the basic diff-amp

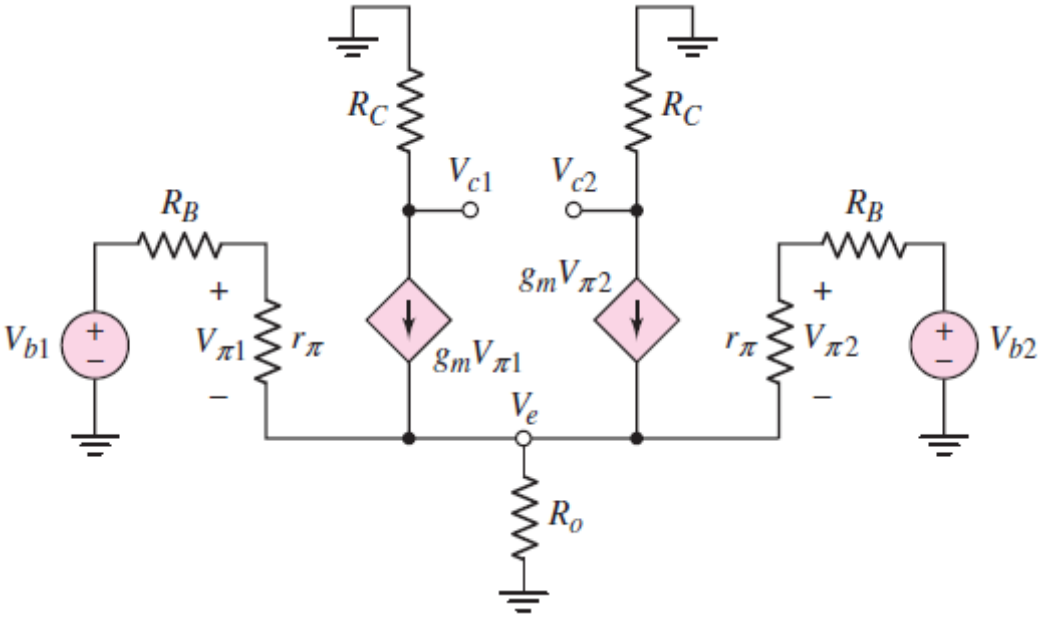
Normalizing i_{C1} and i_{C2} wrt I_Q will give: $\frac{i_{C1}}{I_Q} = \frac{1}{1+\exp\left(\frac{-v_d}{V_T}\right)}$ and $\frac{i_{C2}}{I_Q} = \frac{1}{1+\exp\left(\frac{+v_d}{V_T}\right)}$

The resulting **current-voltage transfer characteristics** are:



- The gain of the diff-amp is nonlinear for wide range of diff-mode inputs – v_d must be kept small to maintain a linear operation;
- If v_d is kept small enough, diff-amp can be represented with its small signal quivalent circuit represented on the next slide

Small-signal equivalent circuit analysis – output voltage



No need to remember long equations. Just be able to derive them.

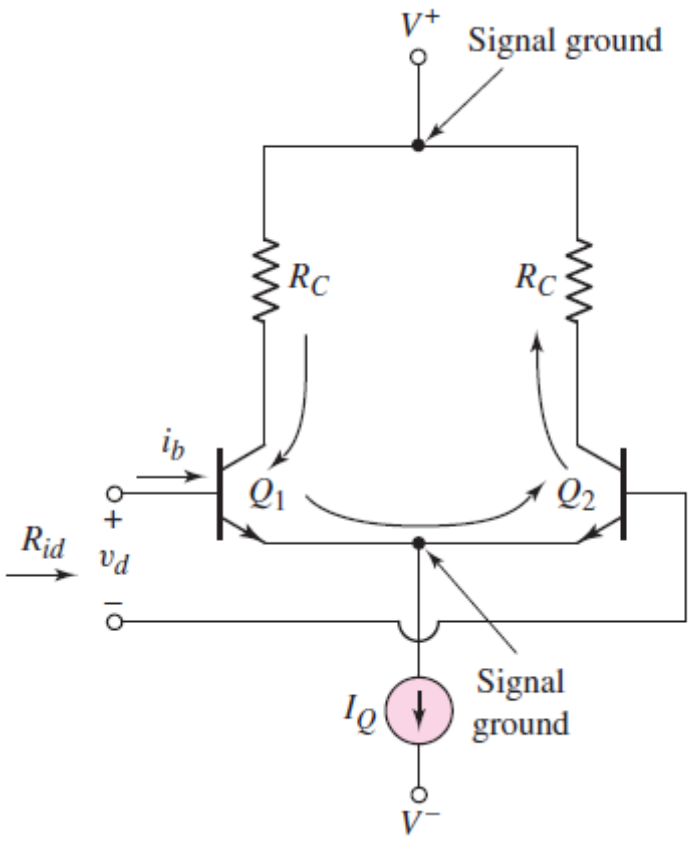
Emitter voltage: $$V_e = \frac{V_{b1} + V_{b2}}{2 + \dfrac{r_\pi + R_B}{(1+\beta)R_o}}$$

Output voltage: $$V_o = \frac{-\beta R_C}{r_\pi + R_B} \left\{ \frac{V_{b2}\left[1 + \dfrac{r_\pi + R_B}{(1+\beta)R_o}\right] - V_{b1}}{2 + \dfrac{r_\pi + R_B}{(1+\beta)R_o}} \right\}$$

From diff- and com-mode signals: $$V_o = \frac{\beta R_C}{2(r_\pi + R_B)} \cdot V_d - \frac{\beta R_C}{r_\pi + R_B + 2(1+\beta)R_o} \cdot V_{cm}$$

Input impedance of the basic diff-amp

The input resistance (or impedance) determines the loading of the circuit on the signal source – the higher the better.



There are:

- **Differential-mode input resistance** – the effective resistance between the two input base terminals when a differential-mode signal is applied:

  For the voltage source current: $i_s = i_b = v_d/2r_\pi$

  Therefore, the internal resistance of the diff-amp in **differential-mode**: $R_{id} = \frac{v_d}{i_s} = 2r_\pi$

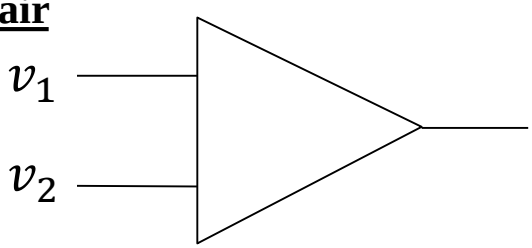
- **Common-mode input resistance** – the effective resistance between the two input base terminals when a common-mode signal is applied:

  For the voltage source current: $i_s = i_{b1} + i_{b2} = 2i_{b1}$

  Therefore, the internal resistance of the diff-amp in common-mode (comm-mode half circuit):

$$R_{icm} = \frac{v_{cm}}{i_s} = \frac{i_{b1}r_\pi + i_{b1}(\beta+1)2R_0}{2i_{b1}} = \frac{r_\pi}{2} + (\beta+1)R_0$$

Summary – basic BJT differential pair



Differential mode

Input resistance

$$R_{id} = 2r_\pi = \frac{4\beta V_T}{I_Q}$$

Voltage gain

$$A_d = \frac{\beta R_C}{2(r_\pi + R_B)}$$

Common mode

Input resistance

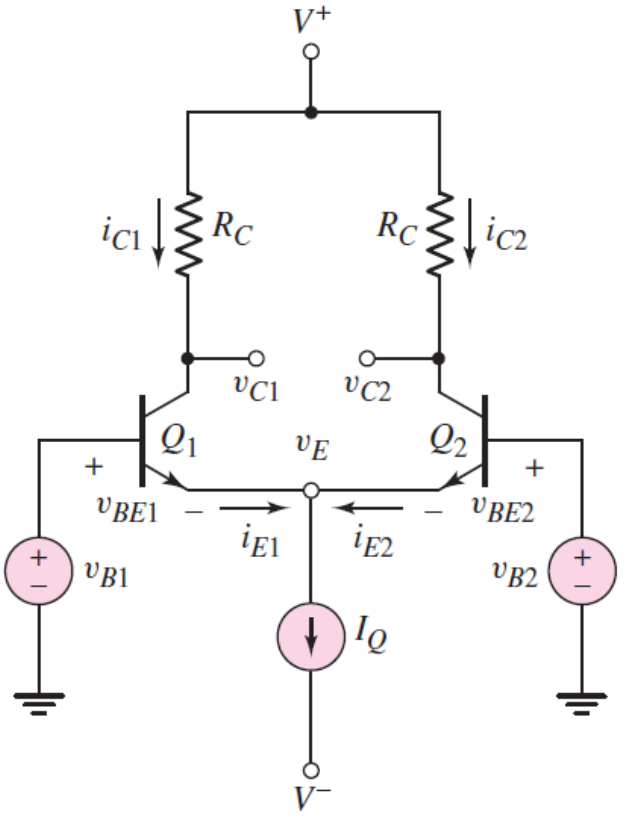
$$R_{icm} = \frac{r_\pi}{2} + (\beta + 1)R_0 \approx \beta R_0$$

Voltage gain

$$\mathrm{A_{cm}} = \frac{-\beta R_C}{r_\pi + R_B + 2(1+\beta)R_0} \approx -\frac{R_C}{2R_0}$$

Common Mode Rejection Ratio

$$CMRR = \left|\frac{A_d}{A_{cm}}\right| \approx \frac{(1+\beta)R_0}{r_\pi + R_B}$$



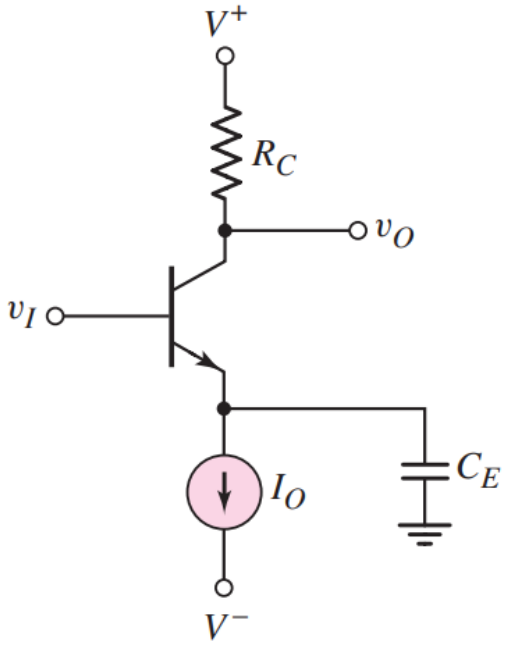
Part 2:

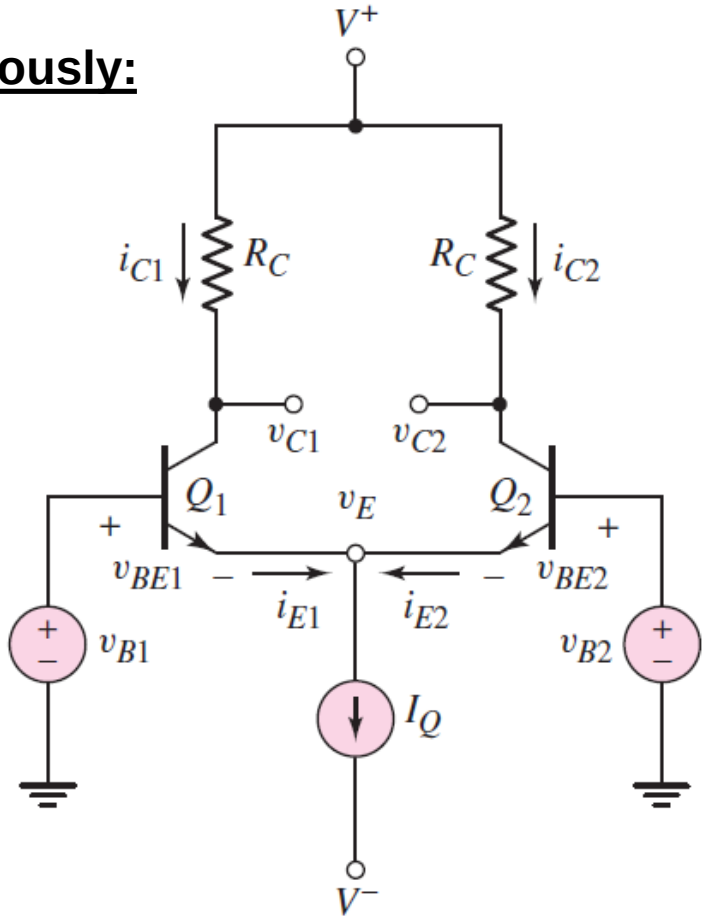
Current Mirror Circuits

- Reading material:
  - Microelectronics: Circuit Analysis and Design:
    - Chapter 10: Sec. 10.1 – Bipolar Transistor Current Sources
    - Chapter 11: Sec. 11.4 – Differential Amplifier with Active Load

- Practice exercises:
  - Microelectronics: Circuit Analysis and Design, Chapter 10
    - Chapter 10: Ex. 10.1-10.7
    - Chapter 11: Ex. 11. 10

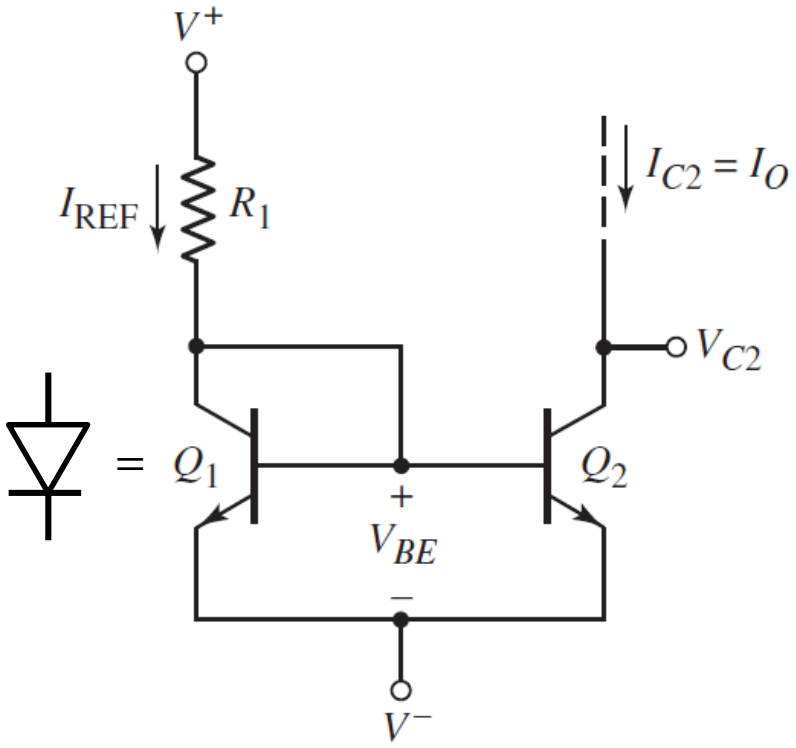
Linear amplifiers you studied previously:





- In the previous lectures, when the bipolar transistors are used within a linear amplifying device, they must be biased in the forward-active mode.
- The bias may be a current source that establishes the quiescent collector current.
- We now need to consider the types of circuits that can be designed to establish the bias currents I_O and I_Q.

Two-transistor current source analysis – Current Relationships



1. The reference current I_{REF} is established by resistor R_1 and transistor Q1 connected as a diode:

$$I_{REF} = \frac{V^+ - V_{BE} - V^-}{R_1}$$

2. As $V_{BE1} = V_{BE2} = V_{BE}$ then $I_{B1} = I_{B2}$ and $I_{C1} = I_{C2}$.

Therefore, KCL for collector node of Q1:

$$I_{REF} = I_{C1} + I_{B1} + I_{B2} = I_{C1} + 2I_{B2}$$

3. Replacing I_{C1} by I_{C2} and noting that $I_{B2} = I_{C2}/\beta$:

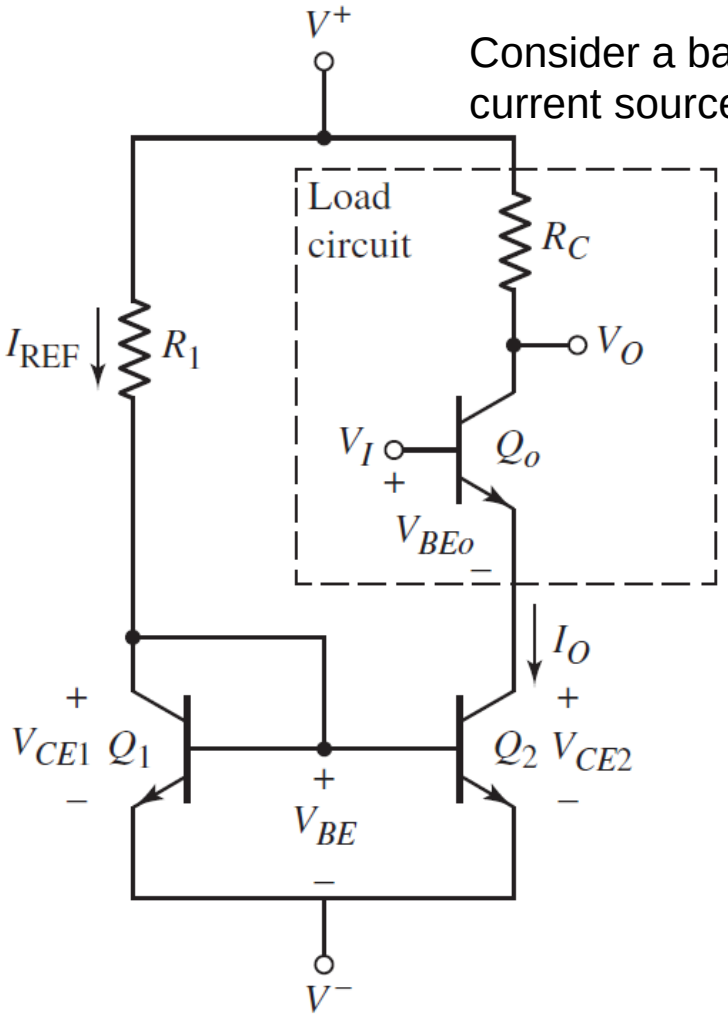
$$I_{REF} = I_{C2} + 2\frac{I_{C2}}{\beta} = I_{C2}\left(1 + \frac{2}{\beta}\right)$$

4. Output current is then:

$$I_O = I_{C2} = \frac{I_{REF}}{\left(1 + \frac{2}{\beta}\right)}$$

Note that the last equation gives the ideal output current for infinite Early voltage ($V_A = \infty$)

Two-transistor current source analysis – Output resistance



Consider a basic transistor amplifier biased with the two-transistor current source. The stability of a load current generated in a constant-current source is a function of the output resistance looking back into the output transistor Q2:

1. The change in load current with a change in voltage $V_{E0} = V_{C2}$ determines the output conductance:

$$\frac{dI_O}{dV_{C2}} = \frac{1}{r_O}$$

2. The output (collector) voltage is determined by:

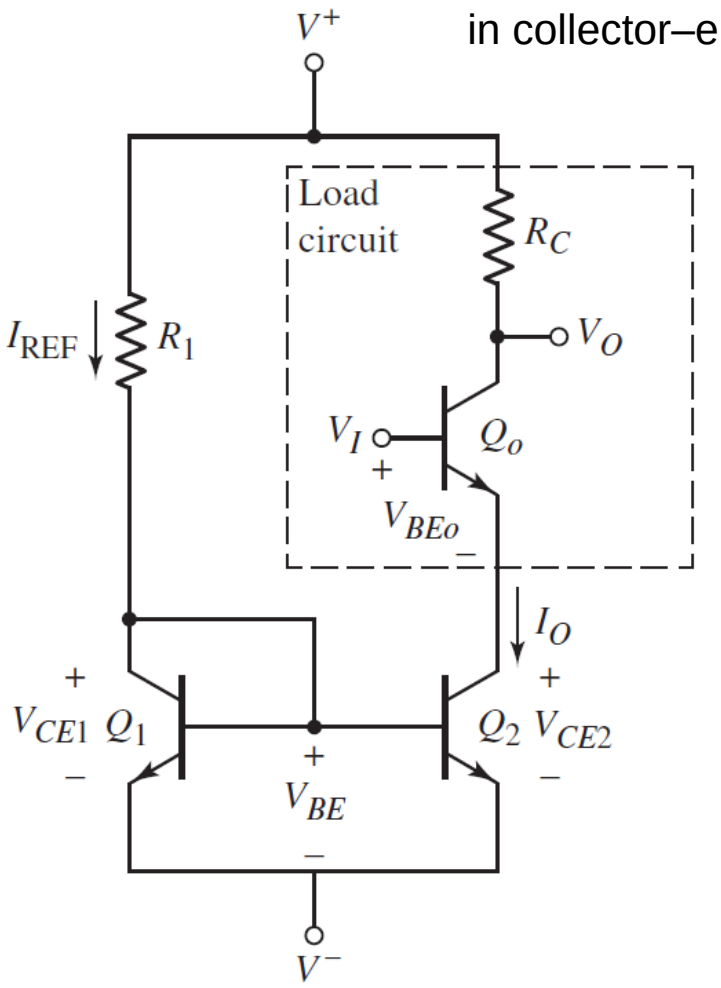
$$V_{C2} = V_{CE2} + V^- \quad \Rightarrow \quad dV_{C2} = dV_{CE2}$$

3. Taking the Early voltage into account, the output-reference currents relationship is established by:

$$I_O = \frac{I_{REF}}{\left(1 + \frac{2}{\beta}\right)} \times \frac{1 + \frac{V_{CE2}}{V_A}}{1 + \frac{V_{CE1}}{V_A}}$$

Exercise:

Task: Determine the change in load current produced by a change in collector–emitter voltage in a two-transistor current source.



Circuit parameters:
$V^+ = 5$ V;
$V^- = -5$ V;
$R_1 = 9.3$ kOhm.

Transistor parameters:
$V_{BE}(on) = 0.7$ V
$\beta = 50$;
$V_A = 80$ V.

Find percentage of I_O change when V_{CE2} varies from 0.7 to 5V:

Solution:

1. The reference current is:

$$I_{REF} = \frac{V^+ - V_{BE}(on) - V^-}{R_1} = 1\ mA;$$

2. Output current for $V_{CE2} = 0.7$ V is:

$$I_O(0.7) = \frac{I_{REF}}{1 + 2/\beta} = 0.962\ mA;$$

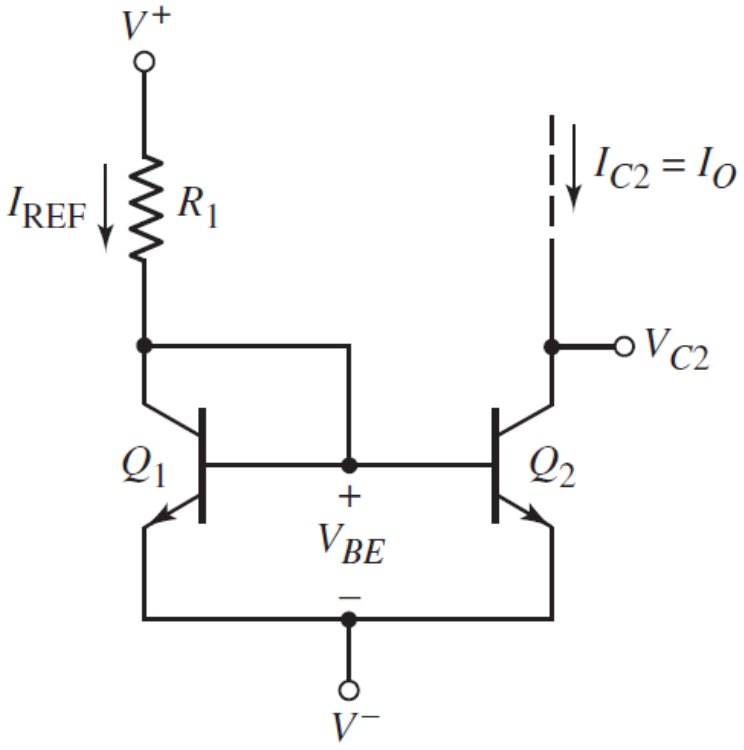
3. The small-signal output resistance is:

$$r_O = \frac{V_A}{I_O} = 83.2\ kOhm;$$

4. The change in the load current can be found:

$$dI_O = \frac{1}{r_O} dV_{CE2} = 0.052\ mA$$ Or in percentages, it is: $dI_O/I_O = 0.054$ or 5.4%.

Two-transistor current source analysis – Mismatched Transistors



1. Consider exponential collector current-voltage relationships (neglecting the Early effect and base currents):

$$I_{REF} \cong I_{C1} = I_{S1} e^{V_{BE1}/V_T}$$

and

$$I_O = I_{C2} = I_{S2} e^{V_{BE2}/V_T}$$

For not identical transistors $I_{S1} \neq I_{S2}$; however, due to the circuit configuration $V_{BE1} = V_{BE2} = V_{BE}$.

Therefore, the relationship between the output (bias) and reference currents is found as:

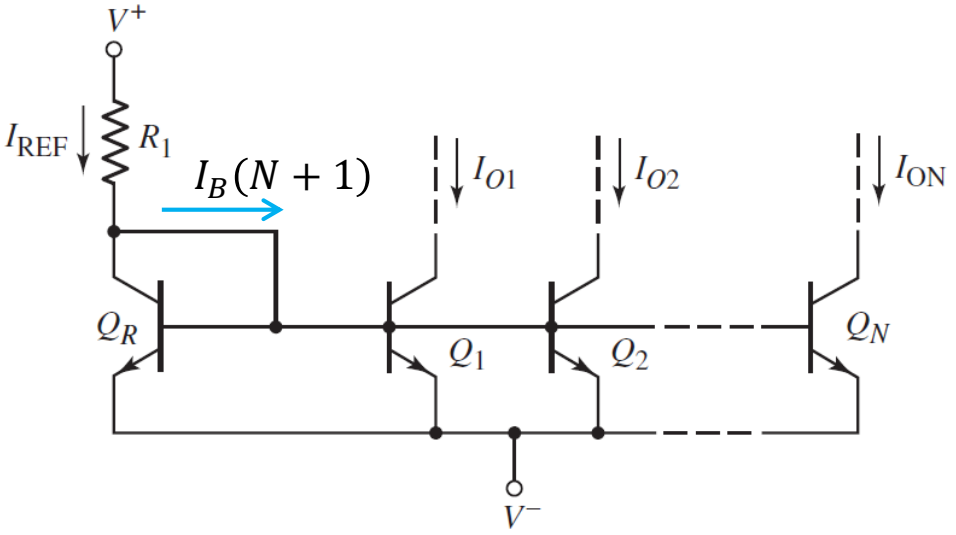
$$I_O = I_{REF} \left(\frac{I_{S2}}{I_{S1}} \right).$$

The reverse-saturation currents I_{S1} and I_{S2} of transistors are functions of the cross-sectional area of the B–E junctions; therefore, it can be used to our advantage. For example, by using different sizes of transistors, we can design the circuit such that $I_O \neq I_{REF}$

Multitransistor Current Mirrors

To generate multiple load currents, the reference transistor is placed alongside a series of transistors with their base-emitter junctions connected in parallel. The reference current is still found as:

$$I_{REF} = \frac{V^+ - V_{BE} - V^-}{R_1}$$



In this circuit, the reference current also feeds all the transistor base currents.

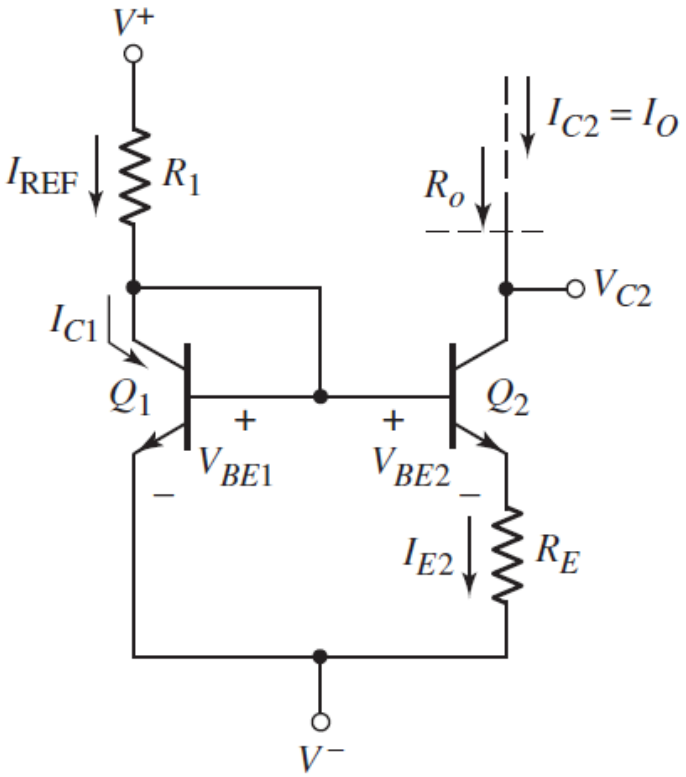
Performing the same analysis as for the two-transistor current mirror, the reference and output currents relationship is:

$$I_{O1} = I_{O2} = \cdots = I_{ON} = \frac{I_{REF}}{1 + (1+N)/\beta}$$

Practice on your own! (based on slide 7)

A limitation of this circuit is that the same current is produced in each load, but usually ***different*** bias currents are required. It is possible to scale the currents - within limits - by scaling up the B-E area of transistors (as discussed previously)

The Widlar current source – Current relationship



1. If Q1 and Q2 are identical and $\beta \gg 1$:

$$I_{REF} \cong I_{C1} = I_S \exp\left(\frac{V^{BE1}}{V_T}\right)$$

and

$$I_O = I_{C2} = I_S \exp\left(\frac{V^{BE2}}{V_T}\right)$$

2. Solving for the B-E voltages:

$$V_{BE1} = V_T \ln\left(\frac{I_{REF}}{I_S}\right) \quad \text{and} \quad V_{BE2} = V_T \ln\left(\frac{I_O}{I_S}\right)$$

3. Their difference yields:

$$V_{BE1} - V_{BE2} = V_T \ln\left(\frac{I_{REF}}{I_O}\right)$$

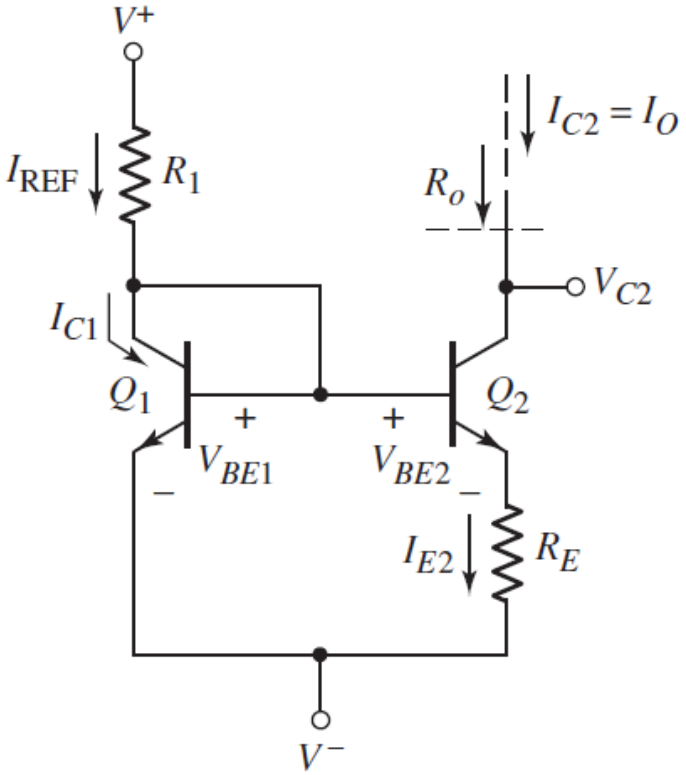
4. Applying KVL to the lower loop we see:

$$V_{BE1} - V_{BE2} = I_{E2} R_E \cong I_O R_E$$

5. Combining (3.) and (4.) will give the currents' relationship: $I_O R_E = V_T \ln\left(\frac{I_{REF}}{I_O}\right)$

This transcendental equation cannot be solved directly for I_O. However, a numerical solution or a trial and error approach can be applied.

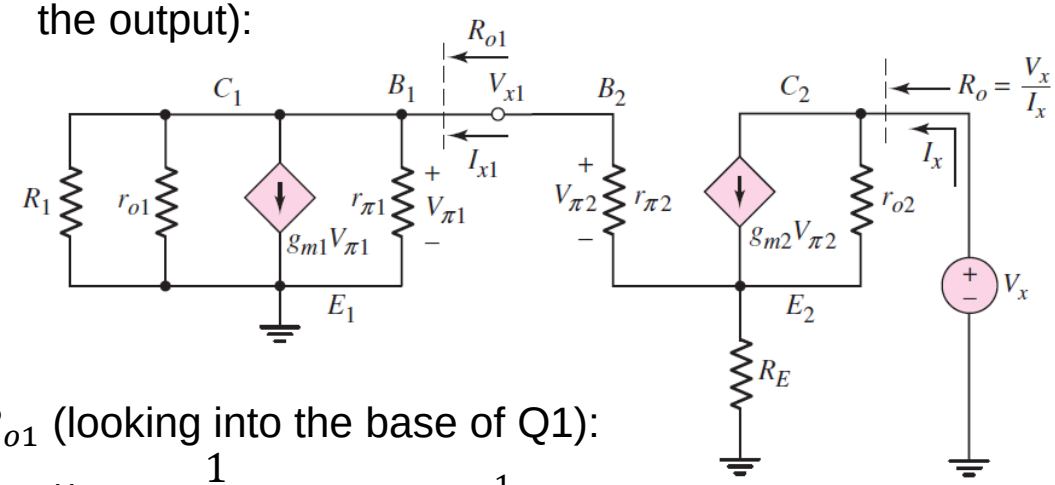
The Widlar current source – Output resistance



Applying test voltage to the output, we need to find output current to derive output resistance as:

$$R_O = \frac{V_x}{I_x}$$

1. This output resistance can be determined using the small-signal equivalent circuit (applying test voltage to the output):



2. First, let us determine resistance R_{o1} (looking into the base of Q1):

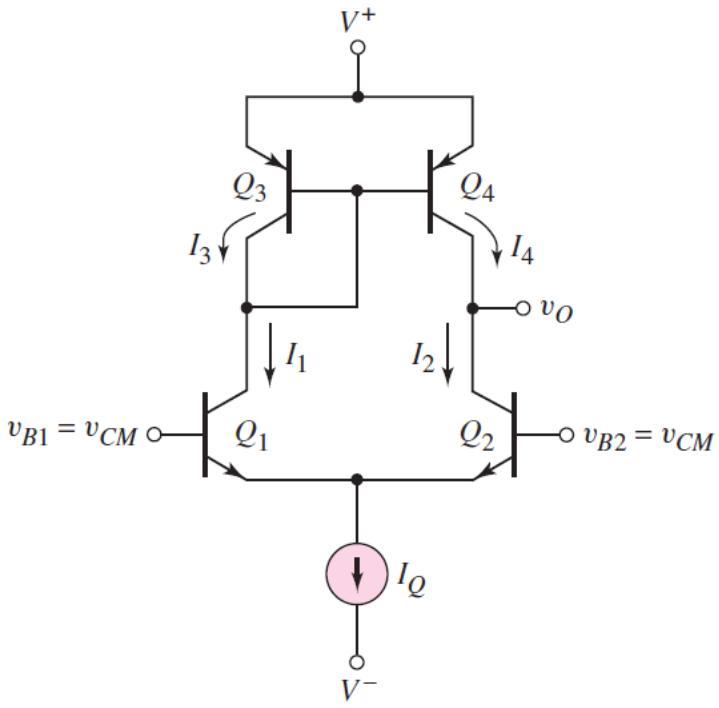
$$R_{o1} = r_{\pi 1} || \frac{1}{g_{m1}} || r_{o1} || R_1 \cong \frac{1}{g_{m1}} \quad \text{because } \frac{1}{g_{m1}} \ll r_{\pi 1}, r_{o1}, \text{ and } R_1$$

For instance, based on the previous example for $I_{REF} = 1\,mA$: $\frac{1}{g_{m1}} = \frac{V_T}{I_{C1}} = 26\,Ohm$

3. Given the fact that $r_{\pi 2} \gg R_{o1}$ we can ignore R_{o1} in the further analysis.

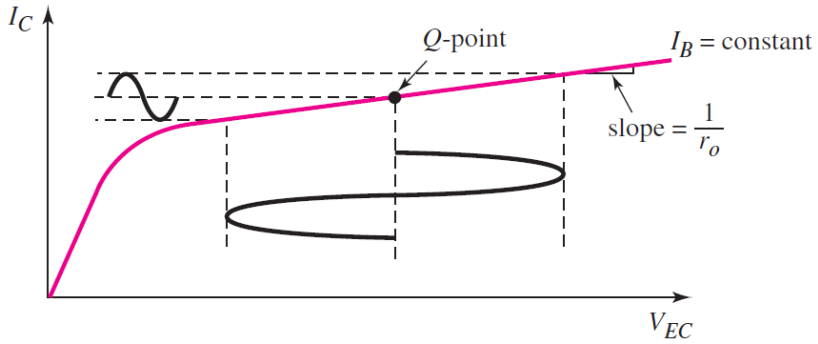
Differential amplifier with active loads – Operational principle

Diff-amp with active load:



Active load is a transistor current source used in place of resistive loads (note, the figure shows pnp transistor current mirror).

The transistors in the active load circuit are biased at a *Q*-point in the forward-active mode as shown below:

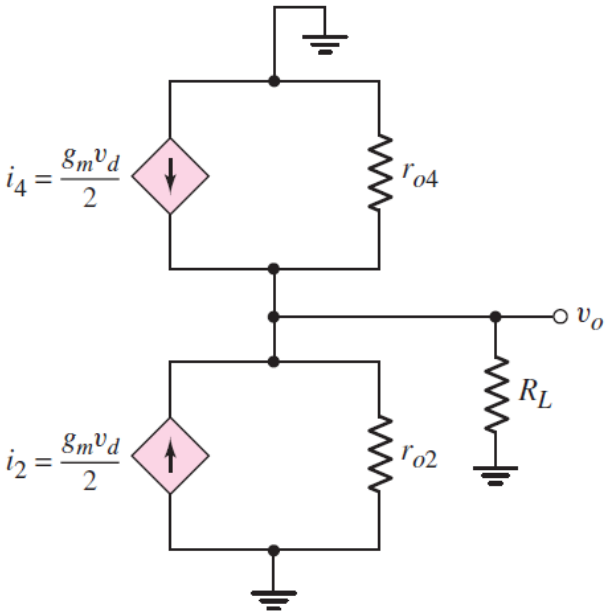


The relation between the change in current and change in voltage is proportional to the small-signal output resistance r_o of the transistor.

Within the same space of IC, the value of r_o can be much larger than that of a discrete resistive load, so the diff-mode voltage gain will be larger with the active load.

Differential amplifier with active loads – Small-signal analysis

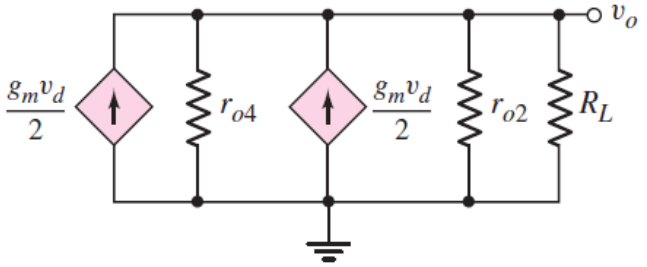
Small-signal equivalent circuit at the collector nodes of *Q*2 and *Q*4:



4. Finally, the output resistance of the diff-amp is nothing but:

$$R_O = r_{o2}||r_{o4}$$

1. Or, it can be rearranged as follows:



2. From the figure above, the output voltage is:

$$v_o = 2\left(\frac{g_m v_d}{2}\right)(r_{o2}||r_{o4}||R_L)$$

3. Therefore, the small-signal diff-mode voltage gain is:

$$A_d = \frac{v_o}{v_d} = g_m(r_{o2}||r_{o4}||R_L)$$

alternatively

$$A_d = \frac{g_m}{g_{o2} + g_{o4} + G_L},$$

where g_{o2}, g_{o4} and G_L are the corresponding conductances.

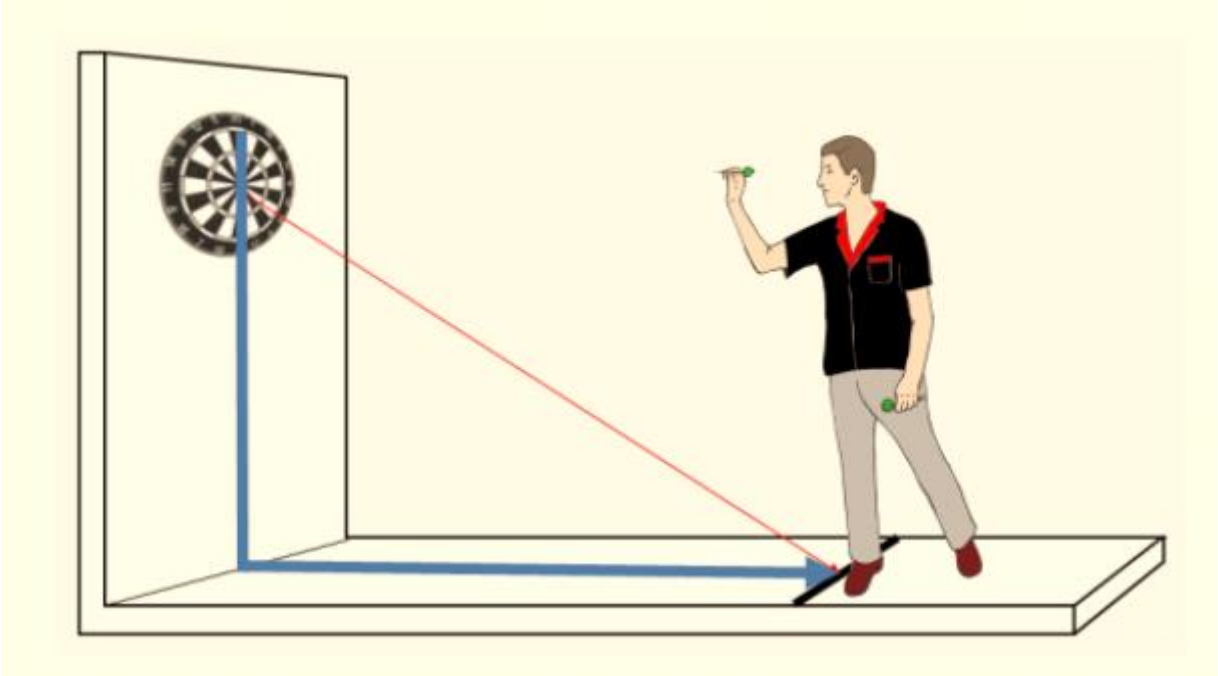
To minimize loading effects, we need $R_L > R_o$. However, since R_o is generally large for active loads, we may not be able to satisfy this condition. And this is the challenge that circuit designers face.

Part 3:
Introduction to Feedback

- Reading material:
  - Microelectronics: Circuit Analysis and Design, Chapter 12:
    - Sec. 12.1 – Introduction to Feedback
    - Sec. 12.2 – Basic Feedback Concepts
    - Sec. 12.3 – Ideal Feedback Topologies
- Practice exercises:
  - Microelectronics: Circuit Analysis and Design, Chapter 12:
    - Ex. 12.1-12.7

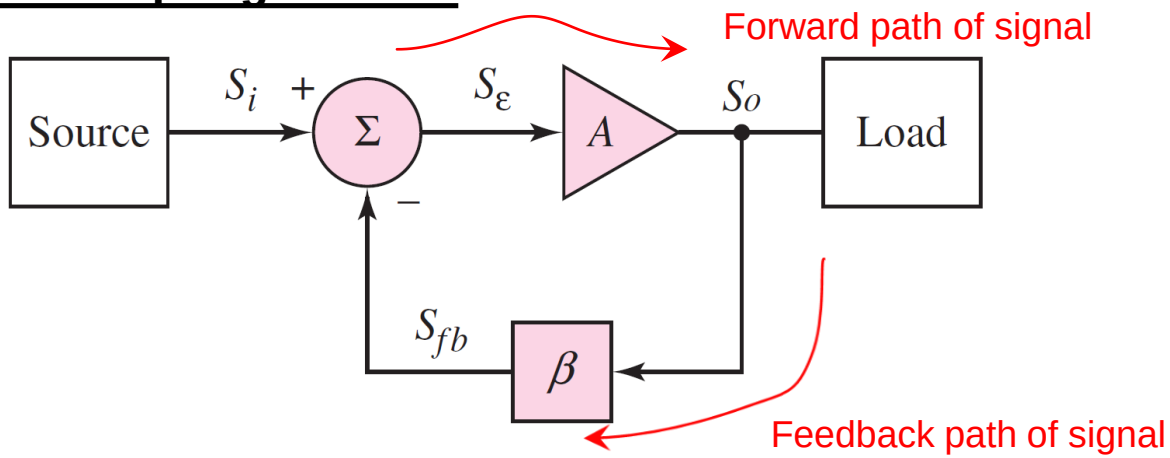
What is feedback?

Example 1: Darts aim and throw



- If you fail at the first time, you will re-adjust the force and the direction to correct it
- This mechanism of **correction** based on the **output** is called **feedback**

Ideal Closed-Loop Signal Gain



Let us analyze the system output wrt to input

1.From the figure, the output signal is:

$$S_o = A\, S_\varepsilon$$

2. At the summing node, we have:

$$S_\varepsilon = S_i - S_{fb}$$

3. The feedback signal is:

$$S_{fb} = \beta\, S_o$$

4.Therefore, the output is found as:

$$S_o = A(S_i - S_{fb}) = A\, S_i - \beta\, A\, S_o$$

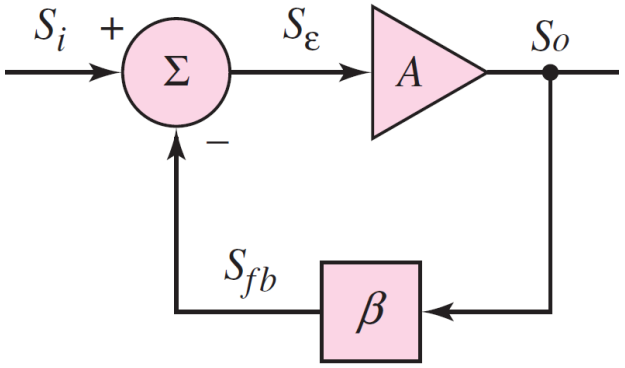
5.After rearrangement, the ideal **closed-loop gain** is found as:

$$A_f = \frac{S_o}{S_i} = \frac{A}{(1+\beta A)} = \frac{A}{(1+T)}$$

where $T = \beta A$ is the loop gain.

Terminology and Notions

$$A_f = \frac{S_o}{S_i} = \frac{A}{(1+\beta A)} = \frac{A}{(1+T)}$$



A_f is the closed-loop gain

A is the open-loop gain

β is the feedback transfer function

$T = \beta A$ is called loop gain

$1 + \beta A$ is called feedback factor

Notice since $S_o = A\, S_\varepsilon$ and $S_{fb} = \beta\, S_o$. Therefore, we have:

$$T = \beta A = S_{fb}/S_\varepsilon$$

In general, the magnitude and phase of the loop gain are also functions of frequency (of the input signal) and they become important for determining the stability of the feedback circuits (will see later).

Normally, the error signal is small, so the expected **loop gain** is large. If the **loop gain** is very large ($\beta A \gg 1$), then:

$$A_f = \frac{S_o}{S_i} = \frac{A}{(1+\beta A)} \approx \frac{A}{\beta A} = \frac{1}{\beta}$$

and the **closed loop gain** is dependent on the **feedback transfer function** only.

This is a very important result, indicating that

- the overall system gain is **no longer dependent** on the gain of the amplifier (A)
- Just make sure that the open loop gain of the amplifier is **large**, so that $\beta A \gg 1$ and the closed-loop gain will be instead set by the **feedback fraction**
- In electronic systems, this often just involves **choosing some resistors** that can be tightly controlled quite easily – and adjusted if desired

Also notice that the closed-loop gain is **reduced** by the feedback factor $(1+\beta A)$ (because this is negative feedback). This quantity is given its special name because it occurs so frequently in feedback theory – it is this same factor by which almost every property of the amplifier circuit is changed e.g. input and output impedances as well as bandwidth

Gain Sensitivity of the feedback system

The sensitivity can be quantified by taking the derivative of A_f with respect to A, while assuming β being a constant:

$$A_f = \frac{S_o}{S_i} = \frac{A}{(1+\beta A)}$$

$$\frac{dA_f}{dA} = \frac{1}{(1+\beta A)} - \frac{A}{(1+\beta A)^2}\beta = \frac{1}{(1+\beta A)^2} \quad \text{or} \quad dA_f = \frac{dA}{(1+\beta A)^2}$$

Dividing both sides by the closed-loop gain A_f yields:

$$\frac{dA_f}{A_f} = \frac{\frac{dA}{(1+\beta A)^2}}{\frac{A}{(1+\beta A)}} = \frac{1}{(1+\beta A)} \cdot \frac{dA}{A}$$

The change in the open-loop gain A of an amplifier (e.g., due to the temperature variation), leads to $(1+\beta A)$ times smaller change in the closed-loop gain A_f.

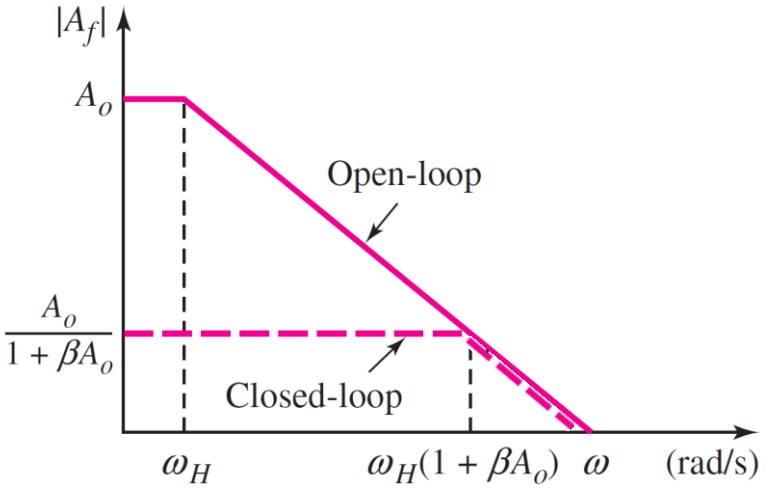
Bandwidth Extension of the feedback system

Assuming the frequency response of a basic amplifier (without feedback) is characterized by a single pole, we can write:

$$A(s) = \frac{A_o}{1 + \frac{s}{\omega_H}}$$

A_o → low-frequency or midband gain

ω_H → upper 3 dB or corner frequency



For the closed-loop gain:

$$A_f(s) = \frac{A(s)}{\left(1 + \beta A(s)\right)} = \frac{\frac{A_o}{1 + \frac{s}{\omega_H}}}{\left(1 + \beta \frac{A_o}{1 + \frac{s}{\omega_H}}\right)} =$$

$$= \frac{A_o}{(1 + \beta A_o)} \cdot \frac{1}{1 + \frac{s}{\omega_H(1 + \beta A_o)}}$$

Low frequency closed-loop gain (A_{fo})

Upper 3 dB frequency (ω_{fH})

We can observe that the gain-bandwidth product will give:

$$A_{fo}\omega_{fH} = \frac{A_o}{(1 + \beta A_o)} \cdot \omega_H(1 + \beta A_o) =$$

$$= A_o\omega_H - \textbf{constant value}$$

- The low-frequency closed loop gain is **reduced** by a factor of $(1 + \beta A_o)$;
- The bandwidth is **extended** by a factor of $(1 + \beta A_o)$;
- Therefore, the gain-bandwidth product is essentially a constant.

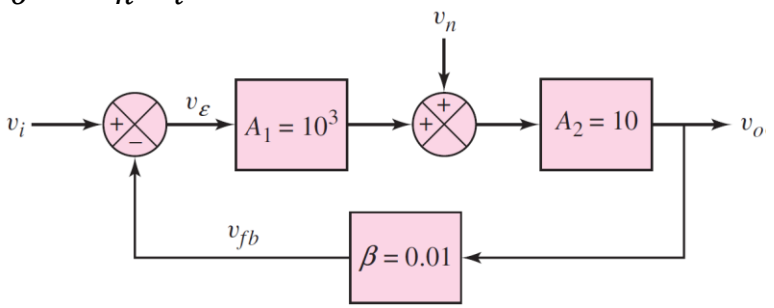
Noise Sensitivity

Noise signal generated within an amplifier can be reduced significantly with the feedback.

First, let us make few definitions:

- The input signal-to-noise ratio: $SNR_i = \frac{S_i}{N_i} = \frac{v_i}{v_n}$ – input source signal, – input noise signal
- The output signal-to-noise ratio: $SNR_o = \frac{S_o}{N_o} = \frac{A_i\, S_i}{A_n\, N_i}$

Consider two amplifiers, where the noise signal is generated between them:



1. The output voltage is: $v_o = A_1 A_2 v_\varepsilon + A_2 v_n$

2. Where the error signal is: $v_\varepsilon = v_i - v_{fb} = v_i - \beta v_o$

3. Solving 1. for v_o will give: $v_o = \frac{A_1 A_2}{(1 + \beta A_1 A_2)} \cdot v_i + \frac{A_2}{(1 + \beta A_1 A_2)} \cdot v_n \cong \frac{1}{\beta} \cdot v_i + \frac{1}{\beta A_1} \cdot v_n$

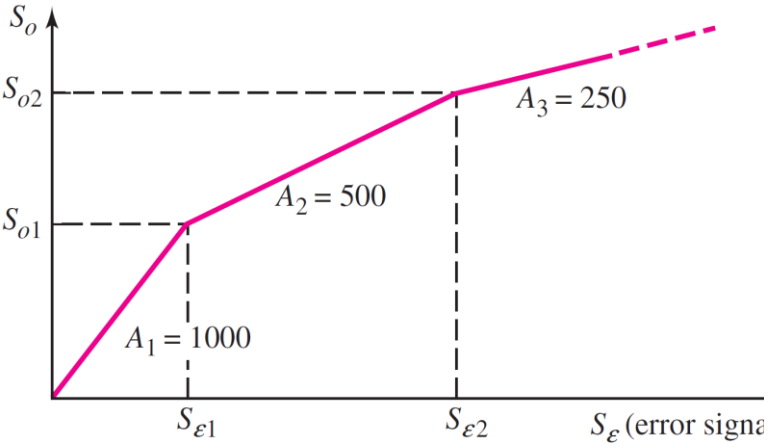
4. Finally, the output SNR: $SNR_o = \frac{S_o}{N_o} = \frac{1/\beta \cdot v_i}{1/\beta A_1 \cdot v_n} = A_1 \frac{S_i}{N_i}$

A large signal-to-noise ratio allows the signal to be detected without any loss of information.

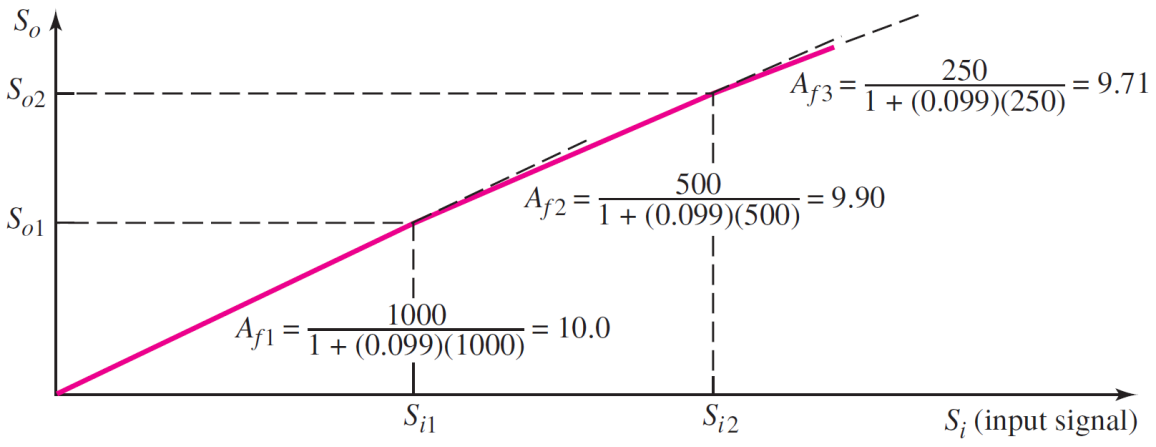
Nonlinear Distortion of the feedback system

Distortion in an output signal is caused by **a change in the basic amplifier gain**, which relates to the nonlinear properties of BJT transistors:

For example, let us assume that the basic amplifier gain is:



For $\beta = 0.099$, the closed-loop gain will look as follows:



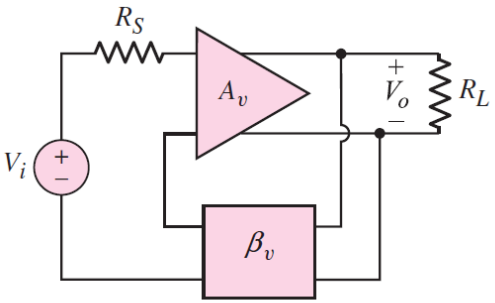
- Whereas the open-loop gain changes by a factor of 2, the closed loop gain changes by only 1% and 2%
- A smaller change in gain means **less distortion**

Basic Feedback Circuit Connection

There are four basic feedback topologies, based on the parameter to be amplified (voltage or current) and the output parameter (voltage or current).

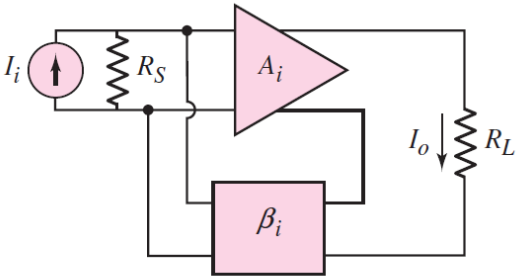
These topologies are distinguished by the types of feedback connections at the input and output of circuits, respectively:

Voltage amplifier:



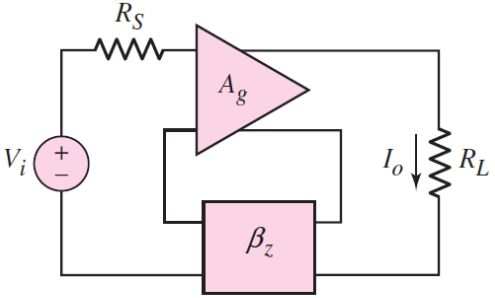
(a) Series–shunt

Current amplifier:



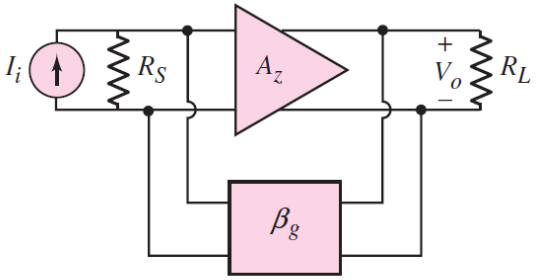
(b) Shunt–series

Transconductance amplifier:



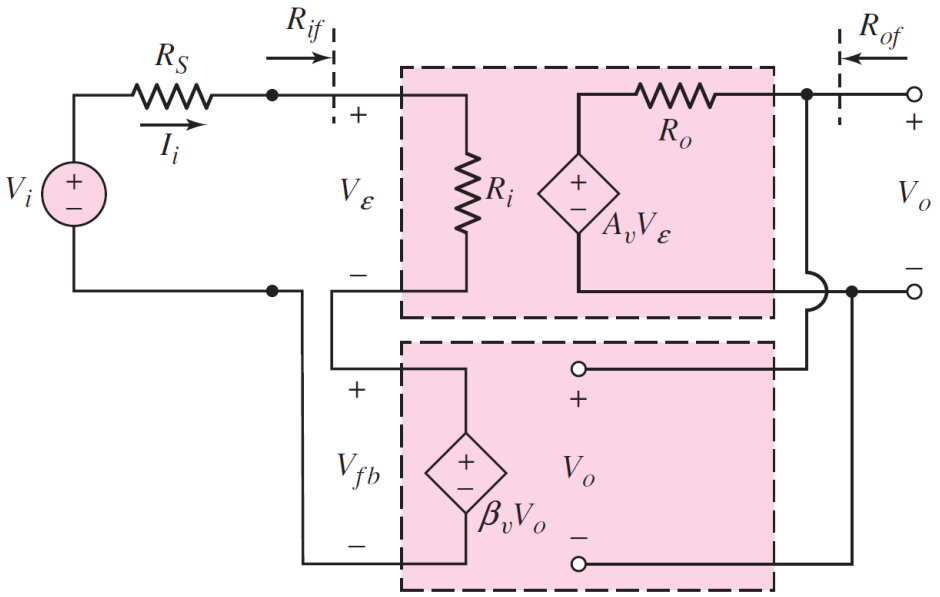
(c) Series–series

Transresistance amplifier:



(d) Shunt–shunt

Series-Shunt Configuration (voltage amplifier):



- The circuit consists of a basic voltage amplifier with an input resistance R_i and open-loop voltage gain A_v;
- The feedback circuit samples the output voltage and produces a feedback voltage V_{fb}, which is in series with the input voltage V_i;
- The error signal voltage $V_\varepsilon = V_i - V_{fb}$ is amplified in the basic voltage amplifier (negative feedback loop).

Let us analyze the circuit using electric laws (i.e., KVL):

1. If the output voltage is: $V_o = A_v V_\varepsilon$

2. The feedback voltage is: $V_{fb} = \beta_v V_o$

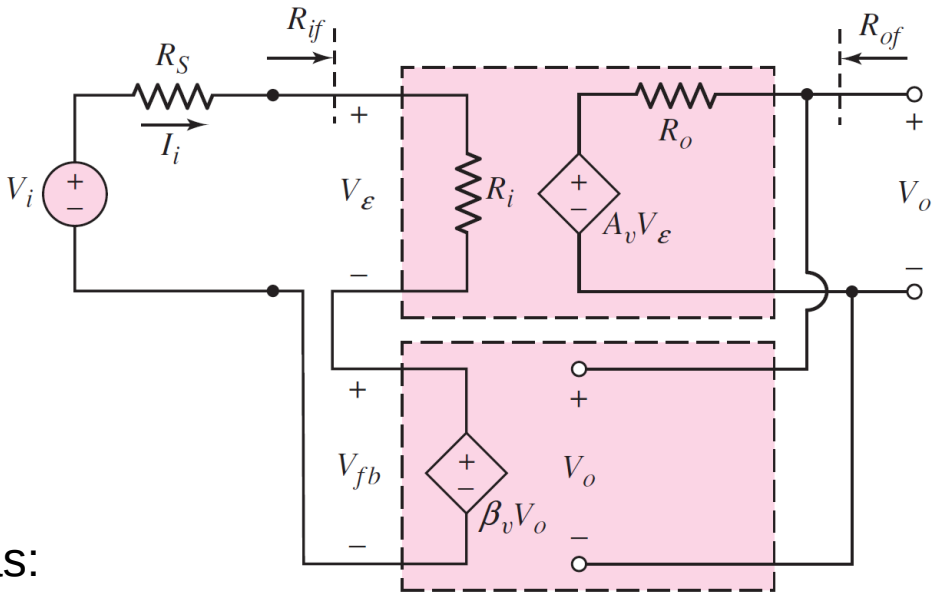
3. The voltage transfer function is then: $$A_{vf} = \frac{V_o}{V_i} = \frac{A_v V_\varepsilon}{V_\varepsilon + V_{fb}} = \frac{A_v}{1 + \beta_v A_v}$$

Series-Shunt Configuration (voltage amplifier):

Input resistance (R_{if})

1. Applying KVL to the input loop:

$$V_i = V_\varepsilon + V_{fb} = V_\varepsilon + \beta_v V_o = V_\varepsilon(1 + \beta_v A_v)$$



2. Finding V_ε will give:

$$V_\varepsilon = \frac{V_i}{(1 + \beta_v A_v)}$$

3. Now the input current can be found as:

$$I_i = \frac{V_\varepsilon}{R_i} = \frac{V_i}{R_i(1 + \beta_v A_v)}$$

4. The effective **input resistance** of the series input connection is:

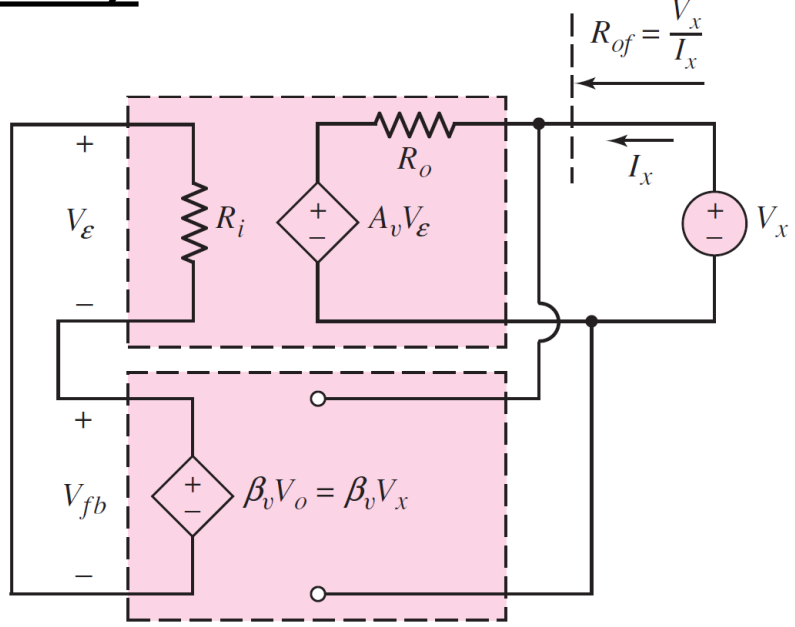
$$R_{if} = \frac{V_i}{I_i} = R_i(1 + \beta_v A_v)$$

A large input resistance is a desirable property of a voltage amplifier. This eliminates loading effects on the input signal source.

Series-Shunt Configuration (voltage amplifier):

Output resistance (R_{of})

0. Short-circuit input and apply test voltage to the output;



1. Applying KVL to the input loop:

$$V_\varepsilon = -\beta_v V_x$$

2. From the output loop, the output current can be found as:

$$I_x = \frac{V_x - A_v V_\varepsilon}{R_o} = \frac{V_x(1 + \beta_v A_v)}{R_o}$$

3. The effective **output resistance** of the shunt output connection is:

$$R_{of} = \frac{V_x}{I_x} = \frac{R_o}{(1 + \beta_v A_v)}$$

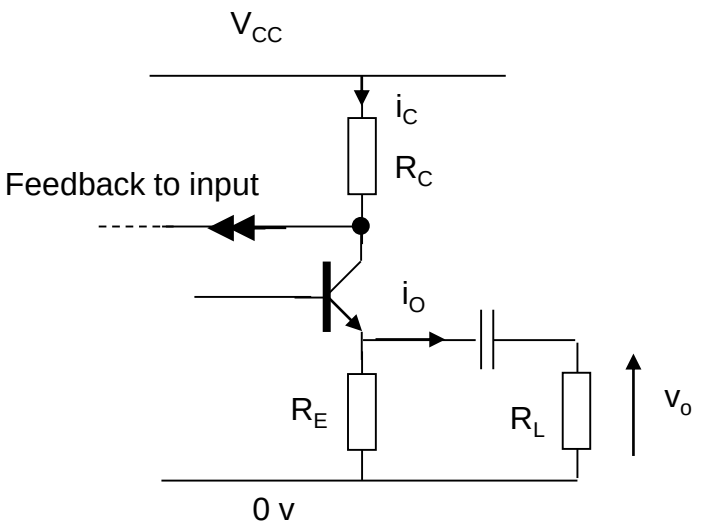
A small output resistance is a desirable property of a voltage amplifier. This eliminates loading effects on the output signal when an output load is connected.

Methods for identifying feedback connections

Input side:

Method 1: If the feedback affects input signal in terms of voltage, it is voltage application (series applied); otherwise, if the feedback affects input signal in terms of current it is current application (shunt applied)

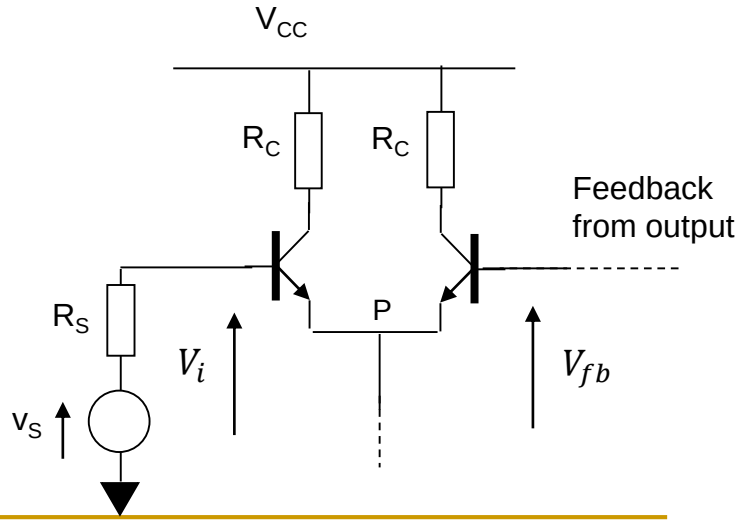
Method 2: if the feedback loop is connected to the same input terminal as the signal source, it is current application (shunt applied); otherwise, it is voltage application (series applied) ***(Recommended)***



Output side:

Method 1: Short-circuit the output voltage/load, if the feedback signal disappears, it is voltage sensing (shunt derived); otherwise, it is current sensing (series derived) ***(Recommended)***

Method 2: If the feedback is directly connected to the output terminal (positive side), it is voltage sensing (shunt derived); otherwise, it is current sensing (series derived) ***(More convenient but prone to mistake)***



Part 4:
Frequency Response and Stability of Amplifier Circuits with Feedback

- Reading material:
  - Microelectronics: Circuit Analysis and Design, Chapter 12:
    - Sec. 12.9 – Stability of the feedback circuit
    - Sec. 12.10 – Frequency compensation
- Practice exercises:
  - Microelectronics: Circuit Analysis and Design, Chapter 12:
    - Ex. 12.18-12.22
    - TYU 12.15-12.17

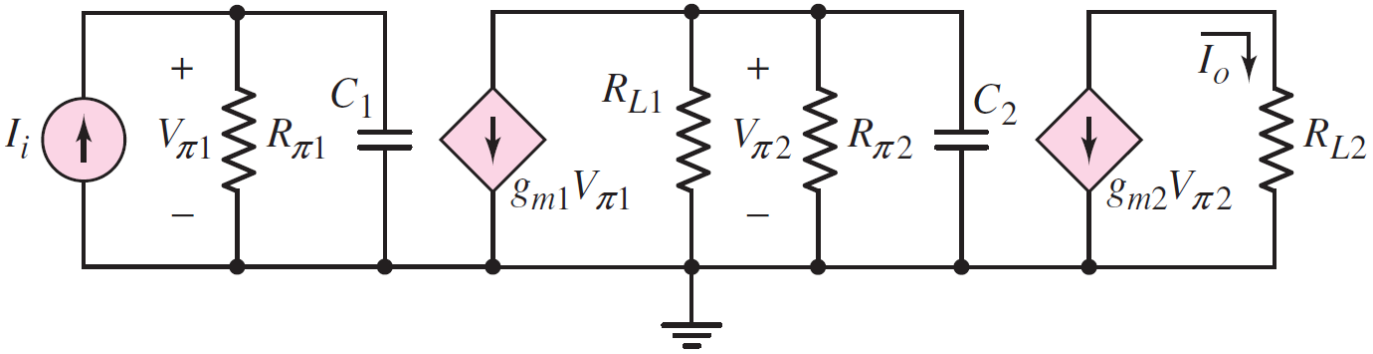
Frequency response analysis (overview)

The circuit frequency response is usually (analytically) determined by using the **complex frequency s**:

1. Each capacitor is represented by its complex impedance $1/sC$, and each inductor is represented by sL. For amplifiers, we only consider **the effect of capacitors** due to Miller effect;
2. Based on the complex impedances, we determine the **system gain (transfer function as a product of polynomials)**;
3. Once a transfer function is found, we set $s = j\omega = j2\pi f$. The system transfer function then reduces to a **complex function of frequency**;
4. The complex function of frequency can be reduced to **a magnitude and a phase**;
5. Finally, we can use analytical tools such as **Bode plots or Nyquist diagram** to analyze the system frequency response.

Two-stage (pole) amplifier: transfer function

For the two-stage amplifier (i.e., common-emitter):



Let us find the current gain of the amplifier ($A_i = I_o/I_i$):

1. The output current is found as:

$$I_o = -g_{m2}V_{\pi 2},$$

where

$$V_{\pi 2} = -g_{m1}V_{\pi 1}\left(R_{L1}||R_{\pi 2}||\frac{1}{sC_2}\right) \text{ and } V_{\pi 1} = I_i\left(R_{\pi 1}||\frac{1}{sC_1}\right)$$

2. The resulting current gain expression will be:

$$A_i = \frac{I_o}{I_i} = (g_{m1}g_{m2})(R_{\pi 1})(R_{L1}||R_{L2})\left[\frac{1}{1+sR_{\pi 1}C_1}\right]\left[\frac{1}{1+s(R_{L1}||R_{\pi 2})C_2}\right]$$

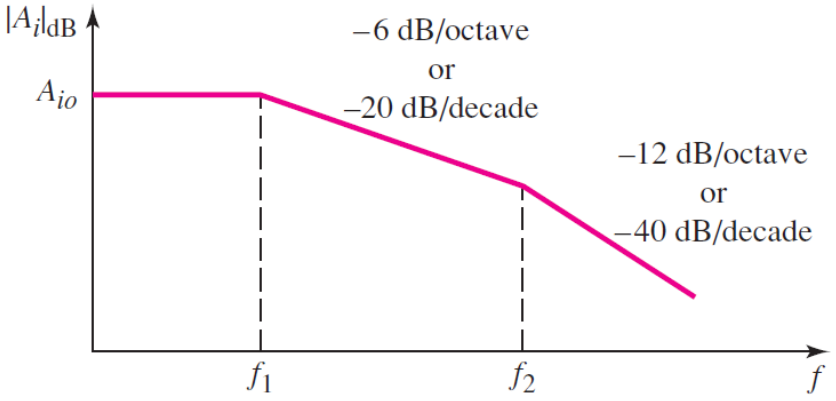
Two-stage (pole) amplifier: Bode plots

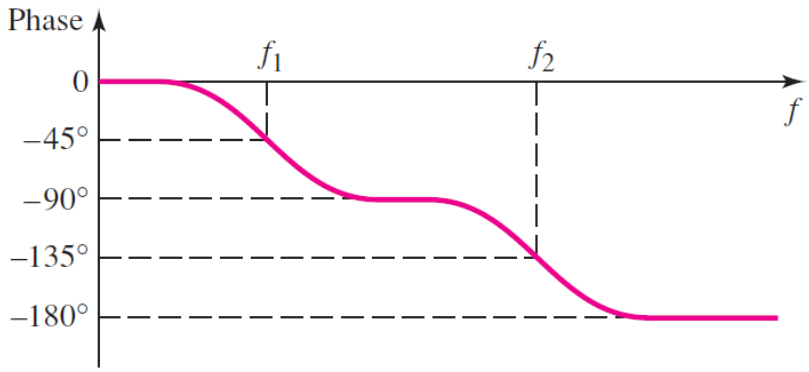
3. Setting $s = j(2\pi f)$, (2.) can be rewritten to the form: $A_i(f) = \dfrac{A_{io}}{\left(1 + j\dfrac{f}{f_1}\right)\left(1 + j\dfrac{f}{f_2}\right)}$

where $f_1 = 1/2\pi R_{\pi 1} C_1$ and $f_2 = 1/2\pi (R_{L1} || R_{\pi 2}) C_2$ are the corner frequencies of the first and the second pole.

4. Finally, represent the complex function in the form of its absolute value and phase (i.e., polar form), and draw the corresponding Bode plots:

$$A_i = \frac{A_{io}}{\sqrt{1 + (f/f_1)^2}\sqrt{1 + (f/f_1)^2}} \angle - \left[\tan^{-1}\left(\frac{f}{f_1}\right) + \tan^{-1}\left(\frac{f}{f_2}\right)\right]$$

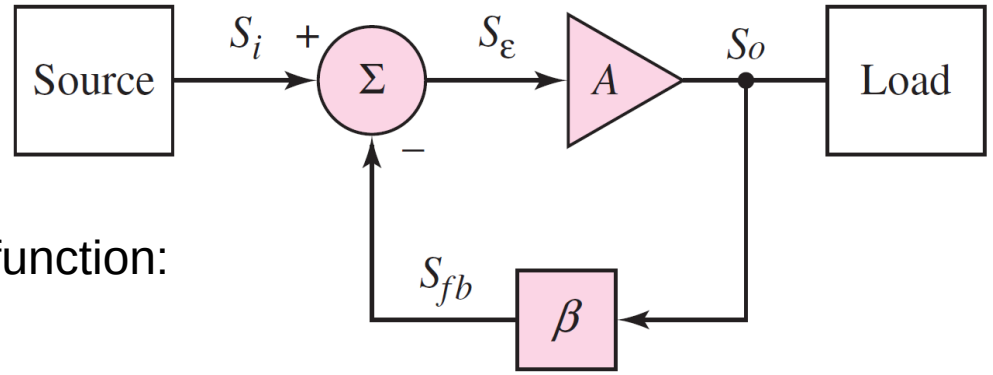




The output current is in phase with the input current at low frequency. At high frequencies, the output current becomes 180 degrees out of phase with respect to the input current.

The Stability Problem

At some frequencies, the subtraction may become addition – the negative feedback becomes positive, resulting in instability.



Recall, the ideal closed-loop transfer function:

$$A_f = \frac{S_o}{S_i} = \frac{A}{1 + \beta A}$$

In practice, the open-loop gain is a function of the individual transistor parameters, including capacitance; therefore, it is also a function of frequency:

$$A_f(s) = \frac{A(s)}{1 + \beta A(s)} = \frac{A(s)}{1 + T(s)},$$

where $T(s) = \beta \mathrm{A}(s)$ is the loop gain and $s = j\omega$ is the complex frequency.

Now, the closed-loop gain function can be presented as:

$$A_f(j\omega) = \frac{A(j\omega)}{1 + |T(j\omega)|\angle\phi}$$

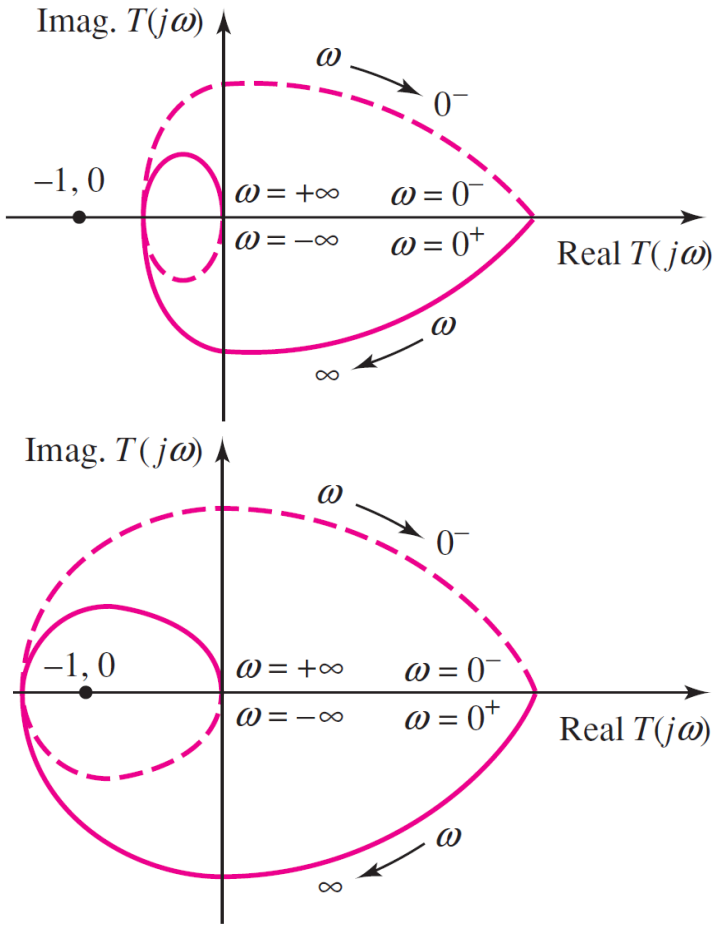
What will happen to the closed-loop gain if $|T(j\omega)| = 1$ and $\phi = 180°$?: $A_f \to \infty$

To study the stability of feedback circuits, we must analyze the frequency response of the loop gain factor $T(j\omega)$.

Nyquist Stability Criterion

Test for stability (without a need to draw Nyquist plot):

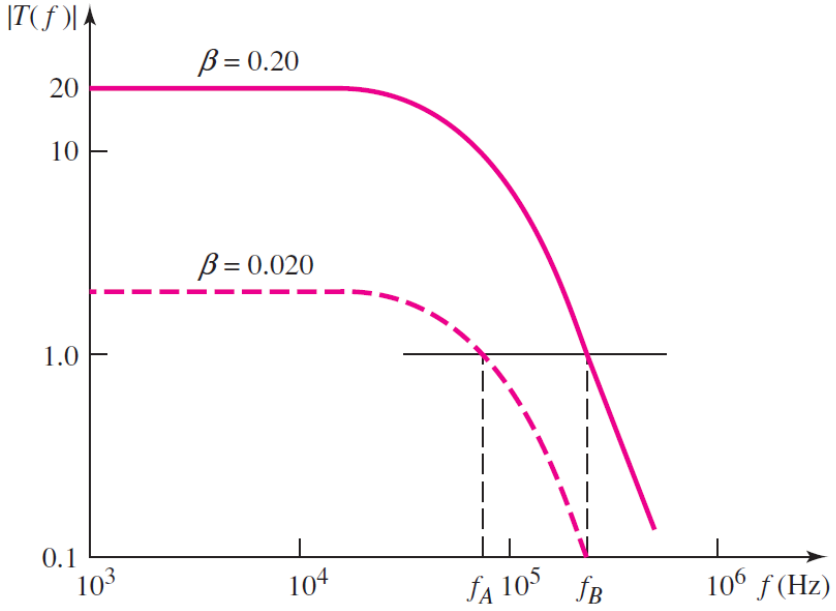
- If $|T(j\omega)| \geq 1$ at the frequency at which the phase is −180 degrees, then the amplifier is unstable.

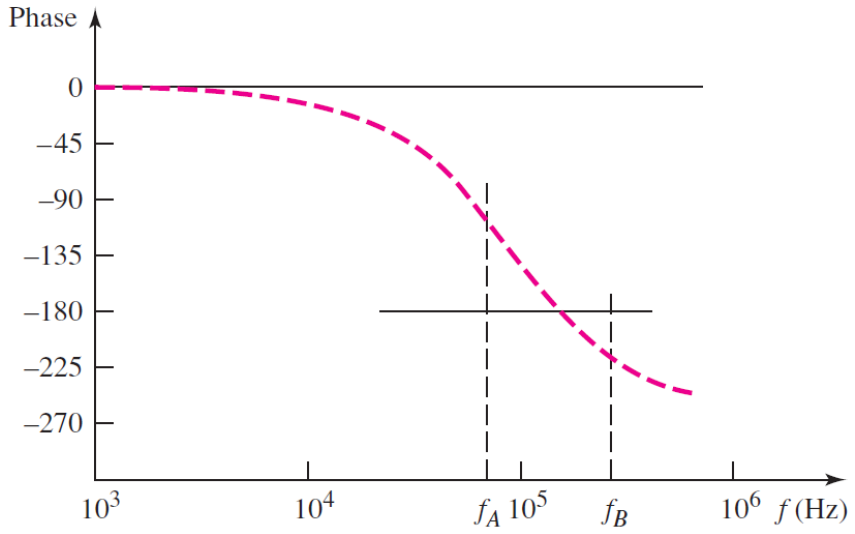


This simple test allows us to use the Bode plots (considered previously), instead of explicitly constructing the Nyquist diagram.

Bode plot stability analysis

Effectively, Bode plots represent the same data as a Nyquist plot, but in a different way; therefore, it can also be used for stability analysis.
Consider the Bode plots of the loop gain from the previous Exercise:

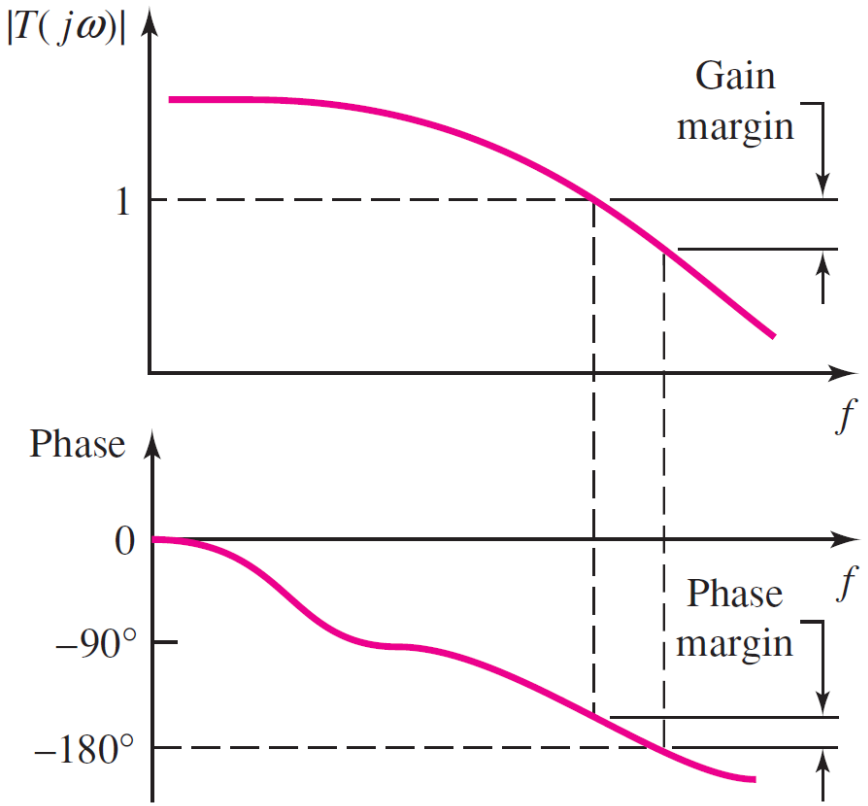




- For $\beta = 0.02$, we see that $|\phi| < 180$ at the frequency when $|T(f)| = 1$ – stable;
- For $\beta = 0.2$, we see that $|\phi| > 180$ at the frequency when $|T(f)| = 1$ – unstable;

Phase and Gain (Stability) Margins

Using Bode plots or Nyquist diagram we can also determine the degree of stability of a feedback amplifier:



So far we know:
If $|\phi(f)| < 180$ when $|T(f)| = 1$ the system is stable. In this case, the stability margin is determined by:

- **Phase margin**: the difference between the phase angle at $f_{|T(f)|=1}$ and -180 degrees:

$$PM = \phi_{|T(f)|=1} - (-180)$$

- **Gain margin:** the difference between the gain magnitude at -180 degrees and one (typically in dB) :

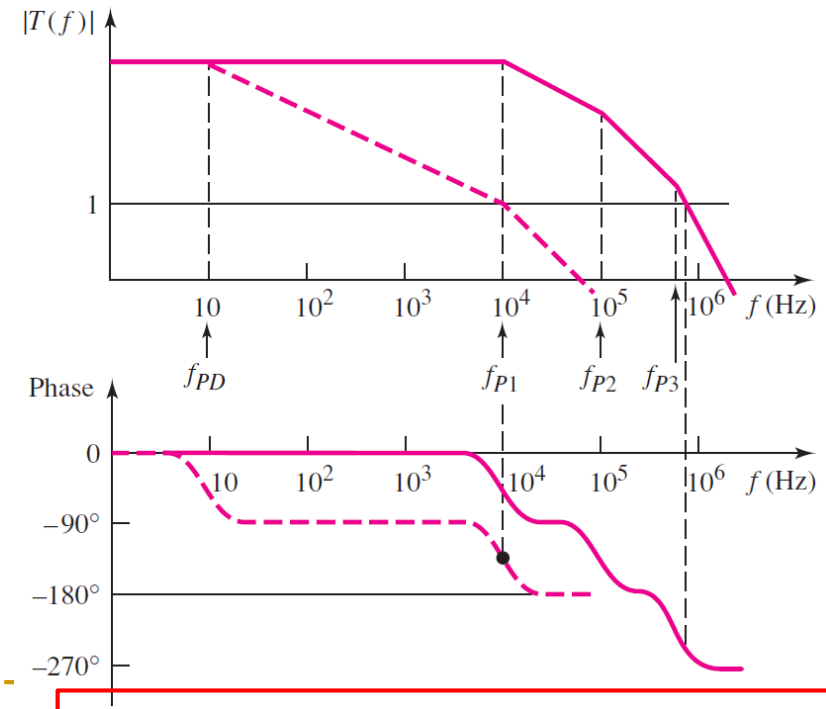
$$GM = -20\log|T(f_{180})|$$

The phase margin indicates how much the loop gain can increase and still maintain stability. A typical desired phase margin is in the range of 45 to 60°

Frequency compensation with dominant pole

The simplest method to stabilize a system is to introduce a new pole in the loop gain function for which the loop gain $|T(f)| = 1$ occurs when $|\phi| < 180°$.

Consider the Bode plots of a three-pole loop gain magnitude and phase:



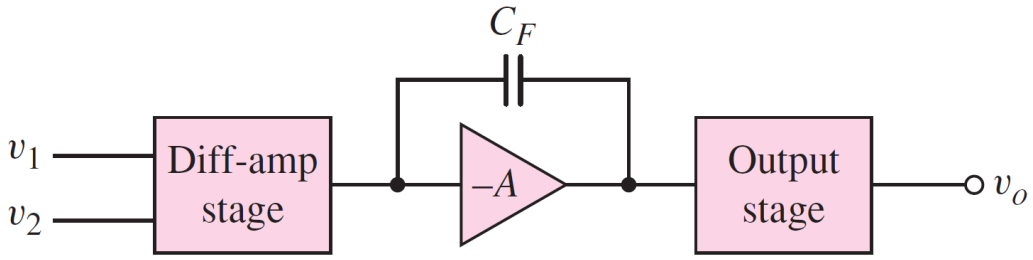
- Original system frequency response is represented by the solid line:
  - The magnitude of the loop gain $|T(f)| = 1$ when $\phi \approx -270°$
    – **the system is unstable.**
- After the introduction of a new pole with a very low corner frequency f_{PD} the new frequency response will be shifted left as shown by dashed line:
  - The magnitude of the loop gain $|T(f)| = 1$ when $|\phi| < 180°$
    – the system is stable.

Since the pole is introduced at a low frequency and since it dominates the frequency response, it is called a dominant pole.

Miller compensation

Instead of adding an extra dominant pole to obtain a stable system, Miller compensation implies moving the first pole f_{P1} (whatever stage it belongs to) to a low frequency.

Consider the three-stage amplifier with a **compensation capacitor** in the 2nd stage:



Miller compensation uses Miller effect for a benefit:

- The effective Miller input capacitance to a transistor amplifier is a feedback capacitance multiplied by the magnitude of the gain of the amplifier stage plus one:

$$C_M = C_F(1 + A)$$

- Knowing this, we can adjust the corner frequency as we wish:

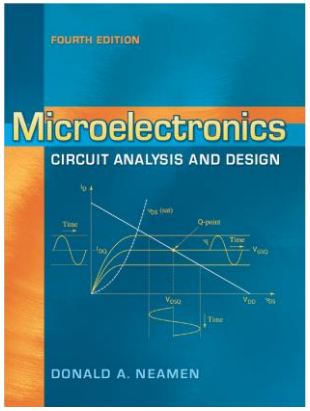
$$f_{P1} = \frac{1}{2\pi R_2 C_M},$$

where R_2 is the effective resistance between the amplifier input node and the ground ($R_2 = R_{1o}||R_{2i}$).

Announcements:

- Provide your feedback on Practical Lectures:
  - Please tap here to proceed…

- Reading material and Practice exercises:
  - **Microelectronics: Circuit Analysis and Design** by Donald A. Neamen
  - Reading/Examples to learn, Exercises to practice
  - **Can help you a lot for exam preparation!**



- My office hours:
  - Regular time: every Thursday in SC465 16:00-18:00

- Module Questionnaire (MQ):
  - Please tap here to proceed…

Thank you for your attention…..

The End