EEE205 – Digital Electronics (II)

Lecture 11

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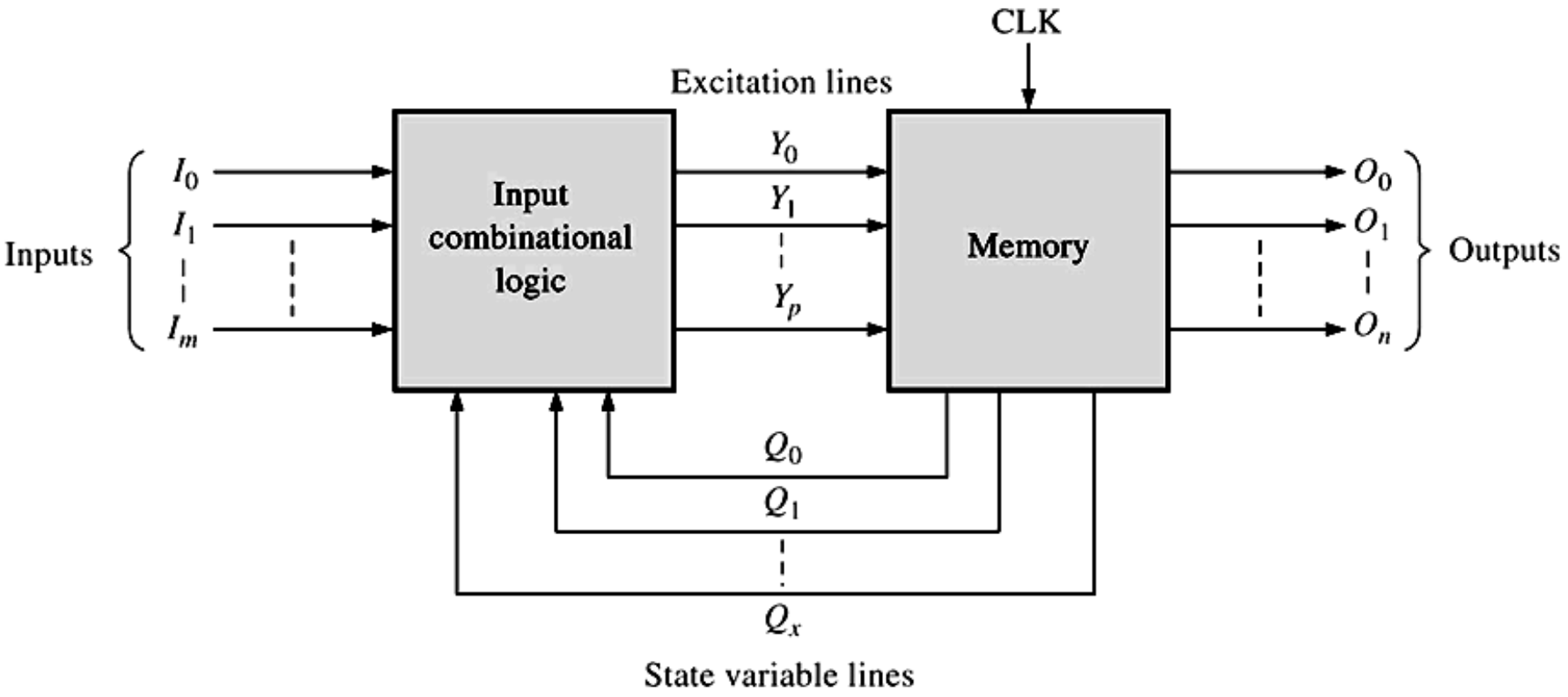
XJTLU

In This Session

- Design of Synchronous Counters

General Model of Sequential Circuits

- A sequential circuit consists of a combinational logic section and a memory section (flip-flops).
- To design a sequential circuit (**state machine**) is to decide the combinational logic.

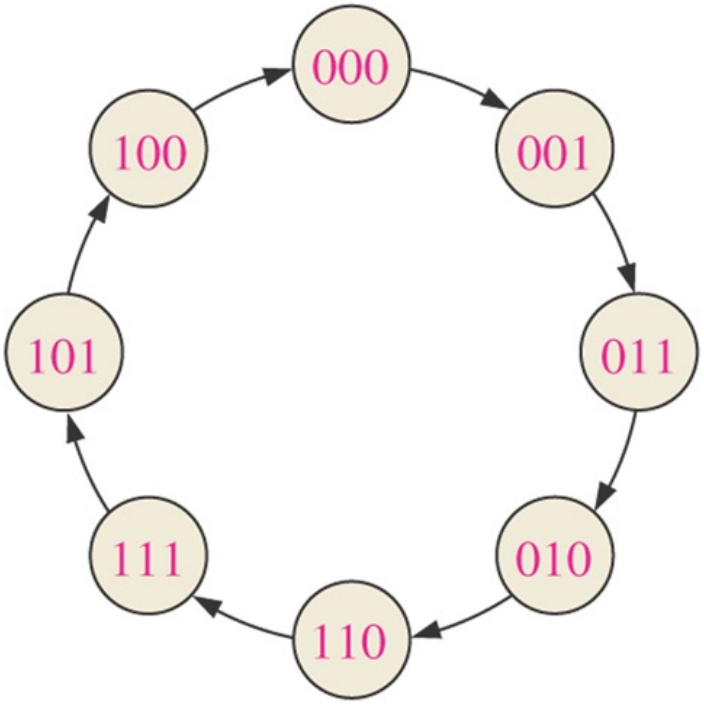


Design of Synchronous Counters

Step 1: State Diagram

- A **state diagram** shows the progression of states when the counter is clocked.

Example: a 3-bit **Gray code counter**, which exhibits only a single bit change from one code number to the next.



Design of Synchronous Counters

Step 2: Next-State Table

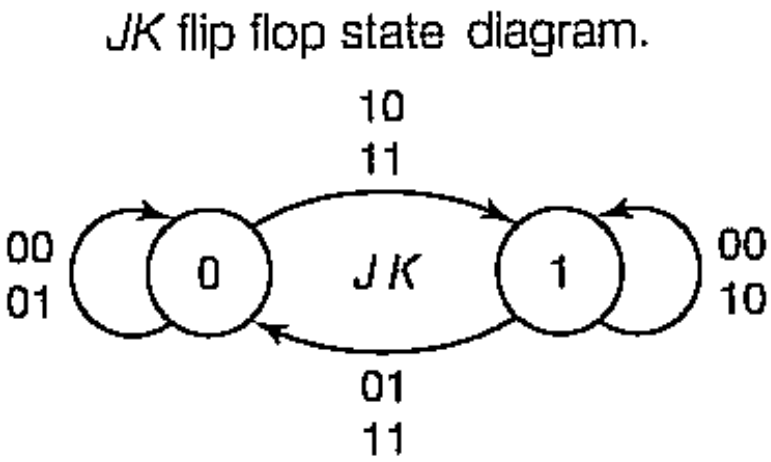
- A **next-state table** lists the present state along with the corresponding next state of the counter.

Present State			Next State		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	0	0	0	1
0	0	1	0	1	1
0	1	1	0	1	0
0	1	0	1	1	0
1	1	0	1	1	1
1	1	1	1	0	1
1	0	1	1	0	0
1	0	0	0	0	0

Design of Synchronous Counters

Step 3: Flip-Flop Transition Table

- A transition table lists all possible output transitions and the corresponding inputs.

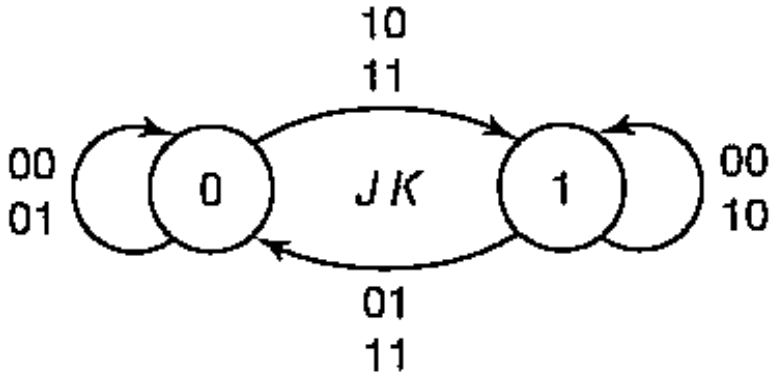


Output Transitions Q_N		Q_{N+1}	Flip-Flop Inputs J	K
0	⟶	0	0	X
0	⟶	1	1	X
1	⟶	0	X	1
1	⟶	1	X	0

Design of Synchronous Counters

More flip-flop transition tables (q* for next states)

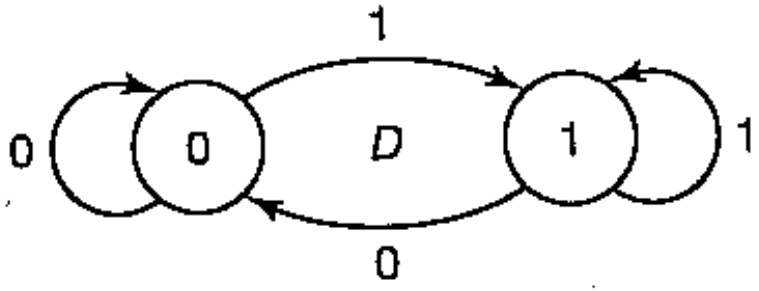
JK flip flop state diagram.



JK flip flop design table.

q	q^*	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

D flip flop state diagram



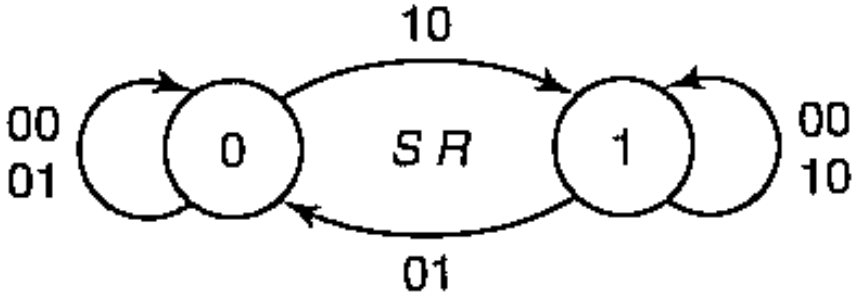
D flip flop design table.

q	q^*	D
0	0	0
0	1	1
1	0	0
1	1	1

Design of Synchronous Counters

More flip-flop transition tables (q* for next states)

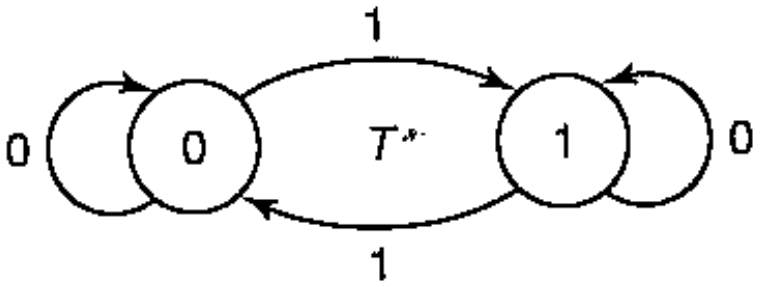
SR flip flop state diagram



SR flip flop design table

q	*q**	*S*	*R*
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

T flip flop state diagram



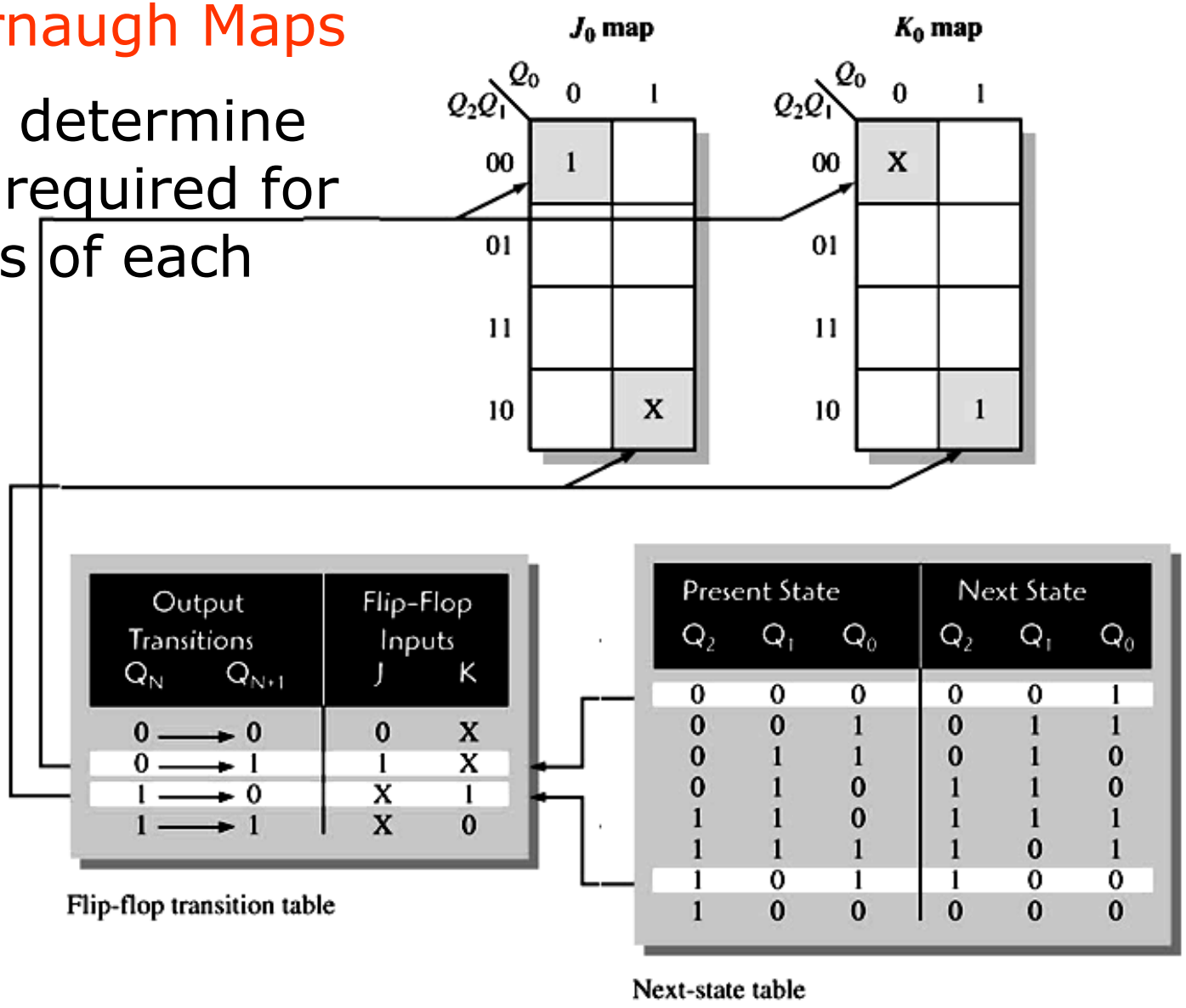
T flip flop design table

q	*q**	*T*
0	0	0
0	1	1
1	0	1
1	1	0

Design of Synchronous Counters

Step 4: Karnaugh Maps

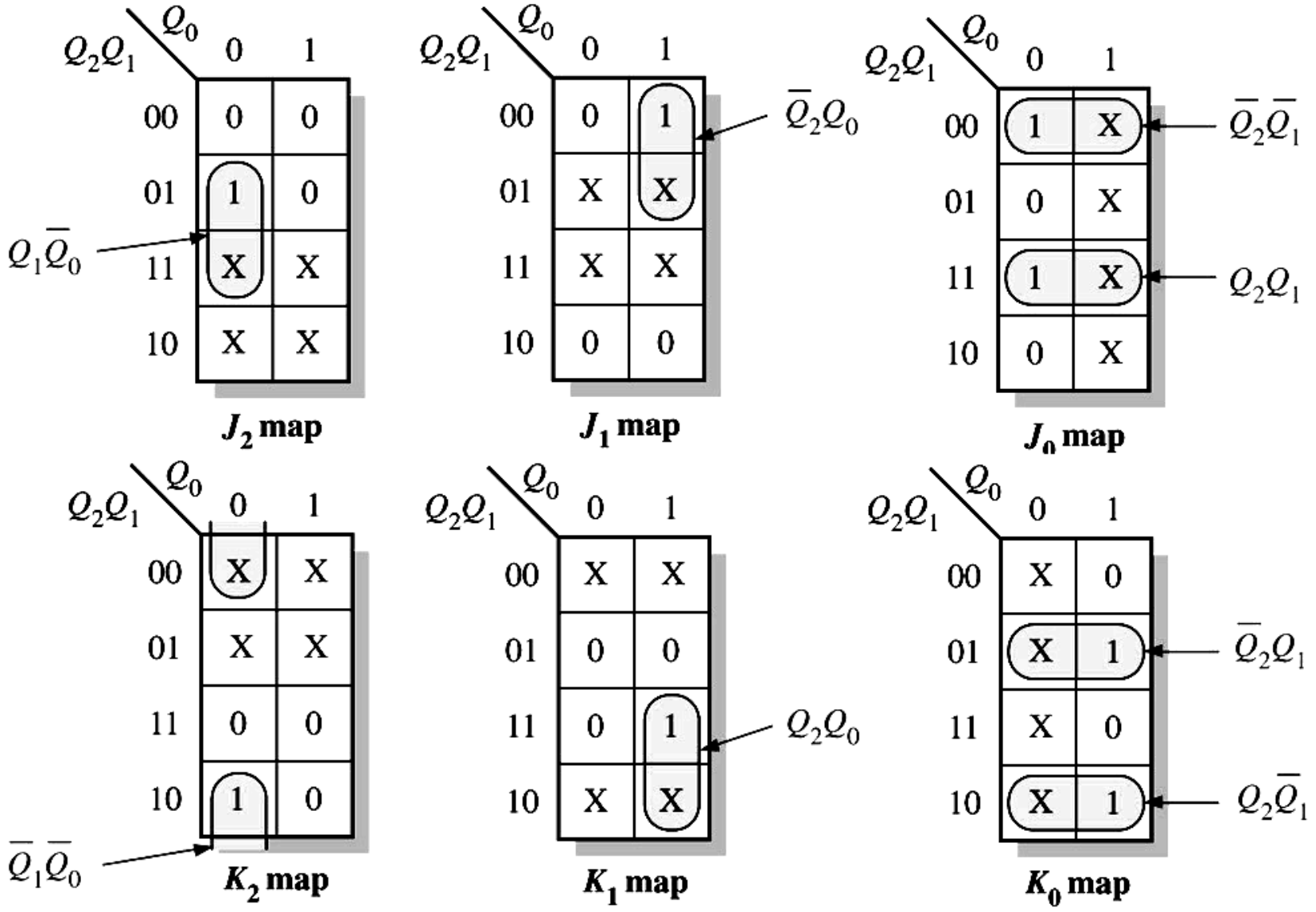
- This is to determine the logic required for the inputs of each flip-flop.



Flip-flop transition table

Next-state table

Design of Synchronous Counters



Design of Synchronous Counters

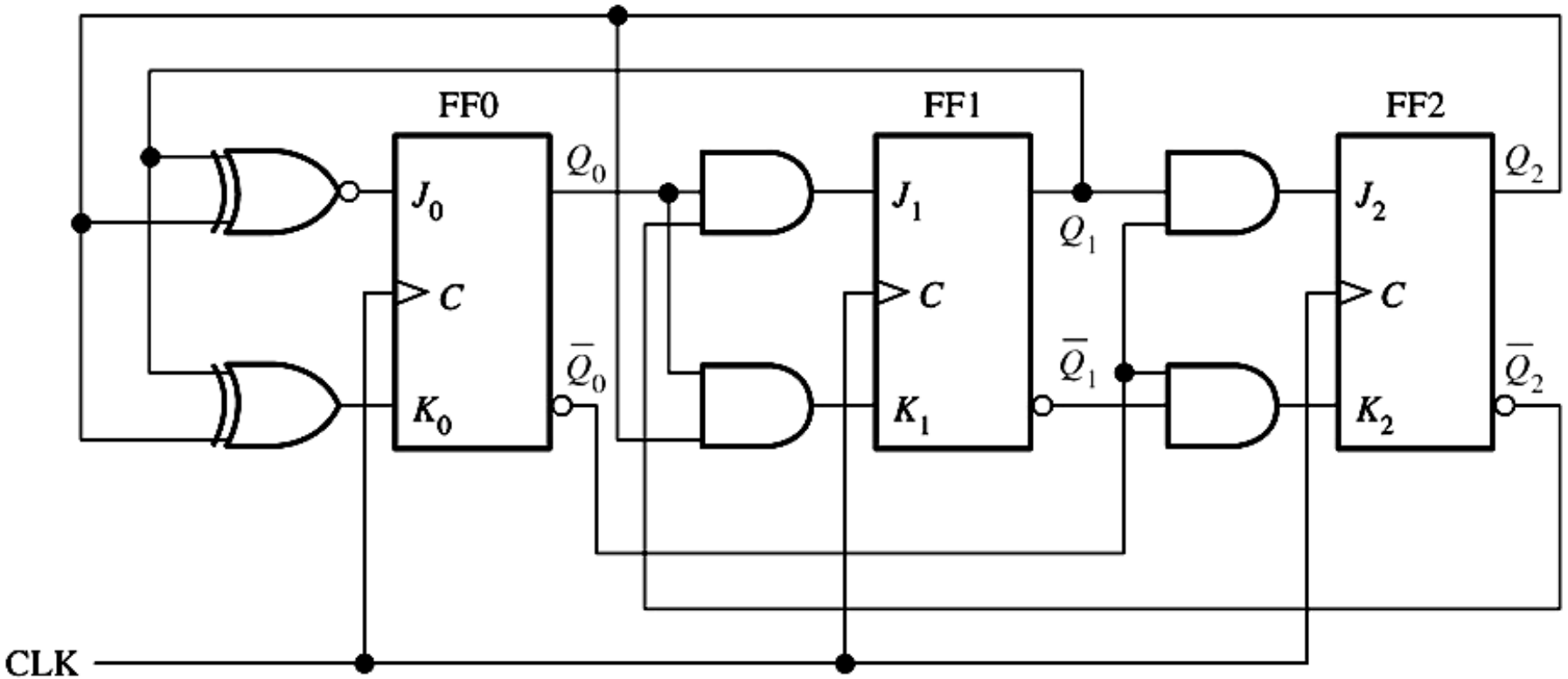
Step 5: Logic Expressions for Flip-Flop Inputs

$$J_0 = Q_2Q_1 + \overline{Q}_2\overline{Q}_1 = \overline{Q_2 \oplus Q_1}$$
$$K_0 = Q_2\overline{Q}_1 + \overline{Q}_2Q_1 = Q_2 \oplus Q_1$$
$$J_1 = \overline{Q}_2Q_0$$
$$K_1 = Q_2Q_0$$
$$J_2 = Q_1\overline{Q}_0$$
$$K_2 = \overline{Q}_1\overline{Q}_0$$

Design of Synchronous Counters

Step 6: Counter Implementation

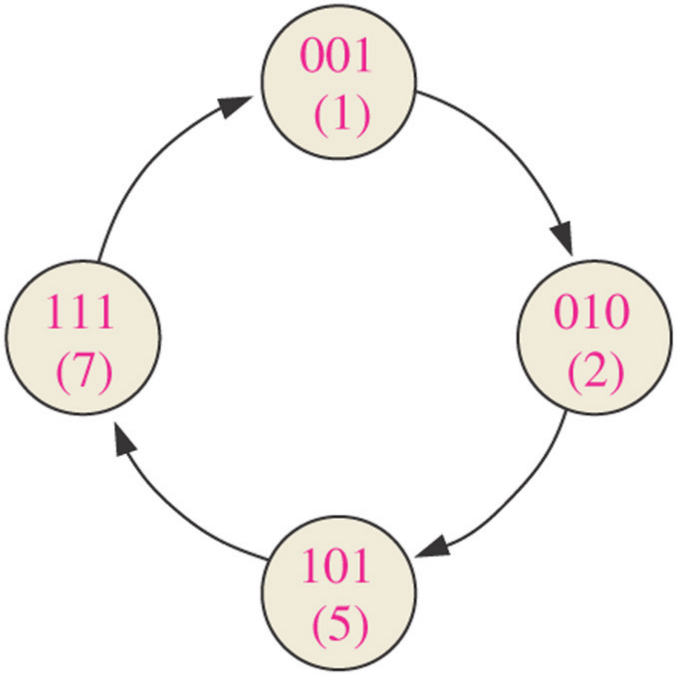
$$J_0 = Q_2Q_1 + \overline{Q}_2\overline{Q}_1 = \overline{Q_2 \oplus Q_1}$$
$$K_0 = Q_2\overline{Q}_1 + \overline{Q}_2Q_1 = Q_2 \oplus Q_1$$
$$J_1 = \overline{Q}_2Q_0$$
$$K_1 = Q_2Q_0$$
$$J_2 = Q_1\overline{Q}_0$$
$$K_2 = \overline{Q}_1\overline{Q}_0$$



Design of Synchronous Counters

Example: Design a counter with **missing states**, as shown in the state diagram. Use J-K flip-flops.

State Diagram

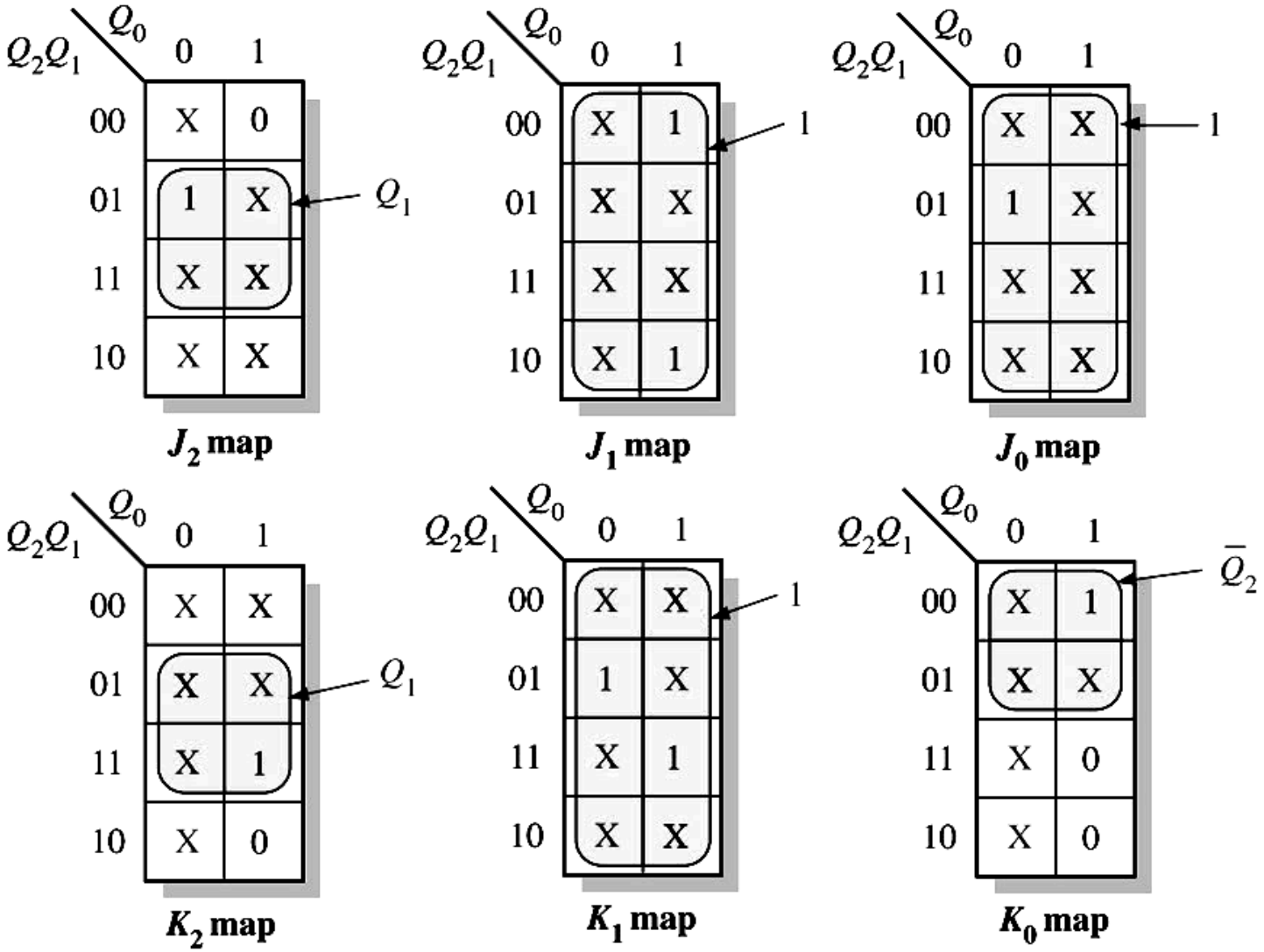


Next-State Table

Present State			Next State		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	1	0	1	0
0	1	0	1	0	1
1	0	1	1	1	1
1	1	1	0	0	1

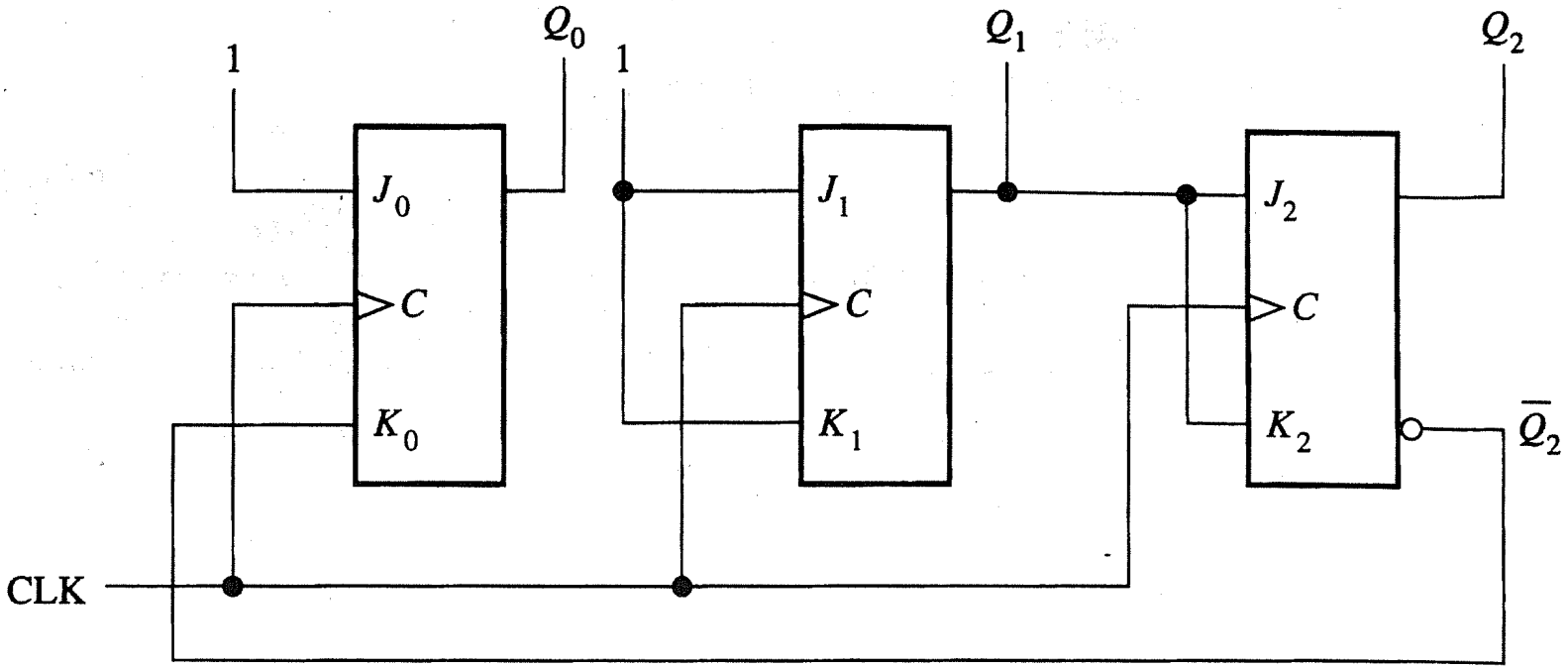
The next state for an invalid state (0, 3, 4 or 6) is "don't care". The J and K inputs are also "don't cares"

Design of Synchronous Counters



Design of Synchronous Counters

$J_0 = 1, K_0 = \overline{Q}_2$
$J_1 = K_1 = 1$
$J_2 = K_2 = Q_1$



Design of Synchronous Counters

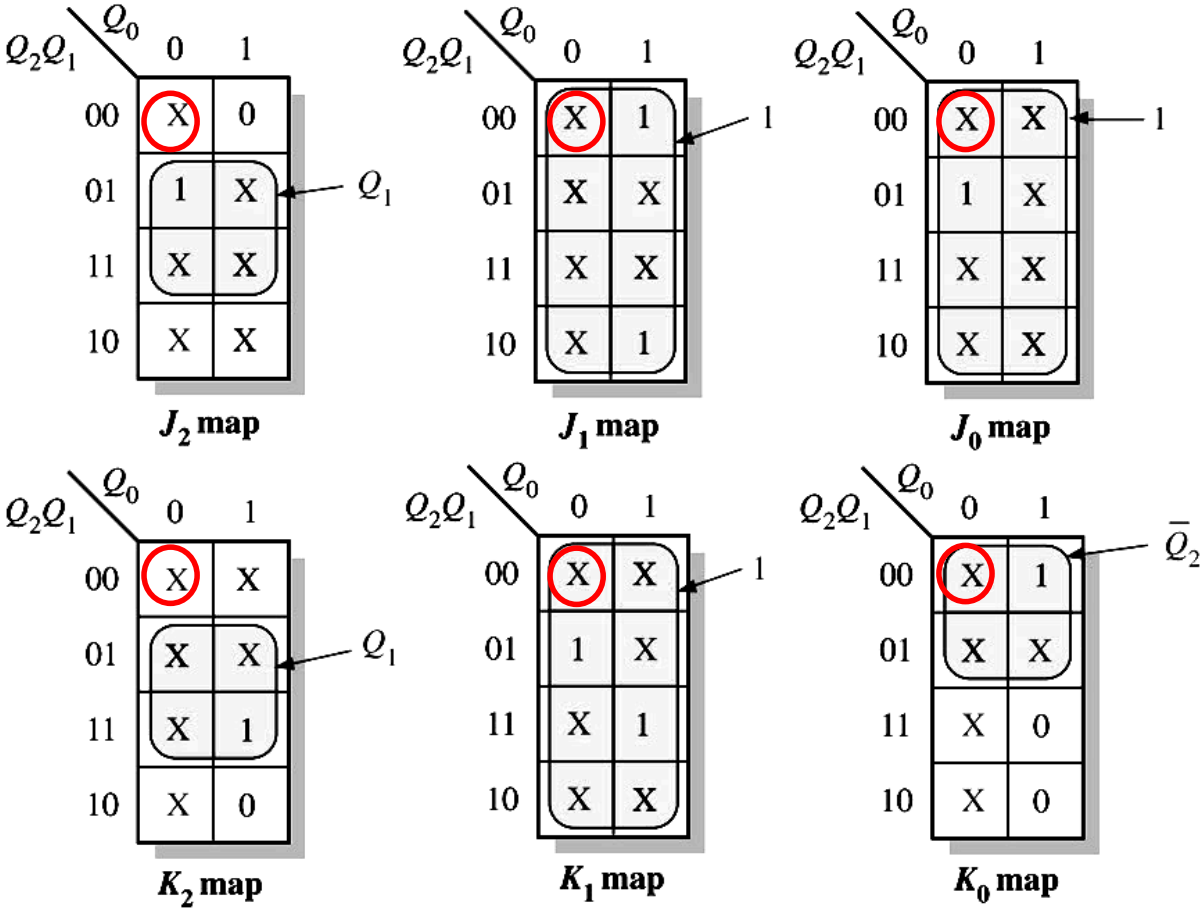
The next state for an invalid state (0, 3, 4 or 6) is originally "don't care" but has a specific value now. From the input equations:

present state									next state		
Q_2	Q_1	Q_0	J_2	K_2	J_1	K_1	J_0	K_0	Q_2	Q_1	Q_0
0	0	0	0	0	1	1	1	1	0	1	1
0	1	1	1	1	1	1	1	1	1	0	0
1	0	0	0	0	1	1	1	0	1	1	1
1	1	0	1	1	1	1	1	0	0	0	1

$$J_0 = 1, K_0 = \overline{Q}_2$$
$$J_1 = K_1 = 1$$
$$J_2 = K_2 = Q_1$$

Design of Synchronous Counters

The next state of missing states can also be derived from the K-map:

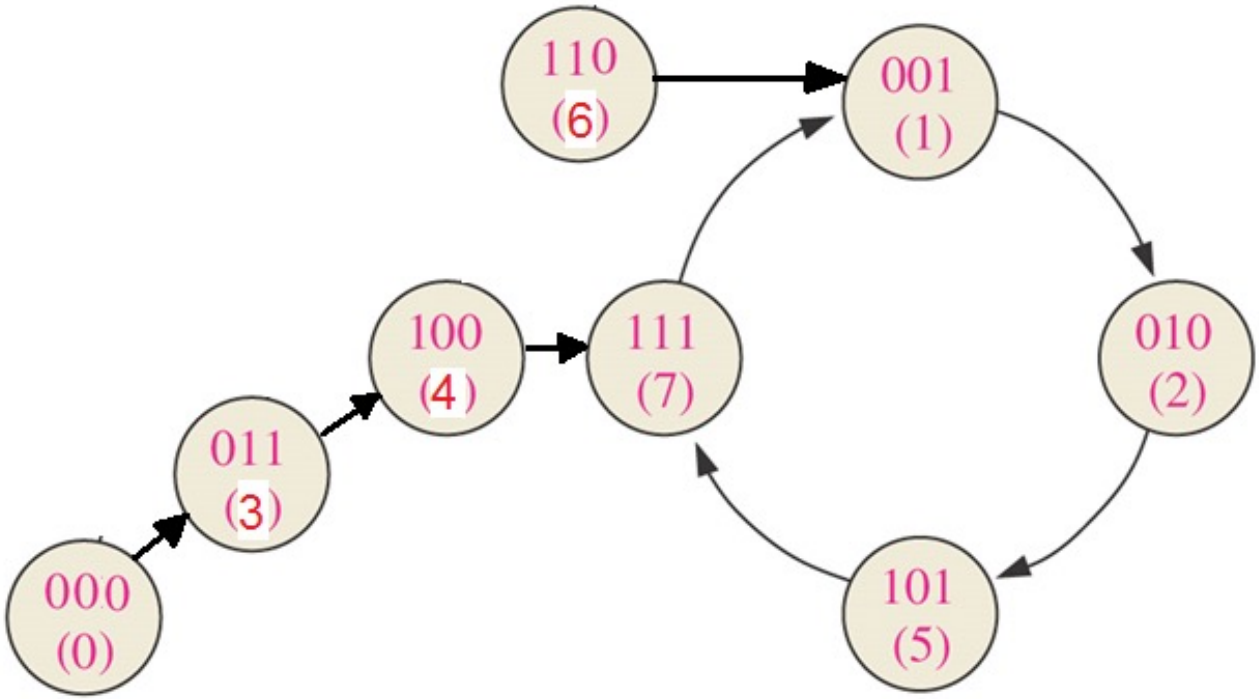


A grouped X is 1;
Otherwise it is 0.

present state
Q2 Q1 Q0
0 0 0
J2 0 K2 0 Q2 0
J1 1 K1 1 Q1 1
J0 1 K0 1 Q0 1

Design of Synchronous Counters

New State Diagram



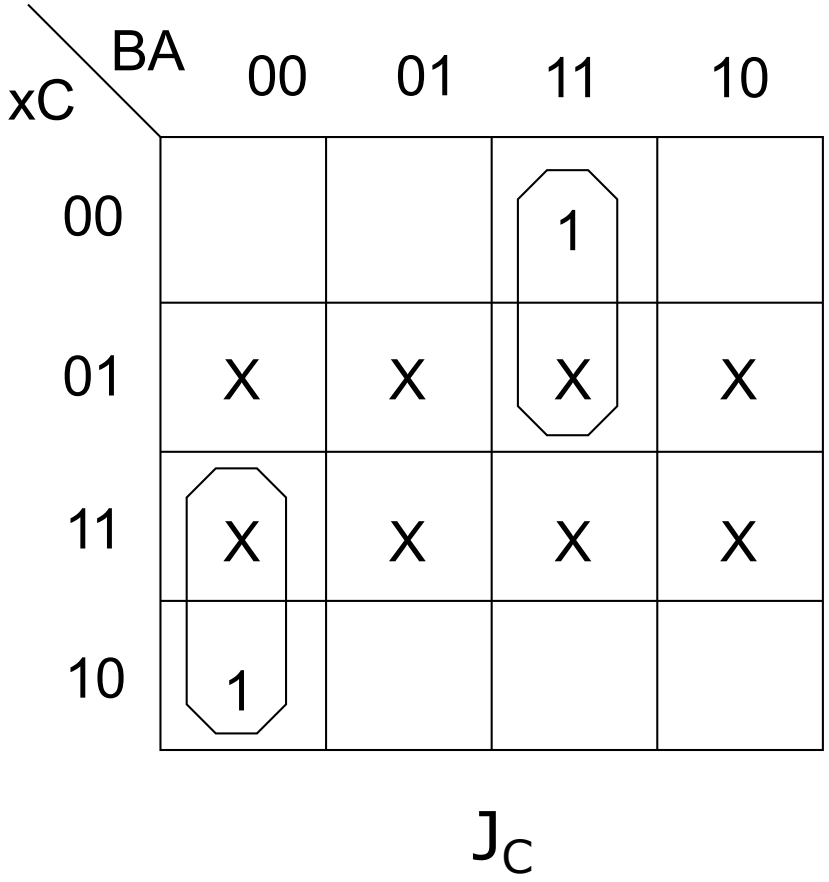
Design of Synchronous Counters

Example: Design a 3-bit up/down counter. Use J-K flip-flops.

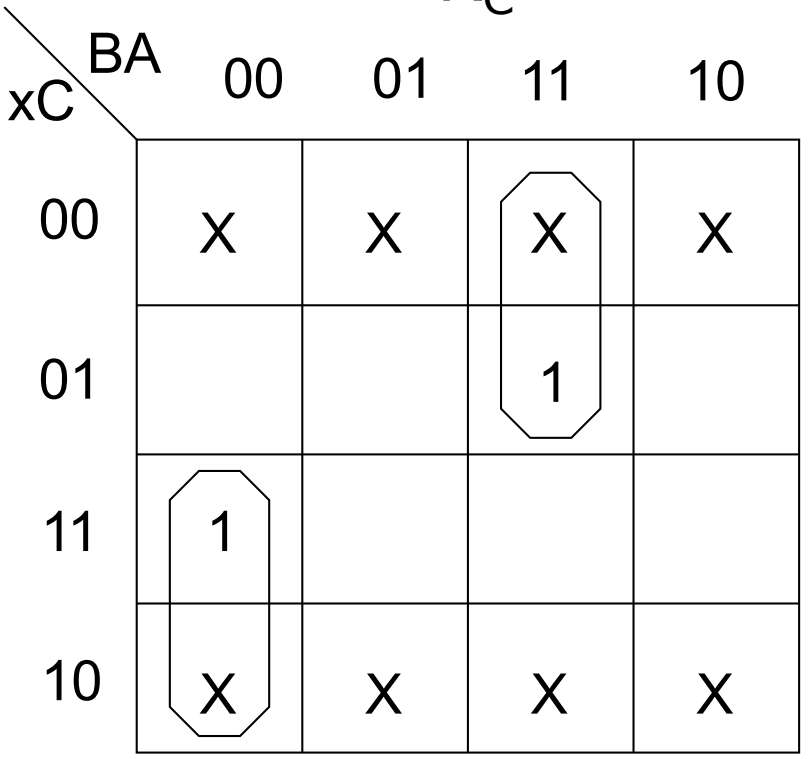
x	C	B	A	C^*	B^*	A^*
0	0	0	0	0	0	1
0	0	0	1	0	1	0
0	0	1	0	0	1	1
0	0	1	1	1	0	0
0	1	0	0	1	0	1
0	1	0	1	1	1	0
0	1	1	0	1	1	1
0	1	1	1	0	0	0
1	0	0	0	1	1	1
1	0	0	1	0	0	0
1	0	1	0	0	0	1
1	0	1	1	0	1	0
1	1	0	0	0	1	1
1	1	0	1	1	0	0
1	1	1	0	1	0	1
1	1	1	1	1	1	0

x is up/down control, 0 for up and 1 for down.

Design of Synchronous Counters

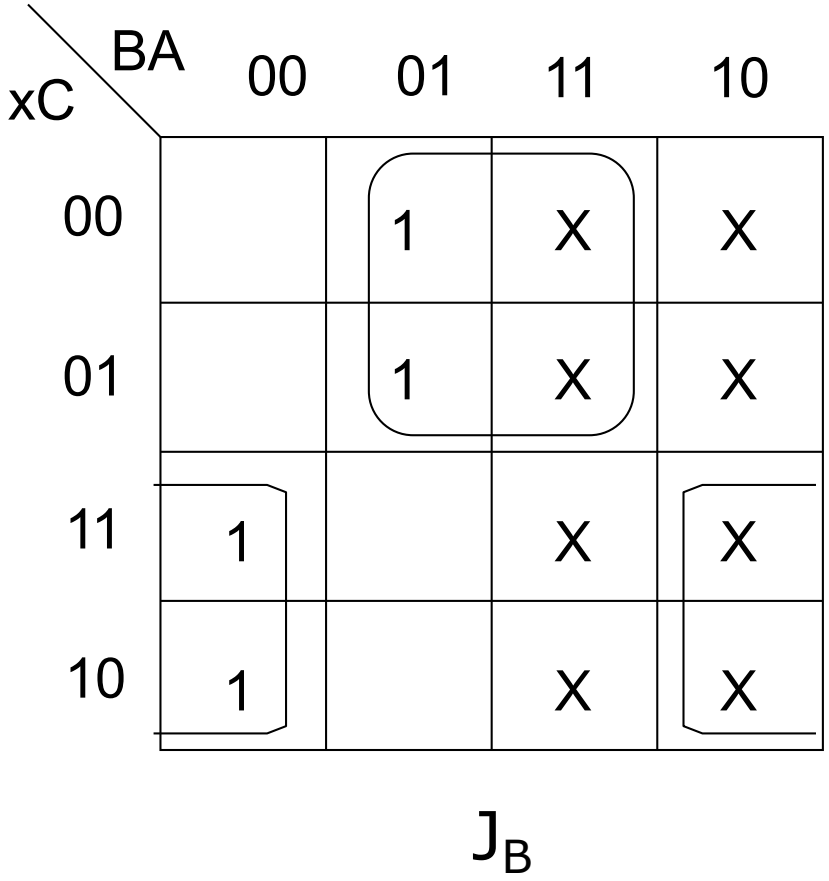


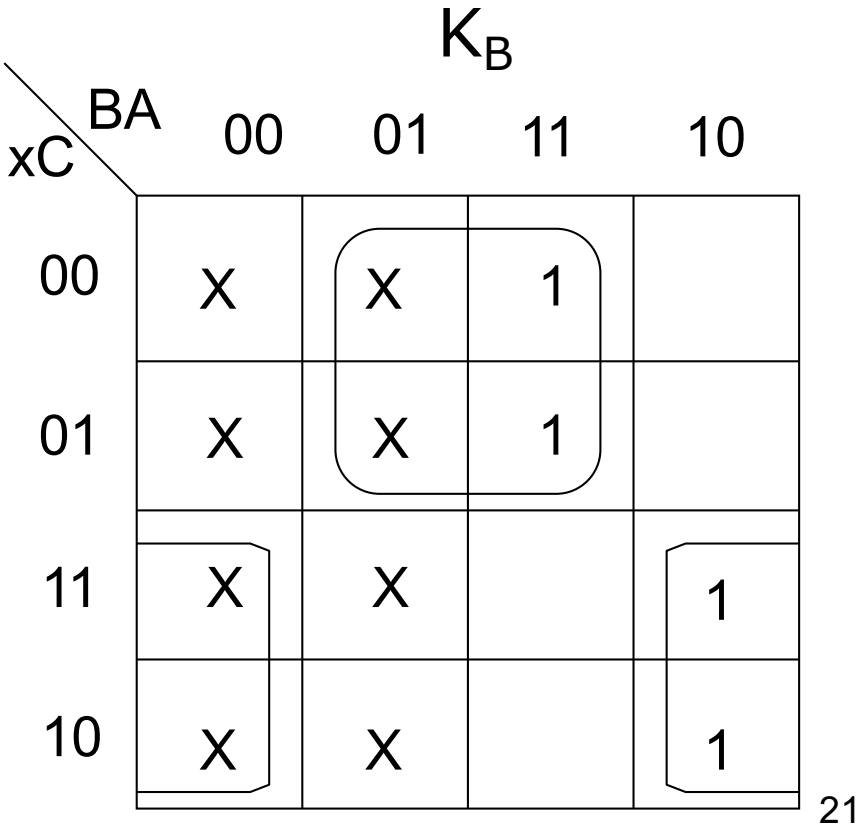
J_C



$$J_C = K_C = x'BA + xB'A'$$

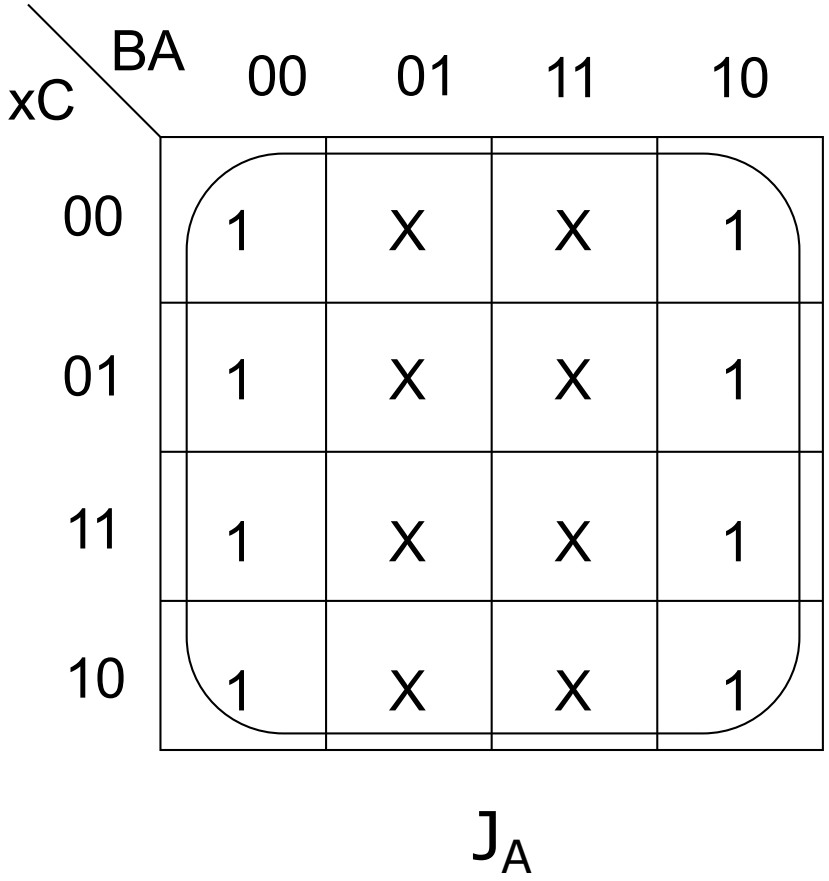
Design of Synchronous Counters



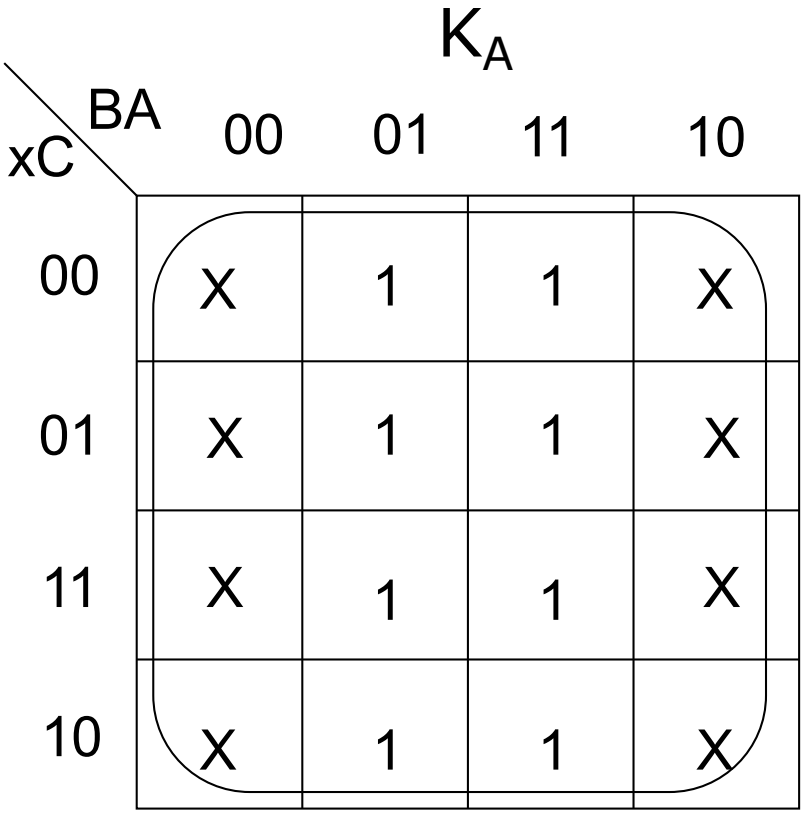


$$J_B = K_B = x'A + xA'$$

Design of Synchronous Counters



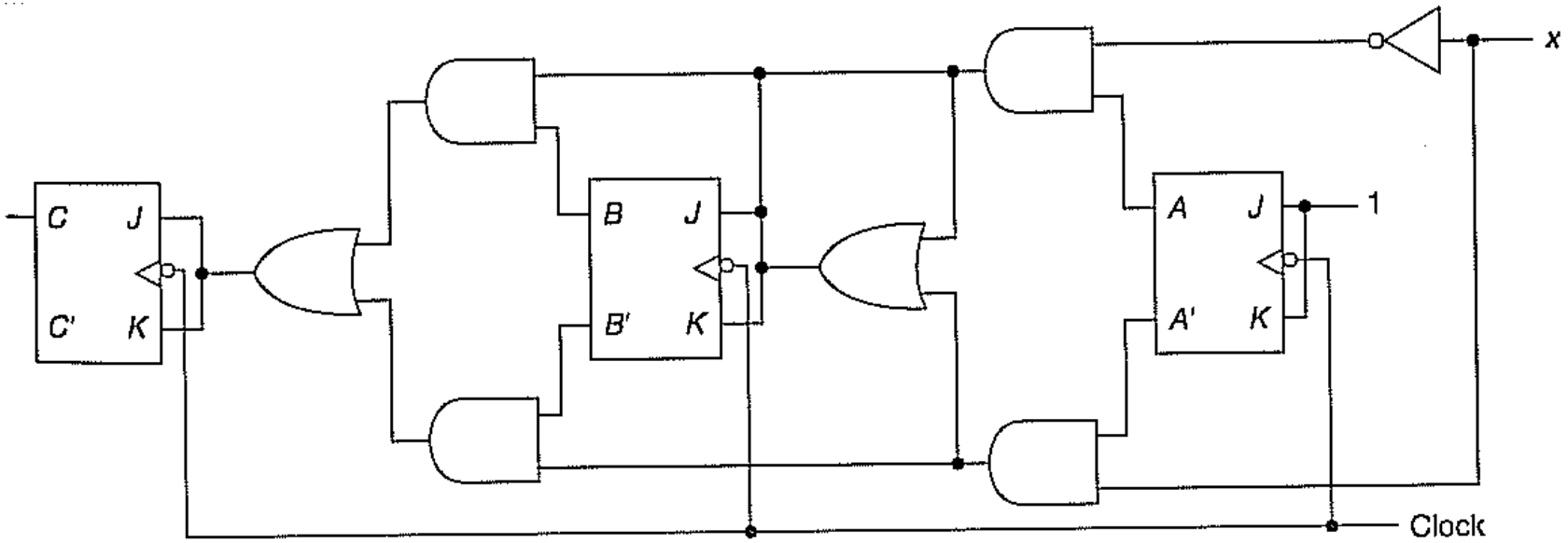
J_A



$$J_A = K_A = 1$$

Design of Synchronous Counters

3-bit up/down counter



$$J_C = K_C = x'BA + xB'A'$$

$$J_B = K_B = x'A + xA'$$

$$J_A = K_A = 1$$