Lecture 7

of

EEE201

CMOS Digital Integrated Circuits

Department of Electrical & Electronic Engineering

Xi'an Jiaotong-Liverpool University (XJTLU)

Tuesday, 24th October & 7th November 2023

- **Building Logic Gates from MOSFETs**
  - combinational logic circuits
  - basic logic gates & their combinations
  - MOSFETs in series or parallel to implement logic functions
  - schematic circuit to IC layout

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Digital Circuits from Logic Gates

(implementing Boolean functions)

- In CMOS digital integrated circuits (ICs), **MOSFETs** are used to build digital **logic gates**.
- Digital **logic gates** implement **Boolean functions** such as **NOT**, AND, OR, XOR, **NAND**, **NOR**, XNOR.
  - Any logic function/operation can be constructed from three basic logic gates: NOT, AND, and OR.
  - In CMOS digital ICs, NOT, NAND and NOR are adopted as the basic logic gates for implementing any complex logic function/operation.
  - Building complex digital circuits starts from the basic logic gates implemented by MOSFETs.
  - focus on NOT, NAND & NOR gates in EEE201

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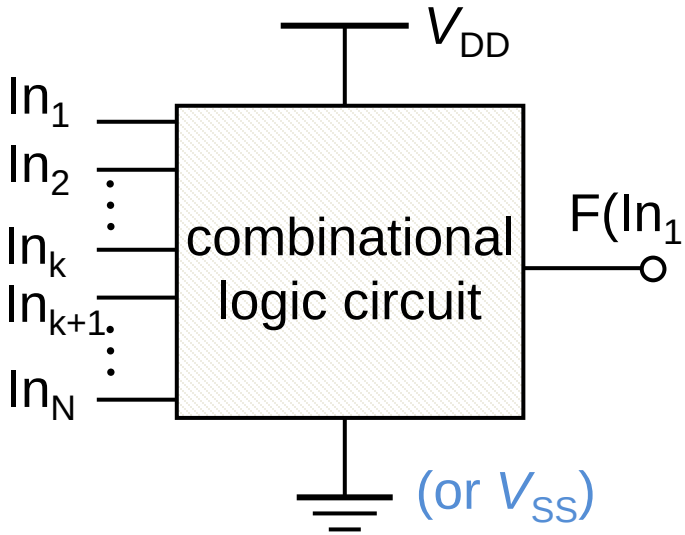
Combinational Logic Circuits

(outputs depends on only current inputs)

- Such digital circuits of implementing any **Boolean function** are called **combinational logic circuits**, of which the outputs depend *only* on the *current* inputs.



- A **combinational logic circuit** is a ***memoryless*** system.
- This is in contrast to **sequential logic circuits**, of which the outputs depend on both the current inputs and previous inputs
- **Sequential logic circuits** requires ***memory*** to store previous inputs.

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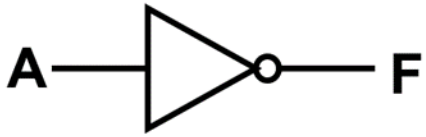
Combinational Logic Circuits

(basic logic gates)

- The ***memoryless*** nature of **combinational logic circuits** can be easily understood from the operation of the basic logic gates.

"NOT"

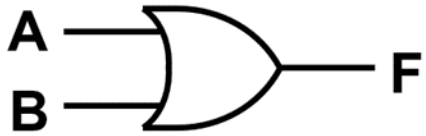


$F = \overline{A}$

A	F
0	1
1	0

also called **inverter**

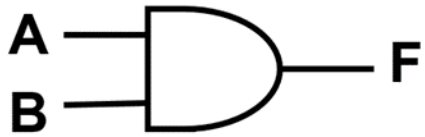
"OR"



$F = A+B$

A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

"AND"



$F = A \bullet B$

A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

- Output ***F*** is a function of only *current* inputs *A* and *B*.

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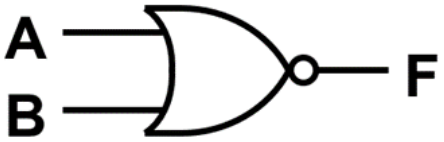
Basic Logic Gates

(XOR as combinational logic)

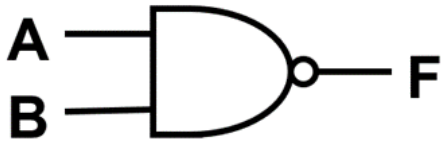
"NOR"



$F = \overline{A+B}$

A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

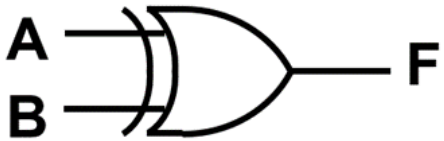
"NAND"



$F = \overline{A \cdot B}$

A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

"XOR"
(exclusive OR)



$F = A \oplus B$

$= A\overline{B} + \overline{A}B$

A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

- Note that the XOR logic function is a combination of NOT, AND and OR.

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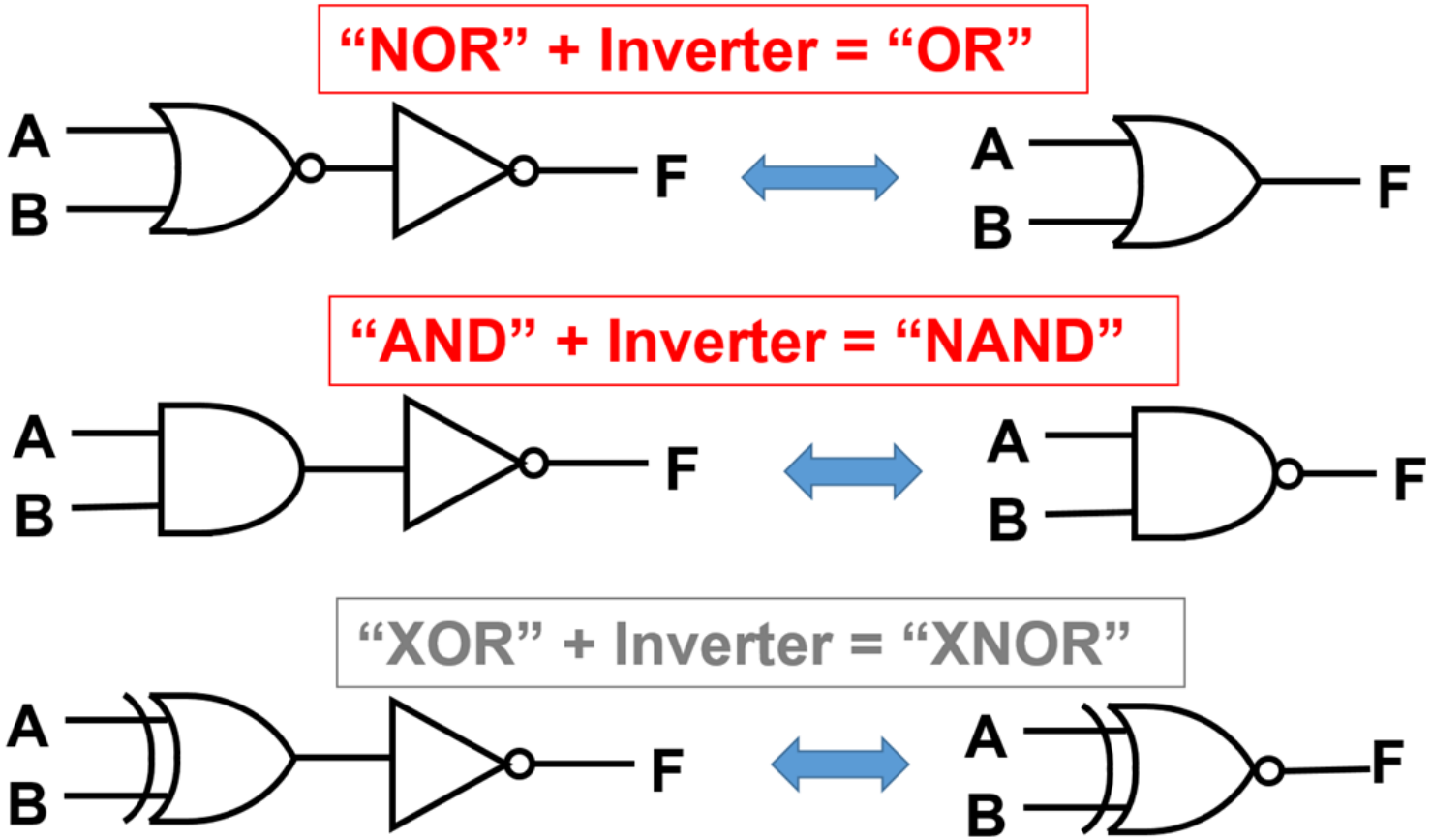
Basic Logic Gates

(OR & AND gates from NOR & NAND gates)



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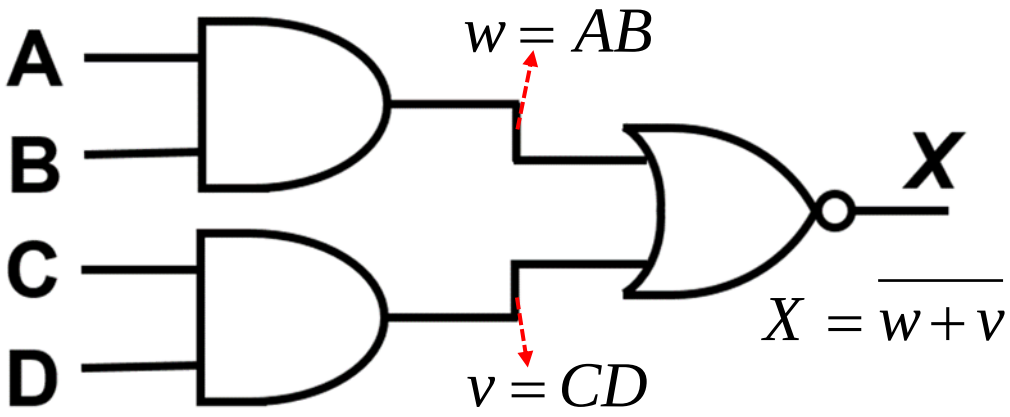
Combination of Logic Gates

(AOI & OAI)

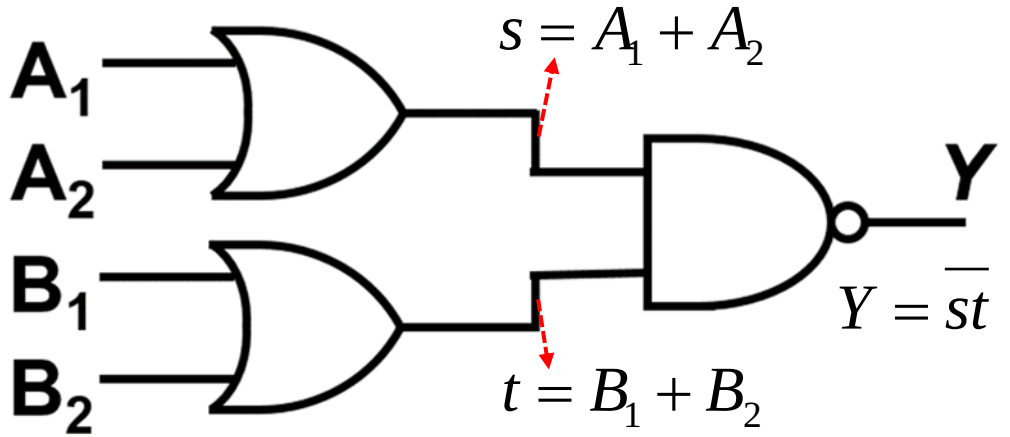
- AND-OR-Inverter (AOI) such as

$$X = \overline{(AB)+(CD)}$$



- OR-AND-Inverter (OAI) such as

$$Y = \overline{(A_1 + A_2)(B_1 + B_2)}$$



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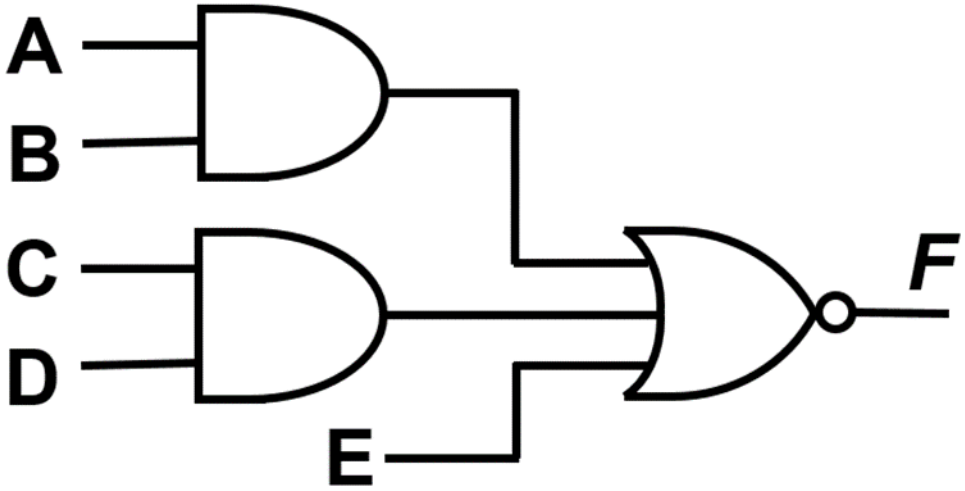
Combination of Logic Gates

(AOI & OAI)

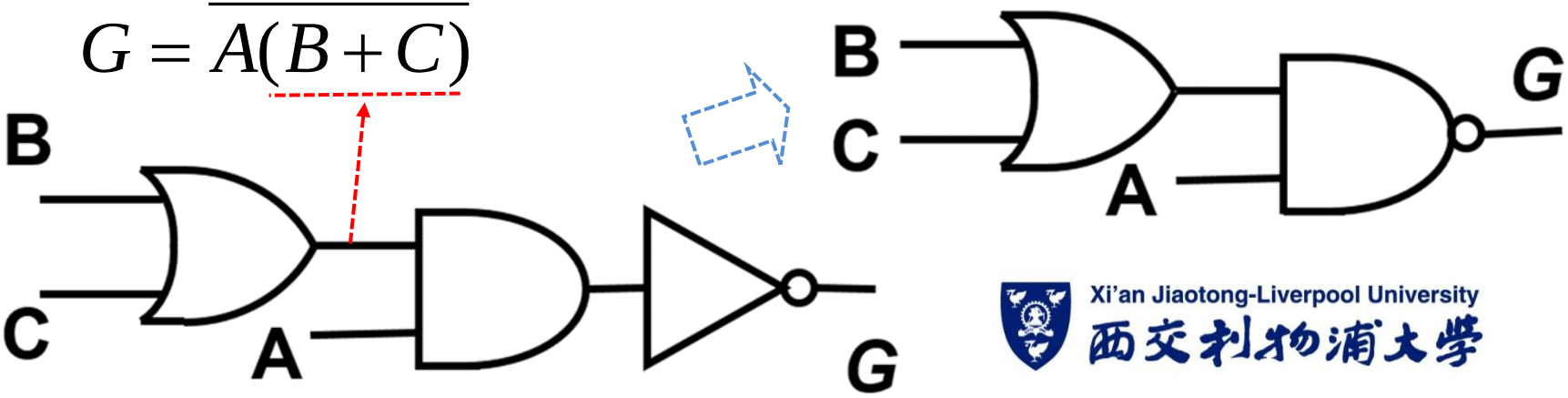
- AND-OR-Inverter (AOI) such as

$$F = \overline{(AB) + (CD) + E}$$



- OR-AND-Inverter (OAI) such as

$$G = \overline{A(B + C)}$$



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CMOS Digital ICs

(start from 3 basic logic gates)

- Digital logic circuits can be constructed using combinations of the three basic logic gates.
- The fundamental start in CMOS digital ICs is to design and construct the three logic gates using MOS transistors.
  - In using MOS transistors, there are a few different ways in the design and construction of the three logic gates.
  - The CMOS way (i.e. using both pMOSFETs and nMOSFETs for complementary circuit operation) is the best so far in terms of speed, power consumption, robustness, etc.

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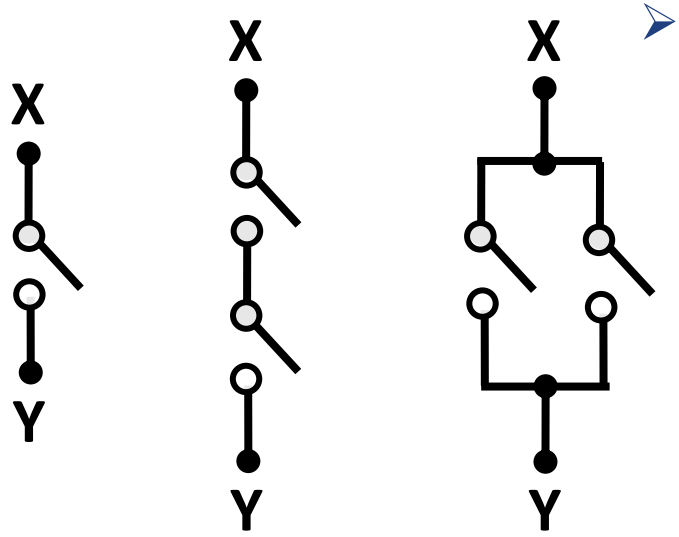
The MOSFET as a Switch

(NOT, AND, OR operations from switches)

- When the MOSFET as a 3-terminal device is used as a **switch**, the NOT, AND, and OR logic functions are achieved by the *series* and *parallel* connections of MOSFETs.



in series *in parallel*

- design & implementation consideration:
  - how close are the MOSFETs' behaviour as that of an (*ideal*) **switch**?
  - how can the MOSFETs be modelled as **switches** in digital circuits?

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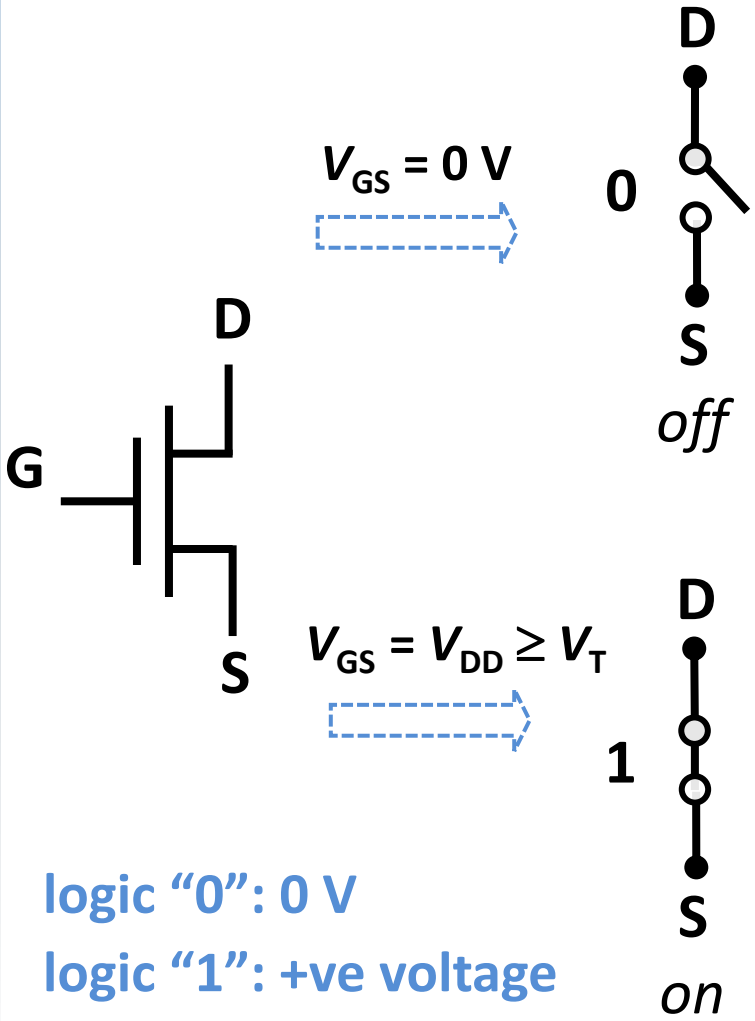
The MOSFET as a Switch

(NOT, AND, OR operations from switches)



- In its off state, the MOSFET behaves as open circuit (as an ***ideal*** switch).

  Note that here logic "0" is represented by 0 V or negative supply voltage; logic "1" by positive supply voltage.

- When turned on, the MOSFET behaves as short circuit (***ideally*** with zero resistance).

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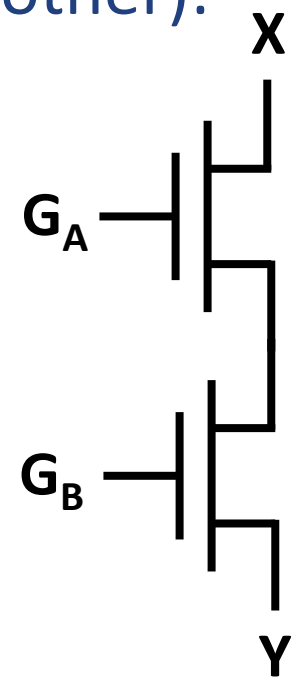
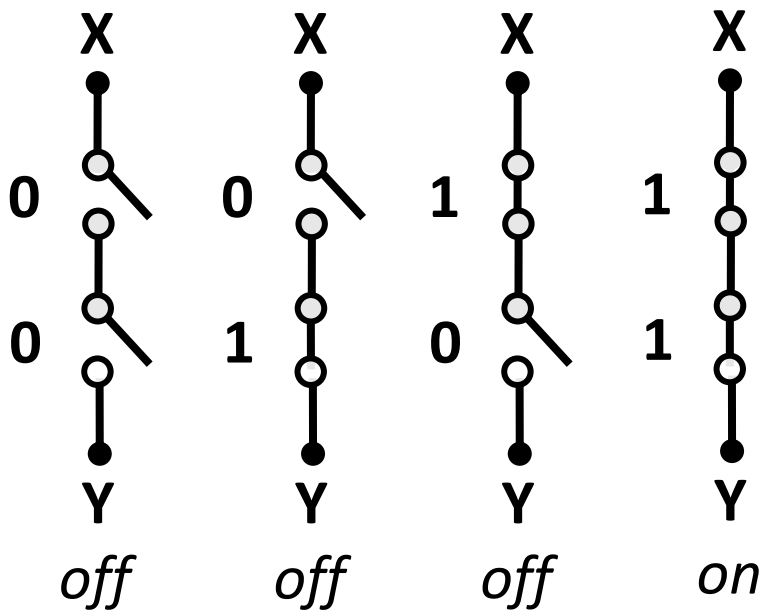
*n*MOSFETs in Series

(AND logic function)

- The AND logic function is achieved by two *n*MOSFETs connected in series (i.e. stacking over another):





$$Output = (G_A \bullet G_B)$$

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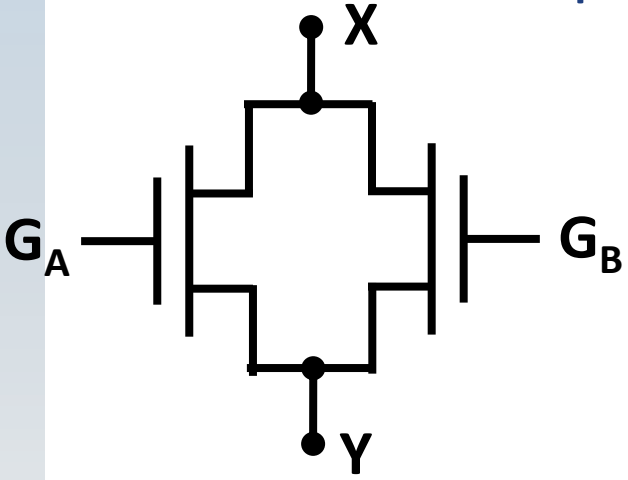
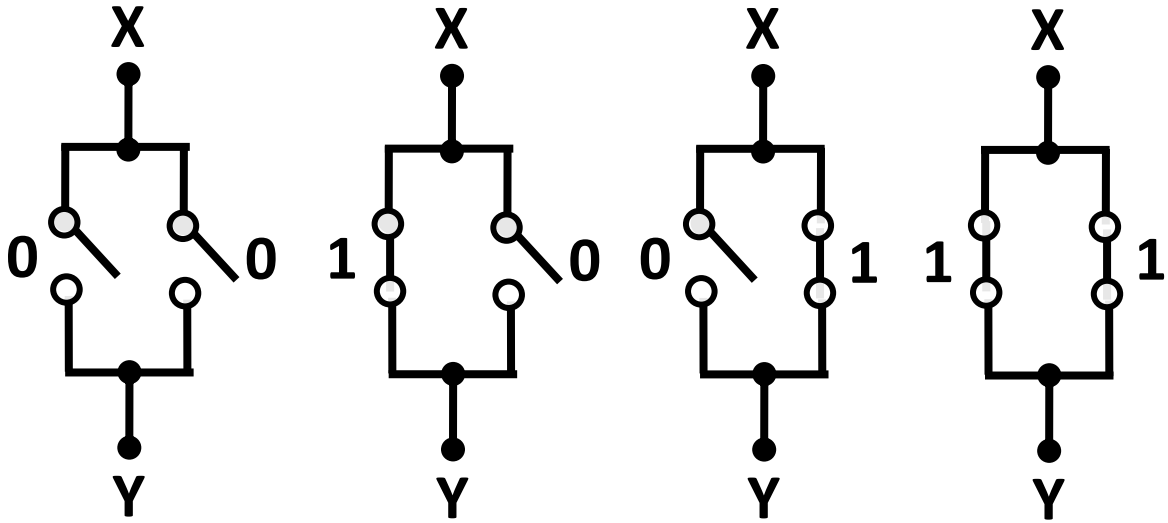
*n*MOSFETs in Parallel

(OR logic function)

- The OR logic function is achieved by two *n*MOSFETs connected in parallel:





off *on* *on* *on*

$$Output = (G_A + G_B)$$

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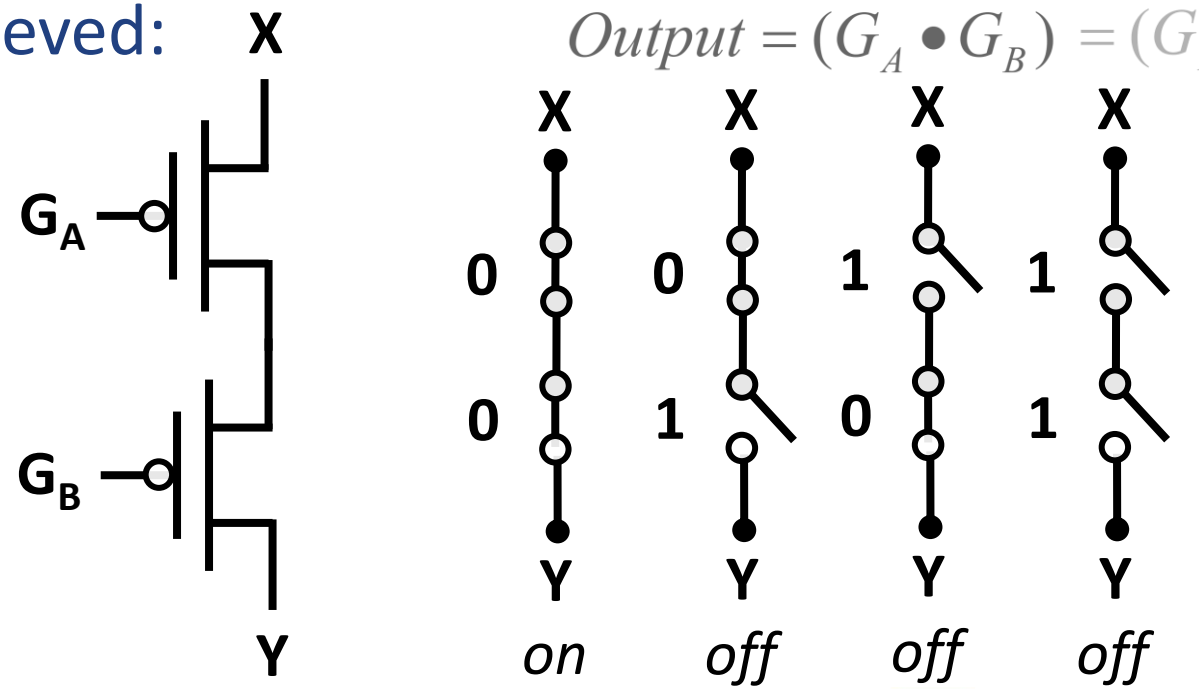
*p*MOSFETs in Series

(NOR logic function)

- When ***p***MOSFETs are connected in series (i.e. stacking over another), the NOR logic function is achieved:

$$Output = (\overline{G_A} \bullet \overline{G_B}) = \overline{(G_A + G_B)}$$



  - exactly opposite to that ***n***MOSFETs in parallel

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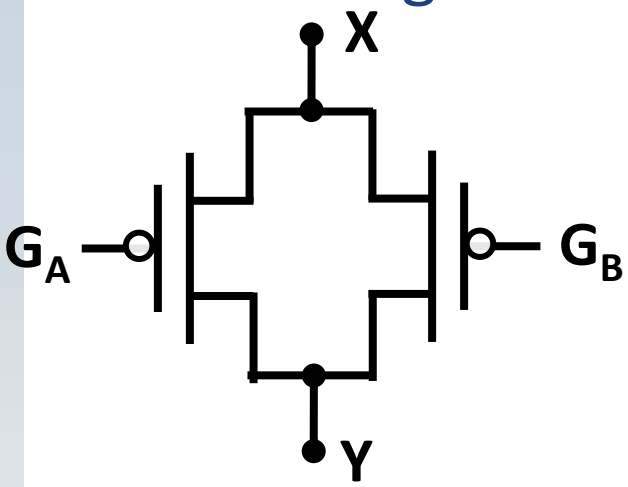
*p*MOSFETs in Parallel

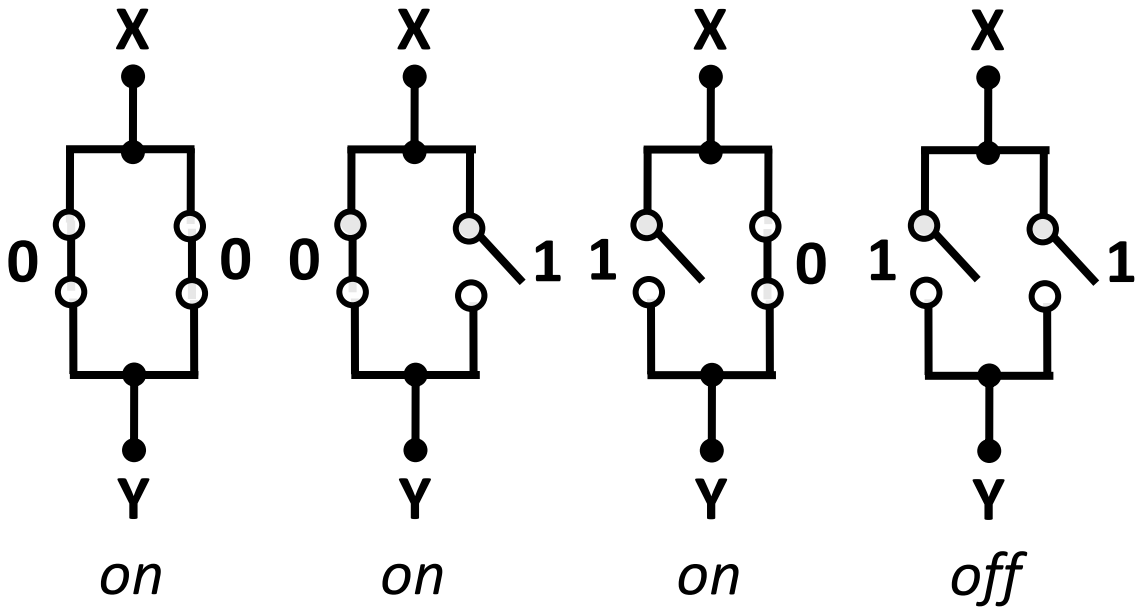
(NAND logic function)

- When ***p***MOSFETs are connected in parallel, the NAND logic function is achieved:



$$Output = (\overline{G_A} + \overline{G_B})$$

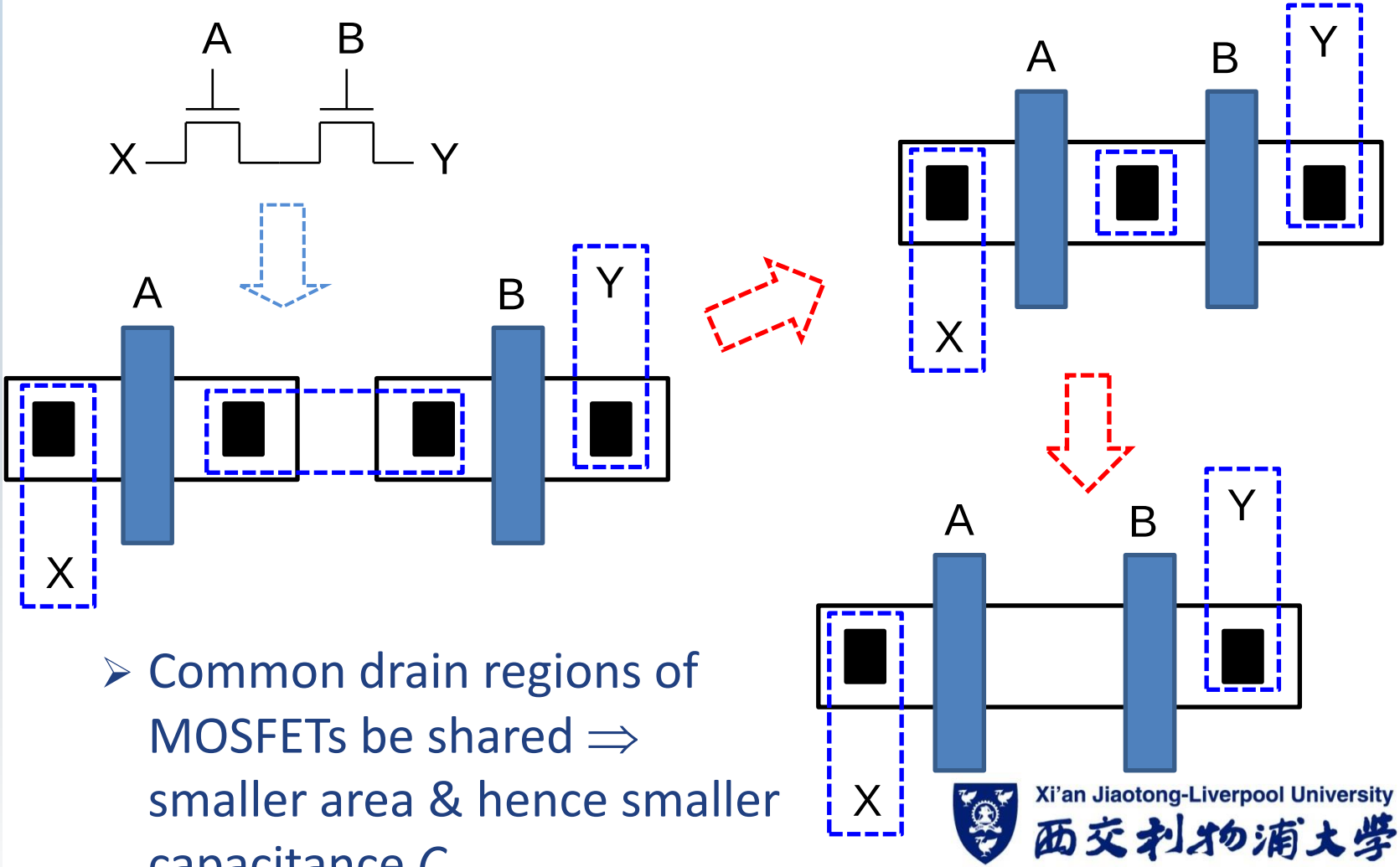
$$= \overline{(G_A \bullet G_B)}$$



  - exactly opposite to that ***n***MOSFETs in series

IC Layout of MOSFETs - sketch

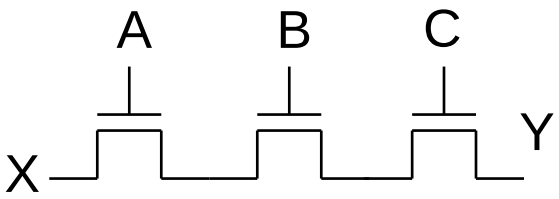
(two MOSFETs in series)

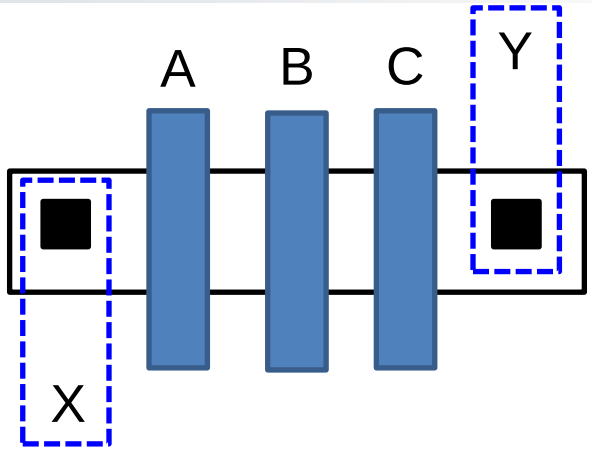


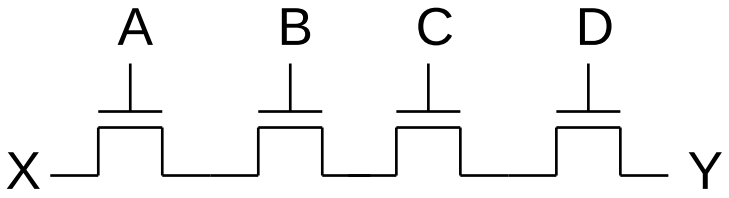
- Common drain regions of MOSFETs be shared ⇒ smaller area & hence smaller capacitance C_{jA}

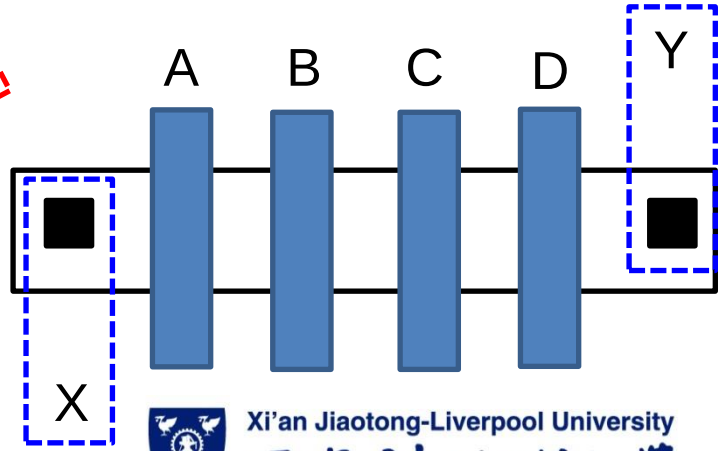
IC Layout of MOSFETs - sketch

(three & four MOSFETs in series)









- The shared common drain regions of MOSFETs can be made even smaller if connection not needed.

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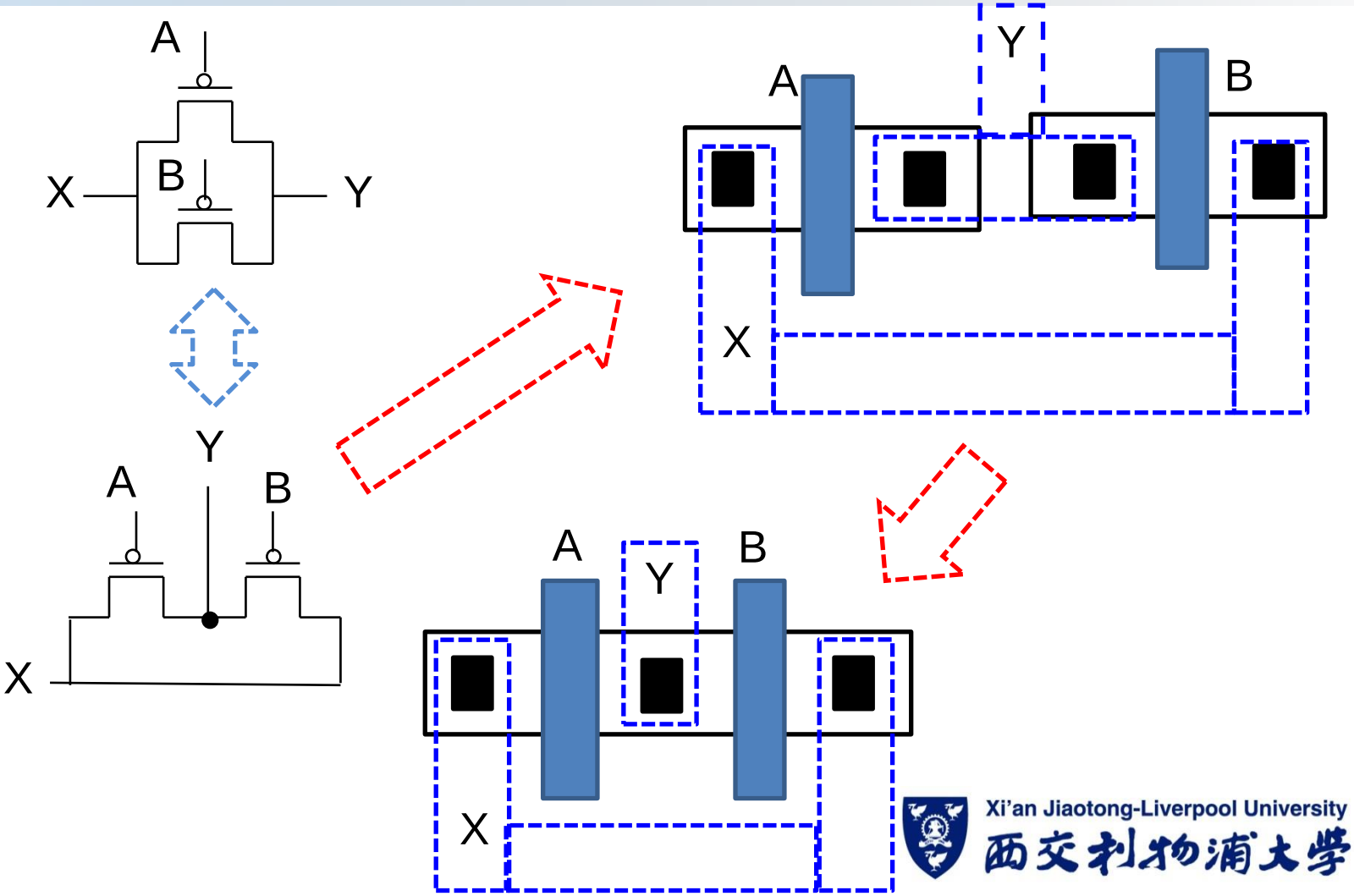
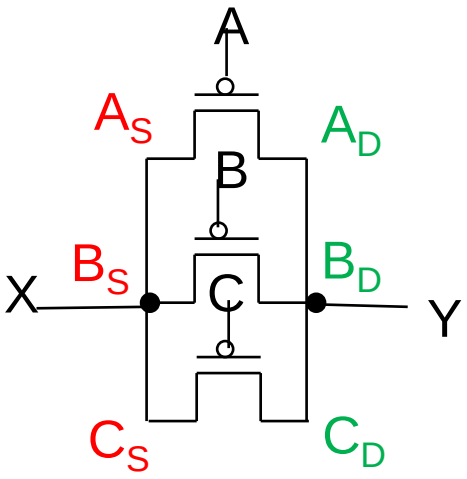
IC Layout of MOSFETs - sketch

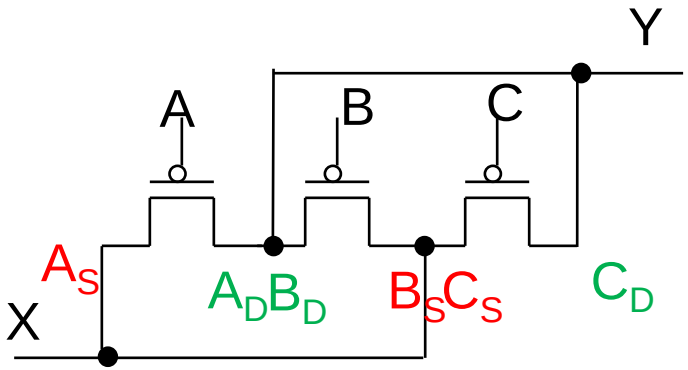
(two MOSFETs in parallel)

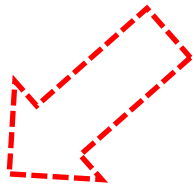


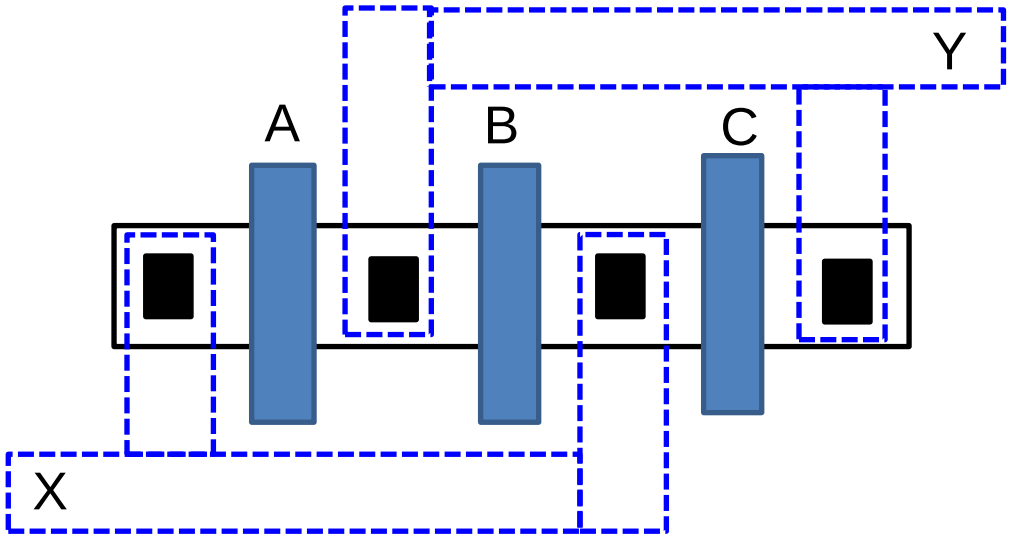
IC Layout of MOSFETs - sketch

(three MOSFETs in parallel)









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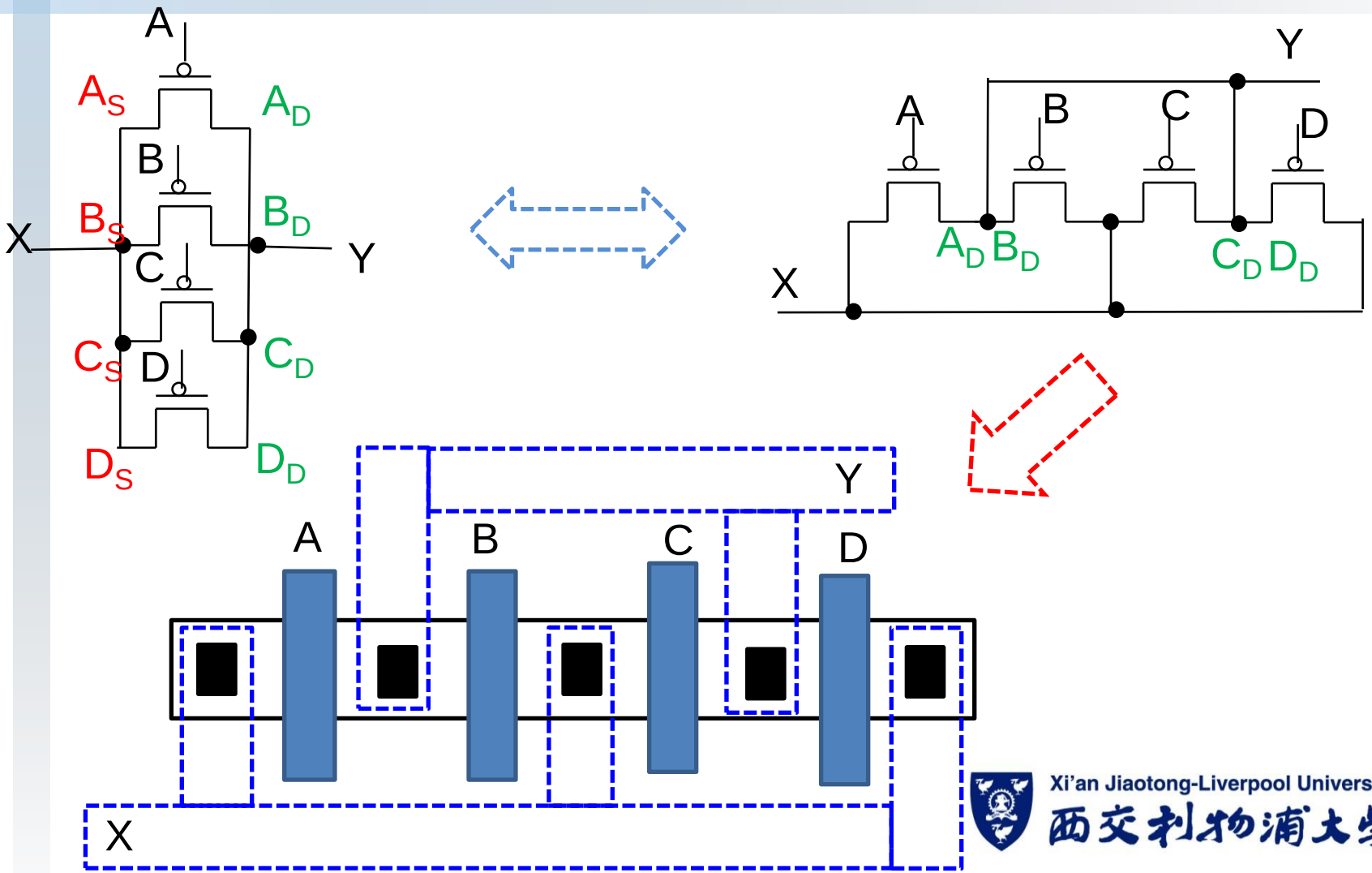
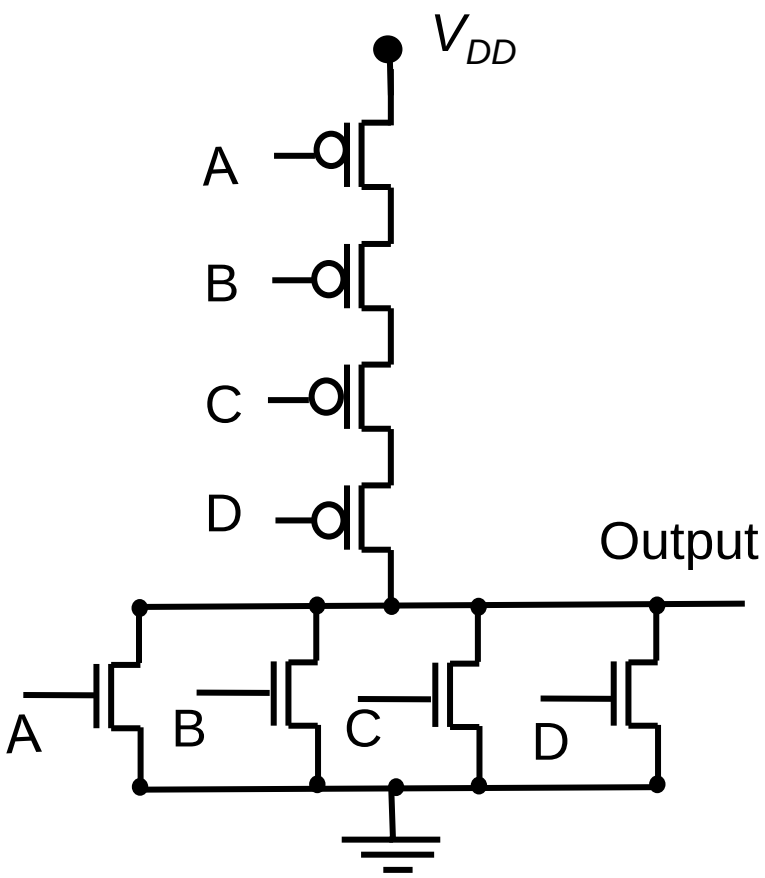
IC Layout of MOSFETs - sketch

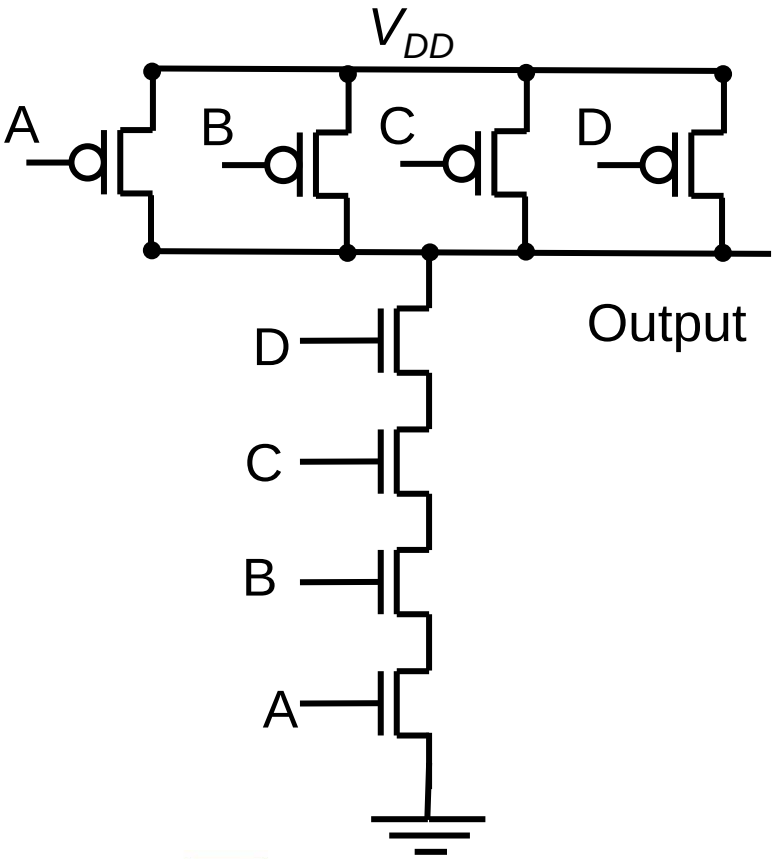
(four MOSFETs in parallel)



Logic Gates Made of MOSFETs

(nMOSFETs & pMOSFETs in series & parallel)





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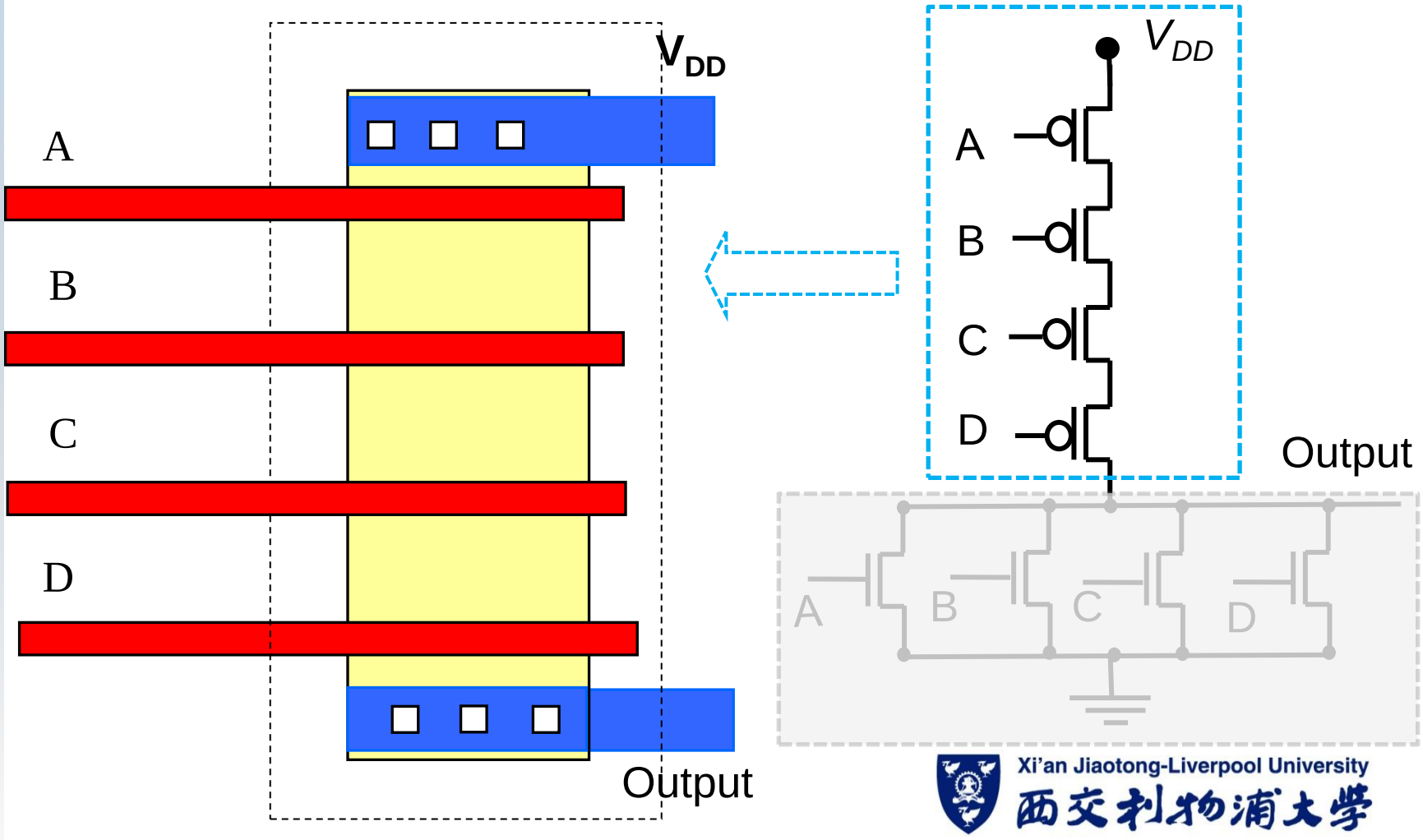
IC Layout of 4-input NOR Gate

(four ***p***MOSFETs in series)



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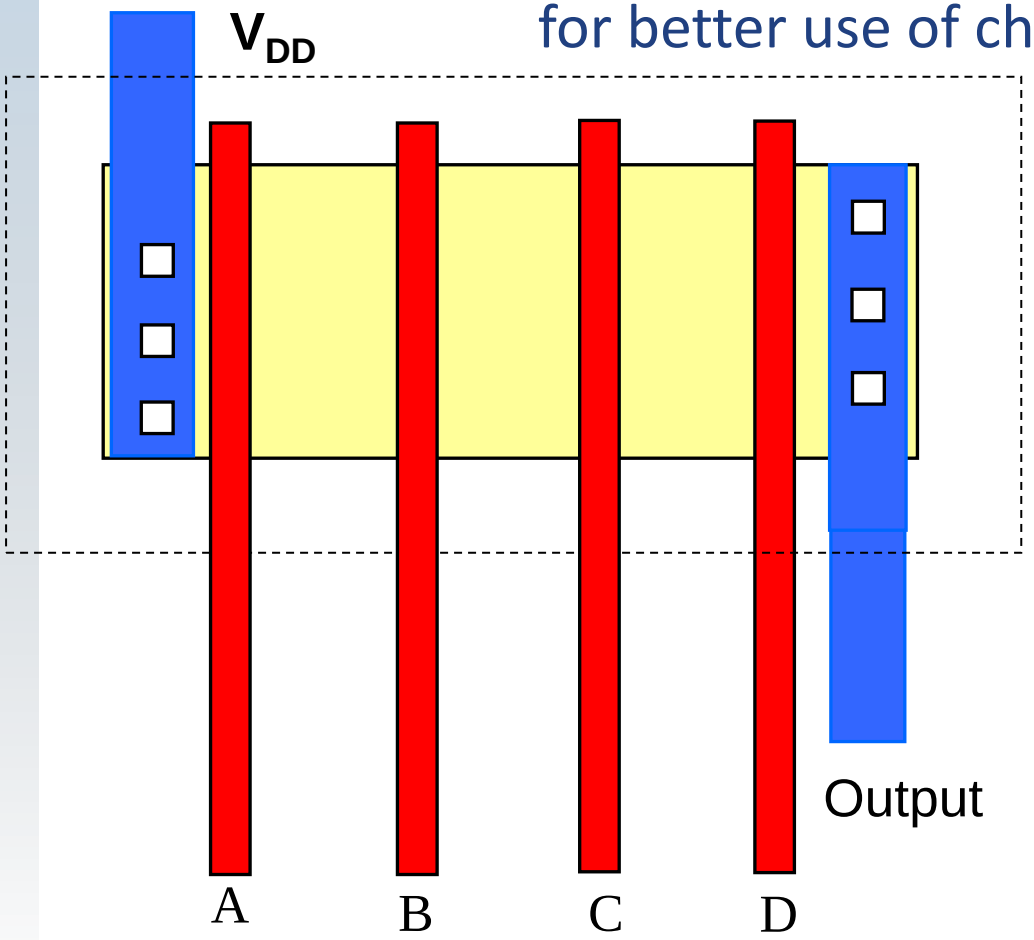
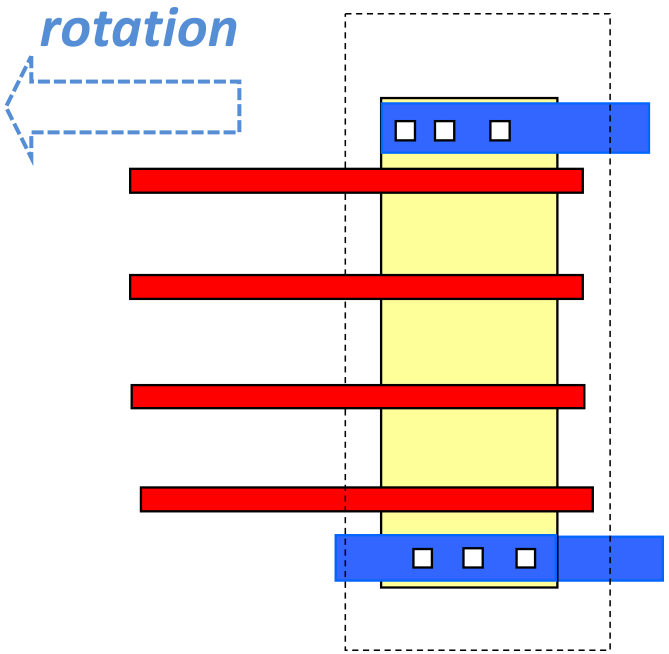
IC Layout of 4-input NOR Gate

(two MOSFETs in series)

- The IC layout of the MOSFETs can be oriented in such a way for better use of chip area and easier routing.





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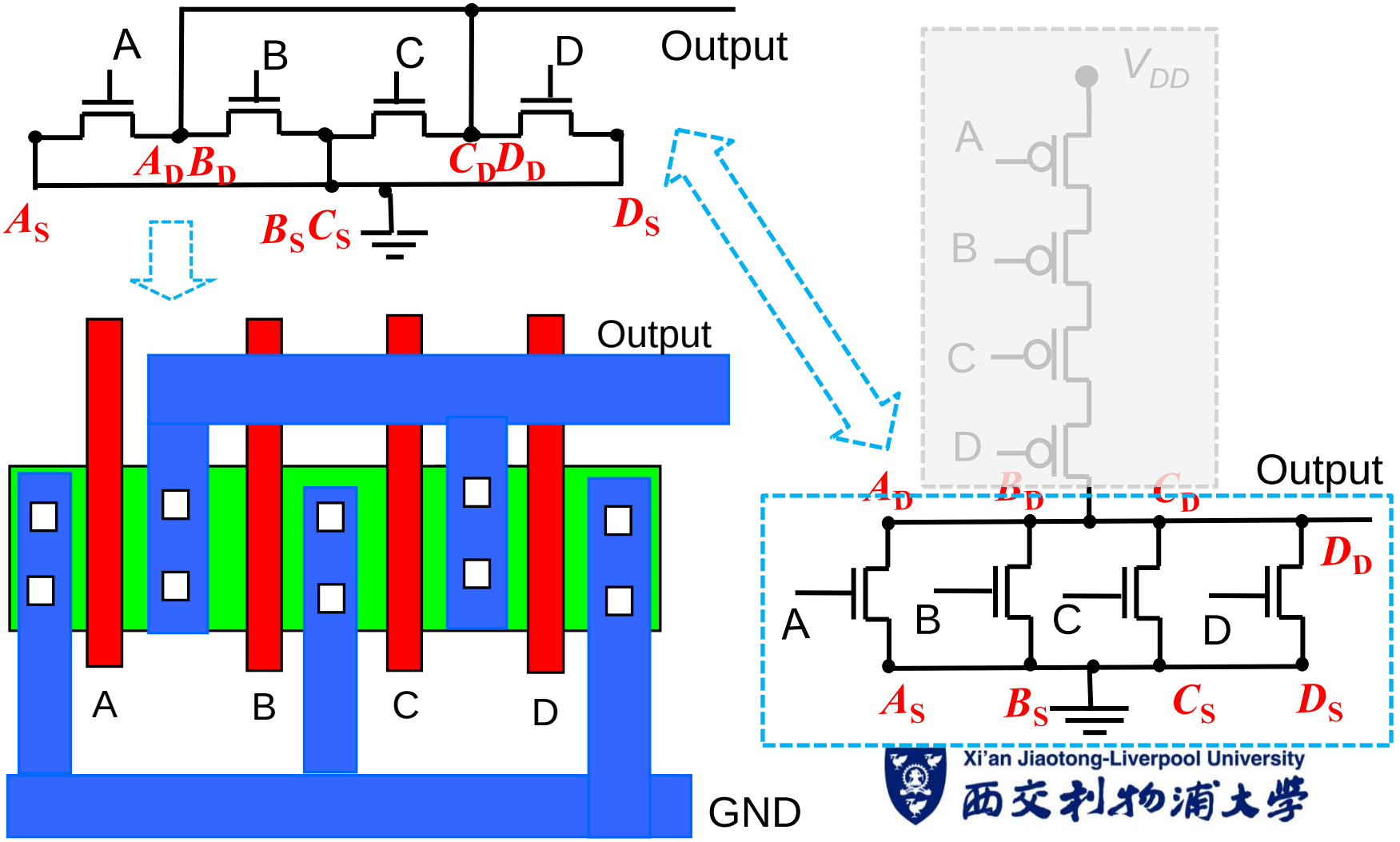
IC Layout of 4-input NOR Gate

(four ***n***MOSFETs in parallel)



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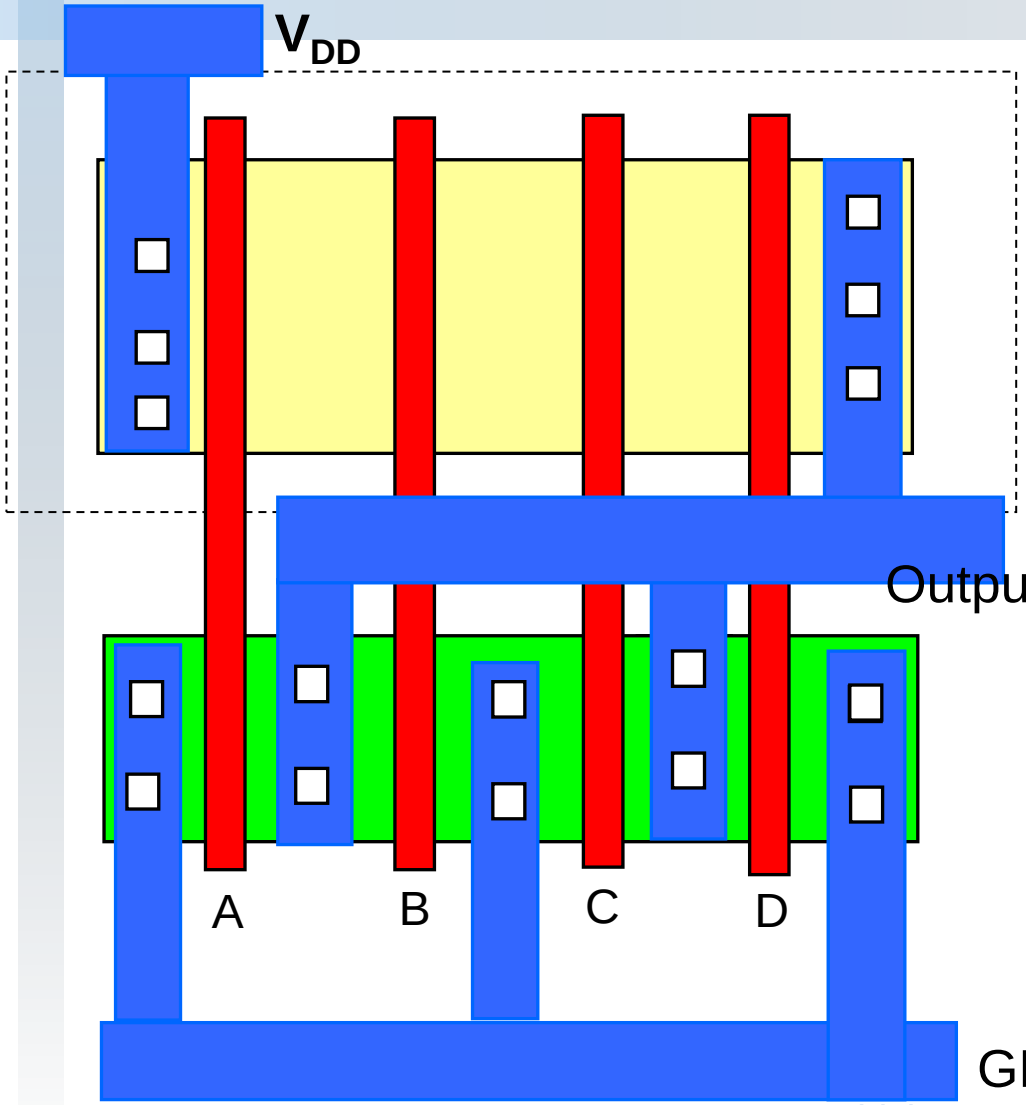
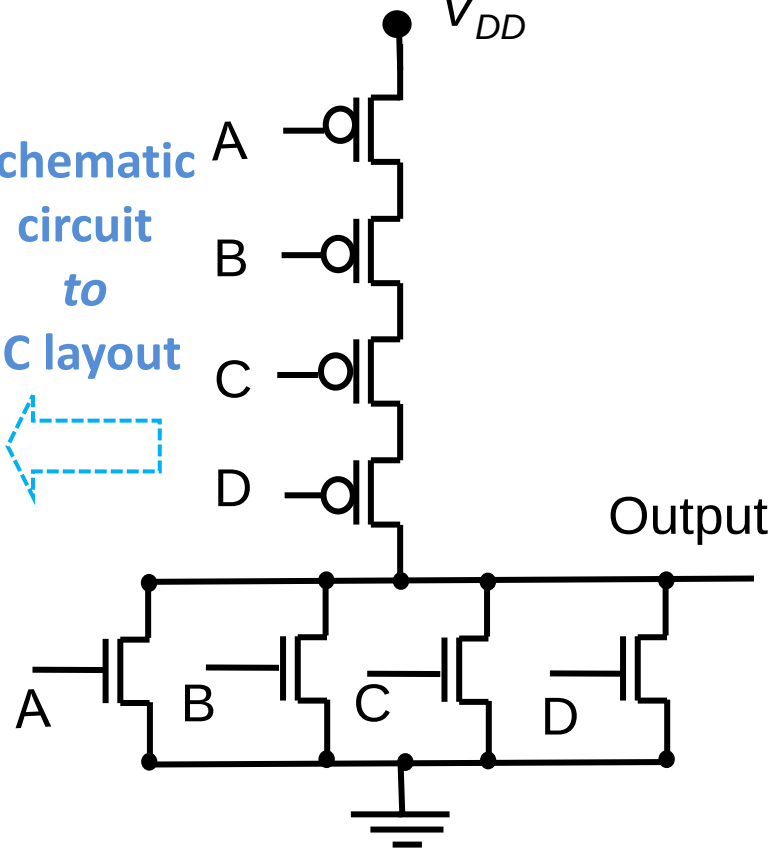
IC Layout of 4-input NOR Gate

(final layout optimised in chip area & routing)



schematic circuit *to* IC layout



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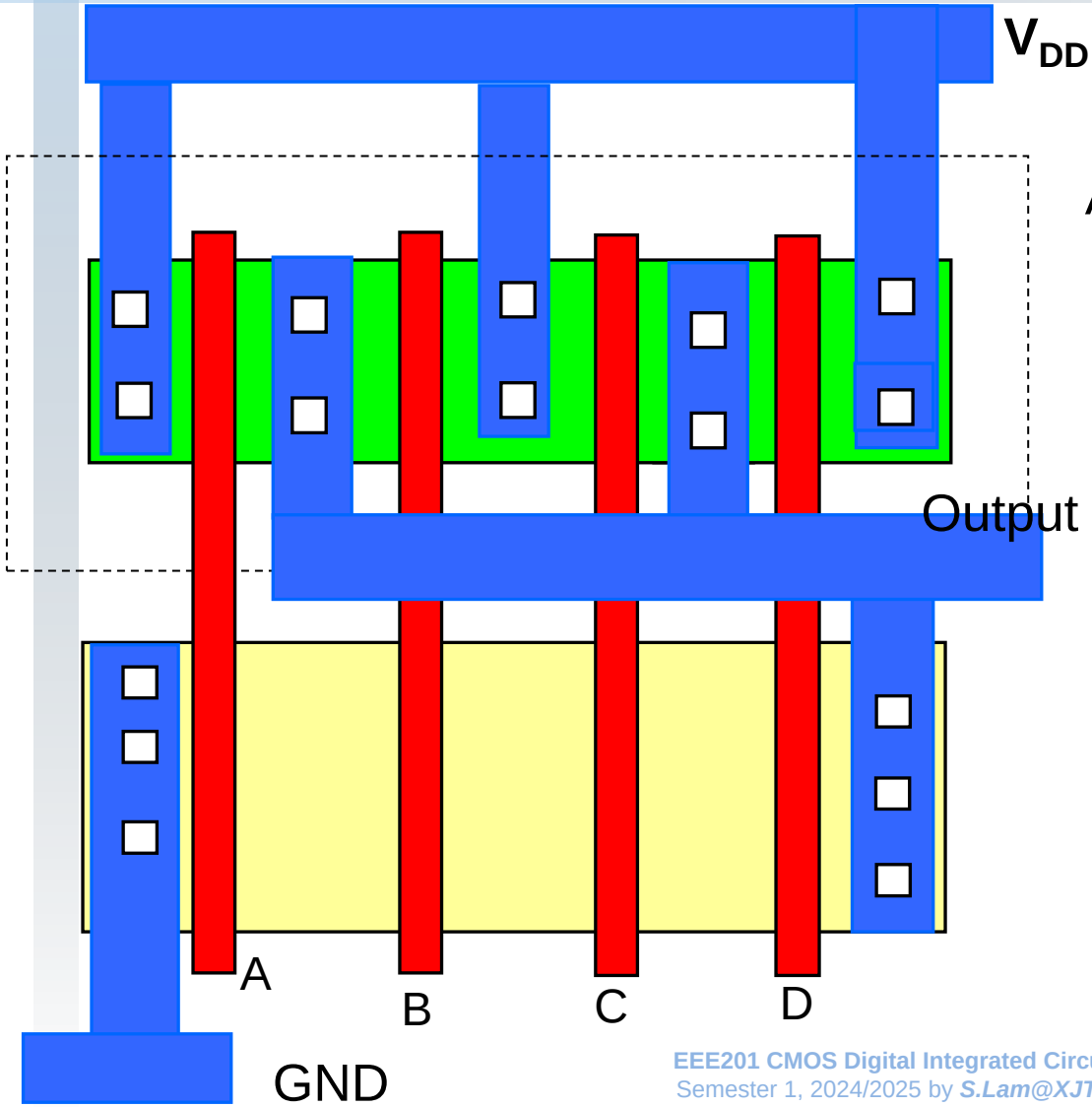
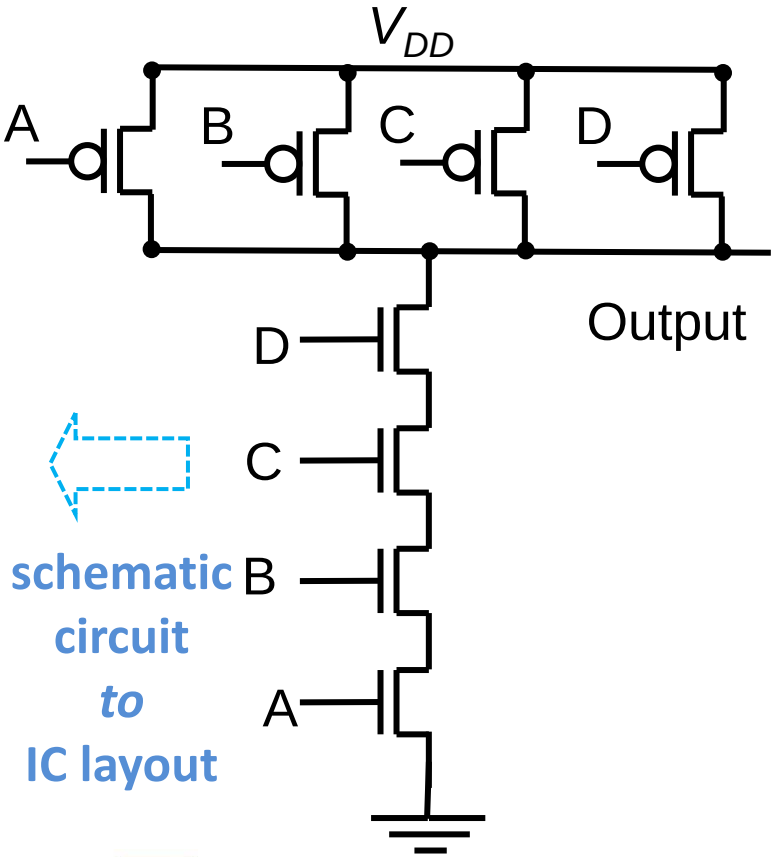
IC Layout of 4-input NAND Gate

(similar methods)





schematic circuit *to* IC layout

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Drawing IC Layout

(precise geometrical shapes & dimensions)

- In drawing the actual layout for IC fabrication, the geometrical shapes and dimensions need to be very *precise*, rather than sketches like those shown in previous slides.

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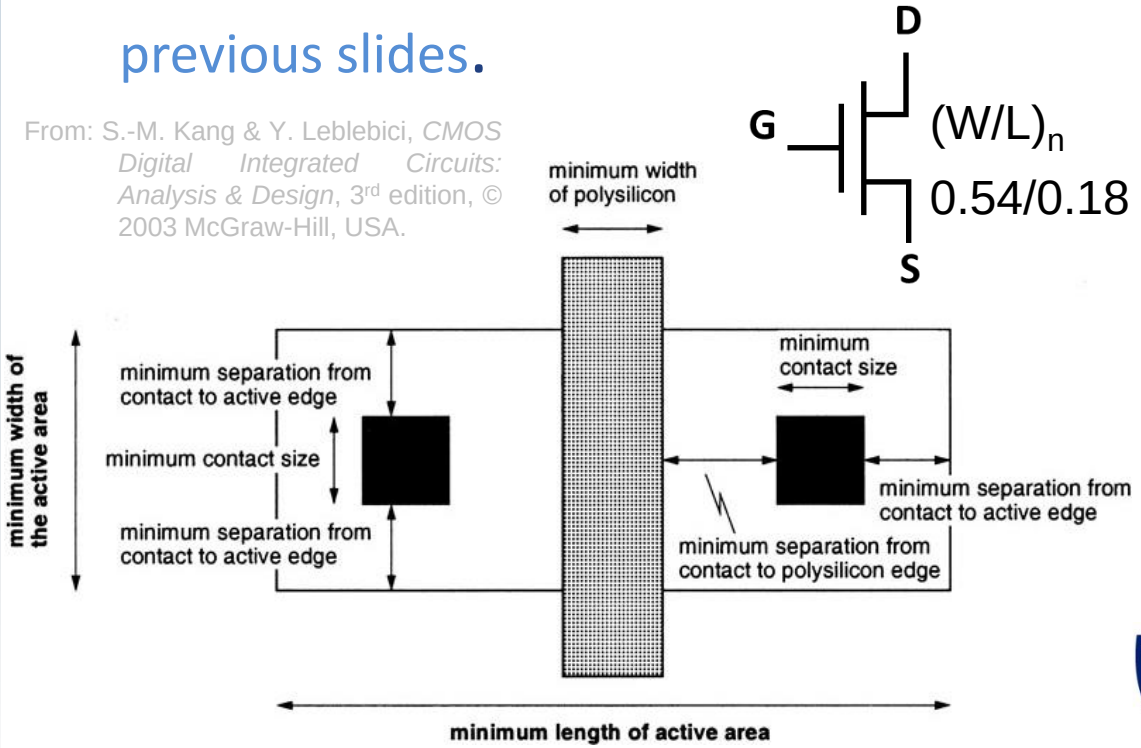

- An example of drawing *precisely* the IC layout of an nMOSFET in a 0.18-μm CMOS technology is shown on the left.

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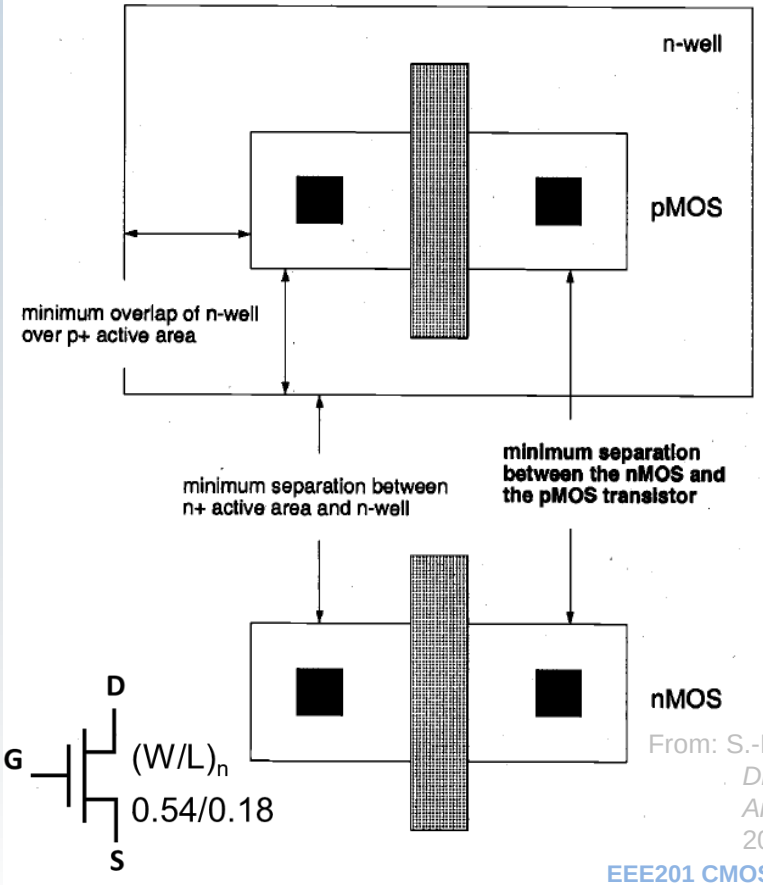
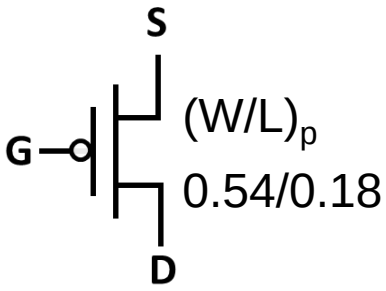
Precise Drawing of IC Layout
(pMOSFET)

- An example of the ***precise*** drawing the IC layout of a pMOSFET in a 0.18-μm CMOS technology is shown below:





- There is the additional ***n*-well** layer (assuming a ***p***-type wafer).
- The ***n*-well** needs certain separation distance from the ***n***-type diffusion regions (source/drain) of ***n***MOSFETs.

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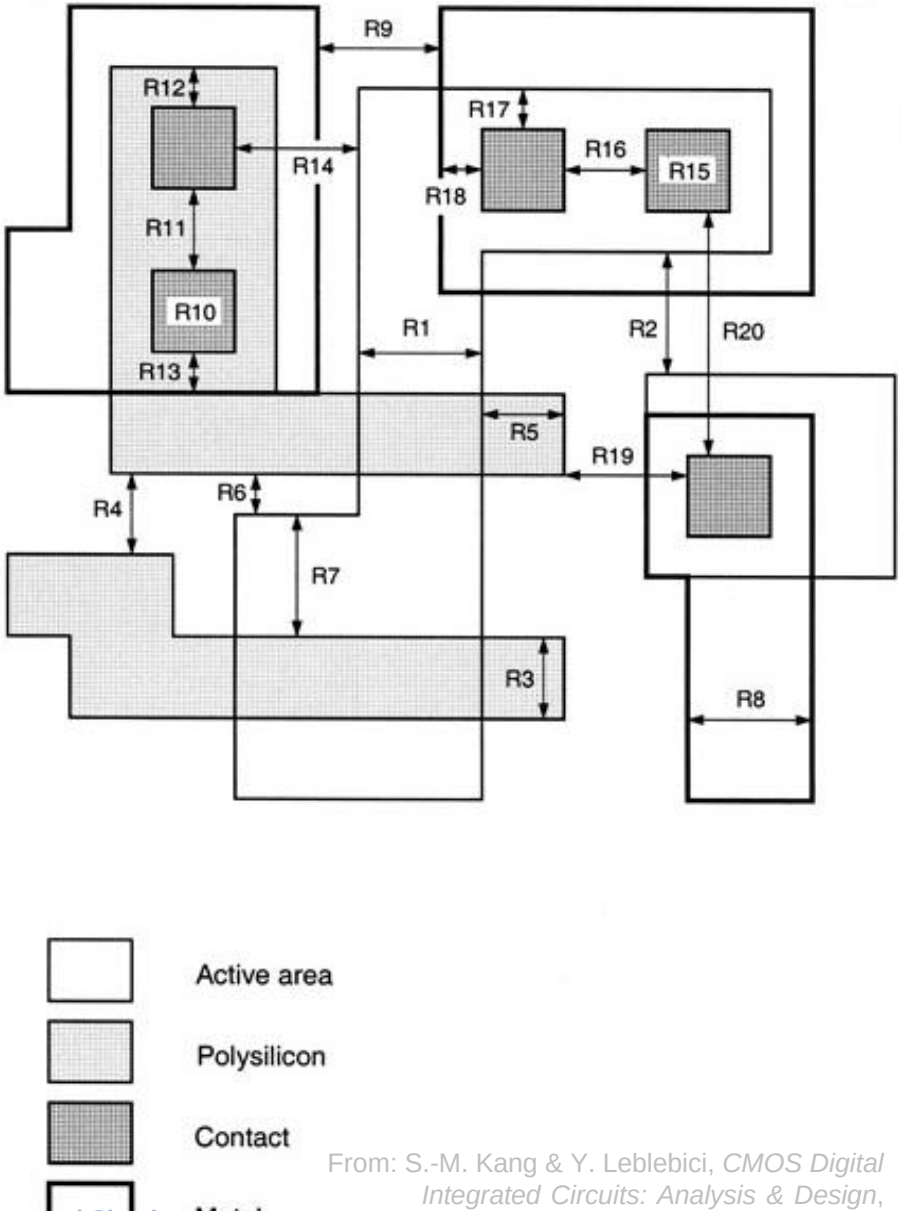
Rules in Drawing IC Layout

Rule number	*Description*	*λ-Rule*
	Active area rules	
R1	Minimum active area width	3λ
R2	Minimum active area spacing	3λ
	Polysilicon rules	
R3	Minimum poly width	2λ
R4	Minimum poly spacing	2λ
R5	Minimum gate extension of poly over active	2λ
R6	Minimum poly-active edge spacing (poly outside active area)	1λ
R7	Minimum poly-active edge spacing (poly inside active area)	3λ
	Metal rules	
R8	Minimum metal width	3λ
R9	Minimum metal spacing	3λ
	Contact rules	
R10	Poly contact size	2λ
R11	Minimum poly contact spacing	2λ
R12	Minimum poly contact to poly edge spacing	1λ
R13	Minimum poly contact to metal edge spacing	1λ
R14	Minimum poly contact to active edge spacing	3λ
R15	Active contact size	2λ
R16	Minimum active contact spacing (on the same active region)	2λ
R17	Minimum active contact to active edge spacing	1λ
R18	Minimum active contact to metal edge spacing	1λ
R19	Minimum active contact to poly edge spacing	3λ
R20	Minimum active contact spacing (on different active regions)	4λ



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