EEE201 CMOS Digital Integrated Circuits
CMOS IC Layout Design Project

Assessment Weighting
This assessment counts **15%** of the module marks.

Aims
This project aims to provide students with an experience of designing a simple silicon **CMOS** integrated circuit (IC) at the layout level, as well as offering an insight into the CMOS manufacturing process flow.

Learning Outcomes
On completion of this project, students should be able to:
1. understand the manufacturing processes involved in fabricating silicon-based devices, in particular CMOS ICs;
2. understand the design process and constraints involved in developing CMOS ICs;
3. design mask layout of a CMOS logic circuit; and
4. produce an engineering-styled report.

Design Task
The objective of this assignment is to design an IC layout of the simple logic circuit shown in Figure 1(a), with a minimal layout area and number of masks required to manufacture the circuit. The transistor schematic diagram of the logic circuit is shown in Figure 1(b).

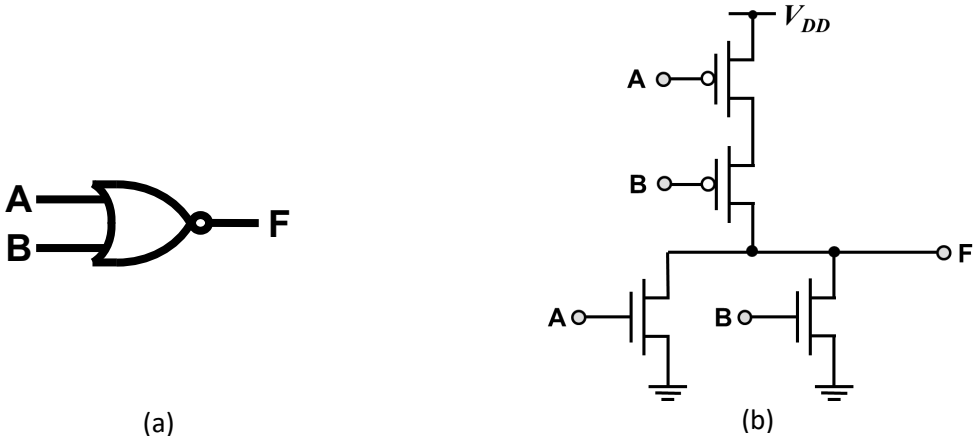

Fig. 1 NOR2 gate: (a) logic symbol and (b) circuit schematic of a CMOS 2-input NOR gate

The process parameters for the design are listed in Table 1. You should use these data to calculate the aspect ratio (or equivalently width/length) of each CMOS transistor and then determine a suitable layout to interconnect the CMOS transistors, while minimising the IC area. Assume fabrication using ***p***-type silicon wafers.

Table 1: CMOS process parameters

Gate oxide areal capacitance C_{ox}	1.2×10^{-2} F/m^2
Threshold Voltage V_T	0.5 V (V_{Tp} = -0.5 V)
Supply Voltage V_{DD}	3.0 V
Electron mobility μ_n	0.036 m^{2}V^{-1}s^{-1}
Hole mobility μ_p	0.018 m^{2}V^{-1}s^{-1}
Minimum feature size	0.20 μm
Maximum alignment error	0.10 μm

Please use the provided graph paper sheet for drawing the IC layout by hand in this semester, 2024/2025.