Lecture 5
of
EEE201

CMOS Digital Integrated Circuits

Department of Electrical & **Electronic Engineering**
Xi'an Jiaotong-Liverpool University (XJTLU)
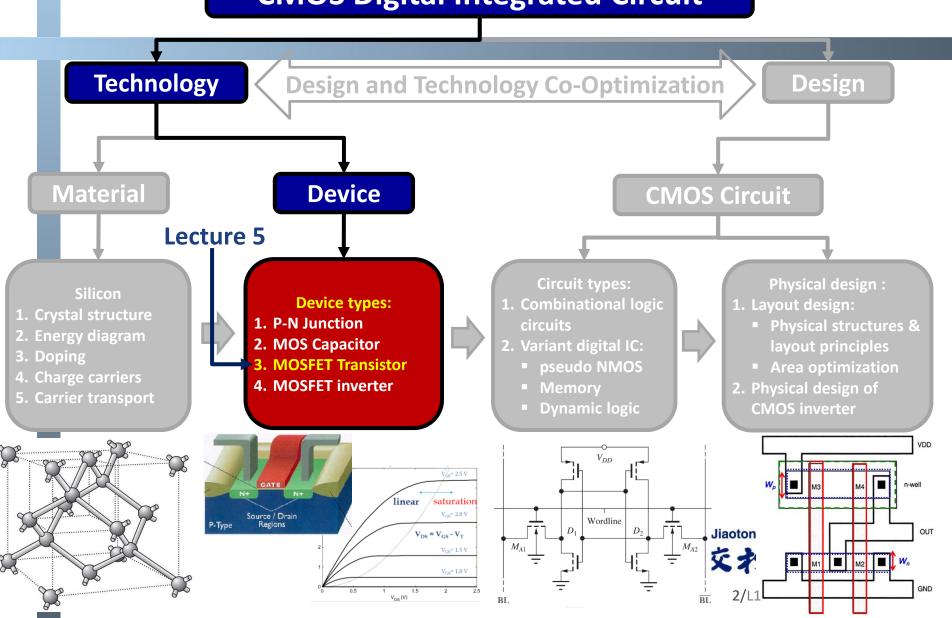
Monday, 14th October 2024

❑ **MOS Transistor**

➢ structure from MOS capacitor

➢ operation modes & I-V characteristics

➢ physical understanding (slides 20-31) in essence
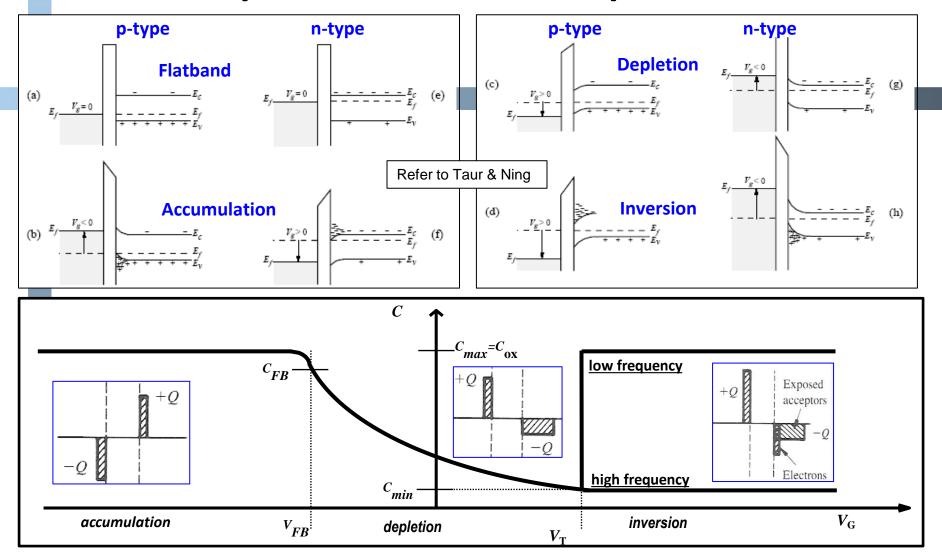
➢ **physical layout** & capacitance

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Module Roadmap

CMOS Digital Integrated Circuit

Technology ← Design and Technology Co-Optimization → **Design**

Material   **Device**   **CMOS Circuit**

Lecture 5

Silicon
1. Crystal structure
2. Energy diagram
3. Doping
4. Charge carriers
5. Carrier transport

Device types:
1. P-N Junction
2. MOS Capacitor
3. **MOSFET Transistor**
4. MOSFET inverter

Circuit types:
1. Combinational logic circuits
2. Variant digital IC:
   - pseudo NMOS
   - Memory
   - Dynamic logic

Physical design :
1. Layout design:
   - Physical structures & layout principles
   - Area optimization
2. Physical design of CMOS inverter

2/L1

Recap: Lecture 4: MOS Capacitance

p-type   **n-type**

Flatband

(a)

(e)

Refer to Taur & Ning

Accumulation

(b)

(f)

p-type   **n-type**

Depletion

(c)

(g)

Inversion

(d)

(h)

low frequency

high frequency

c_{FB}

$C_{max}=C_{ox}$

$+Q$

$-Q$

$+Q$

$-Q$

$+Q$ Exposed acceptors

$-Q$

Electrons

C_{min}

accumulation v_{FB} *depletion* V_T *inversion* V_G

$$V_G = V_{FB} + \phi_s + \frac{\sqrt{2qN_a\varepsilon_{Si}(\phi_s)}}{C_{ox}}$$
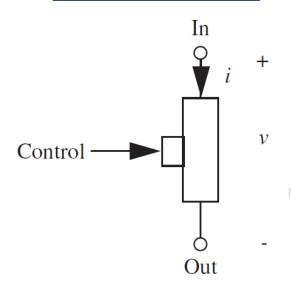
$$V_T = V_{FB} + 2\phi_F + \frac{\sqrt{2qN_a\varepsilon_{Si}(2\phi_F)}}{C_{ox}}$$

ϕ_F = equilibrium Fermi level E_f

2-Terminal MOS Capacitor
(for constructing 3-terminal device)

❑ The two-terminal **MOS capacitor** can be used for constructing a very useful <u>three-terminal device</u>.

❑ In a <u>3-terminal device</u>, the current flowing through the other two terminals can be *controlled* by the <u>third terminal</u>.

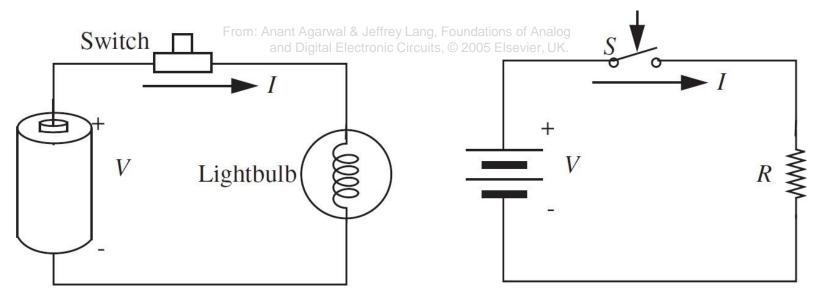❑ Such a 3-terminal device is commonly used as a **switch**, especially in digital circuits.

From: Anant Agarwal & Jeffrey Lang, Foundations of Analog and Digital Electronic Circuits, © 2005 Elsevier, UK.

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Switch & Digital States

(binary states)

❑ When the **switch** is turned on, it can be used to represent a digital state "1"; "0" when off.

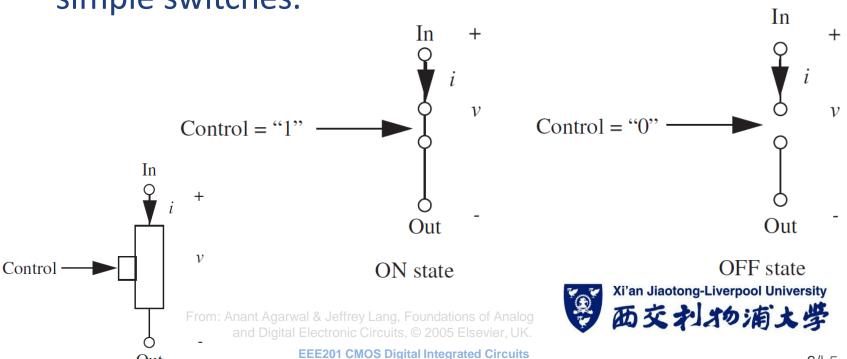From: Anant Agarwal & Jeffrey Lang, Foundations of Analog and Digital Electronic Circuits, © 2005 Elsevier, UK.

3-Terminal Device
(simple switches for building logic circuits)

❑ More importantly, the **switch** itself can be controlled by digital states "1" or "0".

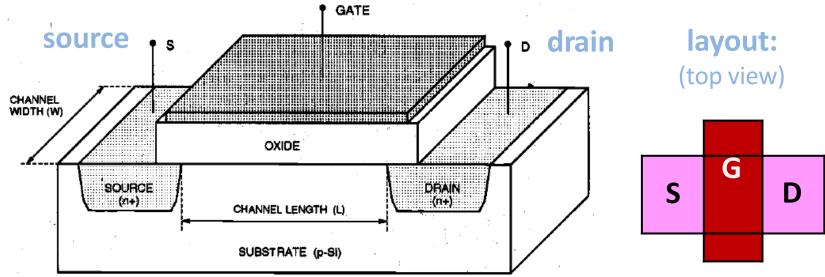❑ Complex **logic circuits** can then be built from such simple switches.

Control = "1" → ON state

Control = "0" → OFF state

From: Anant Agarwal & Jeffrey Lang, Foundations of Analog and Digital Electronic Circuits, © 2005 Elsevier, UK.

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MOSFET from MOS Capacitor

(physical structure)

❑ A highly useful 3-terminal device can be constructed from the **MOS capacitor** with the basic structure shown here:

From: S.-M. Kang & Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis & Design*, 3rd edition, © 2003 McGraw-Hill, USA.
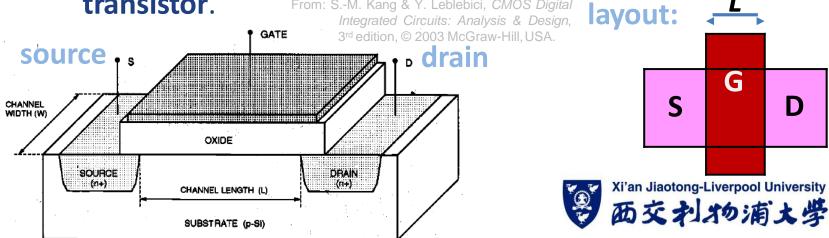
source **drain** **layout:**
(top view)

➢ It is called the **MOS field-effect transistor** (**MOSFET**) or simply **MOS transistor**.
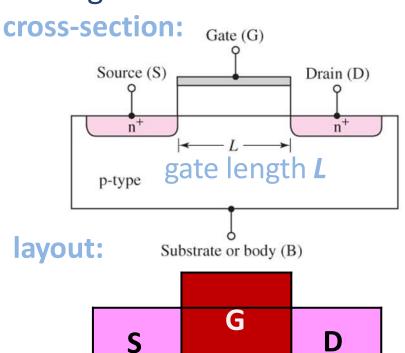
MOSFET from MOS Capacitor
(diffusion regions)

❑ In addition to the **gate electrode** and **substrate** (*p*-type in this case) of the **MOS capacitor**, there are two highly doped regions (called diffusion regions) on two sides of the gate.

➢ The two diffusion regions are called the **source** and the **drain** which are the *conducting* terminals of the **MOS transistor**.

From: S.-M. Kang & Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis & Design*, 3rd edition, © 2003 McGraw-Hill, USA.

source

drain

layout:

MOSFET from MOS Capacitor
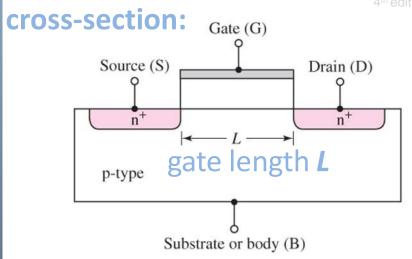(source & drain terminals)

❑ The basic structure of the **MOS transistor** is completely *symmetrical* with respect to the **source** and **drain** regions. From: Donald A. Neamen, *Microelectronics: Circuit Analysis & Design*, 4th edition, © 2010 McGraw-Hill, USA.

cross-section:

Gate (G)

Source (S)   Drain (D)

n+   n+

|← L →|

gate length **L**

p-type

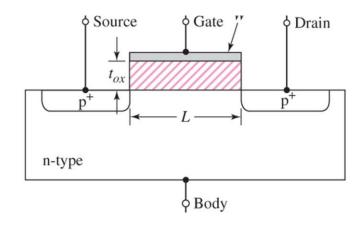Substrate or body (B)

layout:

S   **G**   D

L

➢ The different roles of the **source** and **drain** terminals are defined by the applied terminal voltages and the current flow, especially in digital integrated circuits.

➢ **source** & **drain** for the carriers

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MOSFET from MOS Capacitor

(nMOS & pMOS transistors)

❑ The structure of the nMOS and pMOS transistors are very similar. The differences are in the diffusion regions and the substrate.

From: Donald A. Neamen, *Microelectronics: Circuit Analysis & Design*, 4th edition, © 2010 McGraw-Hill, USA.

cross-section:

gate length **L**

nMOS: **n-type** **source** & **drain** **diffusion regions**; **electrons** as carriers in the **channel**
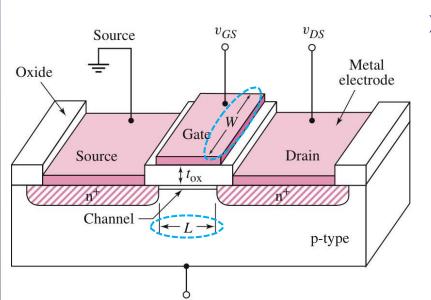
pMOS: **p-type** **diffusion regions**; **holes** as carriers in the **channel**

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MOSFET from MOS Capacitor

(conduction between source & drain)

❑ When an appropriate voltage is applied to the gate, a ***conducting* channel** is formed between the **source** and **drain**.

From: Donald A. Neamen, *Microelectronics: Circuit Analysis & Design*, 4th edition, © 2010 McGraw-Hill, USA.

➢ The ***conducting* channel** is simply the **inversion layer** in the MOS capacitor.

➢ The distance between the **source** and **drain** regions is called the **channel length** which is essentially the same as the **gate length** (defined by geometry).

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MOSFET from MOS Capacitor
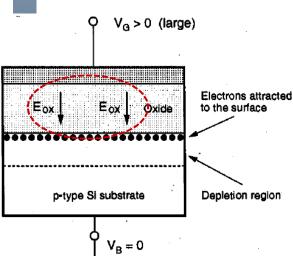## (conduction controlled by electric field)

❑ Depending on the applied gate voltage (as in the case of the **MOS capacitor**), the conduction between the source and drain regions can be controlled from strong to weak and even to cut-off.

From: S.-M. Kang & Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis & Design*, 3rd edition, © 2003 McGraw-Hill, USA.

➢ As the conduction is *controlled* by the **electric field** because of the voltage applied to the gate, which is insulated from the channel, it is named *field-effect* **transistor**. Note that there is no electric current flowing through the gate, in contrast to the bipolar junction transistor (BJT) case.

$V_G > 0$ (large)

E_{ox} E_{ox} Oxide

Electrons attracted to the surface

Depletion region

p-type Si substrate

$V_B = 0$

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MOSFETs

(3-terminal device)

❑ There are several variants of the MOSFET such as the **enhancement-mode** MOSFET which can be regarded as the normally-off transistor.

➢ Compared with the enhancement-mode MOSFET, the **depletion-mode** MOSFET can be regarded as the normally-on transistor.

❑ Looking at the basic structure of the MOSFET, it is a in fact a 4-terminal device. When used in CMOS circuits, two terminals (namely, the **source** and **body**) are typically connected together.

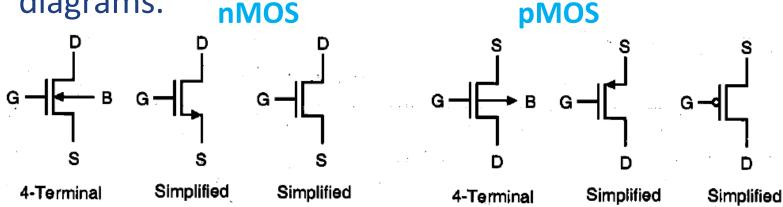➢ 4-terminal ⇒ 3-terminal device
➢ 3-terminal ⇒ 2-terminal?

MOSFETs

(circuit symbols)

❑ The **MOS field-effect transistors** (**MOSFET**s) are represented using circuit symbols in circuit diagrams.

nMOS

pMOS

4-Terminal   Simplified   Simplified   4-Terminal   Simplified   Simplified

➢ Note that the arrows in the MOSFETs' circuit symbols represent the current flow direction, as a sign of the *p-n* junction.
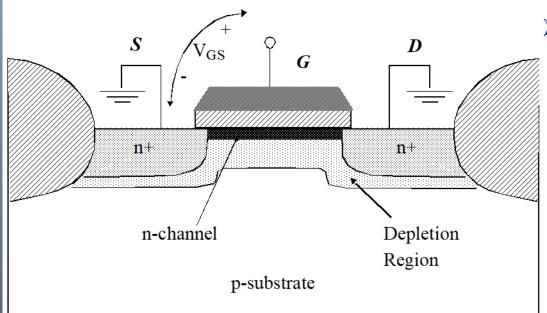
From: S.-M. Kang & Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis & Design*, 3rd edition, © 2003 McGraw-Hill, USA.

➢ Simplified symbols are used usually in digital circuits.

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MOSFET - as MOS Capacitor
(source/drain tied together)

❑ Regardless of the apparent complexity of the MOSFETs of various types or as a 4-terminal device, the **transistor operation** can be understood from the basic principles of the **MOS capacitor**.

➢ When the **source**, **drain** and **body** are connected together, the 4-terminal **MOSFET** becomes the 2-terminal **MOS capacitor**.

S V$_{GS}$ *G* *D*

n+   n-channel   n+   Depletion Region

p-substrate

B

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MOSFET's Operation Regions

(**I_{DS}** dependent on **V_{GS}** & **V_{DS}**)

❑ With the formation of the *conducting* **channel** controlled by the applied **gate voltage V_{GS}**, the current flow **I_{DS}** between the **source** and **drain** depends on the voltage **V_{DS}** applied across the two regions.

From: J. M. Rabaey et al., *Digital Integrated Circuits: A Design Perspective*, 2nd edition, © 2003 Pearson, USA.

➢ The current **I_{DS}** of the **MOSFET** in general is a function of **V_{GS}** and **V_{DS}**.

linear mode
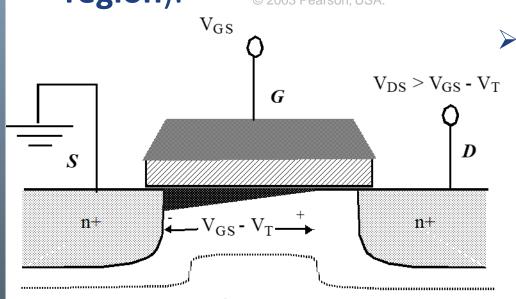
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MOSFET's Operation Regions

(channel pinch-off & saturation region)

❑ With the ***conducting* channel** formed between the **source** and **drain**, there are two major operation regions of the MOSFET: the **saturation region** and the **triode region** (which is also called the **linear region**).

From: J. M. Rabaey et al., *Digital Integrated Circuits: A Design Perspective*, 2nd edition, © 2003 Pearson, USA.

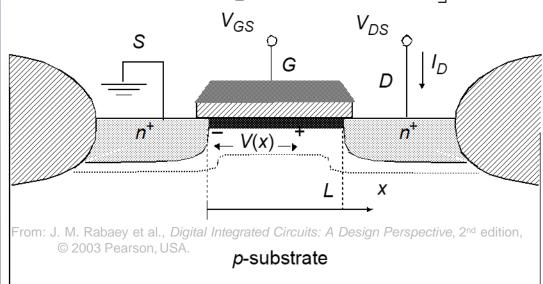➢ Note the different situations of the ***conducting* channel** in the **saturation region** and the **triode region**.

V_{GS}

$V_{DS} > V_{GS} - V_T$

G

S

D

n+

$V_{GS} - V_T$

n+

saturation mode

MOSFET's I-V Characteristics

(linear region)

❑ When $V_{GS} > V_T$ but with small V_{DS}, the current flow I_{DS} between the **source** and **drain** is roughly linearly dependent on the voltage V_{GS} & increases with V_{DS}.

$$I_{D,lin} = \mu_n C_{ox}\left(\frac{W}{L}\right)\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right] \text{ when } V_T \leq V_{GS} \text{ \& } V_{DS} \leq V_{GS} - V_T$$

➢ In the linear region, the **channel** is almost uniform from the source to drain.

From: J. M. Rabaey et al., *Digital Integrated Circuits: A Design Perspective*, 2nd edition, © 2003 Pearson, USA.

linear mode

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MOSFET's I-V Characteristics

(saturation region)

❑ In the **saturation region**, **pinch-off** of the channel occurs at the drain end and the current no longer increases with the V_{DS} in general.

$$I_{D,sat} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right) (V_{GS} - V_T)^2 \text{ when } V_T \leq V_{GS} \leq V_{DS} + V_T$$
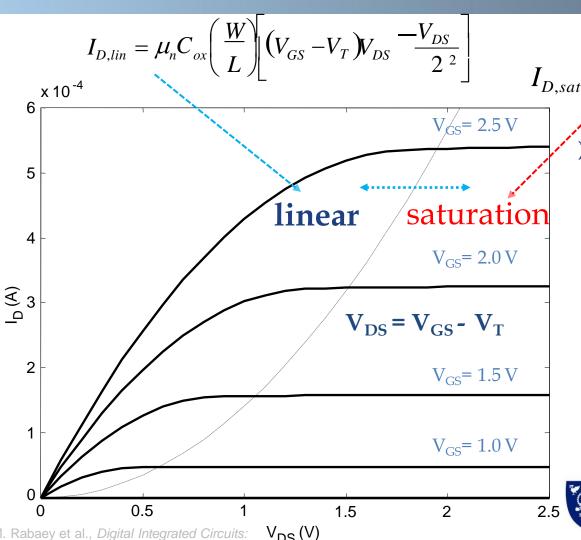
➢ The channel pinch-off occurs because of the reversed-biased **p-n** junction at the drain, **depleting** carriers as V_{DS} keeps increasing.

V_{GS}

$V_{DS} > V_{GS} - V_T$

G

S

D

n+ $V_{GS} - V_T$ n+

saturation mode

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MOSFET's I-V Characteristics

(output characteristics – I_{DS} vs. V_{GS})

$$I_{D,lin} = \mu_n C_{ox} \left(\frac{W}{L}\right)\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$I_{D,sat} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_T)^2$$

x 10^{-4}

V_{GS}= 2.5 V

linear saturation

V_{GS}= 2.0 V

$\mathbf{V_{DS} = V_{GS} - V_T}$

V_{GS}= 1.5 V

V_{GS}= 1.0 V

I_D (A)

V_{DS} (V)
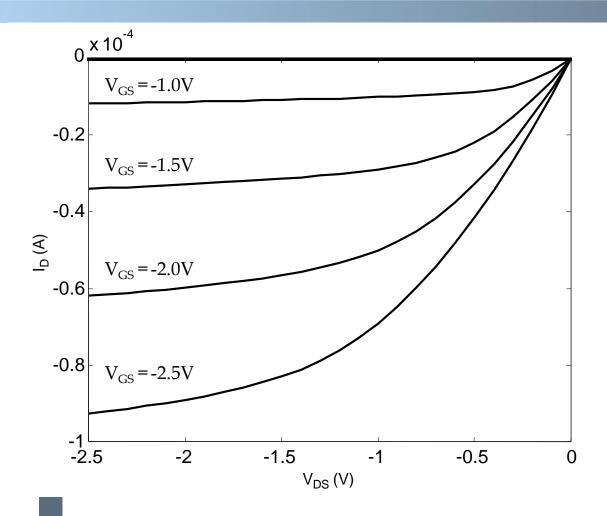
➢ This model for the drain current is not accurate, especially in CMOS technology with a short channel.

From: J. M. Rabaey et al., *Digital Integrated Circuits: A Design Perspective*, 2nd edition, © 2003 Pearson, USA.

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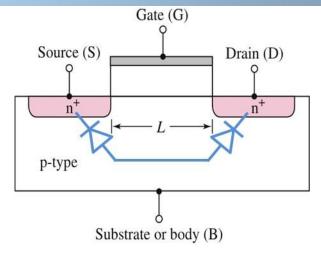
MOSFET's I-V Characteristics

(*p*-type MOSFET)

❑ The derived equations for the nMOS transistor are applicable to the pMOS transistors but with the **polarities** of all **voltages** and **currents** reversed.
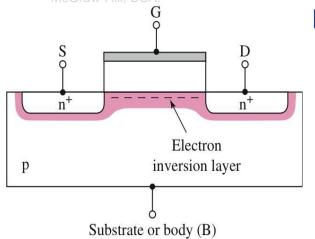
From: J. M. Rabaey et al., *Digital Integrated Circuits: A Design Perspective*, 2nd edition, © 2003 Pearson, USA.

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MOS Field-Effect Transistor

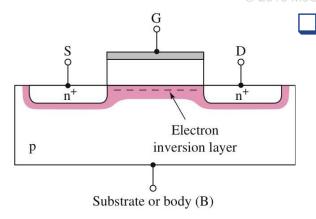## (basic transistor operation)

From: Donald A. Neamen, *Microelectronics: Circuit Analysis & Design*, 4th edition, © 2010 McGraw-Hill, USA.

❑ With zero bias applied to the gate, there is no electrical conduction between the source and drain terminals.

  ➢ This is equivalent to two diodes connected in series but of opposite direction to each other.

❑ When a large enough voltage is applied to the gate, an **inversion layer** is created and *channels* the source & drain terminals.

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MOS Field-Effect Transistor

(basic transistor operation)

❑ With the **inversion layer** as a ***channel***, electric current can be generated between the **source** and **drain** terminals if a voltage is applied to the two terminals. From: Donald A. Neamen, *Microelectronics: Circuit Analysis & Design*, 4th edition, © 2010 McGraw-Hill, USA.

❑ Since a voltage must be applied to the gate to create the **inversion layer**, this type of transistors is called **enhancement-mode MOSFETs**.

❑ It is called an ***n*-channel** MOSFET (or **nMOSFET**) if the carriers of the **inversion layer** are **electrons**; (**pMOSFET** for holes.)

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MOS Field-Effect Transistor

(channel & current)

❑ In an **n**MOSFET, electrons flow from the **source** to the **drain** if a drain-to-source voltage is applied to the two terminals.

➢ This means that the conventional current enters the drain and leaves the source in an **n**MOSFET.

❑ The magnitude of the current depends on the amount of charge in the **inversion layer**.

$$J_{drift} = \sigma E = (en\mu_n + ep\mu_p)E$$

❑ Since the gate terminal is electrically separated from the **channel** by a thin oxide or insulator layer, there is no gate current in MOSFETs.

➢ The **channel** is also separated from the substrate by the depletion region $\Rightarrow$ no current through the substrate *essentially*.

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Threshold Voltage of MOSFETs

("turn-on" voltage)

❑ Since current conduction between the source and drain depends on the channel formation, the **threshold voltage**, denoted by V_{TN} for **n**MOSFETs (V_{TP} for pMOSFETs), is defined:

➤ the applied **gate voltage** needed to create the inversion layer in which the carrier density is equal to the concentration of the majority carrier in the semiconductor substrate.

➤ In simple terms, it is the **gate voltage** required to "**turn on**" the MOSFETs.

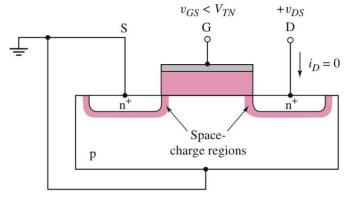➤ For enhancement-mode **n**MOSFETs, V_{TN} is a positive gate voltage;

➤ V_{TP} is a negative gate voltage for **p**MOSFETs.

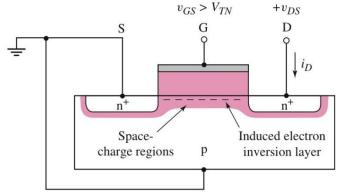Xi'an Jiaotong-Liverpool University
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Threshold Voltage of MOSFETs
(drain current)

❑ In **n**MOSFETs, the **source** and the substrate are usually connected to the ground (i.e. 0 V).

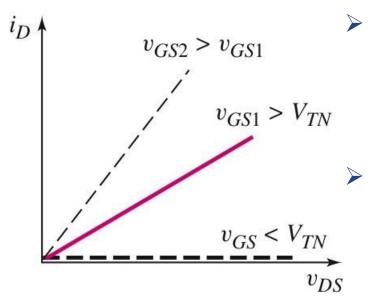From: Donald A. Neamen, *Microelectronics: Circuit Analysis & Design*, 4th edition, © 2010 McGraw-Hill, USA.

➢ When the gate-to-source voltage v_{GS} is smaller than V_{TN}, there is no inversion layer.

$\Rightarrow$ no drain current *essentially* even with a drain-to-source voltage v_{DS}.

➢ When $v_{GS} > V_{TN}$, an inversion layer is created and there is a drain current i_D with an applied *small* v_{DS}.

I-V Characteristics of MOSFETs

(drain current for small enough v_{DS})

❑ When $v_{GS} < V_{TN}$, the drain current i_D is <u>*essentially*</u> 0.

❑ When $v_{GS} > V_{TN}$, i_D increases with the applied v_{DS} up to a certain point.

From: Donald A. Neamen, *Microelectronics: Circuit Analysis & Design*, 4th edition, © 2010 McGraw-Hill, USA.
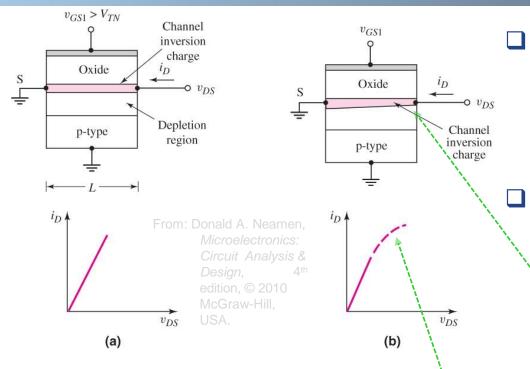
➢ For a larger $v_{GS2} > V_{TN}$, the inversion layer has a larger charge carrier density. Hence, i_D is larger for a given value of v_{DS}.

➢ The increase in i_D *almost linearly* with v_{DS} is only valid for small v_{DS}. This region of MOSFET operation is called the **triode region**.

Note the **voltage notation** of e.g. v_{DS} with the dual subscript, which denotes the voltage between the drain (D) and source (S), with the 1st subscript (D) being the positive voltage and the 2nd subscript (S) being the negative voltage (i.e. v_D - v_S).

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I-V Characteristics of MOSFETs

(triode region)

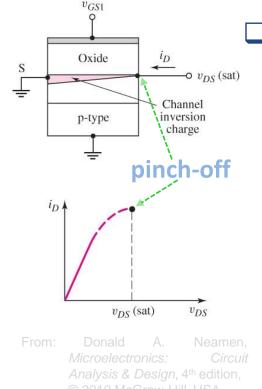From: Donald A. Neamen, *Microelectronics: Circuit Analysis & Design*, 4th edition, © 2010 McGraw-Hill, USA.

❑ When $v_{GS} > V_{TN}$ and *small enough* v_{DS}, i_D increases with the applied v_{DS}. (Fig. (a))

❑ As v_{DS} increases further, the voltage drop across the oxide (i.e. v_{GD}) near the drain decreases.

❑ As a result, the induced **inversion layer** near the drain has a lower charge carrier density (Fig. (b)).

  ➢ The incremental conductance of the channel near the drain then decreases (i.e. $\Delta i_D / \Delta v_{DS}$ decreases).

$$J_{ndrift} = \sigma_n E = (en\mu_n)E$$

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I-V Characteristics of MOSFETs

(pinch-off region)

pinch-off

From: Donald A. Neamen, *Microelectronics: Circuit Analysis & Design*, 4th edition, © 2010 McGraw-Hill, USA.
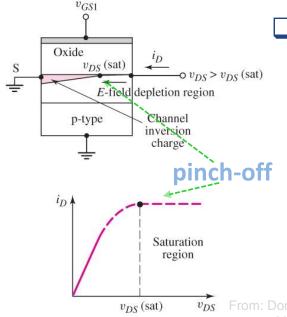
❑ As v_{DS} increases to the point that the voltage drop across the oxide at the drain (i.e. $v_{GD} = v_{GS} - v_{DS}$) is equal to V_{TN}, the induced **inversion** carrier density is <u>zero</u> at the drain.

➢ The MOSFET is said to be at the **pinch-off** condition when $v_{GS} - v_{DS} = V_{TN}$.

➢ The incremental conductance of the channel at the drain becomes zero (i.e. $\Delta i_D / \Delta v_{DS} = 0$ *ideally*).

❑ A voltage $v_{DS(sat)}$ is defined when the **inversion layer** starts to be *pinched off* at the drain:

$$v_{DS(sat)} = v_{GS} - V_{TN}$$

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I-V Characteristics of MOSFETs
(saturation region)

pinch-off

❑ When v_{DS} increases beyond $v_{DS(sat)}$, the **pinch-off** point (at which the inversion charge is just zero) moves toward the source terminal.

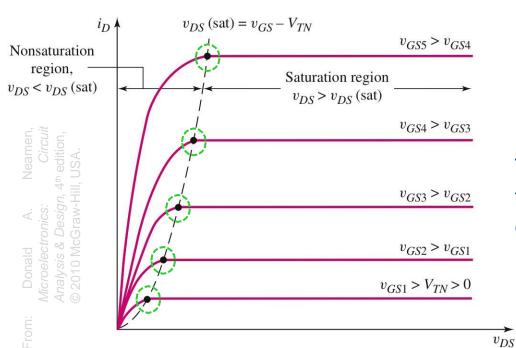 ➤ This is called the **saturation region** of the MOSFET when $v_{DS} > v_{DS(sat)}$.

❑ In the **saturation region** of an nMOSFET, electrons enter the channel at the **source** and travel through the **channel** toward the **drain**, and then at the point where the inversion carrier density goes to zero, are injected into the E-**field depletion region** and are *swept* to the **drain**.

I-V Characteristics of MOSFETs

(*I-V* curves)

❑ The dependence of the **drain current i_D** on the applied **gate-to-source voltage v_{GS}** and the **drain-to-source voltage v_{DS}** can be reflected in a family of i_D - v_{DS} curves.

➢ Note that $v_{DS(sat)}$ is a function of the applied v_{GS}.

$\Rightarrow$ the voltage $v_{DS(sat)}$ is a single point on each of the i_D - v_{DS} curve.

The *I-V* curves shown on the left is of an **enhancement-mode n**MOSFET (based on V_{TN}).

From: Donald A. Neamen, *Microelectronics: Circuit Analysis & Design*, 4th edition, © 2010 McGraw-Hill, USA.

i_D
v_{DS} (sat) = $v_{GS} - V_{TN}$
$v_{GS5} > v_{GS4}$
Nonsaturation region, $v_{DS} < v_{DS}$ (sat)
Saturation region $v_{DS} > v_{DS}$ (sat)
$v_{GS4} > v_{GS3}$
$v_{GS3} > v_{GS2}$
$v_{GS2} > v_{GS1}$
$v_{GS1} > V_{TN} > 0$
v_{DS}

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I-V Characteristics of MOSFETs
(mathematical relationship)

❑ The i_D - v_{DS} characteristics of the MOSFET can be derived from fundamental principles but the derivation is not required in this class. The mathematical relationships are simply given here.

➢ In the **triode region** (also called non-saturation region) where v_{DS} < $v_{DS(sat)}$, $i_D = K_n \left[2\left(v_{GS} - V_{TN}\right)v_{DS} - v_{DS}^2 \right]$

➢ In the **saturation region** where v_{DS} > $v_{DS(sat)}$,

$$i_{Dsat} = K_n \left[(v_{GS} - V_{TN})^2 \right]$$

i_{Dsat} can be obtained by setting v_{DS} = (v_{GS} - v_{TN}) in the 1st eqn.

➢ where K_n is referred as the conduction parameter for simplicity:

$$K_n = \left(\tfrac{1}{2}\right)\mu_n C_{ox}\left(\frac{W}{L}\right) = k_n' \frac{W}{L}$$

$C_{ox} = \varepsilon_{ox} / t_{ox}$ being the MOS **capacitance per unit area** and

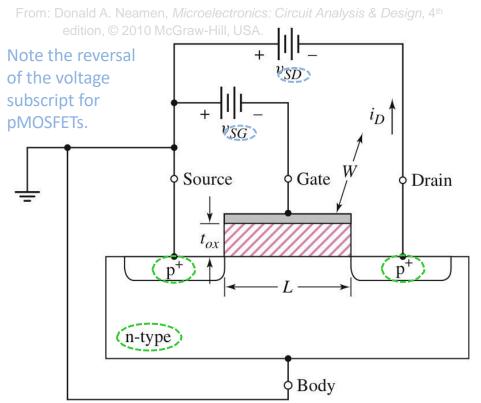$\varepsilon_{ox} = (3.9)(8.85 \times 10^{-12})$ F/m for SiO$_2$

➢ Note that K_n is a function of both electrical & geometrical parameters.

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p-type MOSFET
(*p*-channel)

❑ The complementary transistor of the *n*-channel MOSFET is a *p*-channel MOSFET.

➢ The transistor structure and operation are similar.

From: Donald A. Neamen, *Microelectronics: Circuit Analysis & Design*, 4th edition, © 2010 McGraw-Hill, USA.

Note the reversal of the voltage subscript for pMOSFETs.
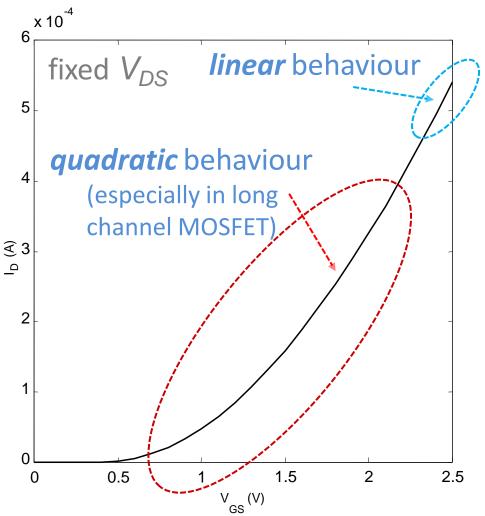

➢ The differences are:

the substrate is *n*-type and the S/D regions are *p*-type for pMOSFET;

holes are the charge carrier in the **channel**;

the threshold voltage is negative (i.e. $V_{TP} < 0$).

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I-V Characteristics of MOSFETs

(transfer characteristics – I_{DS} vs. V_{GS})

fixed V_{DS}

linear behaviour
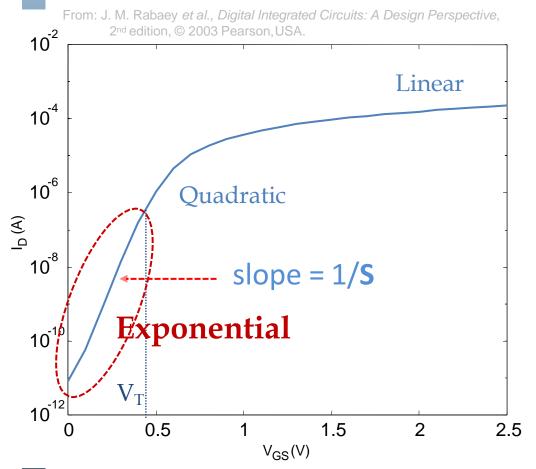
quadratic behaviour
(especially in long channel MOSFET)

- ❑ The device behaviour of the MOSFET (e.g. short-channel transistors) can be revealed more by the **transfer characteristics**.
  - ➢ quadratic or linear dependence of I_{DS} on V_{GS}

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I-V Characteristics of MOSFETs
(sub-threshold conduction)

❑ It can be more obvious in the semi-logarithmic scale.

From: J. M. Rabaey *et al.*, *Digital Integrated Circuits: A Design Perspective*, 2nd edition, © 2003 Pearson, USA.

❑ Note the **exponential** dependence of I_{DS} on V_{GS} below the threshold voltage V_T.

❑ It is **sub-threshold conduction** of the MOSFET.

Sub-threshold Conduction
(60 mV per decade)

❑ The inverse of the slope in the **exponential** dependent part of the curve in semi-log scale is called the **sub-threshold swing S**.

➤ S is ΔV_{GS} for I_{DS2}/I_{DS1} =10.

➤ Typical values for S are from 60 to 100 **mV/decade**.

➤ It tells how well the MOSFET can be turned off (i.e. with almost no current I_{DS} in the off state).

$$I_D \approx I_0 e^{\frac{qV_{GS}}{nkT}} \text{ when } V_{GS} < V_T, \quad n = 1 + \frac{C_D}{C_{ox}}$$

$$S = n\left(\frac{kT}{q}\right)\ln(10)$$

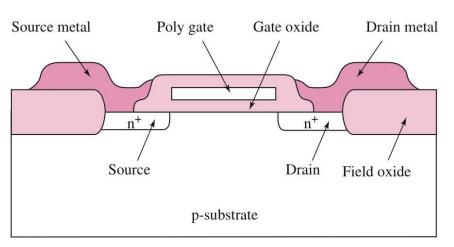Xi'an Jiaotong-Liverpool University
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MOSFET: weak & strong inversion

(leakage current implication)

❑ **Strong Inversion** $V_{GS} > V_T$:

  ➤ linear region (resistive) $V_{DS} < V_{DSAT}$

  ➤ saturated (constant current) $V_{DS} \geq V_{DSAT}$

❑ **Weak Inversion** (**sub-threshold**) $V_{GS} \leq V_T$

  ➤ Exponential in V_{GS} with linear V_{DS} dependence

❑ The **weak inversion** has the implication of the off-state <u>leakage current</u> of the MOSFETs.

  ➤ 0.1 nA for each transistor $\Rightarrow$ 1 A for a chip of 10 billion transistors! $\Rightarrow$ high power dissipation even when the circuits are supposed to be turned off.

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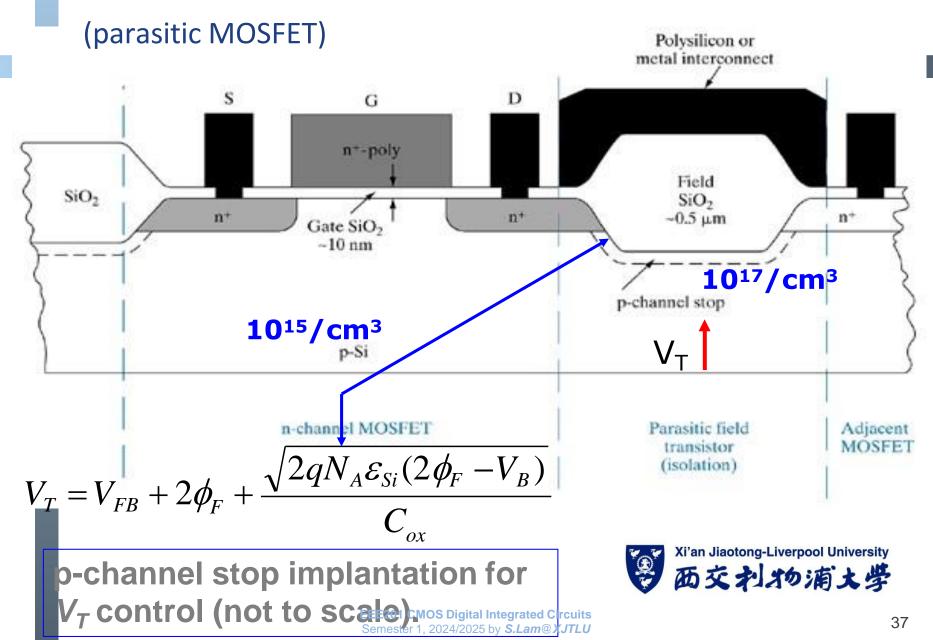西交利物浦大学

MOS Field-Effect Transistor

(actual structure)

❑ In integrated circuits (ICs), the actual MOSFET structure is somewhat more complex.

➤ The gate material is heavily-doped polysilicon of high conductivity comparable to that of metal.

➤ A thick oxide, called the **field oxide**, is deposited outside the device area to isolate from neighbouring MOSFETs.

➤ In commercial IC fabrication, the gate length L is typically smaller than 1 µm (10^{-6} m). The gate oxide thickness is $t_{ox} < 10$ nm.

➤ See MOSIS (www.mosis.com)

From: Donald A. Neamen, *Microelectronics: Circuit Analysis & Design*, 4th edition, © 2010 McGraw-Hill, USA.

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MOS Field-Effect Transistor

(parasitic MOSFET)

$10^{17}/cm^3$

V_T

$10^{15}/cm^3$

$$V_T = V_{FB} + 2\phi_F + \frac{\sqrt{2qN_A\varepsilon_{Si}(2\phi_F - V_B)}}{C_{ox}}$$

p-channel stop implantation for V_T control (not to scale)

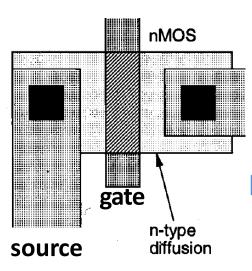Xi'an Jiaotong-Liverpool University
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Layout of MOSFET
(nMOS & pMOS)

❑ Although the actual structure of the MOSFET varies for different fabrication processes, the physical layout of the nMOS and pMOS transistors remain almost the same.
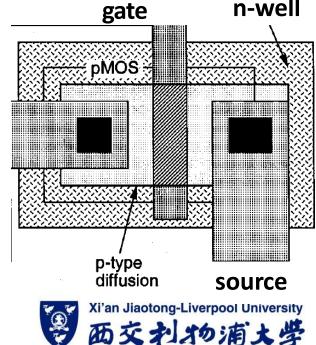
From: S.-M. Kang & Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis & Design*, 3rd edition, © 2003 McGraw-Hill, USA.
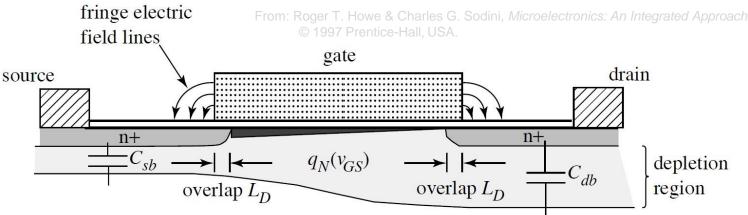
nMOS

drain

gate

source

n-type diffusion

drain

gate

n-well

pMOS

source

p-type diffusion

Note the difference in the layout area of the nMOS & pMOS transistors

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Capacitances of MOSFET
(speed of digital circuits)

❑ In using the MOSFETs as switches to build logic circuits, we want high switching speed for faster logic circuits.

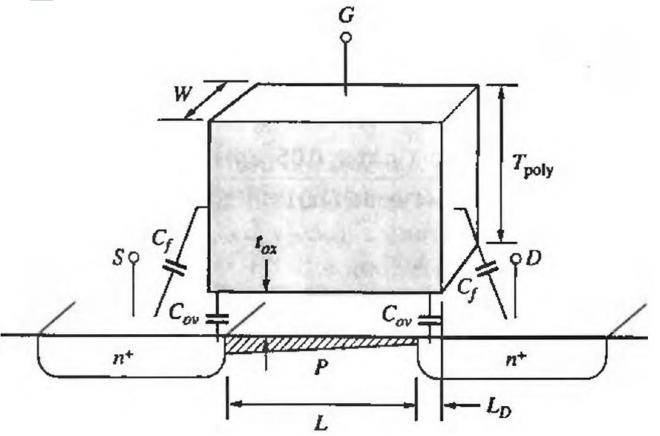❑ The speed of CMOS digital circuits is limited also by the **capacitances** associated with the MOSFET.

From: Roger T. Howe & Charles G. Sodini, *Microelectronics: An Integrated Approach,* © 1997 Prentice-Hall, USA.

➤ associated with the gate & junctions

Capacitances of MOSFET
(associated with the gate)

From: D.A. Hodges *et al.*, *Analysis and Design of Digital Integrated Circuits: In Deep Submicron Technology*, 3rd edition, © 2003 McGraw Hill, USA.

❑ **Capacitances** associated with the gate electrode consist of the **fringing capacitance** C_f and the **overlapping capacitance** C_{ov} besides

the dominant gate oxide capacitance $C_{ox} = \varepsilon_{ox}/t_{ox}$.

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Gate Capacitance of MOSFET

(estimation using the layout)

Polysilicon gate

Source

n^+

x_d

x_d

Drain

W

n^+

L_d

Gate-bulk overlap

top view

Gate oxide

t_{ox}

n^+

L

n^+

cross section

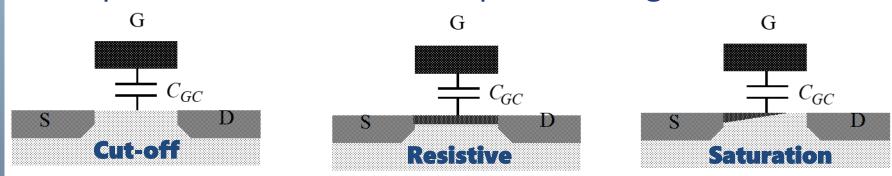❑ The capacitance associated with the gate oxide can be estimated with the physical layout of the MOSFET, with the transistor sizes (**W** & **L**) fixed:

$$C_{gate} = \left(\frac{\varepsilon_{ox}}{t_{ox}} \right) WL$$

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Gate Capacitances of MOSFET
(dependent on operation regions)

❑ The actual **gate capacitances** of the MOSFET depends on the transistor operation regions.

G C_{GC} S D **Cut-off** · G C_{GC} S D **Resistive** · G C_{GC} S D **Saturation**

From: J. M. Rabaey *et al.*, *Digital Integrated Circuits: A Design Perspective*, 2nd edition, © 2003 Pearson, USA.

Operation Region	C_{gb}	C_{gs}	C_{gd}
Cutoff	$C_{ox}WL_{eff}$	0	0
Triode	0	$C_{ox}WL_{eff}/2$	$C_{ox}WL_{eff}/2$
Saturation	0	$(2/3)C_{ox}WL_{eff}$	0

➢ C_{GC}: gate-to-channel capacitance

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Capacitances of MOSFET
(associated with diffusion regions)

Channel-stop implant N_{A^1}

Side wall

Source N_D

Bottom

W

x_j

Side wall

L_S

Channel

Substrate N_A

From: J. M. Rabaey *et al.*, *Digital Integrated Circuits: A Design Perspective*, 2nd edition, © 2003 Pearson, USA.

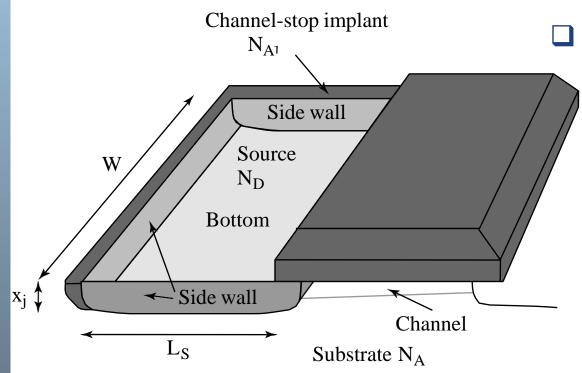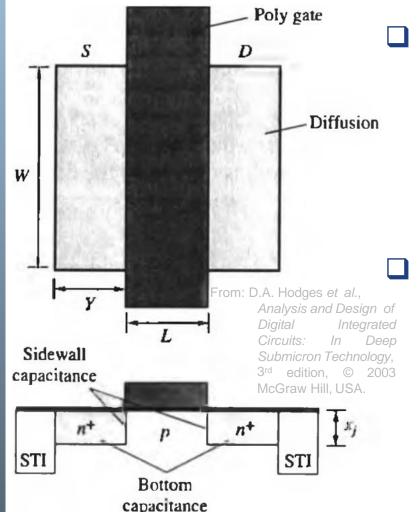❑ The **source** and **drain diffusion regions** inherently contain *parasitic p-n* junctions which give rise to junction capacitances with one component dependent on area & other perimeter.

$$C_{diff} = C_{bottom} + C_{sw} = C_j \times AREA + C_{jsw} \times PERIMETER$$
$$= C_j L_S W + C_{jsw}(2L_S + W)$$

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Diffusion Region Capacitances

(*p-n* junction capacitance)

Poly gate

S

D

Diffusion

W

Y

From: D.A. Hodges *et al.*, *Analysis and Design of Digital Integrated Circuits: In Deep Submicron Technology*, 3rd edition, © 2003 McGraw Hill, USA.

L

Sidewall capacitance

n^+ p n^+ x_j
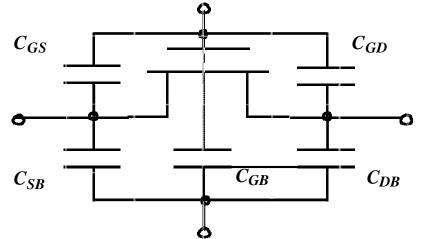
STI   STI

Bottom capacitance

❑ In the *parasitic* ***p-n*** junctions of the **source** and **drain diffusion regions**, the junction boundary is a curved surface.

❑ To estimate the diffusion region capacitance from the physical layout, the ***sidewall*** part is estimated by the perimeter.

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Capacitances of MOSFET
(model for better speed estimation)

❑ In CMOS digital ICs, it is desirable to keep the capacitances minimum in the IC layout design.

❑ Even when the capacitances may not be minimised, they need to be modelled properly.

From: J. M. Rabaey *et al.*, *Digital Integrated Circuits: A Design Perspective*, 2nd edition, © 2003 Pearson, USA.

➢ With the capacitances included properly in the MOSFET model, the **circuit speed** of the digital ICs can be more accurately estimated even before chips are made.

G

C_{GS} C_{GD}

S D

C_{SB} C_{GB} C_{DB}

B

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