

EEE205 – Digital Electronics (II)

Lectures 1-2

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XJTLU

This Module

Contents:

1. Programmable Logic Devices (PLDs)
2. Hardware Description Languages (HDLs)
3. Large Combinational and Sequential Circuits
4. Algorithmic State Machines (ASMs)
5. Processor Interface Circuits

Assessment:

Final exam (80%)

Assignments (10%)

Lab (10%)

Teaching Plan

Dr. Xiaoyang Chen

Week 1: Lectures 1-2

Week 2: Lectures 3-4

Week 3: Lecture 5-6

Week 4: Lectures 7-8
(Ass1 Release)

Office Hours:
Every Thursday 14:00
- 16:00

Dr. Jiangmin Gu

Week 5: Lectures 9-10

Week 6: Lecture 11
(Ass2 Release)

Week 7: Non-teaching

Week 8: Lecture 12, FB
on Ass1 **(Lab)**

Week 9: Lectures 13-14
(Ass3 Release)

Dr. Ming Xu

Week 10: Lectures 15-16

Week 11: Lecture 17, FB
on Ass 2

Week 12: Lecture 18, FB
on Ass 3

Week 13: Revision

In This Session

- Introduction to Programmable Logic Devices (PLDs)
- Programmable Array Logic (PAL)
- Generic Array Logic (GAL)

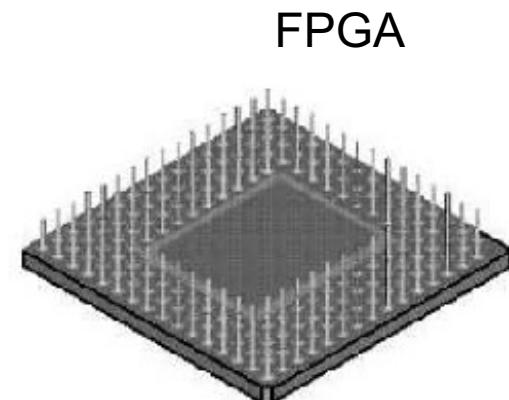
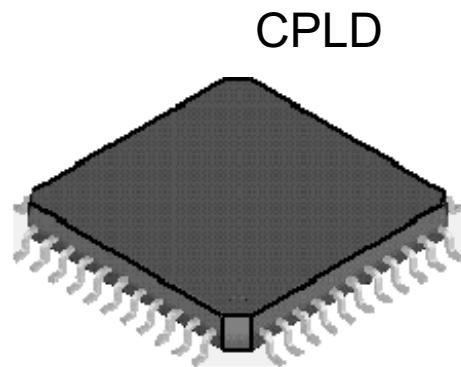
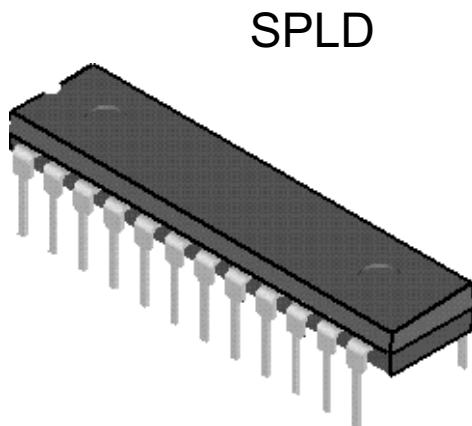
Programmable Logic Devices (PLDs)

- PLDs can be used to implement combinational and sequential logic circuits.
- They can replace logic devices, resulting in fewer parts, lower cost and less space.
- The logic design in PLDs are implemented with programming software.

Programmable Logic Devices (PLDs)

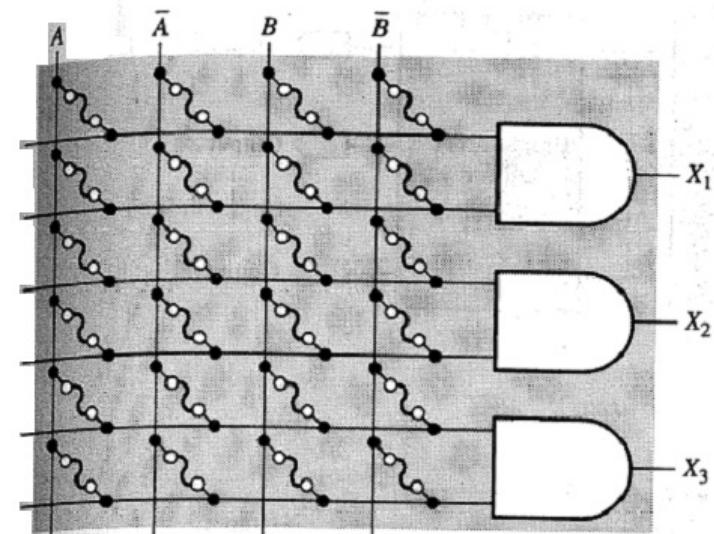
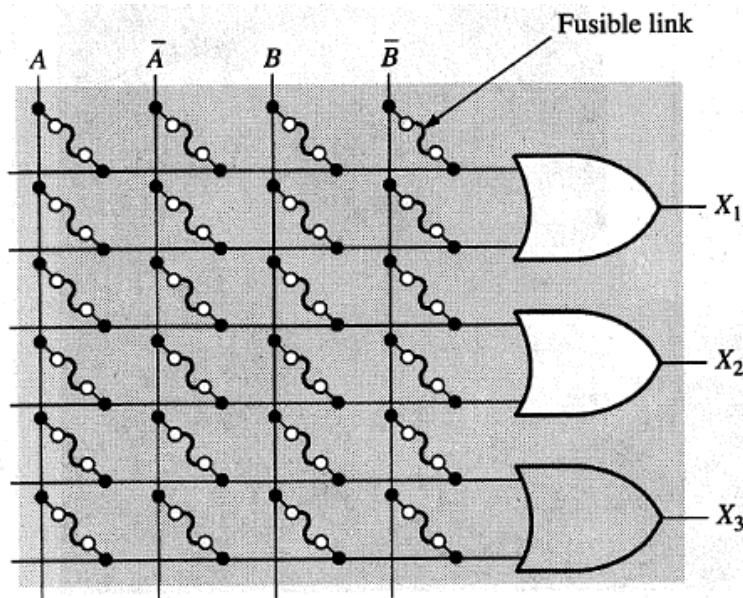
Types (*equivalent gates*: 2-input NAND gates)

- SPLDs — Simple Programmable Logic Devices, up to 600 *equivalent gates* each.
- CPLDs — Complex Programmable Logic Devices, up to thousands of *equivalent gates* each.
- FPGAs — Field Programmable Gate Arrays, hundreds of thousands of *equivalent gates* each.



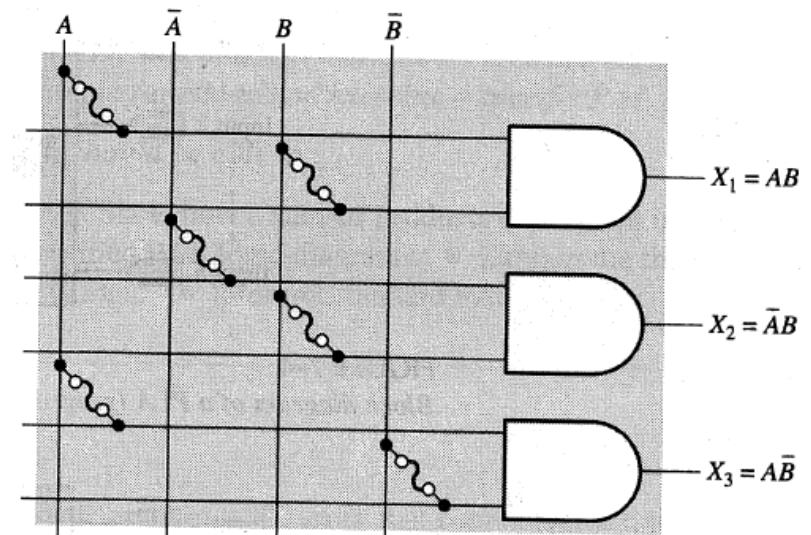
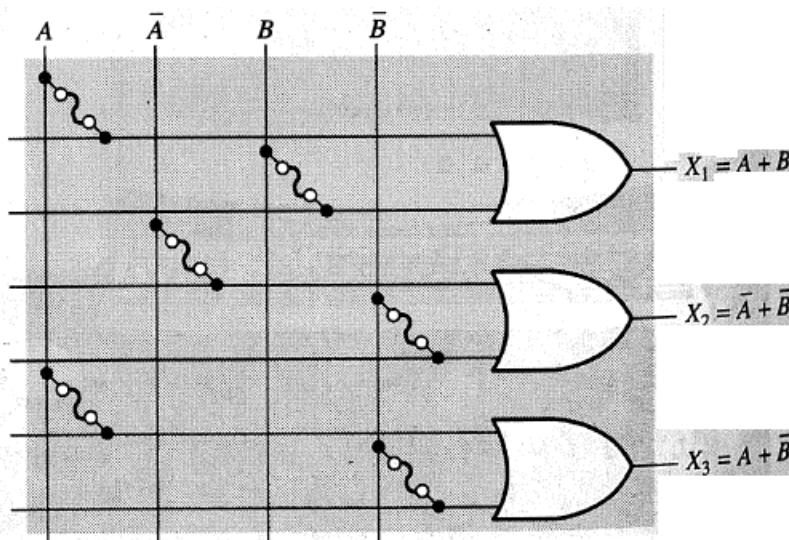
Programmable Arrays

- All SPLDs consist of programmable arrays.
- A *programmable array* is a grid of conductors that form rows and columns with a fusible link at each cross point.



Programmable Arrays

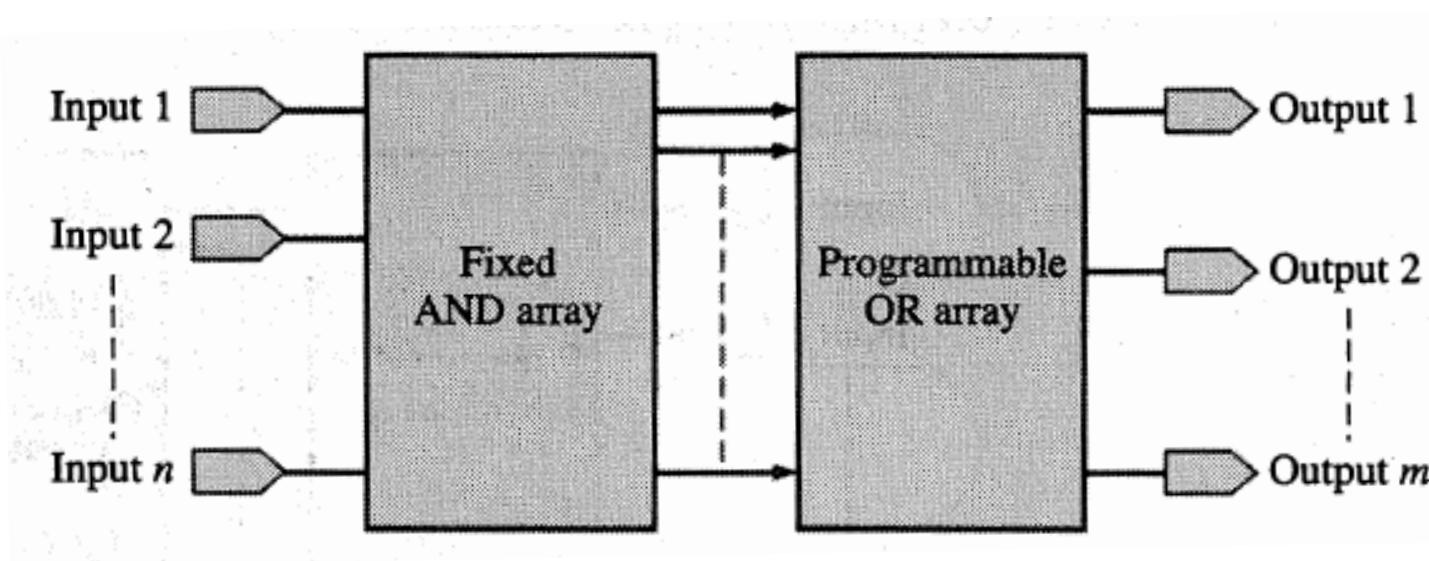
- The array is programmed by blowing fuses to eliminate selected variables from the output.
- An array can be fixed, one-time programmable or re-programmable.



Classifications of SPLDs

1. Programmable Read-Only Memory (PROM)

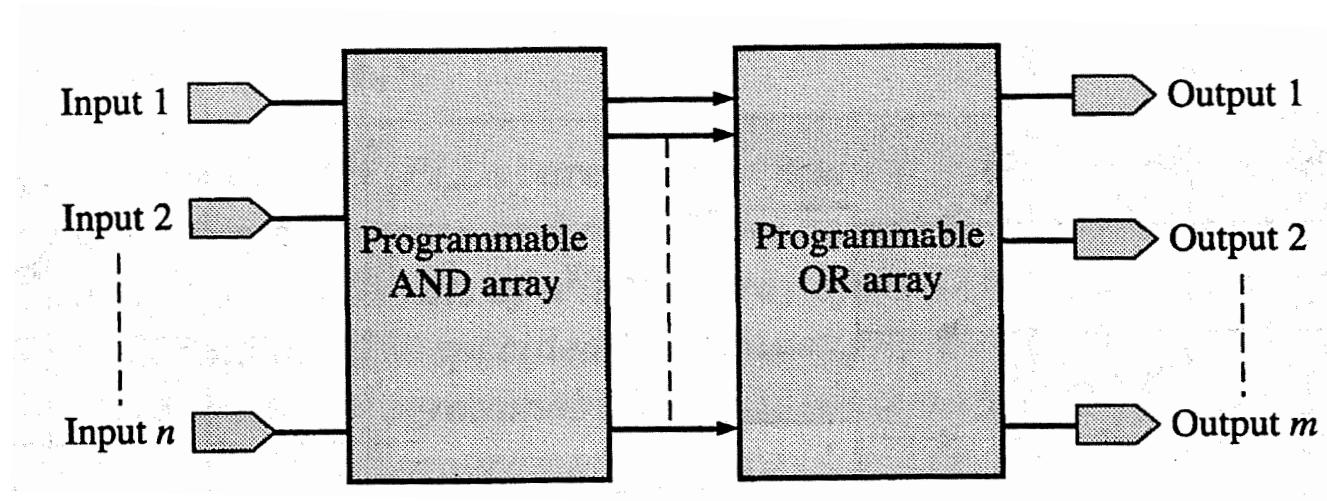
It consists of a fixed AND array and a programmable OR array.



Classifications of SPLDs

2. Programmable Logic Array (PLA)

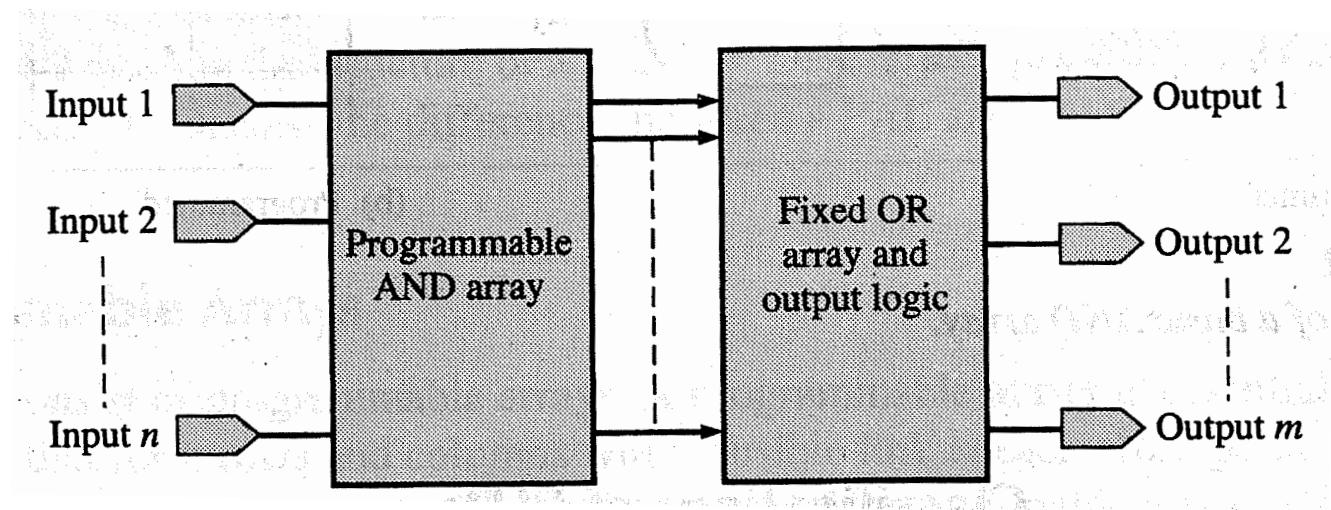
It consists of a programmable AND array and a programmable OR array.



Classifications of SPLDs

3. Programmable Array Logic (PAL)

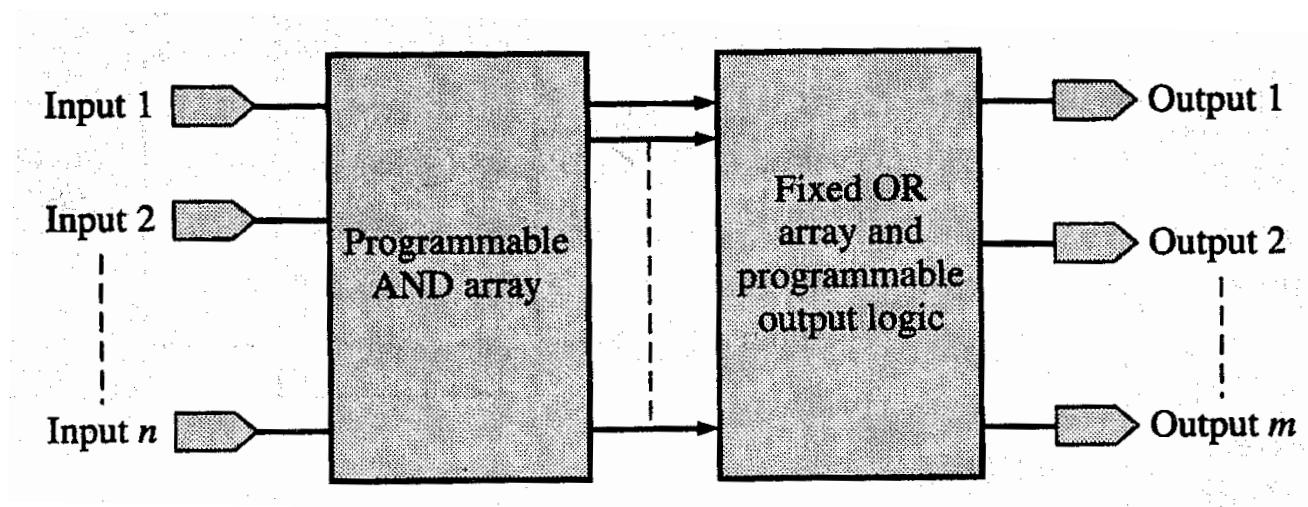
It consists of a one-time programmable AND array and a fixed OR array with output logic.



Classifications of SPLDs

4. Generic Array Logic (GAL)

It consists of a reprogrammable AND array and a fixed OR array with programmable output logic.

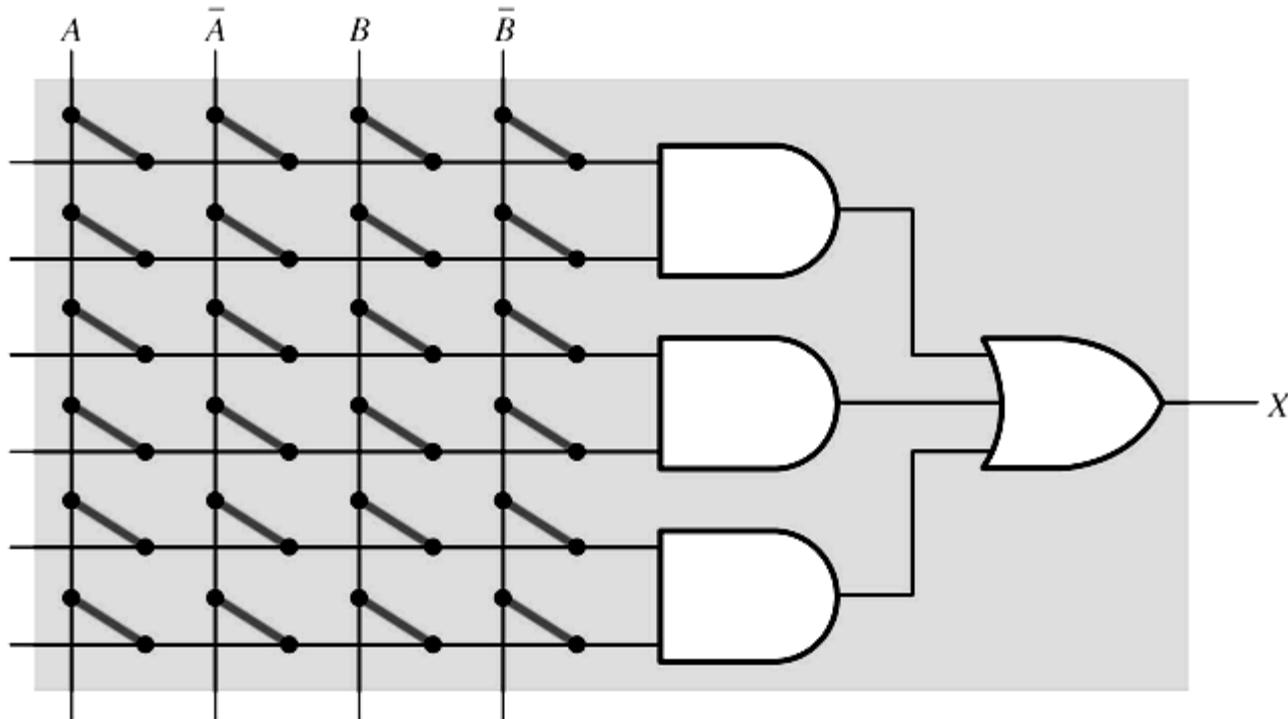


Classifications of SPLDs

- The PAL and the GAL are the most common PLDs used for logic implementation.
- The main differences between them lie in:
 - The GAL is reprogrammable.
 - The GAL has programmable output logic.

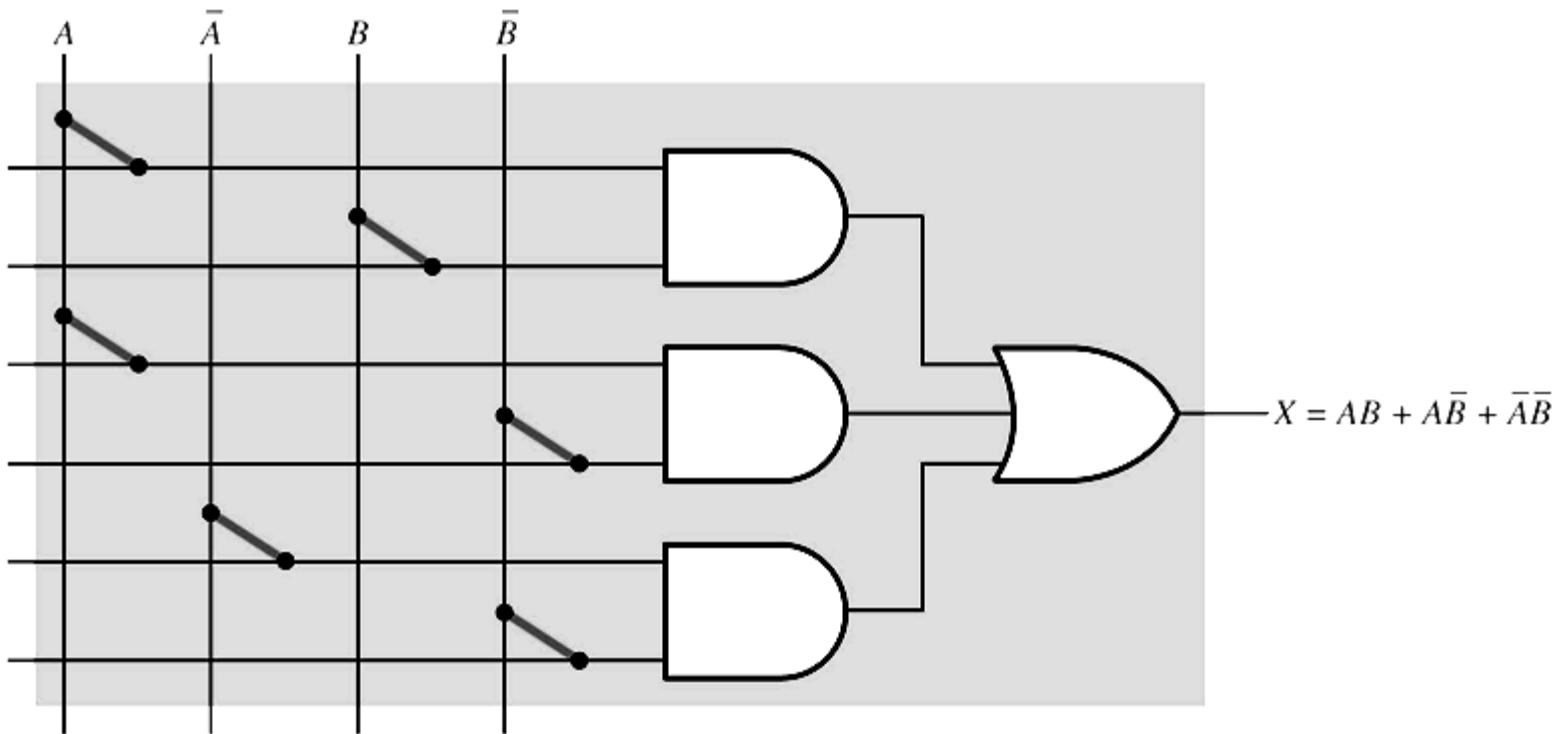
Programmable Array Logic (PAL)

- Its AND/OR structure allows any sum-of-products (SOP) logic expression, not limited to 2 input variables as shown here.
- Any logic function can be expressed in SOP form.



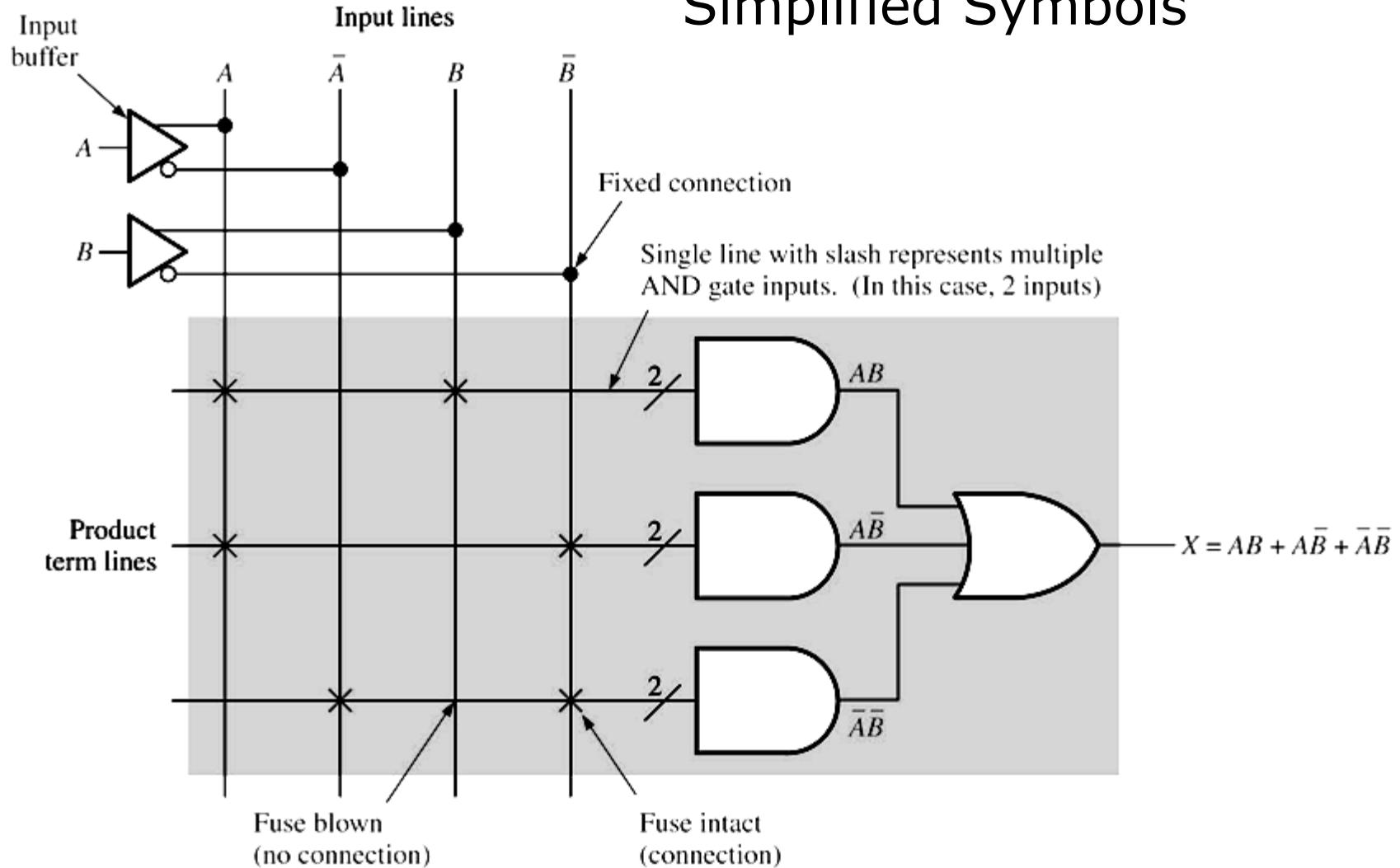
Programmable Array Logic (PAL)

- When the connection is required, the fuse is left intact.
- Otherwise it is blown open during programming.



Programmable Array Logic (PAL)

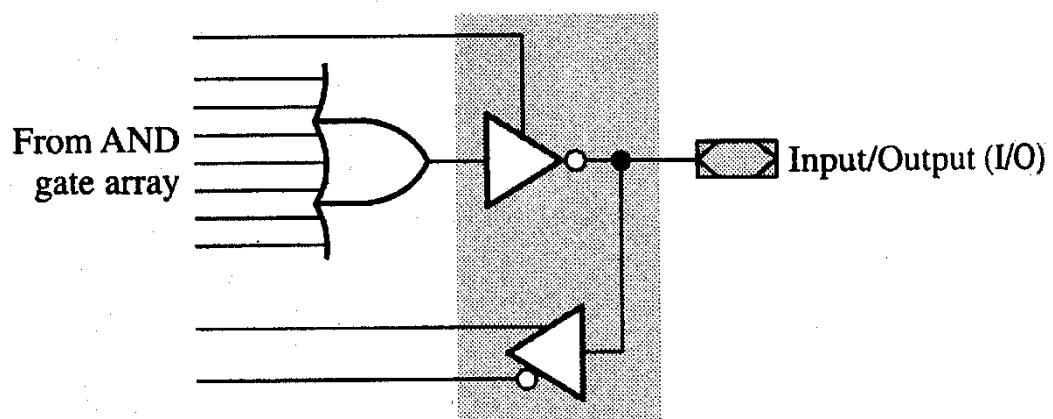
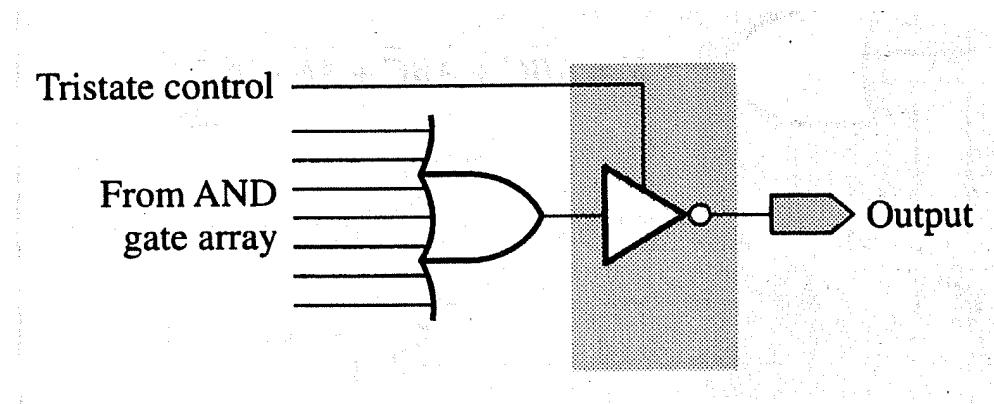
Simplified Symbols



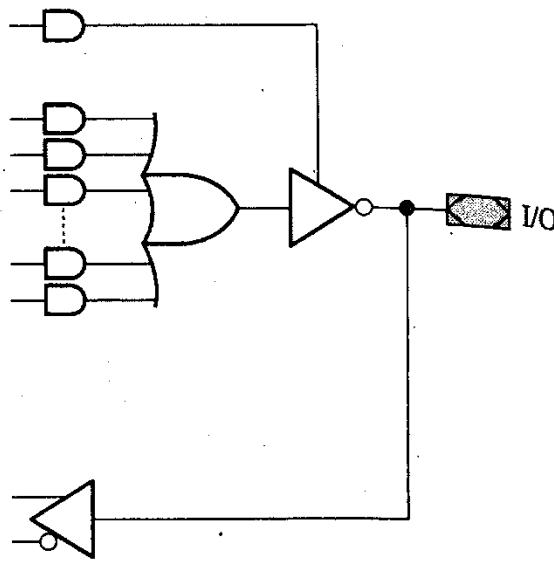
Programmable Array Logic (PAL)

PAL Output Logic

- The output is buffered and can be either active-LOW or active-HIGH.
- The I/O pin can be used as an input or the feedback of an output.

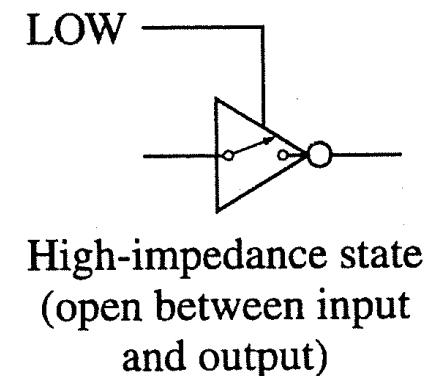
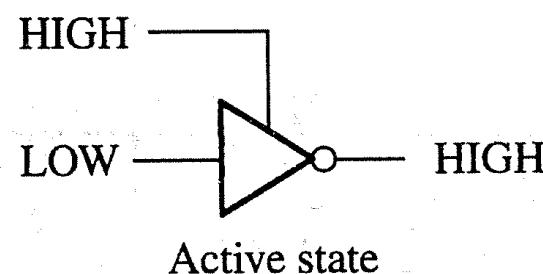
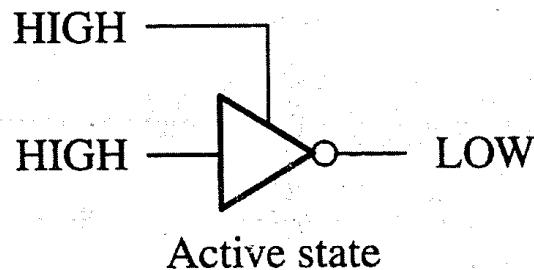


Programmable Array Logic (PAL)



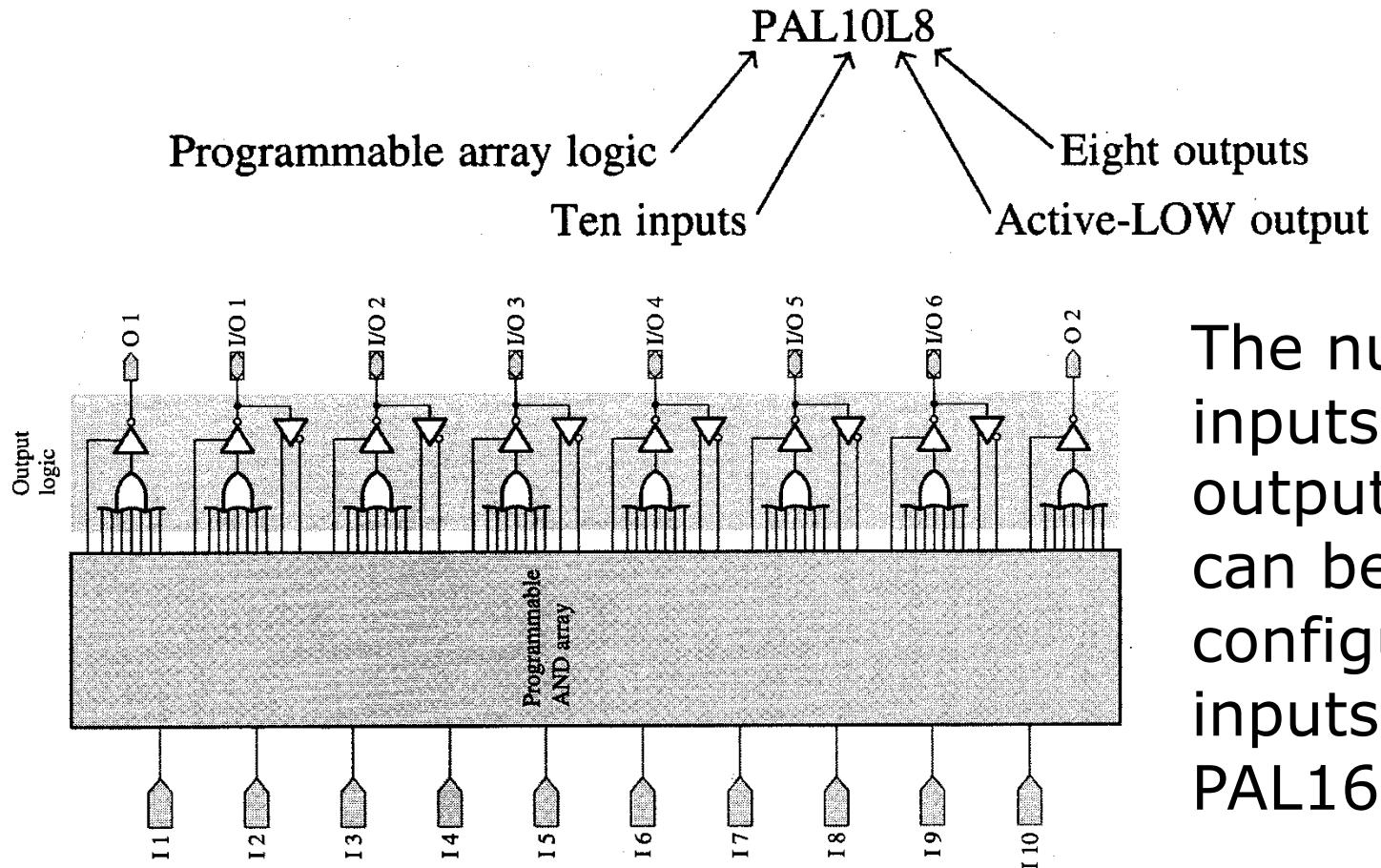
The tristate buffer:

- When the control line is HIGH, the I/O pin is an output which is fed back to the AND array.
- When the control line is LOW, the I/O pin is an input.



Programmable Array Logic (PAL)

Standard PAL Numbering

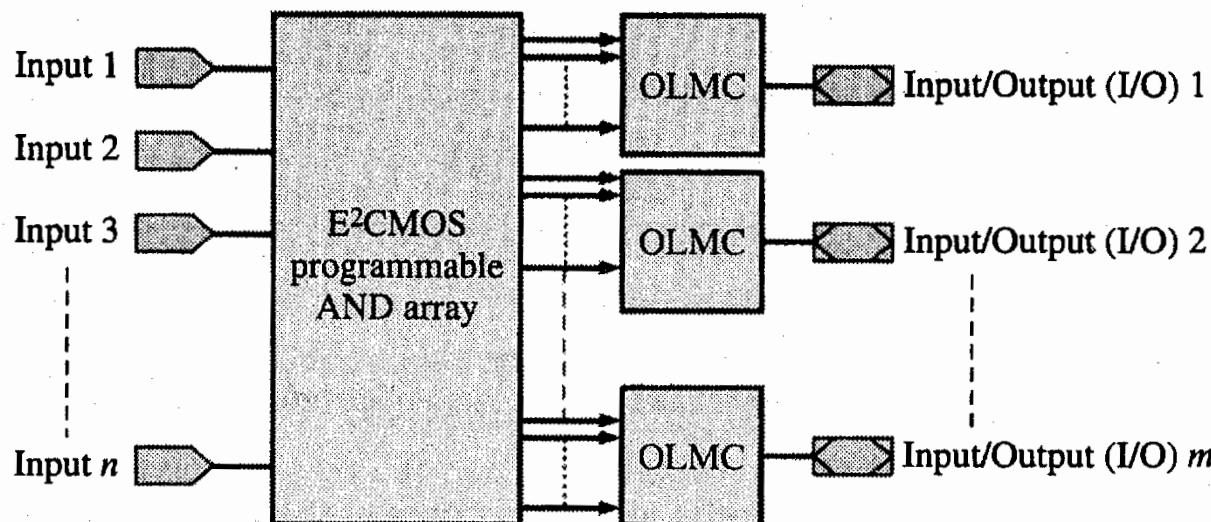


The number of inputs includes outputs that can be configured as inputs, e.g. PAL16L8.

Generic Array Logic (GAL)

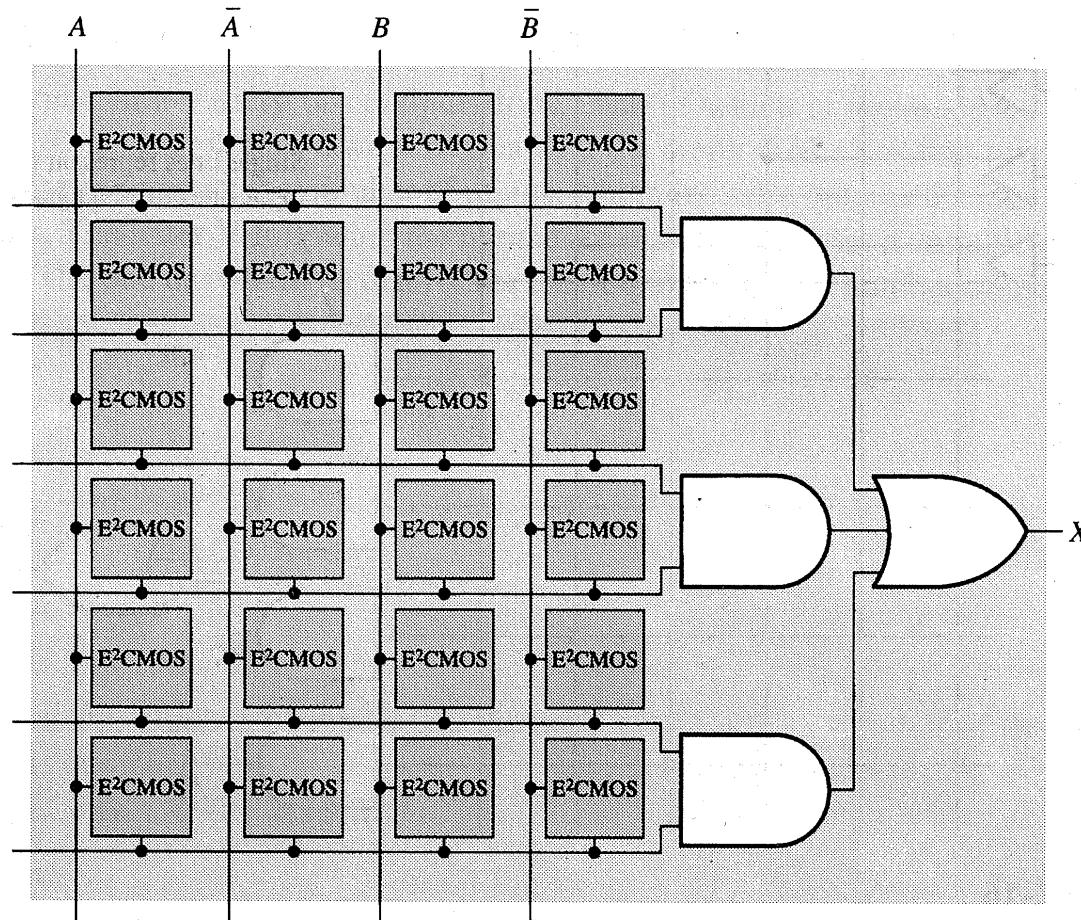
The GAL consists of:

- A reprogrammable AND array
- Output logic macrocells (OLMC), which contain the OR gates and programmable output logic.



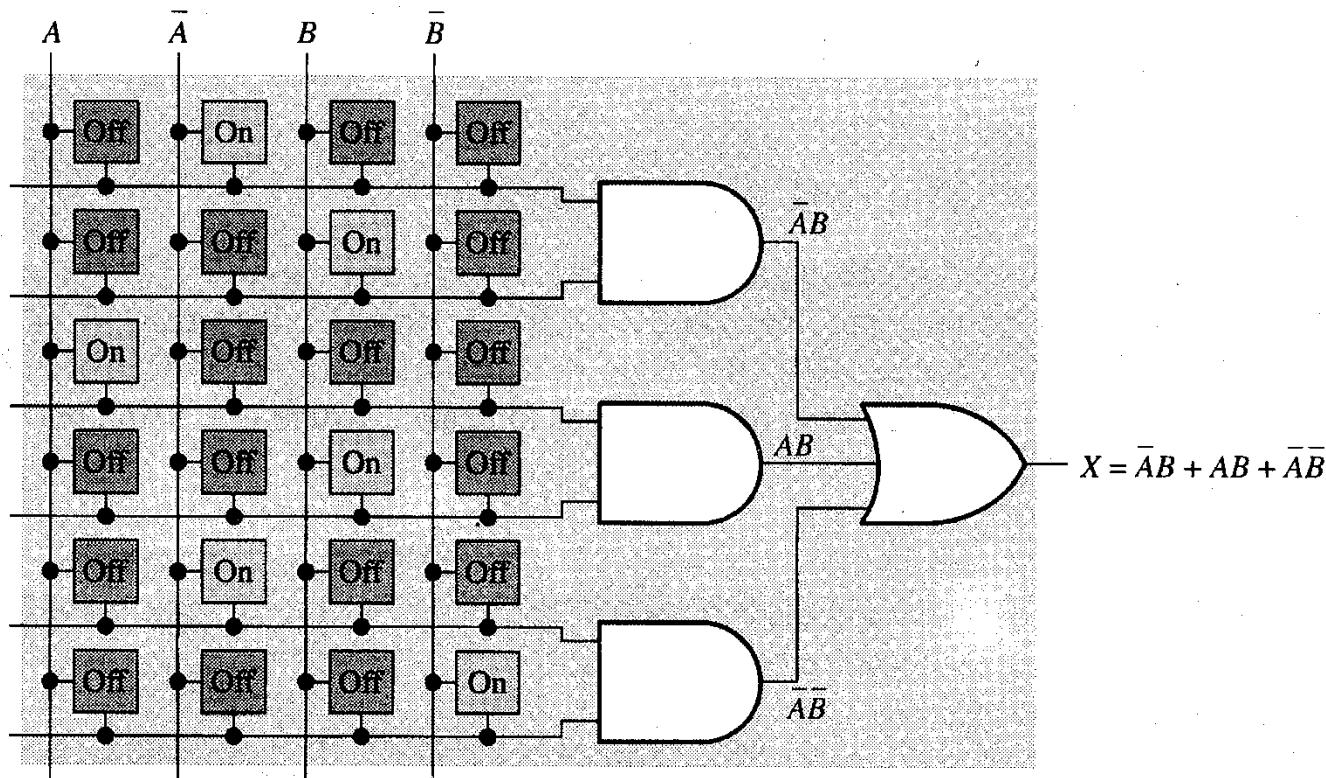
Generic Array Logic (GAL)

- The reprogrammable AND array is made up of electrically erasable CMOS (E2CMOS) cells.



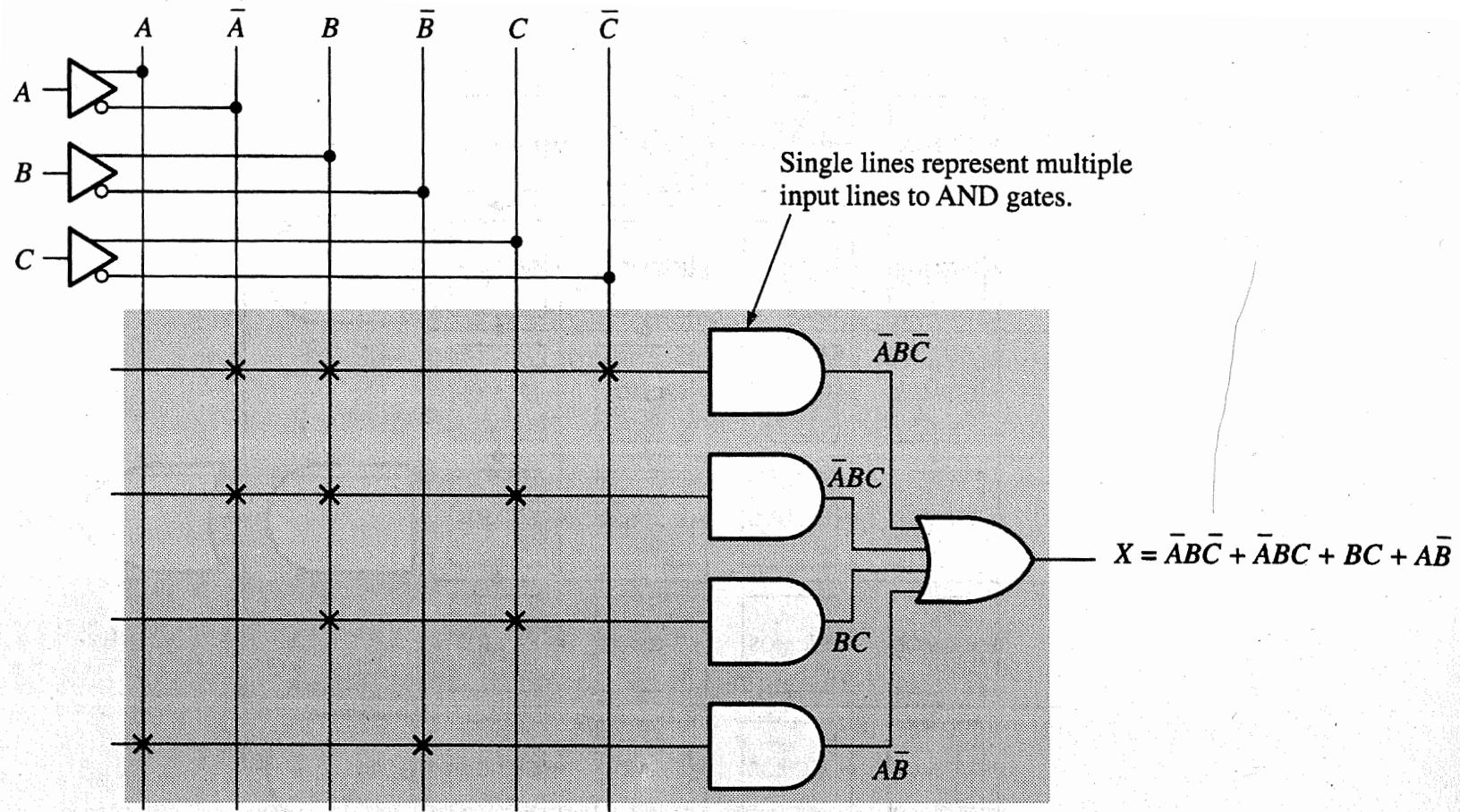
Generic Array Logic (GAL)

- A cell that is on connects its row and column, and a cell that is off disconnects the row and column.



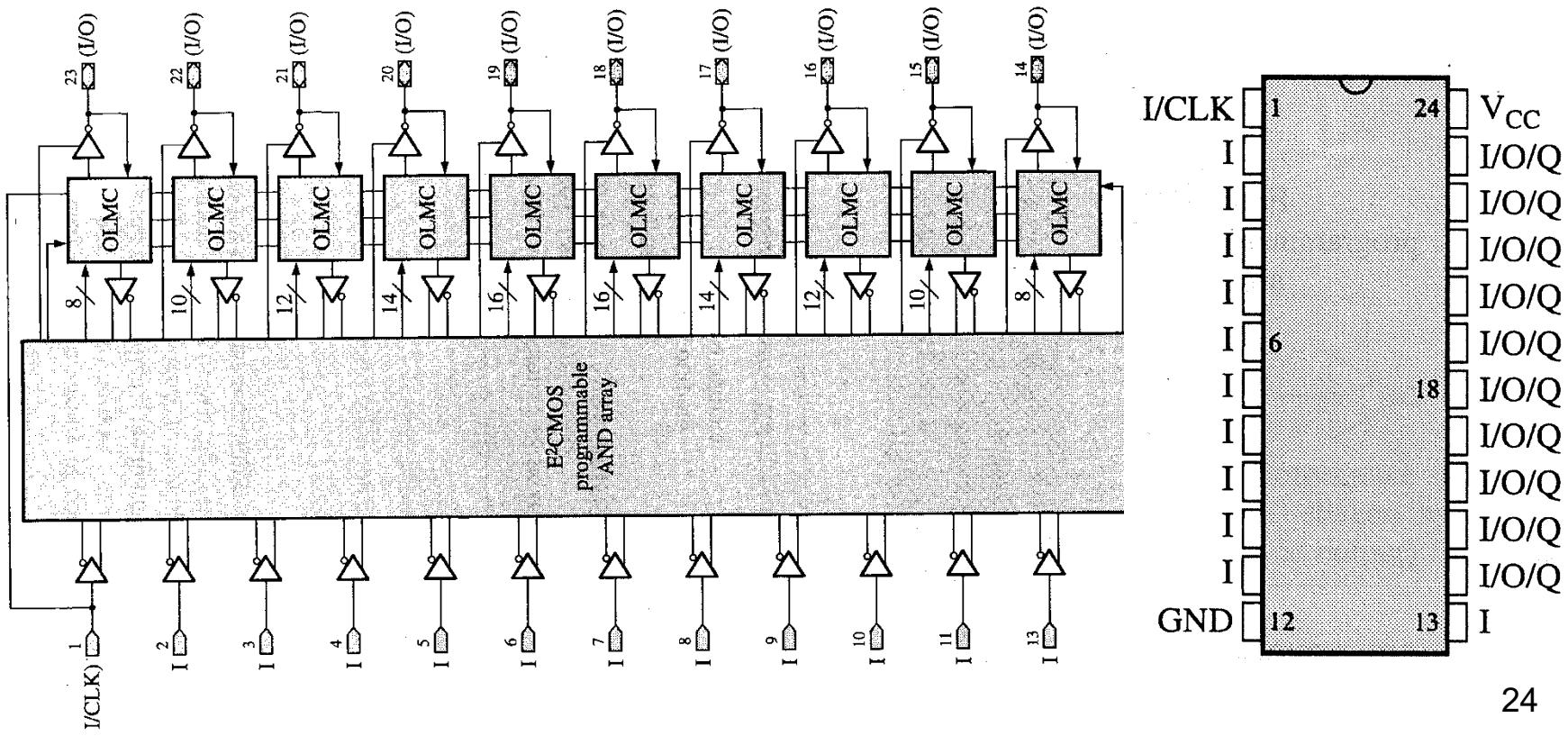
Generic Array Logic (GAL)

- Simplified symbols: a single line represents multiple input lines to AND gates.



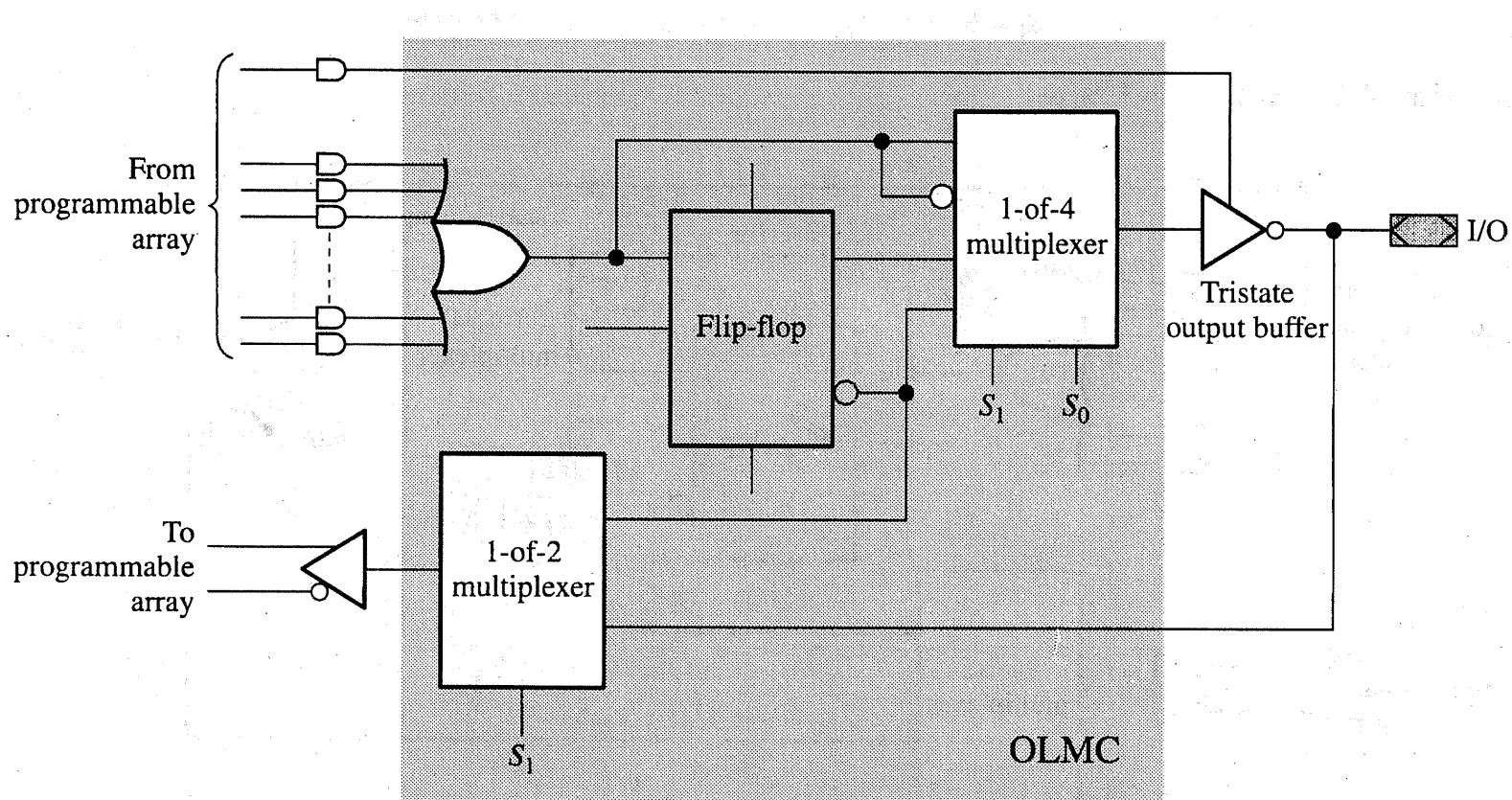
The GAL22V10

- The GAL22V10 contains 12 dedicated inputs and 10 input/outputs (I/Os). So it has up to 22 inputs and up to 10 outputs. Hence the name.



Generic Array Logic (GAL)

- The OLMC can be configured as a combinational output, an input or a registered output.



Generic Array Logic (GAL)

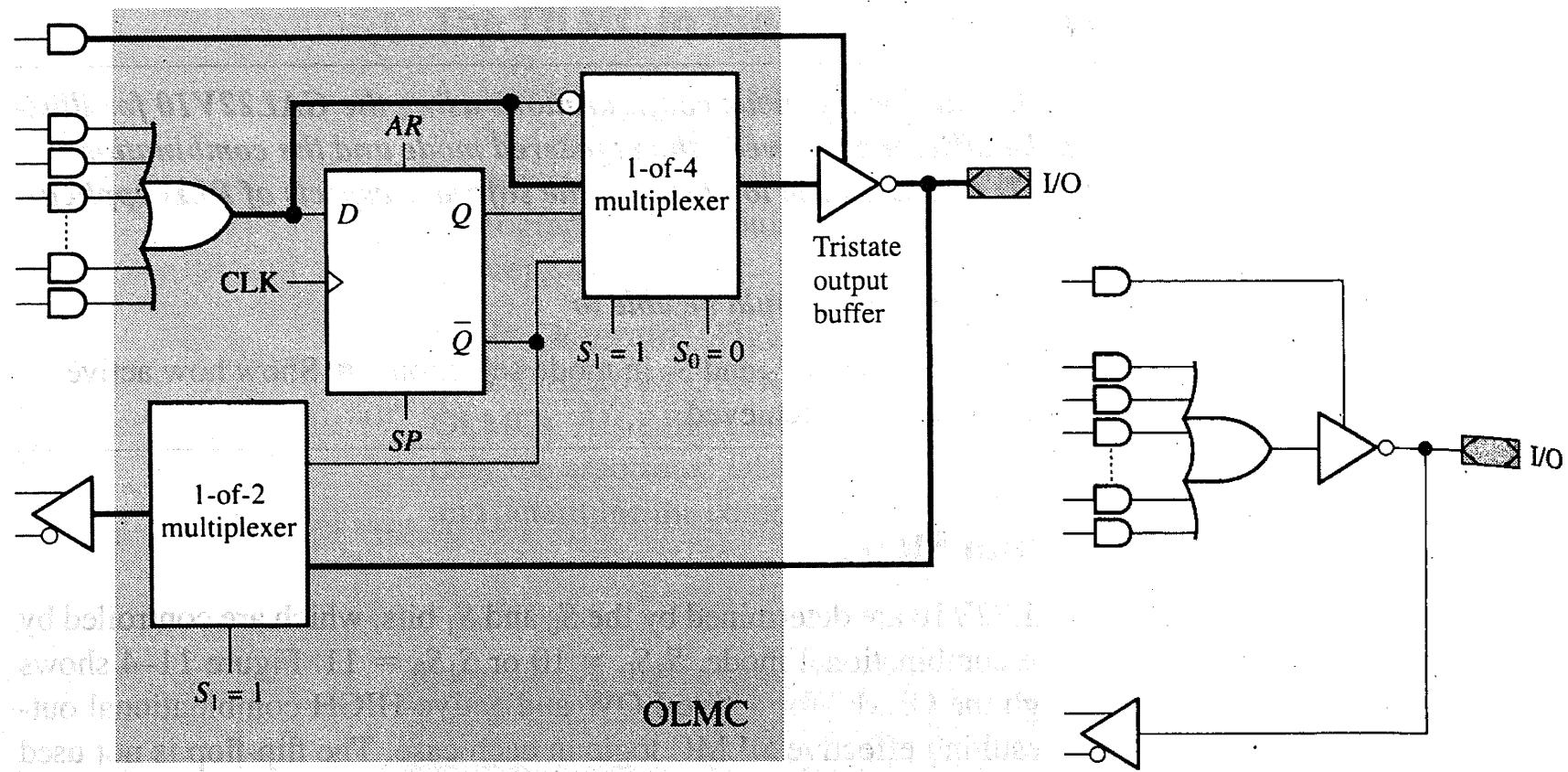
There are four inputs to the 1-of-4 multiplexer:

1. The OR gate output.
2. The complement of the OR gate output.
3. The registered OR gate output.
4. The complement of the registered OR gate output.

which corresponds to the four OLMC configurations.

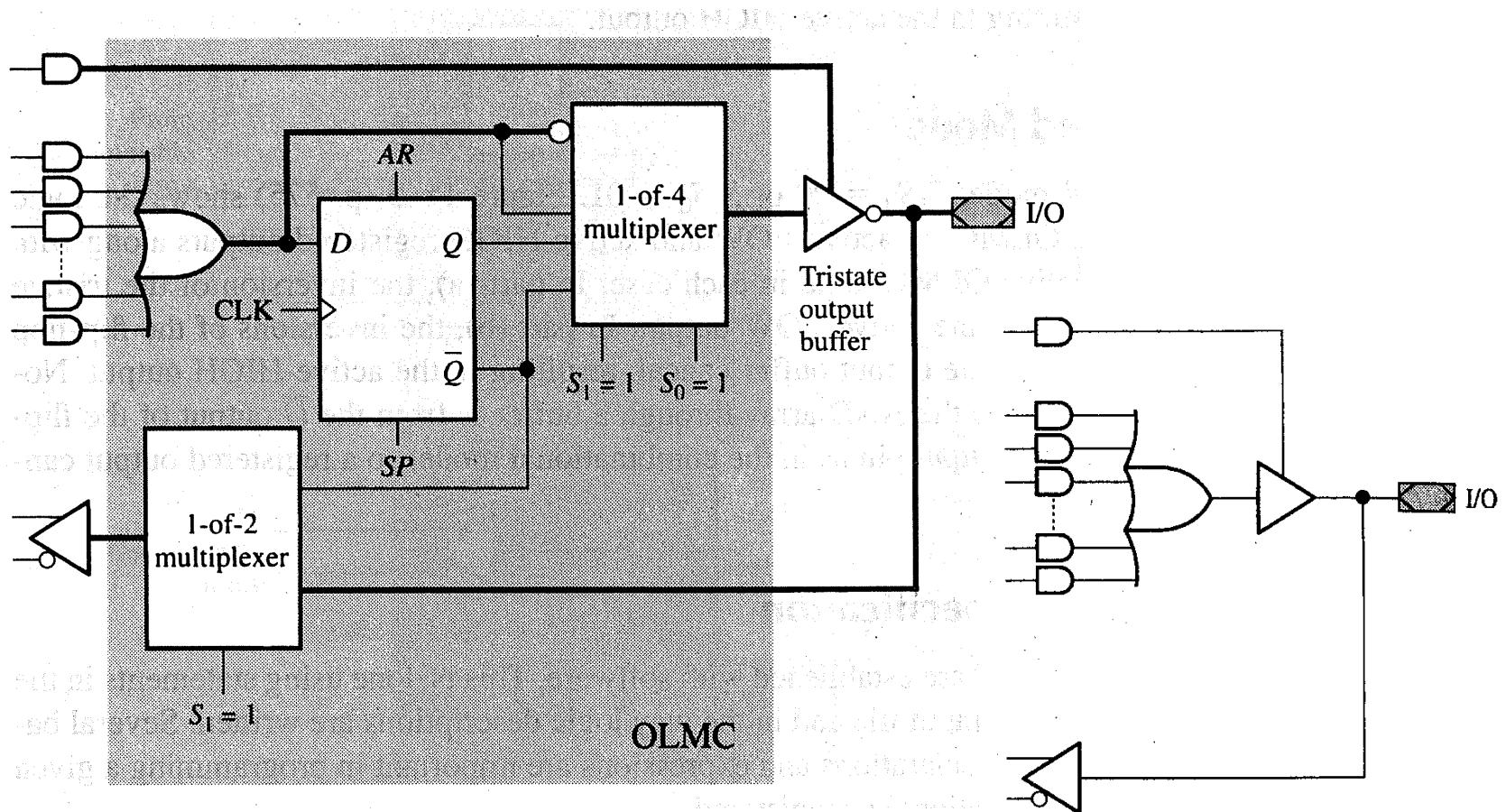
Generic Array Logic (GAL)

1. OLMC in the active-LOW combinational mode



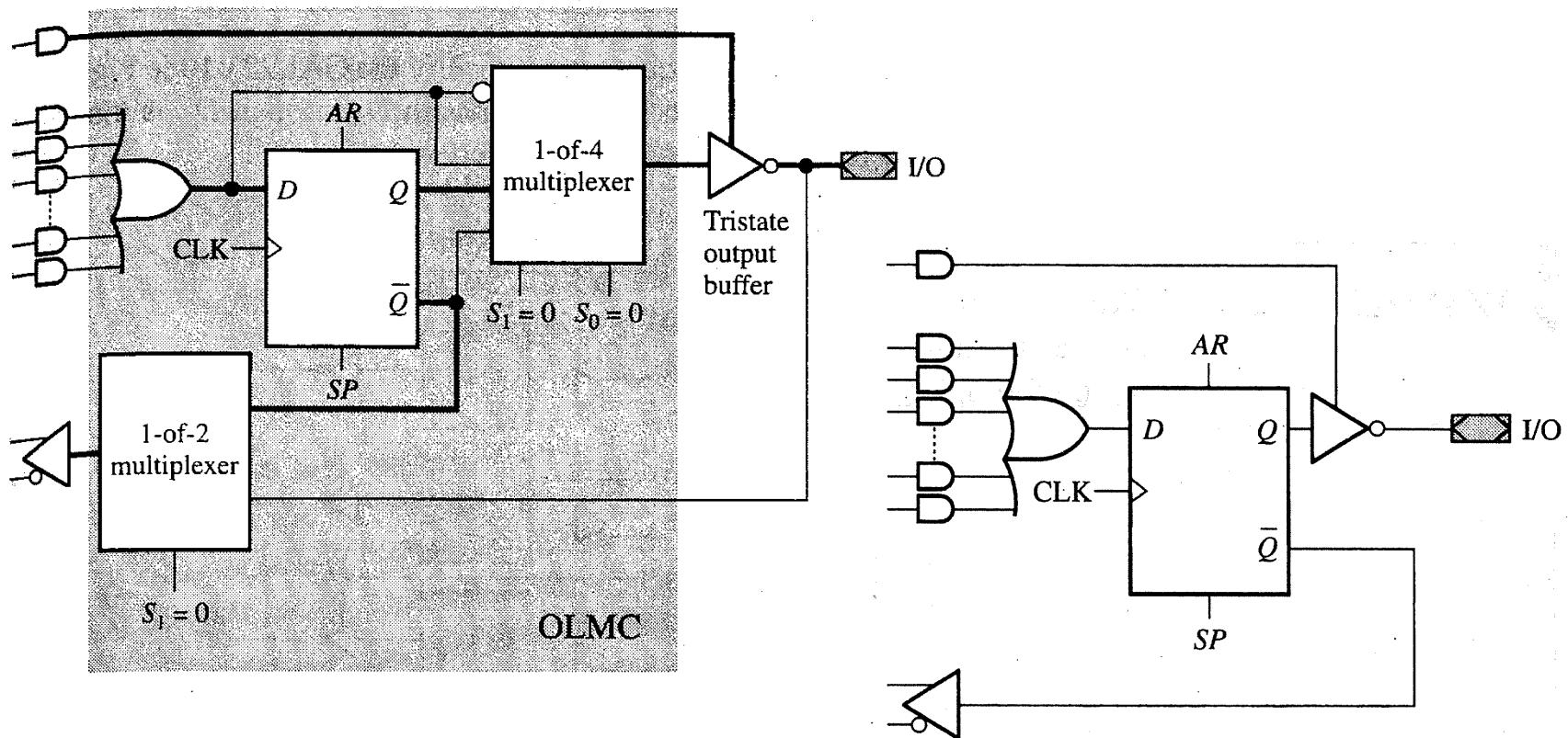
Generic Array Logic (GAL)

2. OLMC in the active-HIGH combinational mode



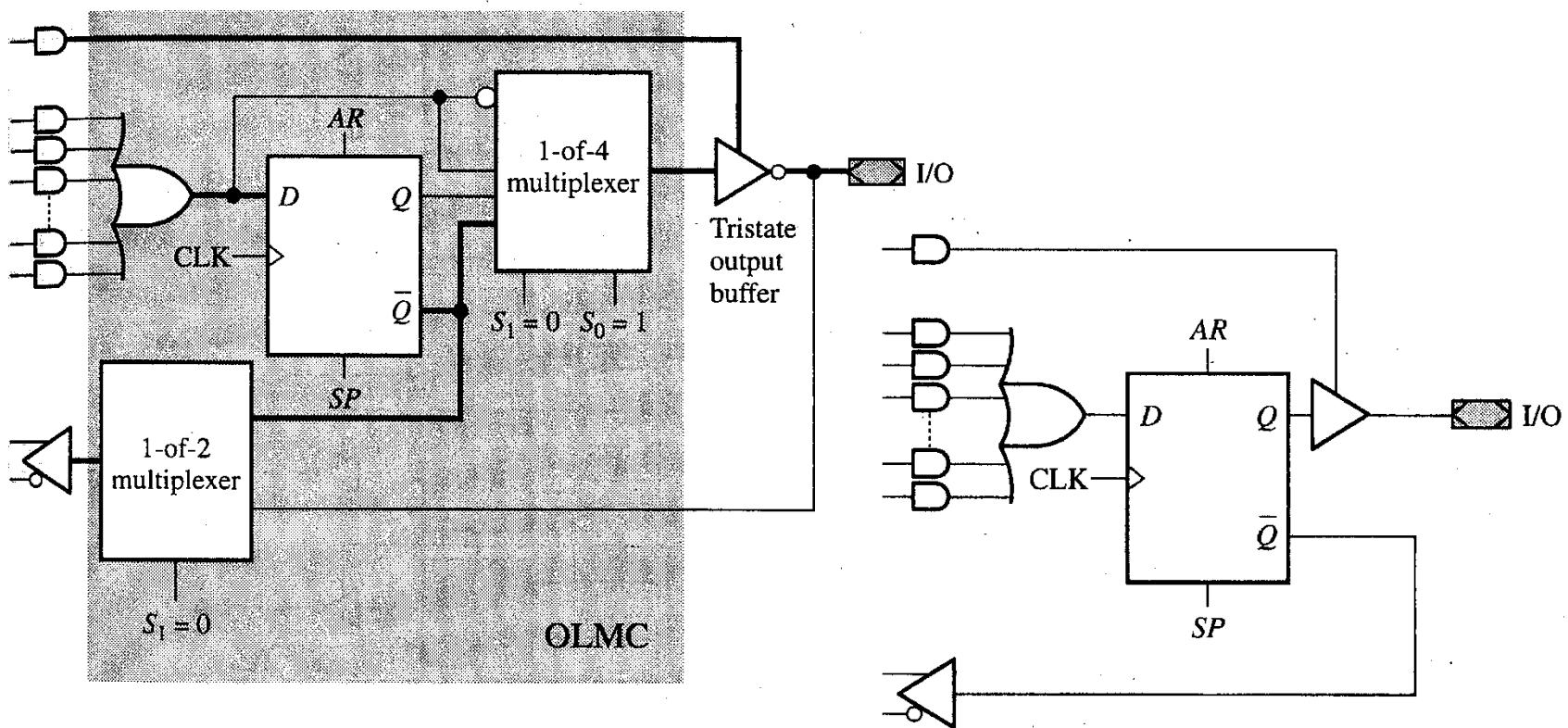
Generic Array Logic (GAL)

3. OLMC in the active-LOW registered mode



Generic Array Logic (GAL)

4. OLMC in the active-HIGH registered mode



Generic Array Logic (GAL)

An example to show how an SOP function is implemented.

$$X = ABCDEF + A\bar{B}C\bar{D}\bar{E}\bar{F} + \bar{A}\bar{B}\bar{C}D\bar{E}\bar{F} + \bar{A}BCDEF + A\bar{B}\bar{C}\bar{D}\bar{E}\bar{F} + \bar{A}\bar{B}\bar{C}D\bar{E}F + \bar{A}\bar{B}\bar{C}DEF$$

