Lecture 11a

of

EEE201

CMOS Digital Integrated Circuits

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Monday, 18th November 2024

- **CMOS Logic Inverter VTC**
  - VTC – static case
  - MOSFET terminal voltages related to V_{in} & V_{out}
  - ***I-V*** curves with same coordinates
  - intersection points of V_{in} & V_{out}

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Voltage Transfer Characteristics

(static characteristics of CMOS inverter)

- The **voltage transfer characteristics** (VTC) of the logic inverter (and in general other logic gates such as NAND and NOR) ***relate*** the <u>output voltage</u> to the <u>input voltage</u>.
  - Note that the VTC refer to the ***static*** case of relationship between the output voltage and the input voltage. It does not take into account of transient behaviour.
  - The logic inverter's VTC are also called **DC transfer characteristics** or simply **static characteristics**.
  - In the ***static*** case, there is no need to consider the charging & discharging processes.

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CMOS Inverter VTC

(definitions of quantities)

- To obtain the CMOS inverter VTC, we need to find how the output voltage $\mathbf{V_{out}}$ varies as a function of the input voltage $\mathbf{V_{in}}$ (from 0 V to V_{DD}).
  - When $\mathbf{V_{in}}$ varies (from 0 V to V_{DD}), the nMOSFET and pMOSFET of the CMOS logic inverter will go through different operation modes.
  - The operation modes of the two MOSFETs depend on the their terminal voltages (mainly V_{GS} & V_{DS}).
  - We need to relate the MOSFETs' terminal voltages to $\mathbf{V_{in}}$ and $\mathbf{V_{out}}$.
  - two sets of MOSFET voltages: V_{GSn}, V_{DSn}, V_{Tn} & V_{GSp}, V_{DSp}, V_{Tp}

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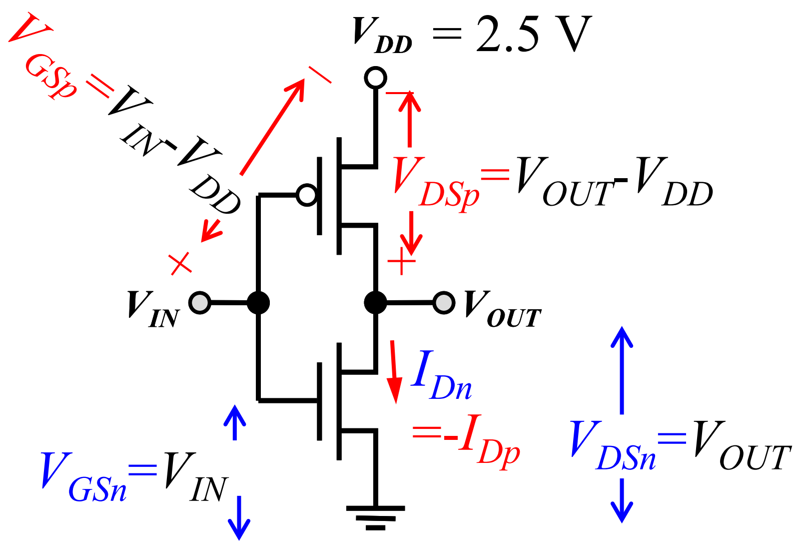
CMOS Inverter VTC

(relate MOSFETs' terminal voltages to V_{in} & V_{out})

- Since there is no need to consider the charging and discharging in the ***static* case**, the drain current flowing out of the pMOSFET must flow into the drain of the nMOSFET $\Rightarrow |I_{DSp}| = |I_{DSn}|$ in the CMOS logic inverter.



$$I_{Dp} = -I_{Dn}$$
$$V_{GSn} = V_{IN}$$
$$V_{GSp} = V_{IN} - V_{DD}$$
$$V_{DSn} = V_{OUT}$$
$$V_{DSp} = V_{OUT} - V_{DD}$$

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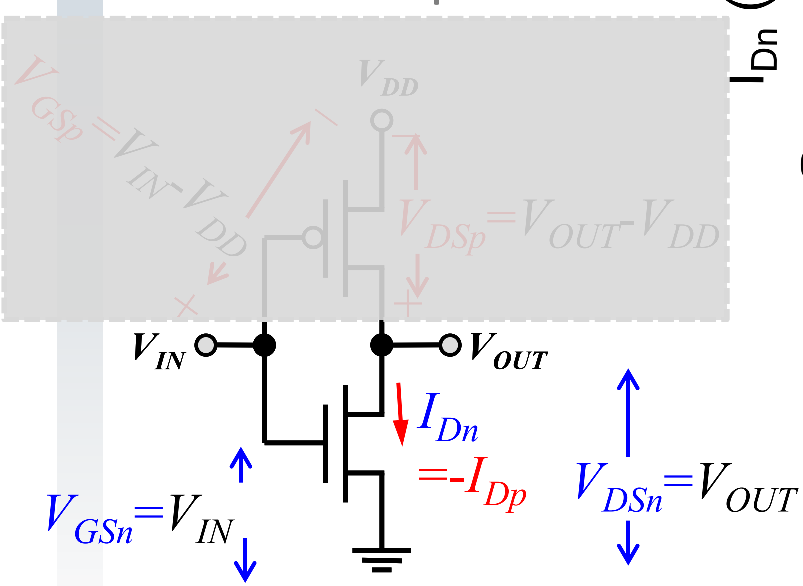
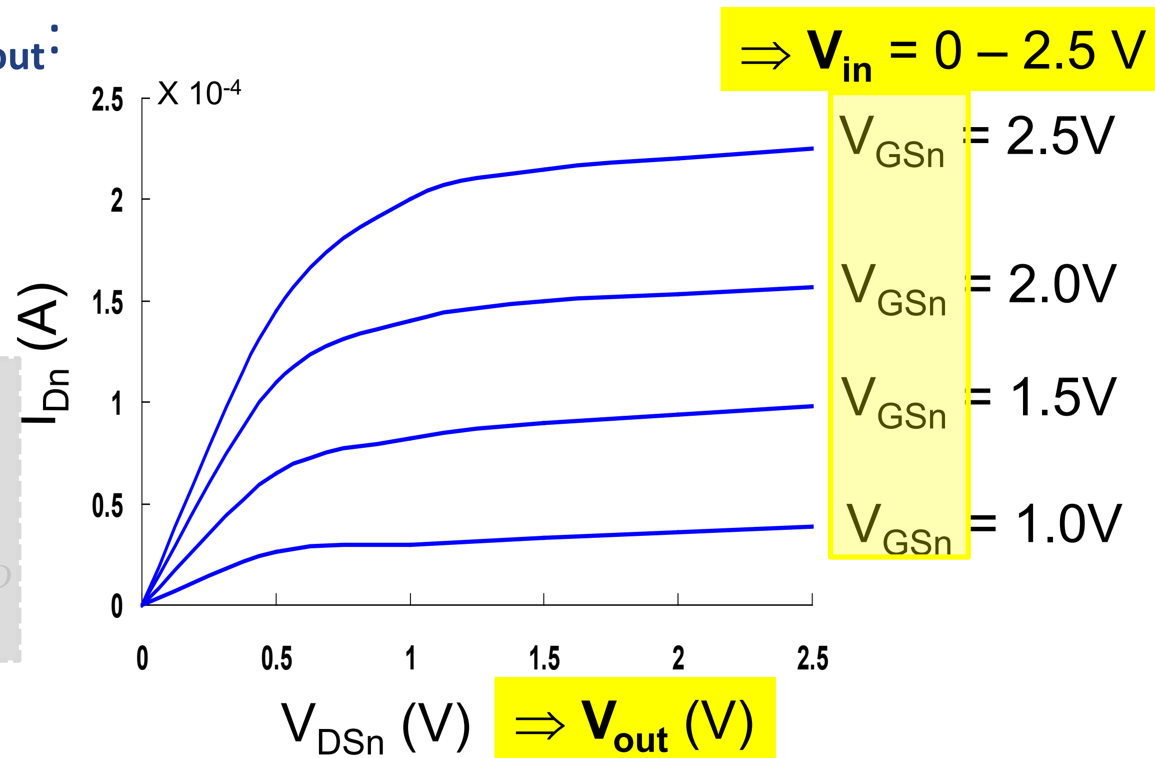
CMOS Inverter VTC

(relate **n**MOSFET terminal voltages to $\mathbf{V_{in}}$ & $\mathbf{V_{out}}$)

- It is straightforward to relate the ***n***MOSFET's terminal voltages to $\mathbf{V_{in}}$ & $\mathbf{V_{out}}$:

V_{Tn0} = 0.4 V & V_{DD} = 2.5 V as an example





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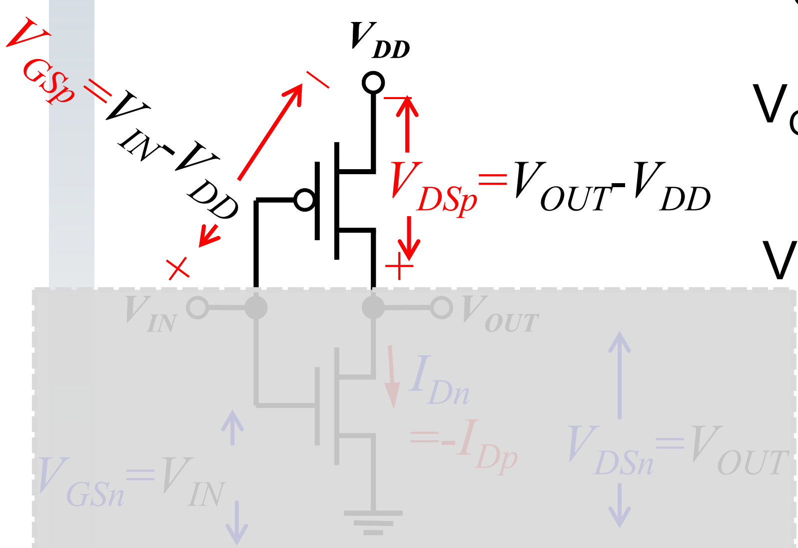
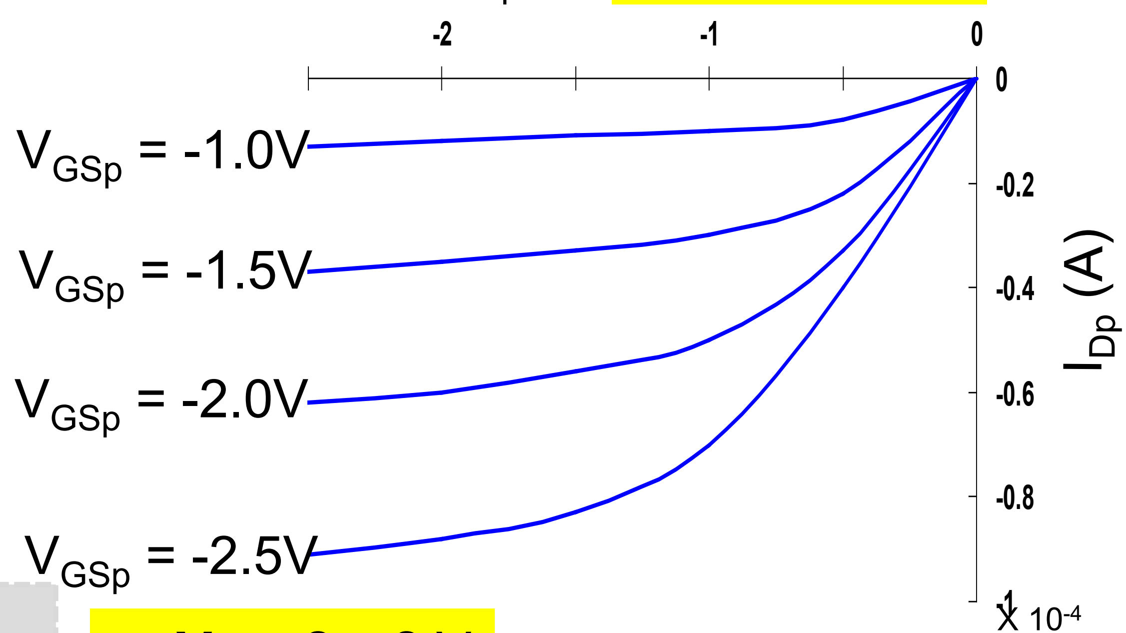
CMOS Inverter VTC

(*I*-*V* curves of **p**MOSFET in the original form)

- To relate the ***p***MOSFET's terminal voltages to $\mathbf{V_{in}}$ & $\mathbf{V_{out}}$, it needs transformation of the curves. V_{DSp} (V) $\Rightarrow$ $\mathbf{V_{out}}$ **= ?** (V)

$V_{Tp0} = -0.4$ V &
$V_{DD} = 2.5$ V as an example





$\Rightarrow$ $\mathbf{V_{in}}$ **= ? – ? V**

$V_{in} = V_{DD} + V_{GSp}$
$= 1.5 – 0$ V

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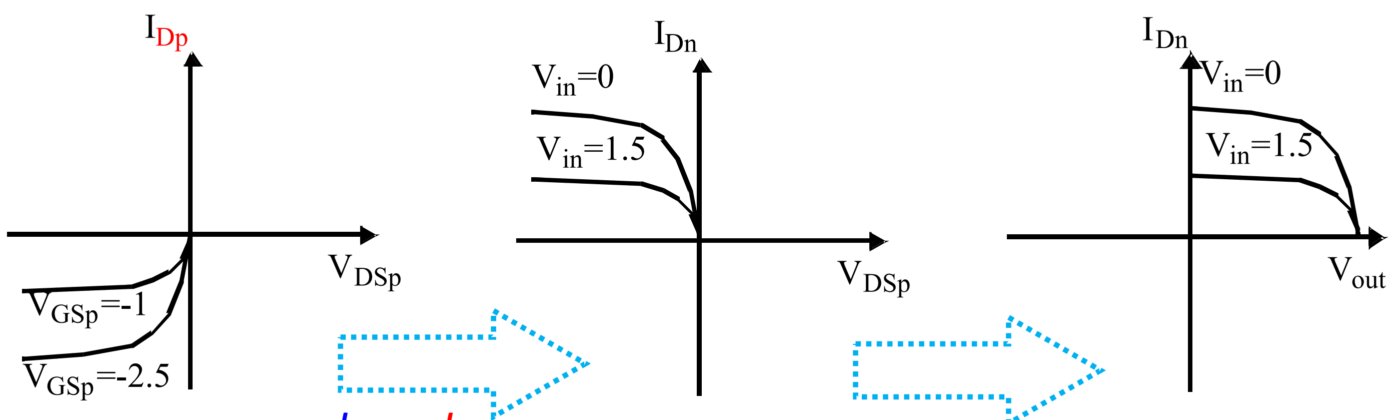
CMOS Inverter VTC

(relate pMOSFET terminal voltages to $\mathbf{V_{in}}$ & $\mathbf{V_{out}}$)

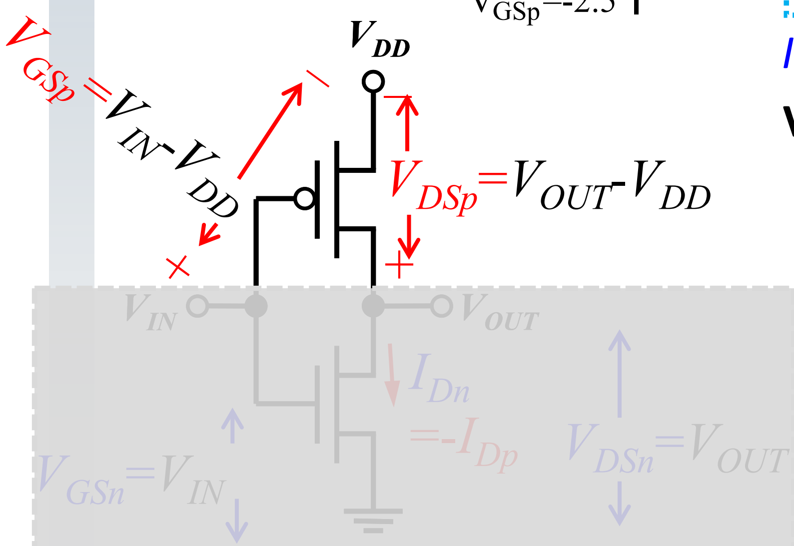
- Transforming the ***p***MOSFET's ***I-V*** curves in terms of $\mathbf{V_{in}}$ & $\mathbf{V_{out}}$:



$I_{Dn} = -I_{Dp}$

$\mathbf{V_{in} = V_{DD} + V_{GSp}}$
$= 1.5 – 0$ V

$\mathbf{V_{out} = V_{DSp} + V_{DD}}$



$V_{Tp0} = –0.4$ V & $V_{DD} = 2.5$ V as an example

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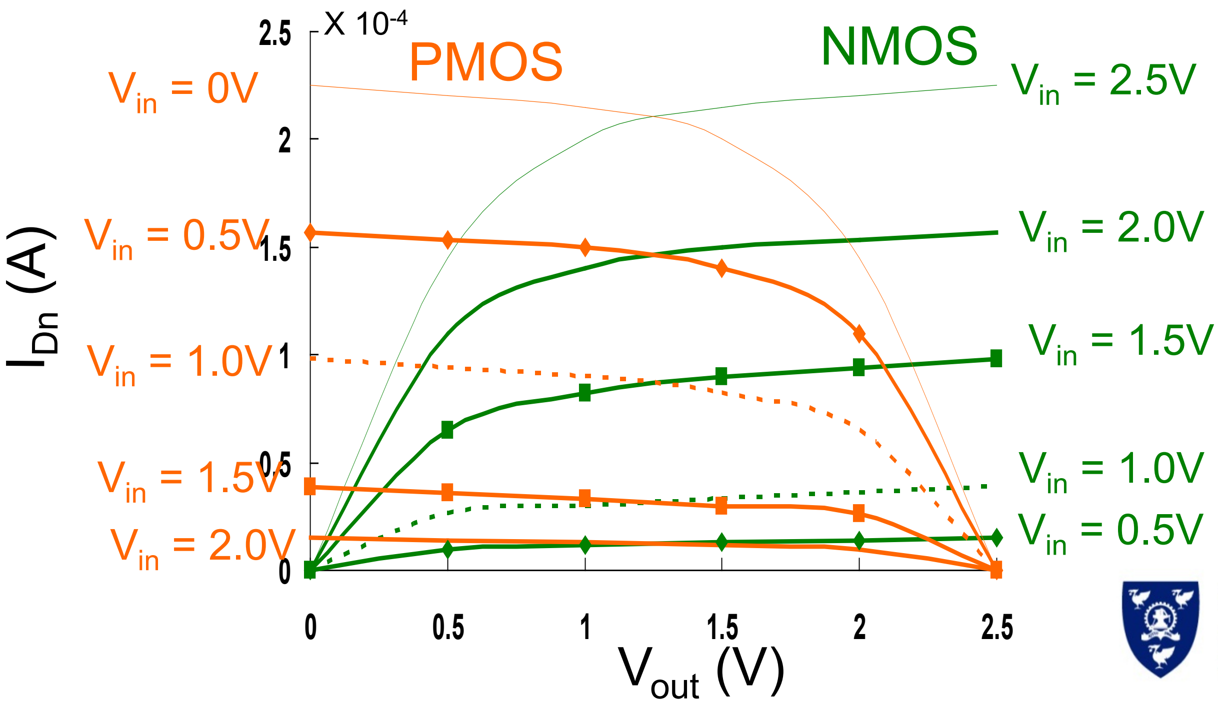
CMOS Inverter VTC

(*I-V* curves with the same coordinates)

- When the ***I-V*** curves of both the nMOSFET and pMOSFET have the same coordinates (i.e. in terms of the same $\mathbf{V_{in}}$ & $\mathbf{V_{out}}$ and $\boldsymbol{I_{Dn}}$), it is now ready for finding out the CMOS inverter's VTC using the graphical approach:



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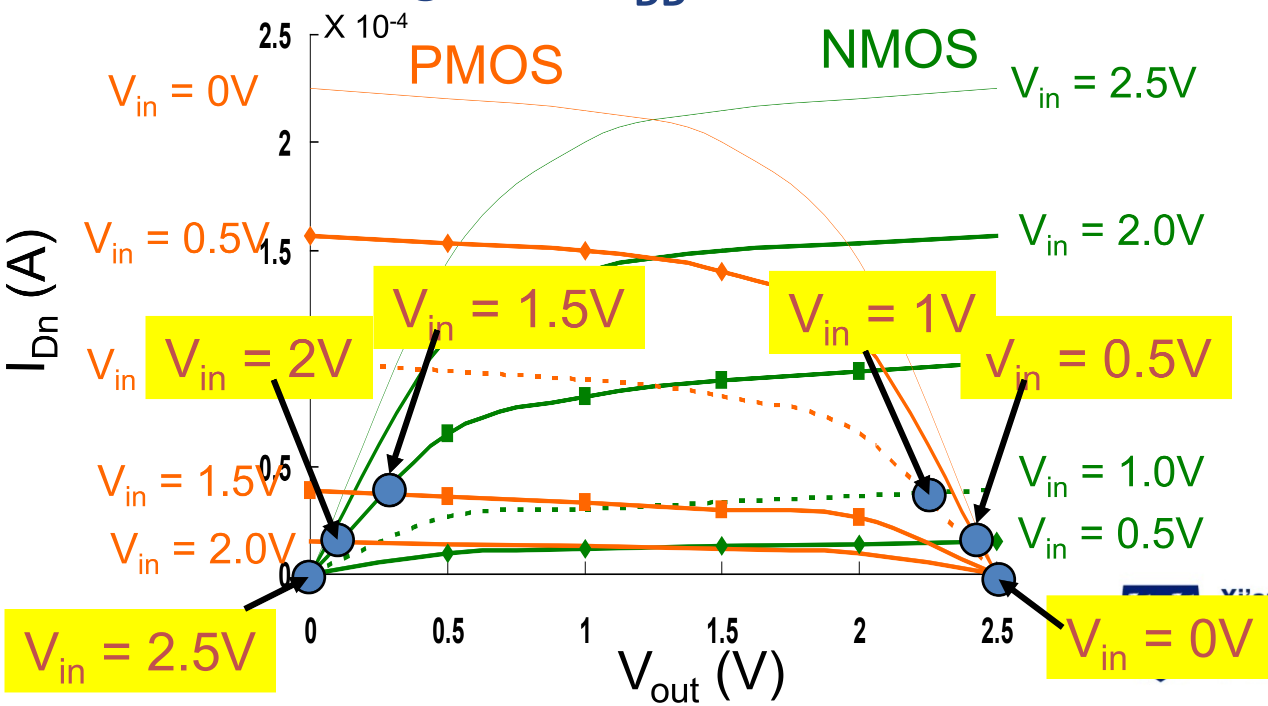
CMOS Inverter VTC

(intersection points of the *I-V* curves)

- As $\mathbf{V_{in}}$ increases from 0 V to V_{DD} = 2.5 V, there are intersection points of the *I-V* curves (nMOS & pMOS).
  - The intersection points correspond also to $\mathbf{V_{out}}$, decreasing from V_{DD} = 2.5 V to 0 V.



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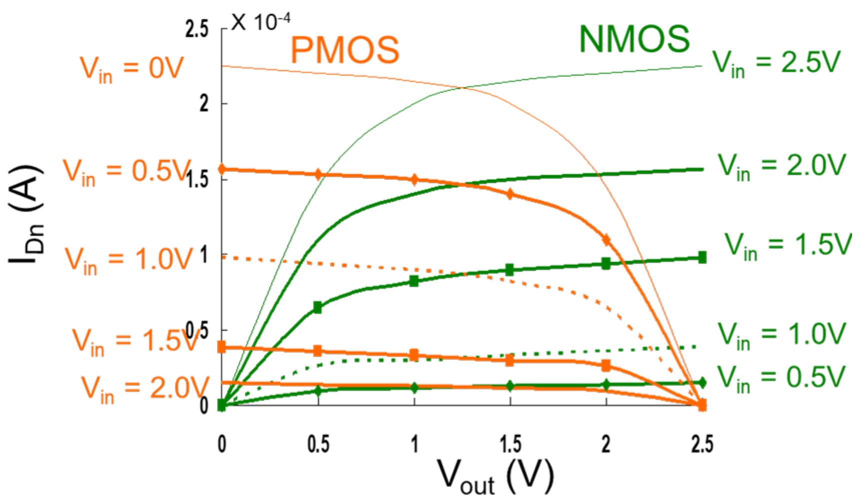
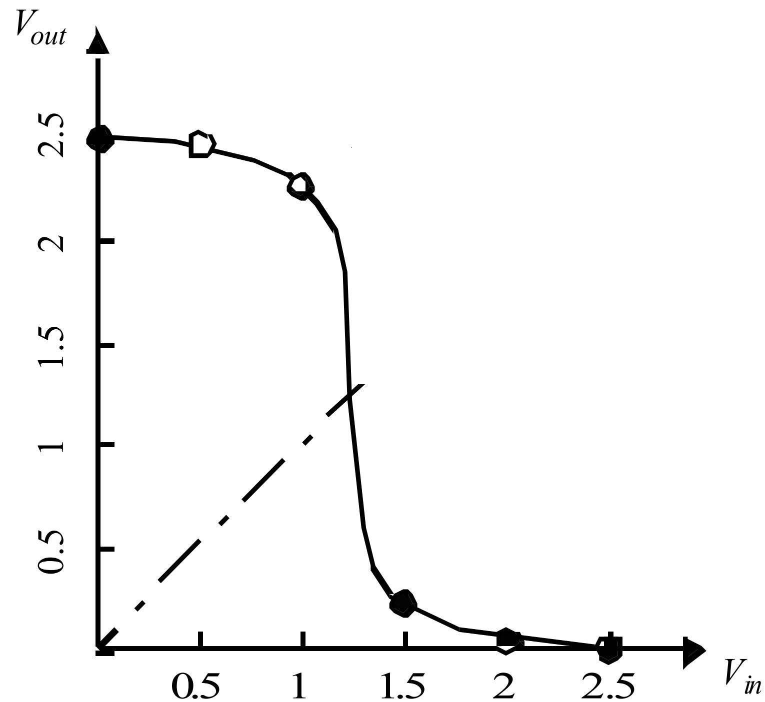
CMOS Inverter VTC

(V_{in} & V_{out} from the intersection points)

- The corresponding intersection points of the ***I-V*** curves of both the nMOSFET and pMOSFET are data points the CMOS inverter's VTC:





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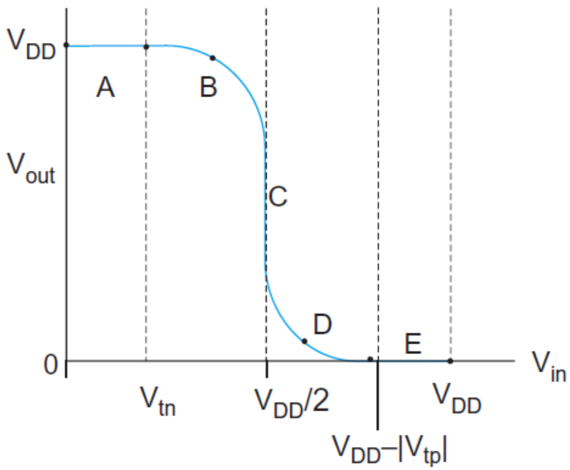
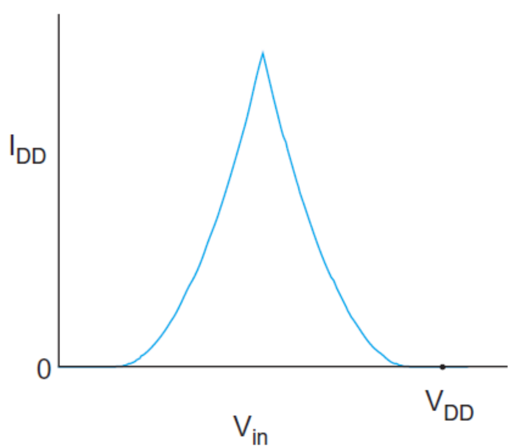
CMOS Inverter VTC

(**dynamic current** during switching)

- Note that there is current flow directly from V_{DD} to ground in the transition region of the CMOS inverter's VTC.





- In the steady state, there is almost zero power consumption in the CMOS inverter (and generally other logic gates).
- However, in the ***dynamic*** situation (i.e. when the input changes from logic "0" to "1" or vice versa, there is current consumption.

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