

# Chapter 5: Basic FET Amplifiers

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# Outline

- Week 1-6
  - ✓ Chapter 1: Semiconductor material and diodes
  - ✓ Chapter 2: Diode circuits
  - ✓ Chapter 3 Field-Effect Transistor
  - ✓ Chapter 4 Bipolar Junction Transistor
- Week 7
  - ✓ Online quiz
- Week 8-13
  - Chapter 5: FET amplifier
  - Chapter 6: BJT amplifier
  - Chapter 7: Frequency response of amplifier circuits

# Module Assessment

- 2 Assignments, 10%
- 2 Lab reports, 15%
  - Submit lab report in two weeks after the lab session
- ✓ Online quiz, 15%
- Final exam, 60%
  - 20 MCQs in Section A, 40 marks → the same format as the **Online Quiz**
  - 3 questions in Section B, 60 marks → the same format as the **Assignment**
    - Q1: Diode circuit, or FET circuit, or BJT circuit, 20 marks
    - Q2: BJT amplifier + frequency response, 20 marks
    - Q3: MOSFET amplifier + frequency response, 20 marks

# Module Assessment

- 2 Assignments, 10% **Submit your assignments and lab reports!! It is EASY to get marks!!!**
- 2 Lab reports, 15%
  - Submit lab report in two weeks after the lab session
- ✓ Online quiz, 15%
- Final exam, 60% → Chapter 2-7
  - 20 MCQs in Section A, 40 marks
  - 3 questions in Section B, 60 marks → **See Past Papers from the Library**
    - Q1: Diode circuit, or FET circuit, or BJT circuit, 20 marks
    - Q2: BJT amplifier + frequency response, 20 marks
    - Q3: MOSFET amplifier + frequency response, 20 marks

# Preview

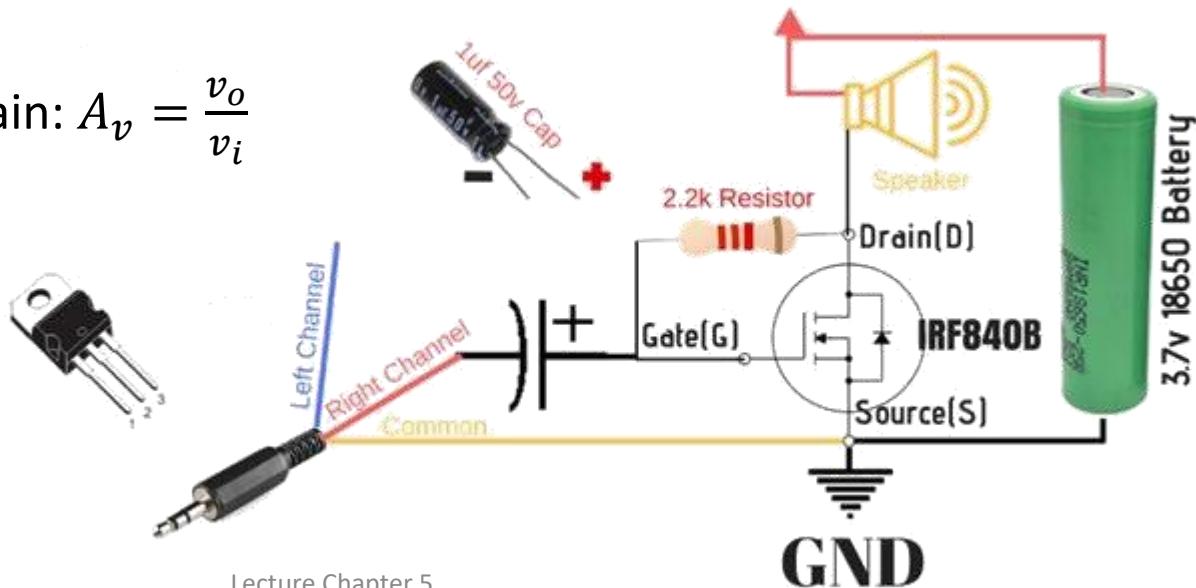
- ✓ Investigate a **single-MOS transistor circuit** that can **amplify** [放大] a small, time-varying input signal.
  - Use the **small-signal model** to analyze linear amplifiers
- ✓ Discuss the **three basic transistor amplifier configurations**
  - Common-source, common-drain, and common-gate amplifiers
  - Compare the general characteristics of the three basic amplifier configurations
- Optional: analyze multitransistor or multistage amplifiers and understand the advantages of these circuits over single-transistor amplifiers

# The MOSFET Amplifier

Investigate the process by which a single-transistor circuit can amplify a small, time-varying input signal and develop the small-signal models of the transistor that are used in the analysis of linear amplifiers.

# Amplifiers [放大器]

- Electronic circuits that process **analog signals** are called **analog circuits**
- One example of an analog circuit is a **linear amplifier**
  - The magnitude of the output signal is larger and **directly proportional** to the input signal
  - Small-signal voltage gain:  $A_v = \frac{v_o}{v_i}$

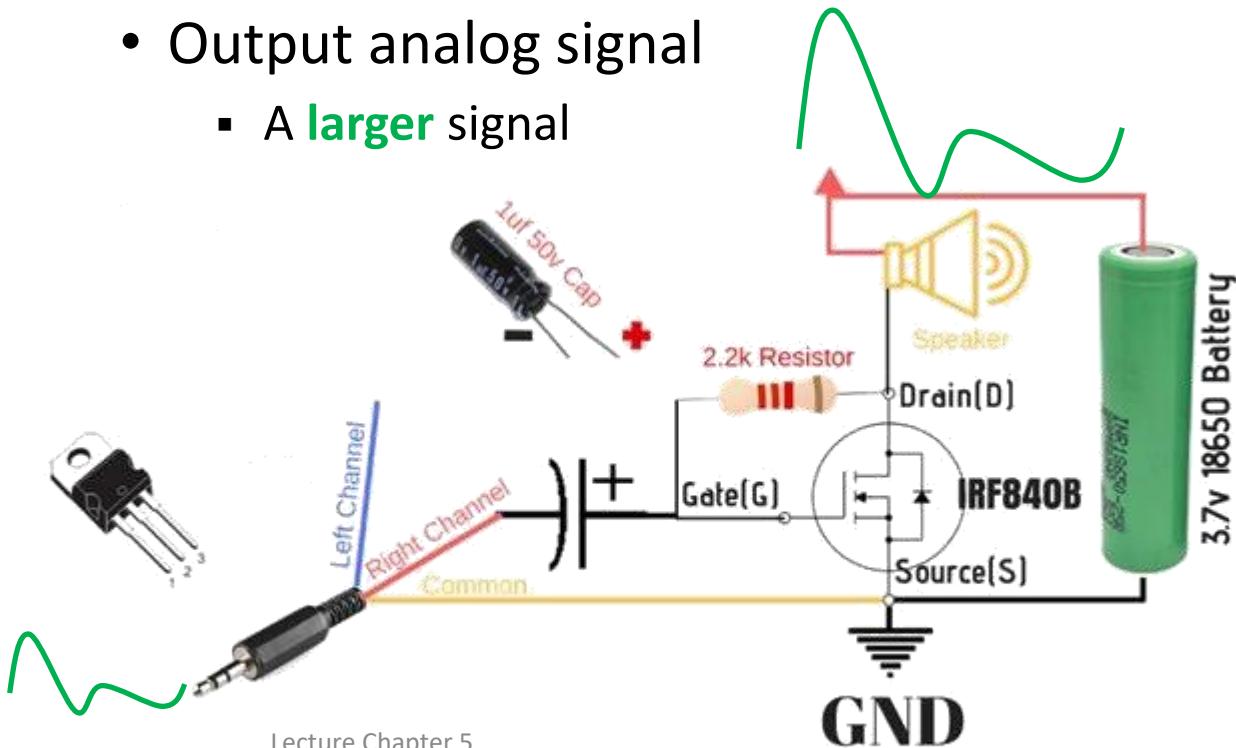




# Amplifiers

- DC voltage source
- MOSFET transistor
- Resistors
- Capacitors

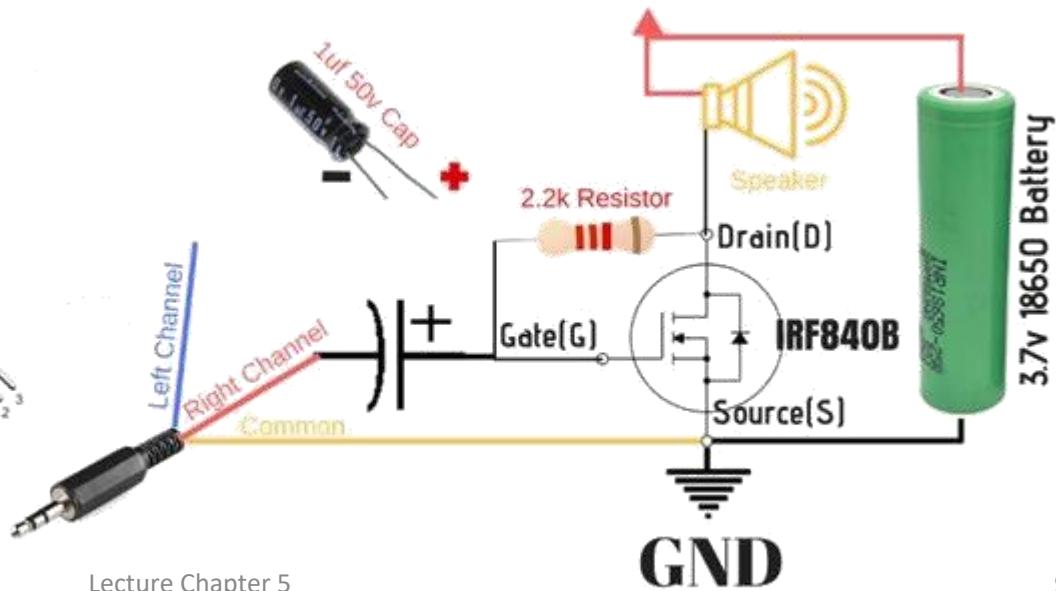
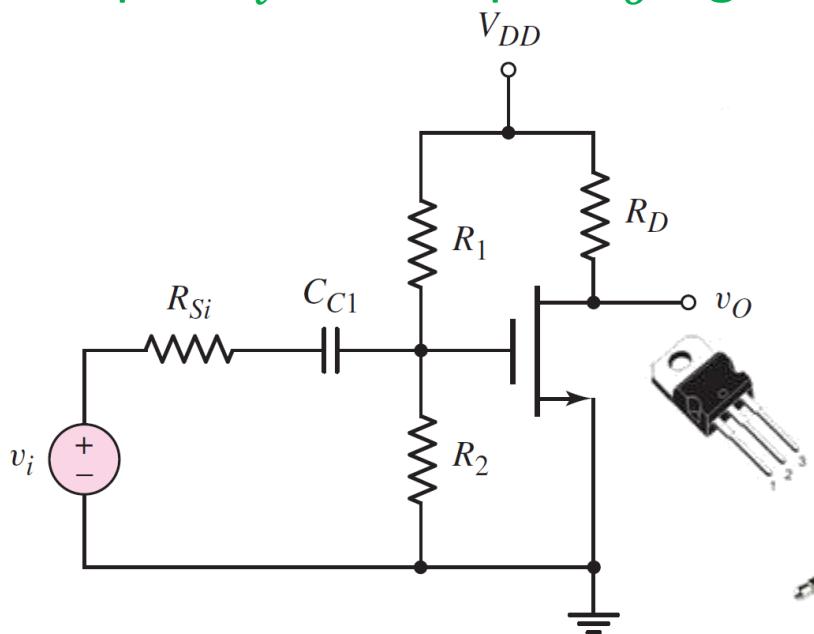
- Input analog signal
  - A **small** signal
- Output analog signal
  - A **larger** signal





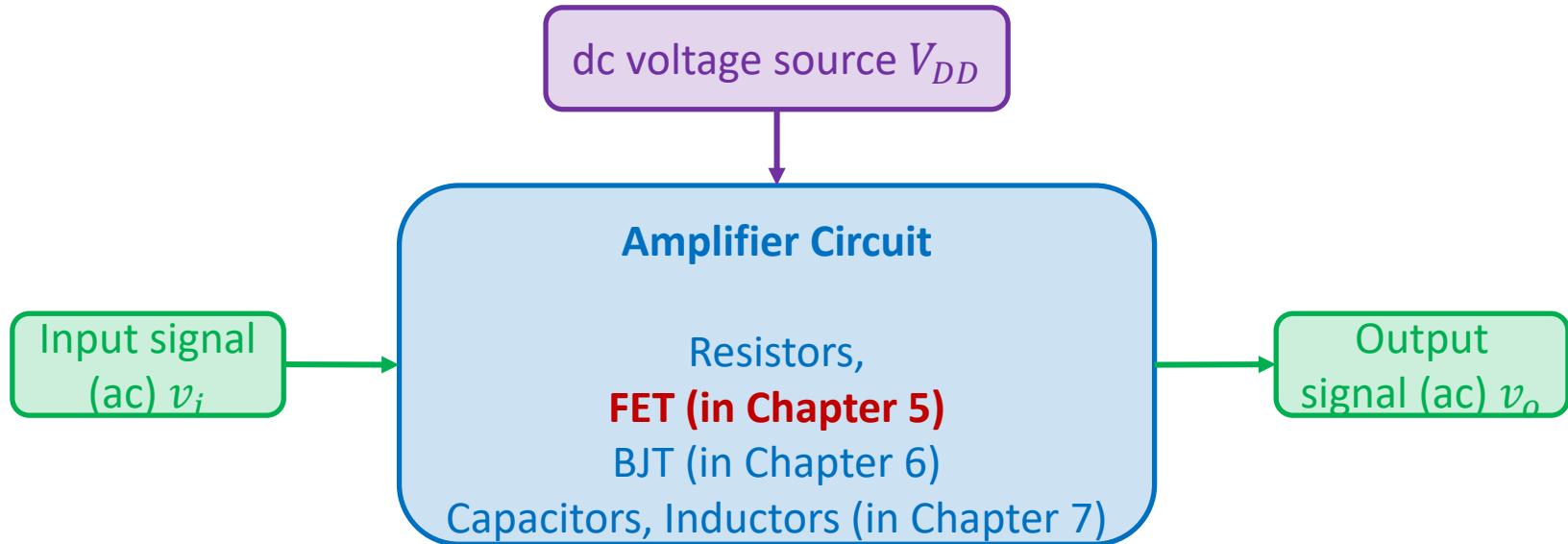
# Amplifiers

- DC voltage source  $V_{DD}$
- MOSFET transistor, resistors  $R_1 R_2 R_D R_{Si}$ , capacitors  $C_{C1}$
- Input  $v_i$  and output  $v_o$  signal (ac signal)



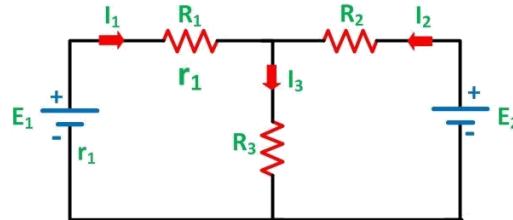
# Amplifiers

- Field-effect transistor (FET) is used as the amplifying device
  - Two sources: dc source and ac source (analog signal)
  - Superposition[叠加]: Total value = dc value + ac value

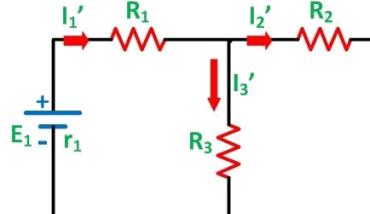


# Superposition Method

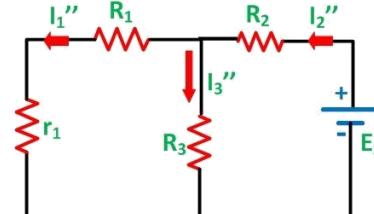
- The response across any element in the circuit is the **sum** of the responses obtained from each source considered **separately**
- Two independent sources in circuit A
- Only consider  $E_1$  (circuit B)
  - Set  $E_2 = 0$ , the current through  $R_3$  is  $I'_3$
- Only consider  $E_2$  (circuit C)
  - Set  $E_1 = 0$ , the current through  $R_3$  is  $I''_3$
- The total current through  $R_1, R_2$ , and  $R_3$ 
  - $I_1 = I'_1 + I''_1$
  - $I_2 = I'_2 + I''_2$
  - $I_3 = I'_3 + I''_3$



Circuit Diagram A



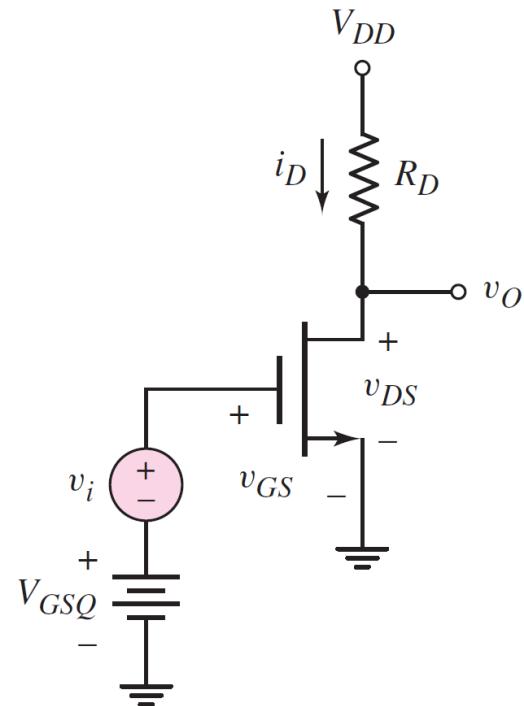
Circuit Diagram B



Circuit Diagram C

# Amplifier Circuit

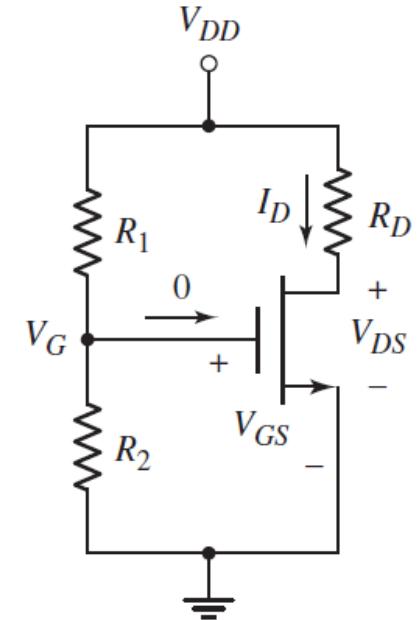
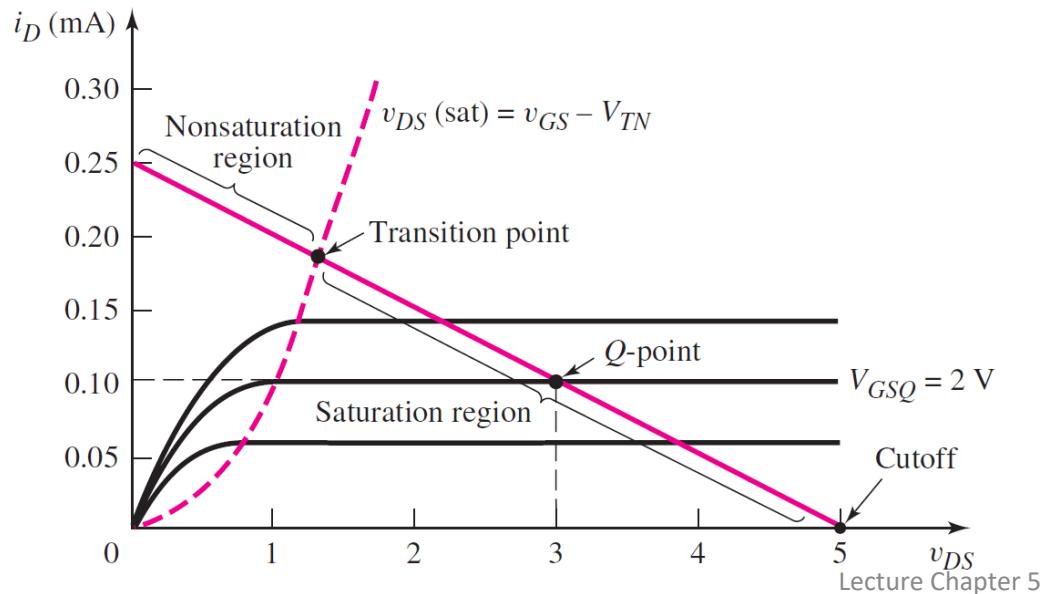
- An NMOS common-source circuit
- **Two** type independent sources in the circuit
  - dc source:  $V_{DD}$  and  $V_{GSQ}$
  - ac source:  $v_i$
- We can use **superposition method**, so that dc analysis and ac analysis of the circuits can be performed **separately**
  - **Step 1:** In dc analysis, set ac source to zero
  - **Step 2:** In ac analysis, set dc source to zero



# Graphical Analysis: DC Load Line

- In amplifier circuits, the FET must be biased in the saturation region

- $$V_{DSQ} > V_{DS(\text{sat})} = V_{GSQ} - V_{TN}$$



# Graphical Analysis: DC + AC

- As  $v_i$  increases

$$v_{GS} = V_{GSQ} + v_i$$

Total value = dc (fixed) + ac (time-varying)

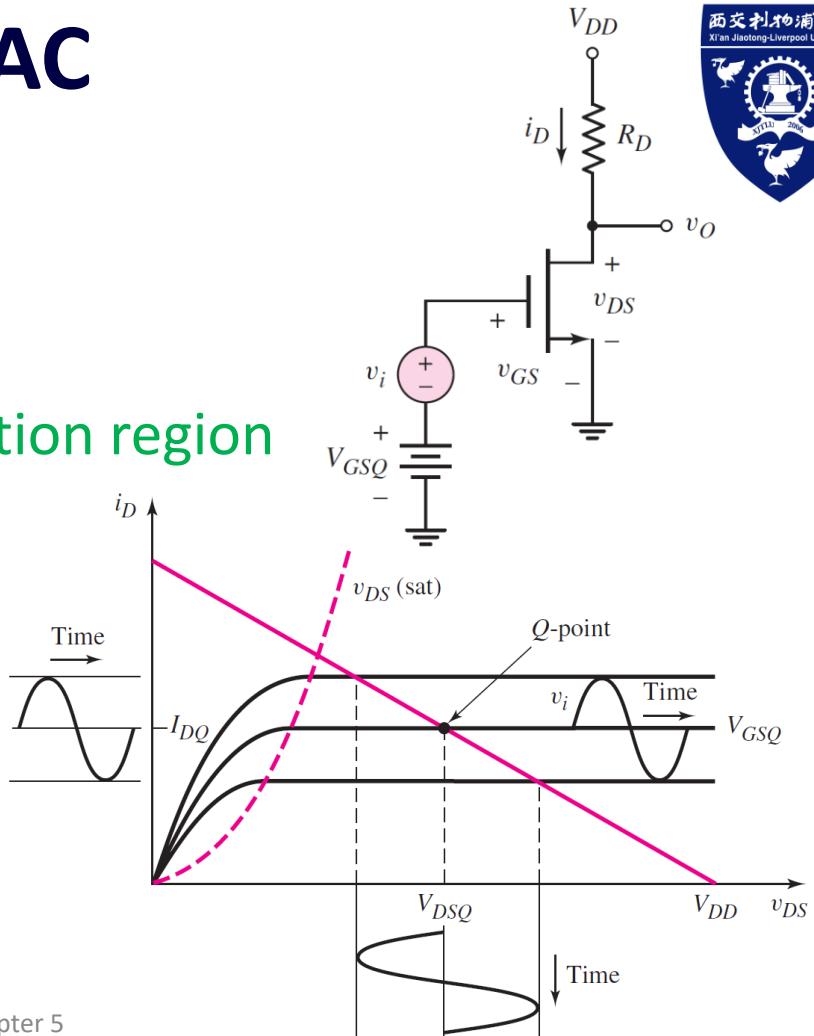
- The transistor is biased in the **saturation region**

$$i_D = K_n(v_{GS} - V_{TN})^2$$

- Write a KVL equation from  $V_{DD}$  to ground

$$-V_{DD} + i_D R_D + v_{DS} = 0$$

- Q point moves up the load line



# Graphical Analysis: DC + AC

- As  $v_i$  decreases

$$v_{GS} = V_{GSQ} + v_i$$

Total value = dc (fixed) + ac (time-varying)

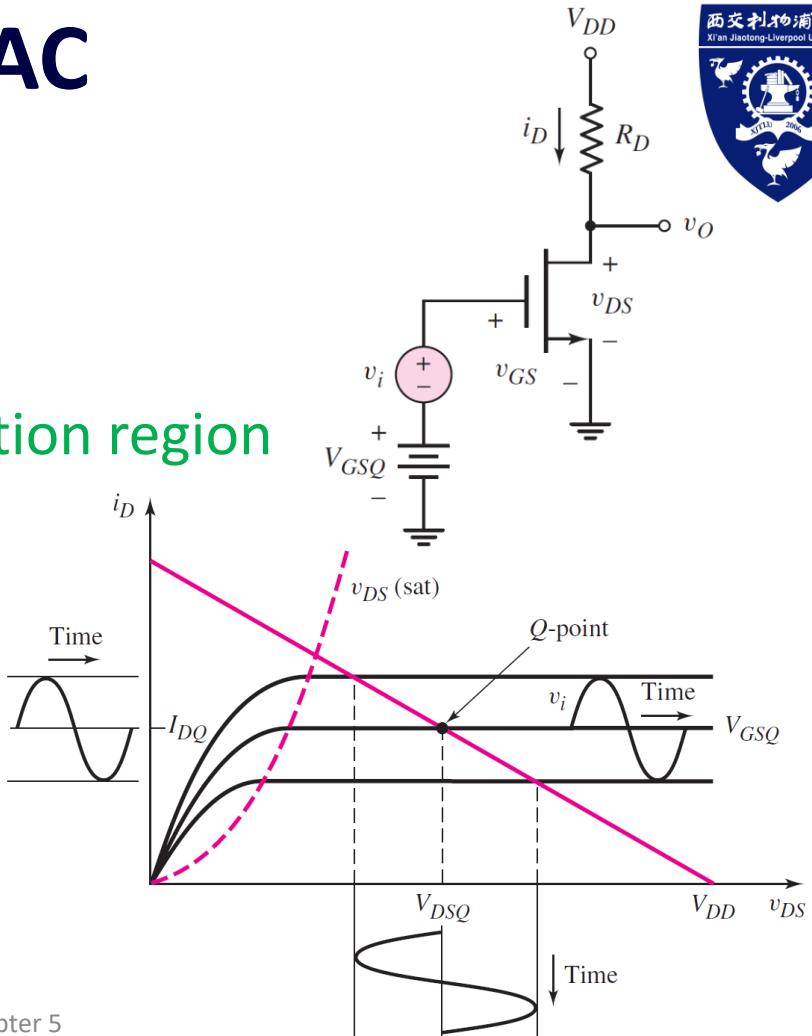
- The transistor is biased in the saturation region

$$i_D = K_n(v_{GS} - V_{TN})^2$$

- Write a KVL equation from  $V_{DD}$  to ground

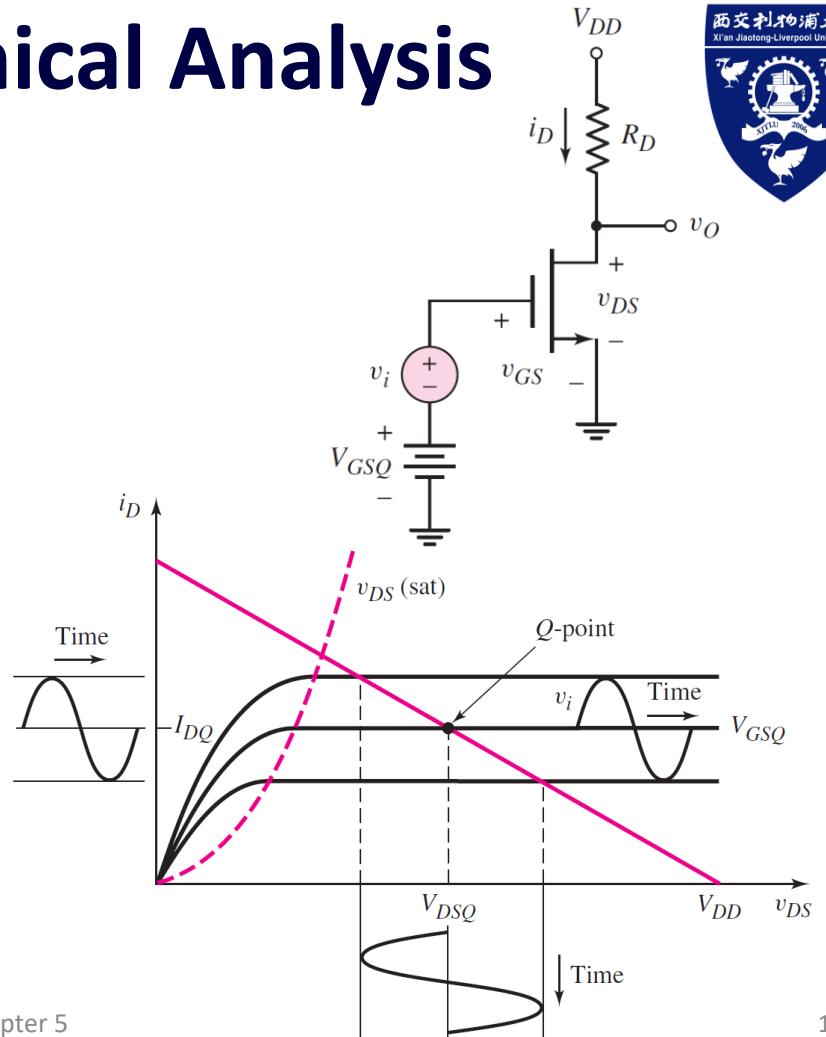
$$-V_{DD} + i_D R_D + v_{DS} = 0$$

- Q point moves down the load line



# A Quick Summary: Graphical Analysis

- As  $v_i$  increases
  - $i_D$  increases
  - $v_{DS}$  decreases
  - Q-point **moves up** the load line
- As  $v_i$  decreases
  - $i_D$  decreases
  - $v_{DS}$  increases
  - Q-point **moves down** the load line
- A **smaller** change at the input ( $v_i$ ), produces a **larger** change at the output ( $v_{DS}$ , i.e.,  $v_O$ )



# Summary of Notations

- **Total value**

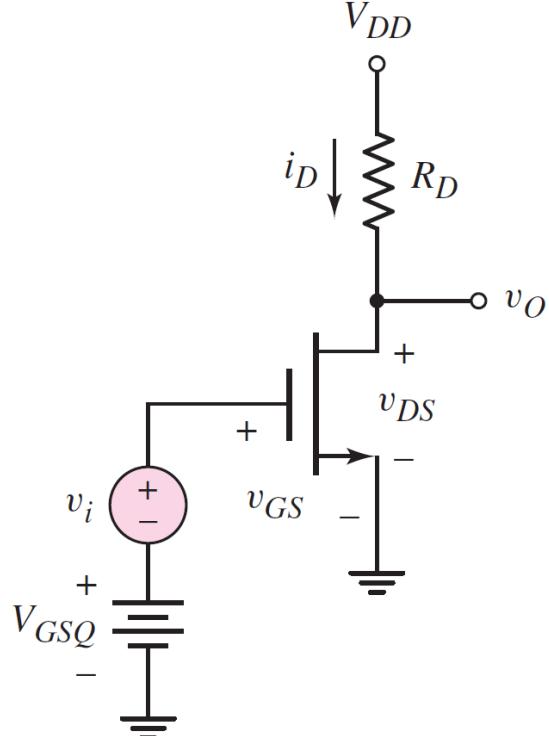
- Lowercase letter and uppercase subscript
- **Total value = dc value + ac value**
  - $i_D = I_{DQ} + i_d$
  - $v_{GS} = V_{GSQ} + v_i$
  - $v_{DS} = v_O = V_{DSQ} + v_{ds}$

- **dc value**

- Uppercase letter and uppercase subscript
- $V_{DD}, V_{GSQ}, I_{DQ}, V_{DSQ}$

- **ac value**

- Lowercase letter and lowercase subscript
- $v_i, i_d, v_{ds}$



# Gate-to-Source Voltage and Drain Current

- The total instantaneous gate-to-source voltage is

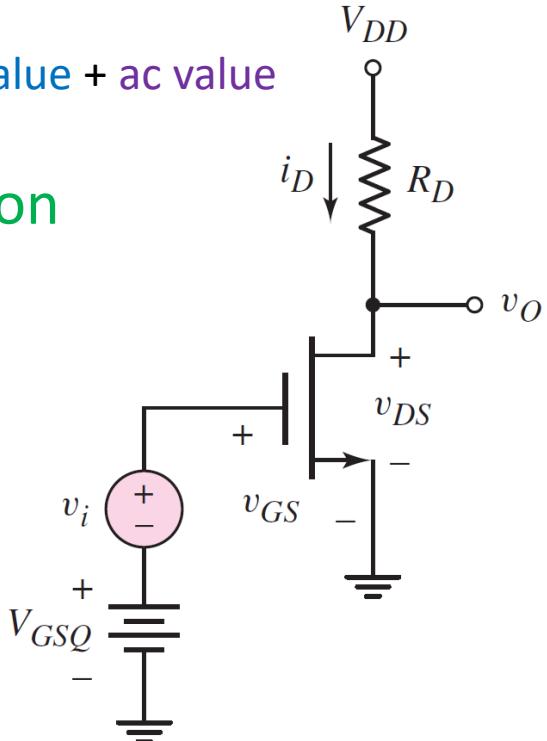
$$v_{GS} = V_{GSQ} + v_i = V_{GSQ} + v_{gs} \rightarrow \text{Total value} = \text{dc value} + \text{ac value}$$

- The transistor is biased in the **saturation region**

$$i_D = K_n(v_{GS} - V_{TN})^2$$

- The **total instantaneous drain current** is

$$i_D = K_n(V_{GSQ} + v_{gs} - V_{TN})^2 = K_n[(V_{GSQ} - V_{TN}) + v_{gs}]^2$$



# Small-Signal: Drain Current

- The total instantaneous drain current is

$$i_D = K_n(V_{GSQ} - V_{TN})^2 + 2K_n(V_{GSQ} - V_{TN})v_{gs} + K_n v_{gs}^2$$

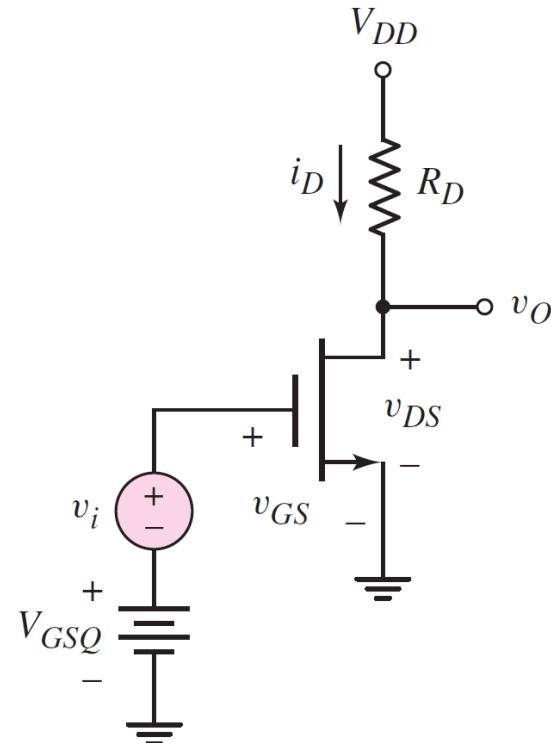
- dc component:  $I_{DQ} = K_n(V_{GSQ} - V_{TN})^2$
- ac component:  $i_d = 2K_n(V_{GSQ} - V_{TN})v_{gs}$ 
  - Small signal condition:  $v_{gs}^2 \ll 2(V_{GSQ} - V_{TN})$

- The  $i_D$  can be simplified as

$$i_D = K_n(V_{GSQ} - V_{TN})^2 + 2K_n(V_{GSQ} - V_{TN})v_{gs}$$

$$i_D = I_{DQ} + i_d$$

Total value = dc value + ac value



# Small-Signal: Drain Current

- The ac component of the drain current is

$$i_d = 2K_n(V_{GSQ} - V_{TN})v_{gs}$$

- Define the transconductance

$$g_m = \frac{i_d}{v_{gs}} = 2K_n(V_{GSQ} - V_{TN}) = 2\sqrt{K_n I_{DQ}} \quad \leftarrow \quad I_{DQ} = K_n(V_{GSQ} - V_{TN})^2$$

- The ac component of the drain current is

$$i_d = g_m v_{gs}$$

# Small-Signal: Output Voltage

- The total instantaneous output voltage is

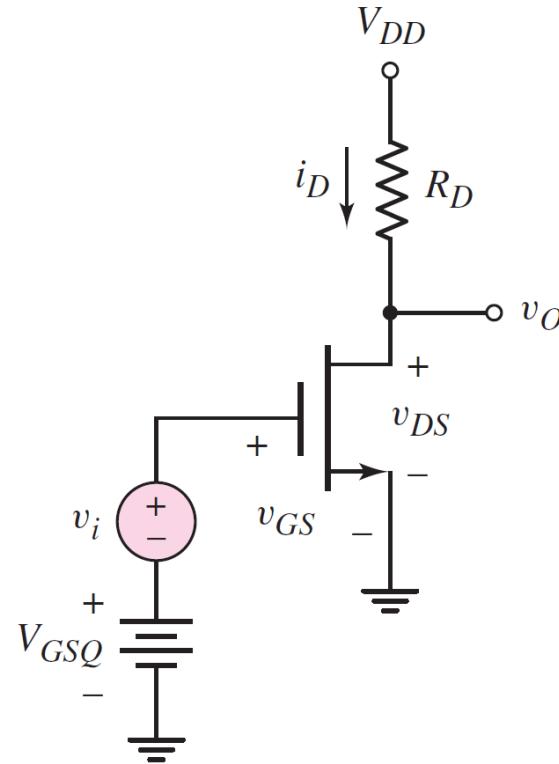
$$v_O = v_{DS} = V_{DD} - i_D R_D \leftarrow \text{KVL equation}$$

$$v_O = V_{DD} - (I_{DQ} + i_d)R_D = (V_{DD} - I_{DQ}R_D) - i_d R_D$$

Total value = dc value + ac value

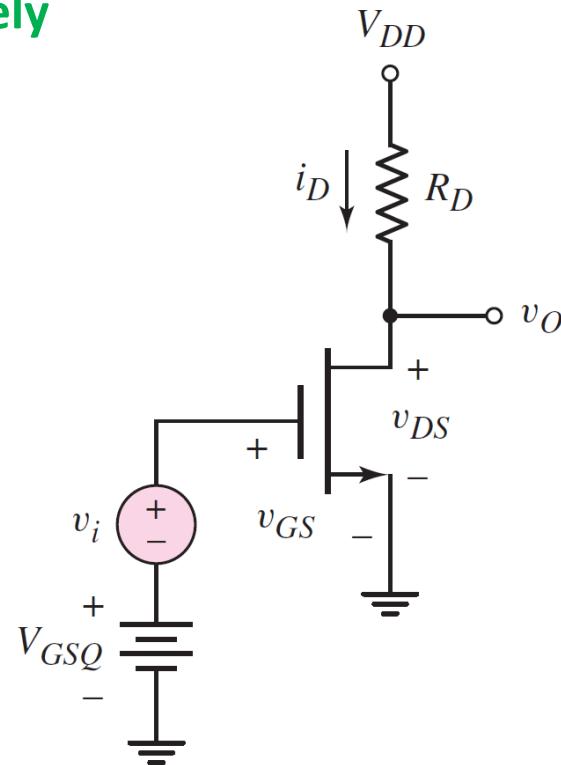
- The ac component of the output voltage is

$$v_o = v_{ds} = -i_d R_D$$



# Superposition: ac analysis + dc analysis

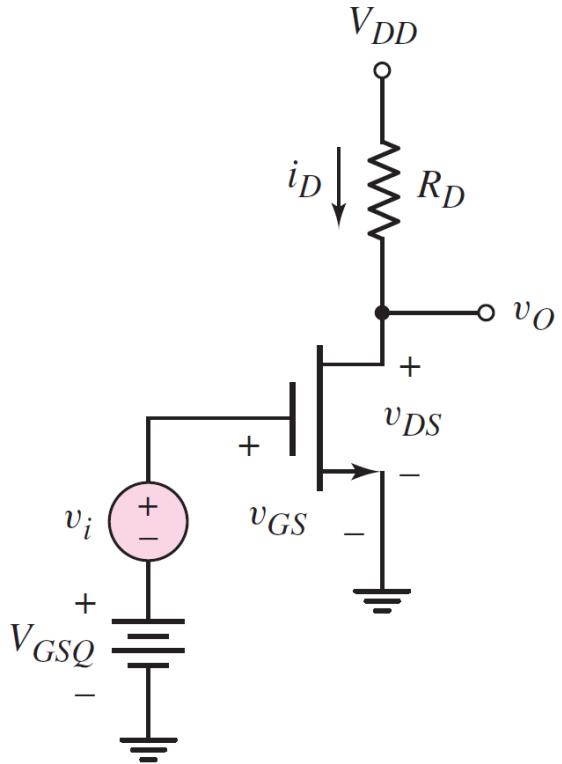
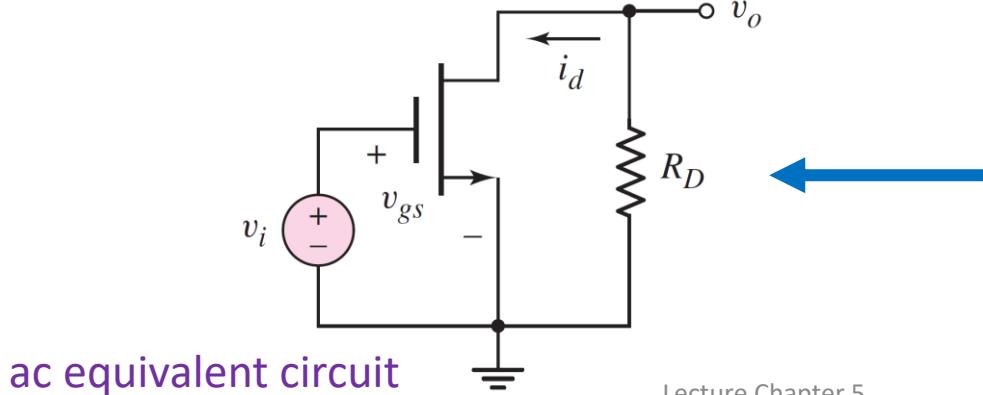
- We use **superposition** method to analysis amplifier circuits
  - dc analysis and **ac analysis** are performed **separately**
    - Step 1: dc analysis
      - The FET must be biased in the saturation region
    - Step 2: ac analysis
- **Step 1: dc analysis → Chapter 3**
  - Set all **ac sources** to zero  $\rightarrow v_i = 0$
  - Find the Q-point ( $V_{DSQ}$ ,  $I_{DQ}$ )



# AC Equivalent Circuit

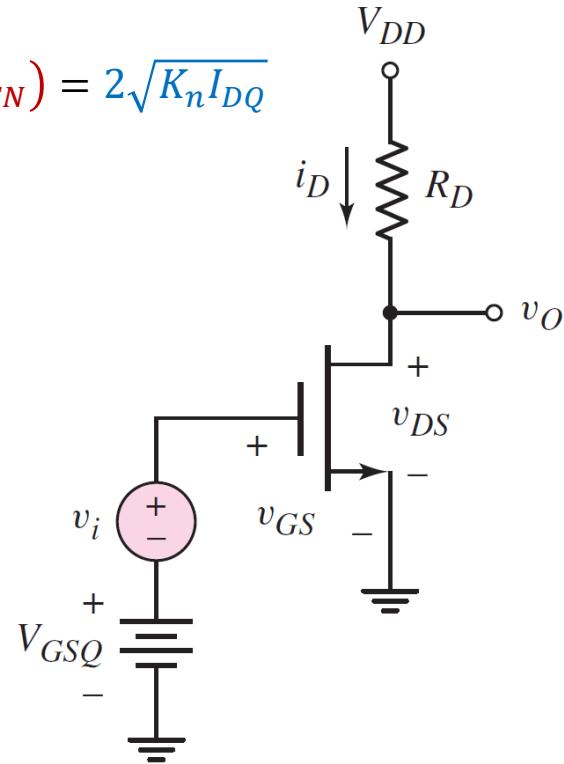
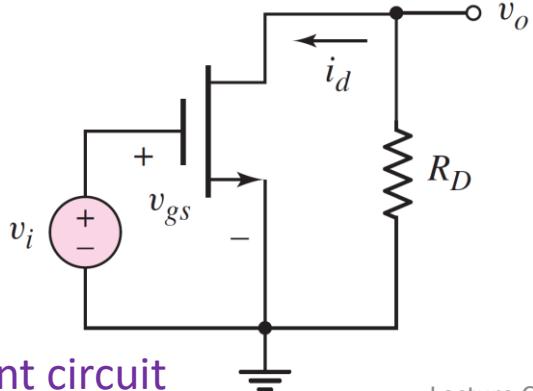
- Step 2: ac analysis

- Set all dc sources to zero  $\rightarrow V_{DD} = 0, V_{GSQ} = 0$



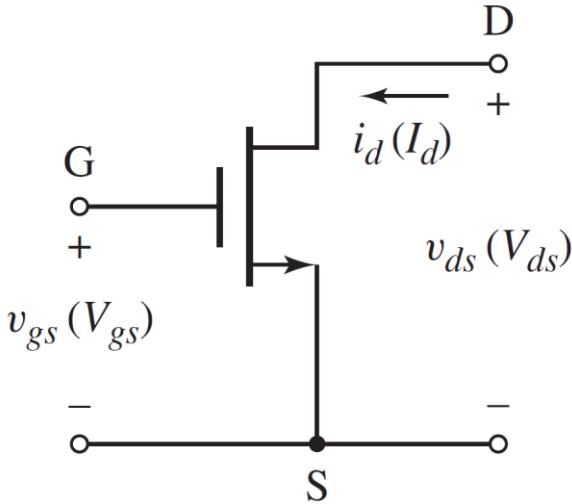
# AC Equivalent Circuit

- In previous slides, we find some **small-signal (ac)** relationships
  - ac component of the drain current is
    - $i_d = g_m v_{gs} = g_m v_i$
    - $g_m = 2K_n(V_{GSQ} - V_{TN}) = 2\sqrt{K_n I_{DQ}}$
  - ac component of the output voltage is
    - $v_o = v_{ds} = -i_d R_D$



# Small-Signal Model of a n-MOSFET

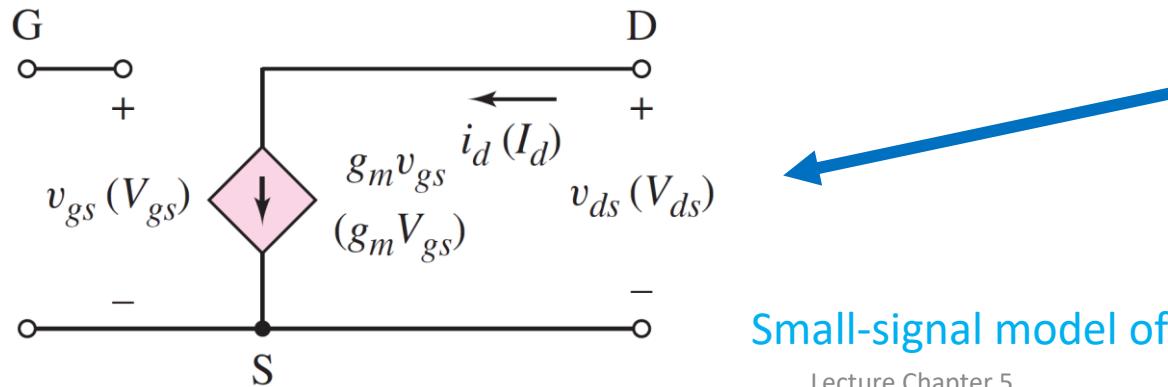
- In ac analysis for a n-MOSFET:
  - Open circuit between gate and source
    - ac value:  $v_{gs}$
    - Phosor value:  $V_{gs}$
  - Current flows from drain to source
    - ac value:  $i_d, v_{ds}$
    - Phosor value:  $I_d, V_{ds}$
  - The relationship between  $V_{gs}$  and  $I_d$  is
    - $I_d = g_m V_{gs}$
    - The gate-to-source voltage controls the drain current



# Small-Signal Model of a n-MOSFET

- In ac analysis for a n-MOSFET:

- Open circuit between gate and source
- Current flows from drain to source
- The gate-to-source voltage controls the drain current:
  - $I_d = g_m V_{gs}$
  - A voltage-controlled current source between drain and source



- In ac analysis for a n-MOSFET:
  - Open circuit between gate and source
  - Current flows from drain to source
  - The gate-to-source voltage controls the drain current
    - $I_d = g_m V_{gs}$
    - A voltage-controlled current source between drain and source

Small-signal model of n-MOSFET

# Small-Signal Model of a n-MOSFET

- NMOS biased in saturation region with finite output resistance
  - Nonzero slope in the  $i_D$  versus  $v_{DS}$  curve

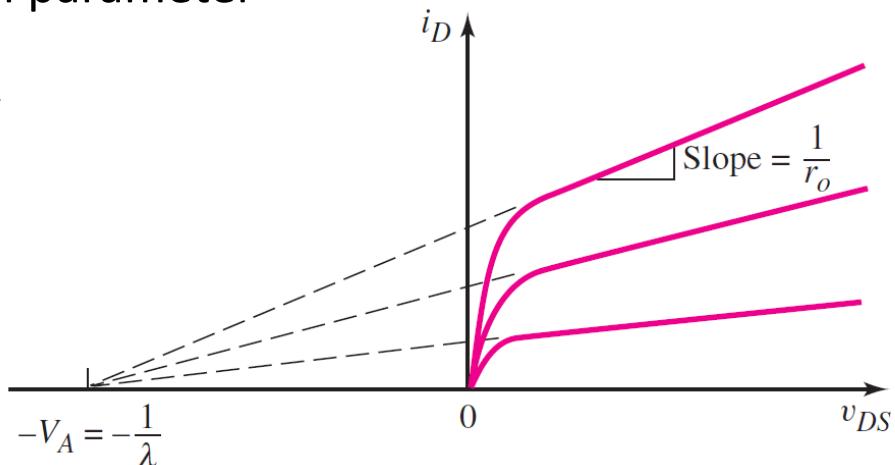
$$i_D = K_n [(v_{GS} - V_{TN})^2 (1 + \lambda v_{DS})]$$

- $\lambda$  is the channel-length modulation parameter

$$r_o = \left( \frac{\partial i_D}{\partial v_{DS}} \right)^{-1} = [\lambda K_n (V_{GSQ} - V_{TN})^2]^{-1}$$

- The finite output resistance is

$$r_o \cong [\lambda I_{DQ}]^{-1}$$



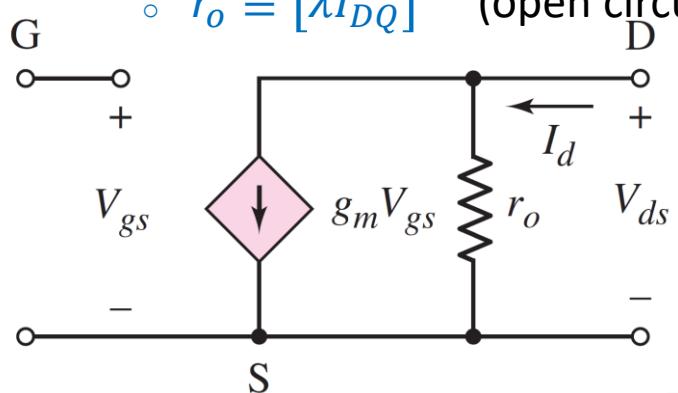
# Small-Signal Model of a n-MOSFET

- The small-signal model of a n-MOSFET consists of three parts:

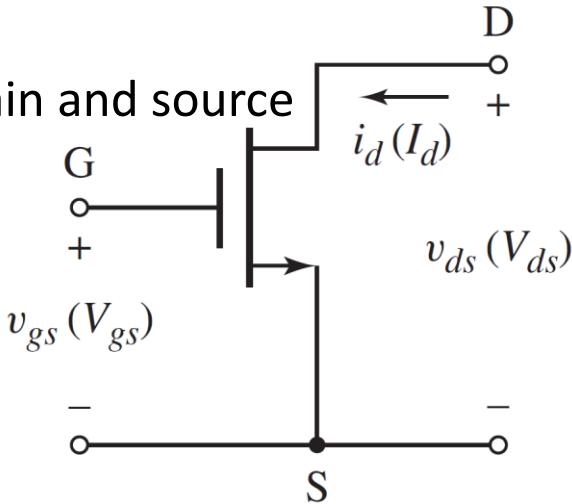
- 1. Open circuit between gate and source
  - $V_{gs}$

- 2. A voltage-controlled current source between drain and source
  - $I_d = g_m V_{gs}$

- 3. A resistor between drain and source
  - $r_o \cong [\lambda I_{DQ}]^{-1}$  (open circuit when  $\lambda = 0$ )

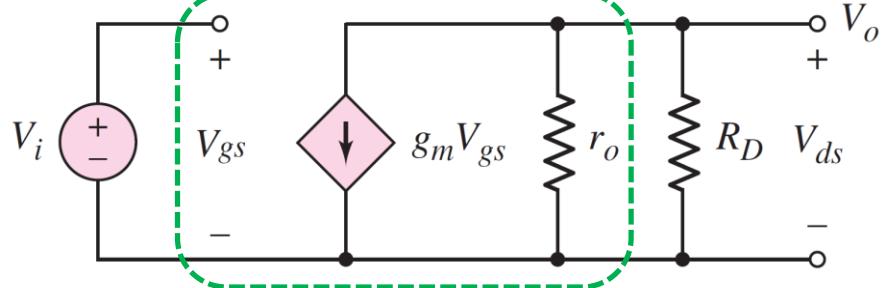


Small-signal model of n-MOSFET  
with finite output resistance

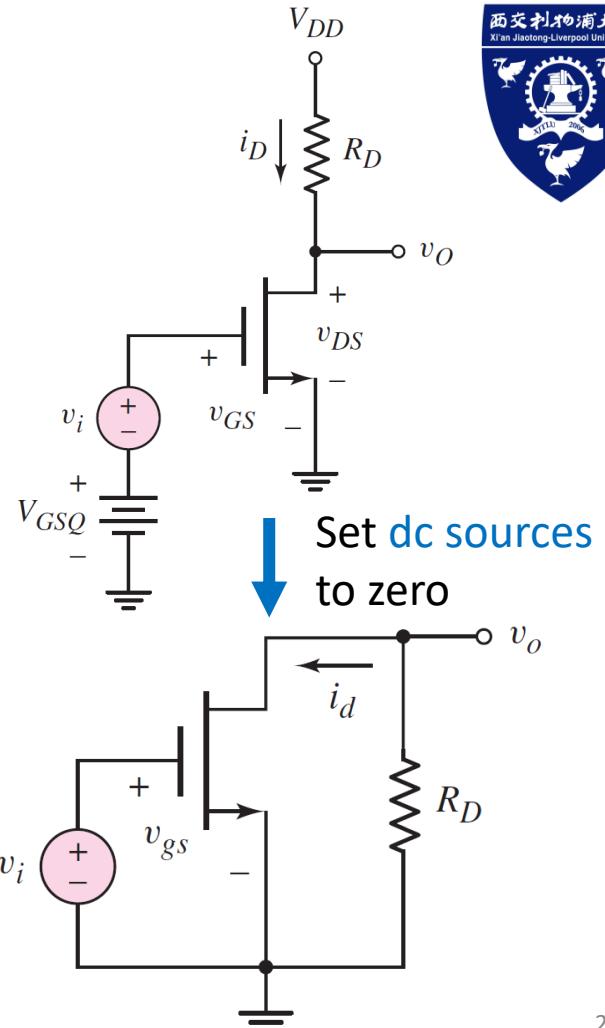


# Small-Signal Equivalent Circuit

- To analyze a linear amplifier circuit
  - Step 1: dc analysis
    - The FET must be biased in the saturation region
  - Step 2: ac analysis
    - Set **dc sources** to zero
    - Small-signal model of FET**
    - Small-signal equivalent circuit** ←



Lecture Chapter 5



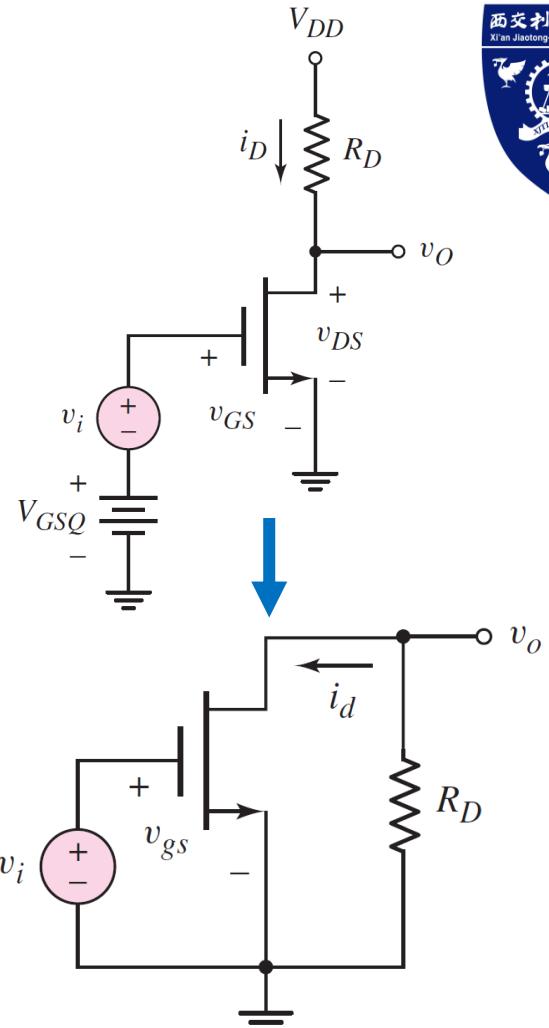
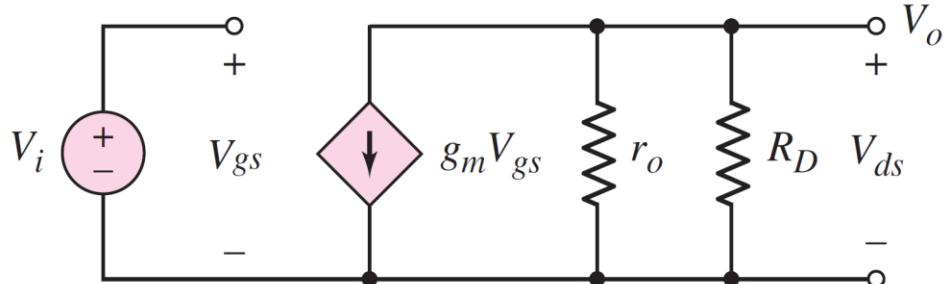
# Small-Signal Voltage Gain

- In this small-signal equivalent circuit
  - The output voltage is

$$V_o = V_{ds} = -g_m V_{gs} (r_o \parallel R_D)$$

- The input voltage is

$$V_i = V_{gs}$$

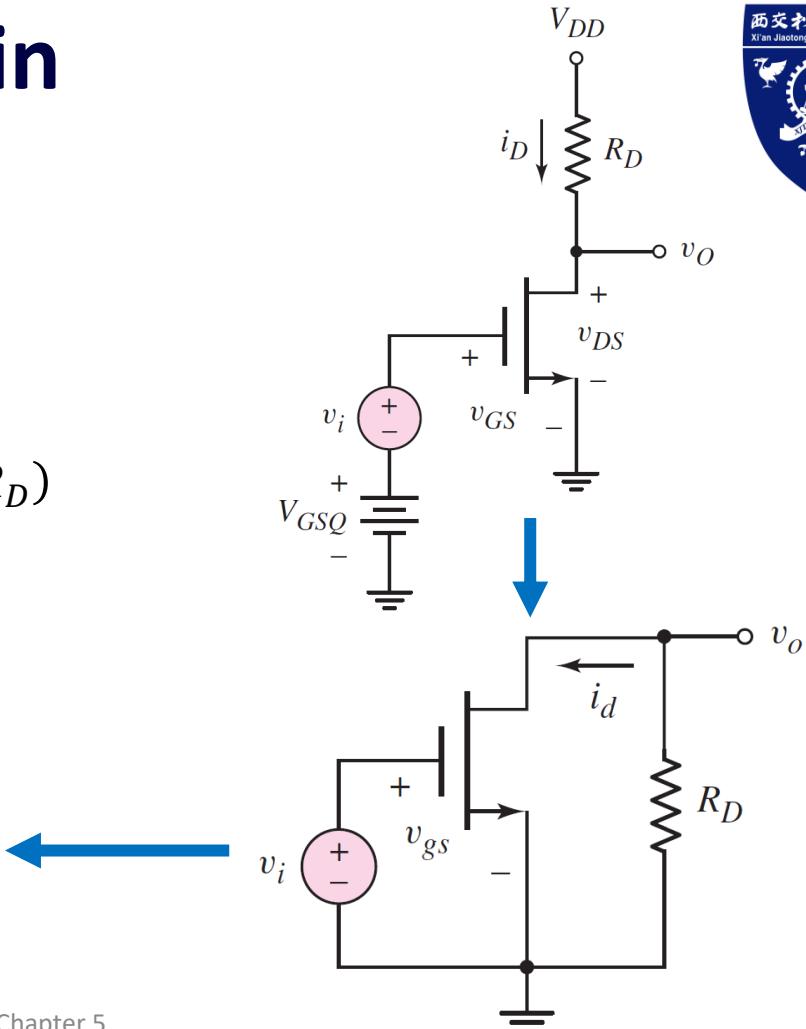
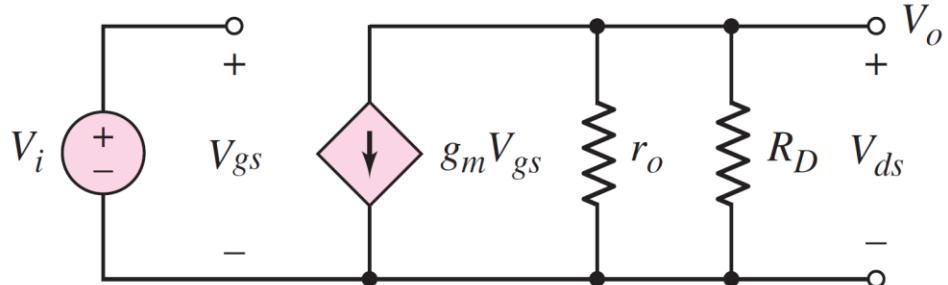


# Small-Signal Voltage Gain

- The small-signal voltage gain  $A_v$  is

- $$A_v = \frac{\text{Output voltage}}{\text{Input voltage}}$$

$$A_v = \frac{V_o}{V_i} = \frac{-g_m V_{gs} (r_o \parallel R_D)}{V_{gs}} = -g_m (r_o \parallel R_D)$$

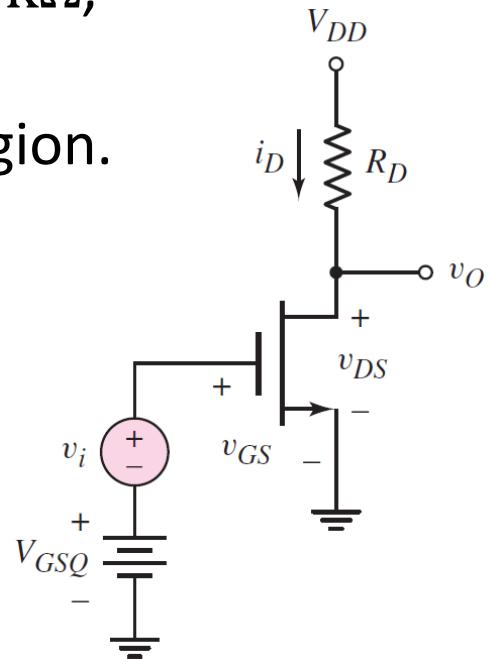


# Example 5.1

Determine the small-signal voltage gain of a MOSFET circuit.

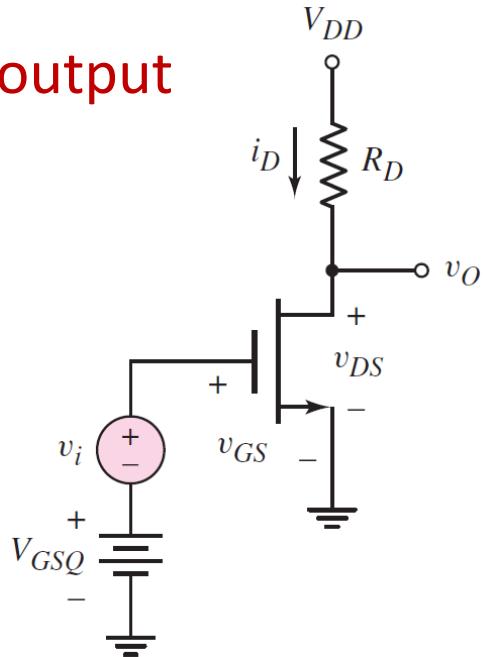
Assumptions:  $V_{GSQ} = 2.21$  V,  $V_{DD} = 5$  V,  $R_D = 2.5$  k $\Omega$ ,  
 $V_{TN} = 1$  V,  $K_n = 0.8$  mA/V $^2$ ,  $\lambda = 0.02$  V $^{-1}$

Assume the transistor is biased in the saturation region.



# Example 5.1-Hints

1. dc analysis: determine  $I_{DQ}$
2. ac analysis: draw the ac equivalent circuit
3. Determine the **transconductance** and the **finite output resistance**



# Problem-Solving Technique

- Superposition
  - The dc and ac analyses are performed **separately**
- The analysis of the MOSFET amplifier proceeds as follows:
  - Step 1. dc analysis
    - Analyze circuit with only the dc sources to find **quiescent solution (Q-point)**.
      - $V_{DSQ}$  and  $I_{DQ}$
    - Transistor must be biased in **saturation region** for linear amplifier.
      - $V_{DSQ} > V_{DS(\text{sat})} = V_{GSQ} - V_{TN}$
  - Step 2. ac analysis
    - Replace elements with **small-signal model**.
    - Analyze small-signal equivalent circuit, **setting dc sources to zero**, to produce the circuit to the time-varying input signals only.

# Practical Skill: General DC & AC Analysis

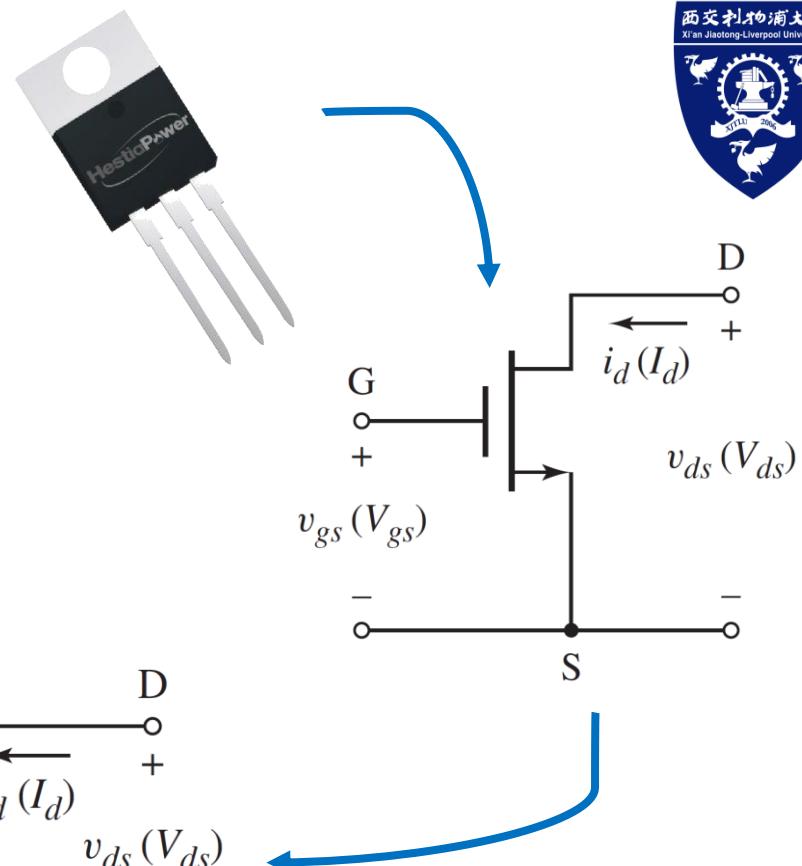
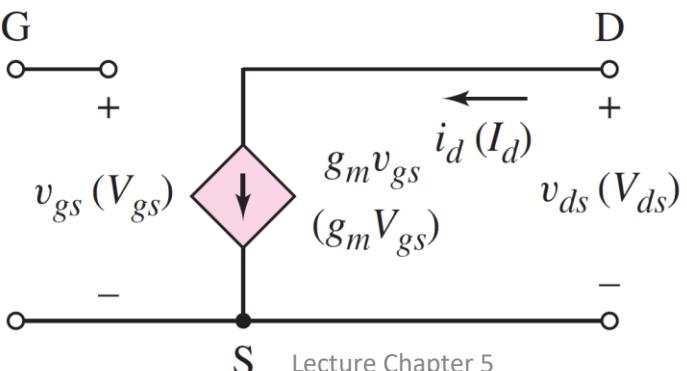
- **dc analysis:** find the dc equivalent circuit
  - Replace all capacitors by open circuits
  - Replace all inductors by short circuits
  - Replacing **ac** voltage sources by short circuits
  - Replacing **ac** current sources by open circuits
- **ac analysis:** find the ac equivalent circuit
  - Replace all capacitors by short circuits
  - Replace all inductors by open circuits
  - Replace **dc** voltage sources by short circuits
  - Replace **dc** current sources by open circuits

# Basic Transistor Amplifier Configuration

Discuss the three basic transistor amplifier configurations

# Amplifier Configurations

- MOSFET is a **three-terminal** device
- Three basic configurations
  - Common source
  - Common drain (source follower)
  - Common gate
- Characteristics of amplifiers
  - Input resistance
  - Output resistance
  - Voltage gain

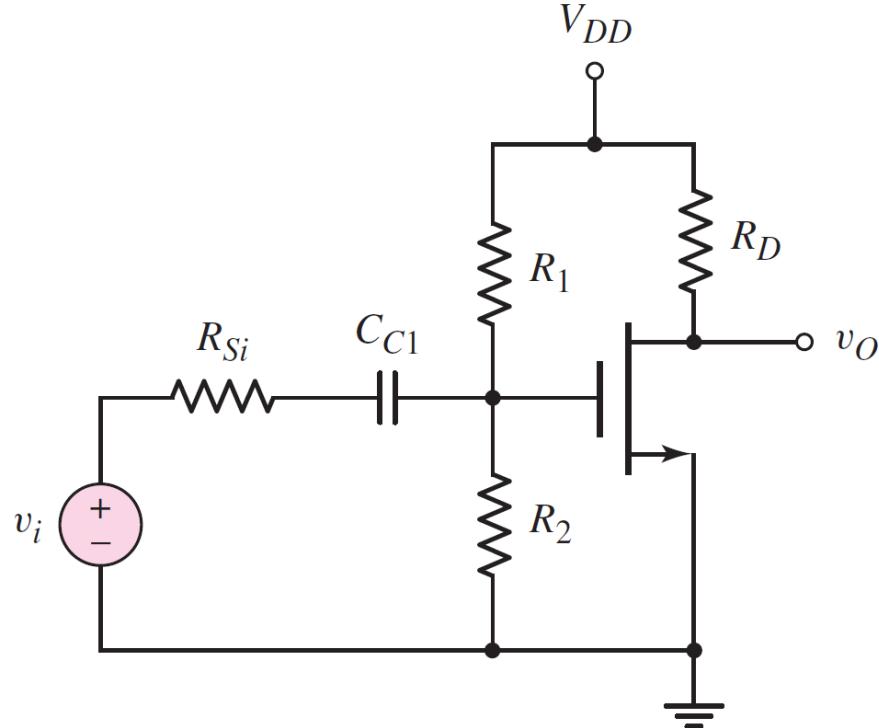


# The Common-Source Amplifier

Analyze the common-source amplifier and become familiar with the general characteristics of this circuit

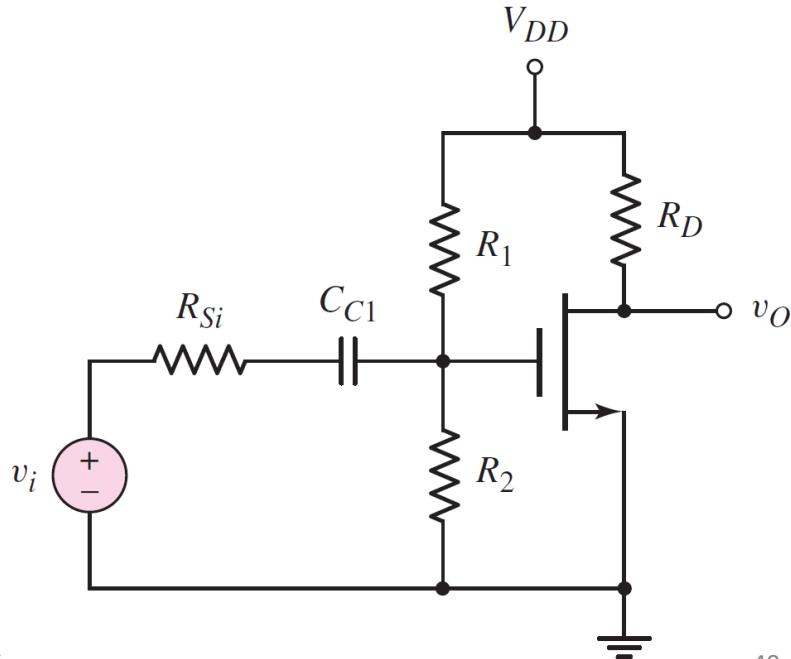
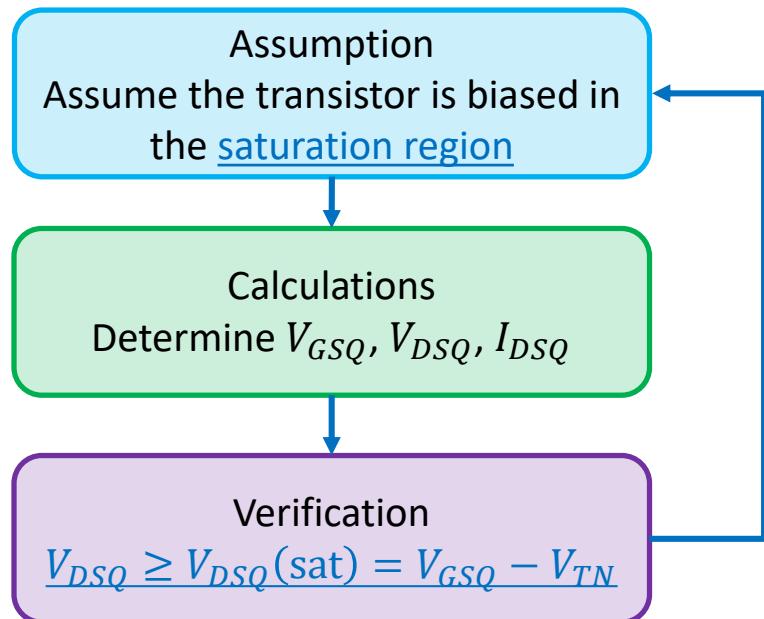
# A Basic Common-Source Configuration

- Common source
  - The source is at **ground** potential
- Coupling capacitor  $C_{C1}$ 
  - Open circuit in dc analysis
  - Short circuit in ac analysis
  - $|Z_C| = \frac{1}{2\pi f C_{C1}}$
- dc transistor **biasing**
  - $R_1$  and  $R_2$



# Common-Source Amplifier Circuit

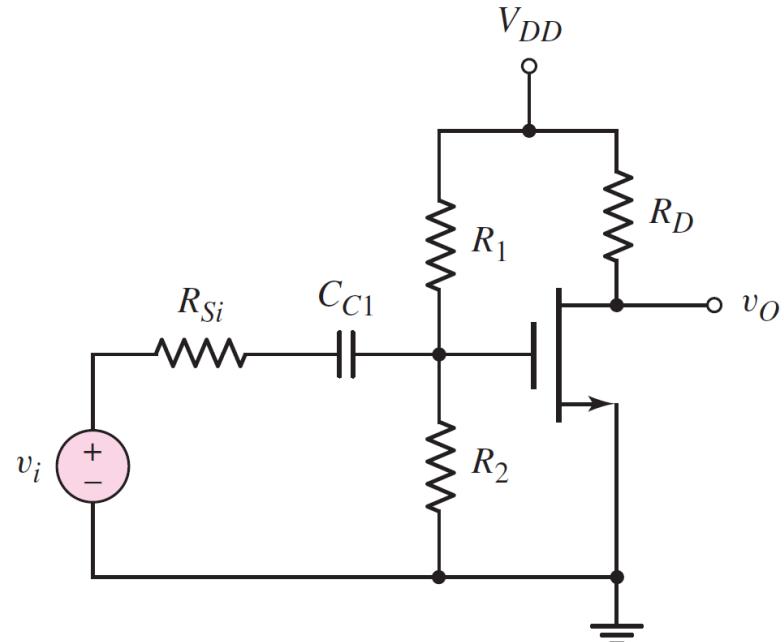
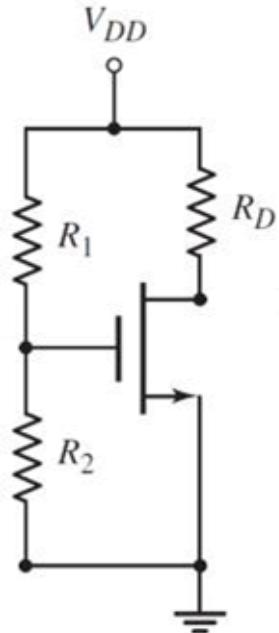
- Signal source:  $v_i$  is in series with  $R_{Si}$
- Step 1: dc analysis → Chapter 3
  - MOSFET is biased in the saturation region



# Step 1: DC Analysis

- Set ac sources to zero, and replace capacitors by open circuits
- Assume transistor is biased in the saturation region

$$I_{DQ} = K_n(V_{GSQ} - V_{TN})^2$$

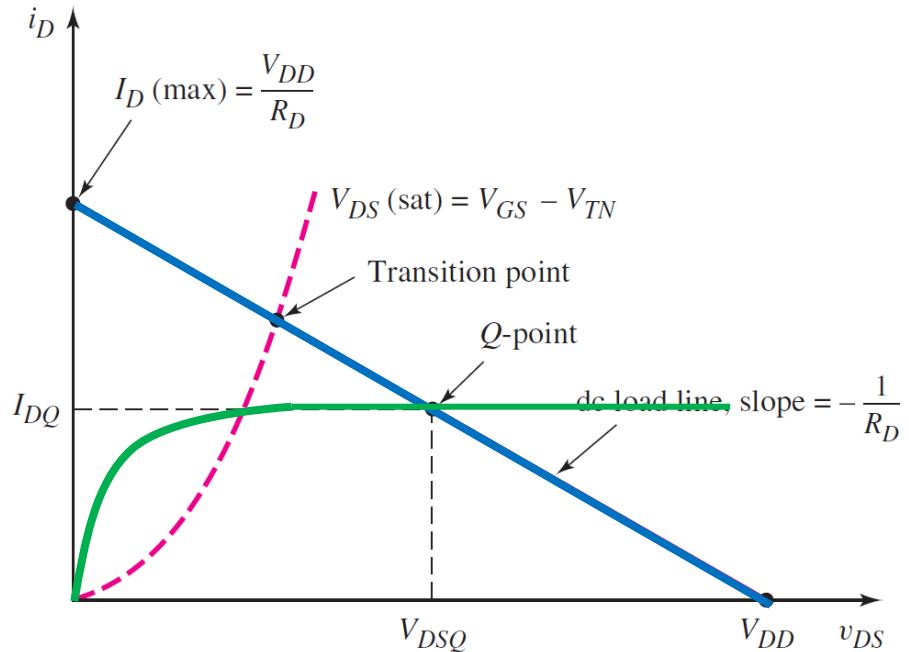
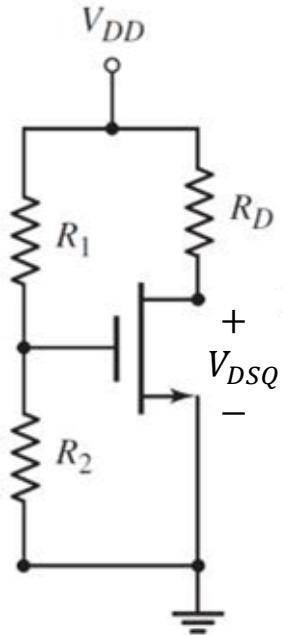


# Step 1: DC Analysis

- Write a KVL equation from  $V_{DD}$ -drain-ground, to obtain the **dc load line**

$$I_{DQ} = -\frac{1}{R_D}V_{DSQ} + V_{DD}$$

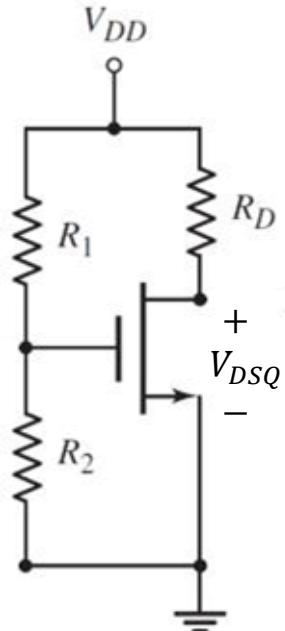
$$I_{DQ} = K_n(V_{GSQ} - V_{TN})^2$$



# Step 1: DC Analysis

- Verify the transistor is biased in the saturation region

$$V_{GSQ} = V_G - V_S = \frac{R_2}{R_1 + R_2} V_{DD} - 0 = \frac{R_2}{R_1 + R_2} V_{DD}$$



$$I_{DQ} = K_n (V_{GSQ} - V_{TN})^2$$

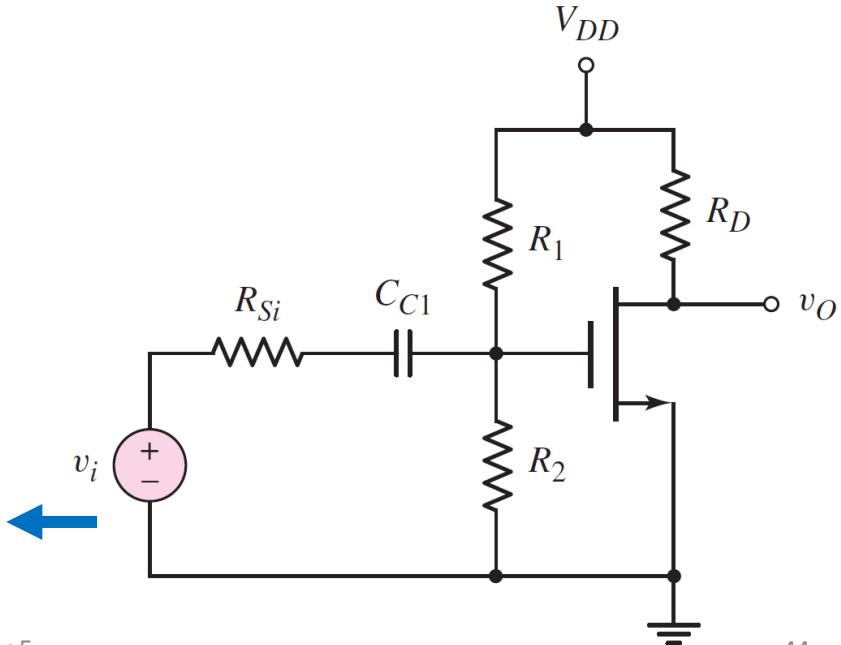
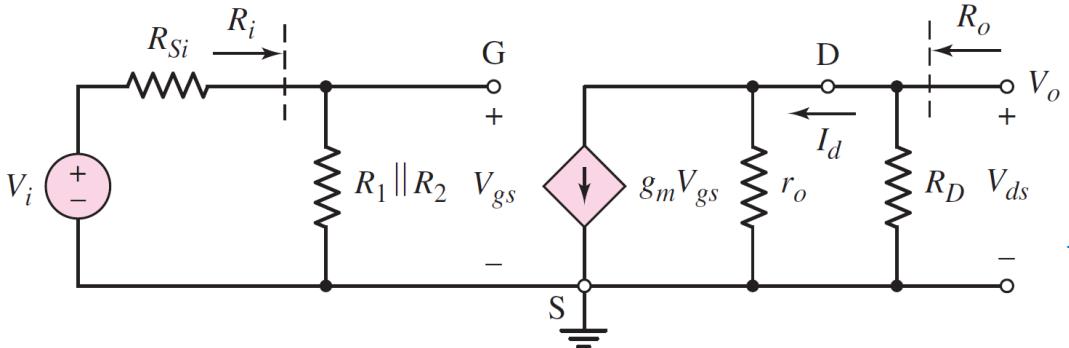
$$I_{DQ} = -\frac{1}{R_D} V_{DSQ} + V_{DD}$$

**Verification:**  $V_{DSQ} \geq V_{DSQ}(\text{sat}) = V_{GSQ} - V_{TN}$

# Step 2: Small-Signal Equivalent Circuit

- In ac analysis

- Set dc voltage sources to zero  $\rightarrow V_{DD} = 0$
- Replace all capacitors by short circuits
- Small-signal model of FET
- Small-signal equivalent circuit

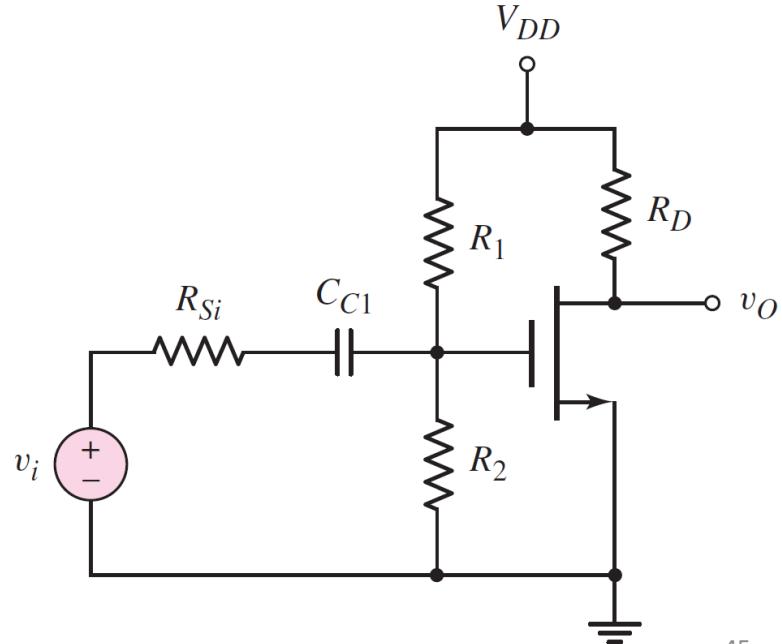
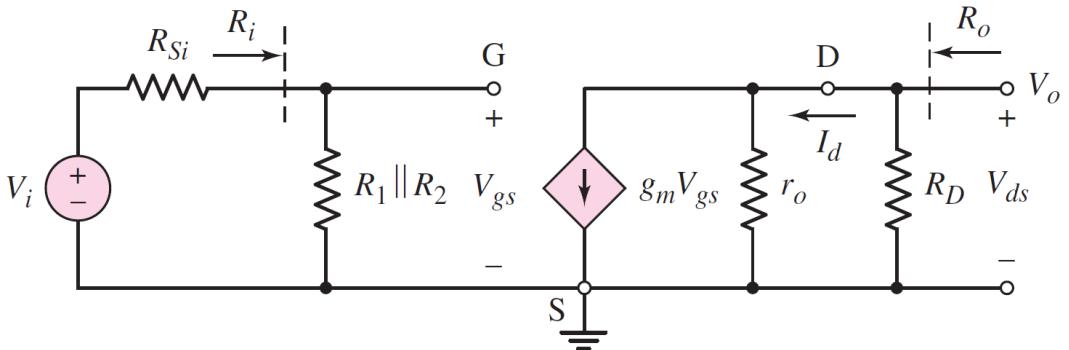


# Step 2: Small-Signal Voltage Gain

- The output voltage is
- The input gate-to-source voltage is

$$V_o = -g_m V_{gs} (r_o \parallel R_D)$$

$$V_{gs} = \frac{R_1 \parallel R_2}{R_1 \parallel R_2 + R_{Si}} V_i$$



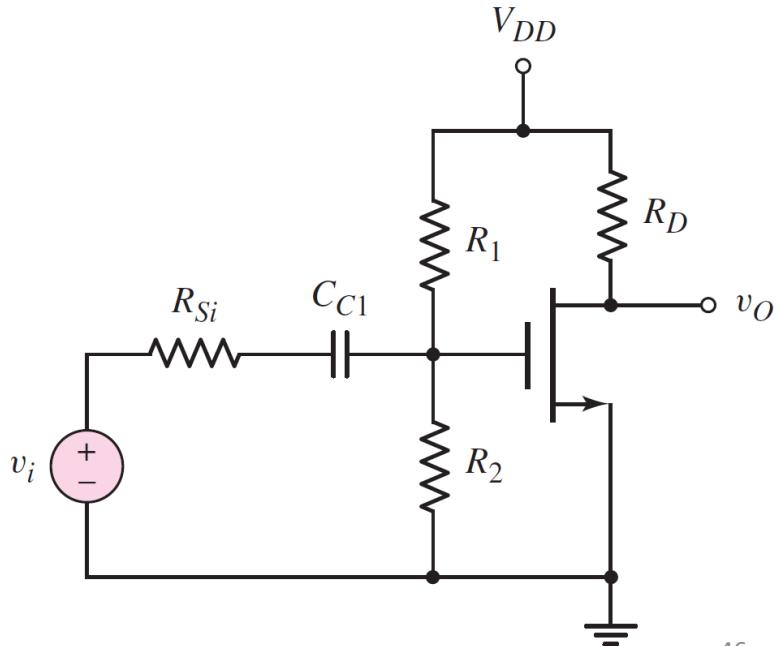
# Step 2: Small-Signal Voltage Gain

- The small-signal voltage gain is

$$A_v = \frac{V_o}{V_i} = -g_m(r_o \parallel R_D) \frac{R_1 \parallel R_2}{R_1 \parallel R_2 + R_{Si}}$$

- $g_m$  and  $r_O$  are small-signal parameters

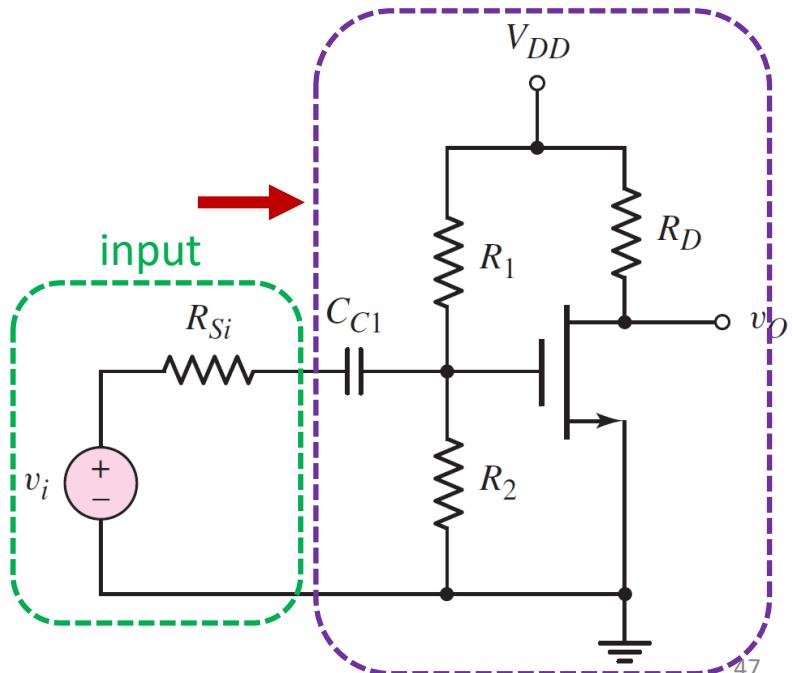
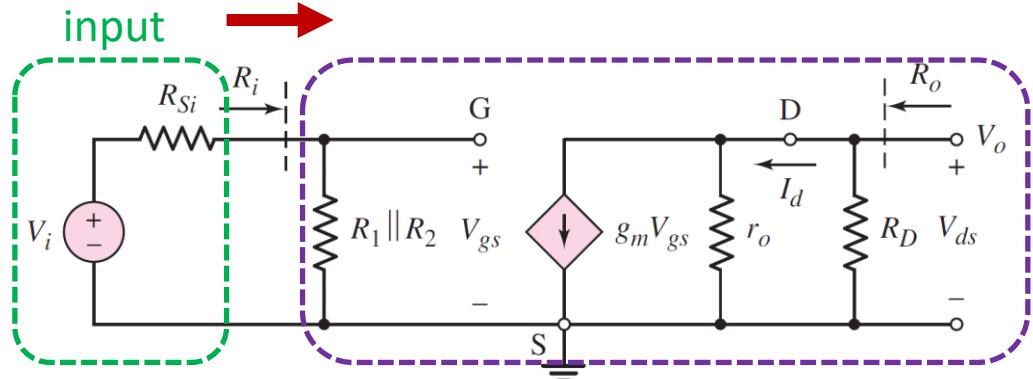
- $g_m = 2K_n(V_{GSQ} - V_{TN}) = 2\sqrt{K_n I_{DQ}}$
  - $r_o = [\lambda I_{DQ}]^{-1}$



# Input and Output Resistance

- The **input resistance** is the equivalent resistance of the circuit **looking into** the gate terminal (because the source signal is applied at the gate)

$$R_i = R_1 \parallel R_2$$



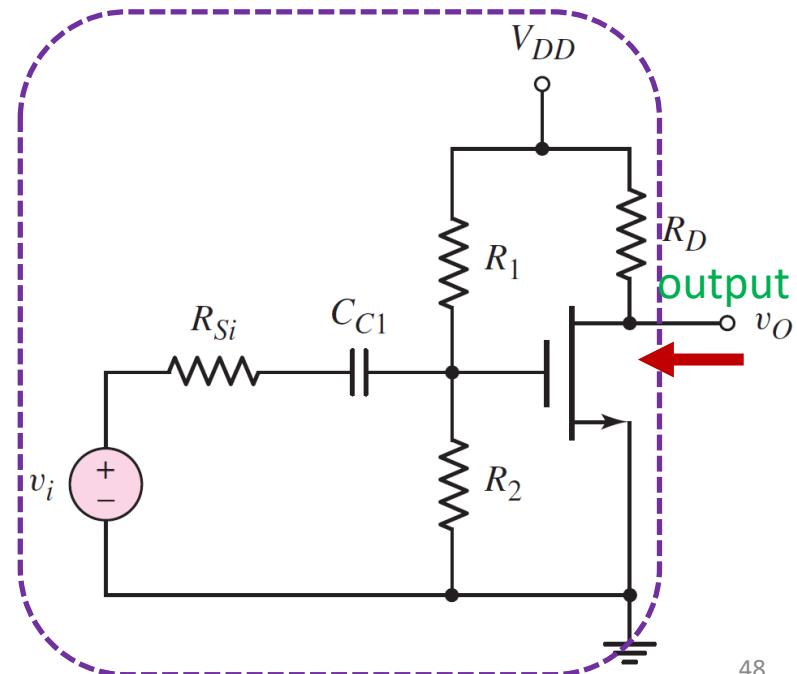
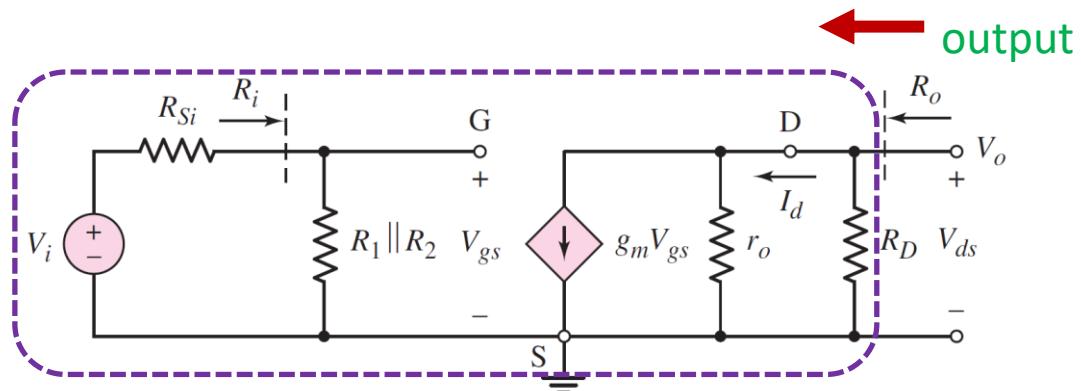
# Input and Output Resistance

- The output resistance is the equivalent resistance looking back into the output terminals

- Set independent source to zero  $V_i = 0$

$$V_i = 0 \rightarrow V_{gs} = 0 \rightarrow g_m V_{gs} = 0 \rightarrow \text{open circuit}$$

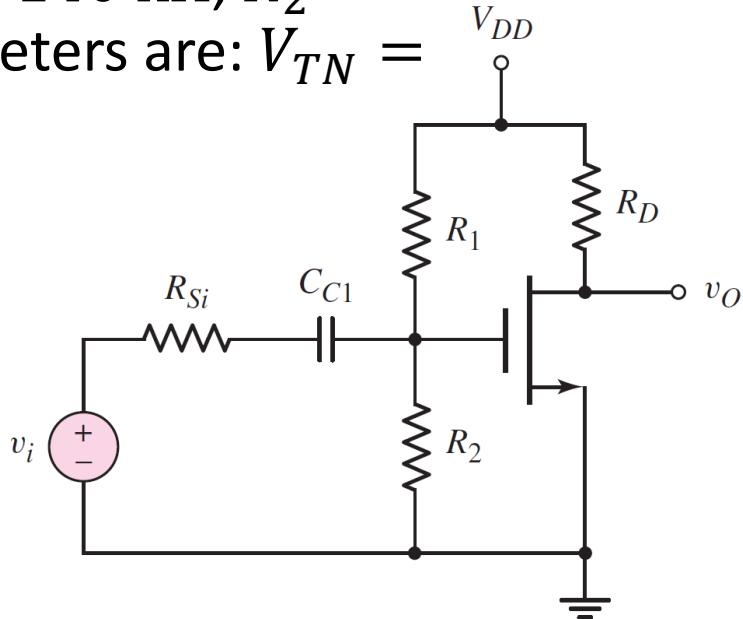
$$R_o = R_D \parallel r_o$$



# Example 5.2

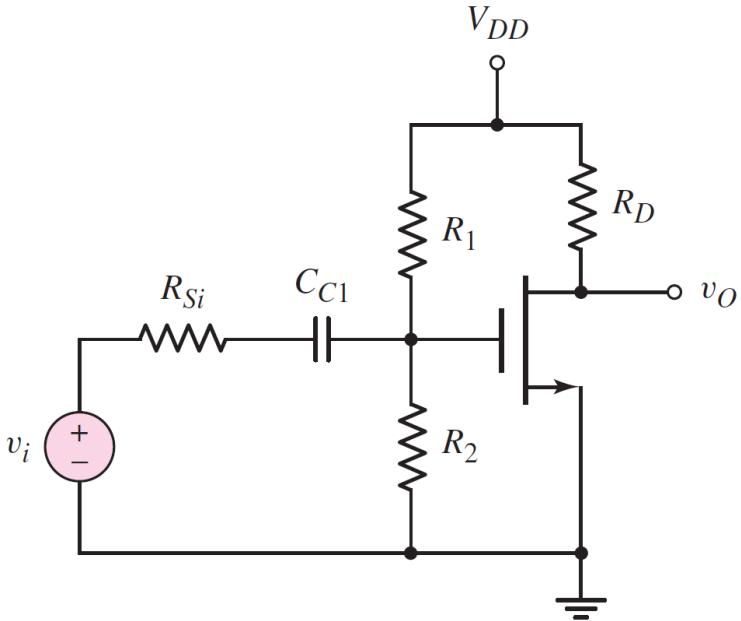
Determine the small-signal voltage gain and input and output resistances of a common-source amplifier.

Assume  $V_{DD} = 3.3$  V,  $R_D = 10$  k $\Omega$ ,  $R_1 = 140$  k $\Omega$ ,  $R_2 = 60$  k $\Omega$ ,  $R_{Si} = 4$  k $\Omega$ . The transistor parameters are:  $V_{TN} = 0.4$  V,  $K_n = 0.5$  mA/V $^2$ ,  $\lambda = 0.02$  V $^{-1}$



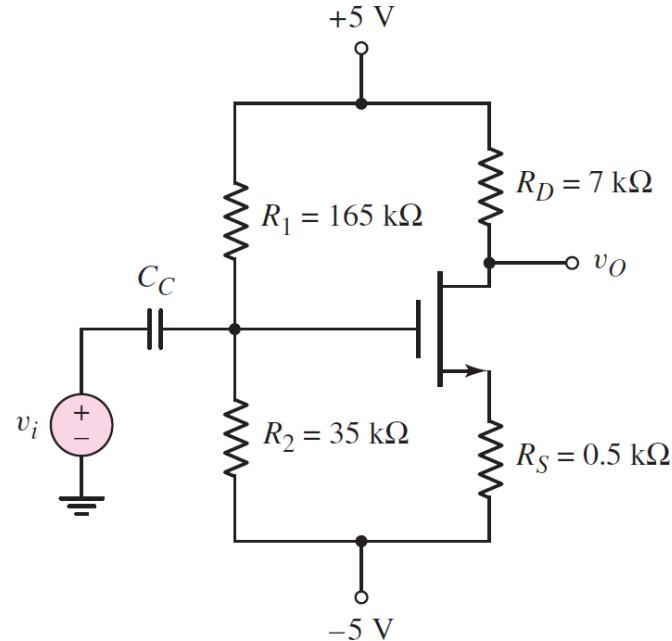
# Example 5.2-Hints

1. dc analysis: determine  $I_{DQ}$
2. ac analysis: small-signal equivalent circuit



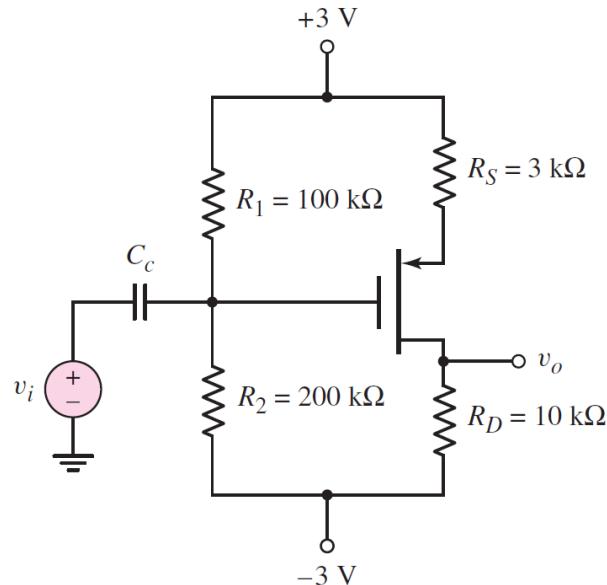
# Common-Source Amplifier with Source Resistor

- There is a resistor  $R_S$  between the source and ground
  - Stabilize** the  $Q$ -point against variations in transistor parameters
  - Reduce the voltage gain



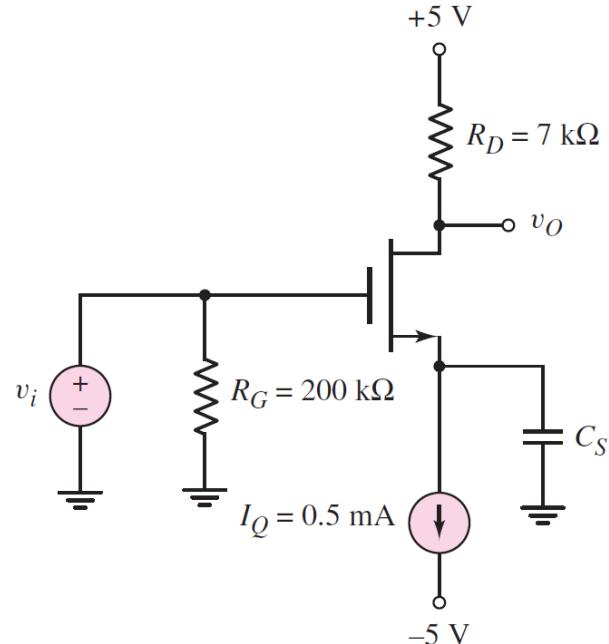
# Example 5.3

Determine the small-signal voltage gain of a PMOS transistor circuit. The transistor parameters are  $V_{TP} = -0.5$  V,  $K_p = 0.80$  mA/V<sup>2</sup>, and  $\lambda = 0$ . The quiescent drain current is found to be  $I_{DQ} = 0.297$  mA.



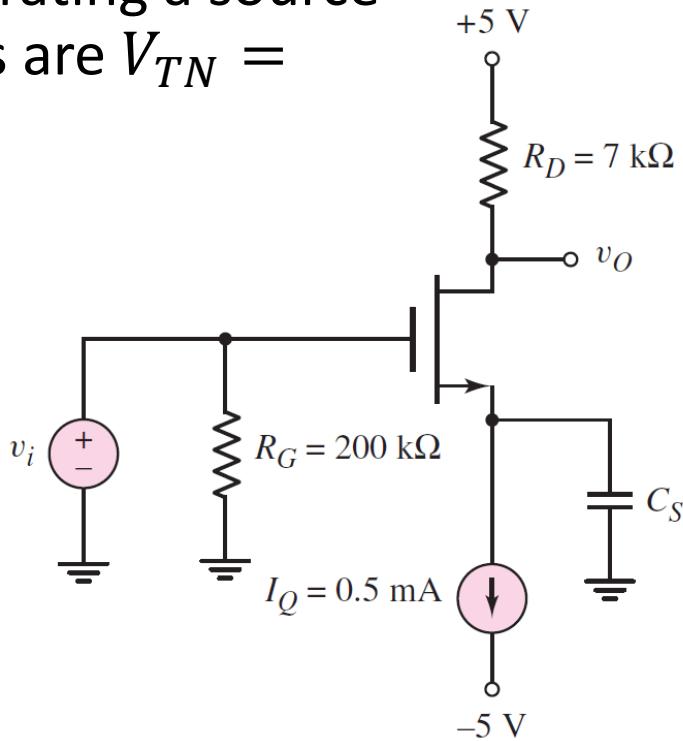
# Common-Source Amplifier with Source Bypass Capacitor

- A **source bypass capacitor** added to the common-source circuit with a source resistor
  - **minimize the loss** in the small-signal voltage gain.
- The source resistor is replaced by the current source to further **stabilize** the  $Q$ -point



# Example 5.4

Determine the small-signal voltage gain of a circuit biased with a constant current source and incorporating a source bypass capacitor. The transistor parameters are  $V_{TN} = 0.8 \text{ V}$ ,  $K_n = 1 \text{ mA/V}^2$ , and  $\lambda = 0$

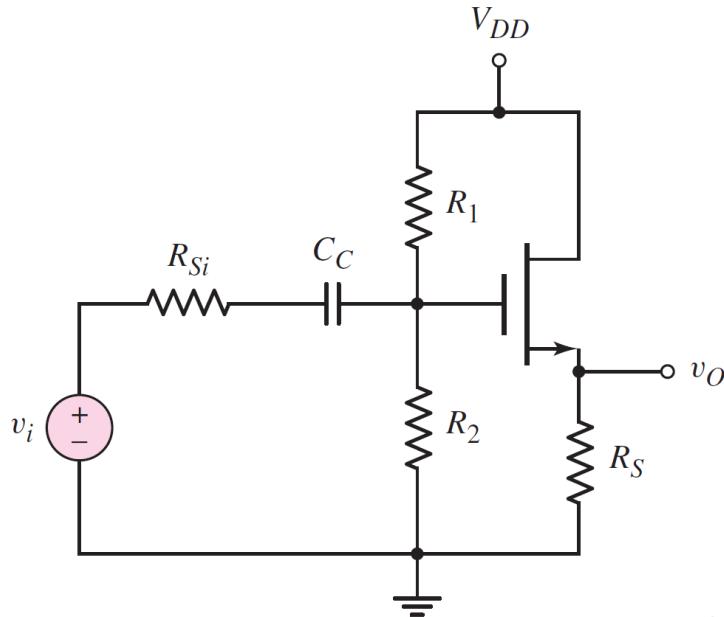


# The Common-Drain (Source-Follower) Amplifier

Analyze the common-drain (source-follower) amplifier and become familiar with the general characteristics of this circuit.

# NMOS Common-Drain Amplifier

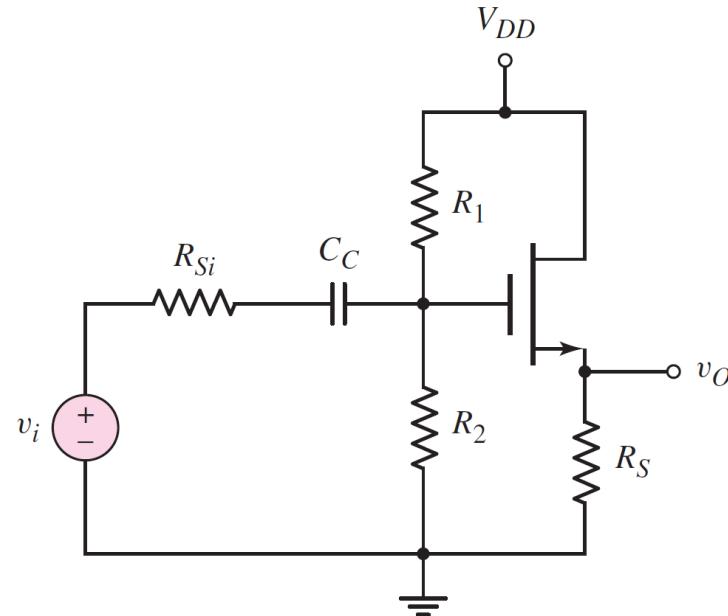
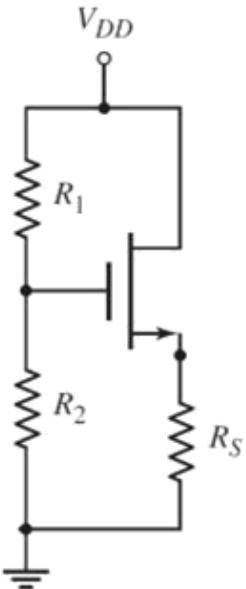
- Common-drain (Source follower) amplifier
- The output signal is taken off the source with respect to ground
- The drain is connected directly to  $V_{DD}$  (ac signal ground)



# Step 1: DC Analysis

- Step 1: dc analysis

- The transistor must be biased in the saturation region
- Determine  $V_{DSQ}$  and  $I_{DQ}$



# Step 1: DC Analysis

- Assume the transistor is biased in the saturation region

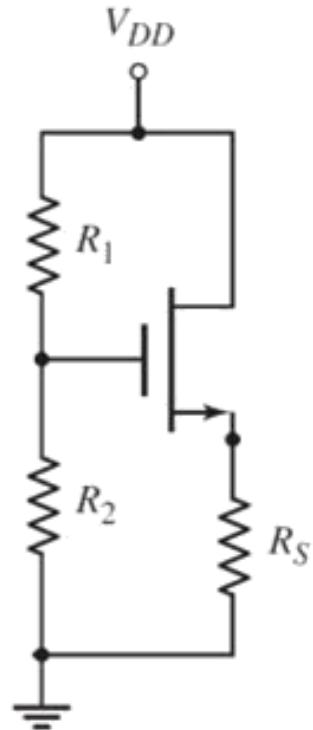
$$I_{DQ} = K_n(V_{GSQ} - V_{TN})^2$$

$$V_{GSQ} = V_G - V_S = \frac{R_2}{R_1 + R_2} V_{DD} - I_{DQ} R_S$$

$$I_{DQ} = K_n \left( \frac{R_2}{R_1 + R_2} V_{DD} - I_{DQ} R_S - V_{TN} \right)^2$$

- A KVL equation from  $V_{DD}$  to ground

$$-V_{DD} + V_{DSQ} + I_{DQ} R_S = 0 \rightarrow V_{DSQ} = V_{DD} - I_{DQ} R_S$$

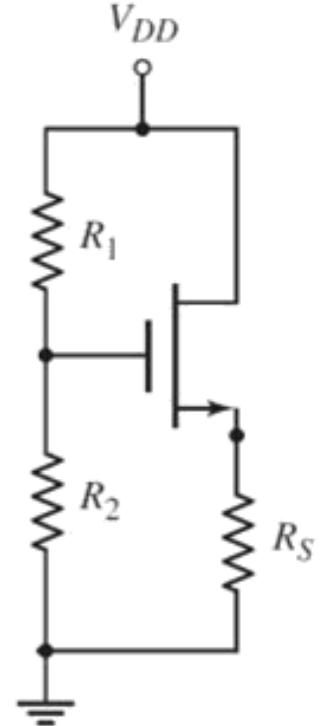


# Step 1: DC Analysis

$$I_{DQ} = K_n \left( \frac{R_2}{R_1 + R_2} V_{DD} - I_{DQ} R_S - V_{TN} \right)^2$$

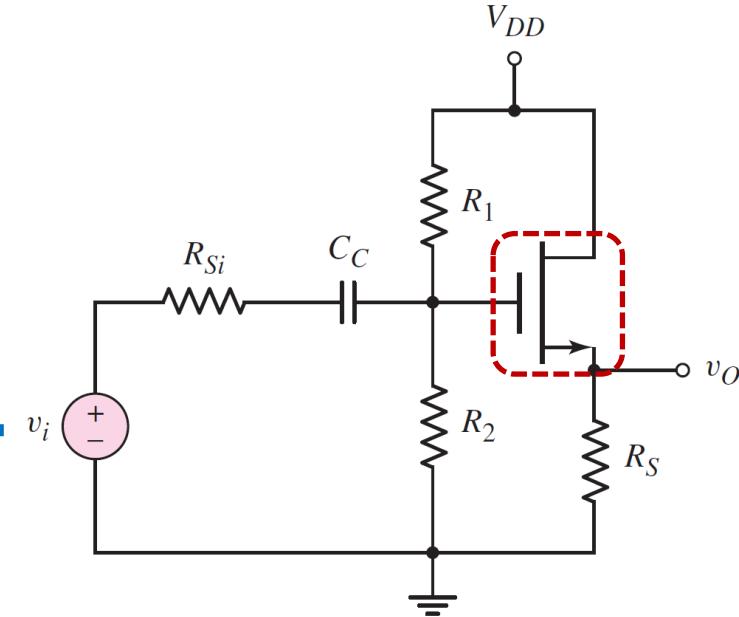
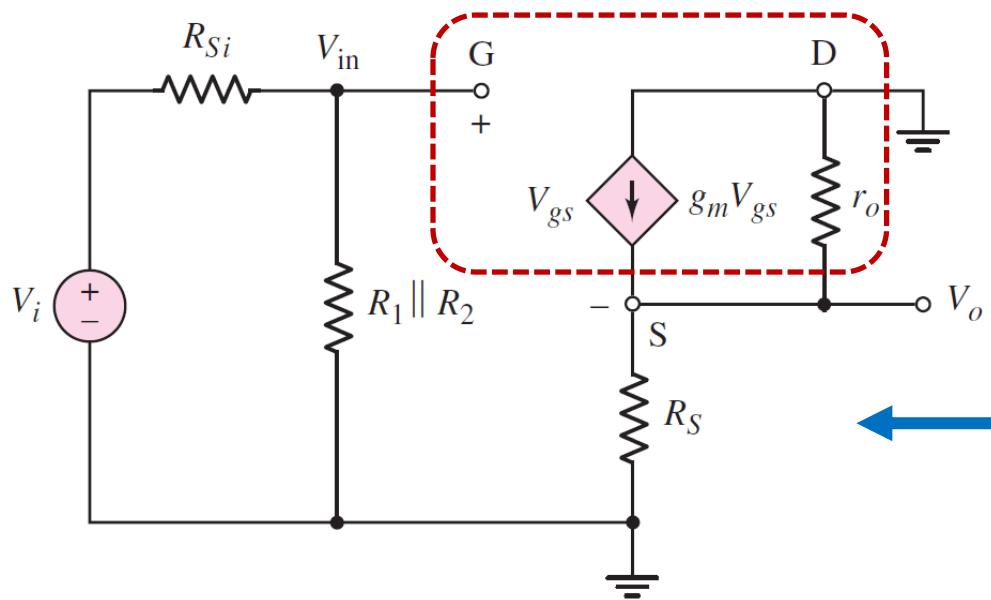
- We will get two solutions  $I_{DQ1}$  and  $I_{DQ2}$ 
  - $I_{DQ1}, V_{GSQ1}, V_{DSQ1}$
  - $I_{DQ2}, V_{GSQ2}, V_{DSQ2}$
- **Verification:**
  - The transistor must be biased in the saturation region
  - Only one solution is valid

$$V_{DSQ} \geq V_{DSQ}(\text{sat}) = V_{GSQ} - V_{TN}$$



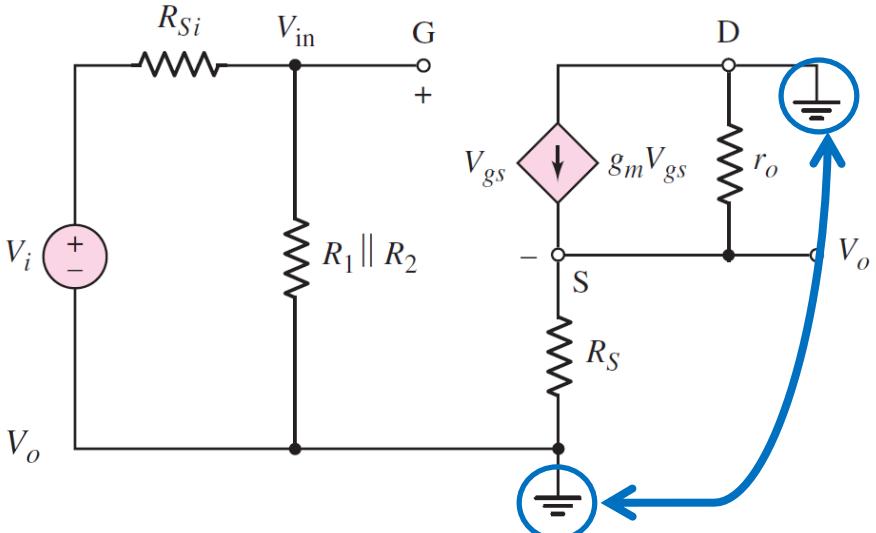
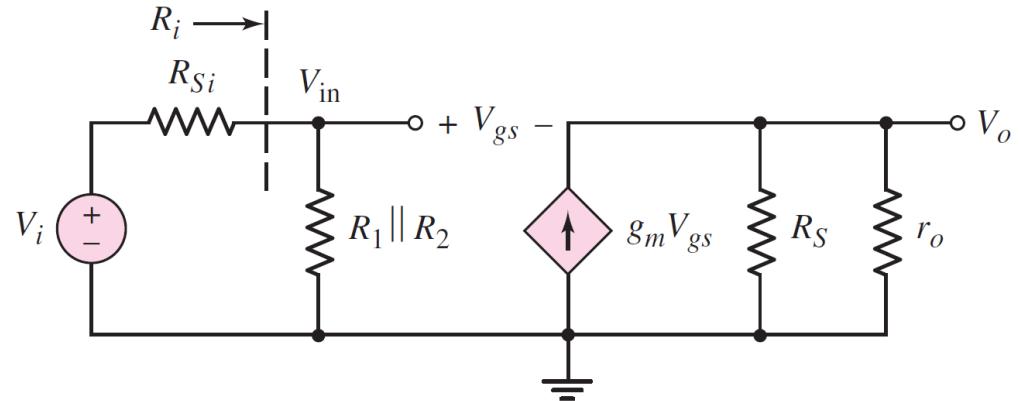
# Step 2: Small-Signal Equivalent Circuit

- Analyze the small-Signal Equivalent Circuit
  - dc source is set to zero, and replace coupling capacitor as short circuit
  - Replace the transistor by its small-signal model



# Step 2: Small-Signal Equivalent Circuit

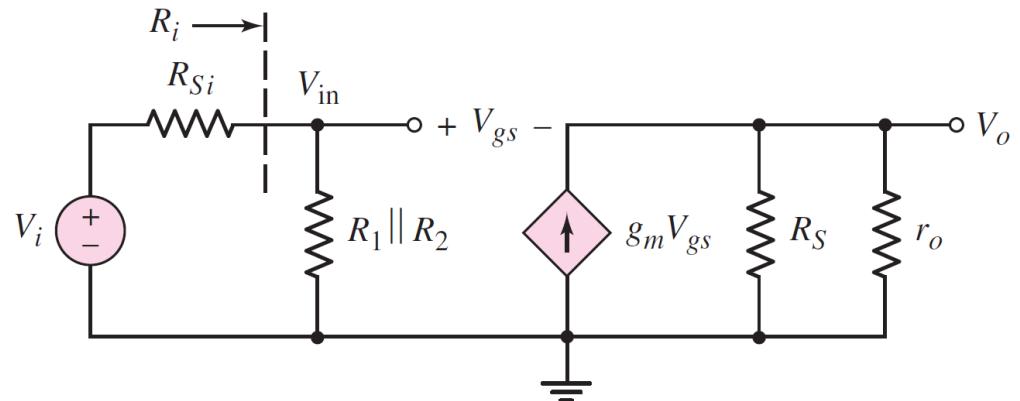
- Connect the drain and the ac signal ground



# Step 2: Small-Signal Voltage Gain

- To find the small-signal voltage gain
  - $V_o \leftrightarrow V_i$
  - $V_o \leftrightarrow V_{gs} \leftrightarrow V_{in} \leftrightarrow V_i$
- Determine the output voltage

$$V_o = g_m V_{gs} (R_S \parallel r_o)$$



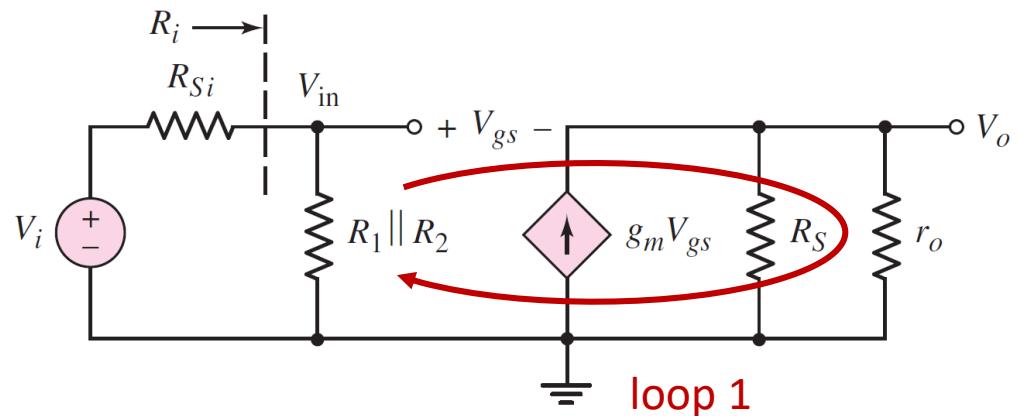
# Step 2: Small-Signal Voltage Gain

- To find the small-signal voltage gain

- $V_o \leftrightarrow V_i$        $V_o \leftrightarrow V_{gs} \leftrightarrow V_{in} \leftrightarrow V_i$

- A KVL equation in loop 1

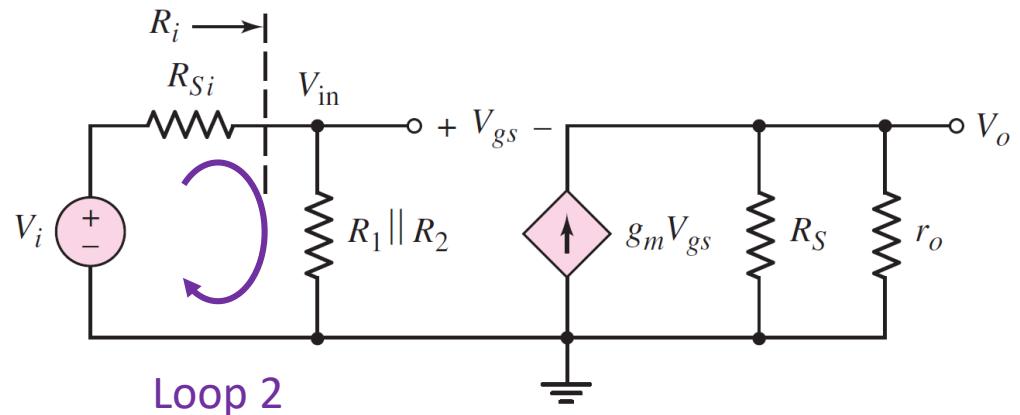
$$-V_{in} + V_{gs} + V_o = 0 \quad V_{in} = V_{gs} + g_m V_{gs} (R_S \parallel r_o)$$



# Step 2: Small-Signal Voltage Gain

- To find the small-signal voltage gain
  - $V_o \leftrightarrow V_i$        $V_o \leftrightarrow V_{gs} \leftrightarrow V_{in} \leftrightarrow V_i$
- A voltage divider equation in loop 2

$$V_{in} = \frac{R_i}{R_i + R_{Si}} V_i$$



# Step 2: Small-Signal Voltage Gain

- To find the small-signal voltage gain

- $V_o \leftrightarrow V_{gs} \leftrightarrow V_{in} \leftrightarrow V_i$

$$V_o = g_m V_{gs} (R_S \parallel r_o)$$

$$V_{in} = V_{gs} + g_m V_{gs} (R_S \parallel r_o)$$

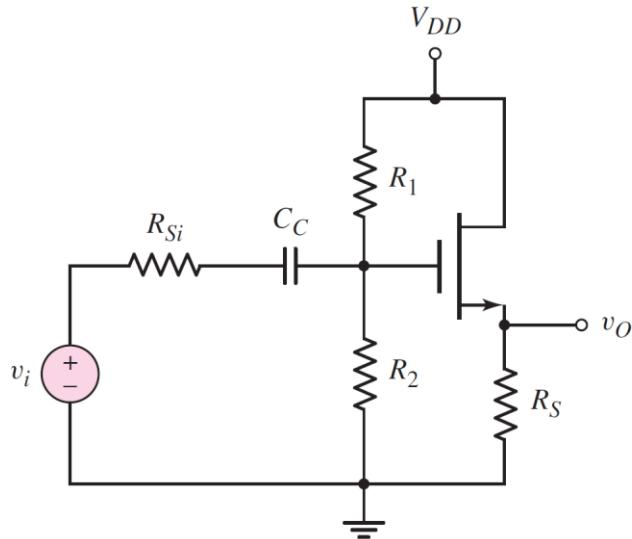
$$V_{in} = \frac{R_i}{R_i + R_{Si}} V_i$$

- The small-signal voltage gain is

$$A_v = \frac{V_o}{V_i} = \frac{g_m (R_S \parallel r_o)}{1 + g_m (R_S \parallel r_o)} \left( \frac{R_i}{R_{Si} + R_i} \right) < 1$$

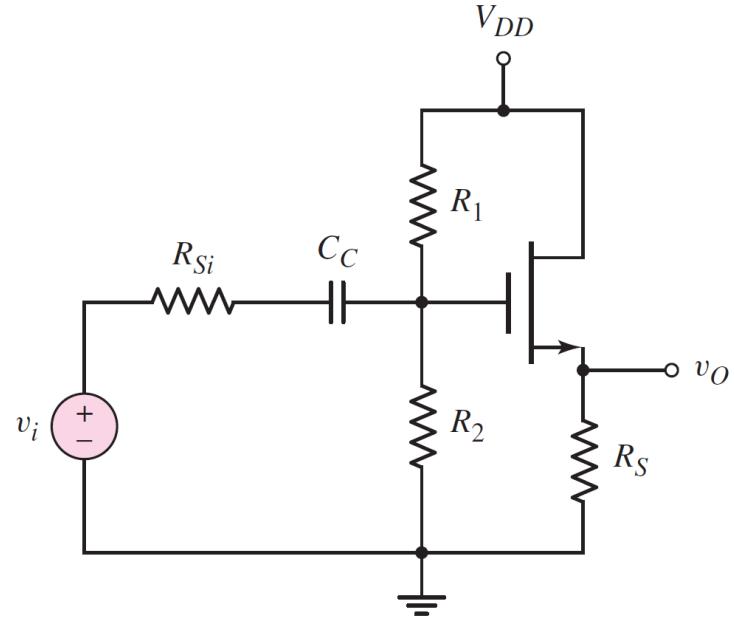
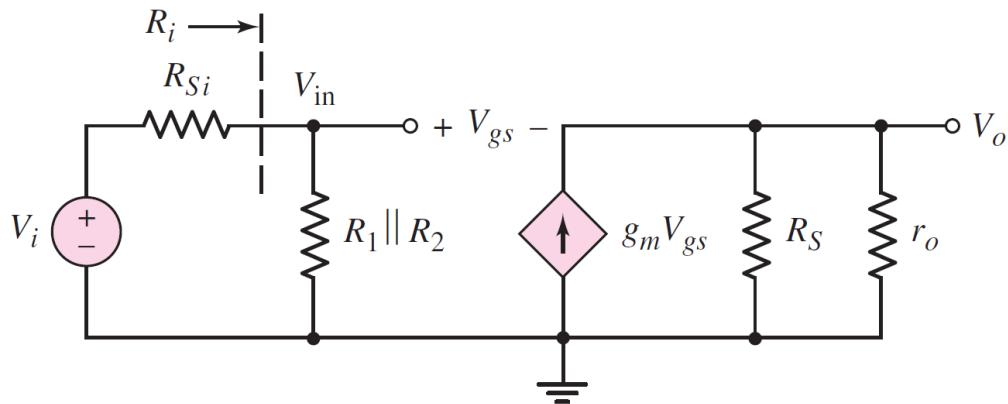
# Example 5.5

Calculate the small-signal voltage gain of the source-follower circuit. Assume the circuit parameters are  $V_{DD} = 12$  V,  $R_1 = 162$  k $\Omega$ ,  $R_2 = 463$  k $\Omega$ , and  $R_S = 0.75$  k $\Omega$ , and the transistor parameters are  $V_{TN} = 1.5$  V,  $K_n = 4$  mA/V $^2$ , and  $\lambda = 0.01$  V $^{-1}$ . Also assume  $R_{Si} = 4$  k $\Omega$ .



# Input and Output Resistance

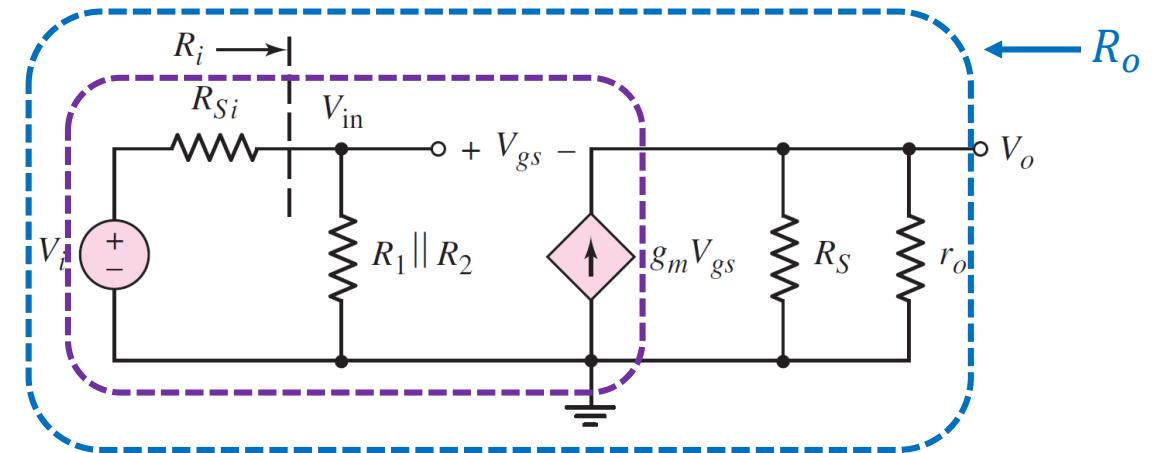
- Input resistance: equivalent resistance looking into the gate
  - $R_i = R_1 \parallel R_2$



# Output Resistance

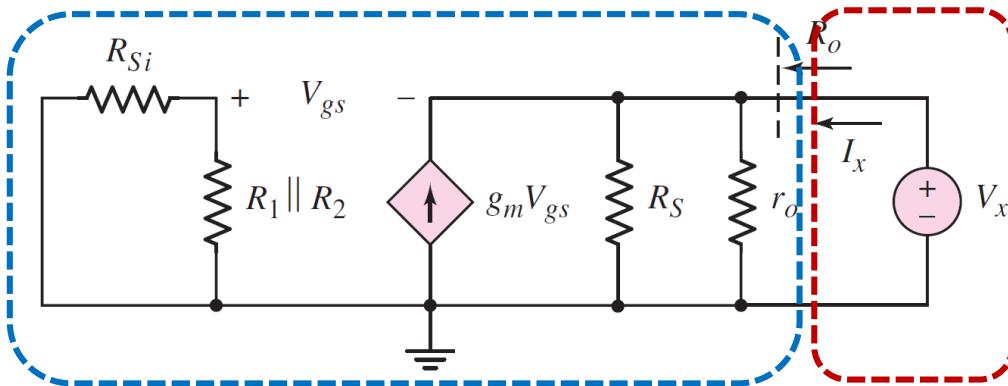
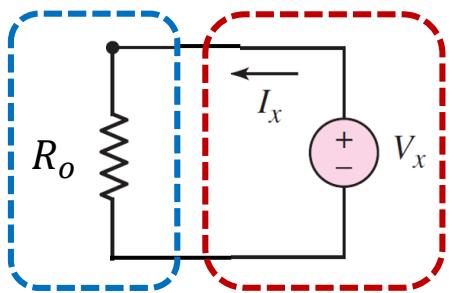
- Set all **independent sources** to zero

- $R_o = r_o \parallel R_S \parallel (?)$
- What is the **resistance** of the dependent current source?



# Output Resistance

- Apply a **test voltage**  $V_x$  to the output terminals, the current is  $I_x$
- The output resistance is  $R_o = \frac{V_x}{I_x}$



# Output Resistance

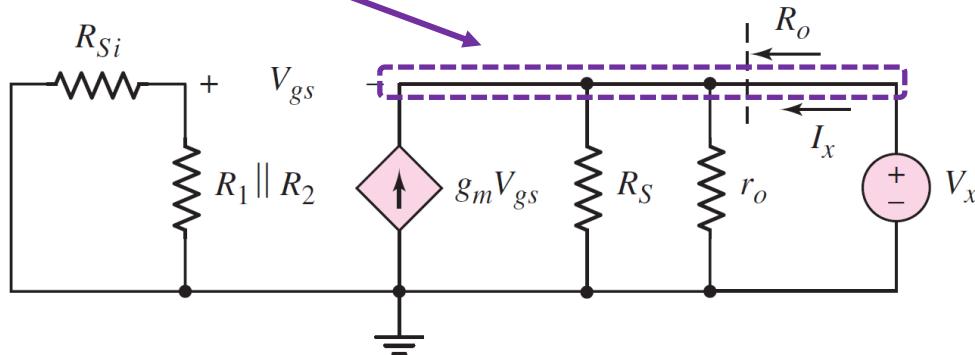
- Writing a KCL equation at the output source terminal

$$g_m V_{gs} + I_x - \frac{V_x}{R_S} - \frac{V_x}{r_o} = 0$$

$$V_{gs} = -V_x$$

$$I_x = g_m V_x + \frac{V_x}{R_S} + \frac{V_x}{r_o}$$

$$\frac{I_x}{V_x} = g_m + \frac{1}{R_S} + \frac{1}{r_o} = \frac{1}{R_o}$$



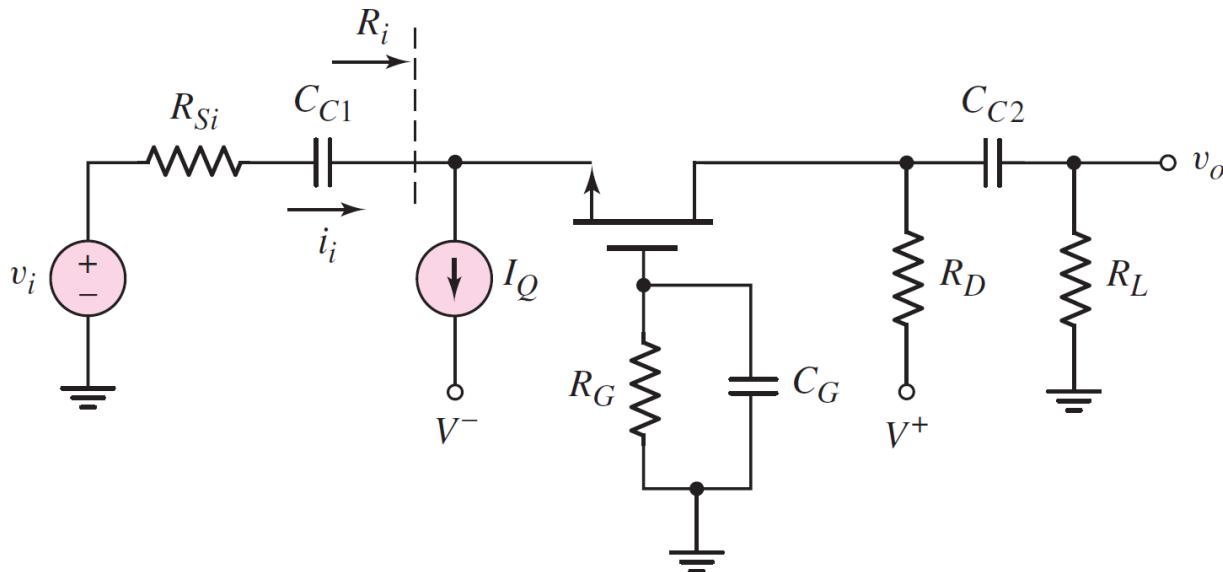
- The output resistance is  $R_o = \frac{V_x}{I_x} = \frac{1}{g_m} \parallel R_S \parallel r_o$

# The Common-Gate Configuration

Analyze the common-gate amplifier and become familiar with the general characteristics of this circuit.

# Common-Gate Amplifier Circuit

- The input signal is applied to the **source** terminal
- $C_G$  ensures the **gate** is at signal ground



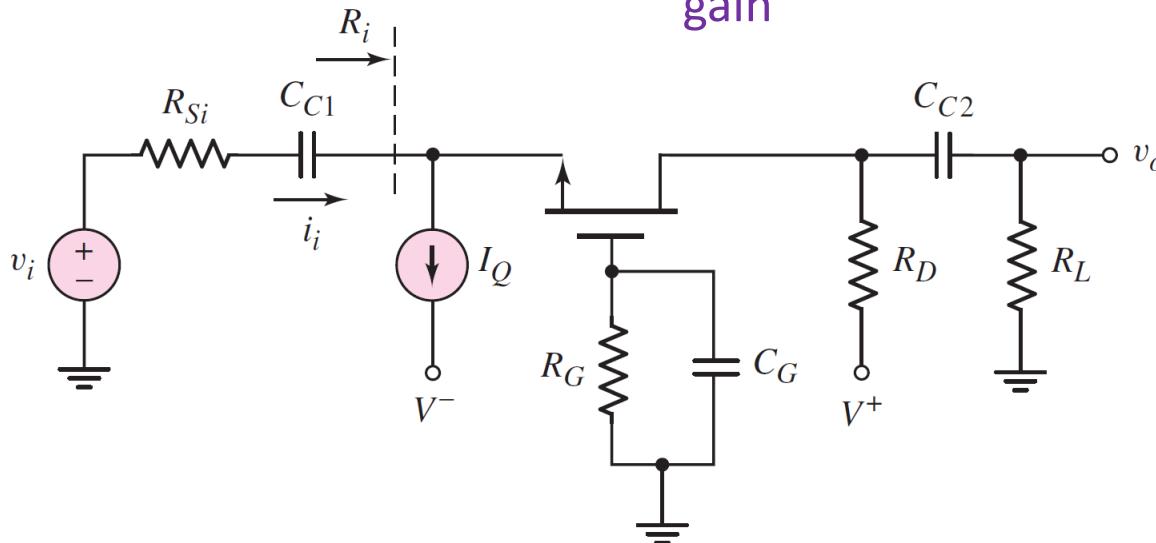
# Common-Gate Amplifier Circuit

- Step 1: dc analysis

- Find the Q-point
- Make sure the transistor is biased in the **saturation region**

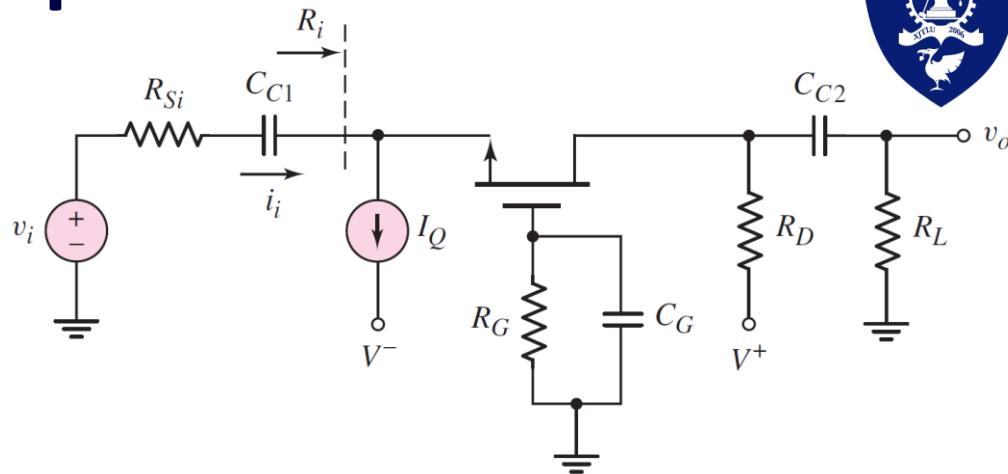
- Step 2: ac analysis

- Draw the **small-signal equivalent circuit**
- Determine the **small-signal voltage gain**



# Step 2: Small-Signal Equivalent Circuit

- Draw the **small-signal equivalent circuit**
- Set **dc sources** to zero
  - $V^+ = V^- = 0$
  - $I_Q = 0$
- Set capacitors as **short circuits**
- Replace the FET by a **small-signal model**
  - assume  $r_o = \infty$



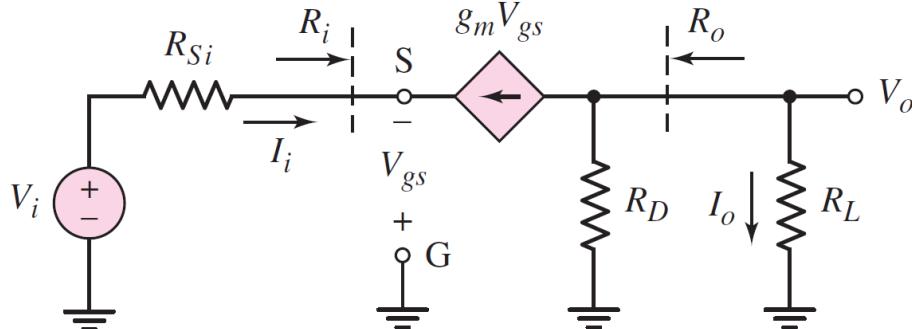
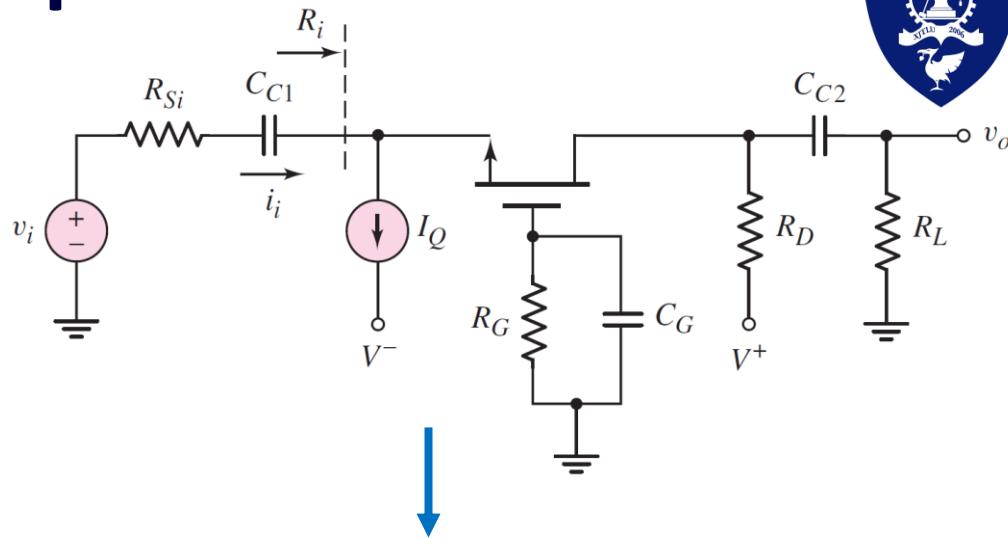
# Step 2: Small-Signal Equivalent Circuit

- To find the **small-signal voltage gain**, we need to find the relationship between
  - $V_{gs}$  is the bridge between input and output signals

$$V_o \leftrightarrow V_{gs} \leftrightarrow V_i$$

- The output voltage is

$$V_o = -g_m V_{gs} (R_D \parallel R_L)$$



# Step 2: Small-Signal Voltage Gain

- A **KVL** equation in loop 1
- The **small-signal voltage gain** is

$$-V_i + I_i R_{Si} - V_{gs} = 0$$

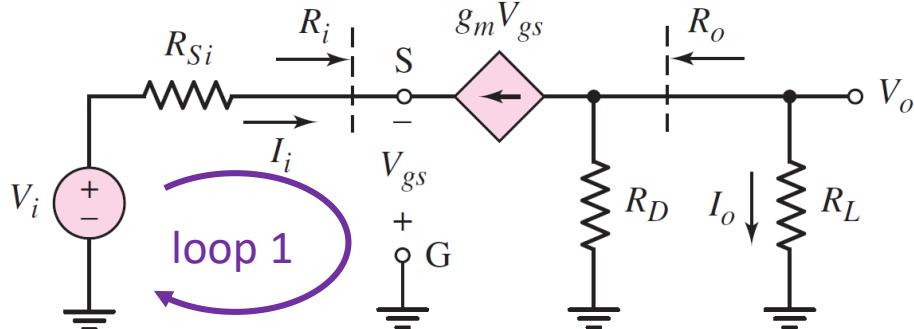
- The input current is in the **opposite direction** with the independent current source

$$I_i = -g_m V_{gs}$$

$$V_{gs} = \frac{-V_i}{g_m R_{Si} + 1}$$

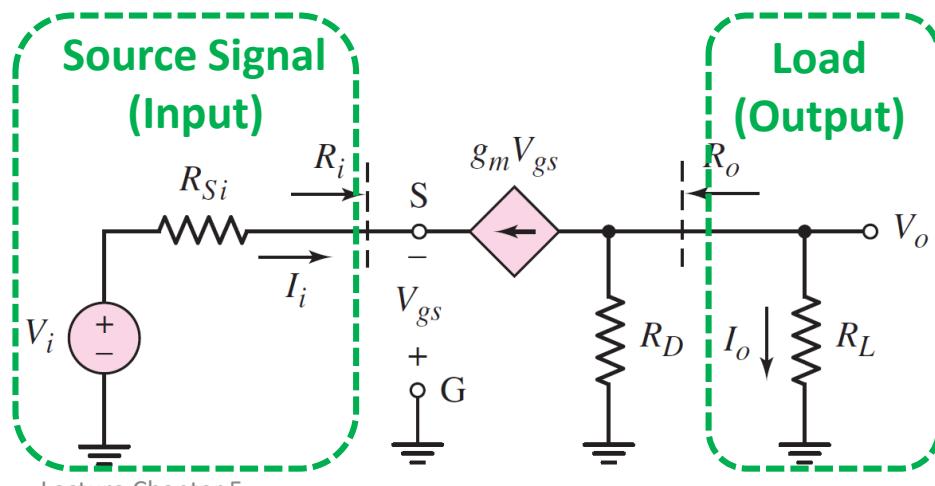
$$A_v = \frac{V_o}{V_i} = + \frac{g_m (R_D \parallel R_L)}{g_m R_{Si} + 1}$$

- The output and input signals are **in phase**



# Input and Output Resistance

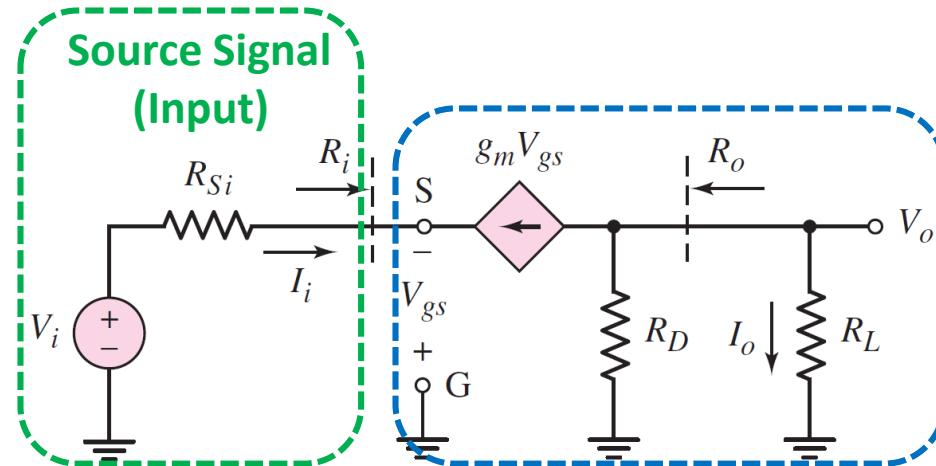
- The input resistance is the equivalent resistance looking into the source
- The output resistance is the equivalent resistance looking in the drain



# Input Resistance

- The voltage at the source terminal is  $-V_{gs}$
- The input current  $I_i = -g_m V_{gs}$
- The input resistance is

$$R_i = \frac{-V_{gs}}{I_i} = \frac{-V_{gs}}{-g_m V_{gs}} = \frac{1}{g_m}$$



# Output Resistance

- To find the output resistance, we need to **set independent source to zero** →  $V_i = 0$  (short circuit)
- Write a KVL equation in **loop 1**

$$I_i R_{Si} - V_{gs} = 0$$

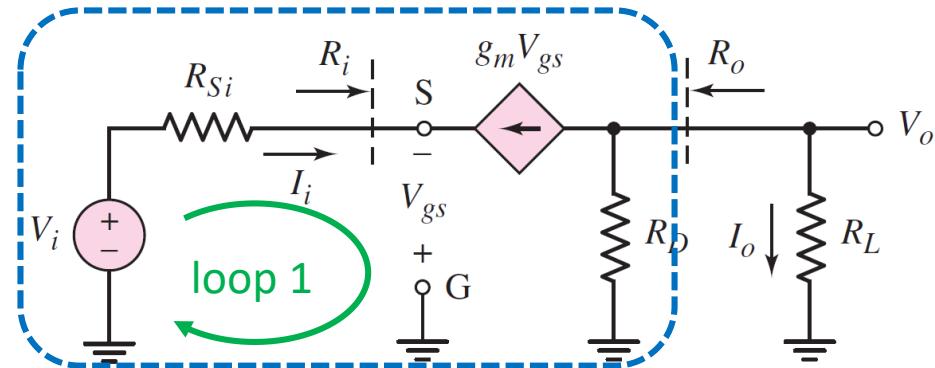
$$I_i = -g_m V_{gs}$$

$$-g_m V_{gs} R_{Si} - V_{gs} = 0$$

$$V_{gs}(1 + g_m R_{Si}) = 0 \rightarrow V_{gs} = 0$$

- The output resistance is

$$R_o = R_D$$



# Small-Signal Current Gain

- To find the small-signal current gain

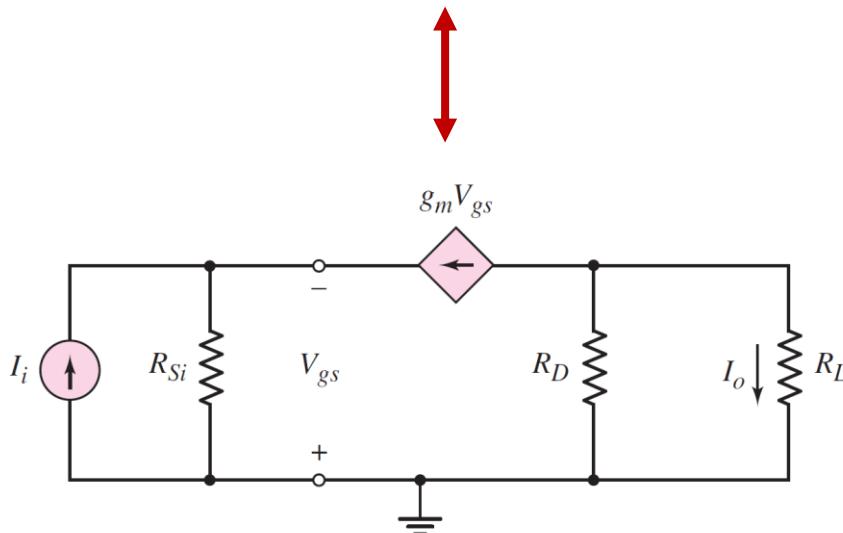
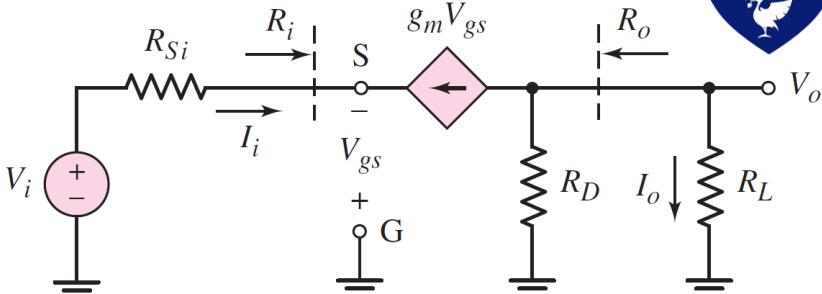
- $$A_i = \frac{\text{Output Current}}{\text{Input Current}} = \frac{I_o}{I_i}$$

- Norton equivalent circuit

A voltage source in series with a resistor



A current source in parallel with a resistor



# Small-Signal Current Gain

- To find the small-signal current gain

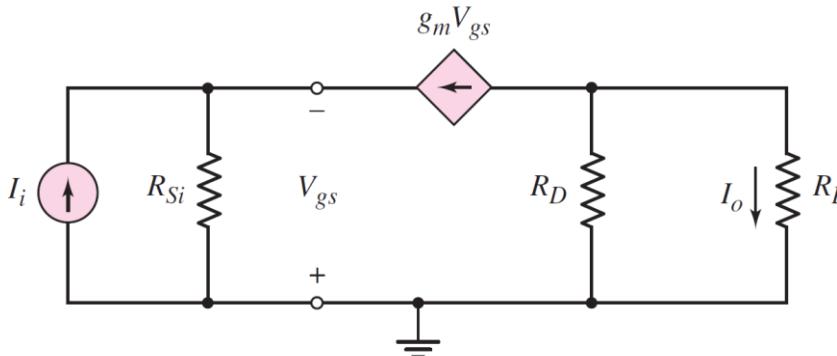
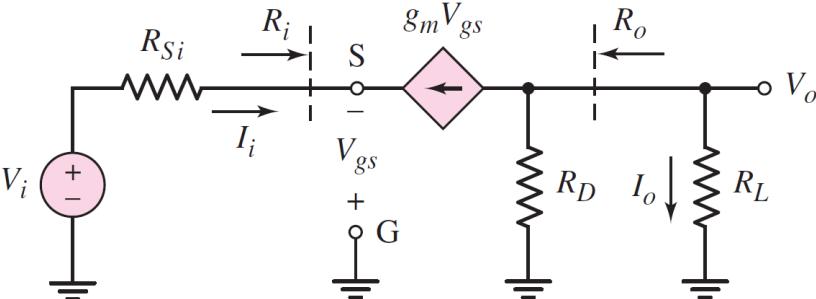
- $I_o \leftrightarrow V_{gs} \leftrightarrow I_i$

- Based on the current divider equation, the output current is

$$I_o = \left( \frac{R_D}{R_D + R_L} \right) (-g_m V_{gs})$$

- The input current is

$$I_i + \frac{V_{gs}}{R_{Si}} + g_m V_{gs} = 0$$



Norton equivalent signal source

# Small-Signal Current Gain

- The small-signal current gain is

$$A_i = \frac{I_o}{I_i} = \frac{\left(\frac{R_D}{R_D+R_L}\right)(-g_m V_{gs})}{-V_{gs}\left(\frac{1}{R_{Si}} + g_m\right)} = \left(\frac{R_D}{R_D+R_L}\right) \left(\frac{g_m R_{Si}}{1 + g_m R_{Si}}\right) \cong 1$$

- The current gain is essentially unity
  - $R_D \gg R_L, g_m R_{Si} \gg 1$

# The Three Basic Amplifier Configurations: Summary and Comparison

Compare the general characteristics of the three basic amplifier configurations.

# Comparison of Three Basic Amplifiers

Configuration	Voltage gain	Current gain	Input resistance	Output resistance
Common source	$A_v > 1$	—	$R_{TH}$ (biased resistor)	Moderate to high ( $R_D$ )
Common drain (source follower)	$A_v \cong 1$ (slightly less than 1)	—	$R_{TH}$ (biased resistor)	Low (a few hundred ohms)
Common gate	$A_v \geq 1$	$A_i \cong 1$	Low (a few hundred ohms) $\frac{1}{g_m}$	Moderate to high ( $R_D$ )

# Summary

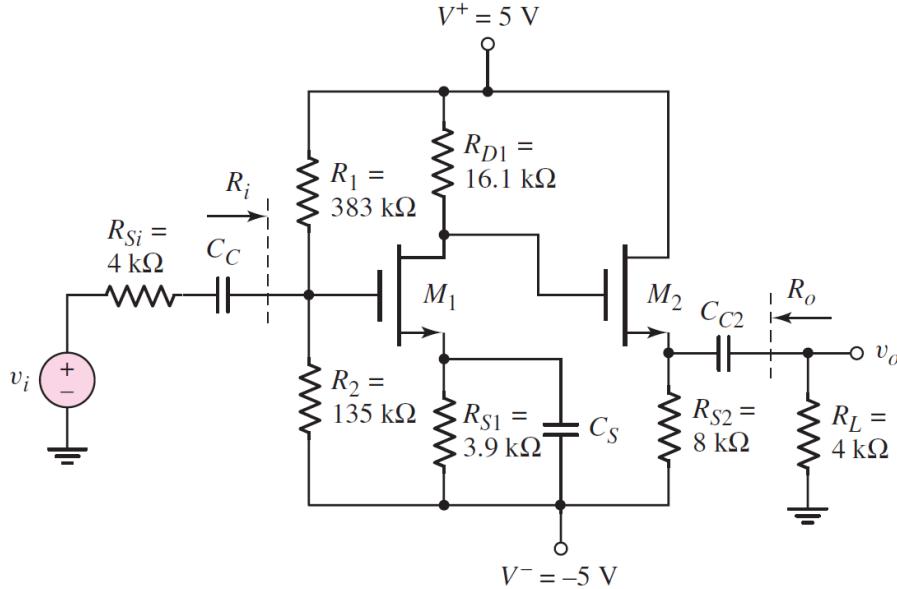
- Explain the **amplification process** in a simple MOSFET amplifier circuit
  - The MOSFET must be biased in the saturation region → dc analysis
  - Describe the small-signal equivalent circuit of the MOSFET → ac analysis
- Analyze three MOSFET amplifier circuits
  - Common-drain amplifier
  - Common-source amplifier
  - Common-gate amplifier
- Characterize the small-signal voltage gain and **input/output resistance** of three amplifiers
- Optional: Apply the MOSFET small-signal equivalent circuit in the analysis of multistage amplifier circuits

# Multistage Amplifiers (Optional)

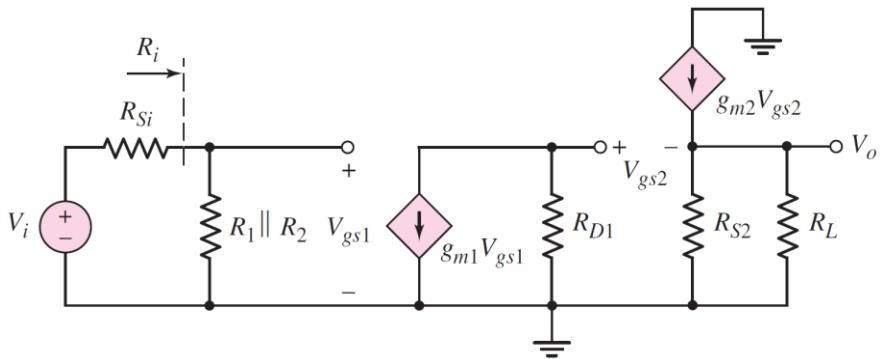
Analyze multitransistor or multistage amplifiers and understand the advantages of these circuits over single-transistor amplifiers.

# Multistage Amplifier: Cascade Circuit

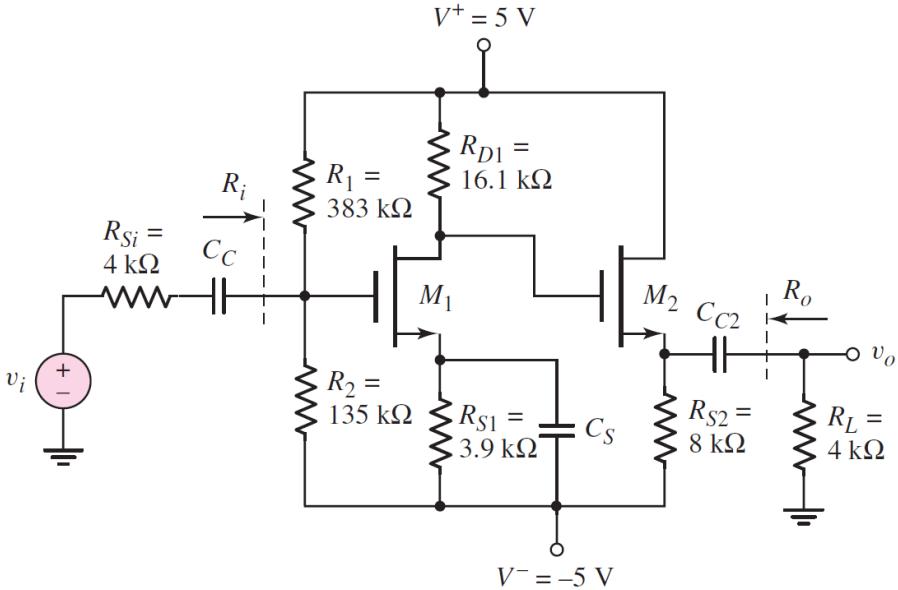
- A **cascade** of a common-source amplifier followed by a Common drain (source-follower) amplifier
- Common-source amplifier
  - High** voltage gain
- Common-drain
  - Low** output impedance



# Small-Signal Equivalent Circuit

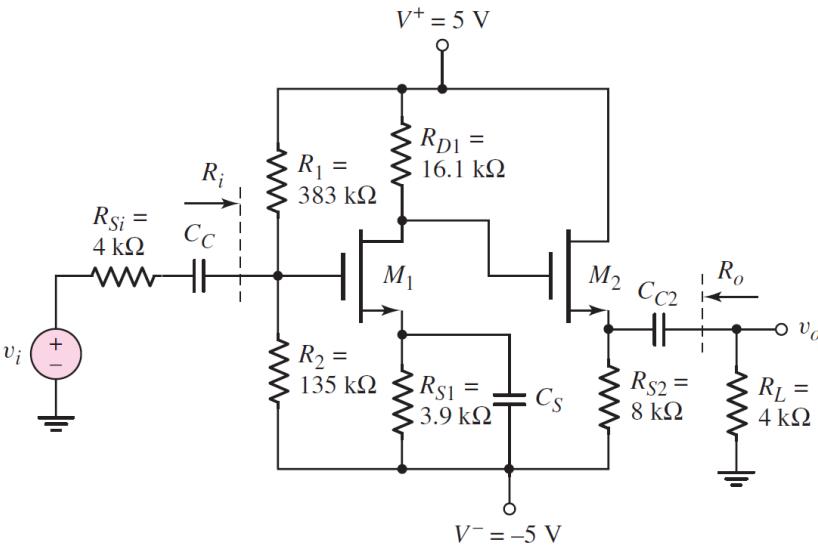


Small-signal equivalent circuit  
of NMOS cascade circuit



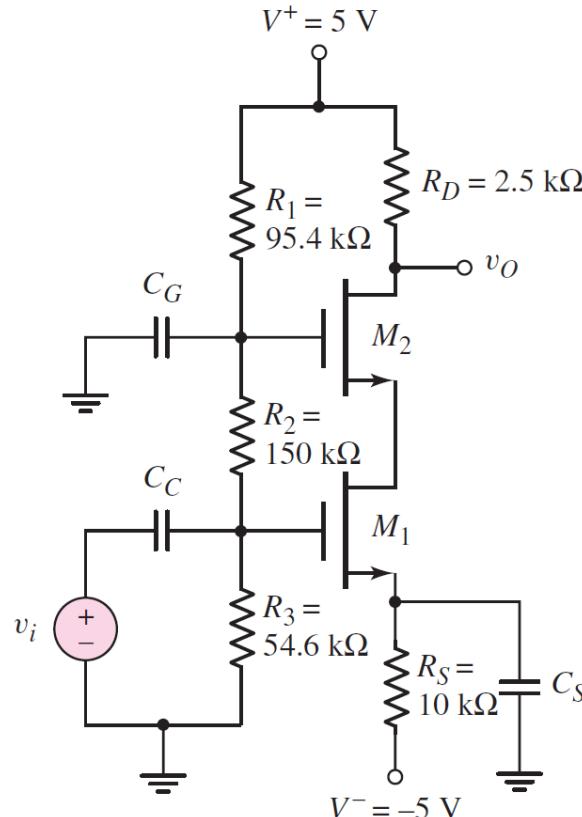
# Example 5.6

Determine the small-signal voltage gain of a multistage cascade circuit. The transistor parameters are  $V_{TN1} = V_{TN2} = 1.2$  V,  $K_{n1} = 0.5 \text{ mA/V}^2$ ,  $K_{n2} = 0.2 \text{ mA/V}^2$  and  $\lambda_1 = \lambda_2 = 0$ . The quiescent drain currents are  $I_{D1} = 0.2 \text{ mA}$  and  $I_{D2} = 0.5 \text{ mA}$

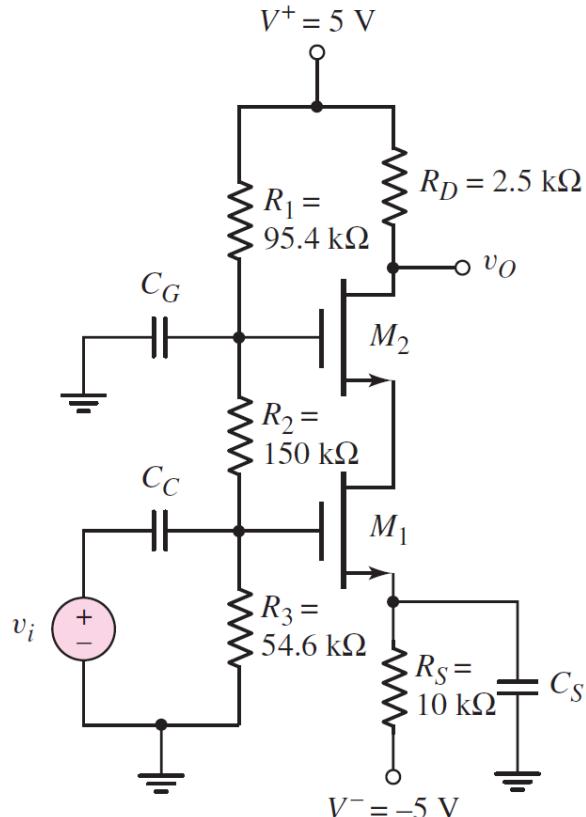
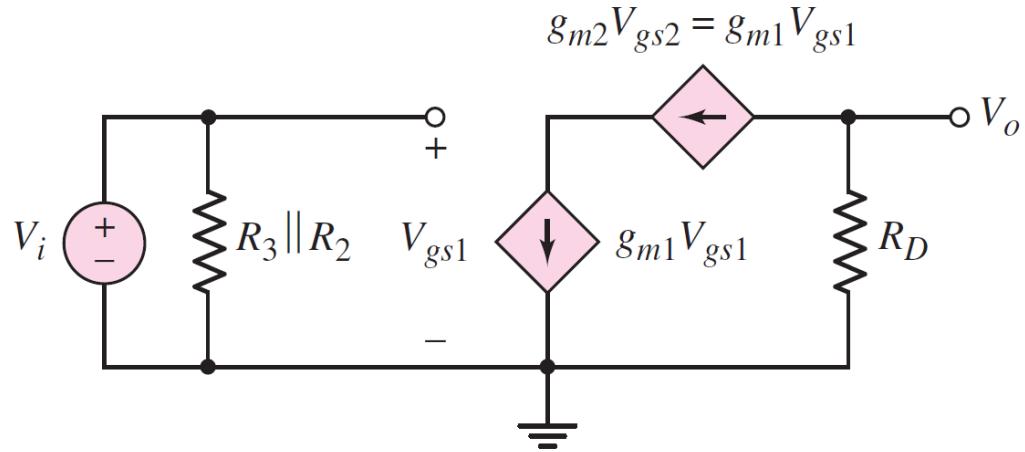


# Multistage Amplifier: Cascode Circuit

- A **cascode** circuit with n-channel MOSFETs
  - $M_1$ : common-source configuration
    - $C_S$  is short circuit in ac analysis
  - $M_2$ : common-gate configuration
    - $C_G$  is short circuit in ac analysis

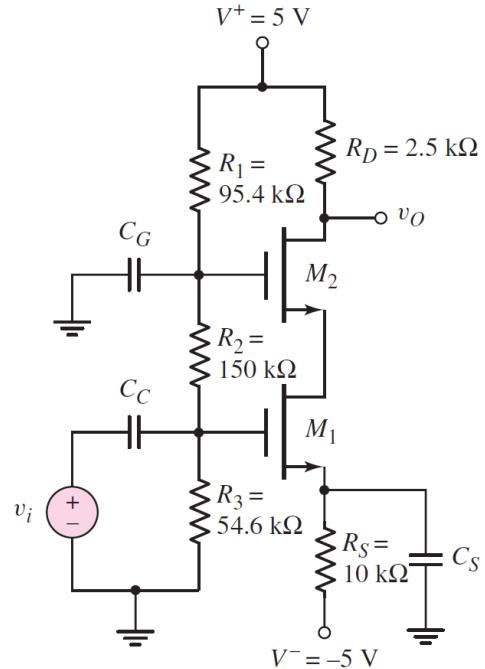


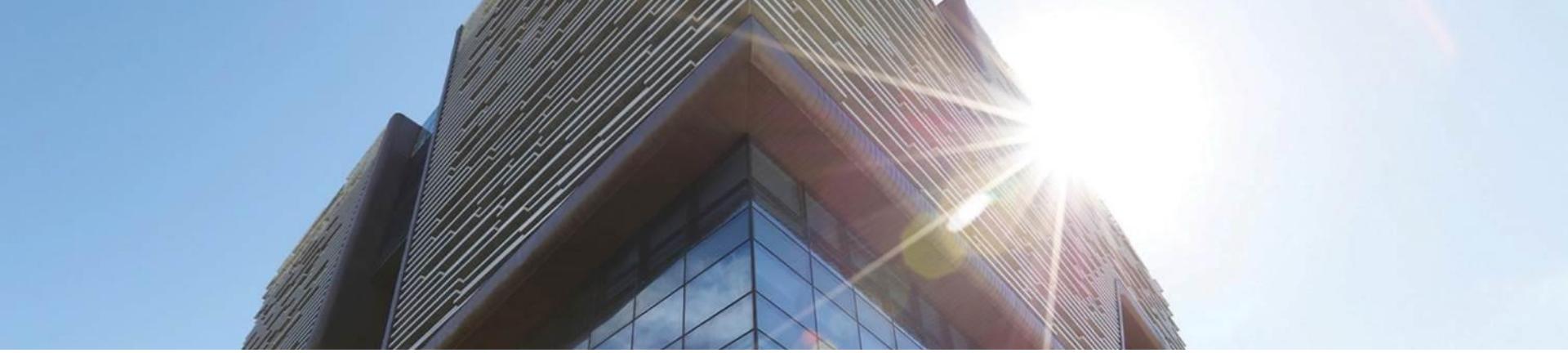
# Small-Signal Equivalent Circuit



# Example 5.7

Determine the small-signal voltage gain of a cascode circuit. The transistor parameters are  $V_{TN1} = V_{TN2} = 1.2$  V,  $K_{n1} = K_{n2} = 0.8$  mA/V<sup>2</sup> and  $\lambda_1 = \lambda_2 = 0$ . The quiescent drain currents are  $I_D = 0.4$  mA in each transistor.





# Thank You

