**Lecture 9b**

*of*

**EEE201**

# CMOS Digital Integrated Circuits

**Department of Electrical & Electronic Engineering**

Xi'an Jiaotong-Liverpool University (XJTLU)

Monday, 04th November 2024

- **CMOS IC Layout Design** continued
  - extend from CMOS inverter foundation
  - NAND & NOR logic gates
  - complicated logic gates

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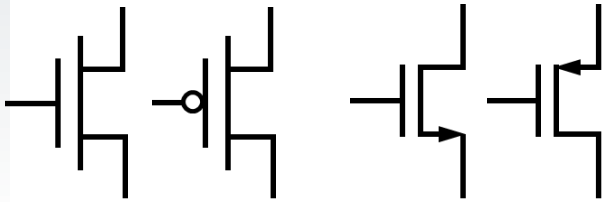
# CMOS Inverter as Foundation

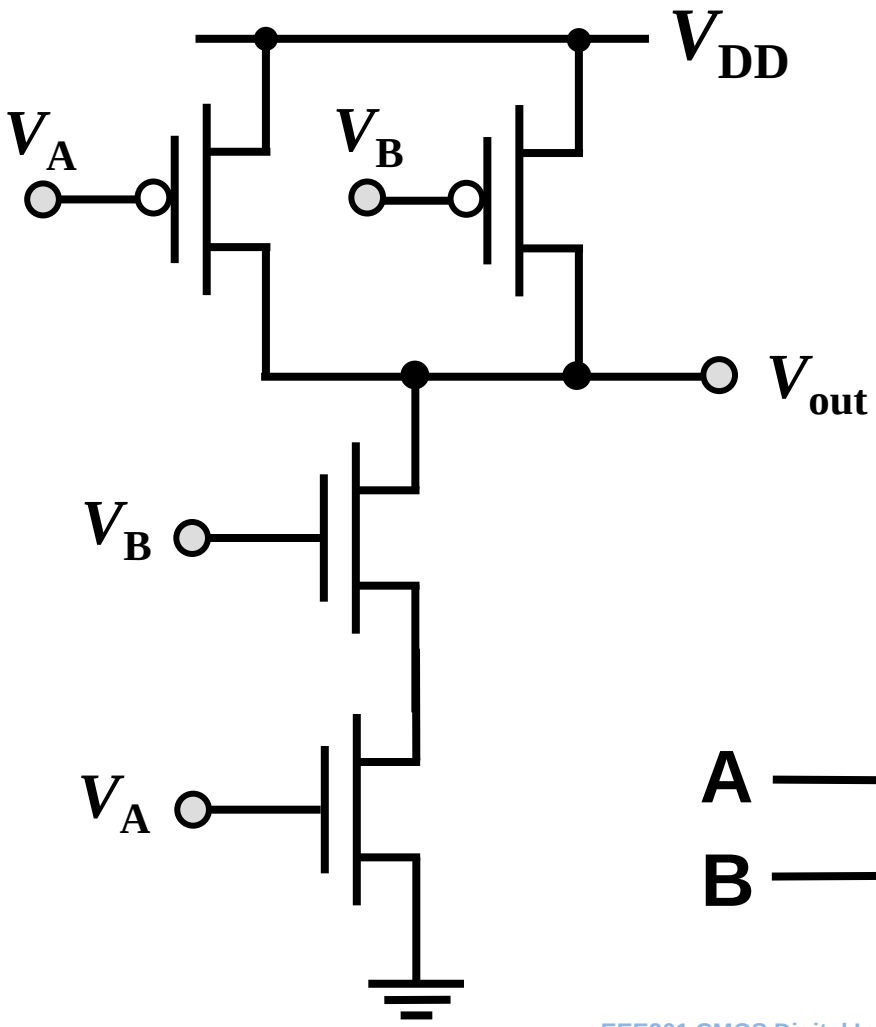
(principles extending to NAND, NOR & other logic gates)

- With the foundation of CMOS inverter's operation and design, the principles can be extended to the NAND gate, the NOR gate and complicated logic gates.
  - logic "0" represented by a low voltage, typically 0 V
  - logic "1" represented by a high voltage, typically $V_{DD}$
  - nMOSFETs & pMOSFETs in ***complementary*** circuit operation
  - assumed proper connection of the body terminals of the MOSFETs if not shown in the circuit symbols:



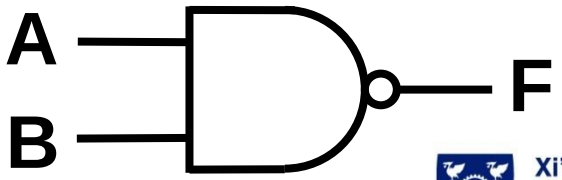
# NAND Logic - CMOS implementation

## (2 nMOSFETs in series & 2 pMOSFETs in parallel)




| $V_A$ | $V_B$ | $V_{out}$ |
|---|---|---|
| 0 V | 0 V | $V_{DD}$ |
| 0 V | $V_{DD}$ | $V_{DD}$ |
| $V_{DD}$ | 0 V | $V_{DD}$ |
| $V_{DD}$ | $V_{DD}$ | 0 V |

$$F = \overline{A \cdot B}$$




| A | B | F |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

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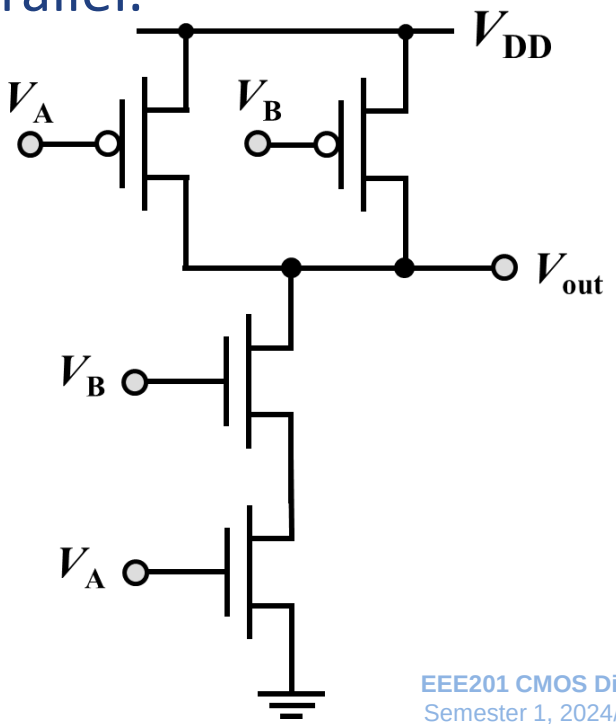
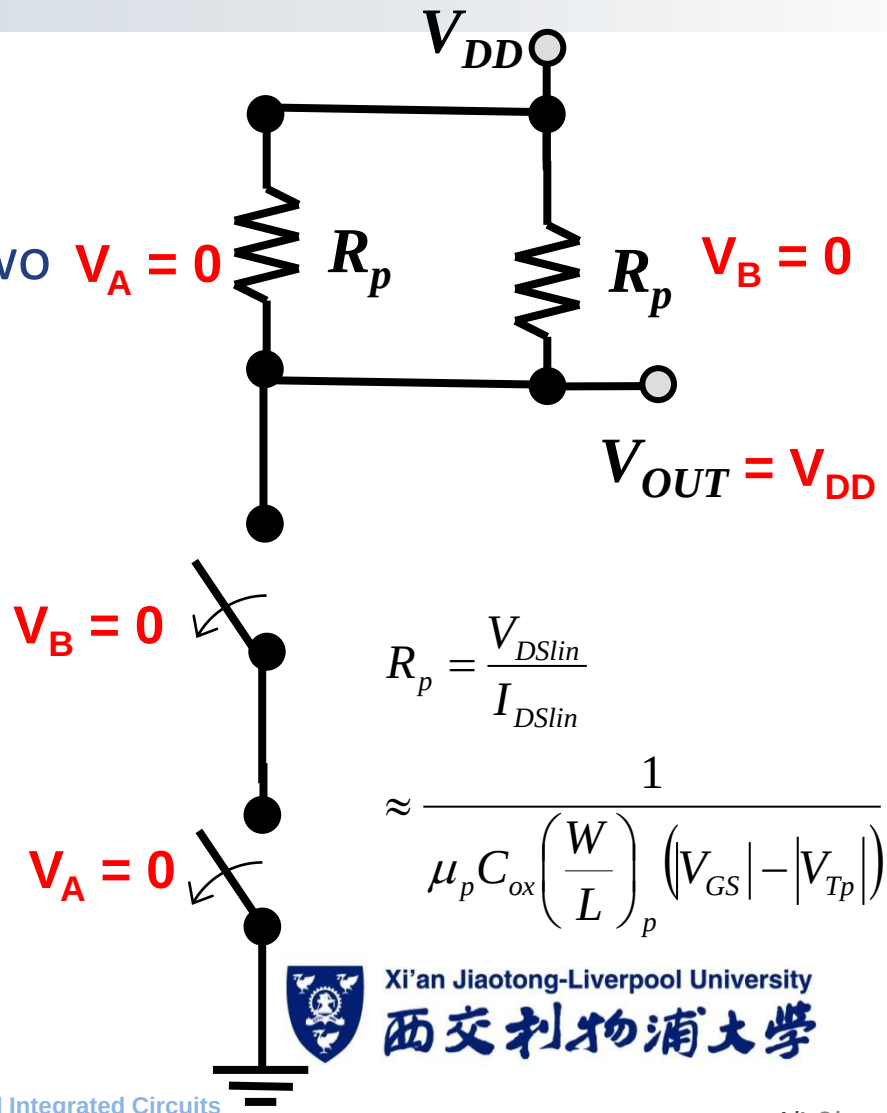
# CMOS NAND Logic Gate

(switch model of the MOSFETs – both logic "0" at inputs)

- When both inputs are logic "0" (i.e. $V_A = V_B = 0$ V), $V_{out}$ is connected to $V_{DD}$ through two equivalent resistances $R_p$ in parallel.




$$R_p = \frac{V_{DSlin}}{I_{DSlin}} \approx \frac{1}{\mu_p C_{ox}\left(\frac{W}{L}\right)_p \left(|V_{GS}| - |V_{Tp}|\right)}$$

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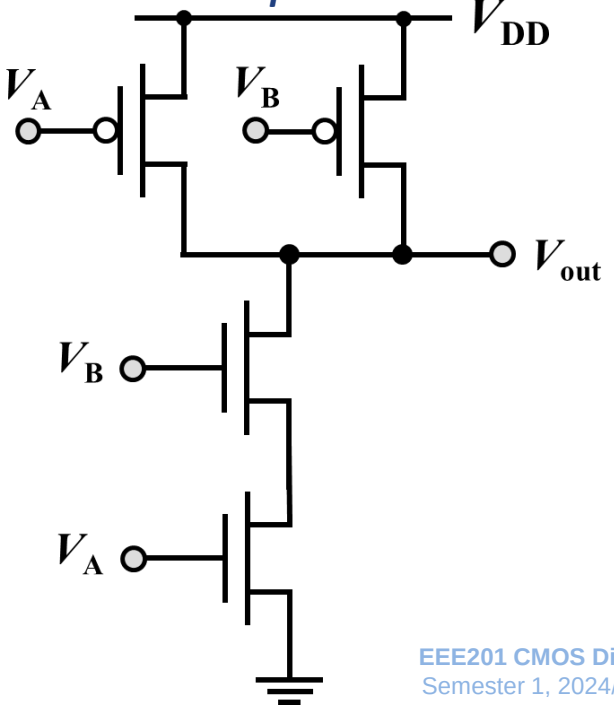
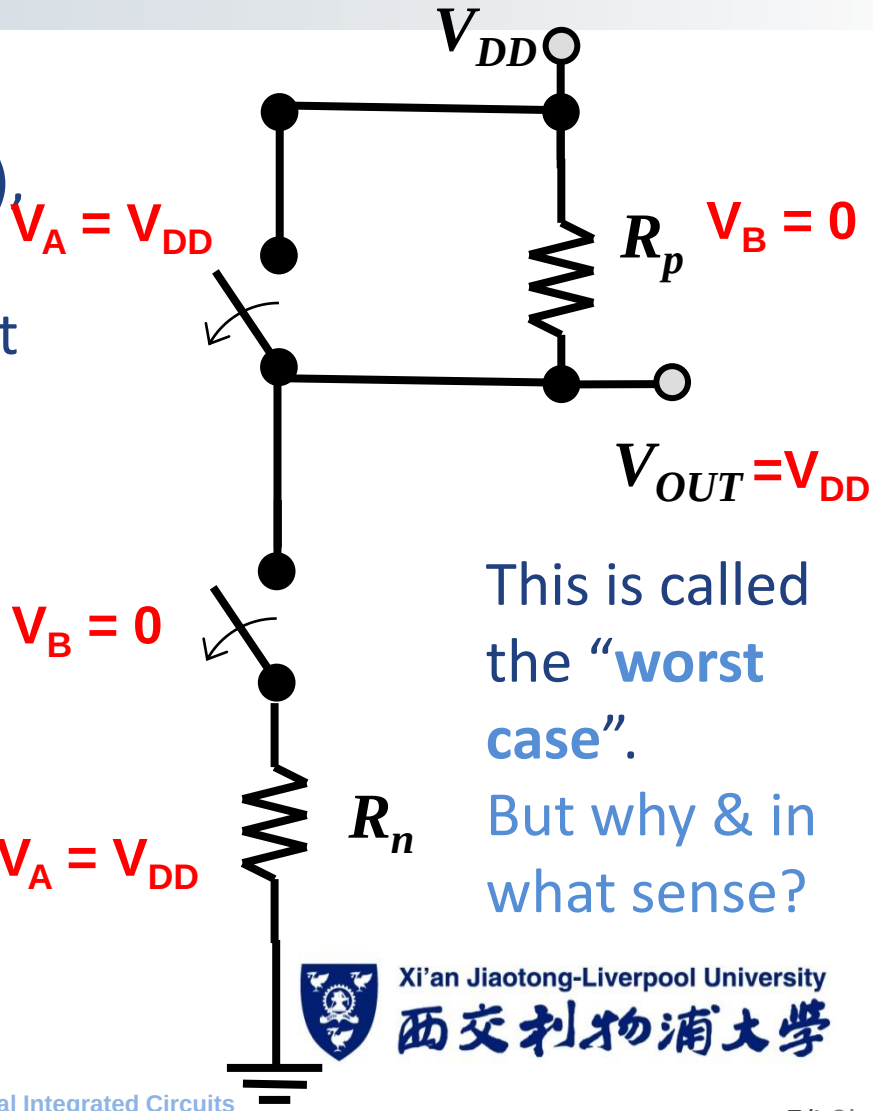
# CMOS NAND Logic Gate

(different inputs)

- When the two inputs are different (e.g. $V_A = V_{DD}$ & $V_B = 0$ V), $V_{out}$ is connected to $V_{DD}$ through only one equivalent resistances $R_p$.




This is called the "**worst case**". But why & in what sense?

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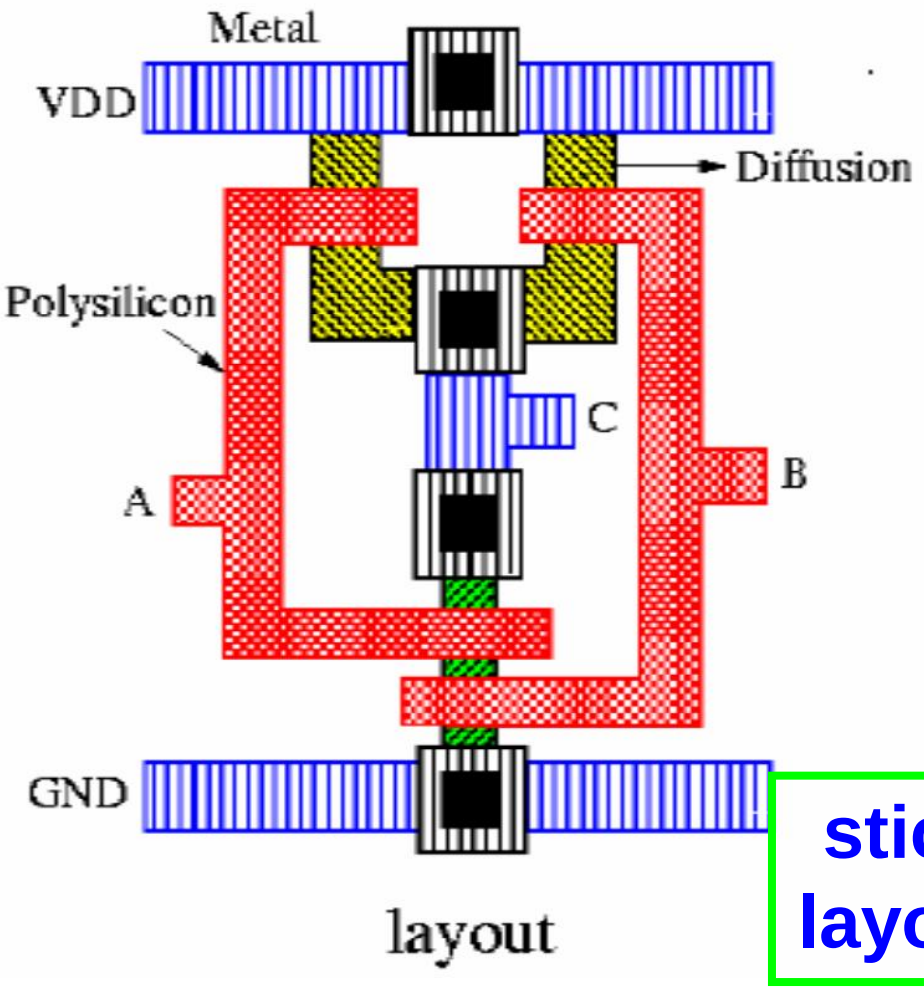
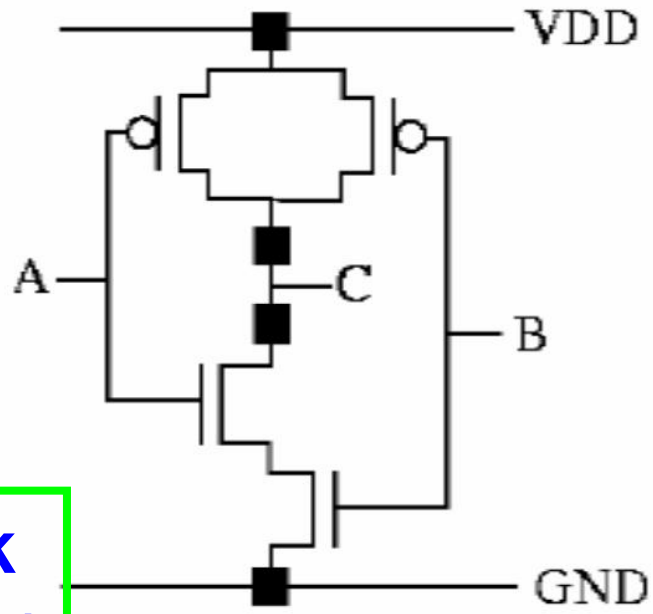
# CMOS NAND Logic Gate

(rough design with stick layout)




in1 in2 out

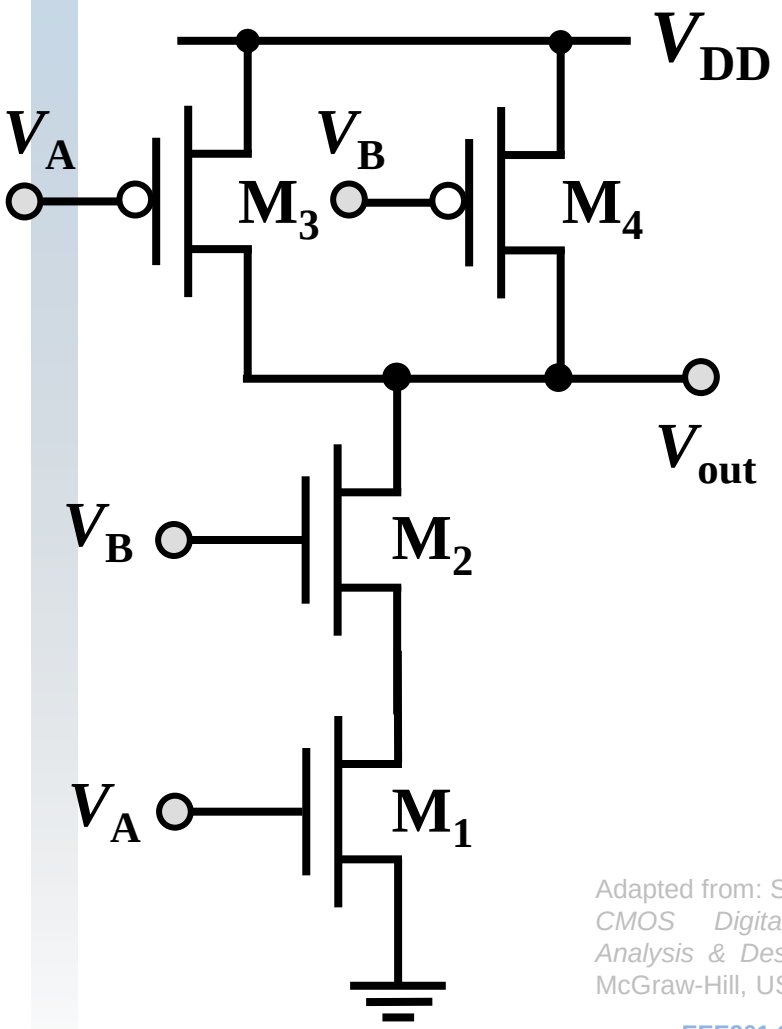
| A | B | C |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

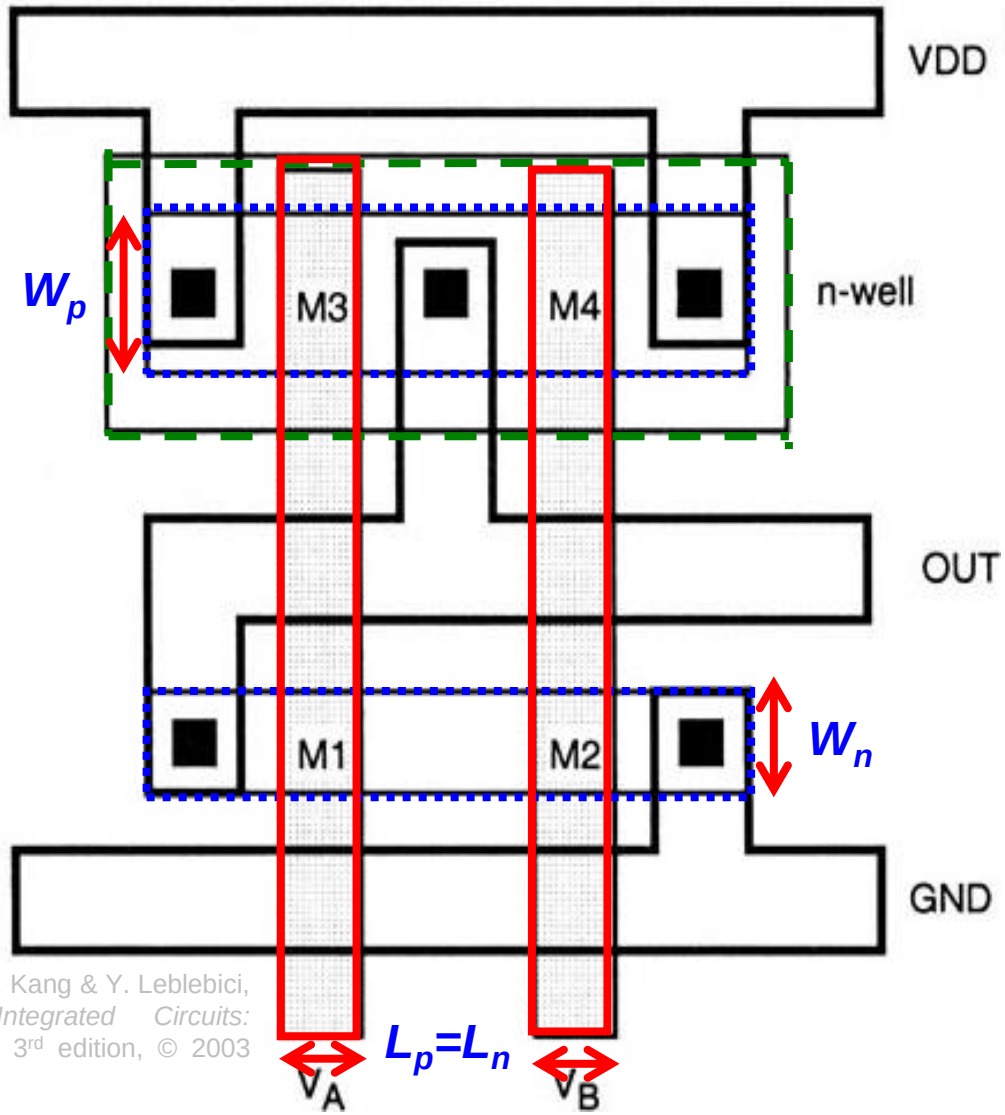



**stick layout**

# CMOS NAND Logic Gate

(proper IC layout improved from stick layout)




Adapted from: S.-M. Kang & Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis & Design*, 3rd edition, © 2003 McGraw-Hill, USA.

# CMOS **NAND** Logic Gate

(MOSFETs' geometry in layout design)

- In drawing the layout of the CMOS NAND gate, there are **design considerations** in the MOSFETs' geometry:
  - typically $L_n = L_p$ (do you know why?)
  - usually $V_{T0n} = |V_{T0p}|$ in CMOS logic technology
  - $I_{Dn} = |I_{Dp}|$ (or equivalently $R_{neq} = R_{peq}$) for the same fall time and rise time at the output
  - if inputs are different (i.e. $V_A \neq V_B$ ), then $\mu_n\left(\frac{W_n}{2L}\right) = \mu_p\left(\frac{W_p}{L}\right)$
  - if inputs are the same (i.e. $V_A = V_B$ ), then $\mu_n\left(\frac{W_n}{2L}\right) = \mu_p\left(\frac{2W_p}{L}\right)$
  - What $W_n$ (then $W_p$) to choose? $\Rightarrow$ designer's decision
  - Consider minimum $W_p$ (= 4λ?), chip area, speed, power, etc.

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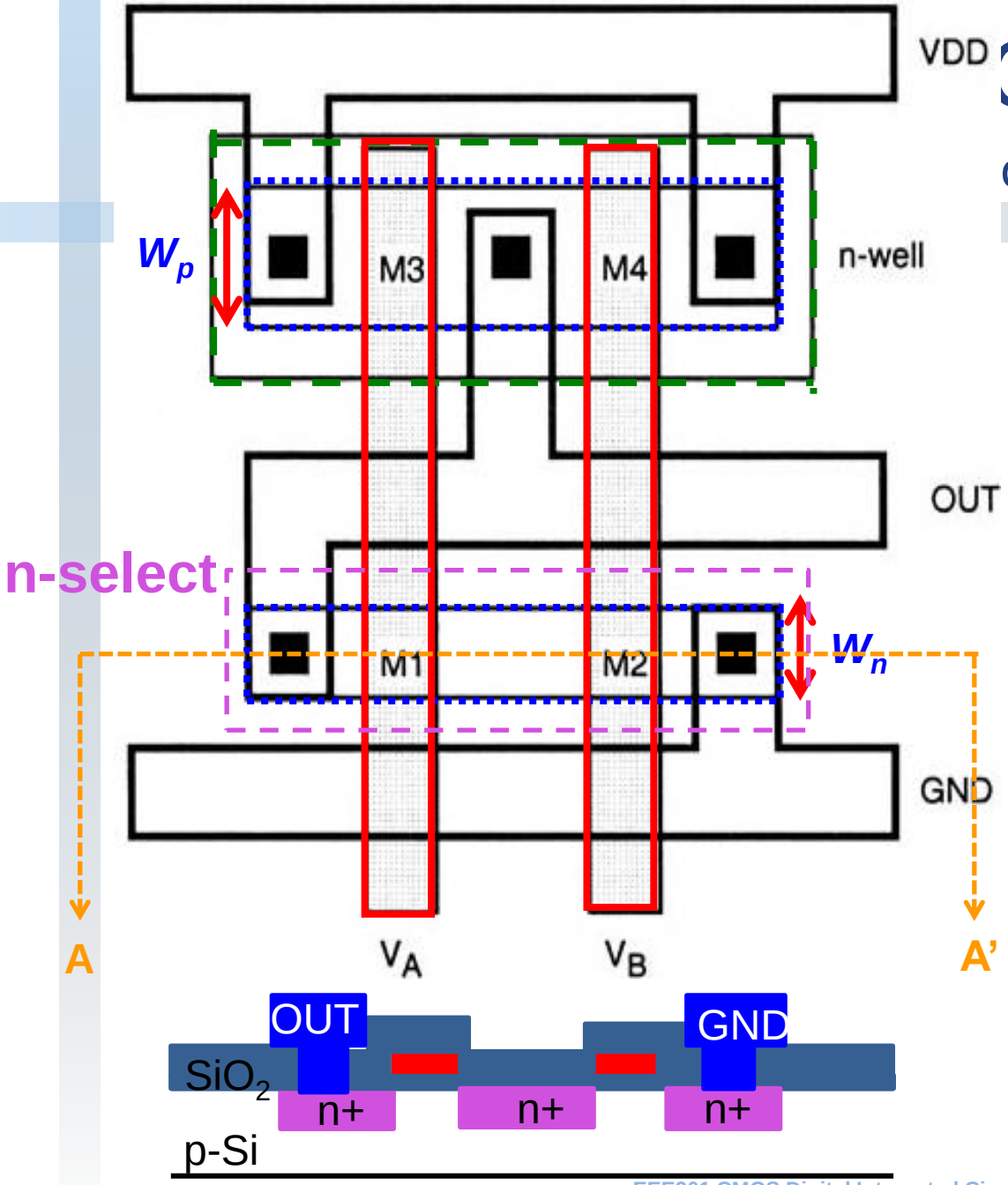
# CMOS NAND2

cross-sectional structure)




- The IC layout determines what device structure will be resulted from the IC fabrication:
  - Can you *visualise* (and sketch) the cross-sectional structure along the line segment AA' in the layout?

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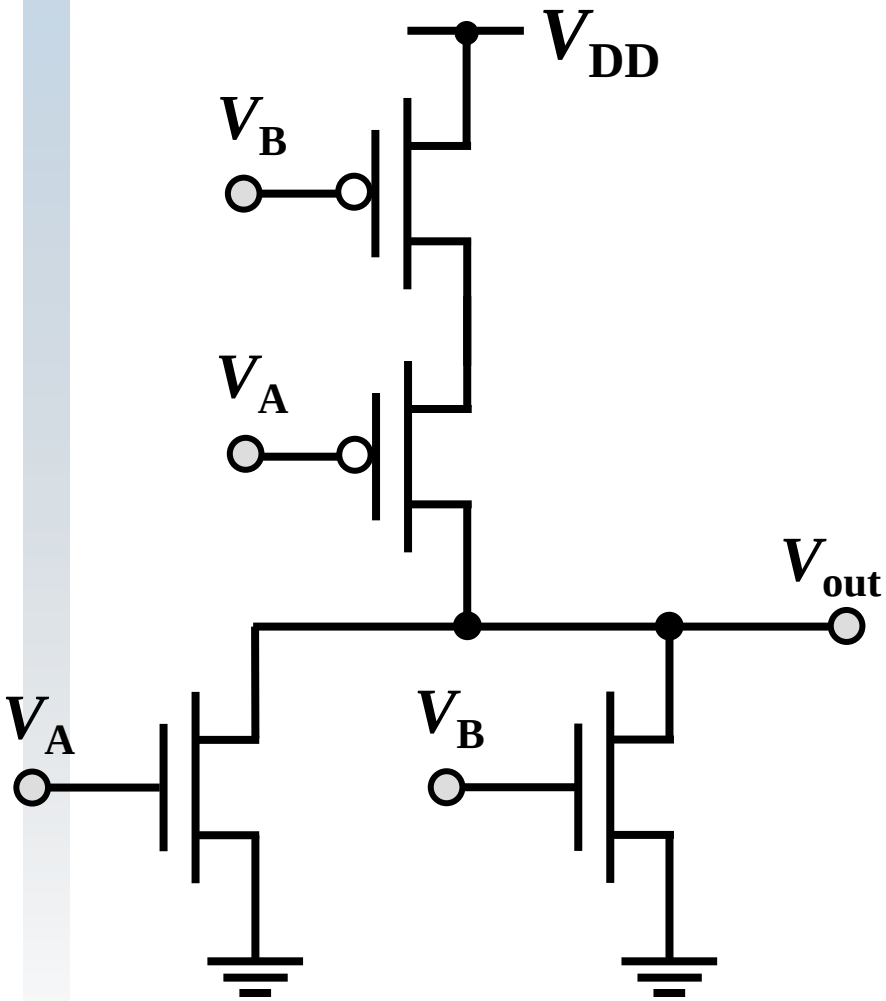
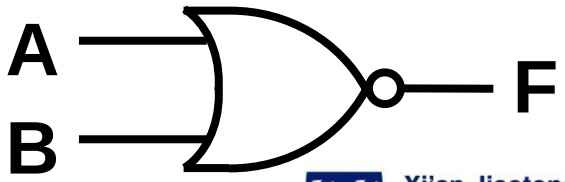
# NOR Logic - CMOS implementation

## (2 nMOSFETs in parallel & 2 pMOSFETs in series)




| $V_A$ | $V_B$ | $V_{out}$ |
|---|---|---|
| 0 V | 0 V | $V_{DD}$ |
| 0 V | $V_{DD}$ | 0 V |
| $V_{DD}$ | 0 V | 0 V |
| $V_{DD}$ | $V_{DD}$ | 0 V |

$$F = \overline{A + B}$$




| A | B | F |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

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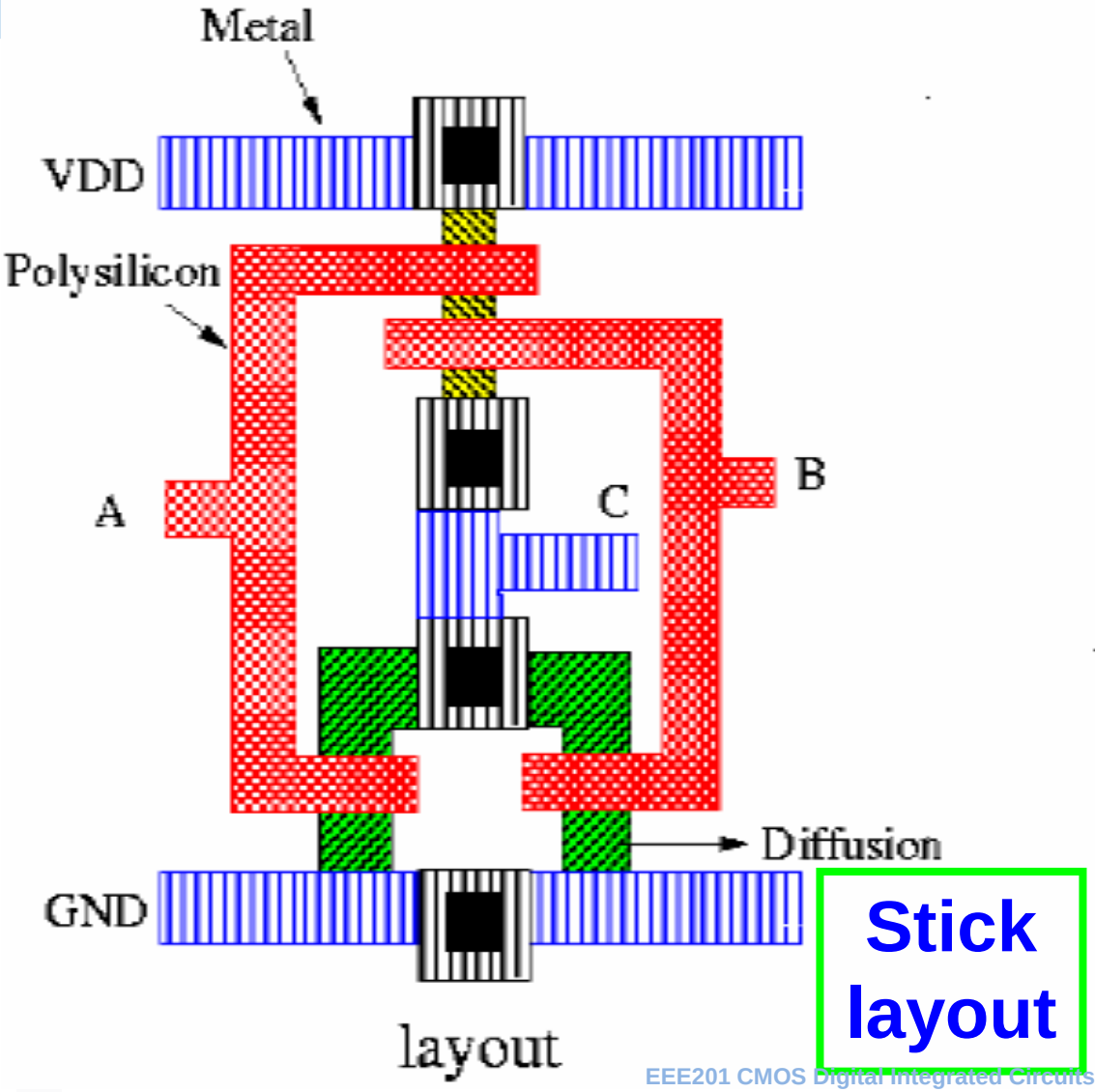
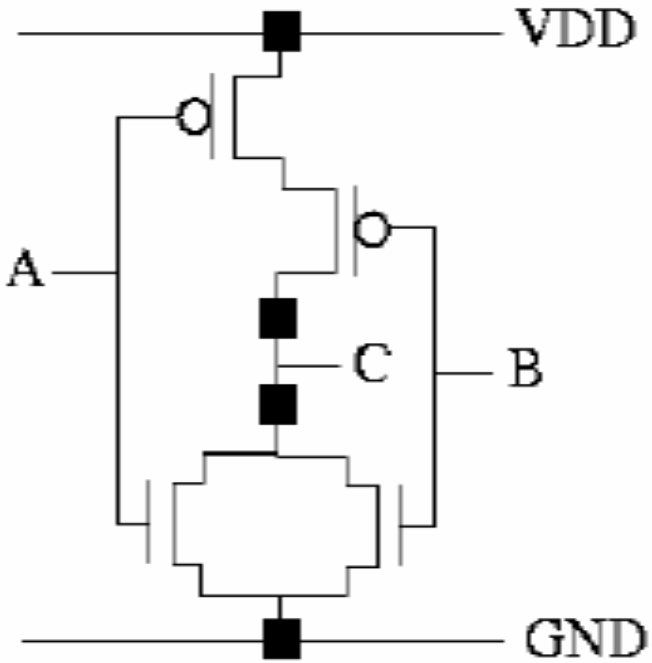
# CMOS NOR Logic Gate

(rough design with stick layout)



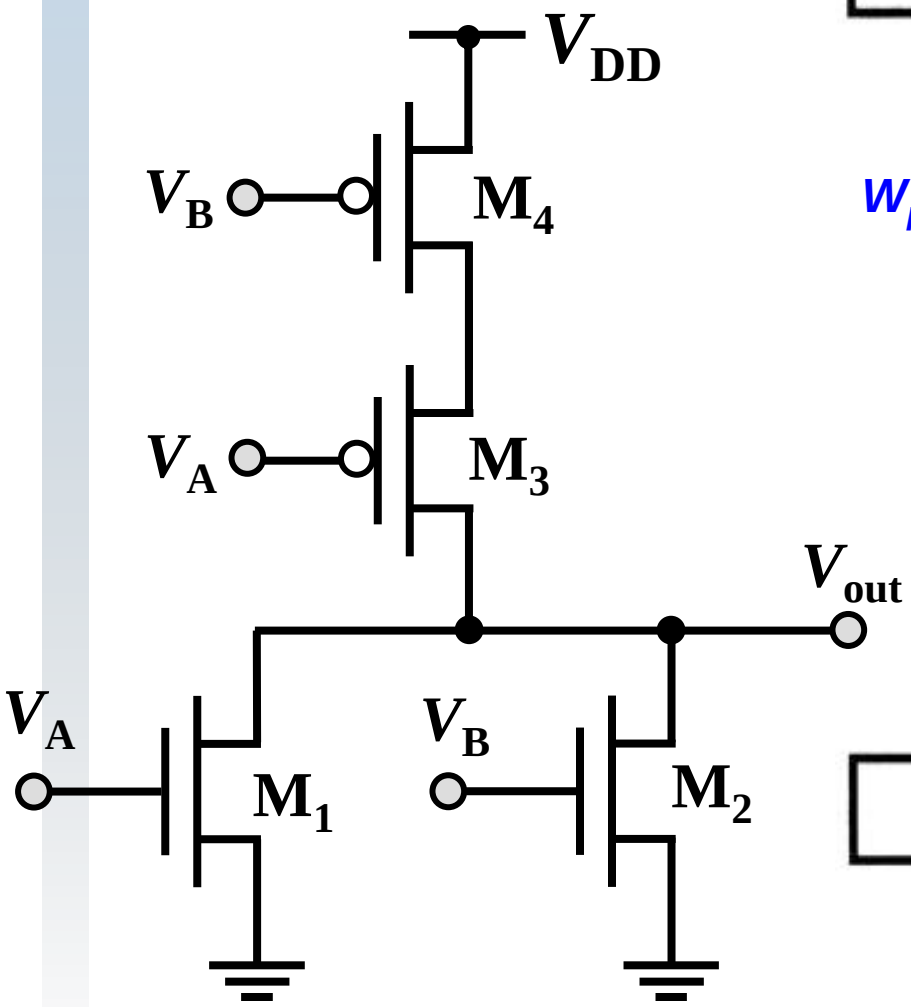

| A | B | C |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

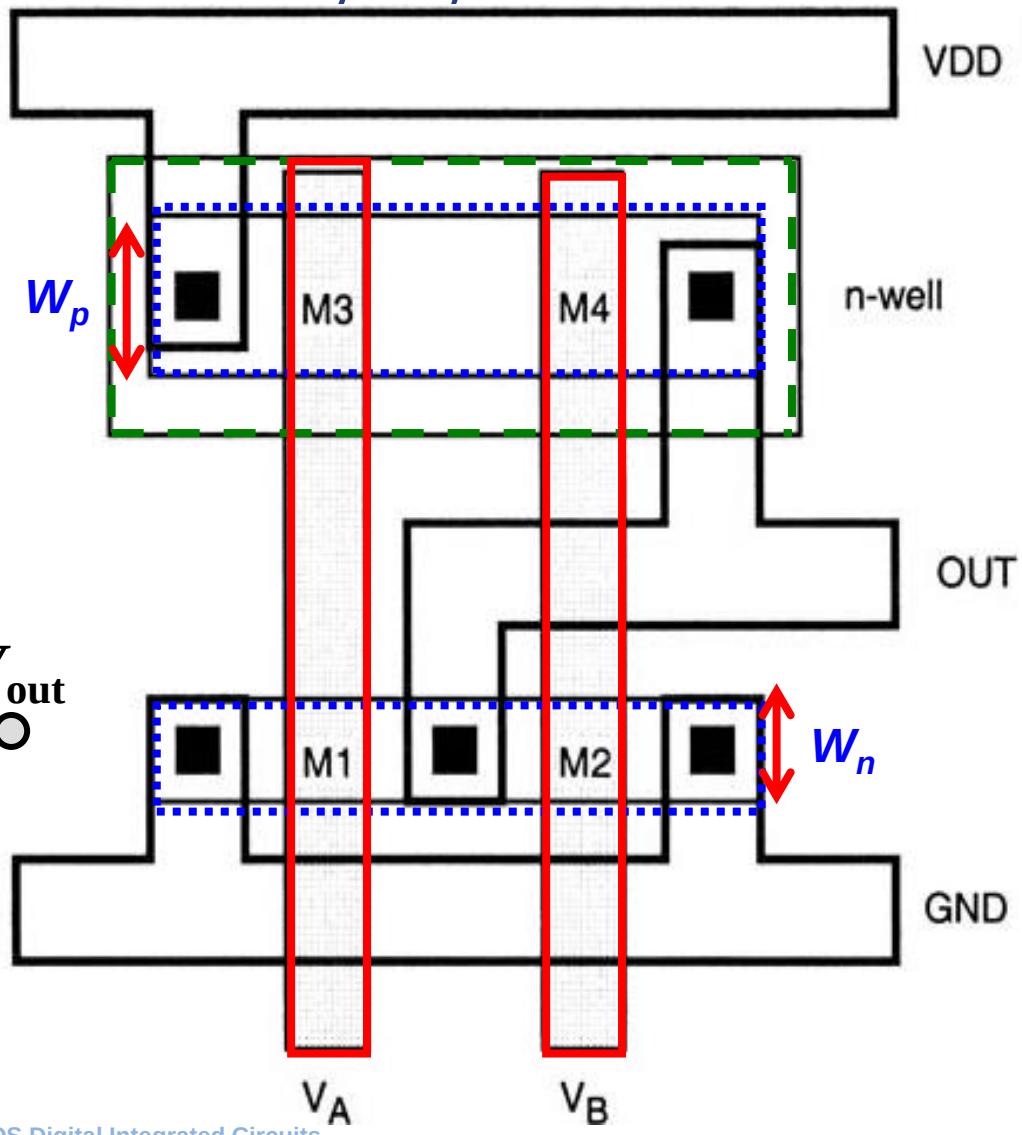



**Stick layout**

# CMOS NOR Logic Gate

(proper IC layout improved from stick layout)



# CMOS **NOR2** – design considerations

(what $W_p$ to choose in the layout)

- In drawing the CMOS NOR gate layout, there are similar **design considerations** like those in the NAND2:
  - normally $L_n = L_p$ (= 2λ as the minimum feature size)
  - usually $V_{T0n} = |V_{T0p}|$ in CMOS logic technology
  - $I_{Dn} = |I_{Dp}|$ (or equivalently $R_{neq} = R_{peq}$) for the same **fall time** and **rise time** at the output
  - if inputs are the same (i.e. $V_A = V_B$ ), then $\mu_n\left(\frac{2W_n}{L}\right) = \mu_p\left(\frac{W_p}{2L}\right)$
  - if inputs are different (i.e. $V_A \neq V_B$ ), then $\mu_n\left(\frac{W_n}{L}\right) = \mu_p\left(\frac{W_p}{2L}\right)$
  - Choose $W_p = 8W_n$ or $W_p = 4W_n$ (when $\mu_n = 2\mu_p$)?
  - Consider minimum $W_n$ (= 4λ?), chip area, speed, power, etc.

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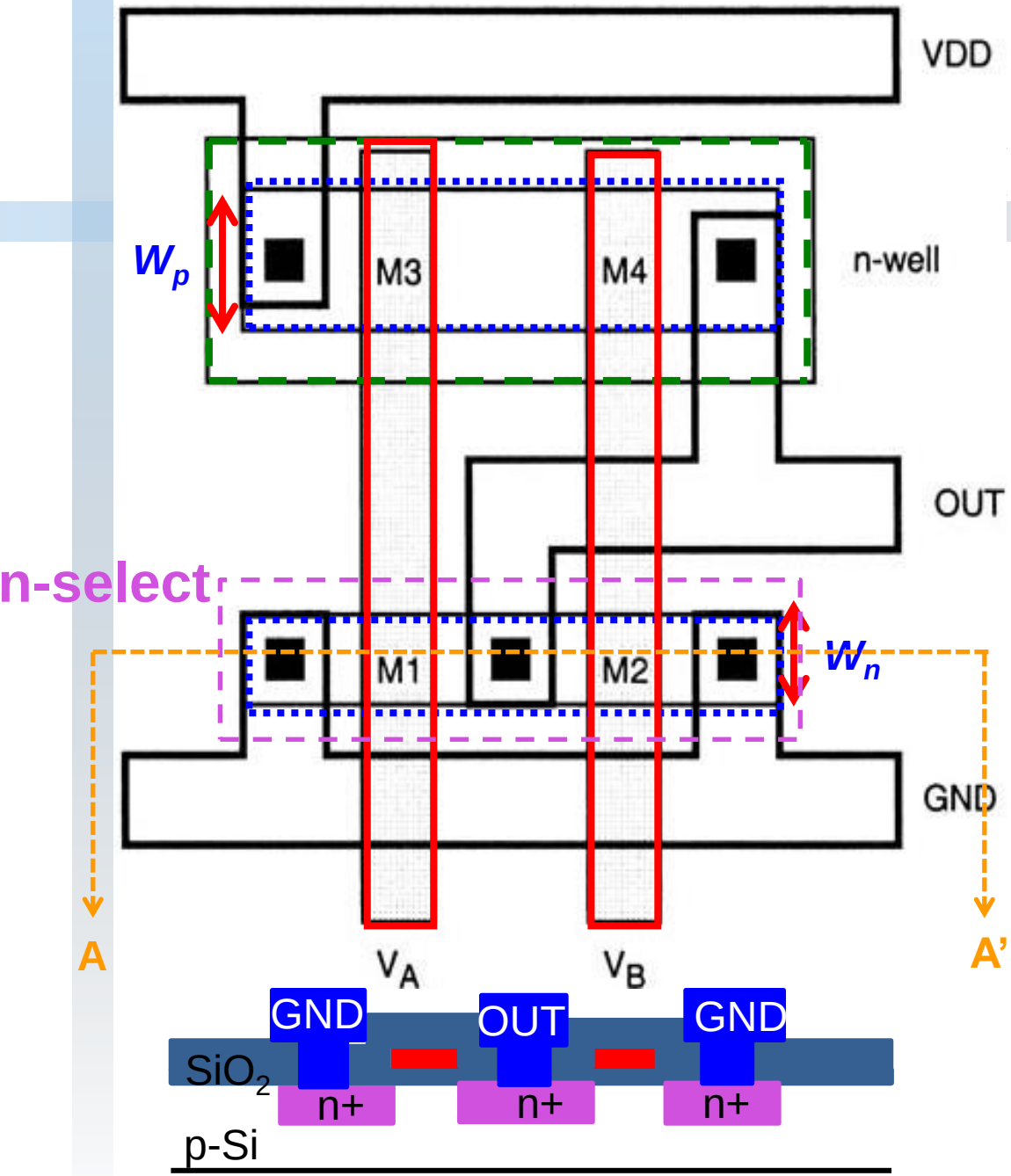
# CMOS NOR2

cross-sectional structure)




- The CMOS NOR gate layout looks similar to that of the NAND counterpart:
  - Can you *visualise* (and sketch) the slightly different cross-sectional structure along the line segment AA' in the layout?

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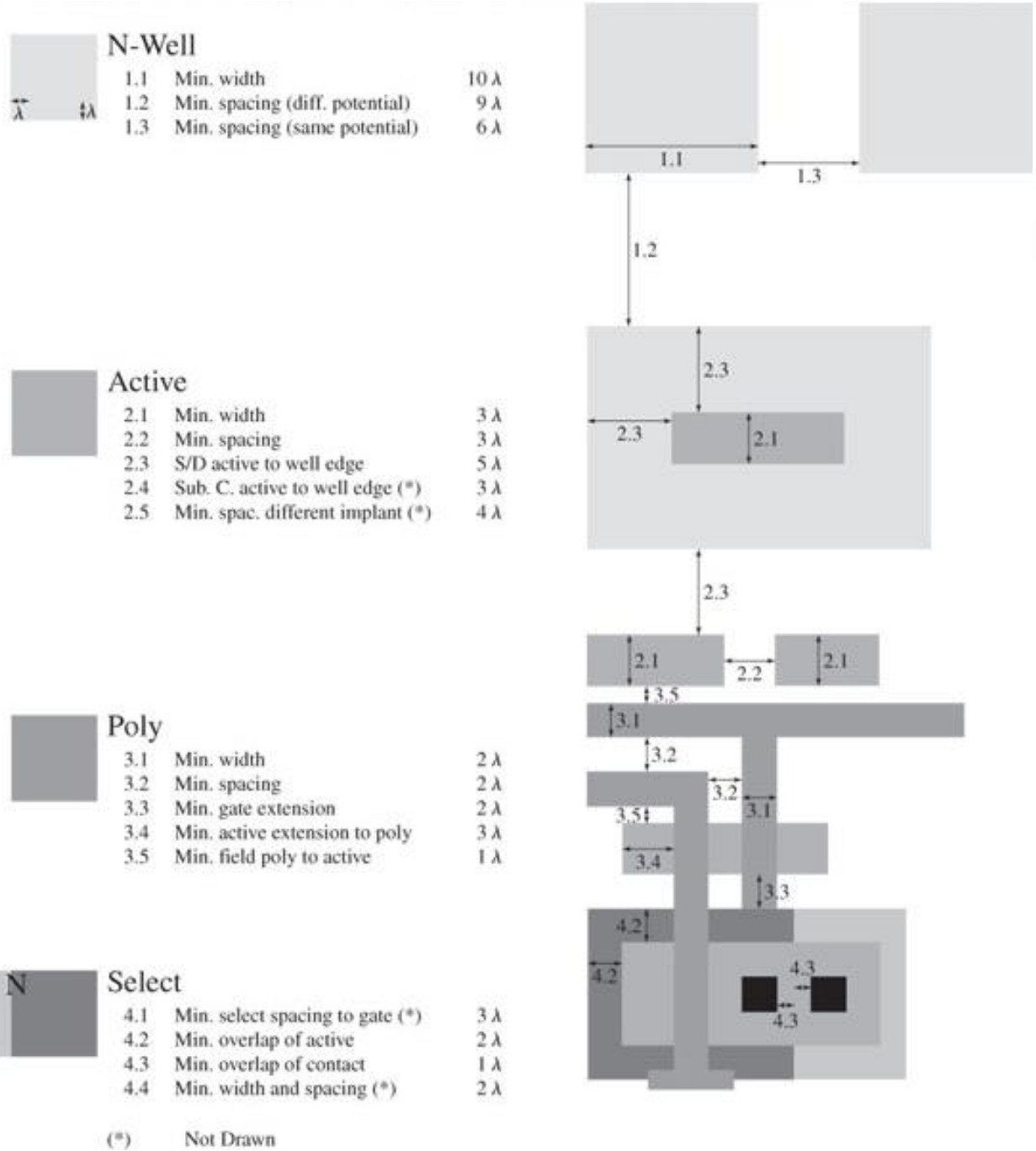
# More Rul

(*n*-well & *n*-select

- In a CMOS process, the *n*-well usually has a much lower doping concentration compared with the source/drain regions of the nMOSFETs defined by the *n*-select.



# More Ru

## (via1 & metal2)

- The **via1** mask layer is similar to (with real difference from) the contact mask layer. It is the vertical electrical connection between **metal1** & **metal2**.

**Contact**

| | | |
|---|---|---|
| 5.1 | Exact contact size | 2 λ |
| 5.2 | Min. poly overlap | 1.5 λ |
| 5.3 | Min. spacing | 2 λ |
| 5.4 | Min. spacing to gate | 2 λ |
| 6.1 | Exact contact size | 2 λ |
| 6.2 | Min. active overlap | 1.5 λ |
| 6.3 | Min. spacing | 2 λ |
| 6.4 | Min. spacing to gate | 2 λ |

**Metal1**

| | | |
|---|---|---|
| 7.1 | Min. width | 3 λ |
| 7.2.a | Min. spacing | 3 λ |
| 7.3 | Min. overlap of any contact | 1 λ |

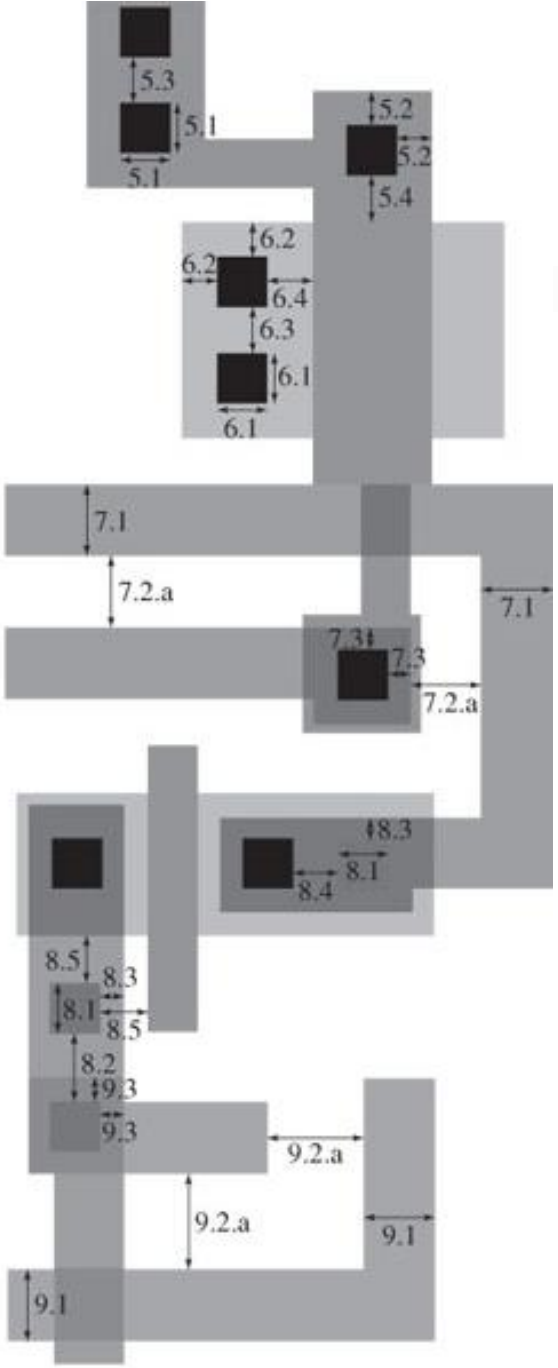
**Via1**

| | | |
|---|---|---|
| 8.1 | Exact size | 2 λ |
| 8.2 | Min. spacing | 3 λ |
| 8.3 | Min. overlap by metal1 | 1 λ |
| 8.4 | Min. spacing to contact | 2 λ |
| 8.5 | Min. spac. to poly or act. edge | 2 λ |

**Metal2**

| | | |
|---|---|---|
| 9.1 | Min. width | 3 λ |
| 9.2.a | Min. spacing | 4 λ |
| 9.3 | Min. overlap to via1 | 1 λ |

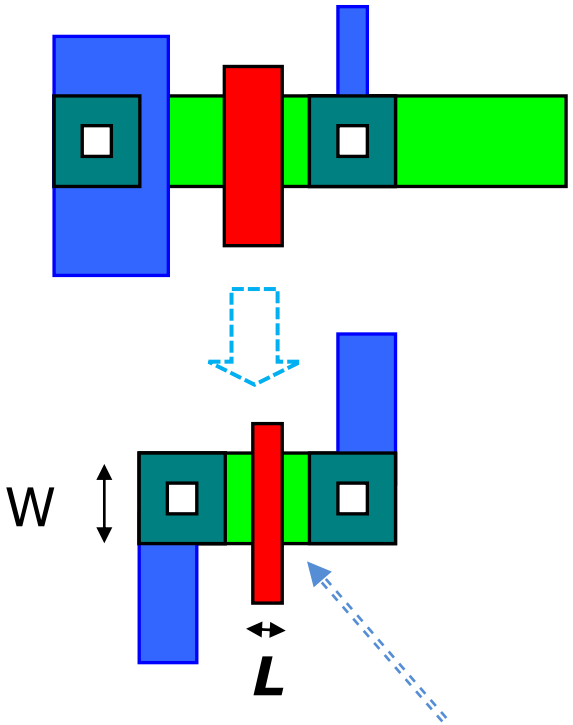
(*) Not Drawn



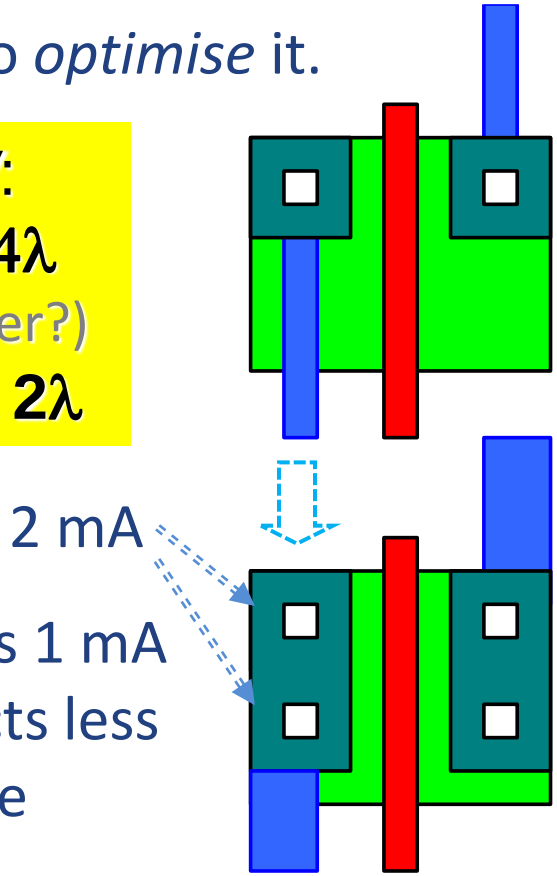
# CMOS IC Layout - practical tips

(minimum channel width & other sizes in the λ-rule)

- In drawing an IC layout, it desirable to *optimise* it.




**minimum *W*:**
**1λ+2λ+1λ = 4λ**
(can it be smaller?)
**minimum *L*: 2λ**




- 1 contact allows 1 mA
- multiple contacts less series resistance

- Minimise source/drain regions
- Use minimum gate length ***L*** (2λ)

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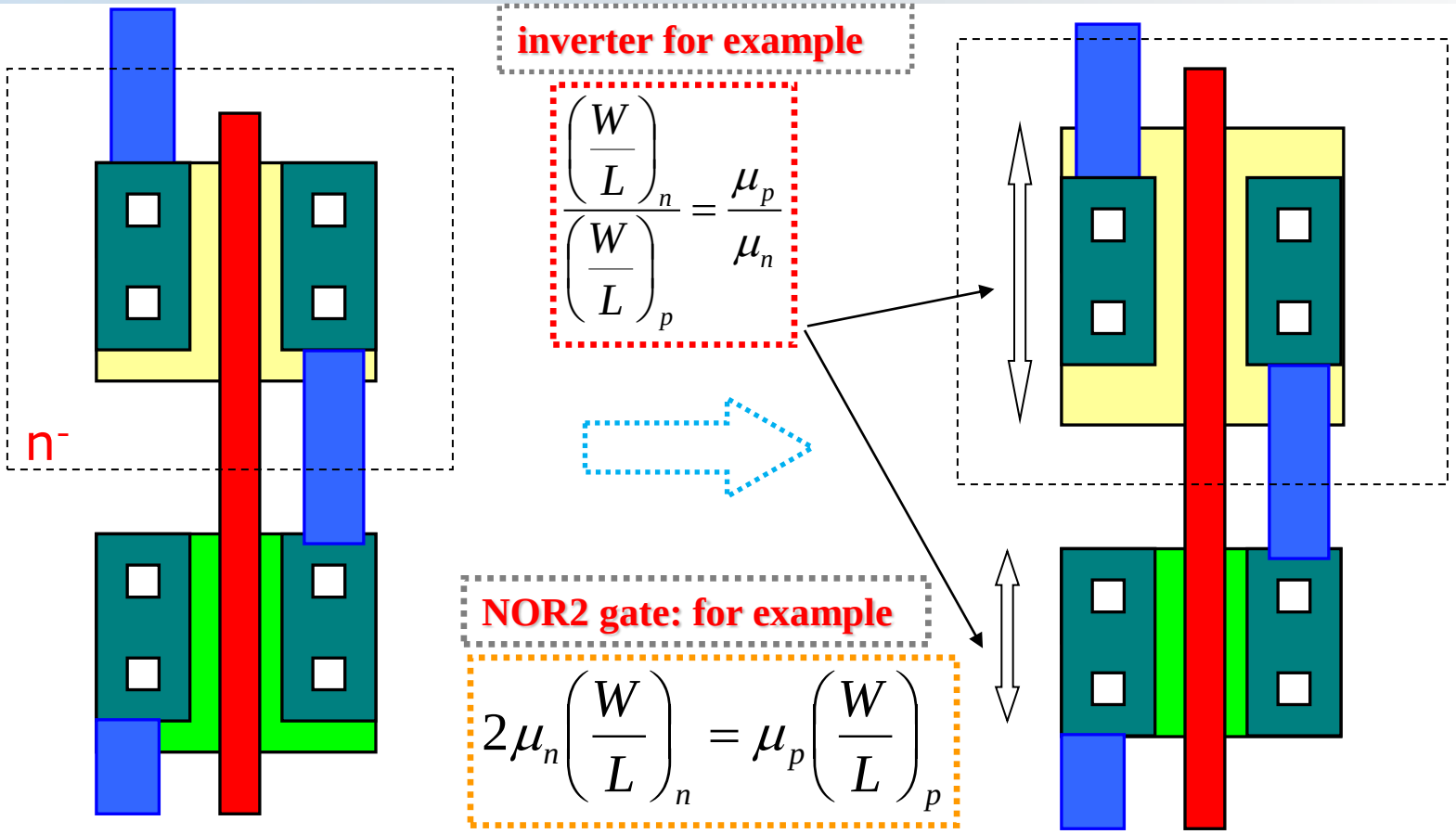
# CMOS IC Layout - practical tips

(MOSFET geometrical sizes)




- ***L* = minimum feature size**
- $W_p = ?W_n \Rightarrow$ decision based on design consideration

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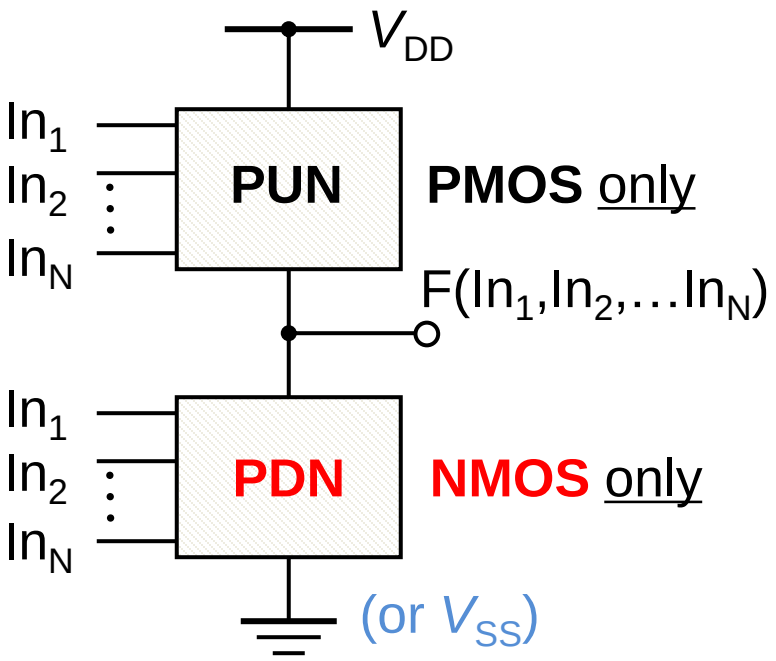
# From Inverter, NAND & NOR

(generalisation to CMOS logic circuits)

- Based on the CMOS logic inverter, NAND and NOR gates, the operation and design principles can be generalised to CMOS combinational logic circuits with ***N*** inputs.




- for any combinations of inputs to produce a logic "1" at the output, the upper network of pMOSFETs should provide a low resistance path from the output to $V_{DD}$;
- otherwise, the PMOS network should be of a high resistance.

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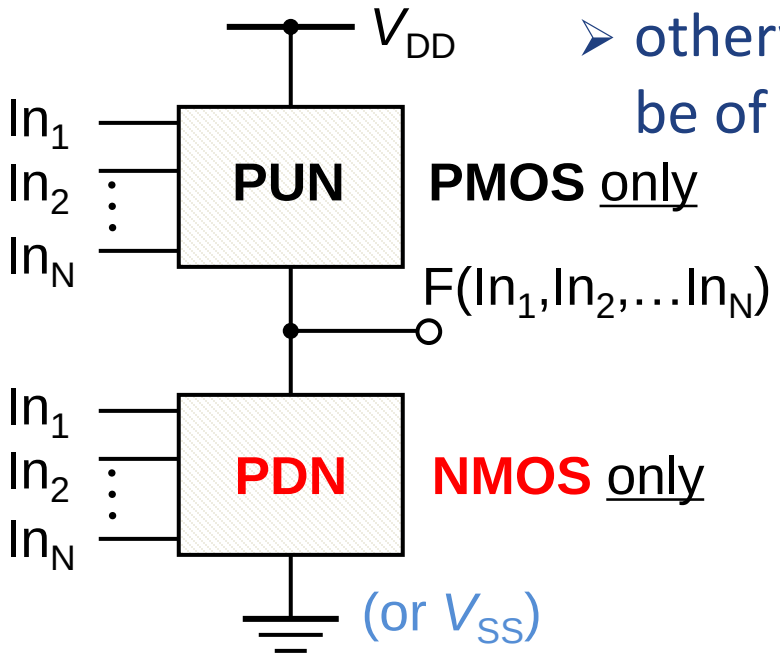
# CMOS Logic Circuits

(low DC power consumption)

- for any combinations of inputs to produce a logic "0" at the output, the bottom network of nMOSFETs should provide a low resistance path from the output to ground;




- otherwise, the NMOS network should be of a high resistance.

- When the output is constant, either logic "0" or "1", the CMOS logic circuits *ideally* draws no current; (it does draw currents when the output ***switches*** from logic "0" to "1" or "1" to "0").

⇒ low DC power consumption in CMOS logic

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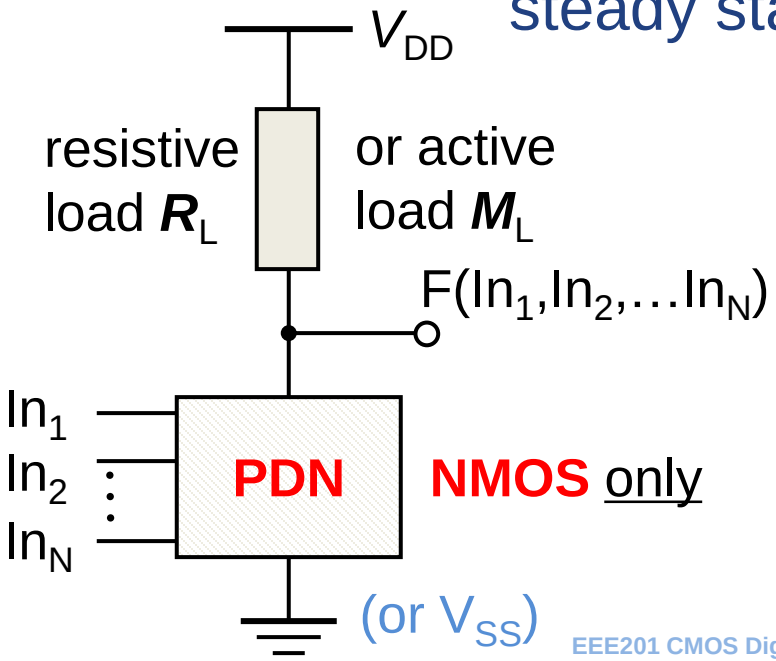
# Logic Circuits with NMOS only

(generalisation to CMOS logic circuits)

- Even without using the PMOS network but a resistive load, the circuits still work (i.e. performing the Boolean logic function).
  - However, DC power consumption is high even in the steady state (i.e. the output is constant).




  - Do you know what output logic state here will draw currents steadily?
  - Can we replace the NMOS network instead with a resistive load? Why or why not?

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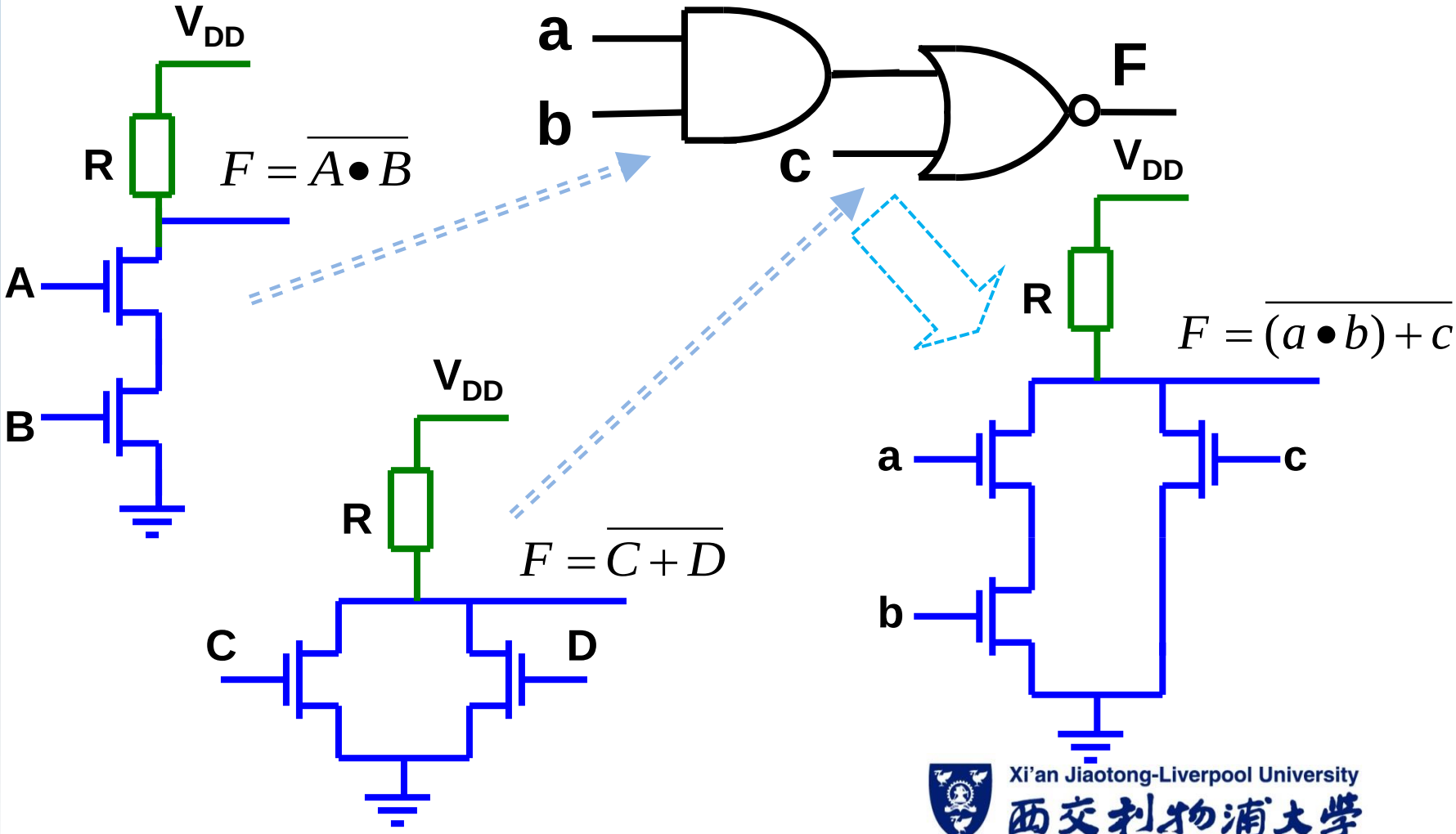
# More Complicated Logic Gates

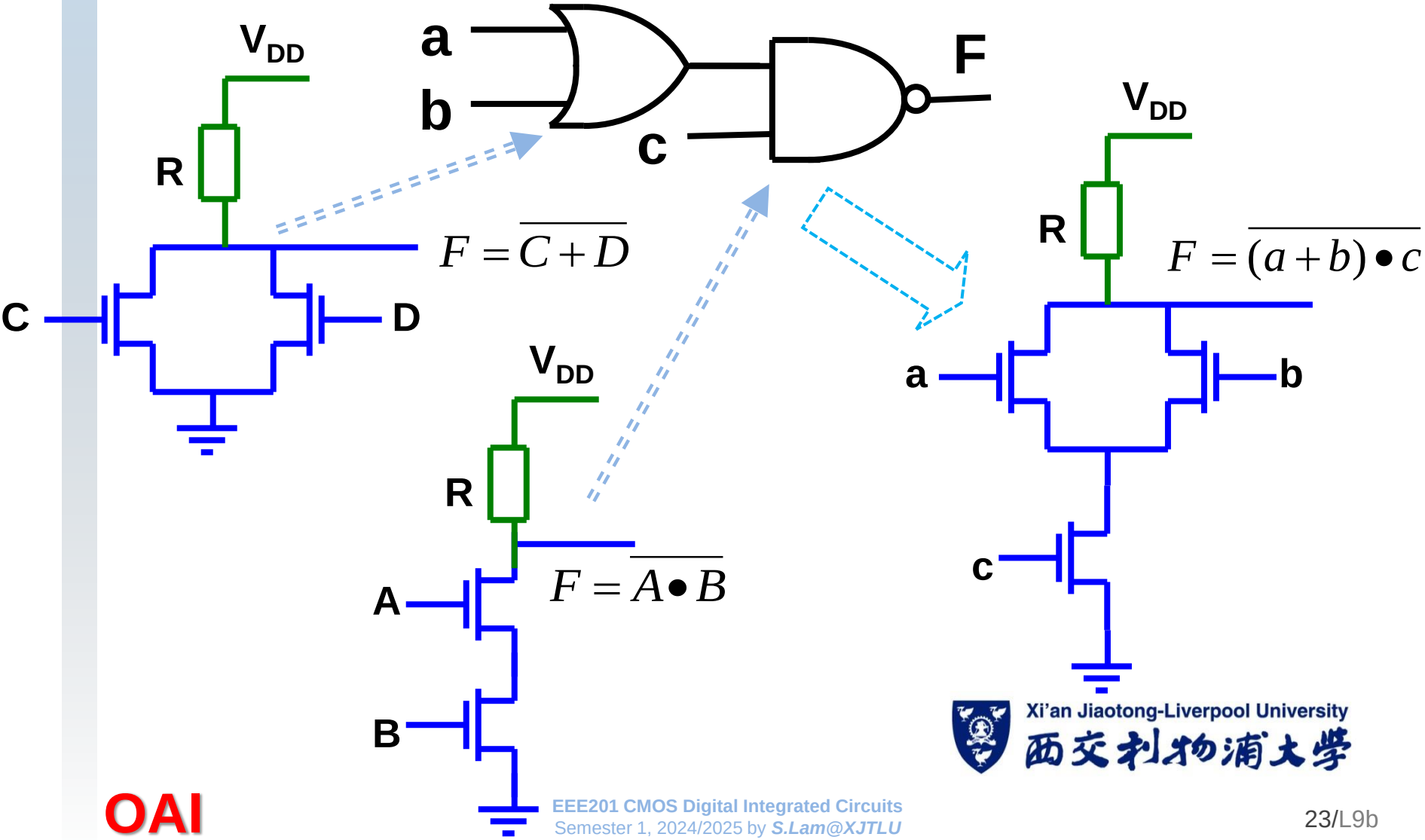
(AND-OR-Inverter)




AOI

# More Complicated Logic Gates

(OR-AND-Inverter)




OAI

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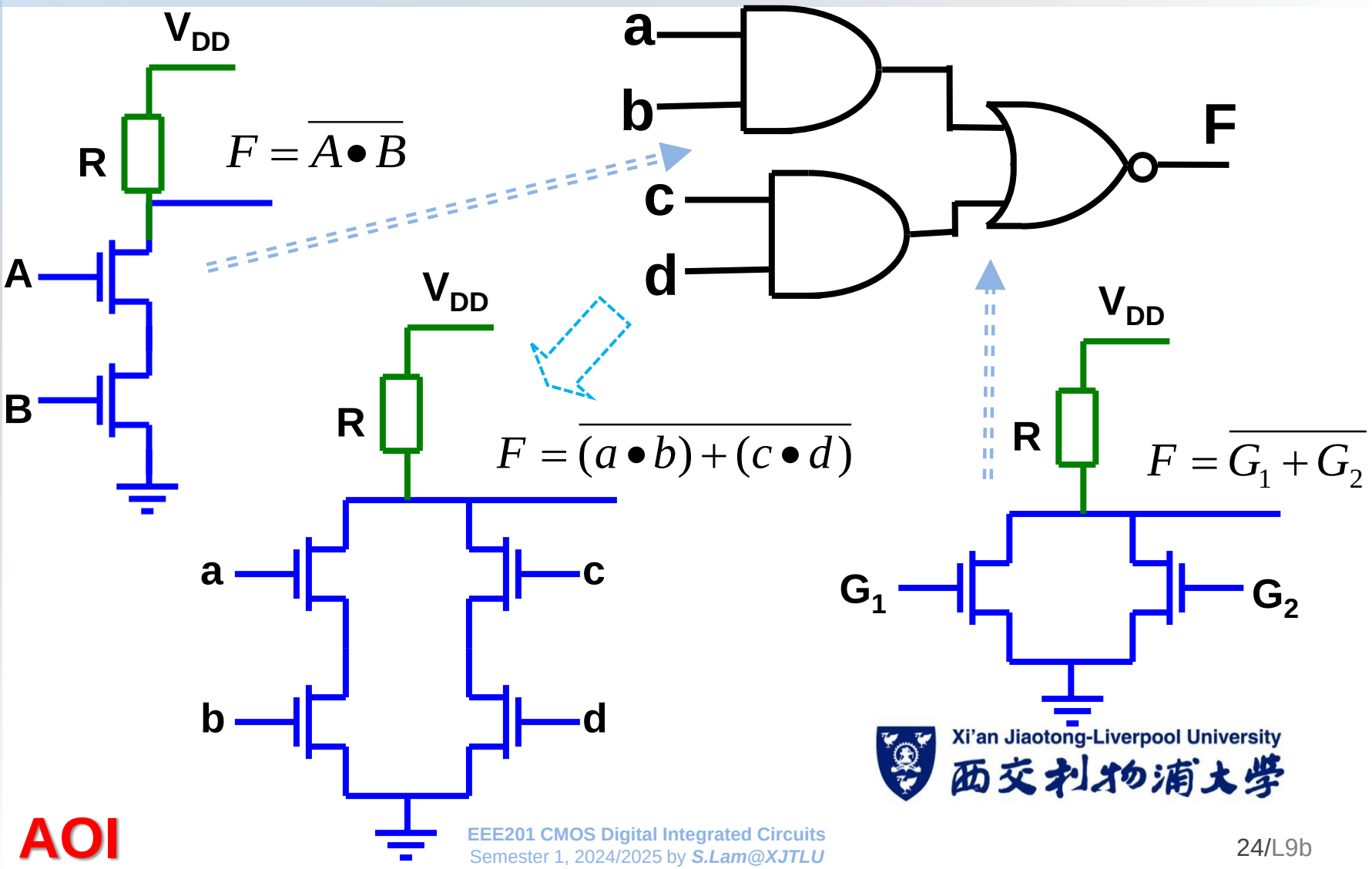
# More Complicated Logic Gates

## (AND-OR-Inverter)




AOI

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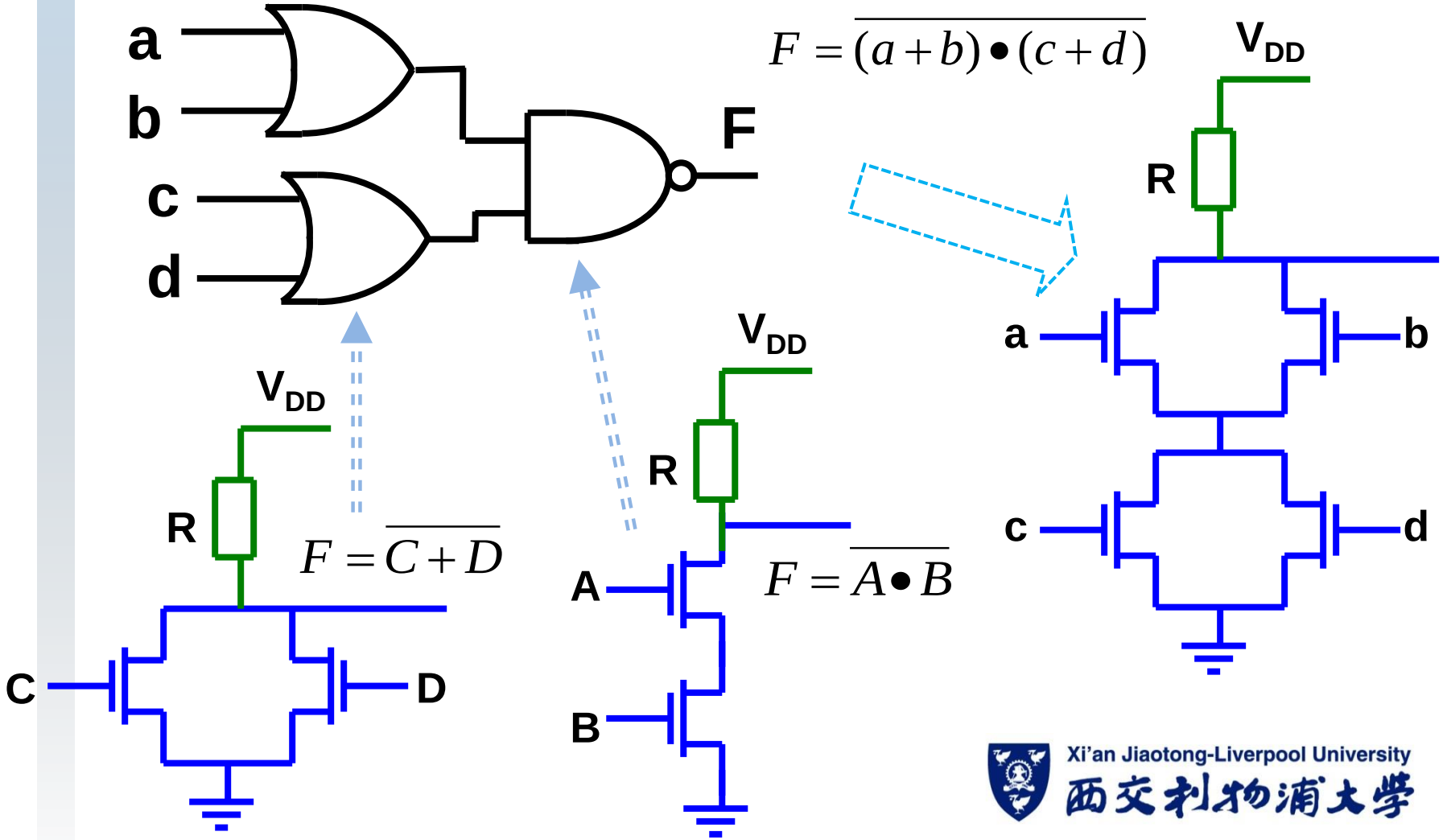
# More Complicated Logic Gates

## (OR-AND-Inverter)




OAI

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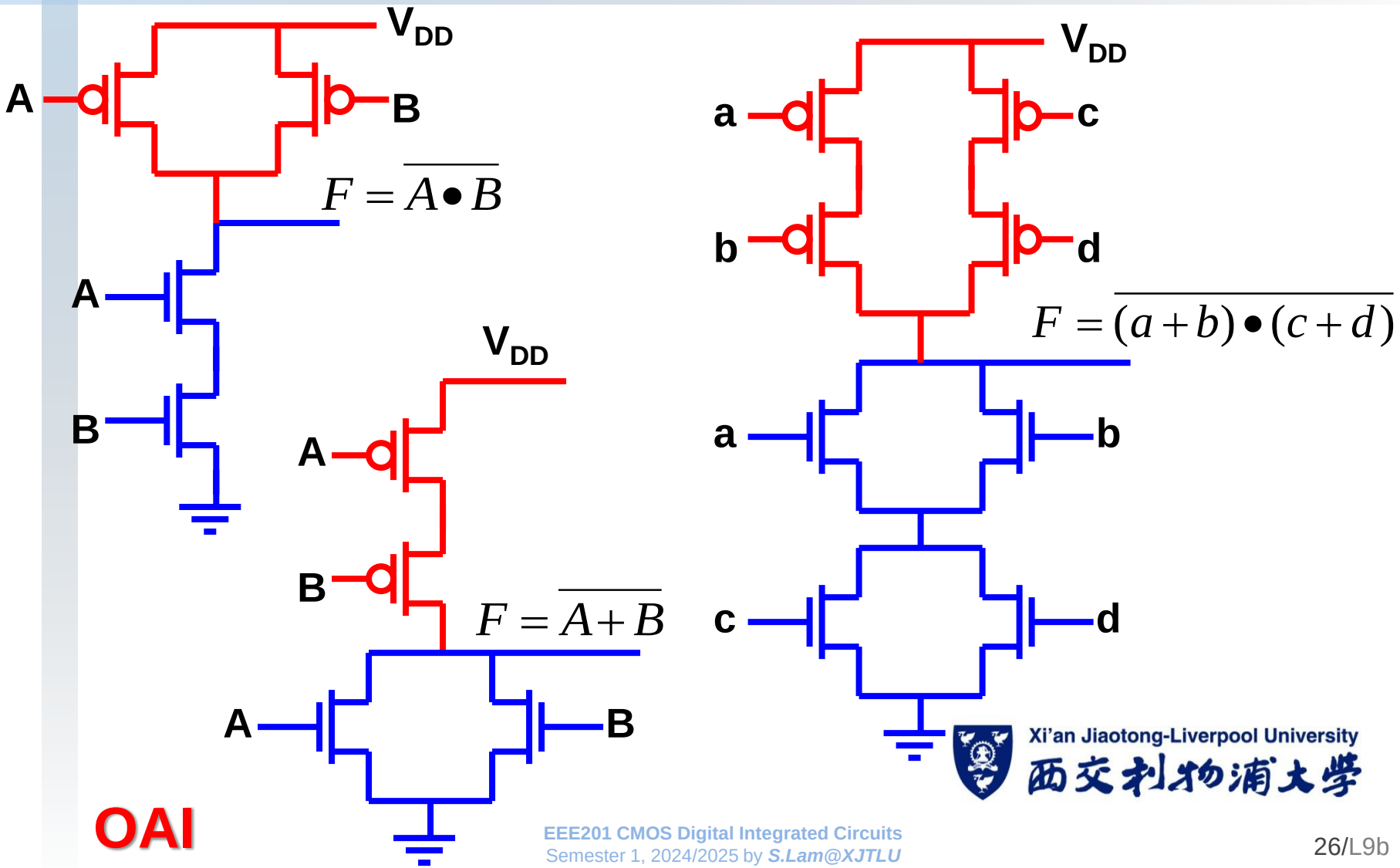
# More Complicated Logic Gates

## (PMOS network)




OAI

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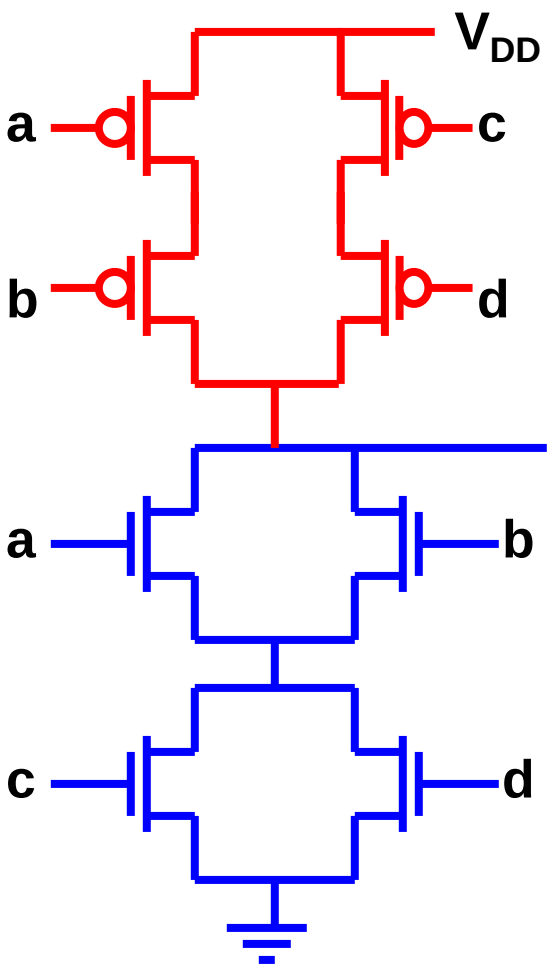
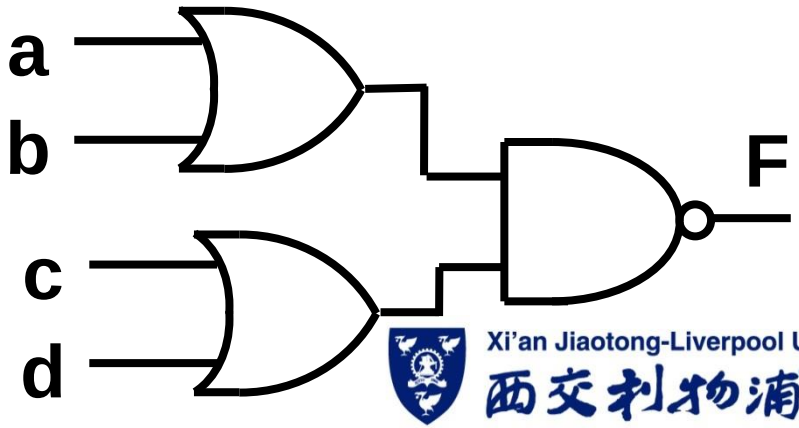
# More Complicated Logic Gates

(built from NAND & NOR circuits )




- It can be seen that complicated CMOS logic gates can be built from the NAND and NOR circuits (with either OAI or AOI combinations).

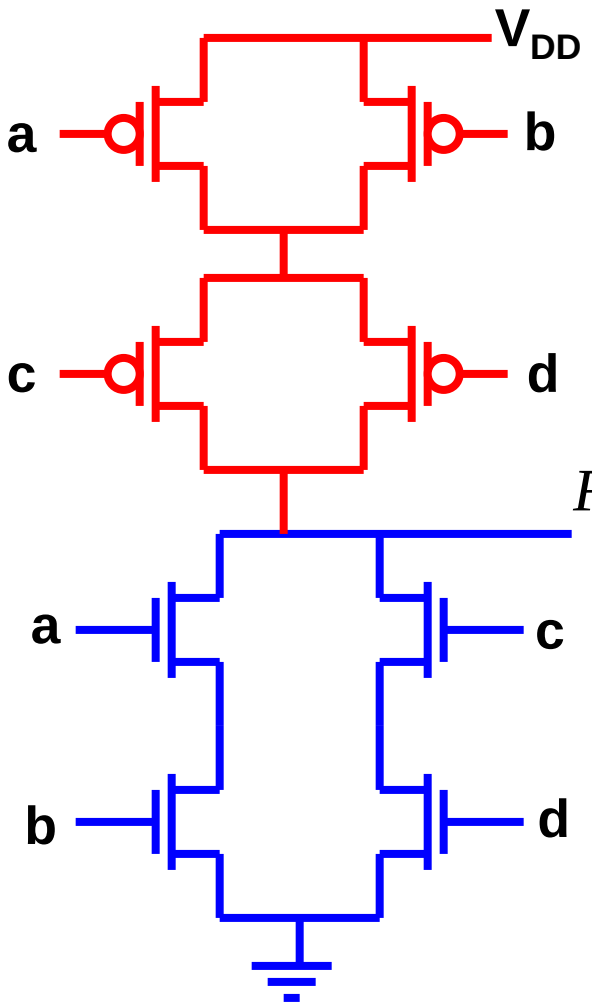
$$F = \overline{(a+b)\bullet(c+d)}$$




OAI

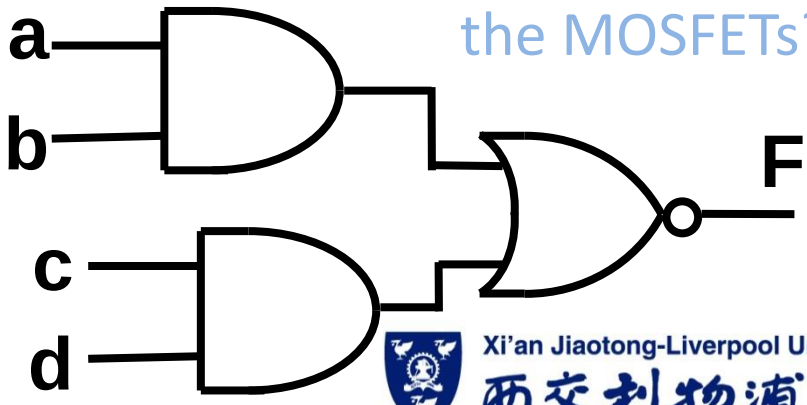
# More Complicated Logic Gates

(OAI vs. AOI combinations)




- Note the same MOSFET configuration as in OAI but with the inputs applied differently.
  - Do you see the differences in the inputs applied to the MOSFETs?

$$F = \overline{(a \bullet b) + (c \bullet d)}$$

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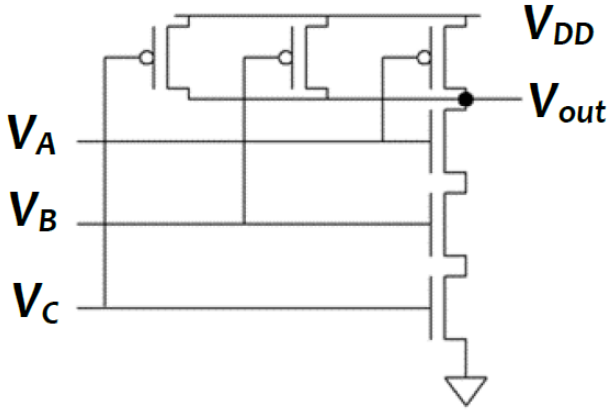
**AOI**

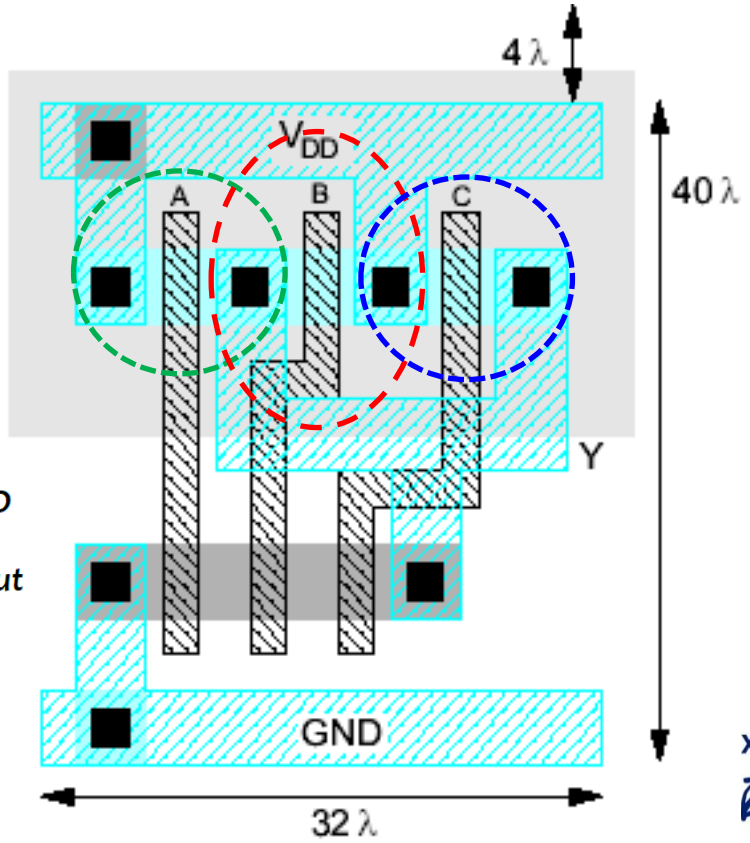
# More Complicated Logic Gates

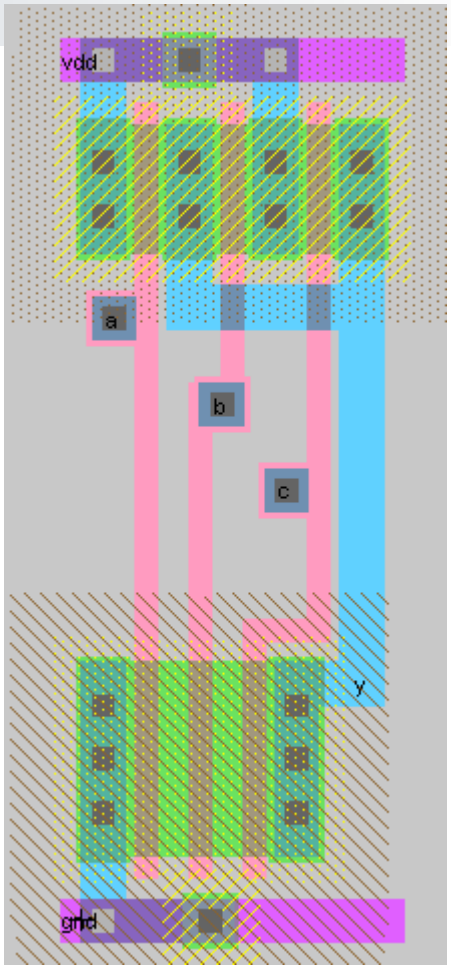
(apply same layout design principles)

- schematic circuit ⇒ physical layout
  - 3-input NAND gate in CMOS

design considerations in $W_p$ & $W_n$, chip area, etc.

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