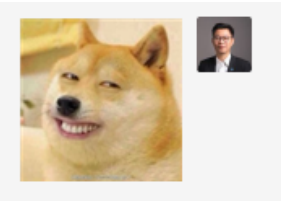
MOS Capacitance

- **MOS structure**
- MOS energy band diagram
- Effects of applied biases
- *Voltage drops



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April 2024

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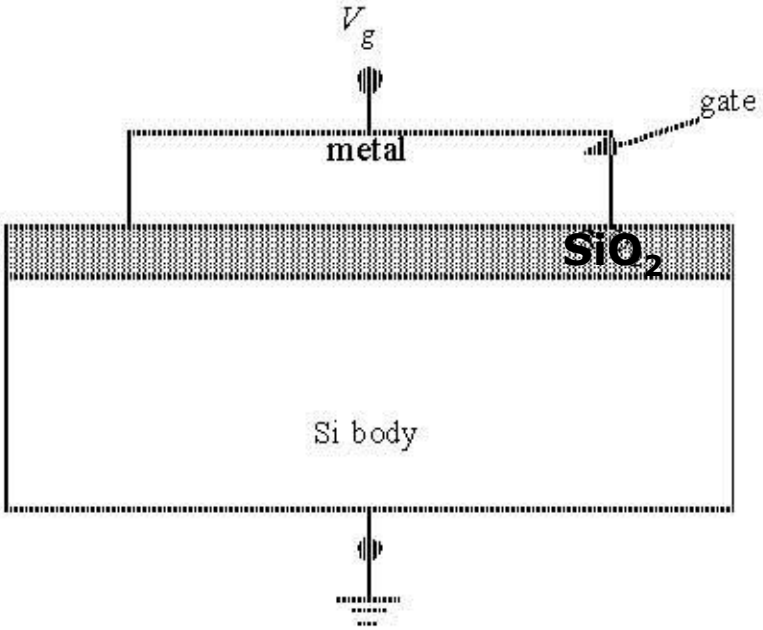
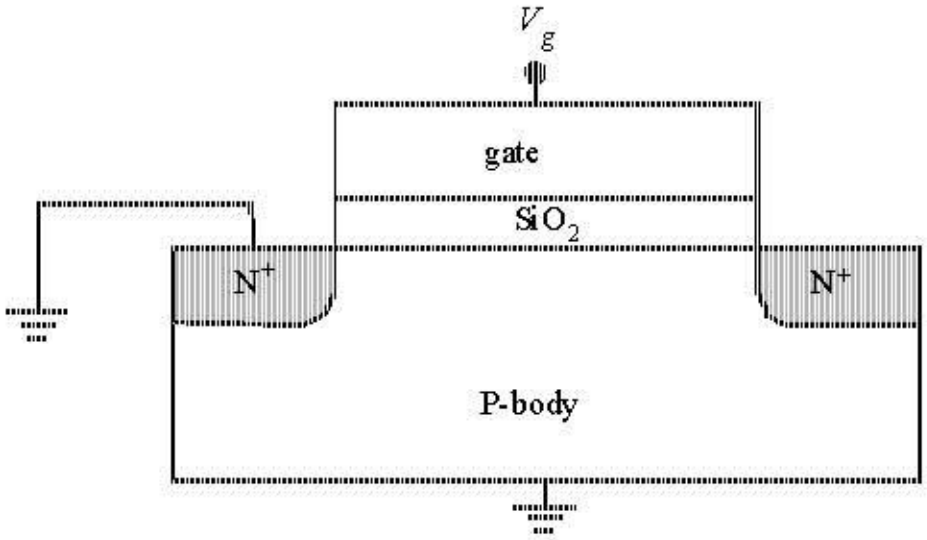
MOS Capacitors

MOS: Metal-Oxide-Semiconductor



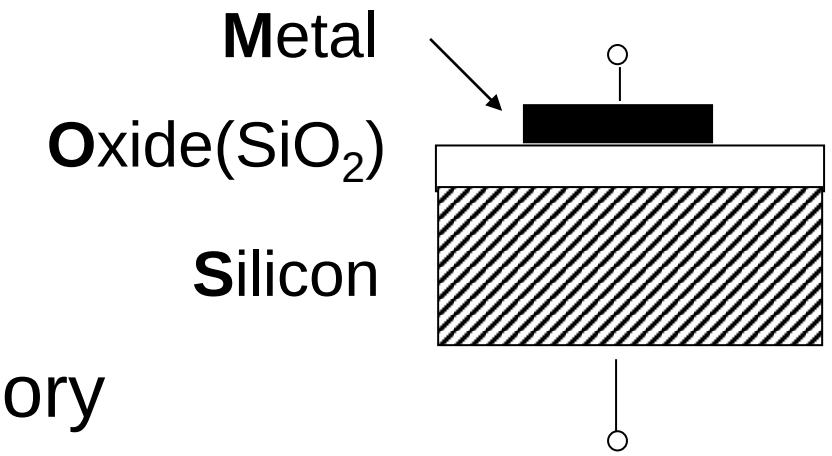
MOS capacitor



MOS transistor

MOS Capacitors

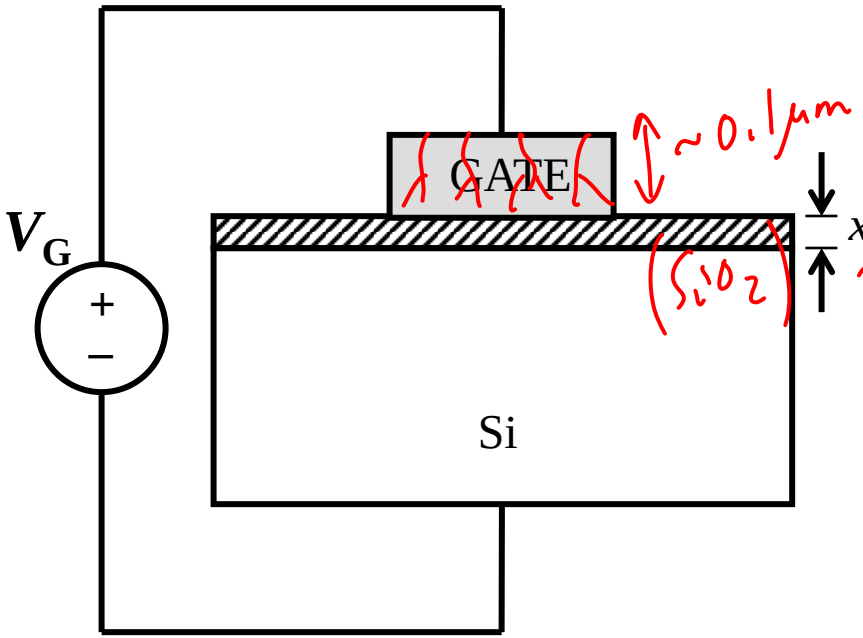
- **Why** capacitors
  - Foundation for **understanding** **MOS transistors**



- **Applications**
  - CCD camera
  - Non-volatile memory
  - Test structure during fabrication
  - As a component

MOS Capacitor Structure

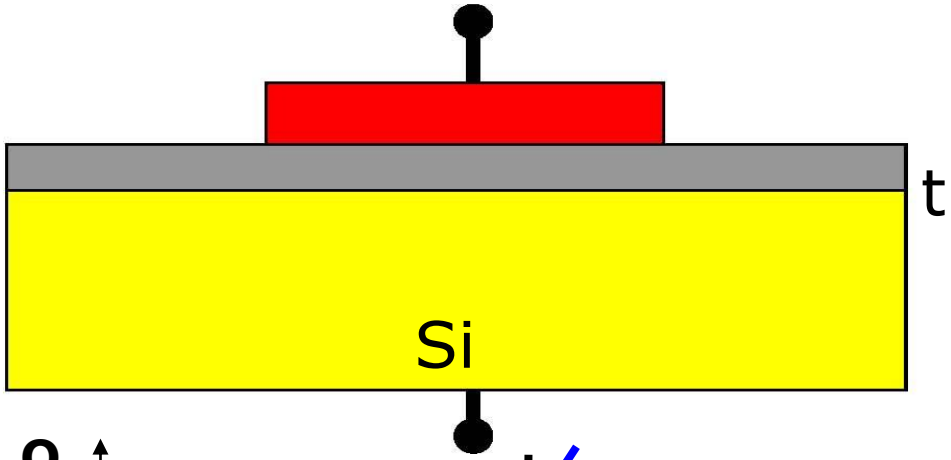
MOS capacitor (cross-sectional view)



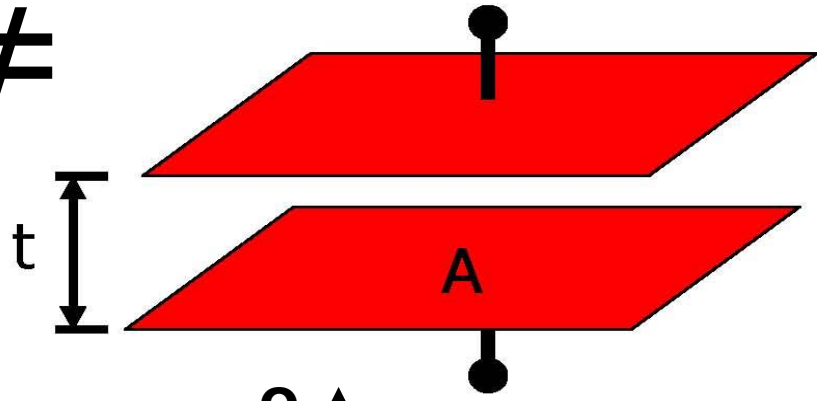
- **Typical MOS capacitors** and transistors in ICs today employ
  - **heavily doped polycrystalline Si** ("poly-Si") film as the gate-electrode material
    - n^+-type, for "n-channel" transistors (NMOS)
    - p^+-type, for "p-channel" transistors (PMOS)
  - **SiO_2 as the gate dielectric**
    - band gap = 9 eV
    - $\varepsilon_{r,SiO2}$ = **3.9**
  - **Si as the semiconductor material**
    - p-type, for "n-channel" transistors (**NMOS**)
    - n-type, for "p-channel" transistors (**PMOS**)

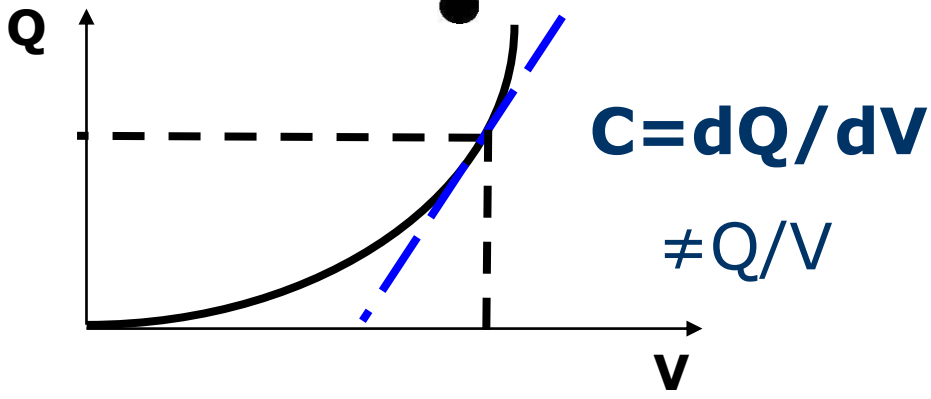
MOS Capacitor

parallel-plate capacitor



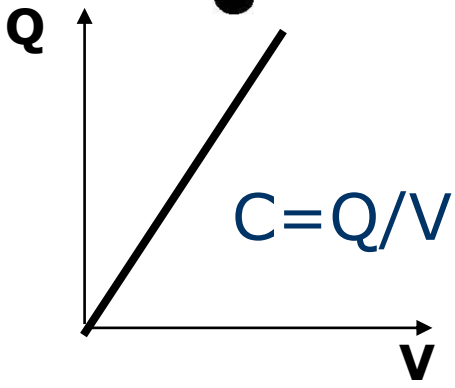
≠





C=dQ/dV

≠Q/V

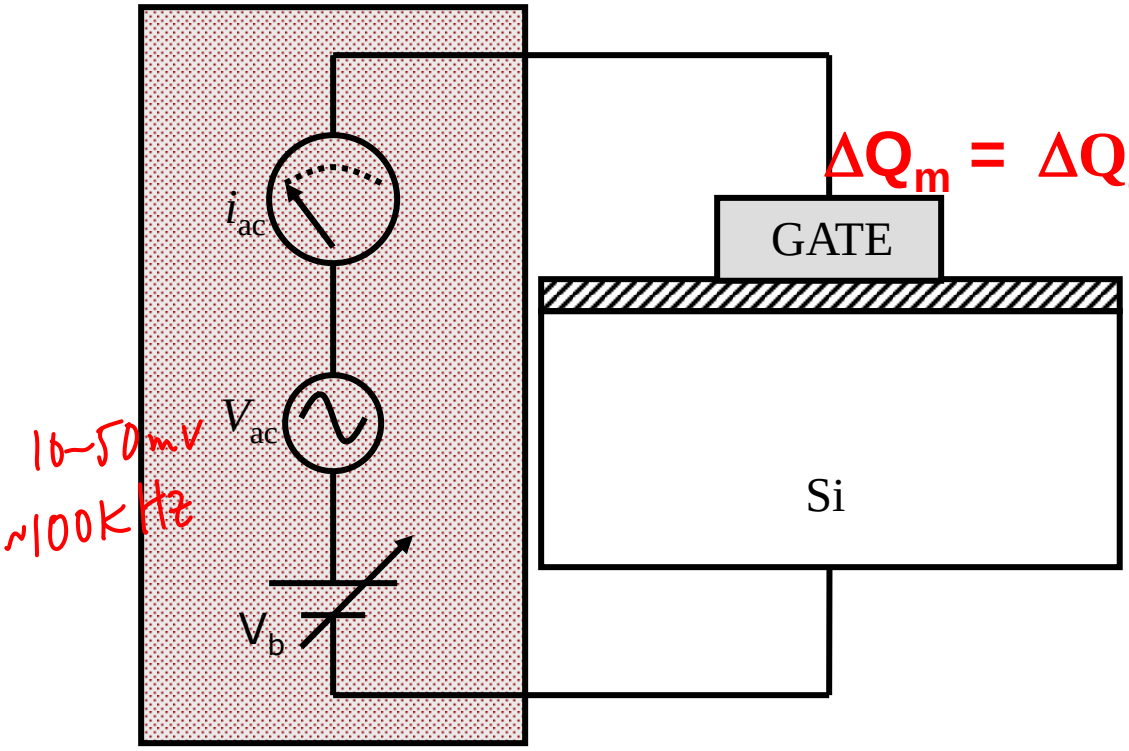


C=Q/V

- Definition: $C = \varepsilon A/t = \varepsilon_r \varepsilon_o A/t$

where $\varepsilon_r (SiO_2) = 3.9$, $\varepsilon_o = 8.85 \times 10^{-14}$ F/cm

MOS Capacitance Measurement



C-V Meter MOS Capacitor

$|V_b| >> |V_{ac}|$

- V_b: **dc biasing** voltage and scanned slowly
- V_{ac}: small **ac** signal
- $V_g = V_b + V_{ac}$

$$C = \left|\frac{dQ_{GATE}}{dV_g}\right| = \left|\frac{dQ_s}{dV_g}\right| = \left|\frac{dQ_s}{dV_{ac}}\right|$$

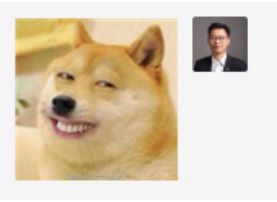
- Capacitive current due to V_{ac} is measured

$$i_{ac} = C\frac{dV_{ac}}{dt}$$

MOS Capacitance

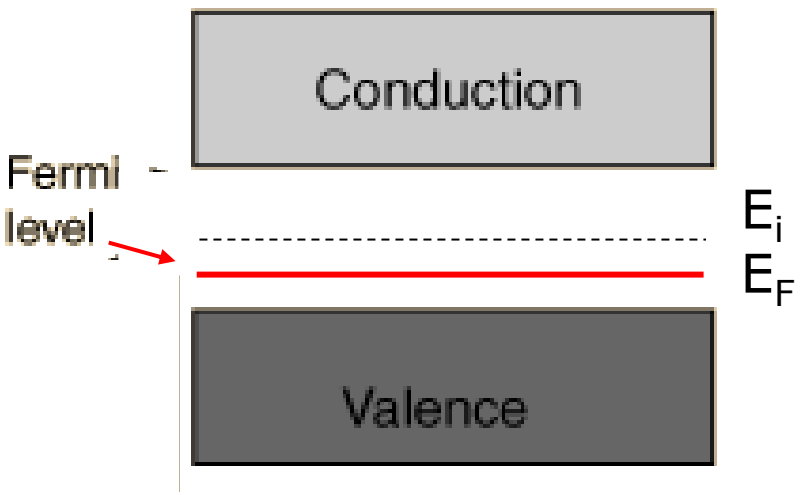
OUTLINE

- MOS structure
- **MOS energy band diagram**
- Effects of applied biases
- *Voltage drops

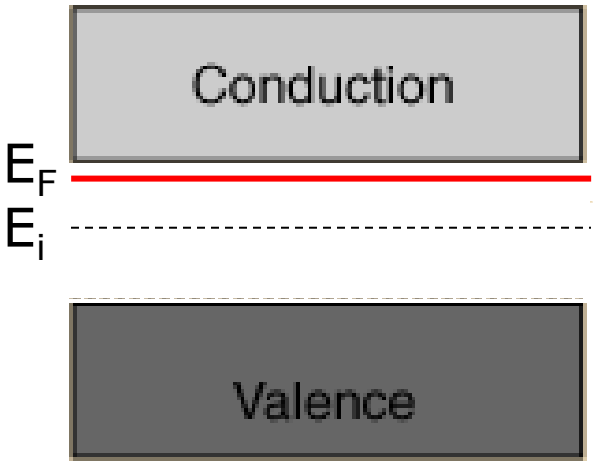


Reference reading: Chapter 6.0-6.4

Which one is the **p-type Si**?

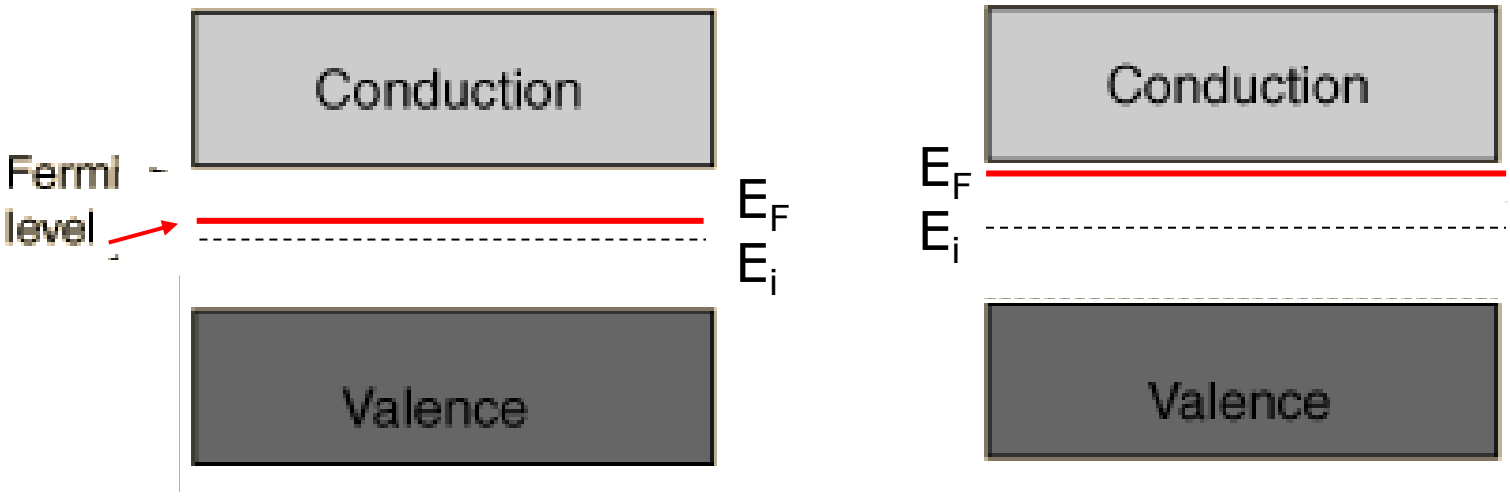


N_A



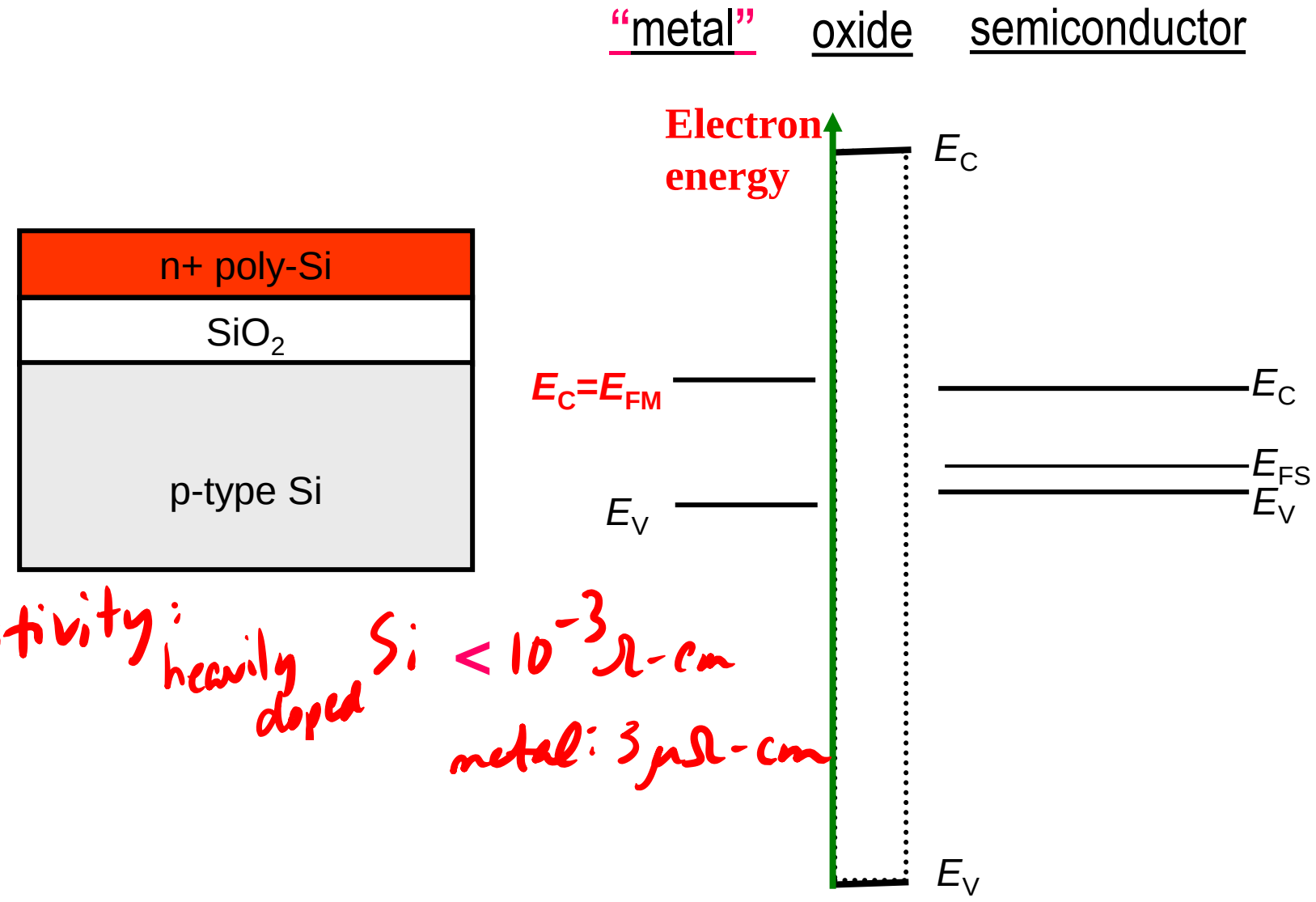
N_D

Which one is the **heavily doped Si?**



$$N_{D1} < N_{D2}$$

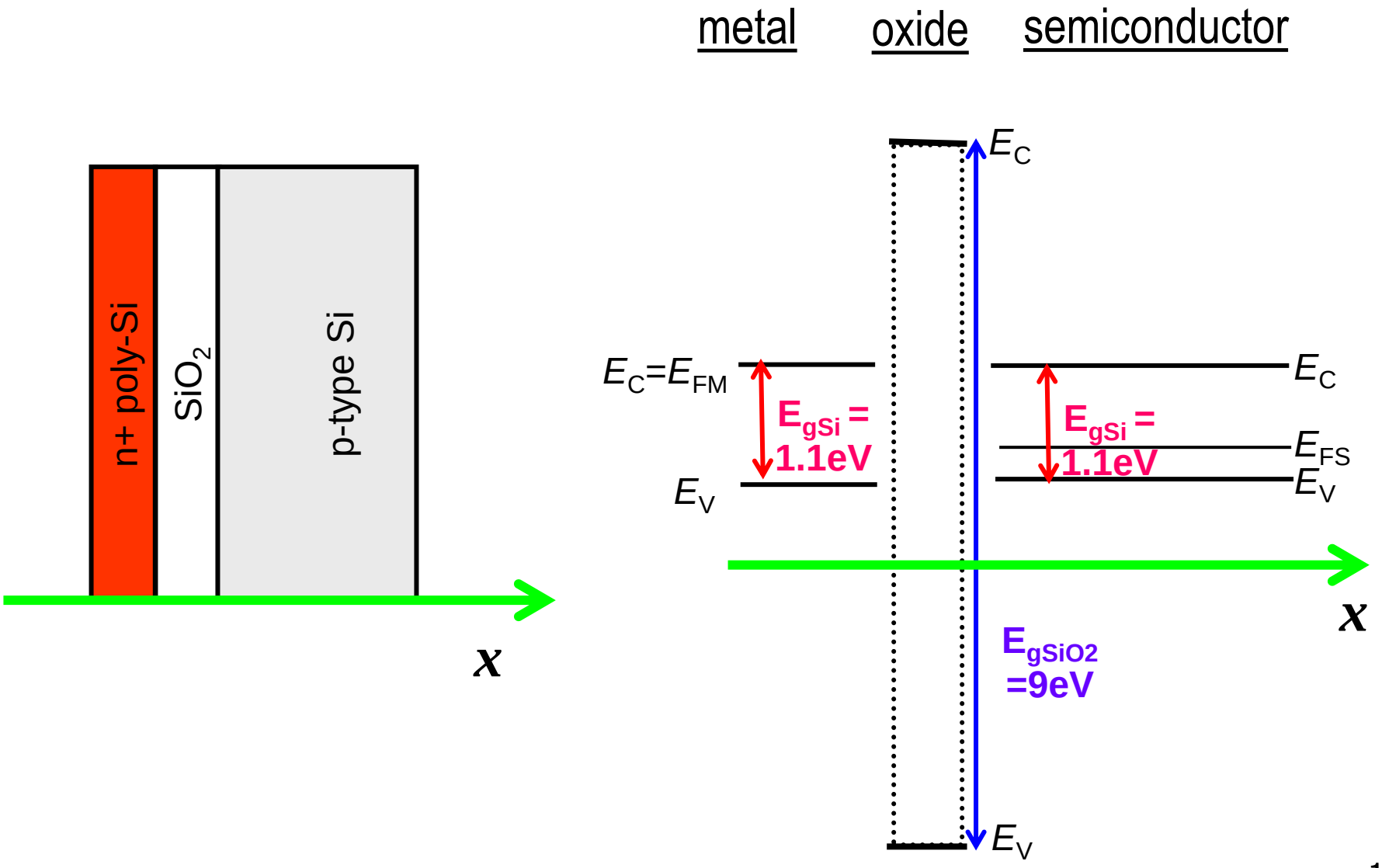
Poly-Si gate



resistivity: heavily doped Si $< 10^{-3}\ \Omega$-cm

metal: $3\ \mu\Omega$-cm

Coordinate system



Guidelines for Drawing MOS Band Diagrams

E_0: vacuum energy level

χ_{SiO2}=0.95eV

E_C

χ_{Si}= 4.05eV

$\Phi_S=\chi_{Si}+(E_C-E_{FS})$

Φ_M

3.1eV
Electron barrier

$E_C=E_{FM}$

E_C

E_{FS}

E_V

E_V

4.8eV
Hole barrier

E_0-E_F : **work function**

E_0-E_C : **electron affinity**

E_V

$qV_{FB} = \Phi_M - \Phi_S$

Guidelines for Drawing MOS Band Diagrams

1) Fermi level E_F is flat (constant with distance x) in the Si

- Since no current flows in the x direction, we can assume that equilibrium conditions prevail

2) Band bending is linear in the oxide

- No charge in the oxide => $d\mathcal{E}/dx = \rho/\varepsilon_{ox} = 0$, so $\mathcal{E}$ **is constant**
  => dE_C/dx is **constant**

$$\mathcal{E} = -dV/dx$$
$$E_C = -qV$$

$$\mathcal{E} = \frac{1}{q}\frac{dE_C}{dx}$$

Guidelines for Drawing MOS Band Diagrams

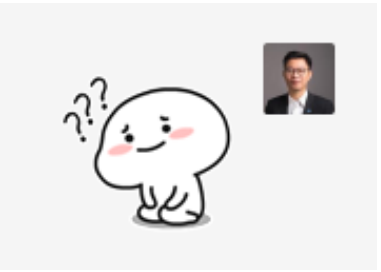
3) The **barrier height** for **conduction-band** electron flow from the **Si** into **SiO_2** is **3.1 eV**

- This is equal to the electron-affinity difference (χ_{Si} and χ_{SiO2})

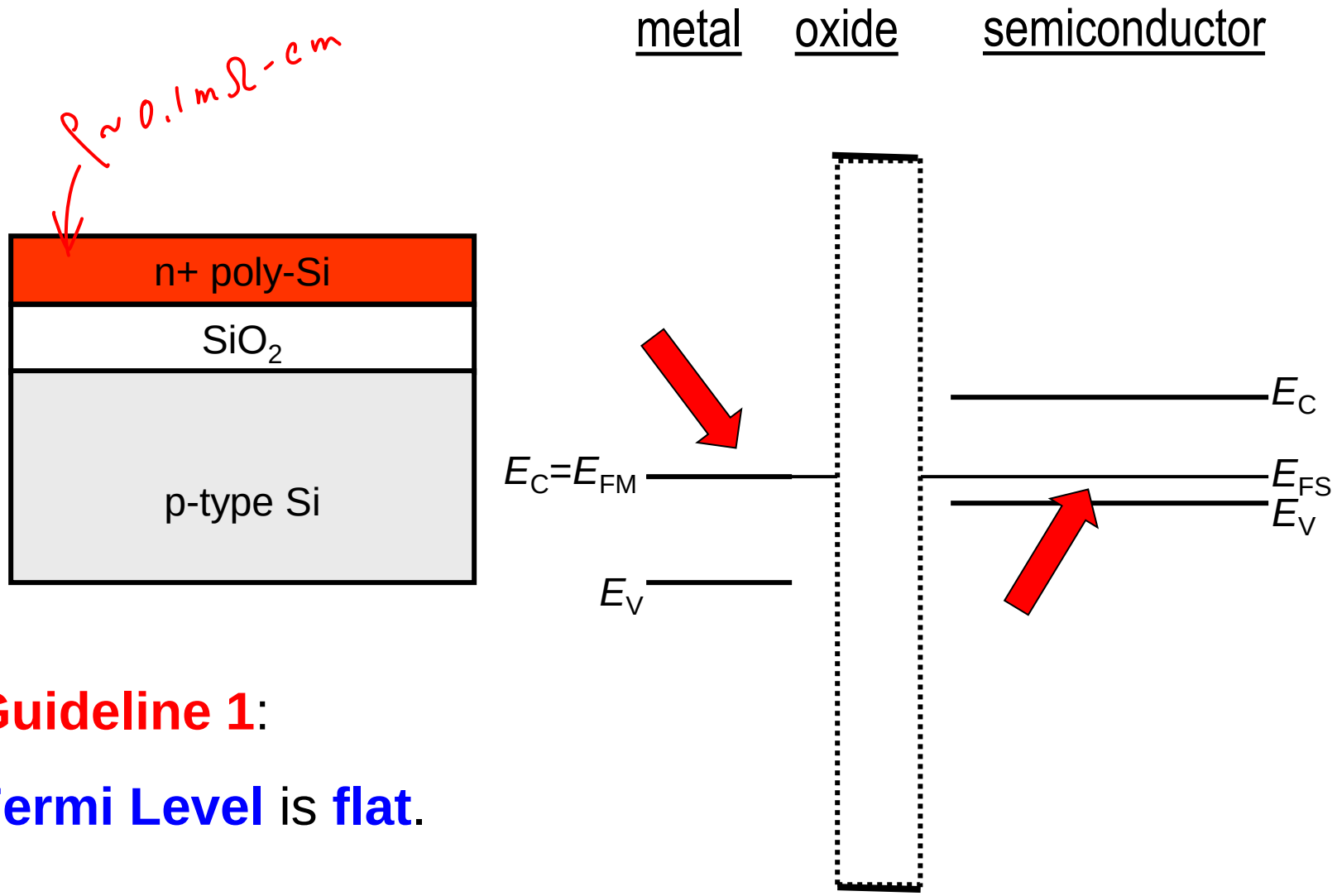
4) The **barrier height** for **valence-band** hole flow from the **Si** into **SiO_2** is **4.8 eV**

5) The **vertical distance** between the **Fermi level** in the **metal, E_{FM}**, and the **Fermi level** in the **Si, E_{FS}**, is equal to the **applied gate voltage**:

$$qV_G = E_{FS} - E_{FM}$$



MOS Equilibrium Energy-Band Diagram

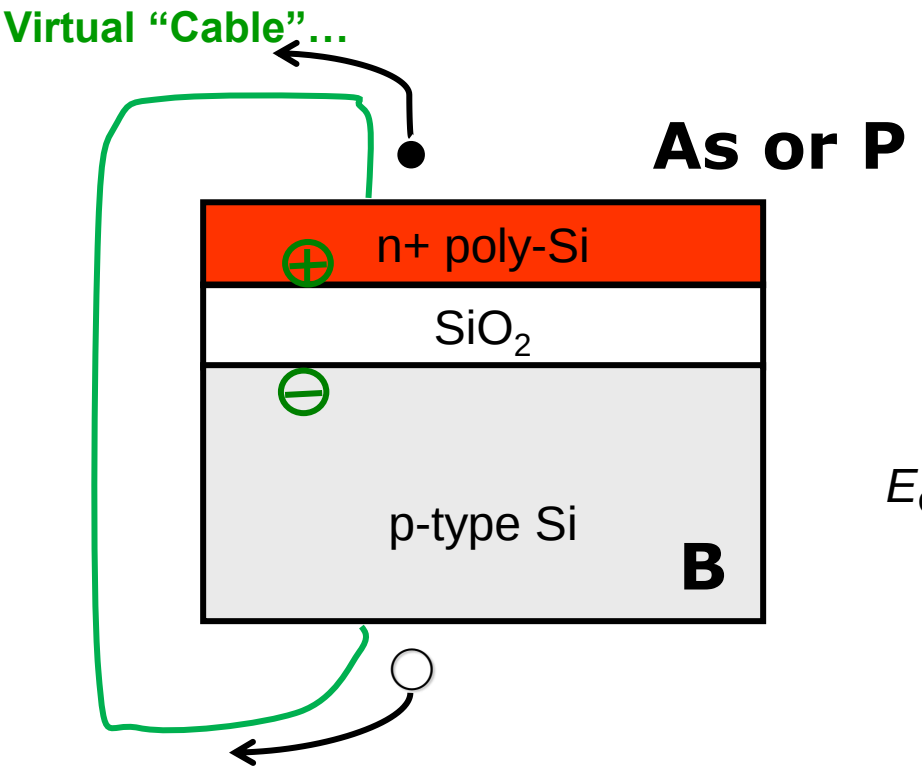


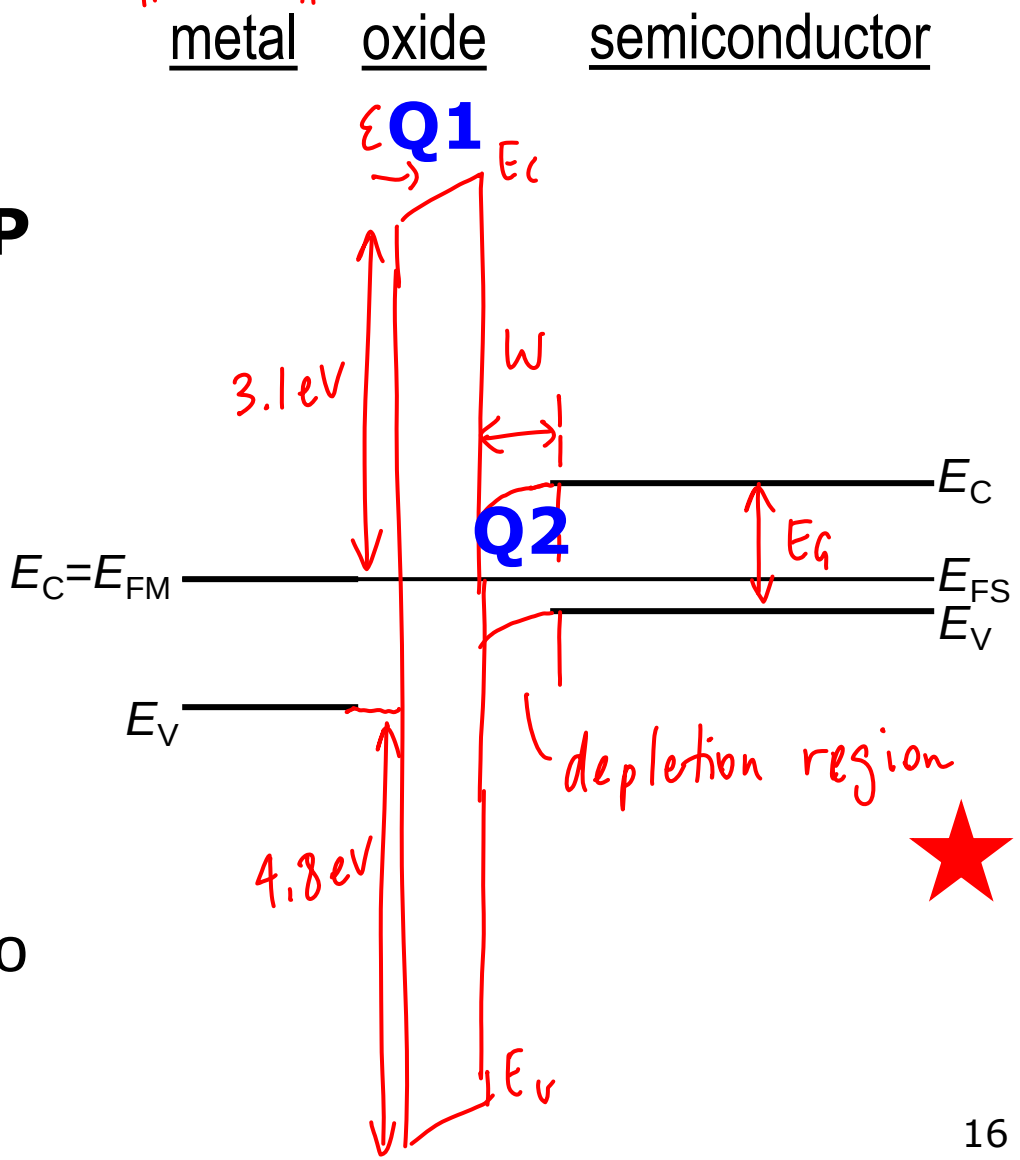
Guideline 1:

Fermi Level is **flat**.

MOS Equilibrium Energy-Band Diagram

Fermi Level is flat.





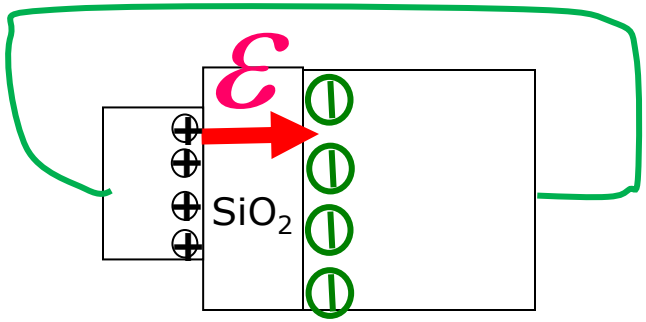
After **contact**, there are two questions: **Q1** & **Q2**.

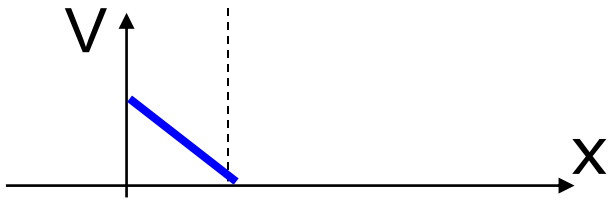
Q1: Carrier and ion in silicon

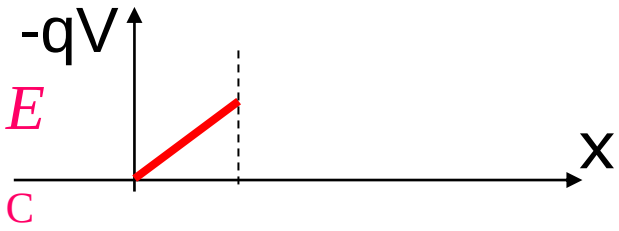
Guideline 2:

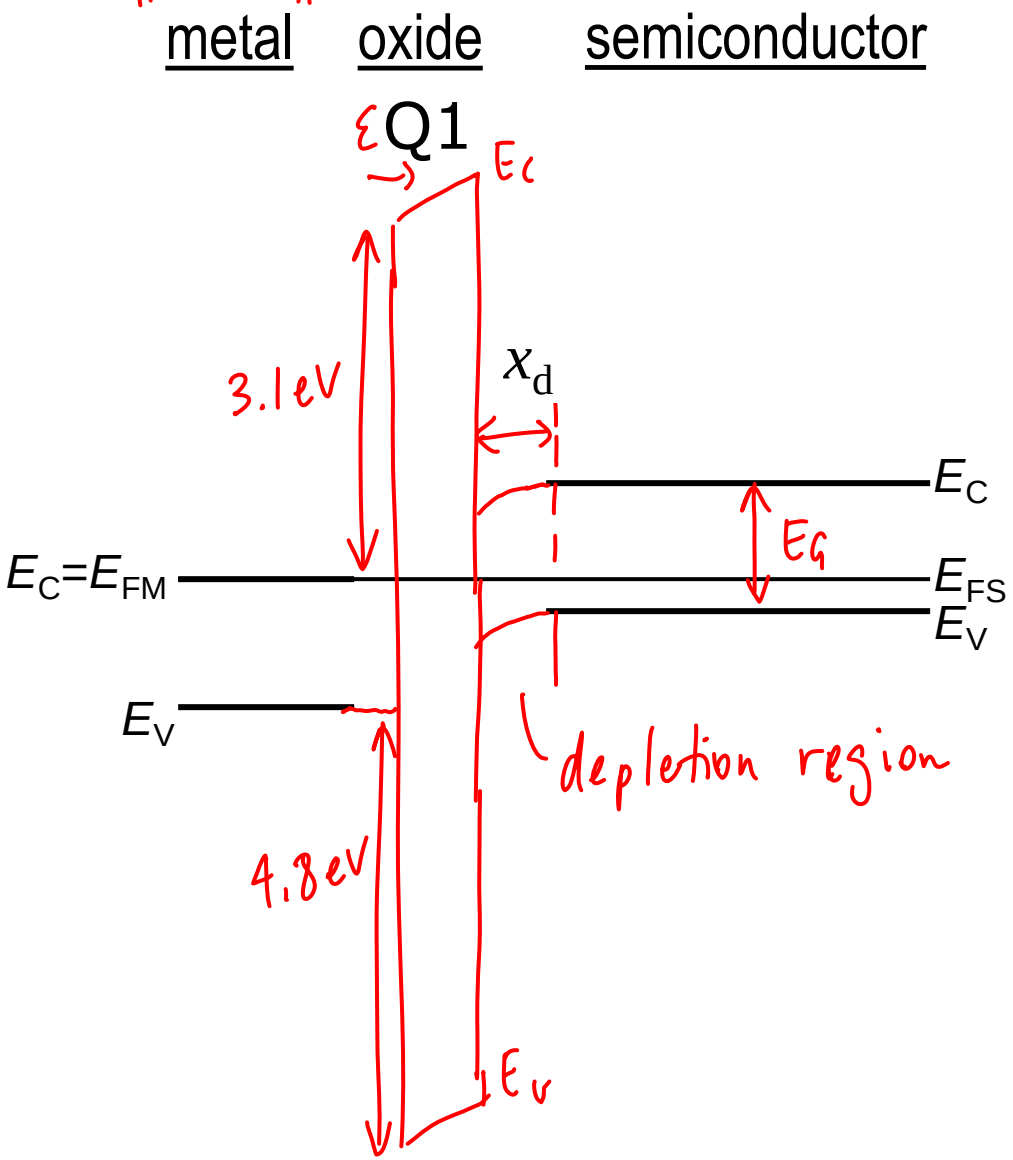
$\mathcal{E}=-dV/dx$

$E_C=-qV$

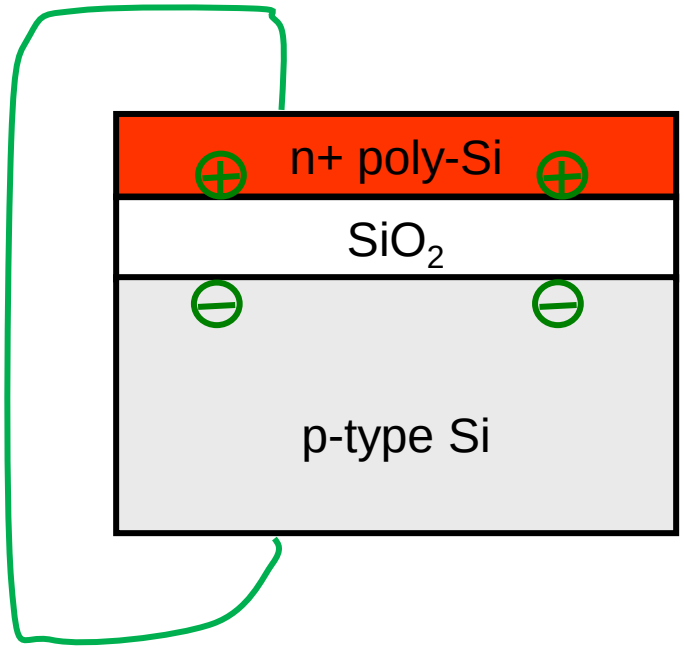


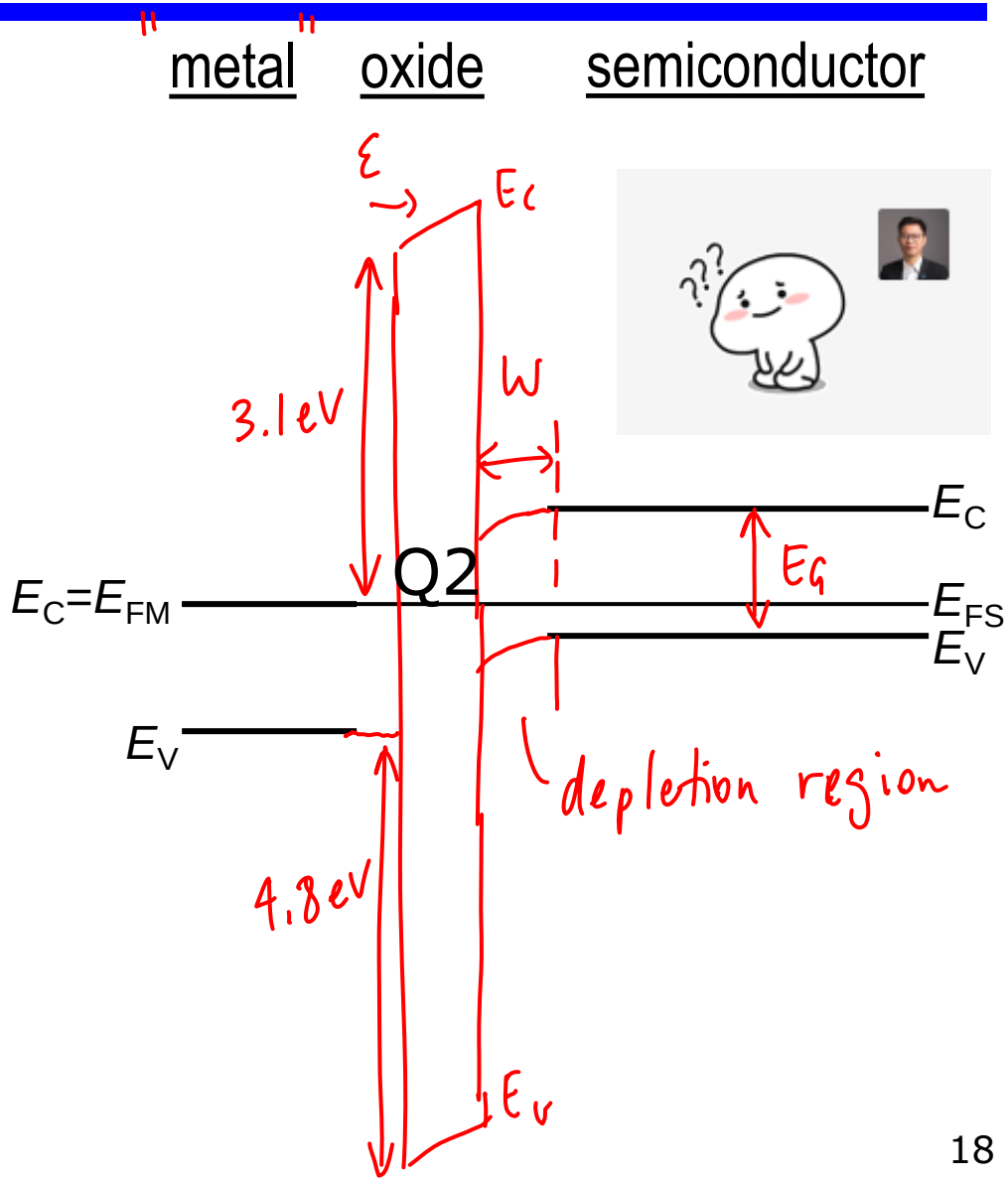




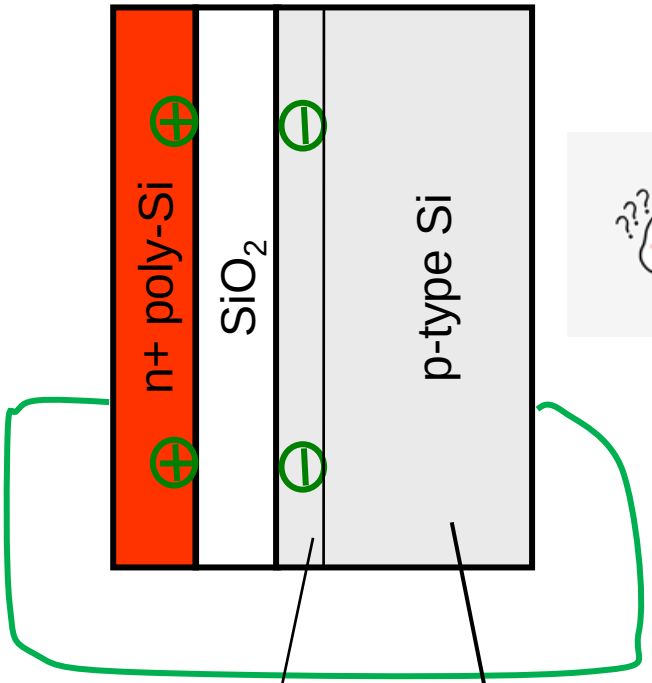


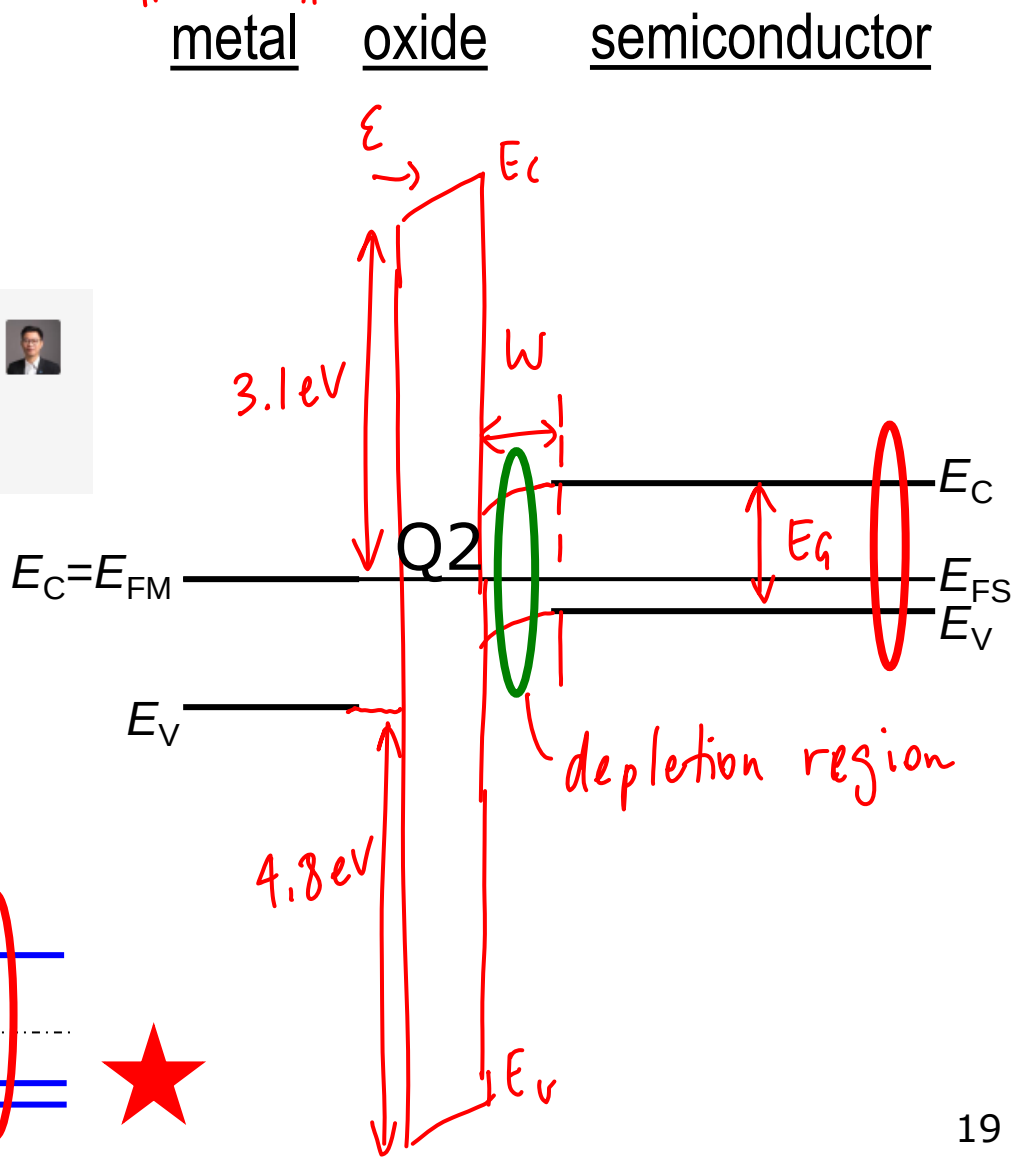
Q2: Carrier and ion in silicon

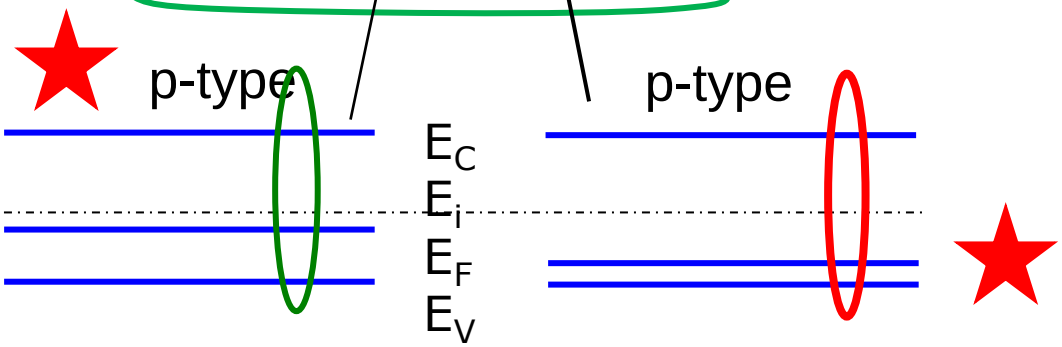




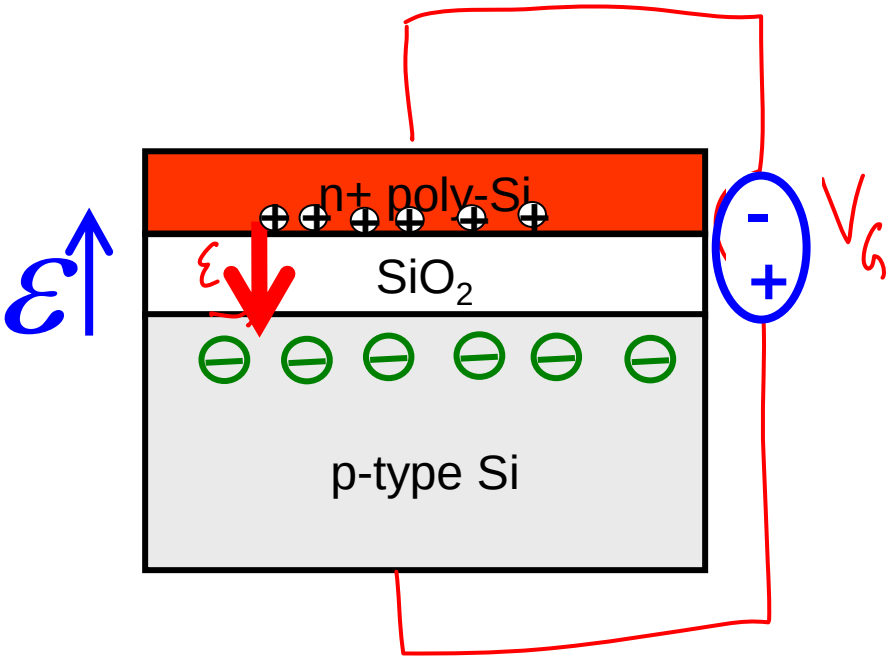
Q2: Carrier and ion in silicon

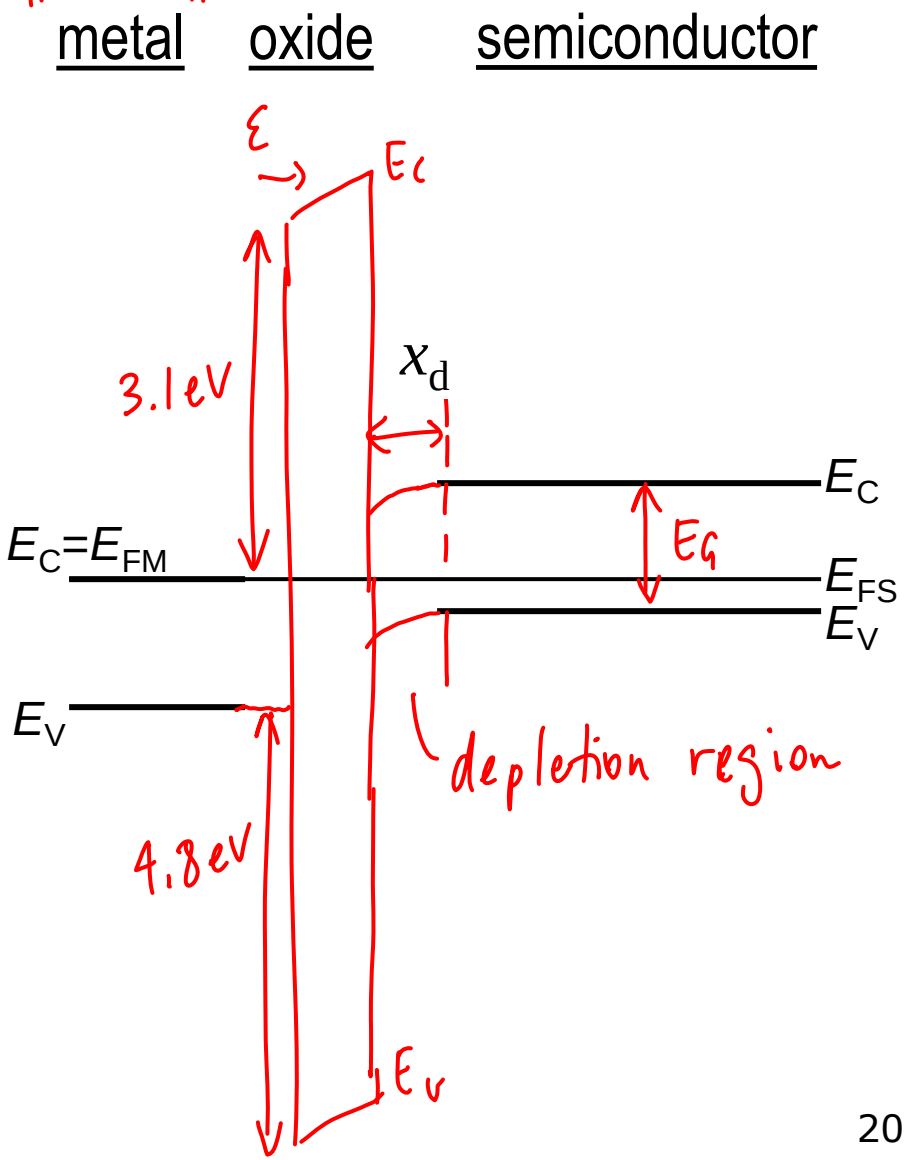




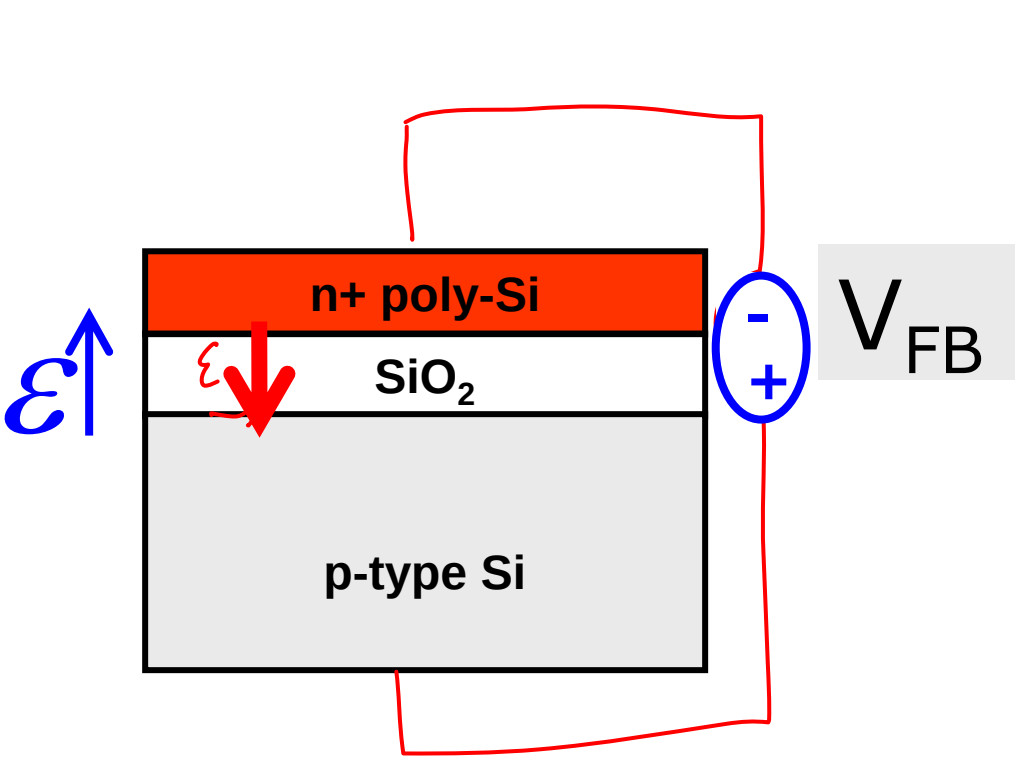


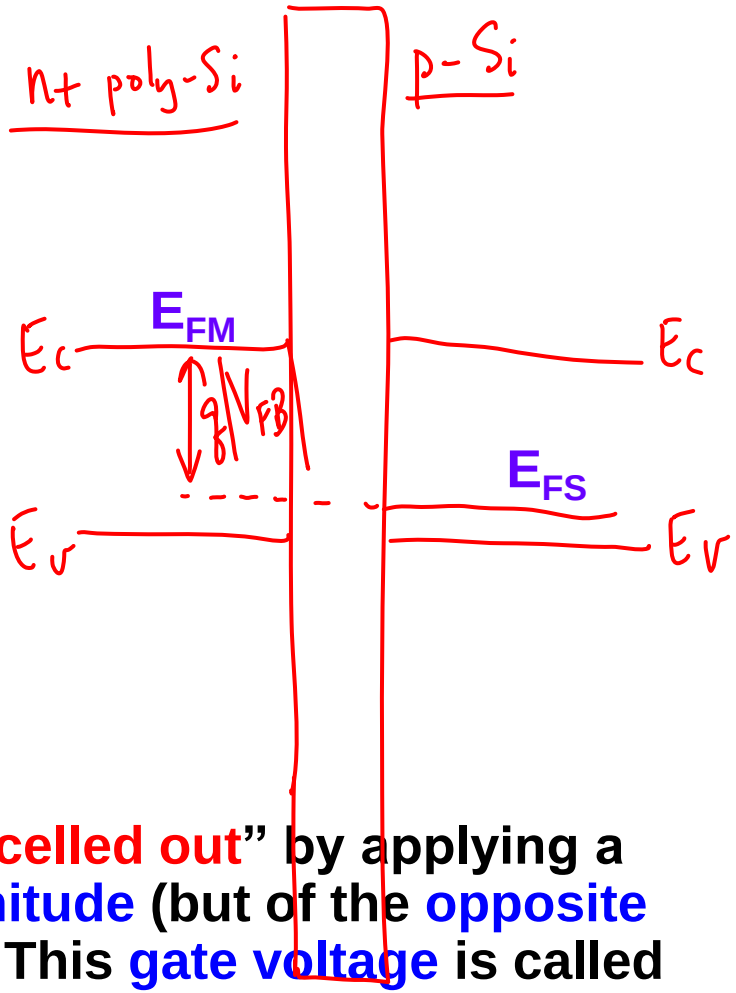
Flat-Band Voltage





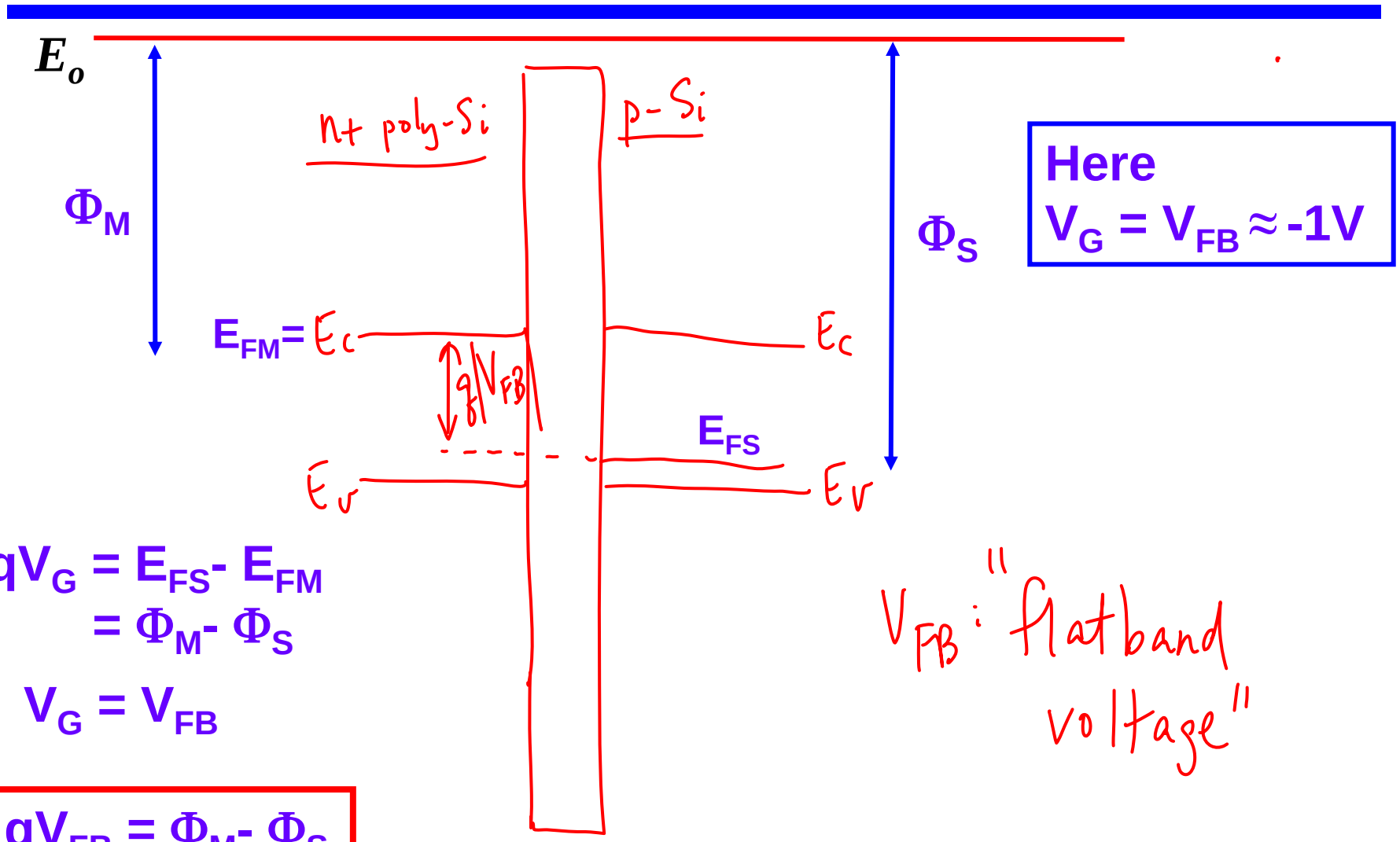
Flat-Band Voltage





- The **built-in potential** can be "**cancelled out**" by applying a **gate voltage** that is **equal in magnitude** (but of the **opposite polarity**) as the built-in potential. This **gate voltage** is called the ***flatband voltage*** because the **resulting potential profile is flat**.

Flat-Band Condition



Here
$V_G = V_{FB} \approx -1V$

$qV_G = E_{FS} - E_{FM}$
$= \Phi_M - \Phi_S$

$V_G = V_{FB}$

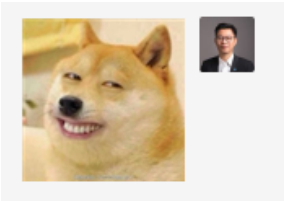
$qV_{FB} = \Phi_M - \Phi_S$

V_{FB}: "flatband voltage"

MOS Capacitance

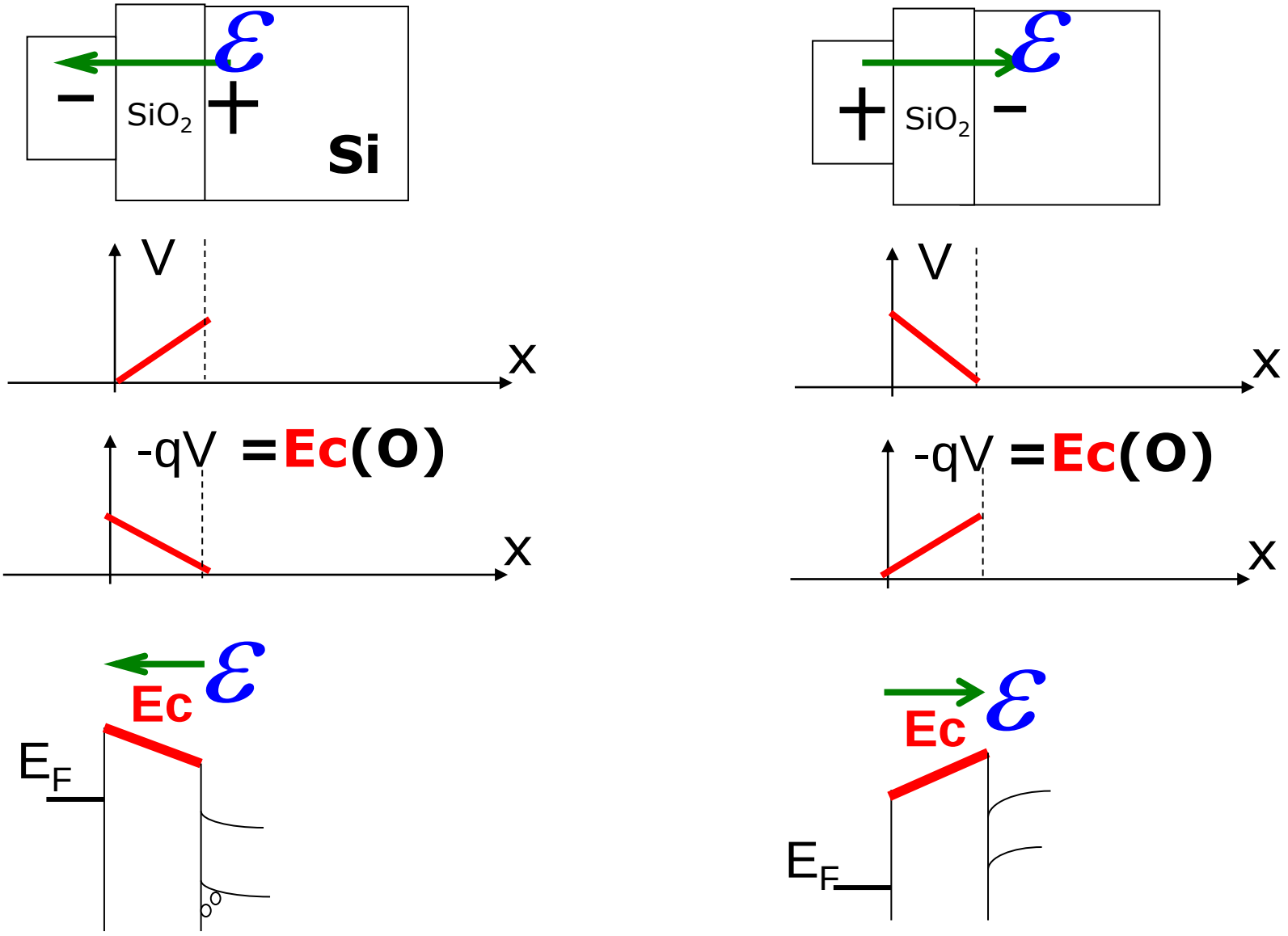
OUTLINE

- MOS structure
- MOS energy band diagram
- **Effects of applied biases**
- *Voltage drops

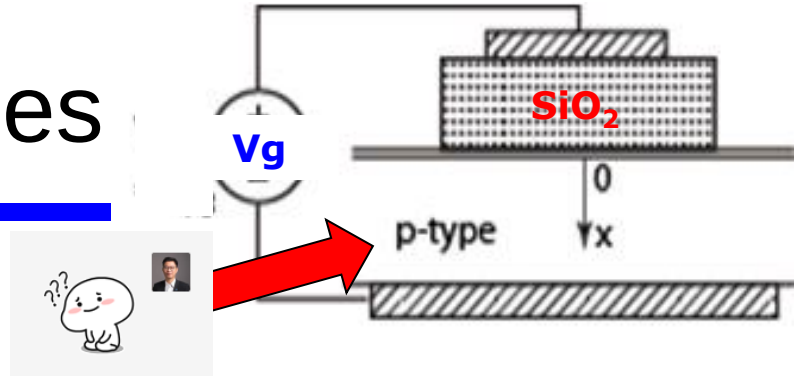


Reference reading: Chapter 6.0-6.4

Ec(O) and **electric field** direction



Effects of applied biases



Vg increase from "-" to "+" :

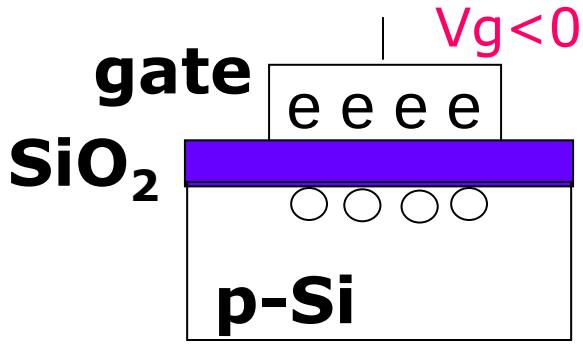
1. $Vg < V_{FB} < 0$	**Accumulation**: Majority carriers
2. $Vg = V_{FB}$	**Flatband**
3. $V_m \geq Vg > V_{FB}$ including Vg=0	**Depletion**: Majority carriers
4.1 $V_T > Vg > V_m$	**Weak Inversion**: Minority carriers
4.2 $Vg \geq V_T$	**Strong Inversion**: Minority carriers

??

What is V_{FB}, V_m and V_T?

1. **Accumulation** (**p-type** Si) : **Vg**<V_{FB}<0

Accumulation:
Majority carriers

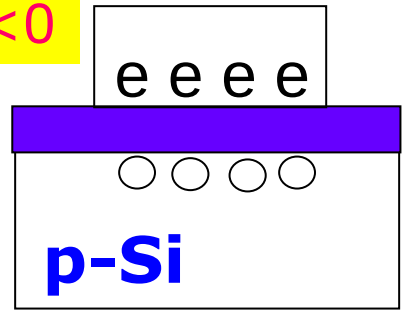


- Physical process: **Vg**<0: **holes** attracted to the **oxide/Si interface** and **accumulate** there.
- Oxide: **separation** between "**-**" and "**+**" charges

1. Accumulation:

Energy band & block charge density

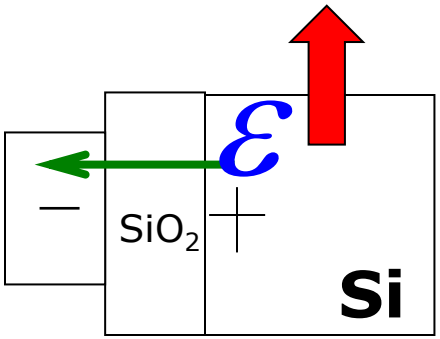
Vg<0

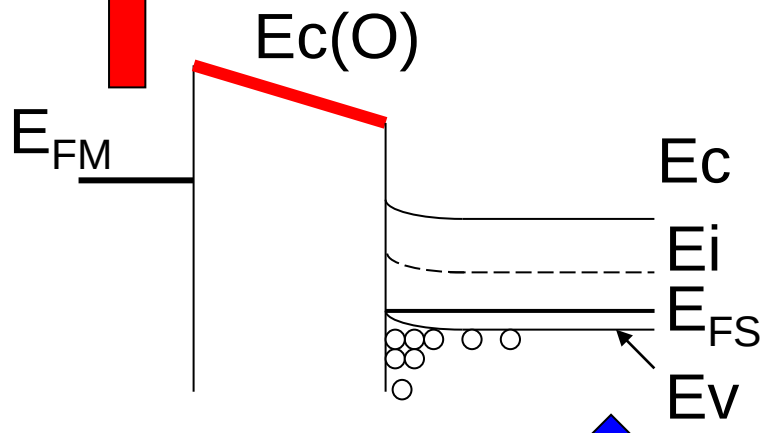


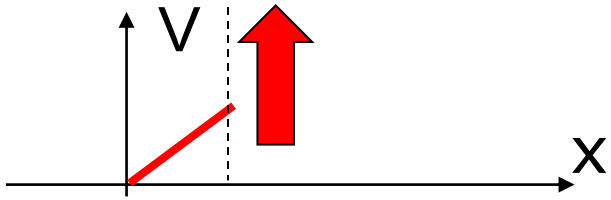
More negative: higher electron energy (band bending up)

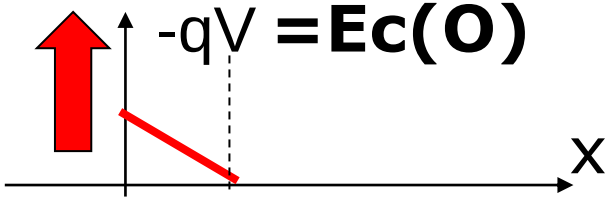
$\Delta Vg \rightarrow \Delta Q_{acc}$

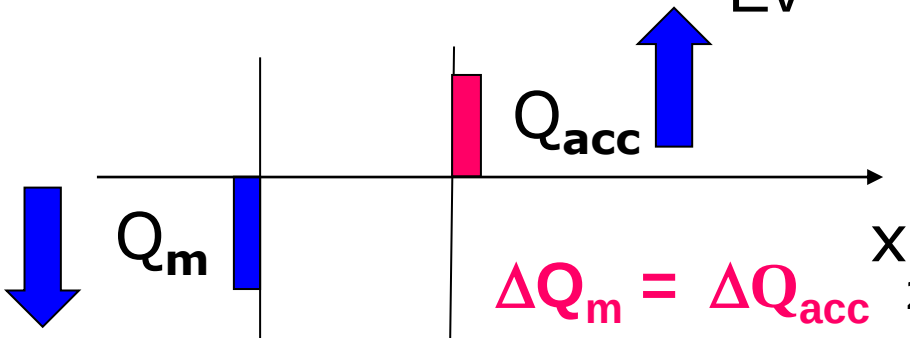
$qVg = E_{FS} - E_{FM}$







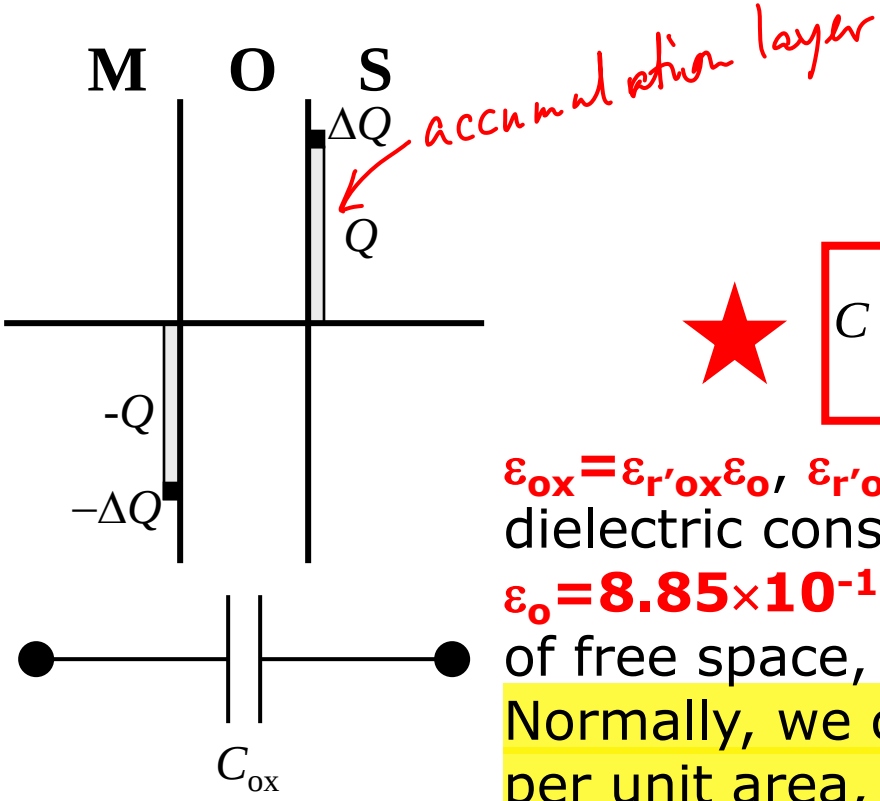




$\Delta Q_m = \Delta Q_{acc}$

1. **Capacitance** in **Accumulation**

- As the **gate voltage** is varied, **incremental charge** is added/subtracted to/from the gate and substrate.
- The **incremental charges** are separated by the **gate oxide**.



accumulation layer

$$C = \left|\frac{dQ_{acc}}{dV_g}\right| = C_{ox}$$

★

$$C = C_{ox} = \frac{\varepsilon_{ox} A}{t_{ox}} = \text{constant}$$

$\varepsilon_{ox} = \varepsilon_{r'ox}\varepsilon_o$, $\varepsilon_{r'ox} = 3.9$ is the relative dielectric constant of the oxide

$\varepsilon_o = 8.85 \times 10^{-12}$ **F/m** is the permittivity of free space, t_{ox} is the oxide thickness.

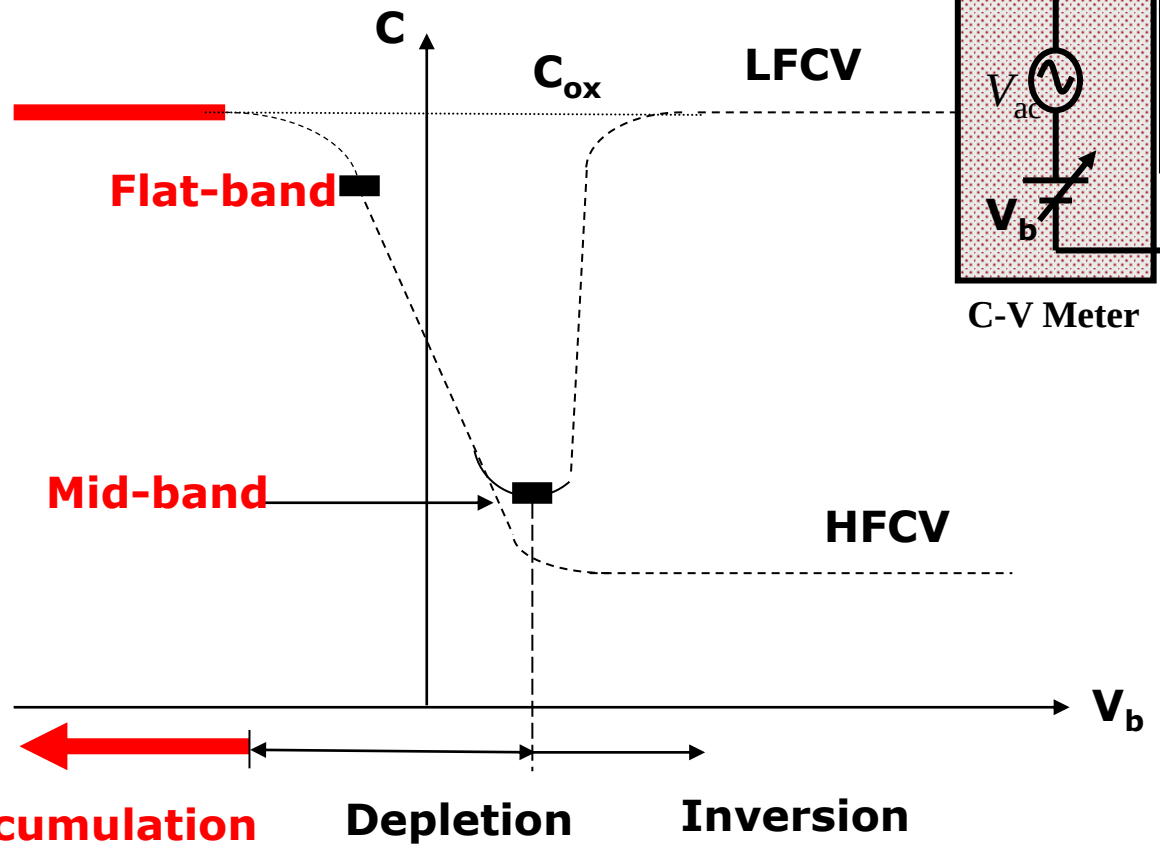
Normally, we consider the capacitance per unit area, so **A=1**.

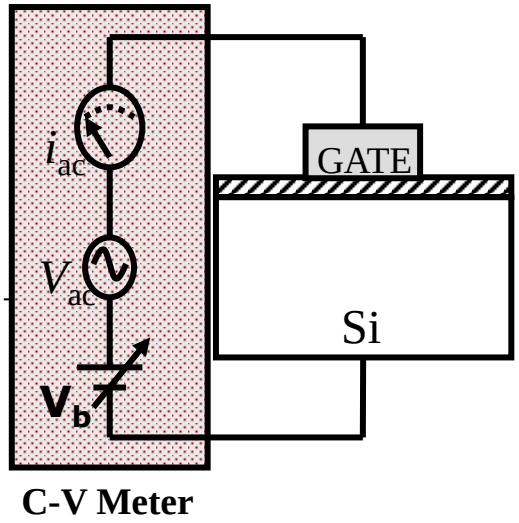
1. **Accumulation**:

Capacitance-voltage (C-V) characteristics

- Example: **p-Si**

$$C = C_{ox} = \frac{\varepsilon_{ox} A}{t_{ox}}$$

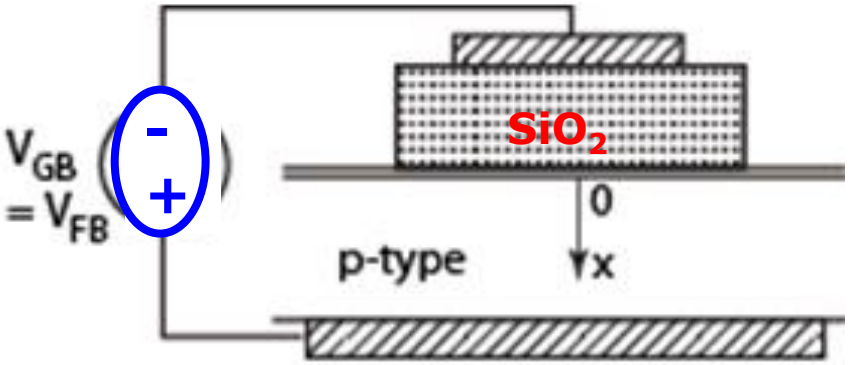


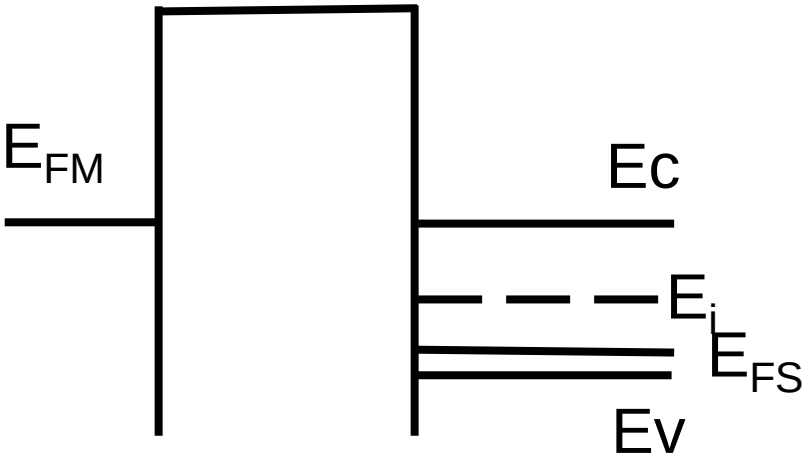


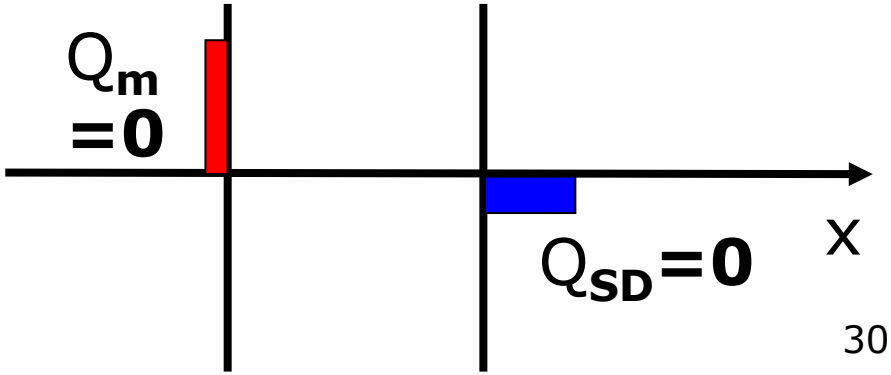
2. Flatband Voltage, V_{FB}

- The **built-in potential** can be "**cancelled out**" by applying a **gate voltage** that is **equal in magnitude** (but of the **opposite polarity**) as the built-in potential. This **gate voltage** is called the ***flatband voltage*** because the **resulting potential profile is flat**.

$Vg=V_{FB}$







There is no **net charge** (*i.e.* $\rho(x)=0$) in the semiconductor under $V_{GB} = V_{FB}$.

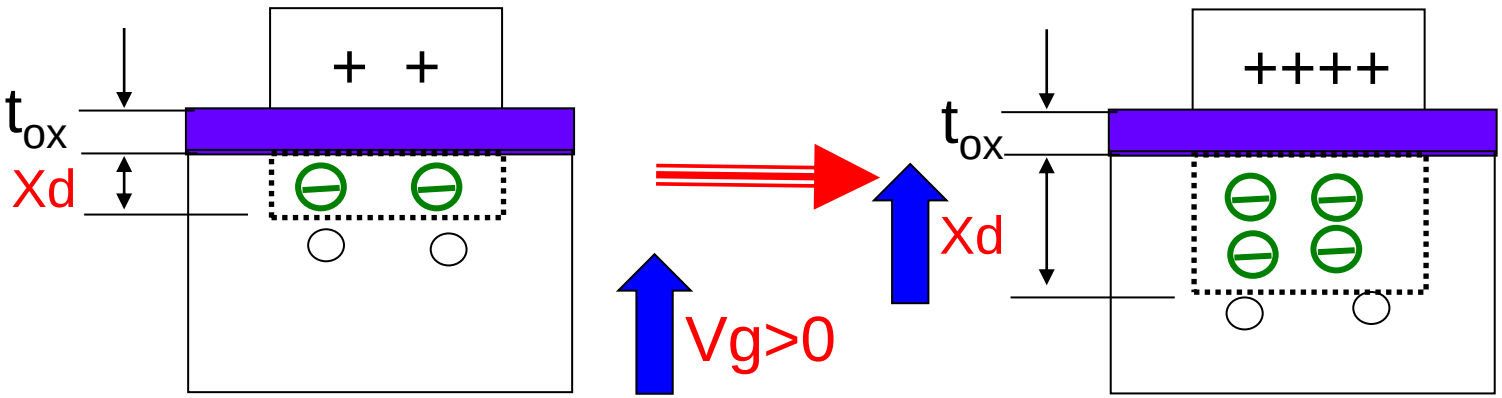
3. **Depletion**: Vg > V_{FB}

Depletion: Majority carriers

- Physical process:
  - **holes** repelled from the **interface**
  - **fixed negative charge** left behind
  - More "**+**" charges on the gate, **holes** are pushed further from the **interface**, to expose more "**-**" space charges.

○: Hole

⊖ : **B^-**

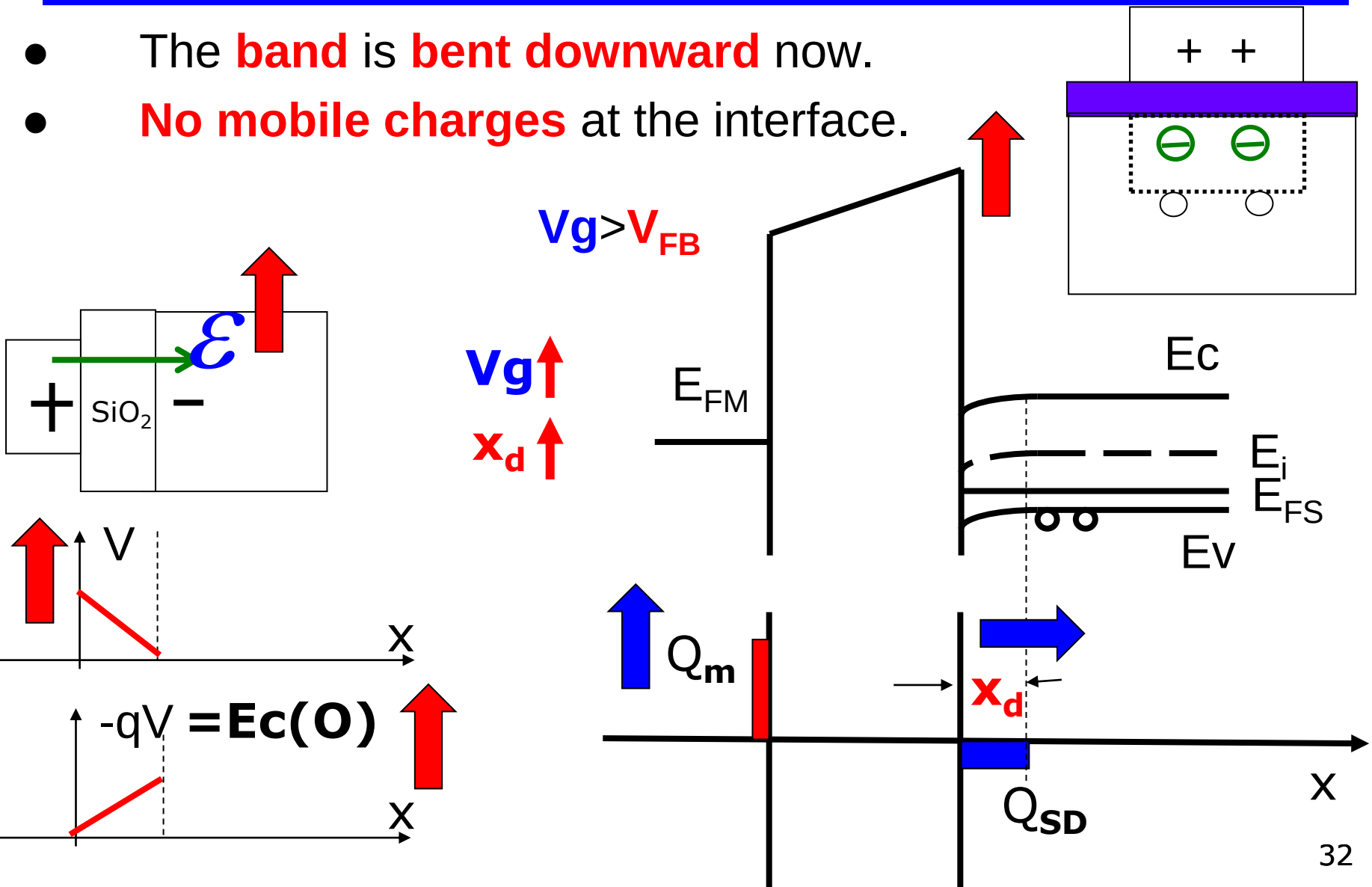


3. Depletion:

Energy band diagram: $V_g > V_{FB}$

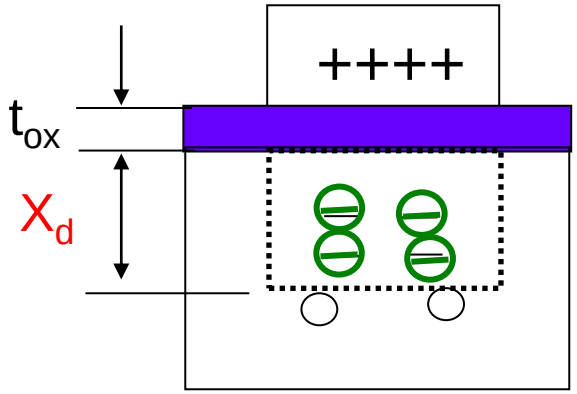
$qV_g = E_{FS} - E_{FM}$

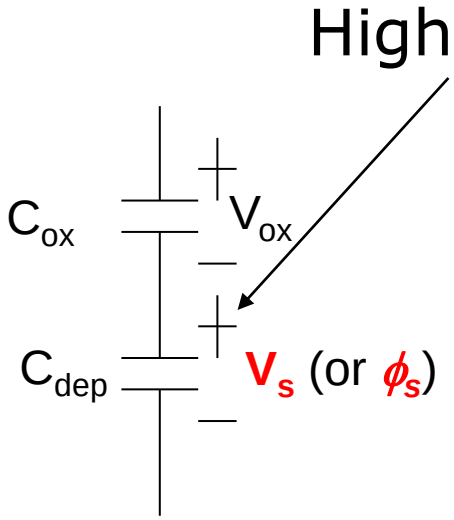
- The band is bent downward now.
- No mobile charges at the interface.



3. Depletion Capacitor

- **Capacitance**





$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

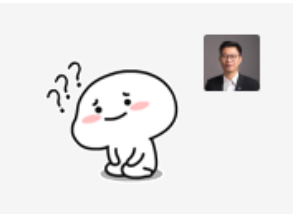
$$C_{dep} = \frac{\varepsilon_{Si}}{x_d}$$

- When **Vg** increases, **Xd** increases and **C_{dep}** reduces. This in turn reduces **C**.
- Solving Poisson's equation, we have

$$x_d = \left(\frac{2\varepsilon_{Si} V_S}{qN_a} \right)^{1/2}$$

$$C_{dep} = \frac{\varepsilon_{Si}}{x_d}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

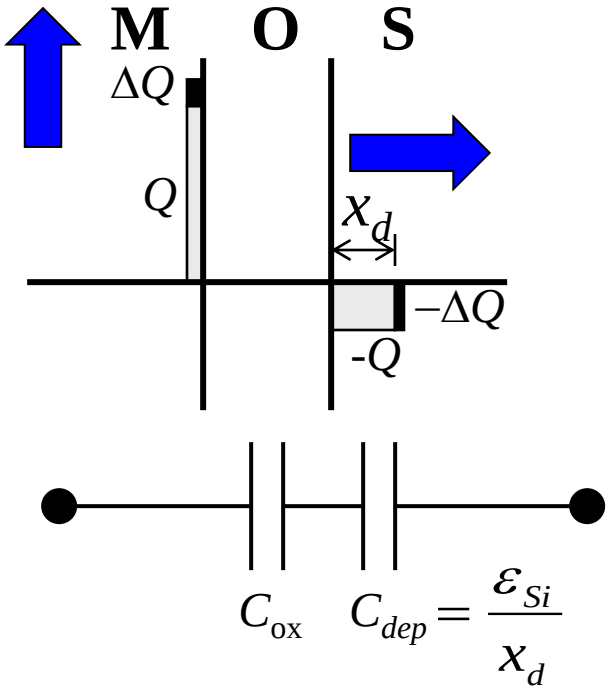


C ??

3. **Capacitance in Depletion**

- As the **gate voltage** is varied, the **width of the depletion** region varies.

Incremental charge is effectively added/subtracted at a **depth x_d** in the substrate.



$$C = \left| \frac{dQ}{dV_G} \right|$$

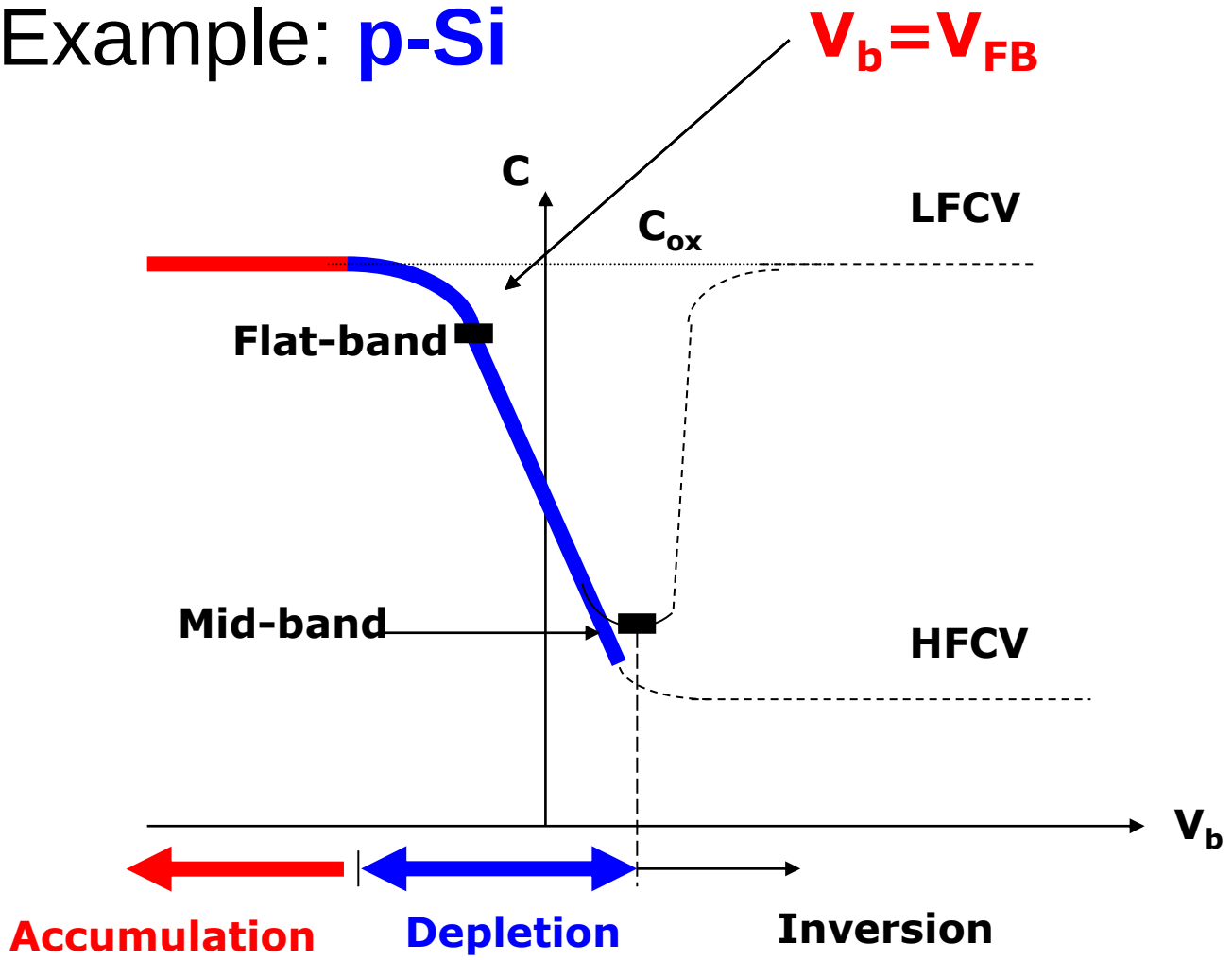
$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}} = \frac{1}{C_{ox}} + \frac{x_d}{\varepsilon_{Si}}$$

$\varepsilon_{Si} = \varepsilon_{r'Si}\varepsilon_o$, $\varepsilon_{r'Si} = 11.9$ is the **relative dielectric constant** of silicon,.

3. **Depletion**:

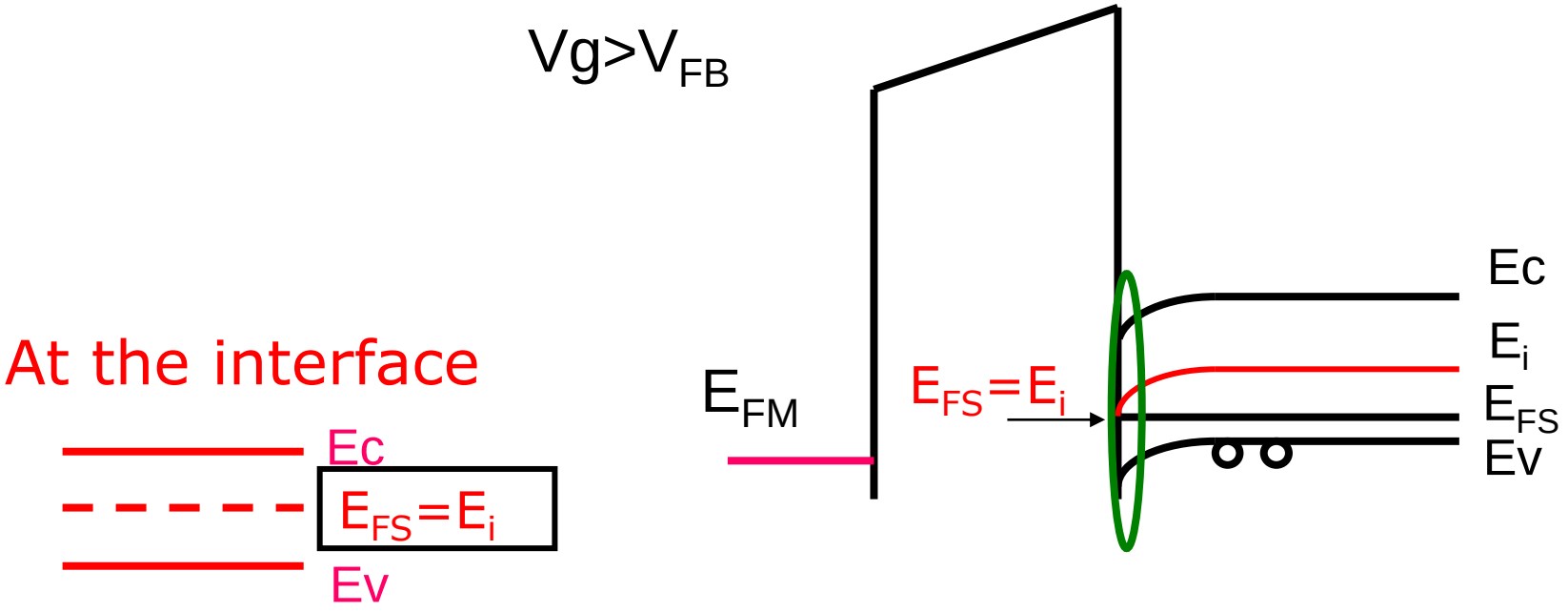
Capacitance-voltage (C-V) characteristics

- Example: **p-Si**



Midband: further increase **Vg**

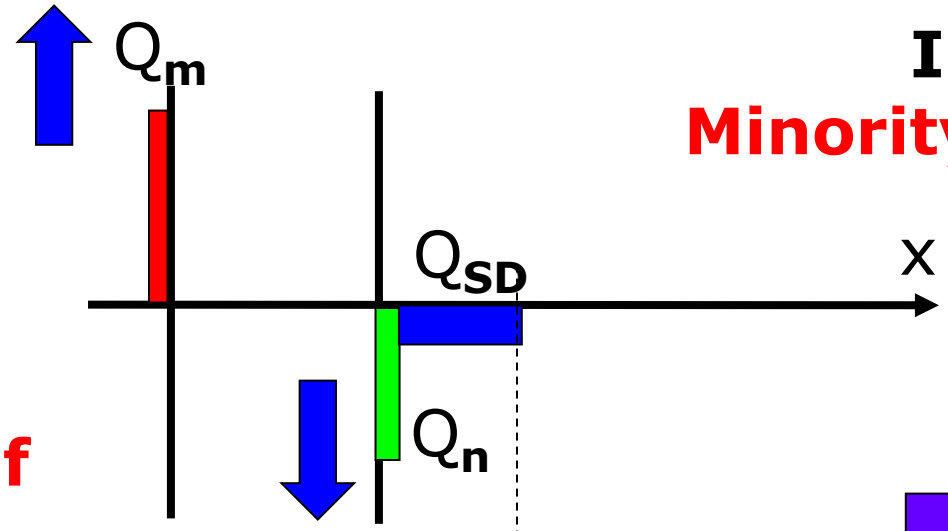
- E_{FS} **= Ei** = **(Ec+Ev)/2** at **interface**
- **Silicon** becomes **"intrinsic"** at **surface**
- This is '**Midband**': **Vg**=**Vm**



$qV_g = E_{FS} - E_{FM}$

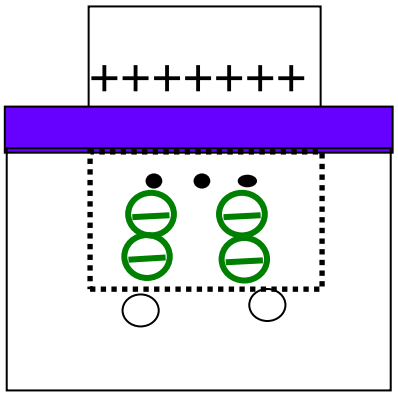
4. Energy band diagram: $V_g > V_m$

Vg ↑

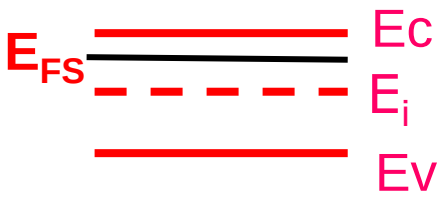


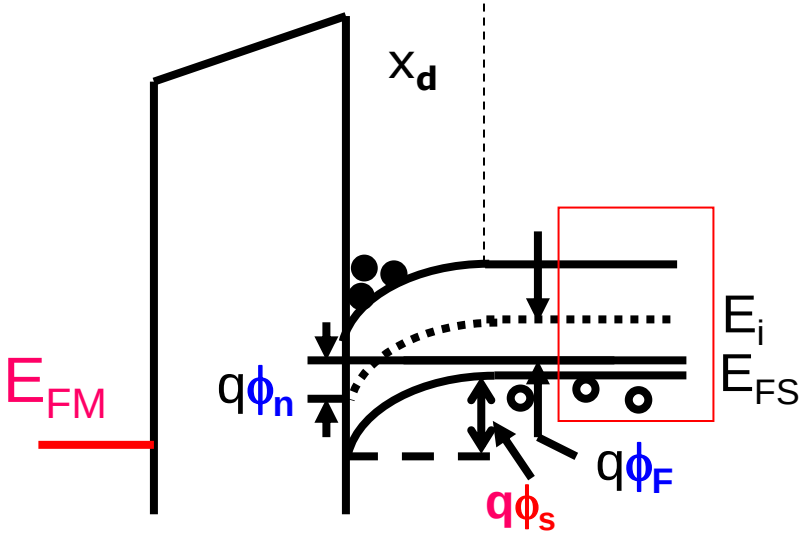
Inversion:
Minority carriers

As **Vg**>**Vm**, E_{FS} is at the **up-half** of the bandgap



At the interface



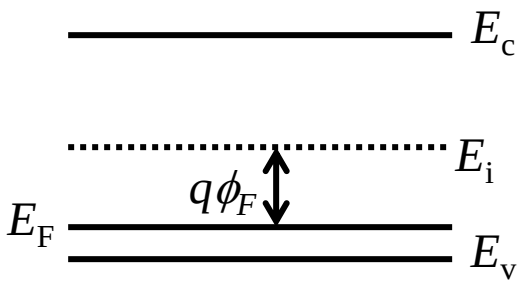


Bulk Semiconductor Potential, ϕ_F

$$q\phi_F \equiv E_i - E_F$$

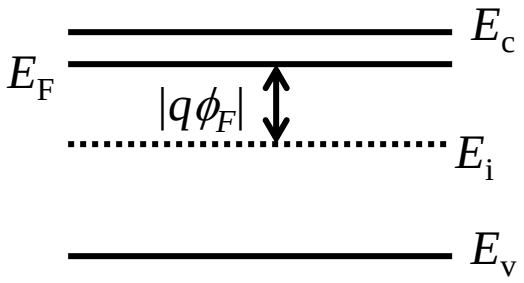
- **p-type** Si:

$$\phi_F = \frac{kT}{q}\ln(N_A / n_i) > 0$$



- **n-type** Si:

$$\phi_F = -\frac{kT}{q}\ln(N_D / n_i) < 0$$



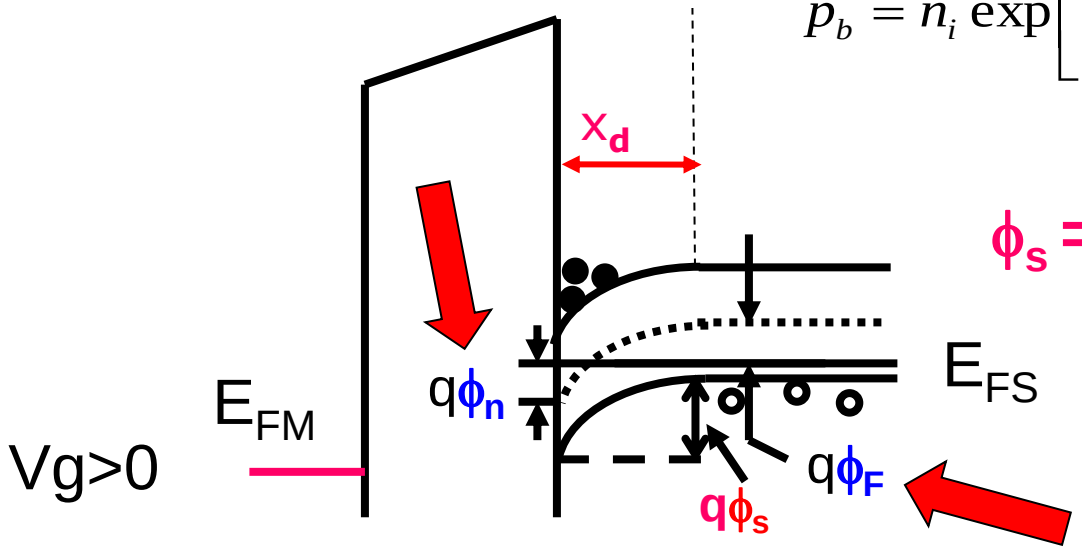
4. **Inversion**: large positive ($Vg-V_{FB}$)

- **Weak Inversion**: $0<\phi_n<\phi_F$ ($\phi_F < \phi_S < 2\phi_F$) $\phi_s = \phi_F + \phi_n$
- **Strong Inversion:** $\phi_n \geq \phi_F$ ($\phi_S \geq 2\phi_F$), **electron density** at the **interface** ≥ **hole density** in **Si bulk**.
- **Vg** for **strong inversion**: V_T '**threshold voltage**'.

$Vg = V_T \rightarrow \phi_s = 2\phi_F \quad \rightarrow n_s = p_b$

$$n_s = n_i \exp\left[\frac{(E_F - E_{i,surf})}{kT}\right]$$

$$p_b = n_i \exp\left[\frac{-(E_F - E_{i,bulk})}{kT}\right]$$



$\phi_s = \phi_F + \phi_n$

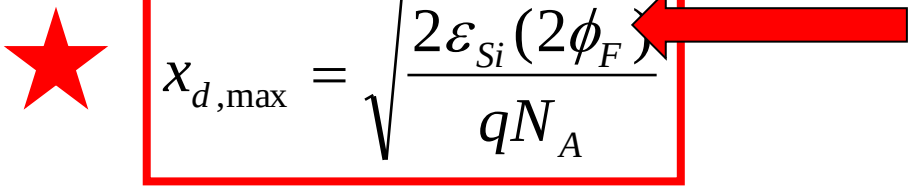
Maximum Depletion Depth, $x_{d,max}$

- As V_G is increased above V_T, ϕ_S and hence the **depth of the depletion region** (x_d) increases very slowly.

$$\phi_s \approx 2\phi_F$$

  - *This is because n increases exponentially with ϕ_S, whereas x_d increases with the square root of ϕ_S. Thus, most of the incremental negative charge in the semiconductor comes from additional conduction electrons rather than additional ionized acceptor atoms, when n exceeds N_A.*

→ x_d can be reasonably approximated to reach a **maximum value** ($x_{d,max}$) for $V_G \geq V_T$.

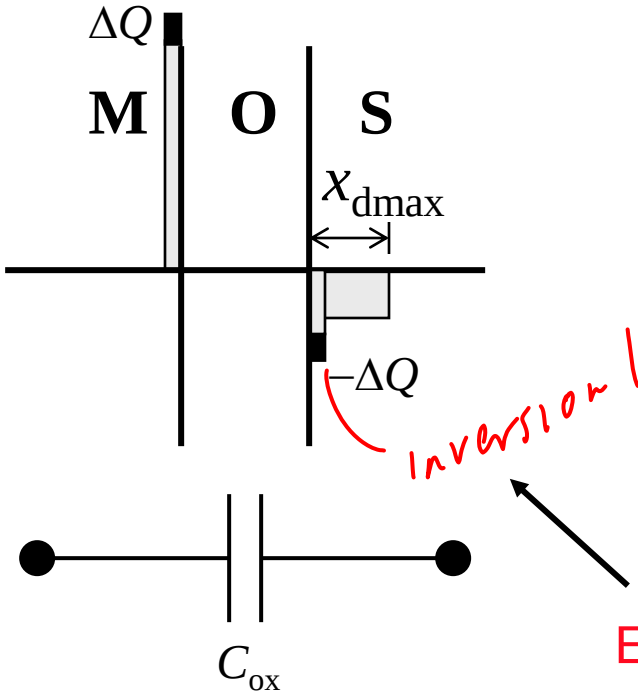


$$x_{d,\max} = \sqrt{\frac{2\varepsilon_{Si}(2\phi_F)}{qN_A}}$$

4. Capacitance in Inversion: Low Frequency

CASE 1: Inversion-layer charge *can* be supplied/removed quickly enough to respond to **changes** in the **gate voltage**.

→ **Incremental charge** is effectively added/subtracted at the **surface of the substrate**.



Time required to **build inversion-layer charge** = $2N_A\tau_o/n_i$, where
τ_o = **minority-carrier lifetime at surface**

inversion layer charge (electrons

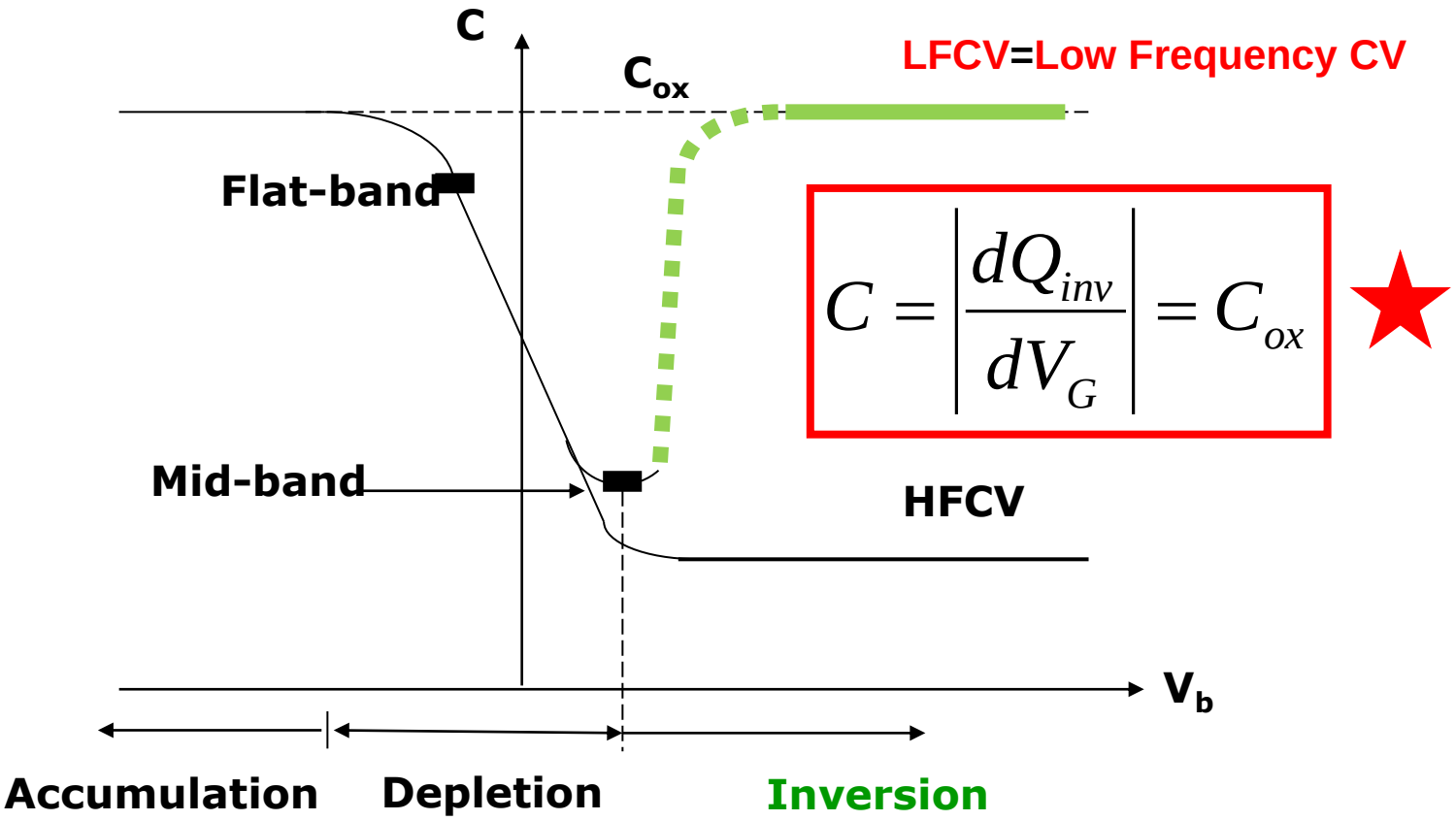
$$C = \left|\frac{dQ_{inv}}{dV_G}\right| = C_{ox}$$

Electrons can respond to the change in Vac

4. Inversion:

CASE 1: Capacitance-voltage (C-V) characteristics

- Example: **p-Si**



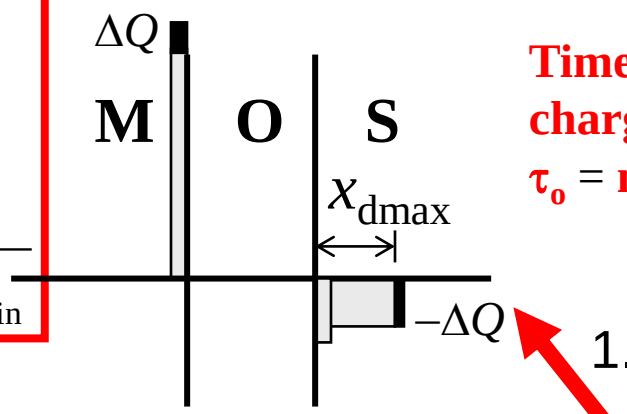
4. Capacitance in Inversion: High Frequency

CASE 2: Inversion-layer charge *cannot* be supplied/removed quickly enough to respond to **changes** in the **gate voltage**.

→ **Incremental charge** is effectively added/subtracted at **a depth x_{dmax} in the substrate**.

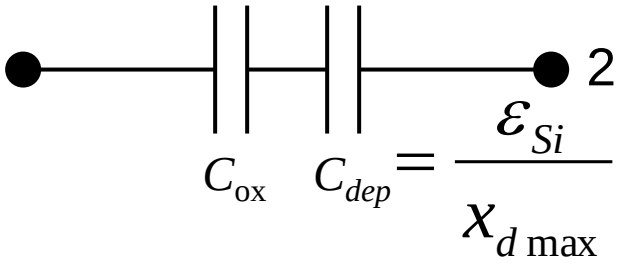
$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}}$$

$$= \frac{1}{C_{ox}} + \frac{x_{d\,\max}}{\varepsilon_{Si}} \equiv \frac{1}{C_{\min}}$$



Time required to **build inversion-layer charge** = $2N_A\tau_o/n_i$, where
τ_o = **minority-carrier lifetime at surface**

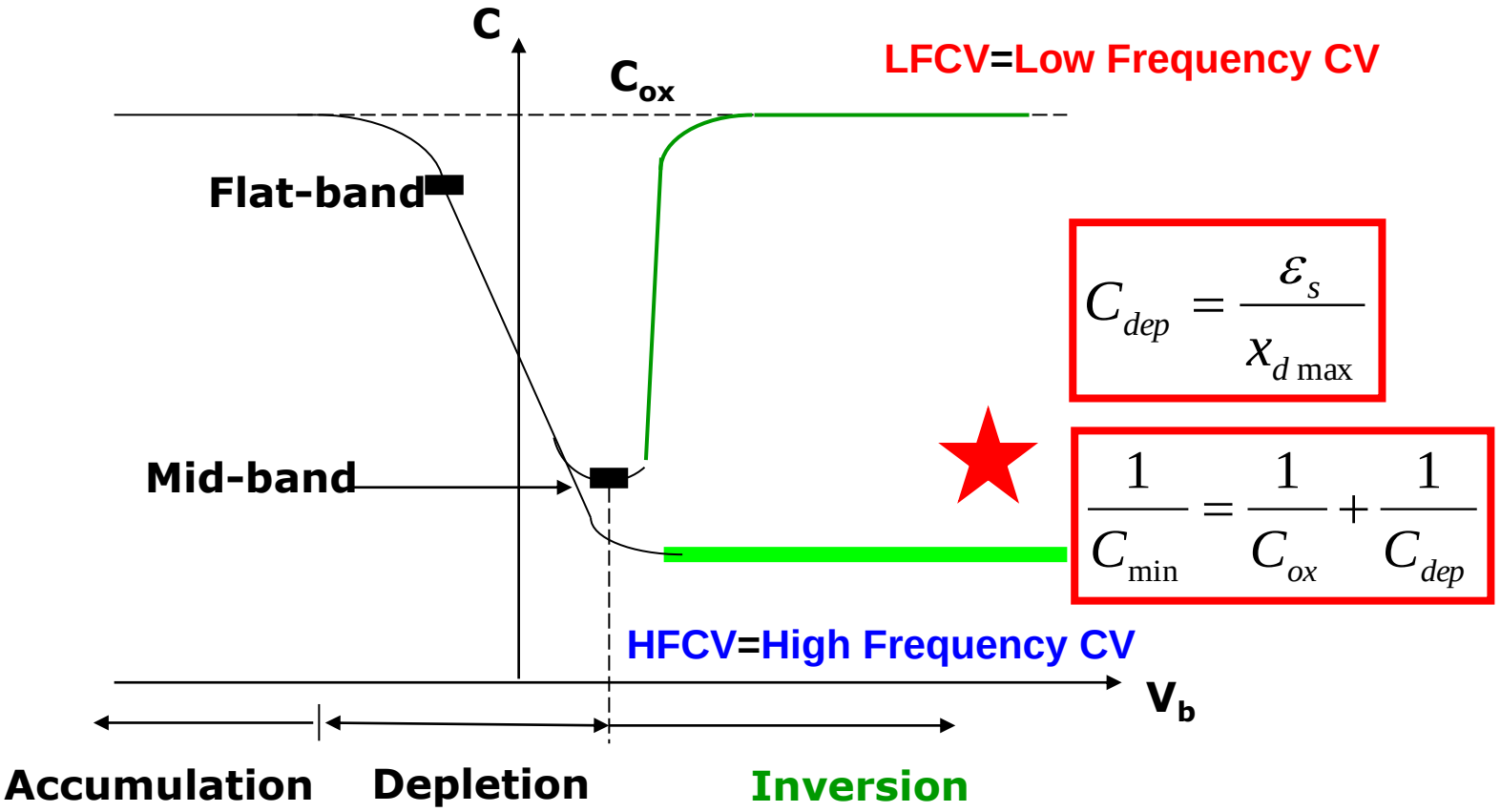
1. When **Vac** changes rapidly (e.g., **1MHz**), **electron** creation **cannot** keep up.
2. **Negative charges** supplied by **pushing holes away**.



4. Inversion

CASE 2: Capacitance-voltage (C-V) characteristics

- Example: p-Si



HW8

- A MOS capacitor has:

  Xox=40nm, **Nd=$10^{21}m^{-3}$**, **ϕ_F=0.3V**, **ε_{ox}=3.9**, **ε_s=11.8**

- Determine:

  (i) **C(HF)** in **accumulation**; (ii) **C(HF)** in **strong inversion**

  (iii) **C(LF)** in **strong inversion**

- Solution:

HW9

- An **MOS capacitor** is made on uniformly doped **p type material**. With **-20V** on the gate with respect to the substrate it has a capacitance of **20pF**. With **+20V** on the gate it has a capacitance of **10pF**. What is the **thickness** of the **depletion layer** if the **capacitor** has an area of $10^{-6}m^2$.

- **Solution**

HW10

- A MOS capacitor has:

  Xox=10nm, **Na=$10^{17}m^{-3}$**, **ε_{ox}=3.9**, **ε_s=11.8**

- Determine:

  (i) **C(HF)** in **accumulation;**

  (ii) **C(HF)** in **strong inversion;**

  (iii) **C(LF)** in **strong inversion**

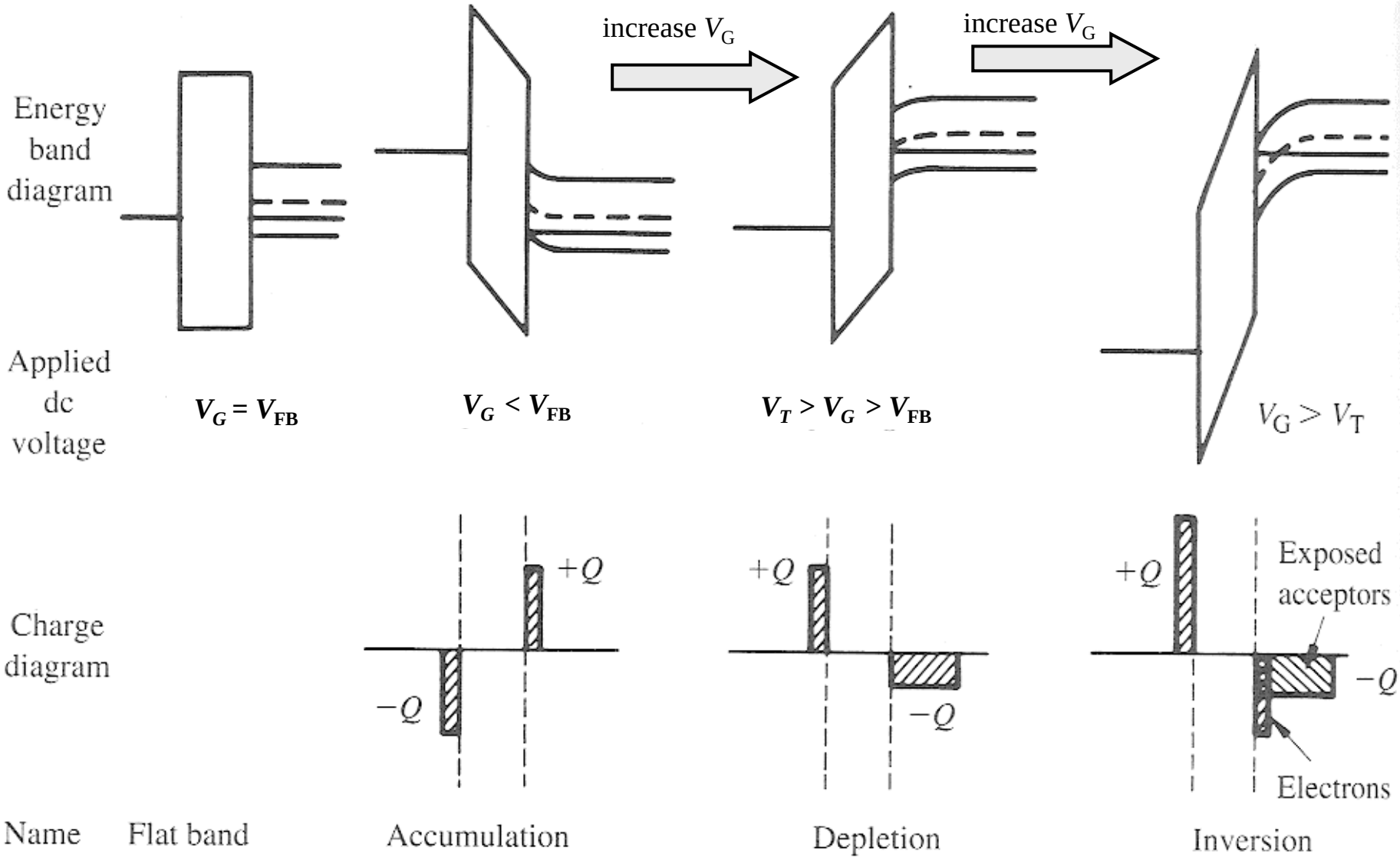
Summary: Three diagrams

1. **Block charge density diagram**
2. **Energy band diagram**
3. **CV diagram**

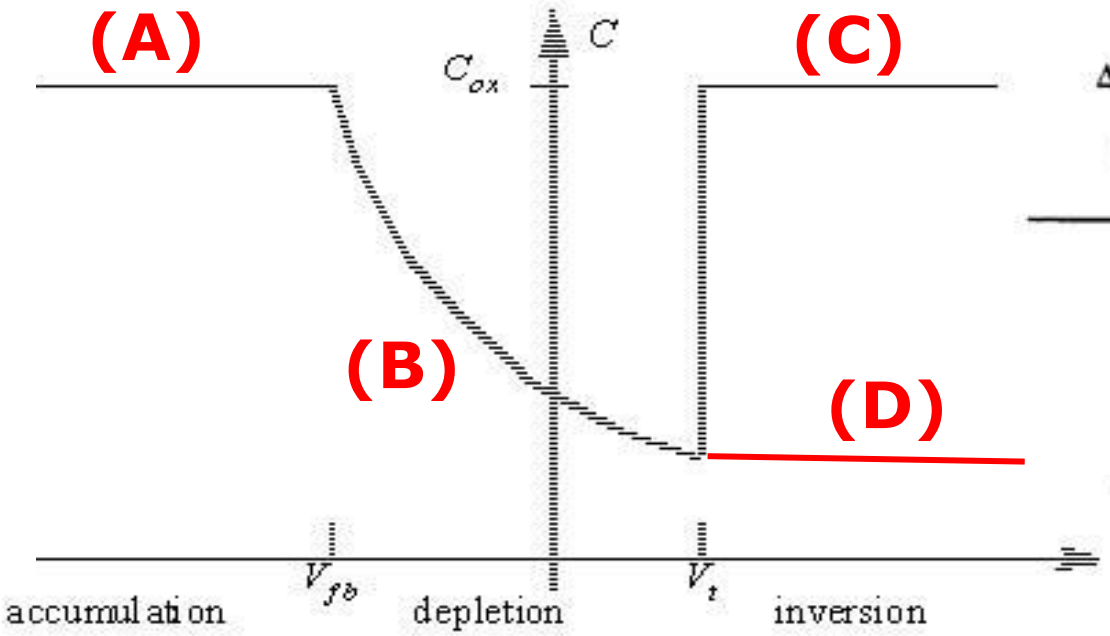
Vg change from – to +: from accumulation to inversion (p-type sub.)

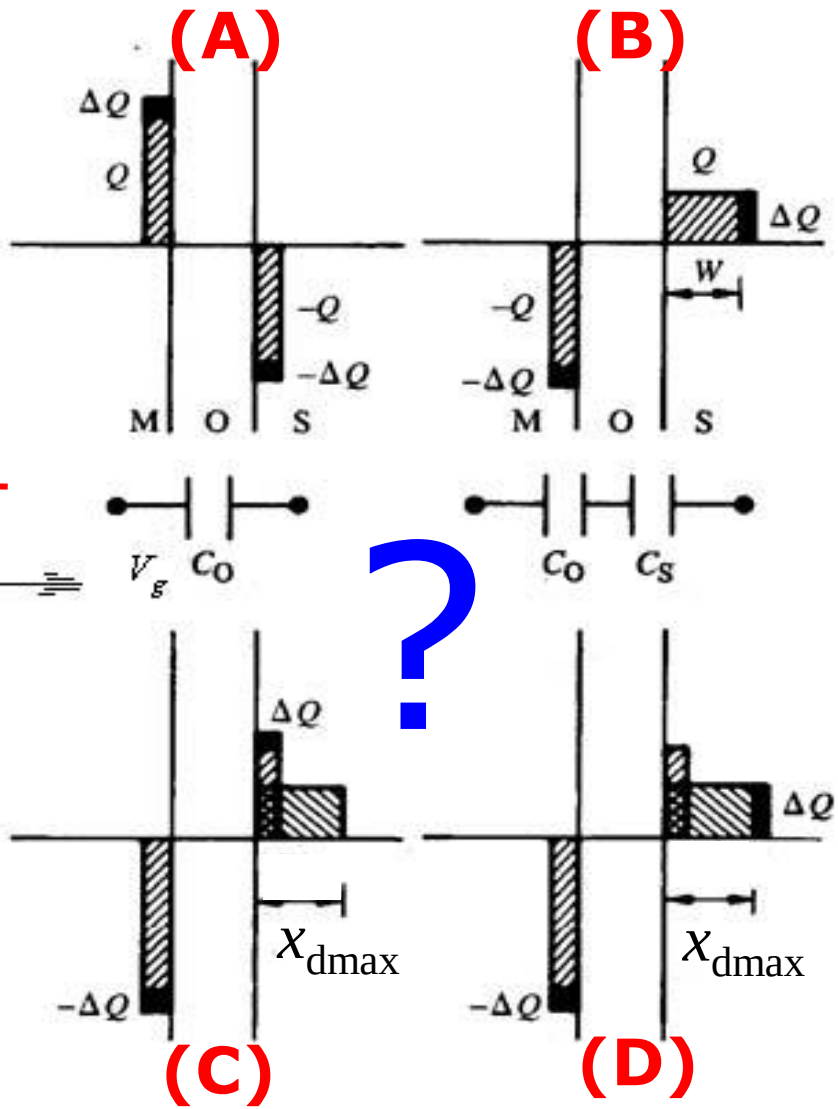
Summary

Biasing Conditions for p-type Si



Summary

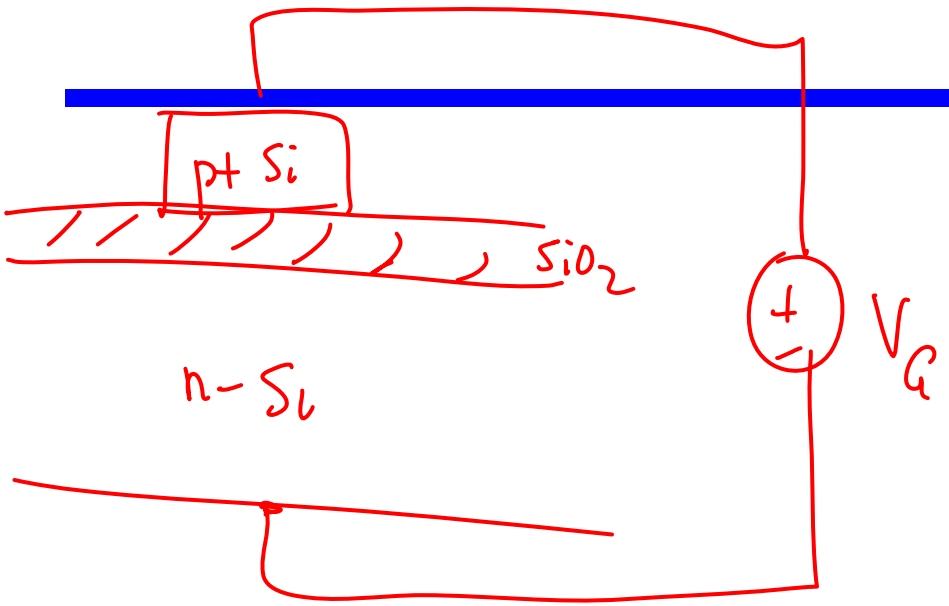


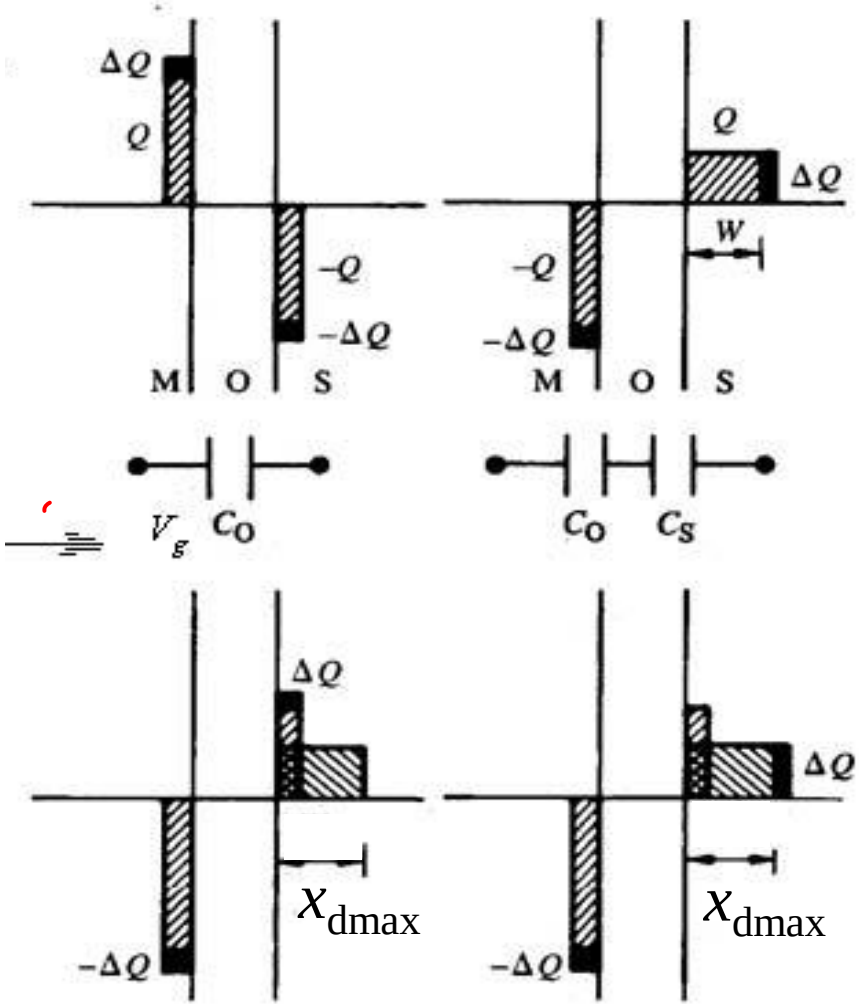


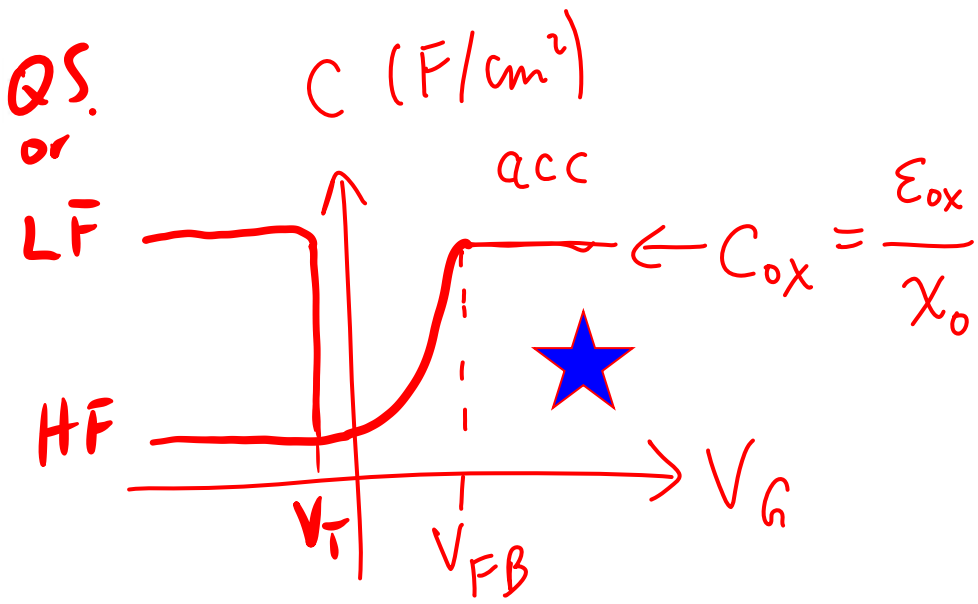
$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}}$$

$$\frac{1}{C} = \sqrt{\frac{1}{C_{ox}^2} + \frac{2(V_g - V_{fb})}{qN_a\varepsilon_s}}$$

n-type Si


p+ Si
SiO2
n-Si
+
−
VG

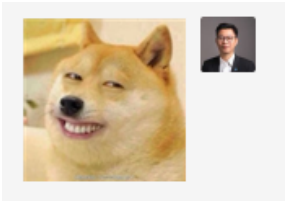

ΔQ
Q
−Q
−ΔQ
M O S
Vg
CO
W
CS
xdmax


QS.
or
LF
HF
C (F/cm²)
acc
← COX = εox / xo
VT
VFB
VG

MOS Capacitance

OUTLINE

- MOS structure
- MOS energy band diagram
- Effects of applied biases
- ***Voltage drops**



Voltage dropped in the silicon

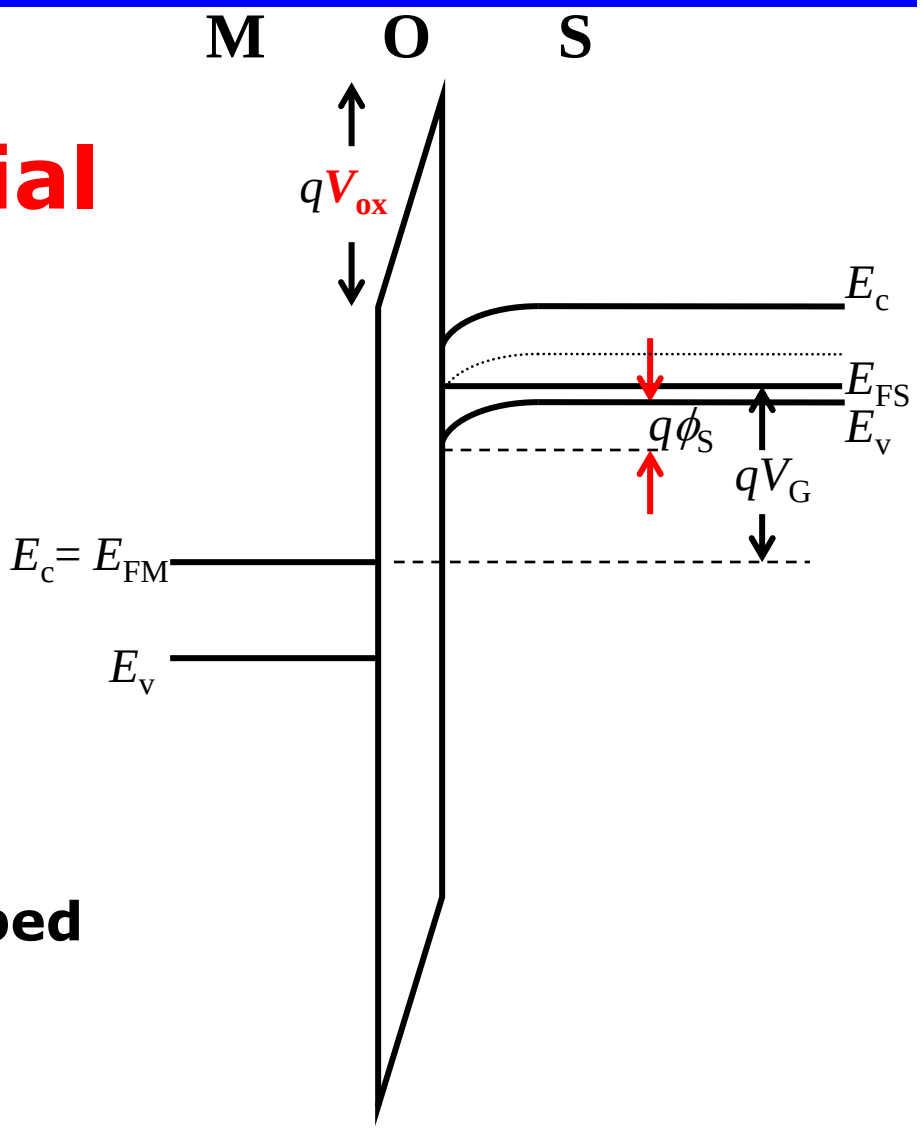
Surface Potential

$$q\phi_S = qV_S$$

$$q\phi_S = E_i(bulk) - E_i(surface)$$

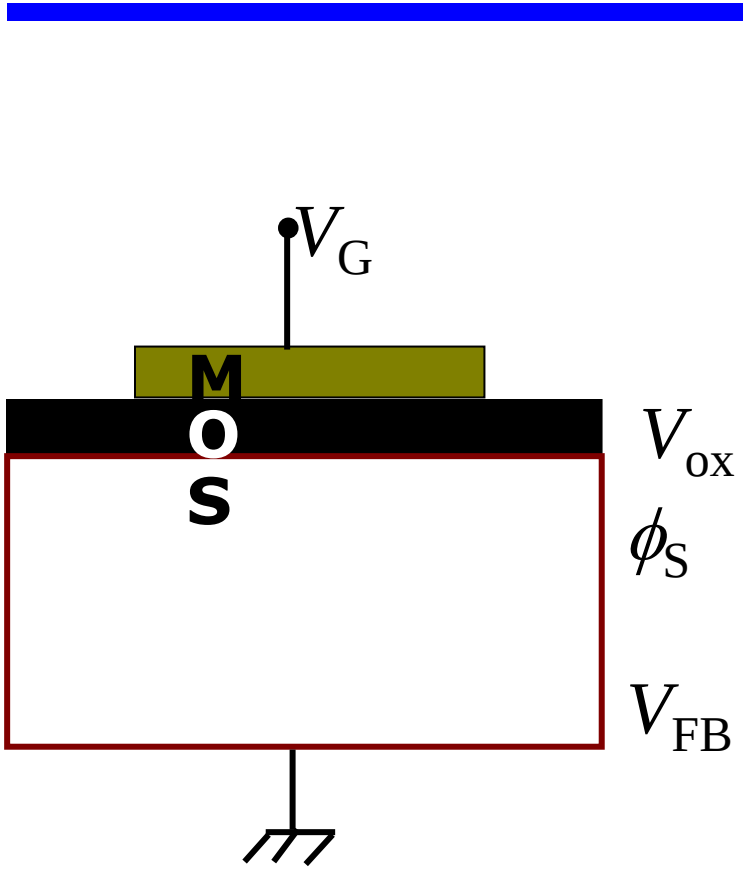
$$q\phi_S = E_C(bulk) - E_C(surface)$$

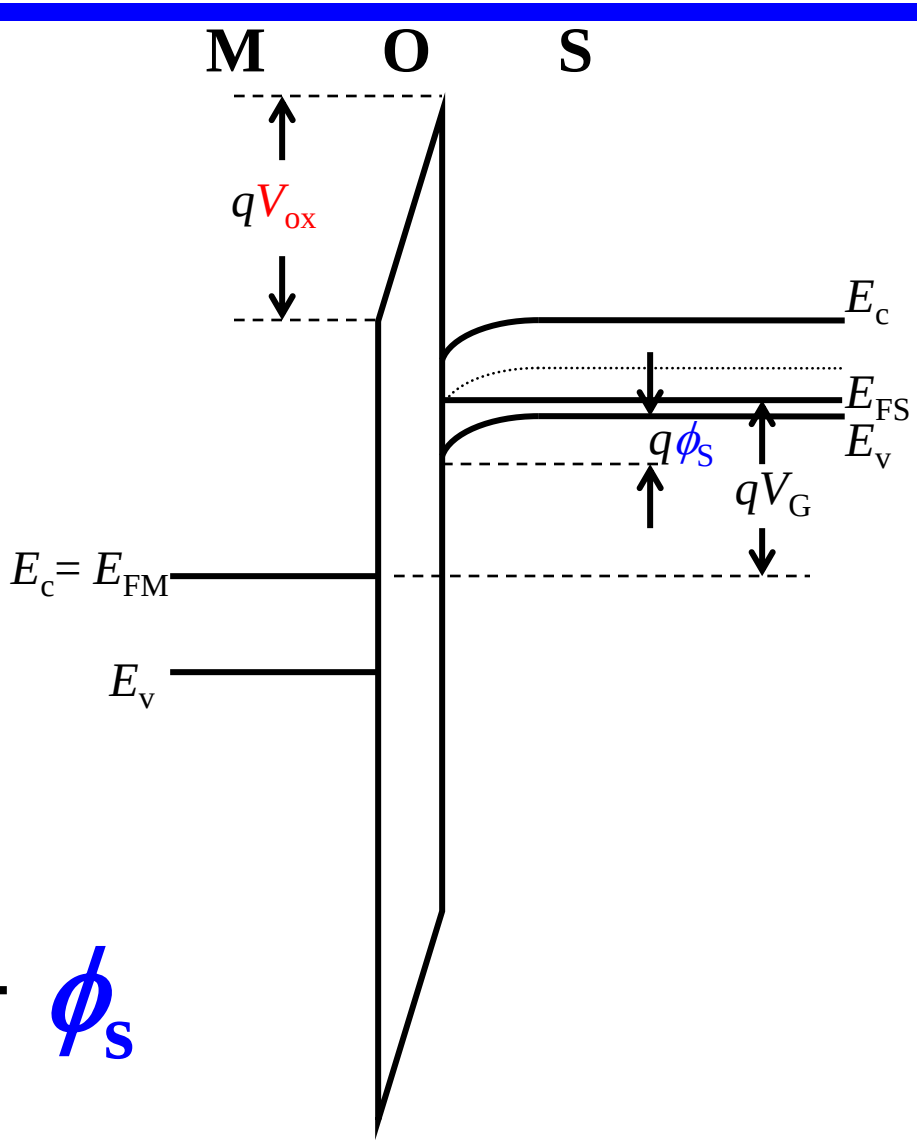
$$q\phi_S = E_V(bulk) - E_V(surface)$$



V_{ox} is the voltage dropped across the oxide

Voltage Drops in the MOS System





$$V_G - V_{FB} = V_{ox} + \phi_s$$

Voltage Drops in the MOS System

- In general,

$$V_G = V_{FB} + V_{ox} + \phi_s$$

where

$qV_{FB} = \Phi_{MS} = \Phi_M - \Phi_S$

V_{ox} is the voltage dropped across the oxide
(V_{ox} = total amount of band bending in the oxide)

ϕ_s is the voltage dropped in the silicon
(total amount of band bending in the silicon)

$$q\phi_S = E_i(bulk) - E_i(surface)$$

For example: When $V_G = V_{FB}$, $V_{ox} = \phi_s = 0$
i.e. there is no band bending

Voltage Drops in the MOS System

$$V_G = V_{FB} + V_{ox} + \phi_s$$

$V_g = V_T \rightarrow$
$\phi_s = 2\phi_F$

$$V_T = V_{FB} + V_{ox} + 2\phi_F$$

$$V_{ox} = -\frac{\sqrt{2qN_D\varepsilon_{Si}\left|2\phi_F\right|}}{C_{ox}}$$

$$V_T = V_{FB} + 2\phi_F - \frac{\sqrt{2qN_D\varepsilon_{Si}\left|2\phi_F\right|}}{C_{ox}}$$

HW8

- A MOS capacitor has:
  Xox=40nm, Nd=$10^{21}\mathbf{m}^{-3}$, ϕ_F=0.3V, ε_{ox}=3.9, ε_s=11.8
- Determine:
  (i) C(HF) in accumulation; (ii) C(HF) in strong inversion
  (iii) C(LF) in strong inversion
- Solution:

(i) $C(HF)= C_{ox}=\varepsilon_o\varepsilon_{ox}/Xox$
$=8.85E\text{-}12\times3.9/4.0E\text{-}8$
$=8.63E\text{-}4\ F/m^2$

(ii) In inversion

$V_S=2\phi_F=0.6V$

$$x_d=\left(\frac{2\varepsilon_o\varepsilon_s V_S}{qN_d}\right)^{1/2}$$

$x_d=8.85E\text{-}7\ m$

$C_s=\varepsilon_o\varepsilon_s/x_d = 1.18E\text{-}4F/m^2$

$C(HF)=C_{ox}C_s/(C_{ox}+C_s)=1.04E\text{-}4F/m^2$

(iii) $C(LF)=C_{ox}=8.63E\text{-}4\ F/m^2$

HW9

- **Problem**
- An MOS capacitor is made on uniformly doped p type material. With -20V on the gate with respect to the substrate it has a capacitance of 20pF. With +20V on the gate it has a capacitance of 10pF. What is the thickness of the depletion layer if the capacitor has an area of $10^{-6}m^2$.

- **Solution**
- With negative bias on the top electrode: C = Cox. (20pF)
- With positive bias: 1/C = 1/Cox+1/Cs
- since $Cs=(1/C - 1/Cox)^{-1}= (1/10 - 1/20)^{-1} =20$ pF. The thickness of the depletion layer xd is obtained from $Cs=A\varepsilon_s\varepsilon_0/ x_d$,
- $x_d =10^{-6}*12* 8.8*10^{-12}/ 20*10^{-12} =$**$5*10^{-6}$m**