



EEE205 – Digital Electronics (II)

Lectures 17-18

DAC and ADC

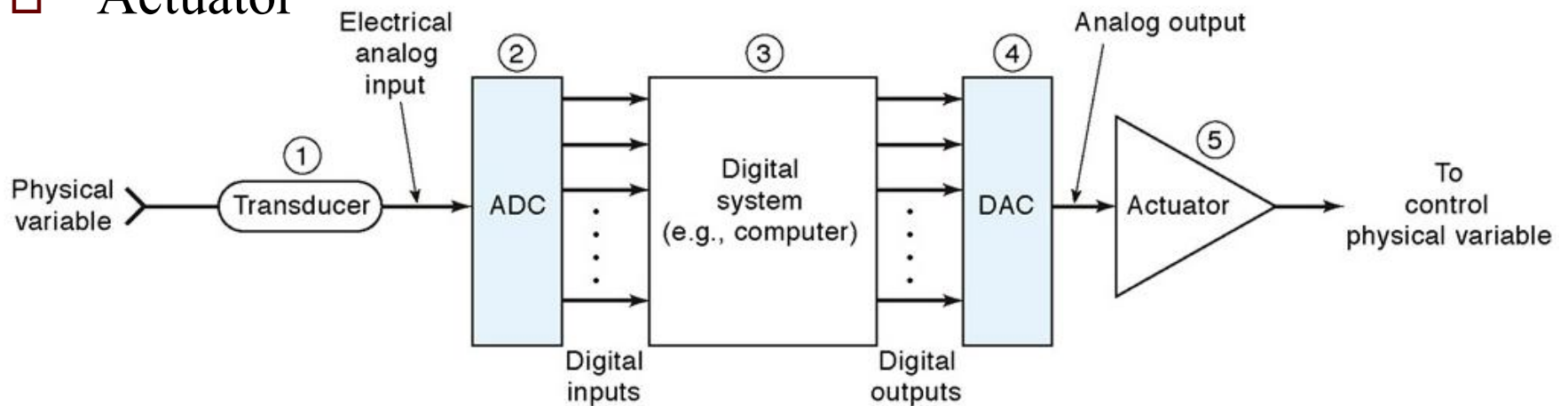
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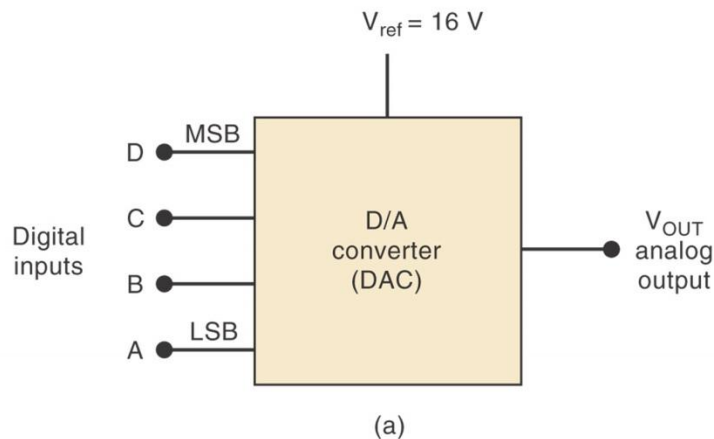
Interfacing With the Analog World

- ❑ Transducer
- ❑ ADC
- ❑ Computer
- ❑ DAC
- ❑ Actuator



Digital to Analog Conversion

- The conversion process:
 - Digital code is converted to a proportional voltage/current
 - Reference voltage determines the max DAC output
- Analog (pseudo analog) output

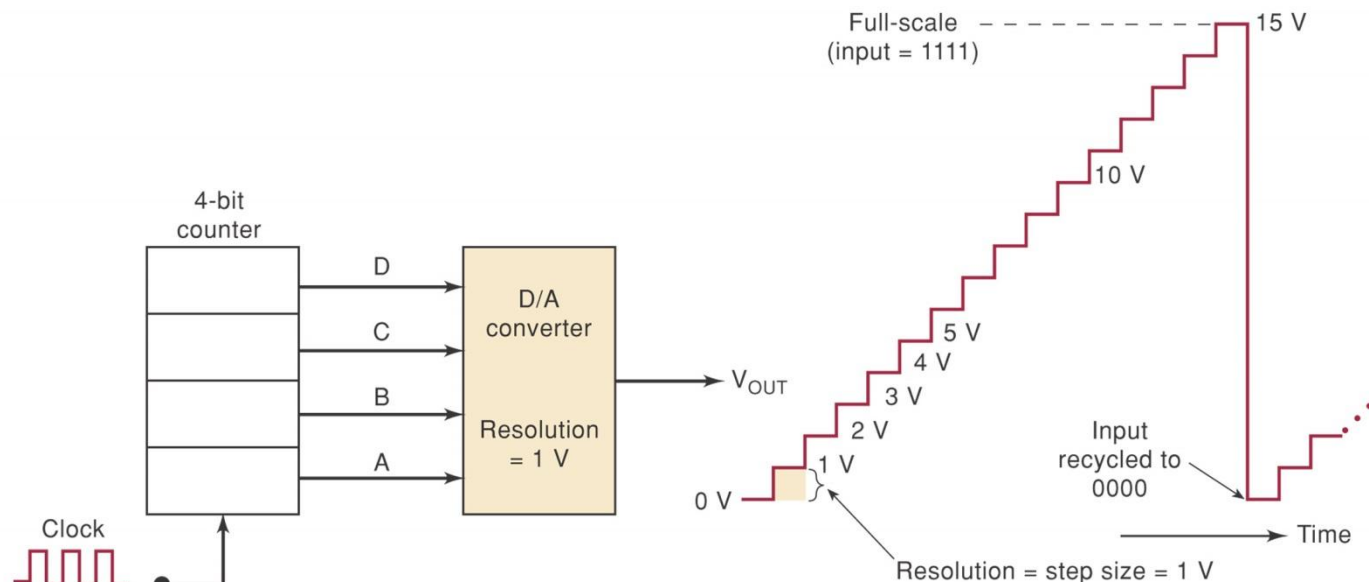


D	C	B	A	V_{OUT}	
0	0	0	0	0	Volts
0	0	0	1	1	
0	0	1	0	2	
0	0	1	1	3	
0	1	0	0	4	
0	1	0	1	5	
0	1	1	0	6	
0	1	1	1	7	
1	0	0	0	8	Volts
1	0	0	1	9	
1	0	1	0	10	
1	0	1	1	11	
1	1	0	0	12	
1	1	0	1	13	
1	1	1	0	14	
1	1	1	1	15	

(b)

Digital to Analog Conversion

- Resolution (step size) = analog full-scale output divided by $2^n - 1$, where n is the number of bits.
- Analog output = resolution \times digital input





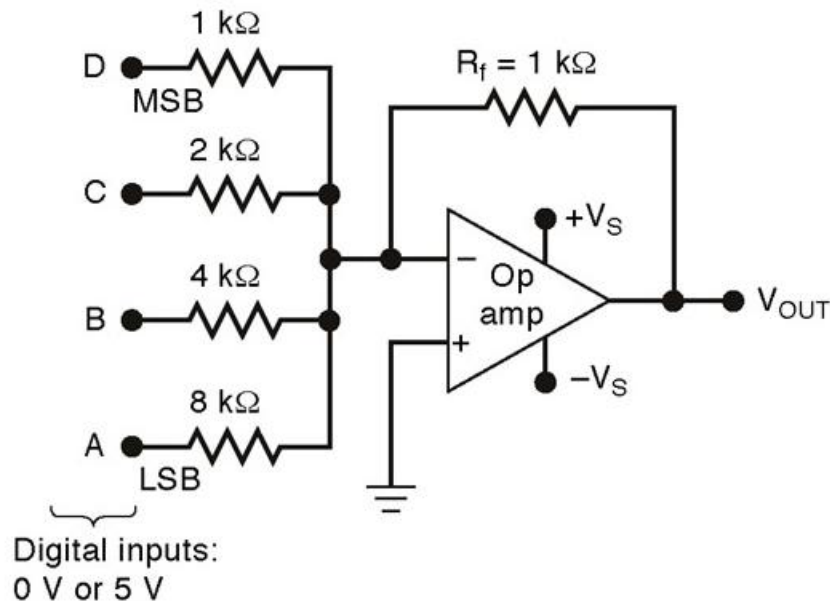
Digital to Analog Conversion

□ Bipolar DACs

- Many DACs produce both positive and negative values
- 2's complement can be used to represent negative voltages

D/A Converter Circuitry

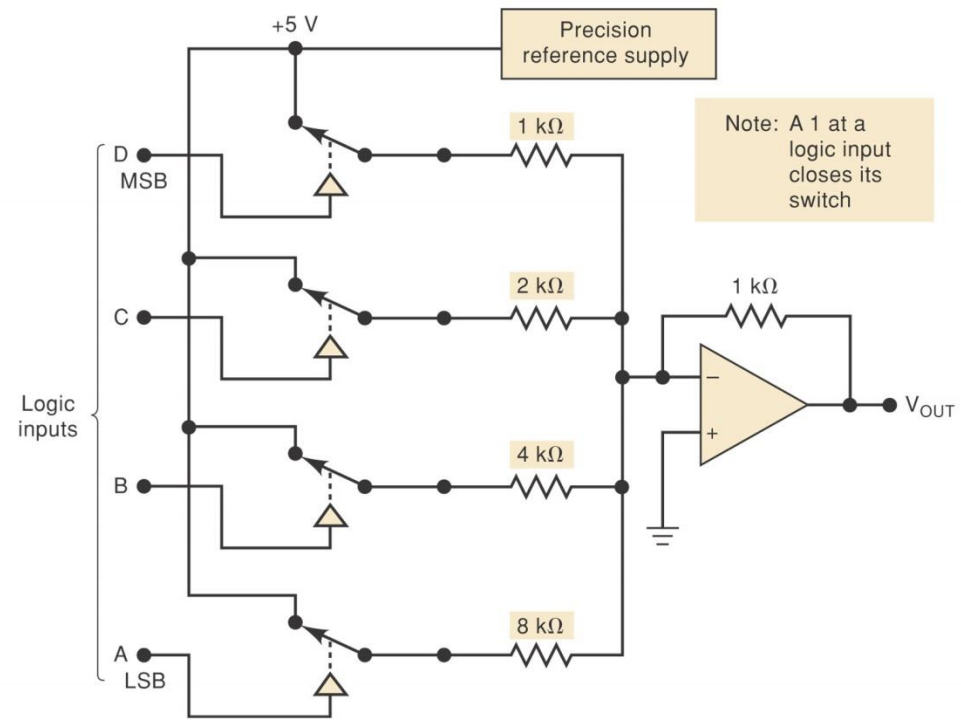
- A summing operational amplifier with a resolution of .625 V. $V_{OUT} = -(V_D + V_C/2 + V_B/4 + V_A/8)$



Input code				V_{OUT} (volts)
D	C	B	A	
0	0	0	0	0
0	0	0	1	-0.625 ← LSB
0	0	1	0	-1.250
0	0	1	1	-1.875
0	1	0	0	-2.500
0	1	0	1	-3.125
0	1	1	0	-3.750
0	1	1	1	-4.375
1	0	0	0	-5.000
1	0	0	1	-5.625
1	0	1	0	-6.250
1	0	1	1	-6.875
1	1	0	0	-7.500
1	1	0	1	-8.125
1	1	1	0	-8.750
1	1	1	1	-9.375 ← Full-scale

D/A Converter Circuitry

- The digital inputs cannot be taken directly from FFs or logic gates
- Each digital input controls a semi-conductor switch to a precision reference supply.



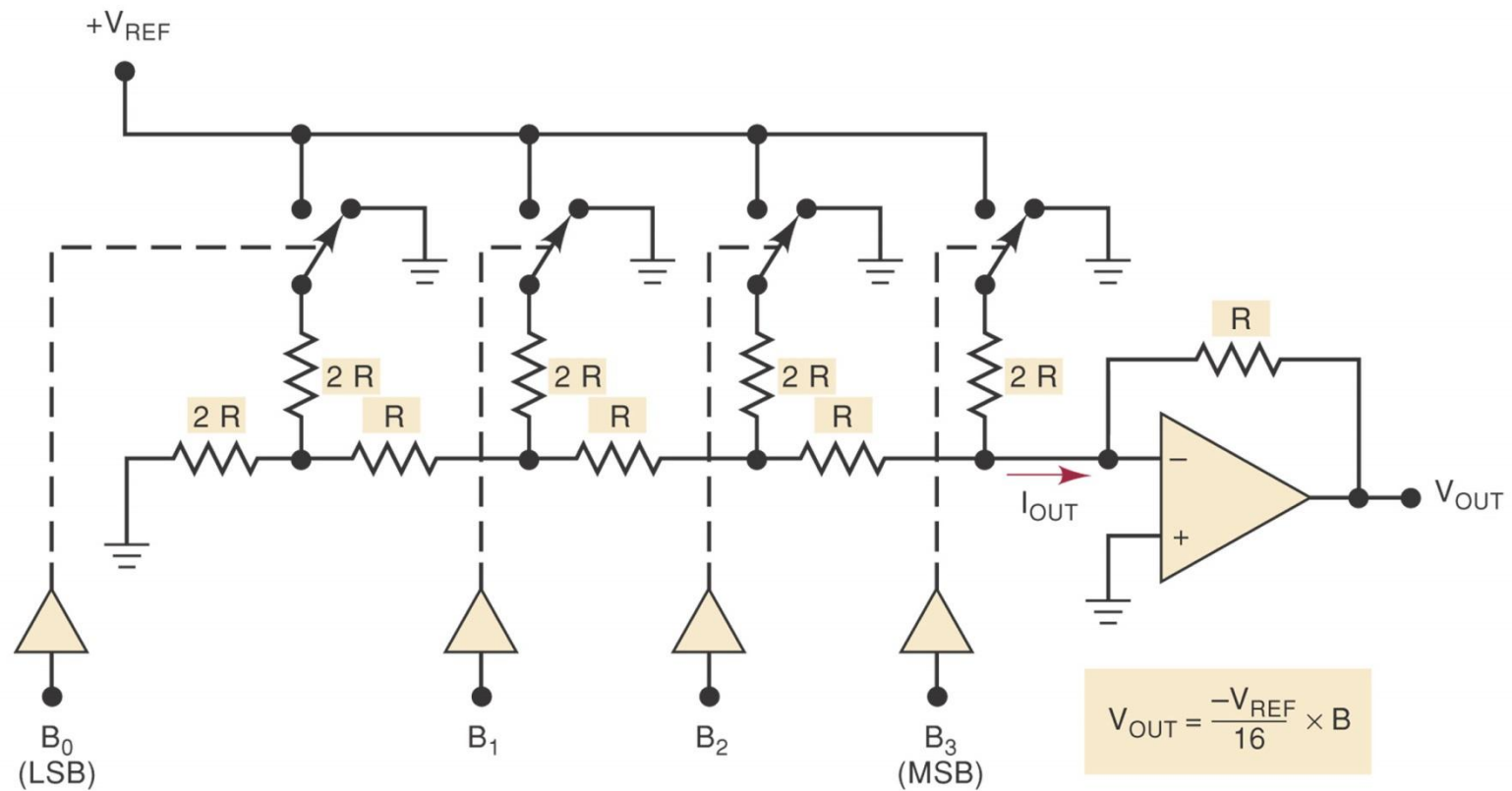
D/A Converter Circuitry

□ R/2R ladder

- Circuits with binary weighted resistors cause a problem due to the large difference in R values between LSB and MSB
- The R/2R ladder uses resistances that span only a 2 to 1 range

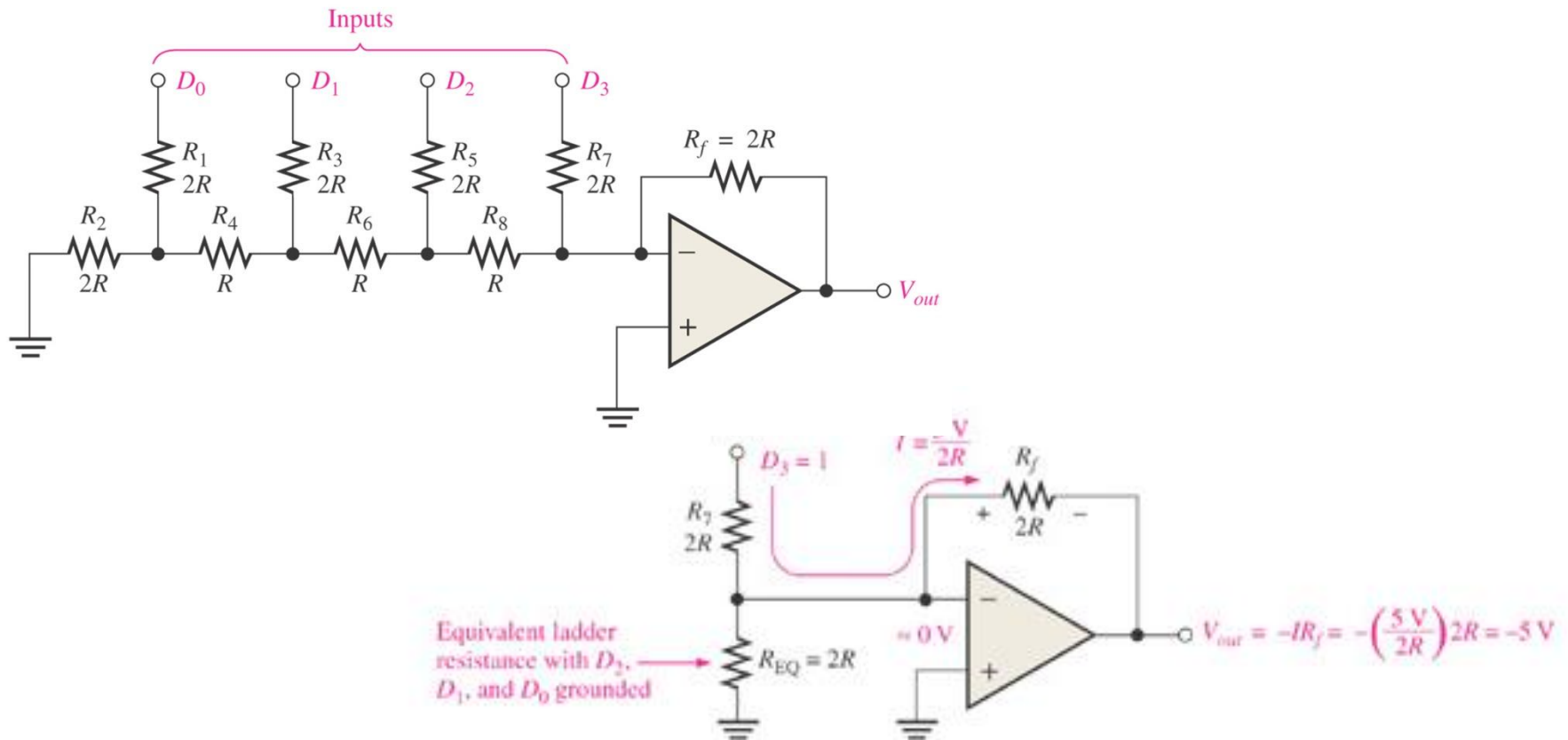
D/A Converter Circuitry

□ R/2R ladder DAC



D/A Converter Circuitry

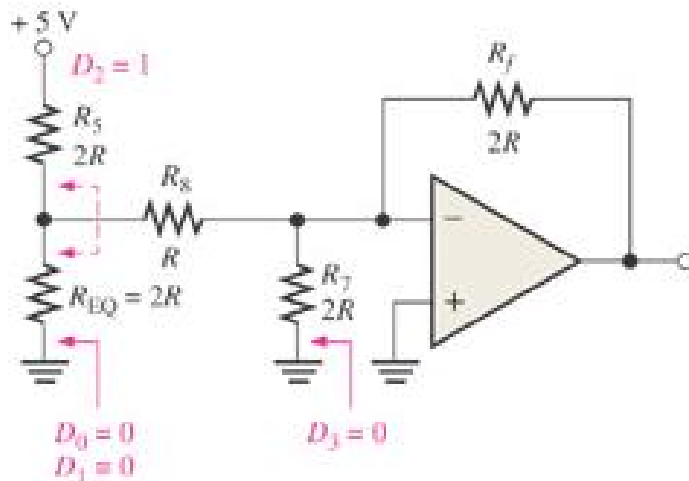
□ R/2R ladder DAC



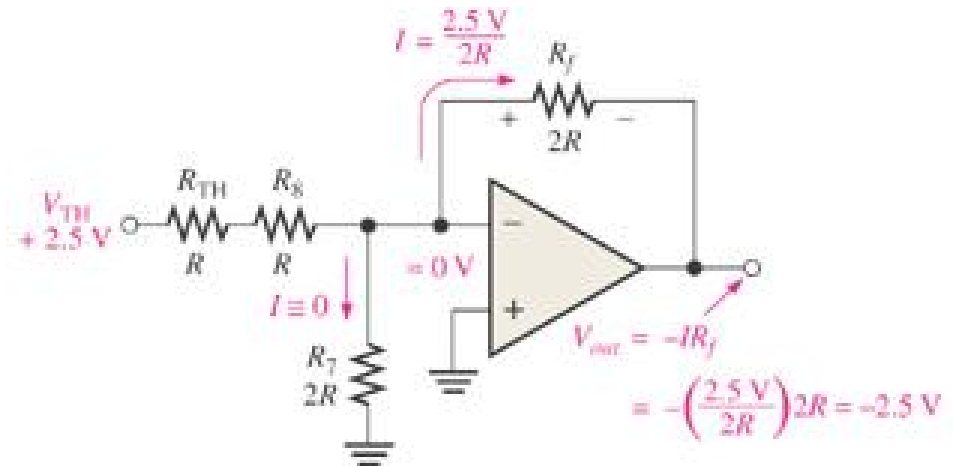
(a) Equivalent circuit for $D_3 = 1, D_2 = 0, D_1 = 0, D_0 = 0$

D/A Converter Circuitry

□ R/2R ladder DAC

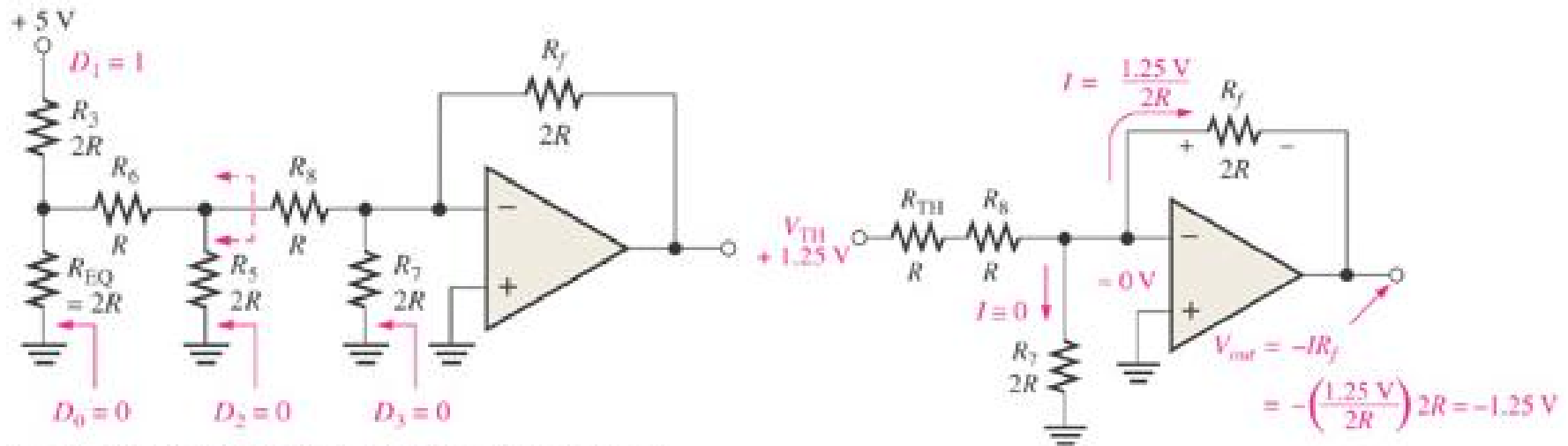


(b) Equivalent circuit for $D_3 = 0$, $D_2 = 1$, $D_1 = 0$, $D_0 = 0$



D/A Converter Circuitry

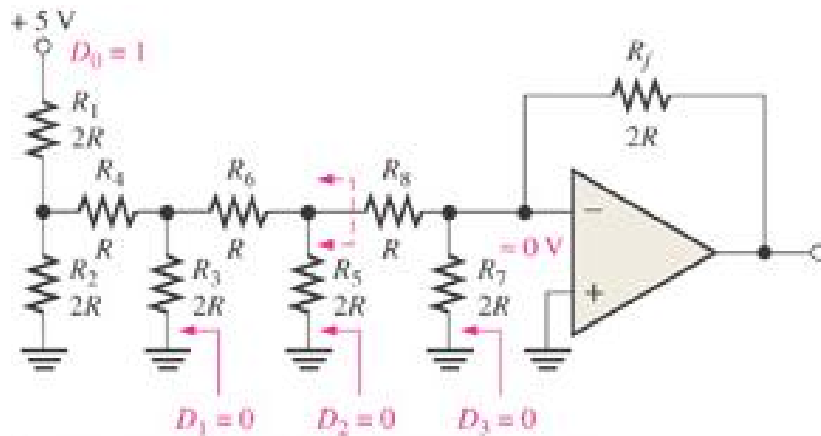
□ R/2R ladder DAC



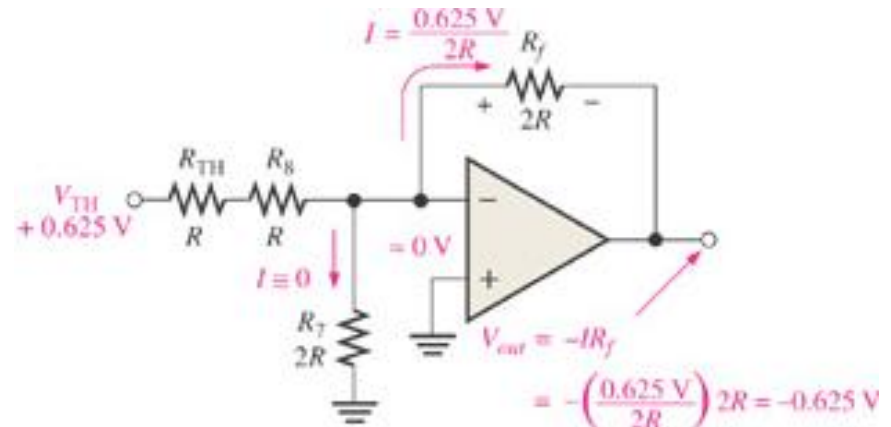
(c) Equivalent circuit for $D_3 = 0$, $D_2 = 0$, $D_1 = 1$, $D_0 = 0$

D/A Converter Circuitry

□ R/2R ladder DAC



(d) Equivalent circuit for $D_3 = 0, D_2 = 0, D_1 = 0, D_0 = 1$



DAC Specifications

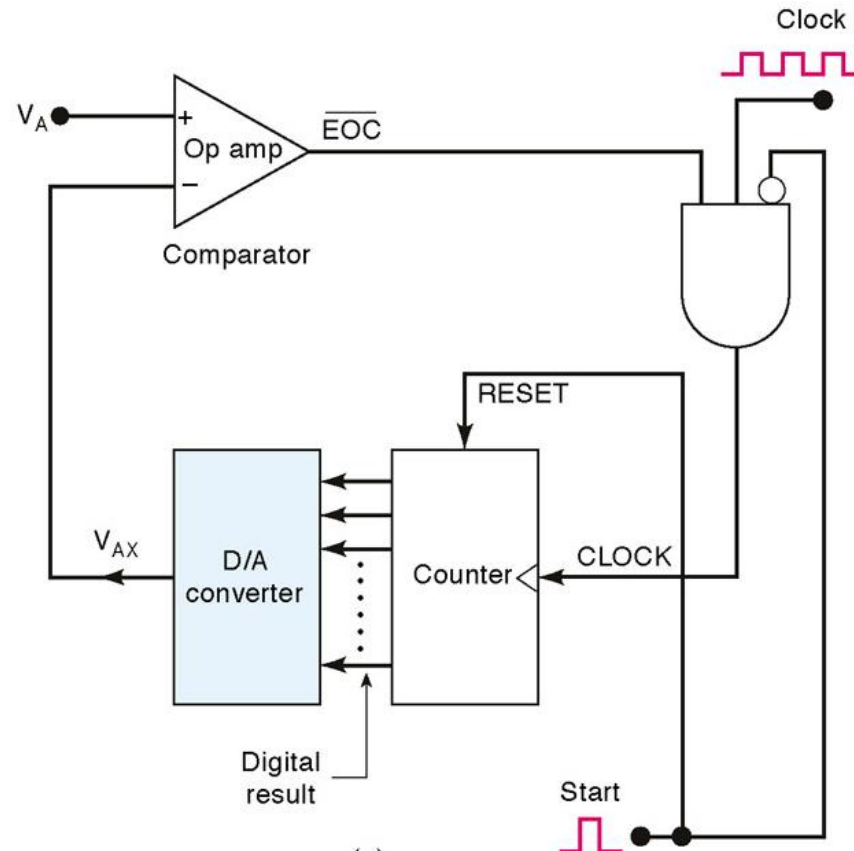
- ❑ Many DACs are available as ICs or self contained packages. Key specifications are:
 - Resolution: number of bits
 - Accuracy: maximum deviation from ideal value, as a percentage of full scale.
 - Offset error: output for a zero binary input.
 - Settling time: time to go from zero to full scale.
 - Monotonicity: output increases with binary input.

Analog to digital Conversion

- ❑ ADC – digital code represents the analog input
- ❑ Generally more complex and time consuming than DAC
- ❑ Several types of ADC use DAC circuits
- ❑ The Op amp comparator ADC
 - Variations differ in how the control section continually modifies numbers in the register

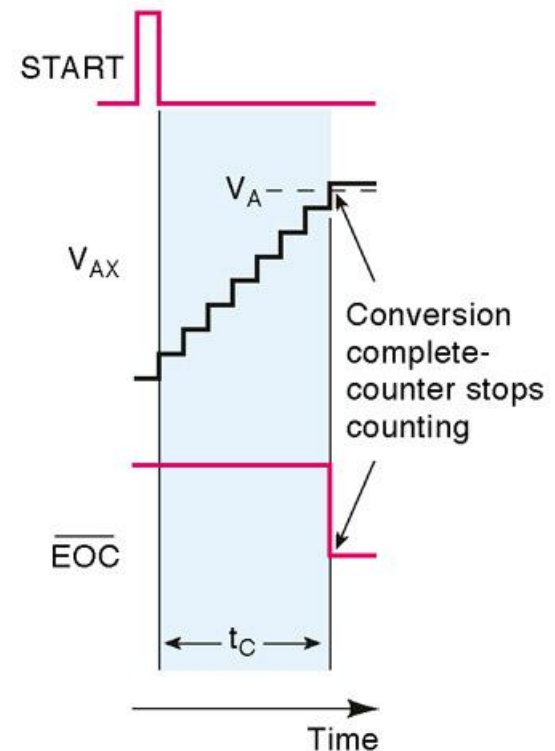
Digital Ramp ADC

- A binary counter is used as the register and allows clock to increment the counter a step at a time until $V_{AX} \geq V_A$



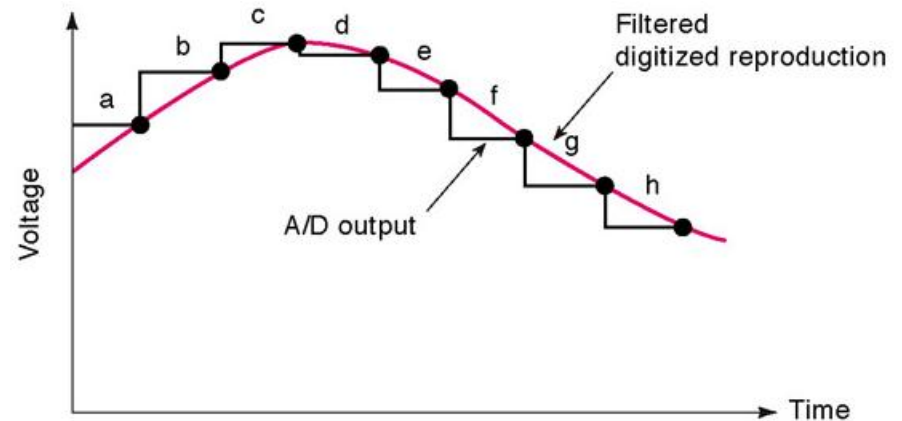
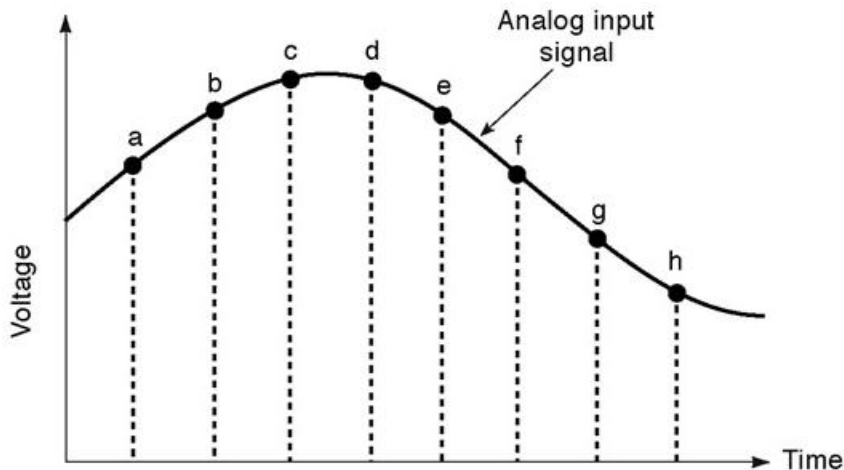
Digital Ramp ADC

- A/D resolution and accuracy
 - Measurement error is unavoidable
 - Reducing the step size can reduce but not eliminate potential error
 - This is called quantization error



Data Acquisition

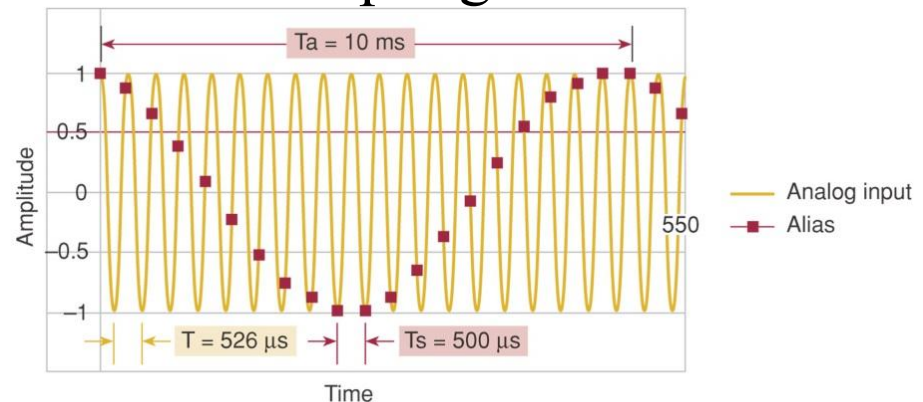
- Digitizing analog data and transferring to memory is data acquisition
- Acquiring a single data point value is sampling
- Reconstructing a digitized signal



Data Acquisition

□ Aliasing

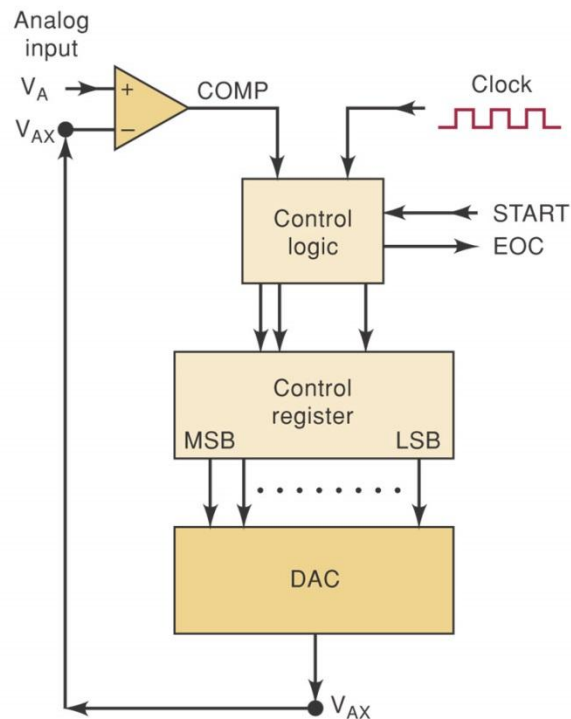
- Caused by under sampling
- Harry Nyquist
 - The sampling frequency must be at least twice the highest input frequency
 - Sampling at a frequency less than twice the input frequency results in under sampling and incorrect reproduction



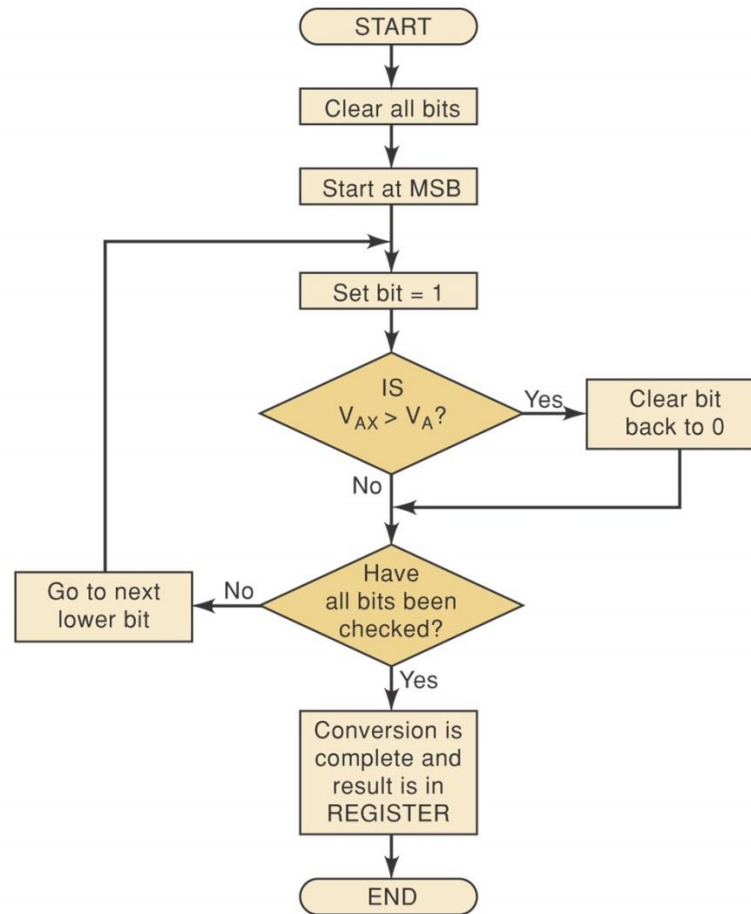
Successive Approximation ADC

- ❑ Widely used ADC
- ❑ More complex than digital ramp but has a shorter conversion time
- ❑ Conversion time is fixed and not dependent on the analog input
- ❑ Many SACs are available as ICs.

Successive Approximation ADC



(a)

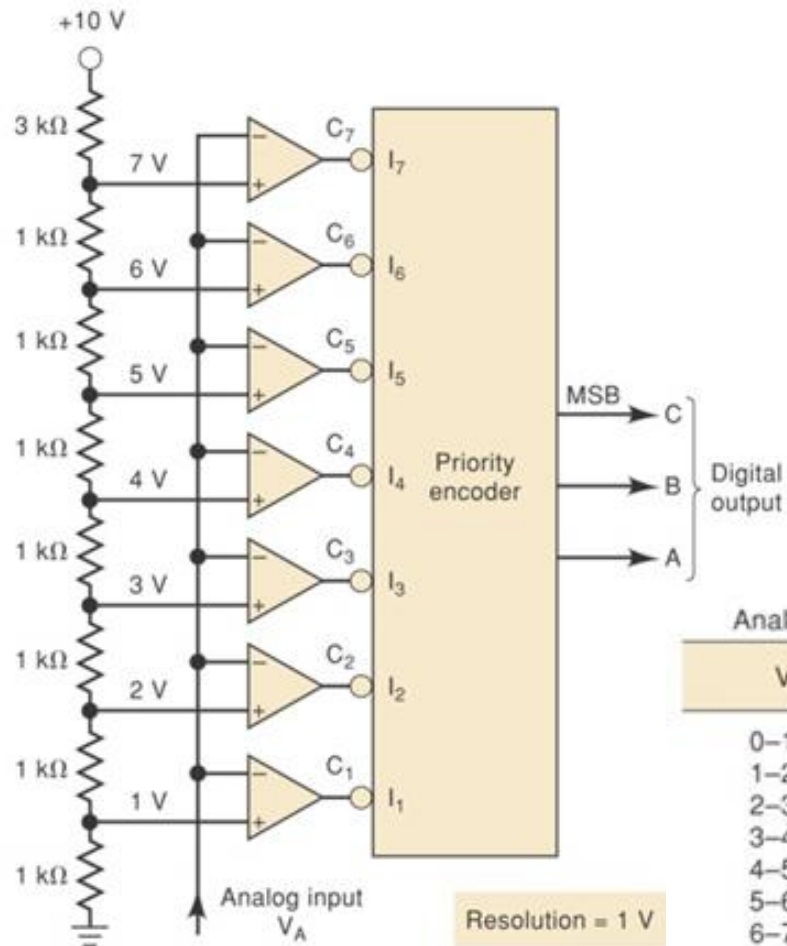


(b)

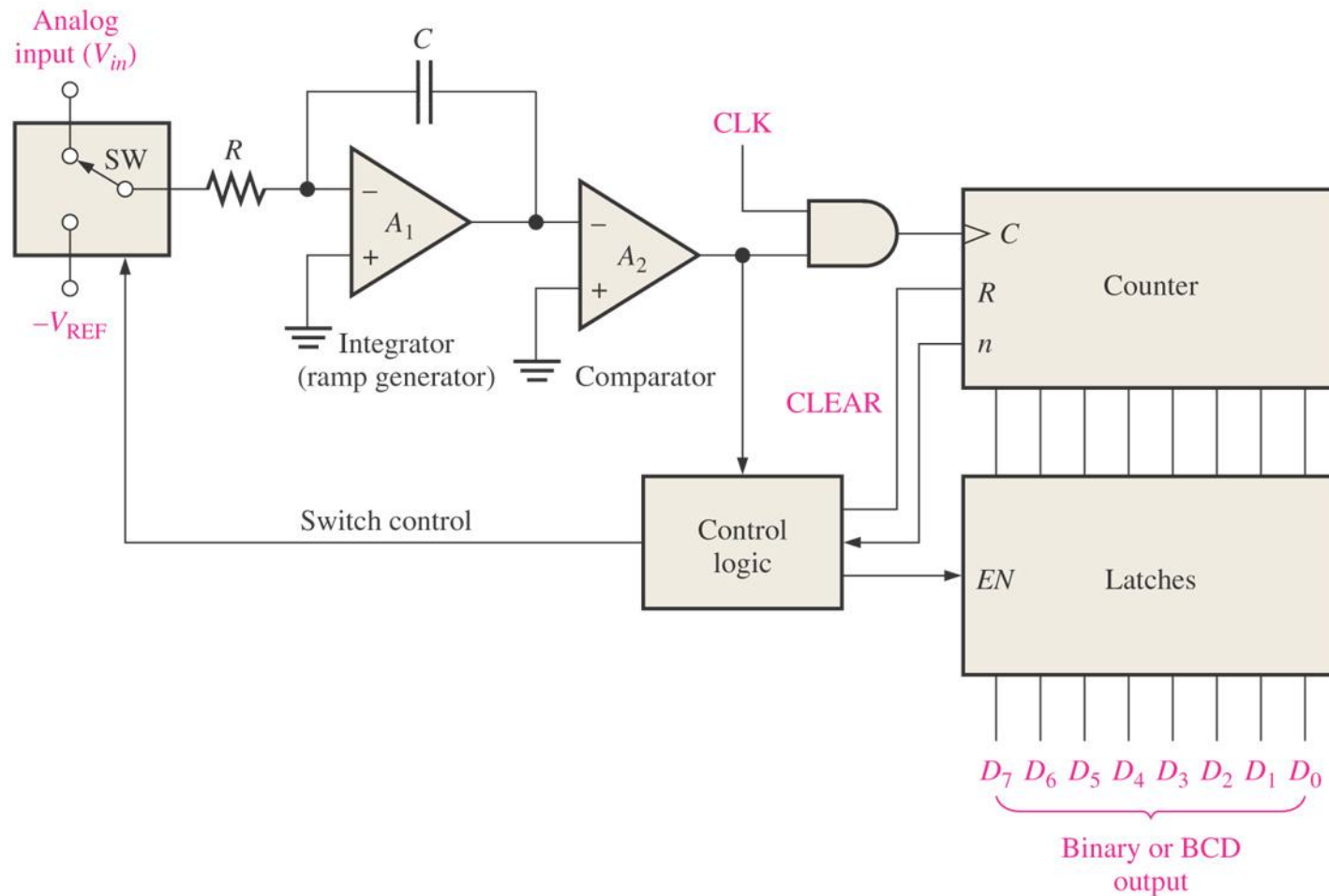
Flash ADCs

- High speed conversion
- Much more complex circuitry
 - 6 bit flash ADC requires 63 analog comparators
 - 8 bit flash ADC requires 255 comparators
 - 10 bit flash ADC requires 1023 comparators
- A 3 bit flash converter is described in figure 11-22
- Conversion time – No clock signal is used, so the conversion is continuous. This makes for very short conversion times, typically under 17 ns.

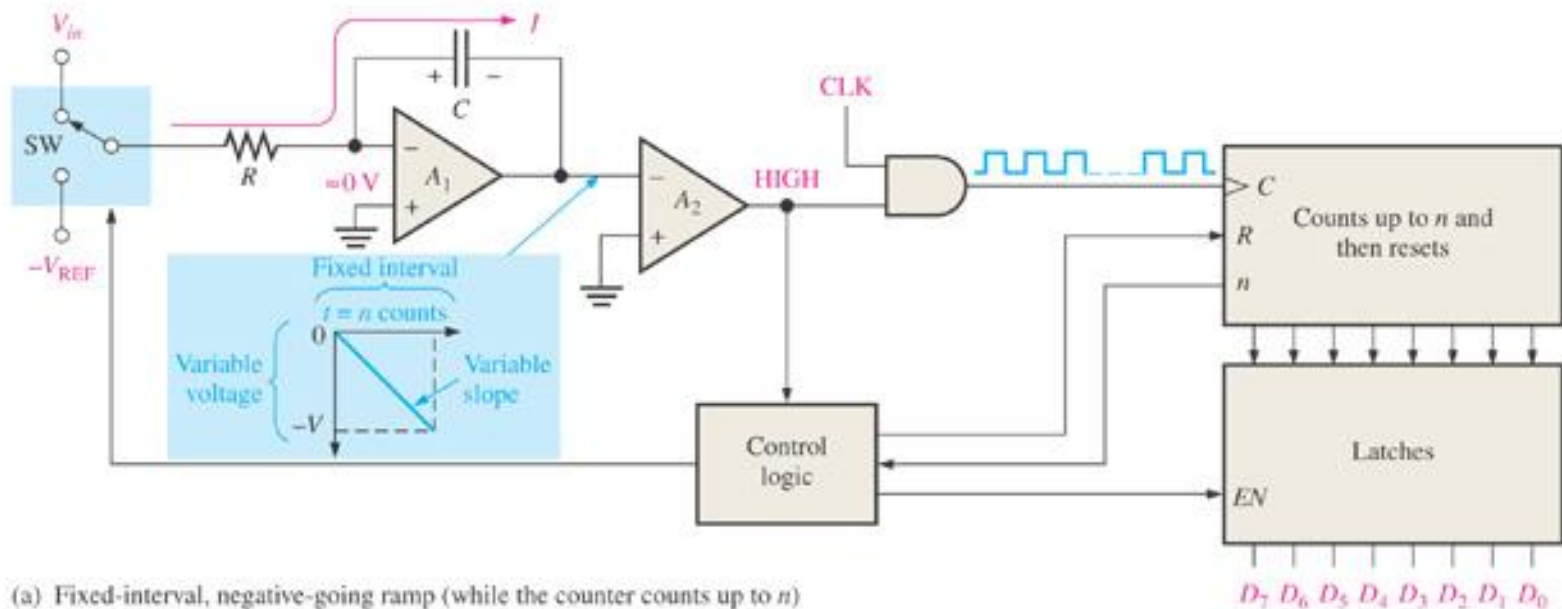
Flash ADCs

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Dual Slope ADCs

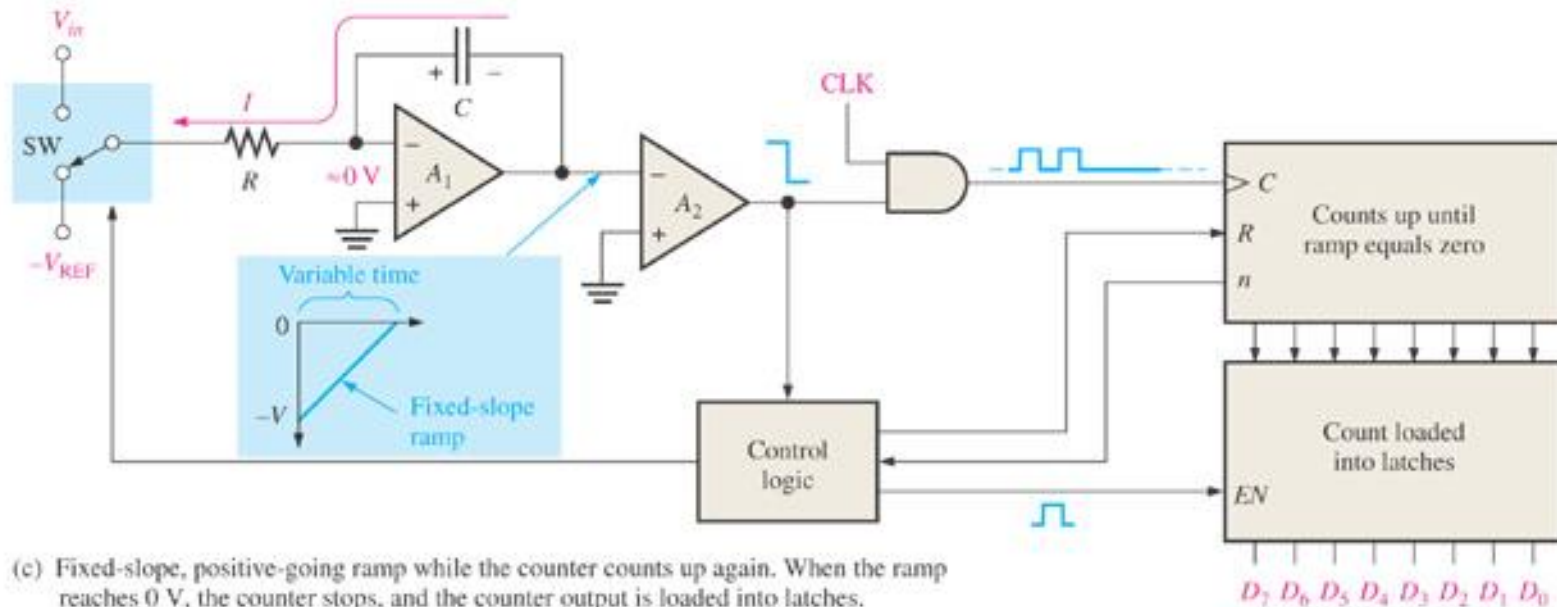


Dual Slope ADCs



- In stage 1, SW is switched to V_{in} . C is charged. At a fixed count, the counter is reset and switches SW to $-V_{REF}$.

Dual Slope ADCs



- In stage 2, C is discharged to zero. The number of clock cycles is proportional to V_{in} .

Other A/D Conversion Methods

- ❑ There are many other methods of A/D conversion. Each has pros and cons:
 - Up/down digital-ramp ADC (tracking ADC)
 - Voltage to frequency ADC
 - Sigma/delta modulation
- ❑ The method used will depend on the application