Lecture 4

of

EEE201

CMOS Digital Integrated Circuits

Department of Electrical & Electronic Engineering

Xi'an Jiaotong-Liverpool University (XJTLU)

Monday, 7th October 2024

- **MOS Capacitor**
  - physical structure
  - operation modes & band diagrams
  - capacitance

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Module Roadmap

CMOS Digital Integrated Circuit

Technology ⟷ Design and Technology Co-Optimization ⟷ **Design**

Material | **Device** | **CMOS Circuit**

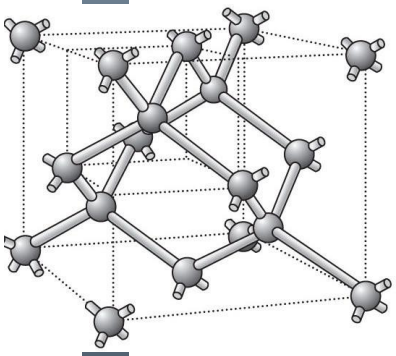
Lecture 4

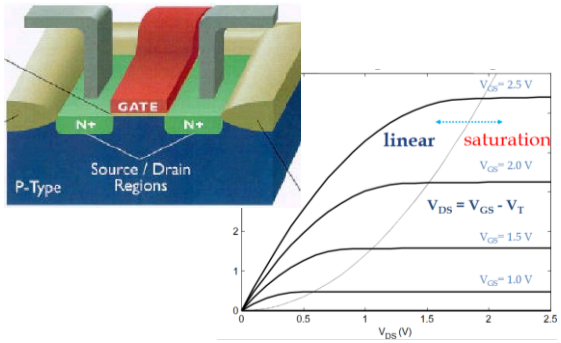
Silicon
1. Crystal structure
2. Energy diagram
3. Doping
4. Charge carriers
5. Carrier transport

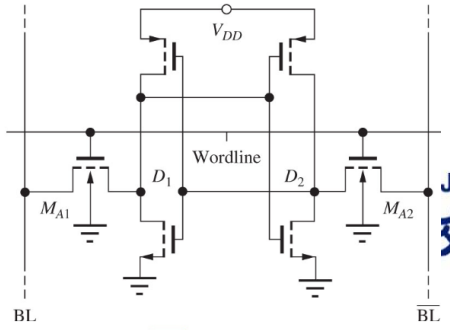
Device types:
1. P-N Junction
2. MOS Capacitor
3. MOSFET Transistor
4. MOSFET inverter

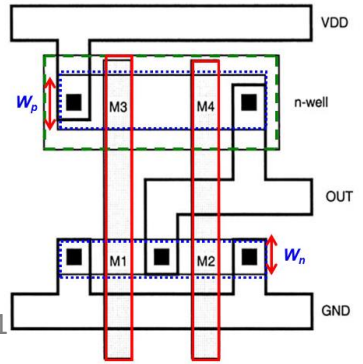
Circuit types:
1. Combinational logic circuits
2. Variant digital IC:
   - pseudo NMOS
   - Memory
   - Dynamic logic

Physical design :
1. Layout design:
   - Physical structures & layout principles
   - Area optimization
2. Physical design of CMOS inverter









Jiaoton

Recap: Lecture 3

MOS Transistor: IC Building Blocks

PN Junction

Electrostatic

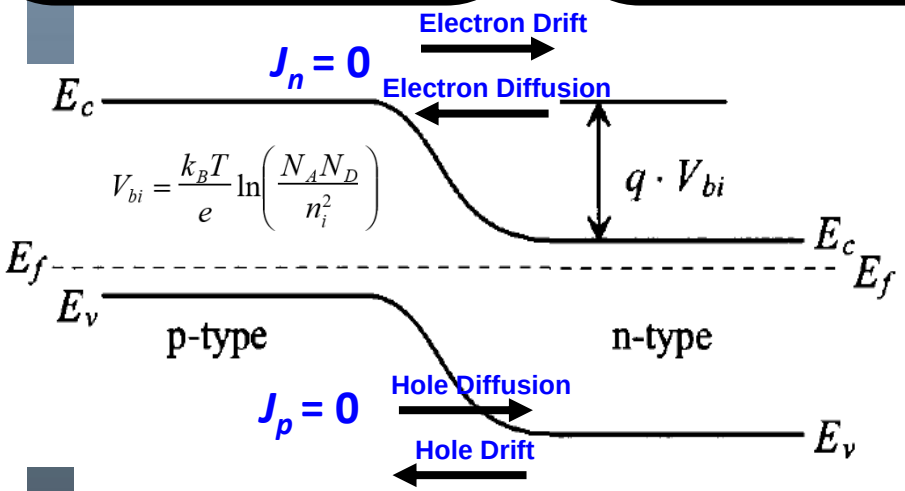
1. **Concentration gradient** ⇒ Diffusion current (J_{diff})
2. **Depletion regions** (immobile ionized dopant and acceptors) ⇒ Drift current (J_{drift})
3. **Built-in potential** (V_{bi}) to balance J_{diff} and J_{drift} ⇒ zero net current at equilibrium.
4. At equilibrium, $J_n = J_p = 0$

Current Characteristics

1. **Forward Bias:**
   - Dominant Current: Diffusion current of majority carriers.
   - Large current flow through junction
2. **Reverse Bias:**
   - Dominant Current: Drift current of minority carriers.
   - Small reverse saturation current until breakdown occurs.

Capacitance Characteristics

1. Impacts circuit **dynamics behavior**.
2. Depletion Region as a Capacitor:
   - Depletion regions with fixed charge ⇒ electric field and act as the plates of a capacitor.
   - Depletion width ⇒ distance between the capacitor plates.
   - Applying a reverse (forward) bias increases (decreases) W, reducing (increasing) capacitance.



$$W_0 = W_p + W_n = \sqrt{\frac{2\varepsilon_{Si}(N_A + N_D)V_{bi}}{eN_A N_D}}$$

$$I_D = I_{so}\left[\exp\left(\frac{eV}{k_B T}\right) - 1\right] \quad C = \frac{\varepsilon A}{d} \Rightarrow C_j = \frac{\varepsilon_{Si} A_j}{W_0}$$

MOS Capacitor

(fundamental to MOS transistor)

- CMOS digital ICs are constructed predominantly with **MOS transistors**.
- The **MOS transistor** is based on the **MOS capacitor** which is also a *fundamental* semiconductor structure apart from the ***p-n* junction**.
  - The **MOS capacitor** is also a two-terminal device like the ***p-n* junction** diode.
  - Knowledge of the **MOS capacitor** would be helpful to understand the operation and electrical properties of the **MOS transistor** or called the MOSFET.

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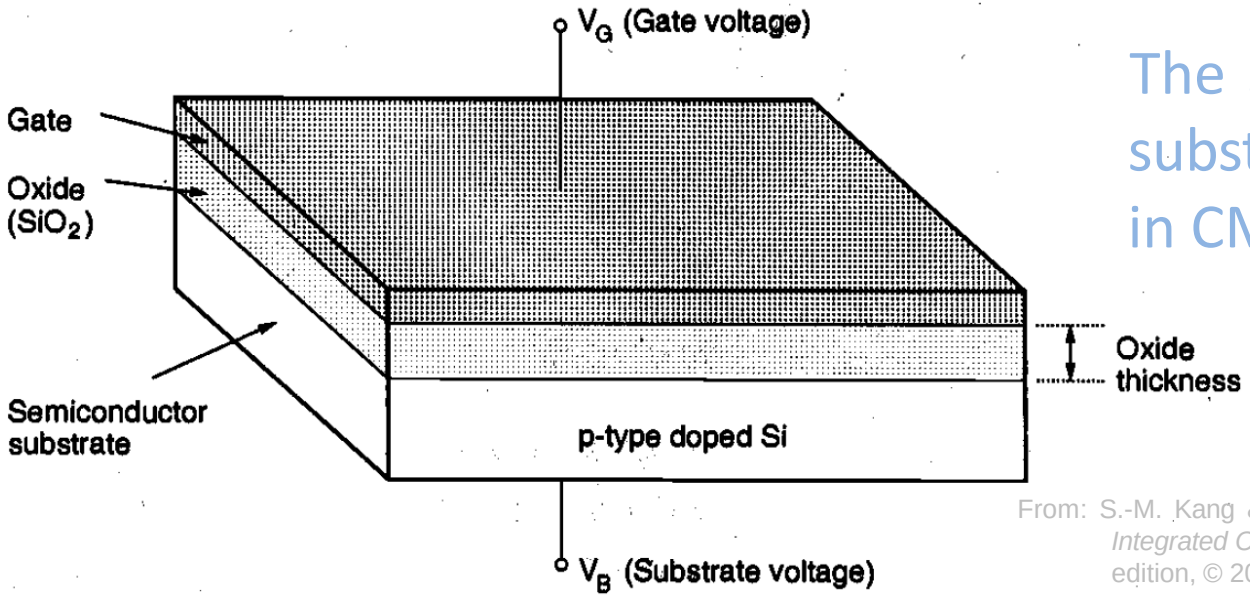
MOS Capacitor

(3-layered physical structure)

- The **MOS** capacitor consists of three layers:
  - the **metal** or polysilicon gate electrode
  - the insulating **oxide** (typically SiO_2)



The semiconductor substrate is silicon in CMOS digital ICs.

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  - the **semiconductor** substrate

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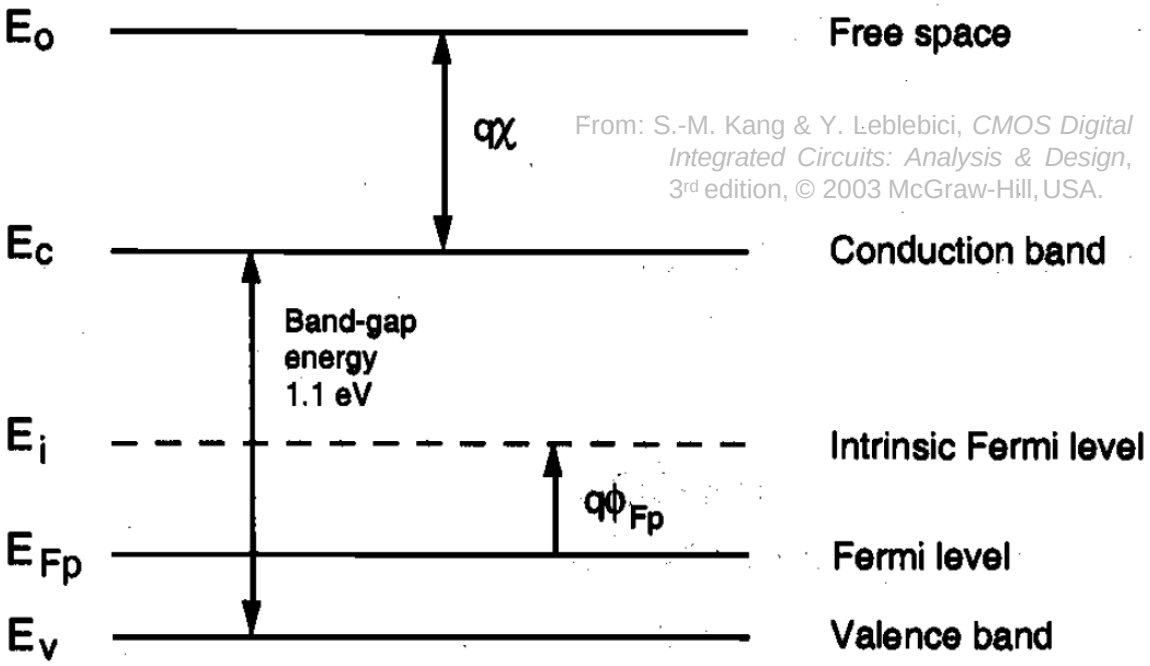
MOS Capacitor

(band diagram of silicon substrate)

- An insightful understanding of the MOS capacitor needs to use the electronic **energy band diagrams**.



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- Note the **free space energy level** (or called **vacuum level**), where electrons would be set free from the material.

- The above energy band diagram is *p*-type silicon. (Do you know why?)

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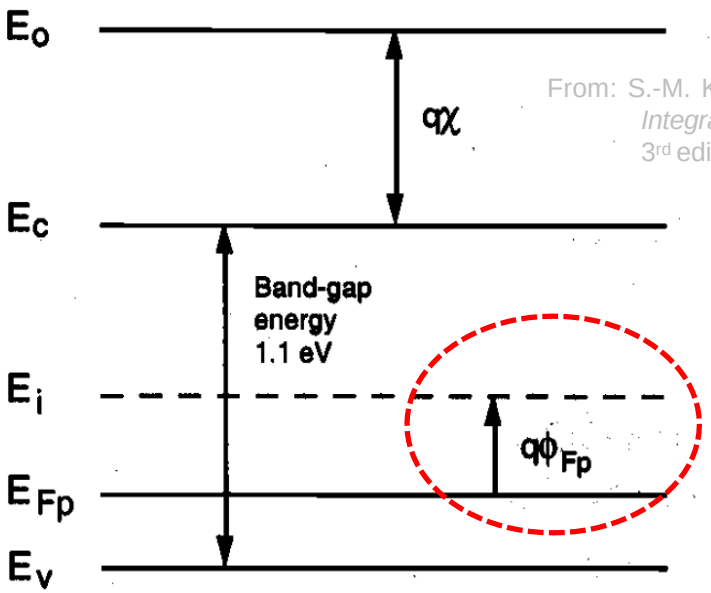
MOS Capacitor

(Fermi potential ϕ_F)

- In a doped semiconductor, the position of the *equilibrium* **Fermi level E_{Fp}** (or **E_{Fn}**) relative to the *intrinsic* **Fermi level E_i** can be quantified as ϕ_F:



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$$\phi_F \equiv \frac{E_F - E_i}{q}$$

$$\phi_F = \frac{kT}{q}\ln\left(\frac{n_i}{p}\right) \approx \frac{kT}{q}\ln\left(\frac{n_i}{N_A}\right)$$

$$\phi_{Fn} = \frac{kT}{q}\ln\left(\frac{n}{n_i}\right) \approx \frac{kT}{q}\ln\left(\frac{N_D}{n_i}\right)$$

- ϕ_F will be used to define **inversion**.

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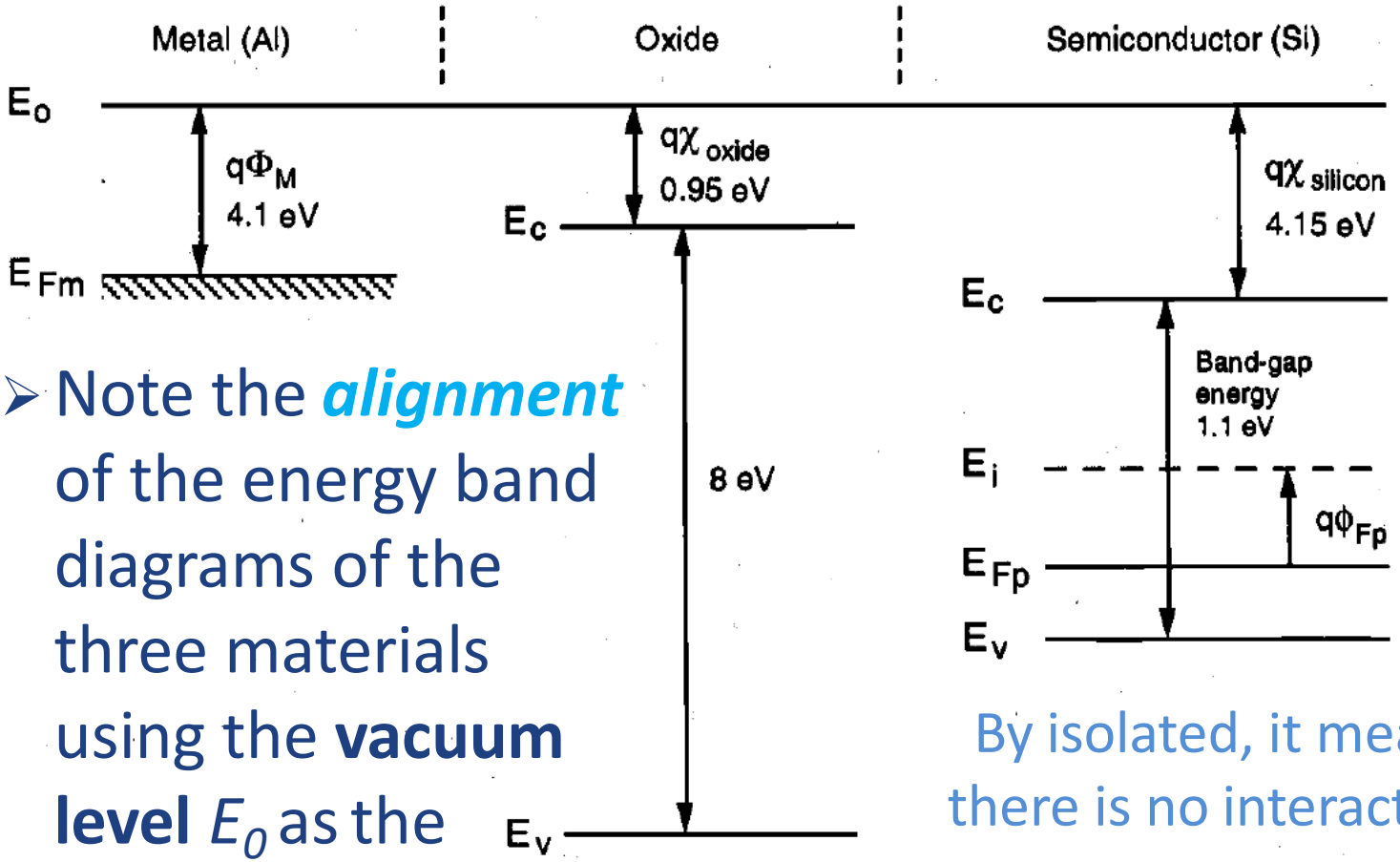
Energy Band Diagram of MOS

(three layers isolated)



- Note the ***alignment*** of the energy band diagrams of the three materials using the **vacuum level** E_0 as the reference.

By isolated, it means there is no interaction.

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Metal's Energy Band Diagram

(work function)

- The energy band diagram of metal consists of the vacuum level E_0 and the Fermi level E_{Fm}.
- The energy difference between E_0 and E_{Fm} is called the **work function $q\Phi$**.
  - It is the energy required for an electron to set free from the metal.

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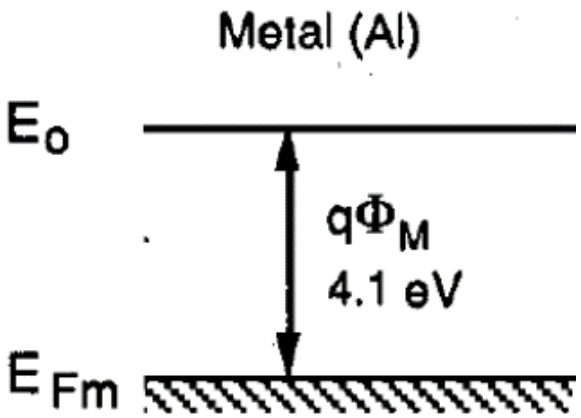

- Note that in metal there are states for electrons at E_{Fm}. In contrast, in semiconductor, E_F is typically in the band gap where there is no state for electrons.

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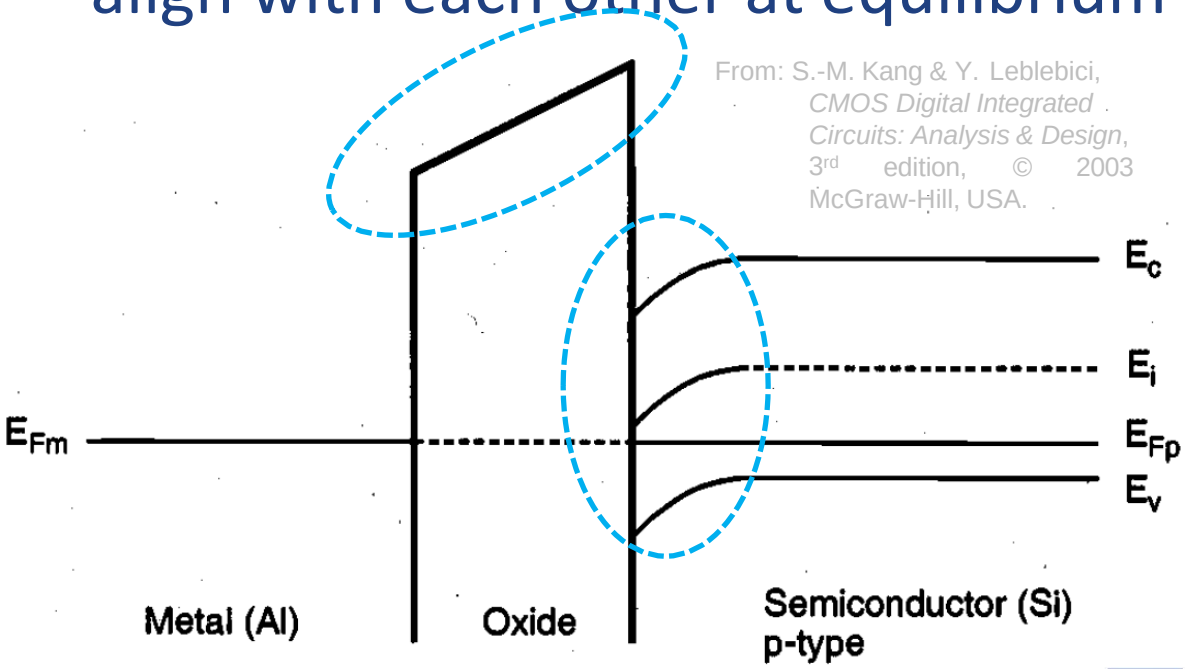
Energy Band Diagram of MOS

(three layers brought together)

- When the three materials are brought together, the **Fermi levels** of the metal and semiconductor align with each other at equilibrium (open-circuit).



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- Note the band bending in the oxide layer and in the surface region of the semiconductor near the oxide.
- What does the band bending mean?

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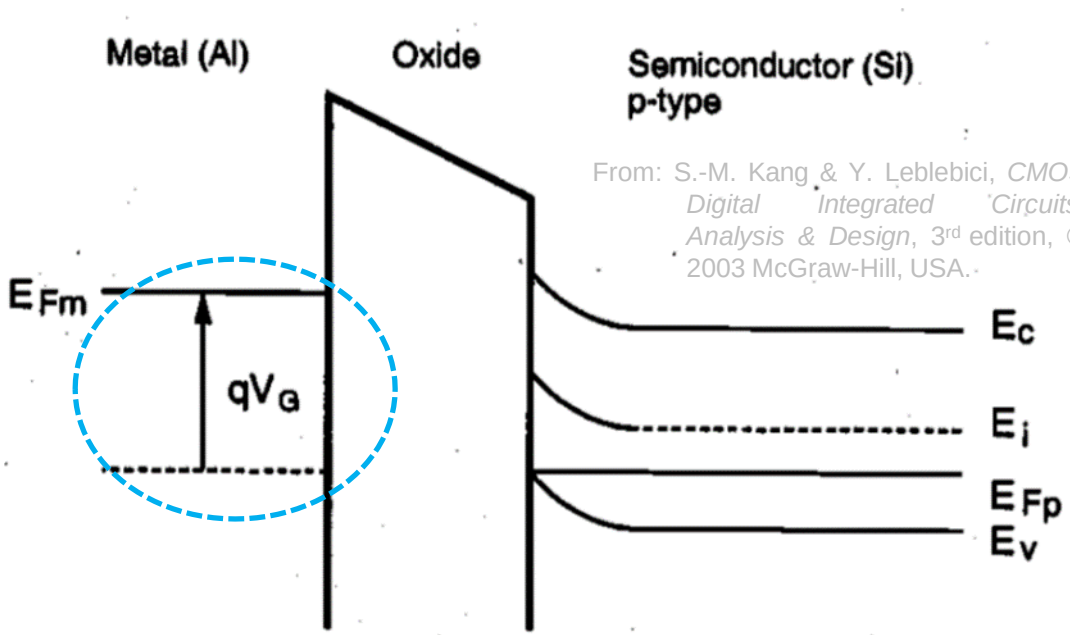
Energy Band Diagram of MOS

(negative voltage at the gate)

- The energy band diagram of the MOS capacitor can be changed by an applied gate voltage V_G (assuming the substrate is grounded i.e. $V_B = 0$).
  - negative $V_G \Rightarrow$ raised *electronic* energy at the gate



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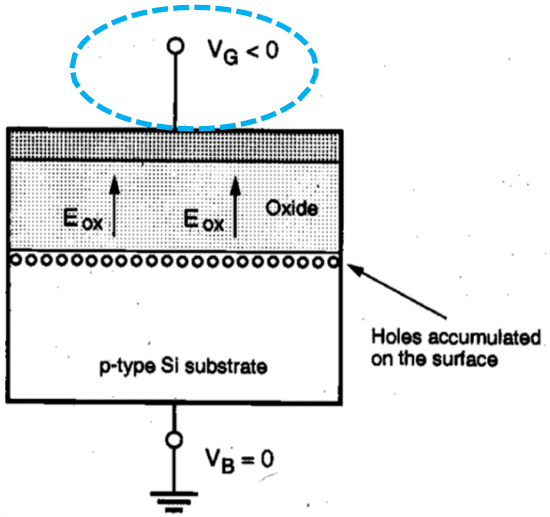

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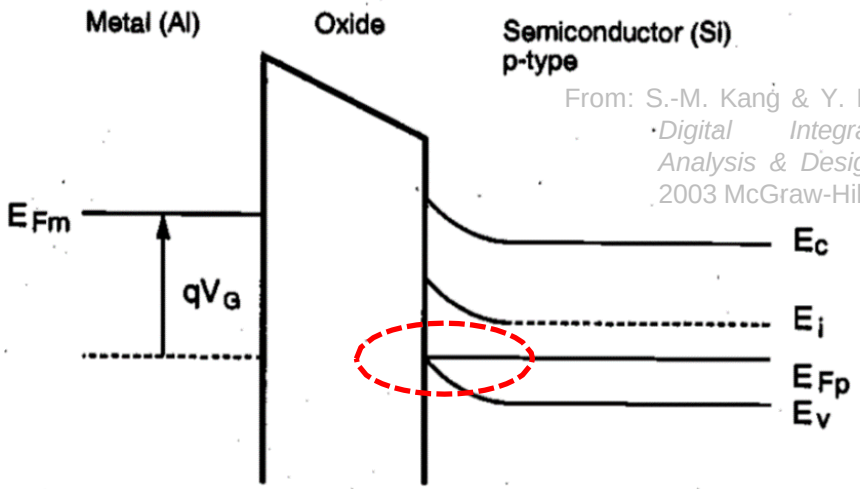
Hole Accumulation

(accumulation mode)

- With the raised *electronic* energy at the gate, it causes band-bending in the oxide and in the surface region of the semiconductor.
  - At the semiconductor surface location, E_{Fp} is close to E_v.
  - The hole concentration increases further at the surface.
  - Holes are ***accumulated*** at the surface.



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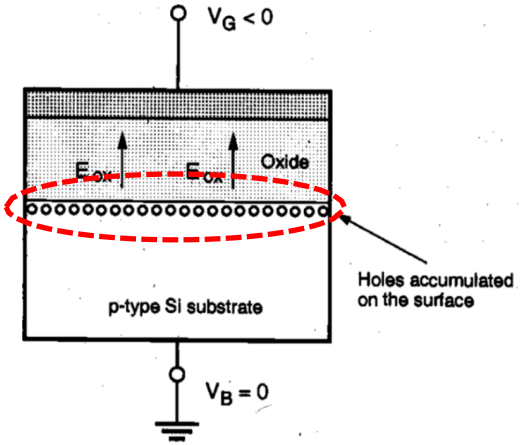

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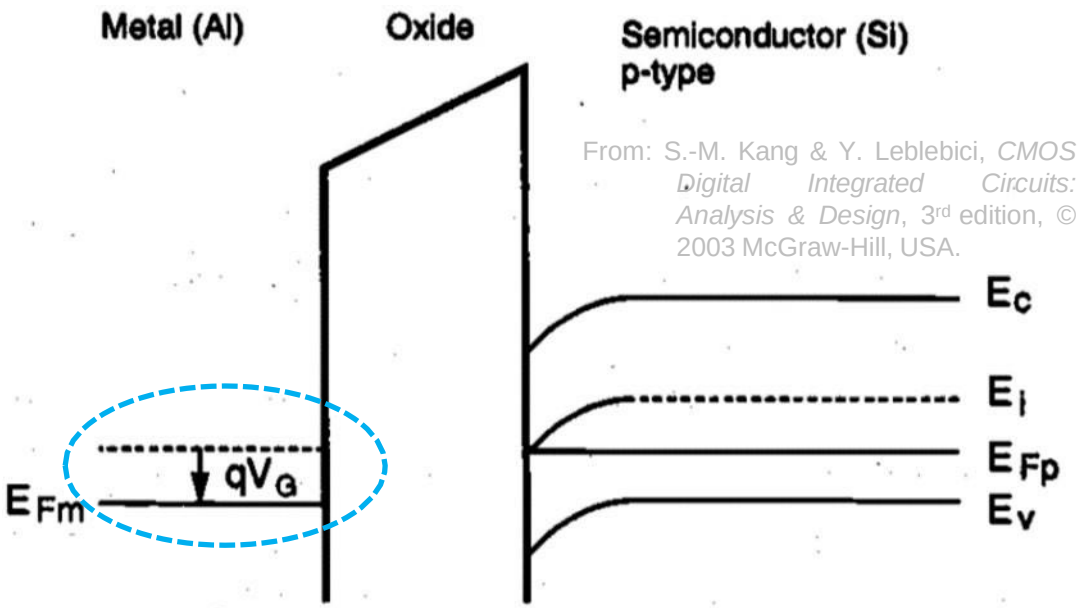
Energy Band Diagram of MOS

(positive voltage at the gate)

- If the gate voltage is positive, the *electronic* energy at the gate is lowered.
  - The metal's Fermi level E_{Fm} is lowered by qV_G from the open-circuit level.



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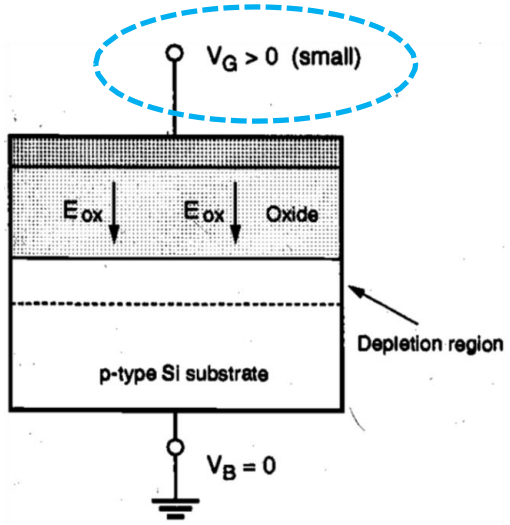

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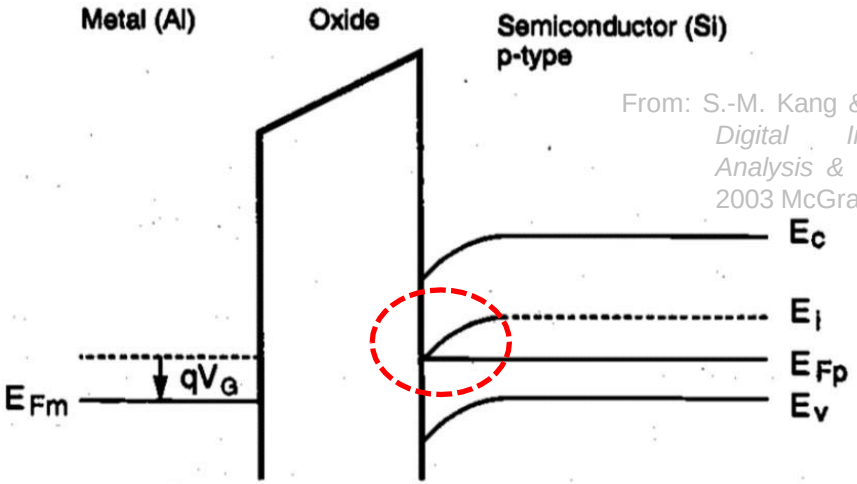
Holes Depleted in Surface Region

(depletion mode)

- With the *electronic* energy at the gate lowered, it also causes band-bending in the oxide and in the surface region of the semiconductor.
  - At the semiconductor surface location, $E_{Fp} \approx E_{Fi}$.
  - The hole concentration decreases at the surface location.
  - Holes are ***depleted*** from the surface.



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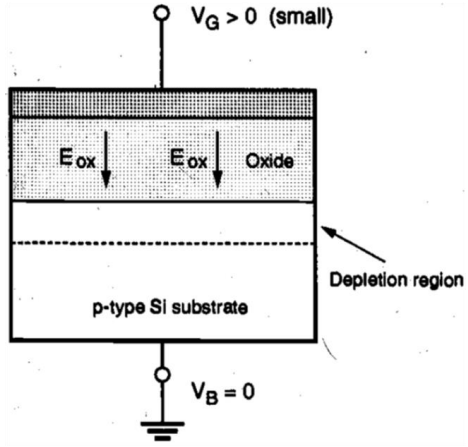

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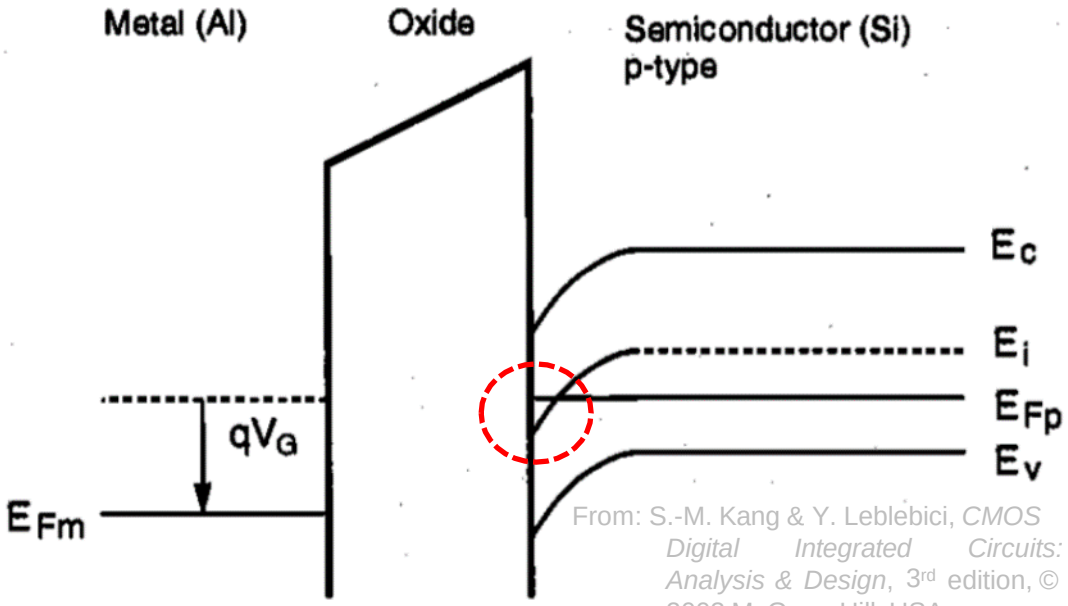
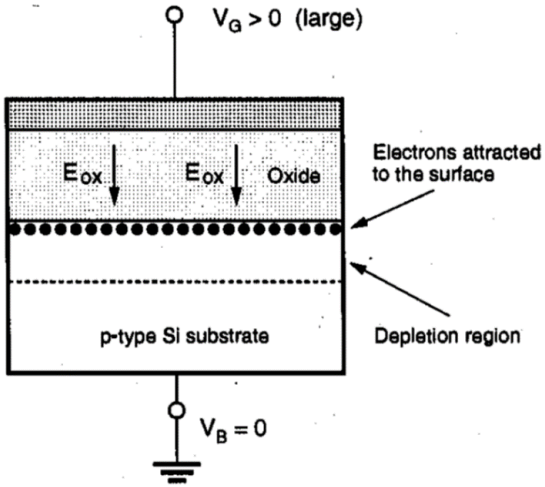
Energy Band Diagram of MOS

(larger positive voltage at the gate)

- When the positive voltage at the gate is even larger, there is more band bending such that E_{Fp} is now above E_{Fi}.
  - What is the implication?





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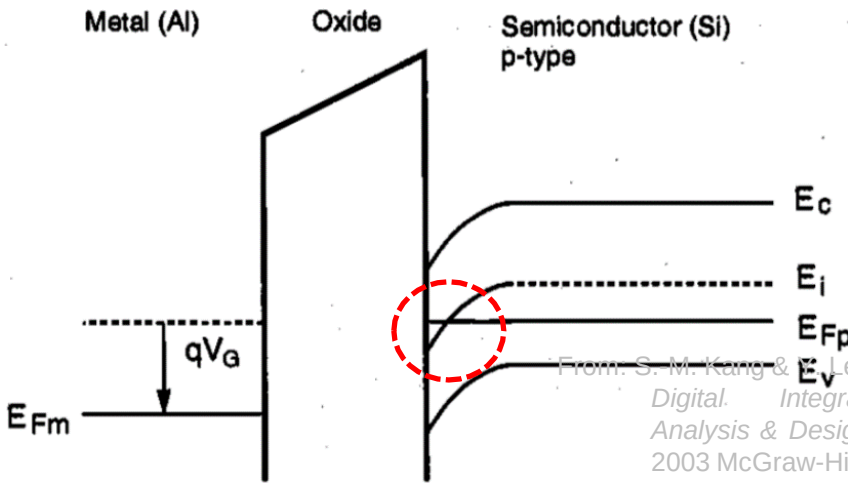
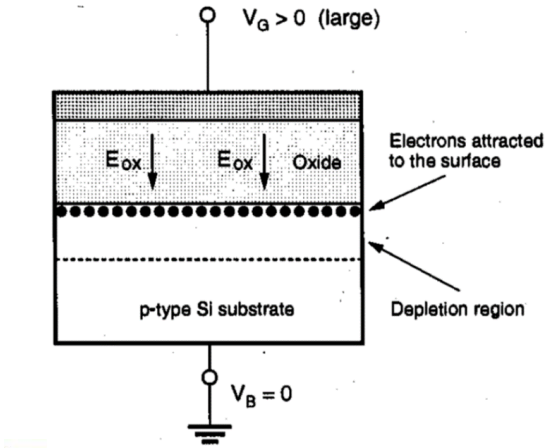
"Minority" Carriers at Surface

(weak inversion)

- With E_{Fp} above E_{Fi} in the surface region of the semiconductor, the electrons as the "minority" carriers in the *p*-type substrate has even higher concentration than the holes.
  - There is ***inversion*** of **charge carriers** in the surface region of the semiconductor.





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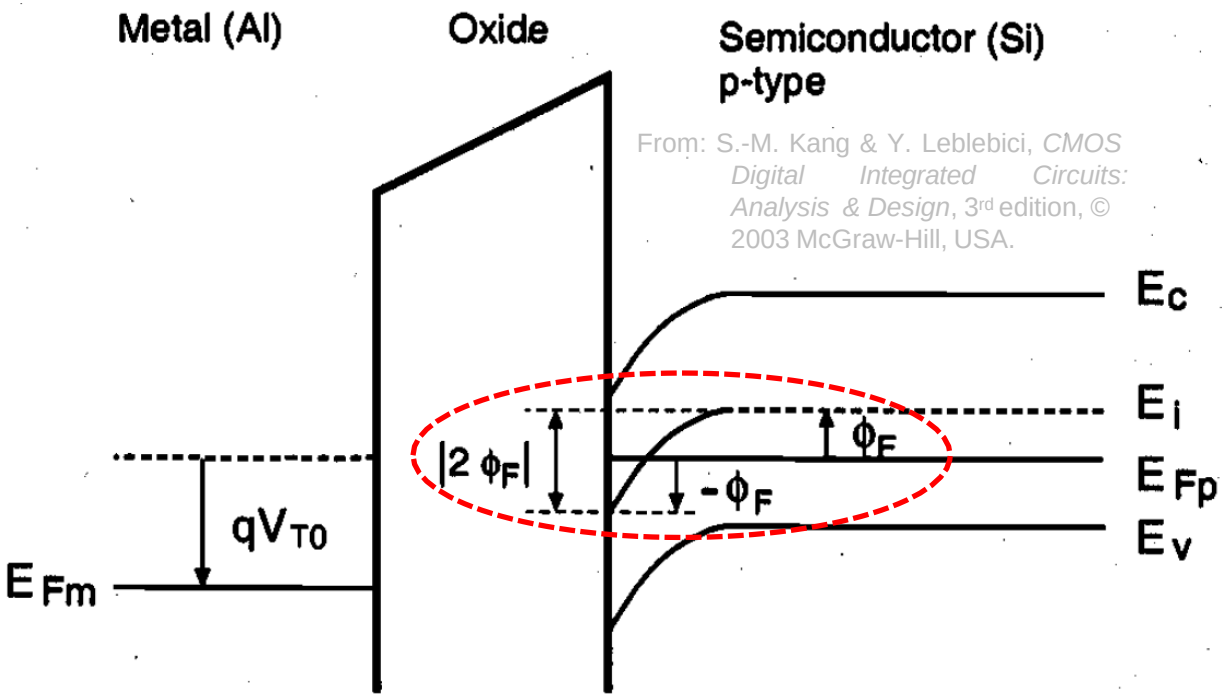
"Minority" Carriers at Surface

(strong inversion)

- With a large enough positive V_G, E_{Fp} is now one ϕ_F above E_{Fi}. What is the implication?



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- It is described as the **surface potential** $\phi_S = |2\phi_F|$
- $n_S = p_p \approx N_A$
- $n_p \approx n_i^2/N_A$

- In this situation, it is called **strong inversion**.

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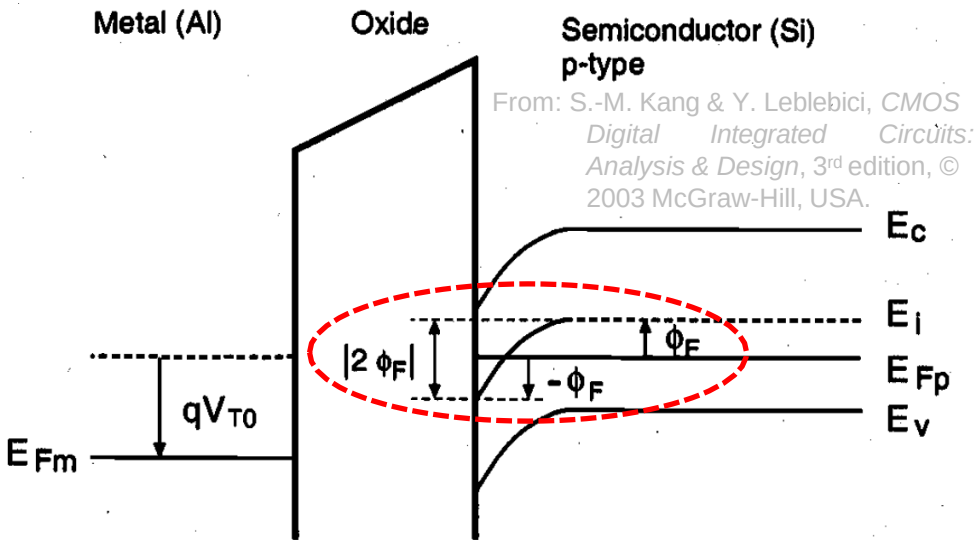
Threshold Voltage

(gate voltage for strong inversion)

- The positive V_G that causes the band bending near the surface of the ***p***-type substrate to have $|\phi_S| = |2\phi_F|$ is called the **threshold voltage** V_T.
  - Do not confuse V_T with the thermal voltage k_BT/q.
  - V_T is typically positive for a *p*-type substrate.



- V_T is typically negative if the MOS structure has an *n*-type substrate. (Do you know why?)

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Threshold Voltage

(three components)

- There are typically three components in the **threshold voltage** V_T corresponding respectively the three changes in the energy band diagram.

$$V_T = V_{FB} + 2\phi_F + \frac{\sqrt{2qN_a\varepsilon_{Si}(2\phi_F)}}{C_{ox}}$$

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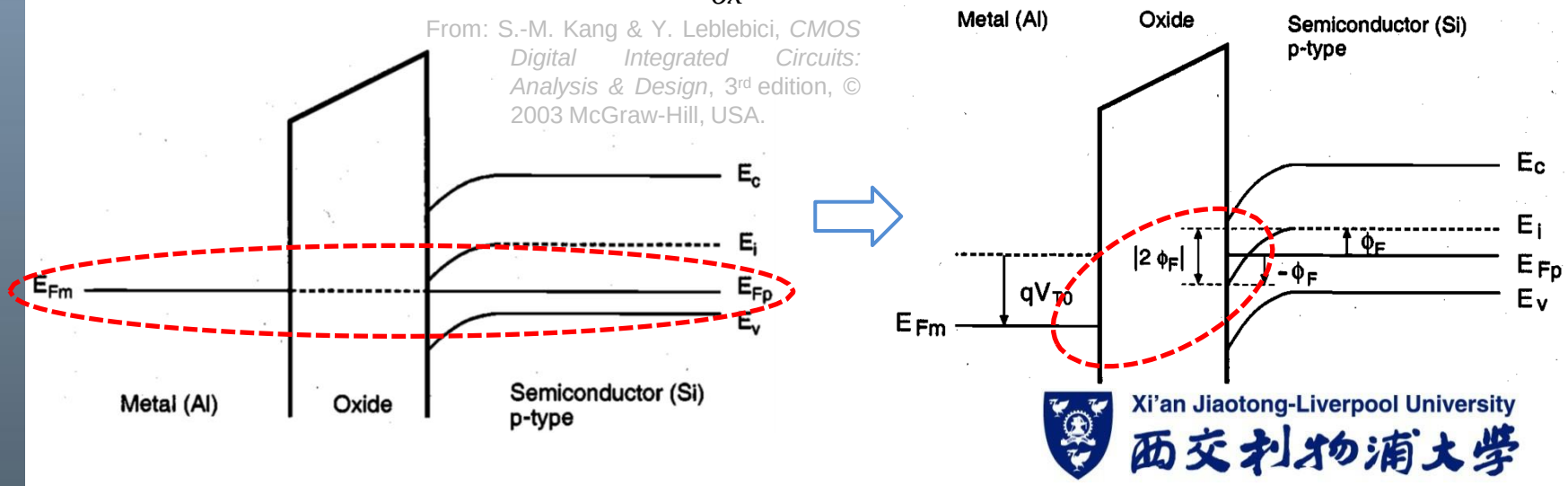

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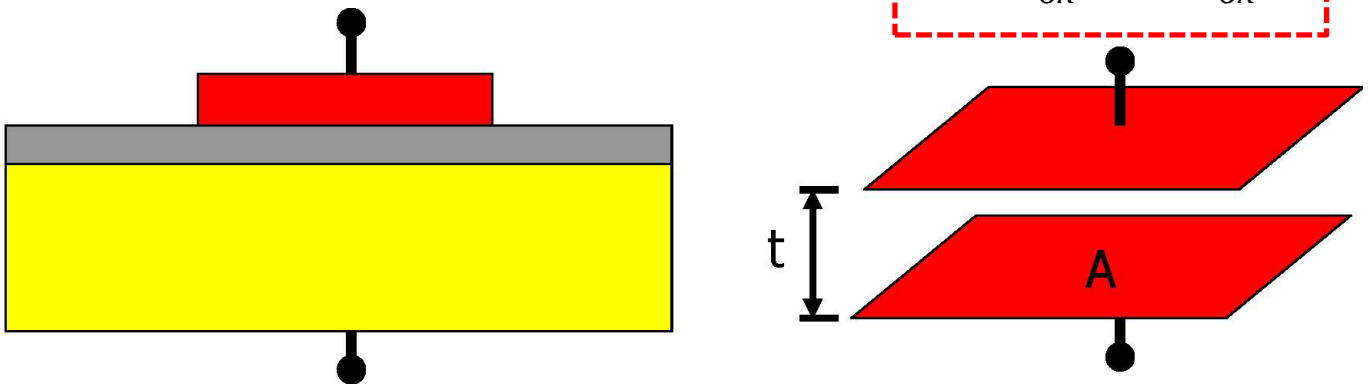
Capacitance of MOS Structure

(similar structure to parallel-plate capacitor)

- Apparently, the MOS capacitor has a structure of a *parallel-plate* capacitor.

$$C = \frac{\varepsilon A}{t_{ox}} = \frac{\varepsilon_r \varepsilon_0 A}{t_{ox}}$$



  - $\varepsilon_{r,SiO2} = 3.9$, $\varepsilon_{r,Si} = 11.9$, $\varepsilon_o = 8.85 \times 10^{-14}$ F/cm

- The **MOS capacitor** has different capacitance behaviour.
  - voltage dependence

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Capacitance of MOS Structure

(voltage dependence)

- The voltage dependence of the MOS capacitance is because of the change of charges in the surface region of the substrate as the gate voltage varies.
- In the **accumulation** and **strong inversion** modes, there are respectively charge layers of holes and electrons right underneath the oxide layer;
- The MOS capacitance in these two modes can be estimated by the parallel-plate capacitance formula:

$$C = \frac{\varepsilon A}{t_{ox}} = \frac{\varepsilon_r \varepsilon_0 A}{t_{ox}} \quad \Rightarrow \frac{C}{A} = C_{ox} = \frac{\varepsilon_r \varepsilon_0}{t_{ox}}$$

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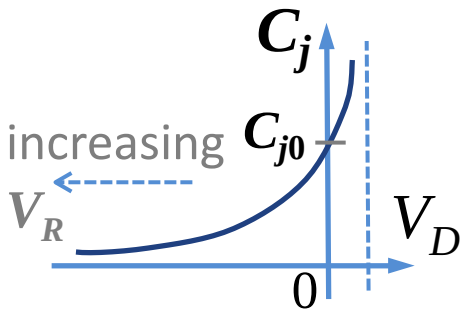
Capacitance of MOS Structure

(depletion capacitance)

- In the **depletion mode**, there is neither a layer of electrons nor a layer of holes right underneath the insulating oxide layer.
- Instead, there is a **depletion region** in which there is a layer of fixed dopant ions (a **space-charge layer**).
  - This is similar to the **depletion region** in the reverse-biased ***p-n* junction**.



$$C_j = \frac{C_{j0}}{\sqrt{1+\frac{V_R}{V_{bi}}}}$$

- The **depletion capacitance** decreases as the magnitude of the voltage increases.

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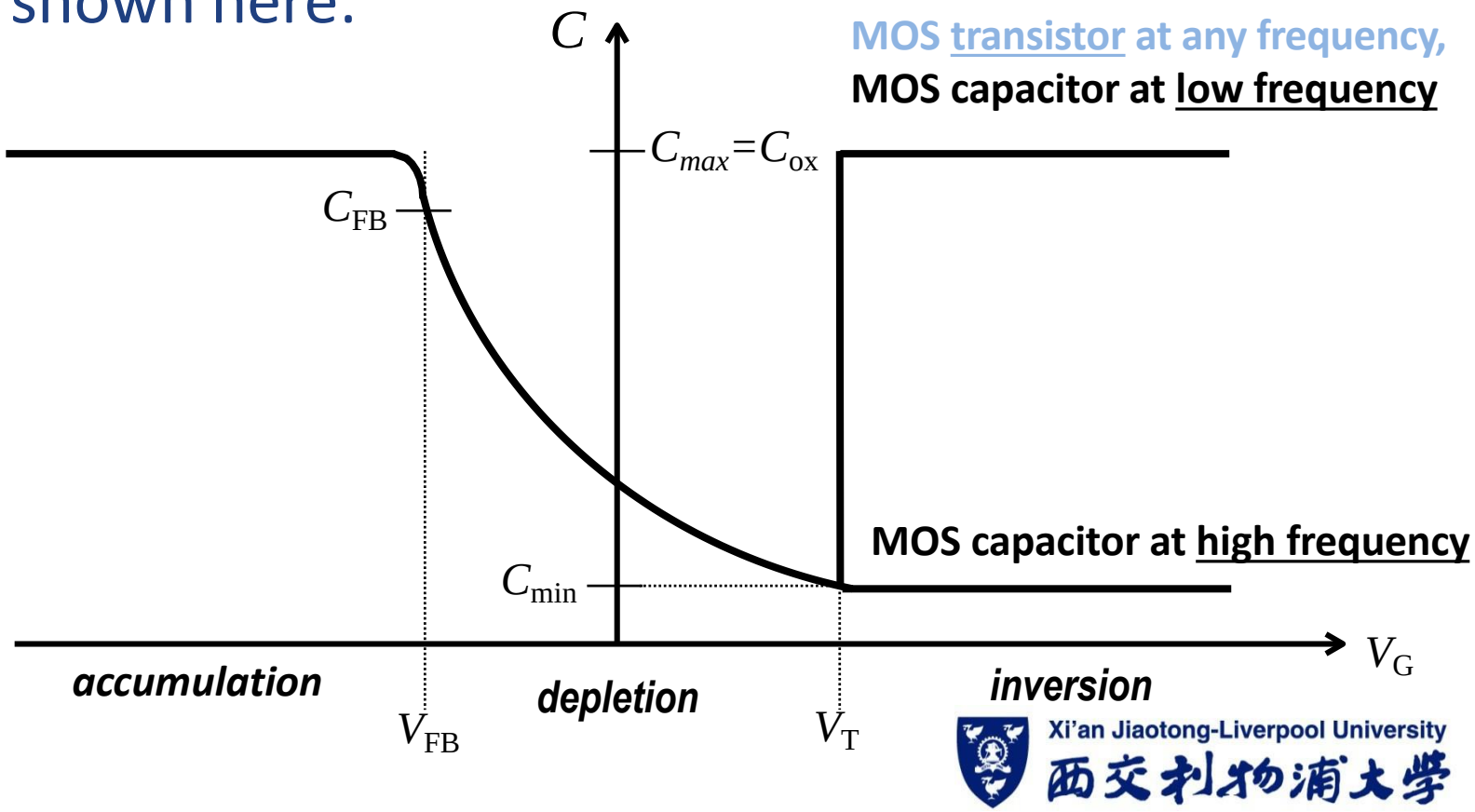
Capacitance of MOS Structure

(C-V curves)

- The *voltage-dependent* **MOS capacitance** of is shown here:



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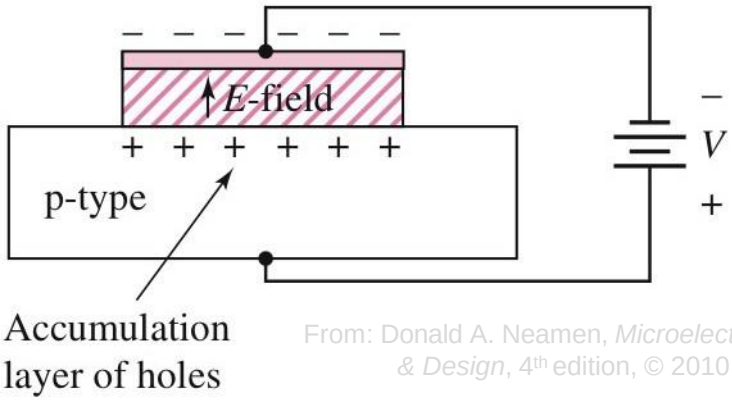
MOS Capacitor – qualitative summary

(accumulation of majority carriers)

- We learn about the **MOS capacitor** with three **operation regions**, depending on the voltage applied to the gate (with the substrate grounded): **accumulation**, **depletion**, and **inversion** (**weak & strong inversion**).
  - **accumulation**: **majority carriers** of the substrate ***accumulate*** near the surface (oxide-semiconductor interface), with the carrier concentration even higher than the equilibrium concentration.



From: Donald A. Neamen, *Microelectronics: Circuit Analysis & Design*, 4th edition, © 2010 McGraw-Hill, USA.

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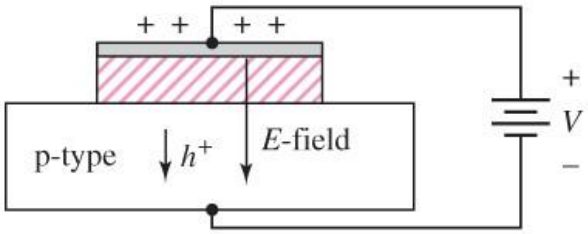
MOS Capacitor – qualitative summary

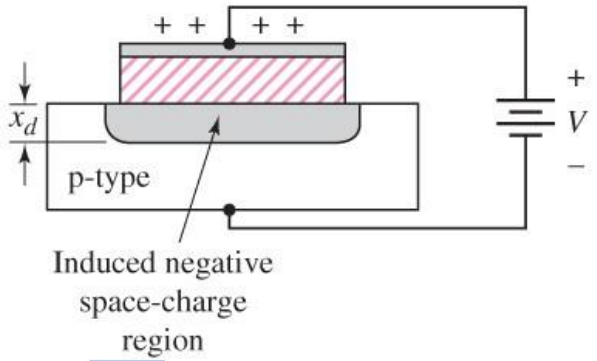
(depletion region & width)

- **depletion**: **majority carriers** of the substrate are ***depleted*** beneath the surface, resulting in a region without any mobile carriers but fixed dopant ions in space; it's called a **depletion region** or **space-charge** region.
- This is similar to the reverse-biased ***p-n*** junction.

$$x_d = \sqrt{\frac{2\varepsilon_{Si}\left|\phi_s - \phi_F\right|}{qN_a}}$$

x_d : depletion layer thickness





p-n junction:

$$W_0 = \sqrt{\frac{2\varepsilon_{Si}\left(N_a + N_d\right)\left|V_{bias} - V_{bi}\right|}{eN_aN_d}}$$

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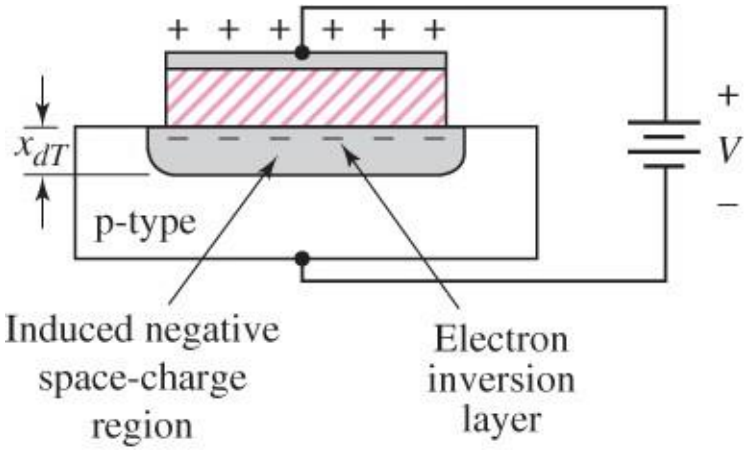
MOS Capacitor – qualitative summary

(strong inversion)

- **inversion**: a very thin charge layer of **minority carriers** is formed right beneath the surface of the semiconductor when an appropriate gate voltage is applied.



From: Donald A. Neamen, *Microelectronics: Circuit Analysis & Design*, 4th edition, © 2010 McGraw-Hill, USA.

- When the **minority carrier concentration** of the **inversion layer** is the same as the majority carrier concentration in the substrate, it is called **strong inversion**.

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MOS Capacitor – qualitative summary

(inversion & threshold voltage)

- At ***strong* inversion**, the corresponding gate voltage is called the **threshold voltage V_T**:

$$V_T = V_{FB} + 2\phi_F + \frac{\sqrt{2qN_a\varepsilon_{Si}(2\phi_F)}}{C_{ox}}$$

- When the minority carrier concentration in the inversion layer is smaller than the majority carrier concentration, it is called ***weak* inversion**.
- In ***weak* inversion**, the gate voltage is slightly below the **threshold voltage V_T**.
- This accounts for the **sub-threshold characteristics** of the MOS transistor.

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MOS Capacitor – qualitative summary

(2-terminal device)

- If the substrate is not connected to ground but with a biased voltage V_B, V_T needs to be modified as follows (for MOSFET):

$$V_T = V_{FB} + 2\phi_F + \frac{\sqrt{2qN_A\varepsilon_{Si}(2\phi_F - V_B)}}{C_{ox}}$$

- The MOS capacitor is a two-terminal device and it is not very useful by itself in digital ICs.
  - two electrodes: **gate** (denoted by G) & **substrate** (or called **bulk**/**body**) (denoted by B)
  - The MOS capacitor is however useful in analogue ICs in some circuits as well as CCD image sensors.
  - The ***p*-*n*** junction is also a 2-terminal device.

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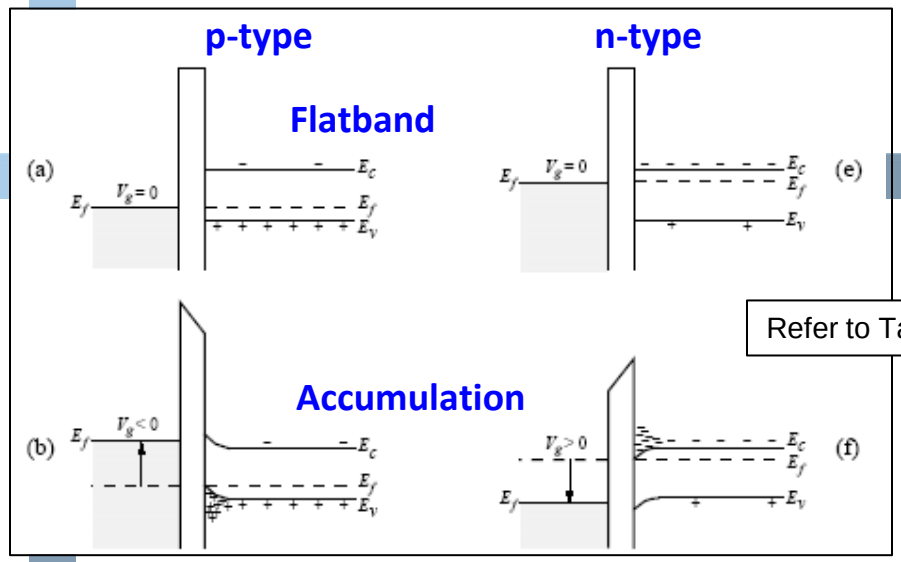
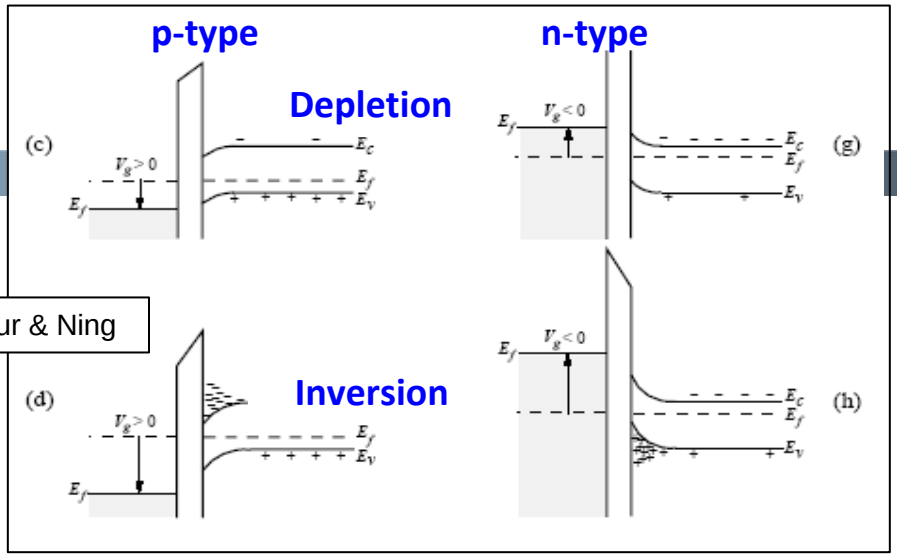
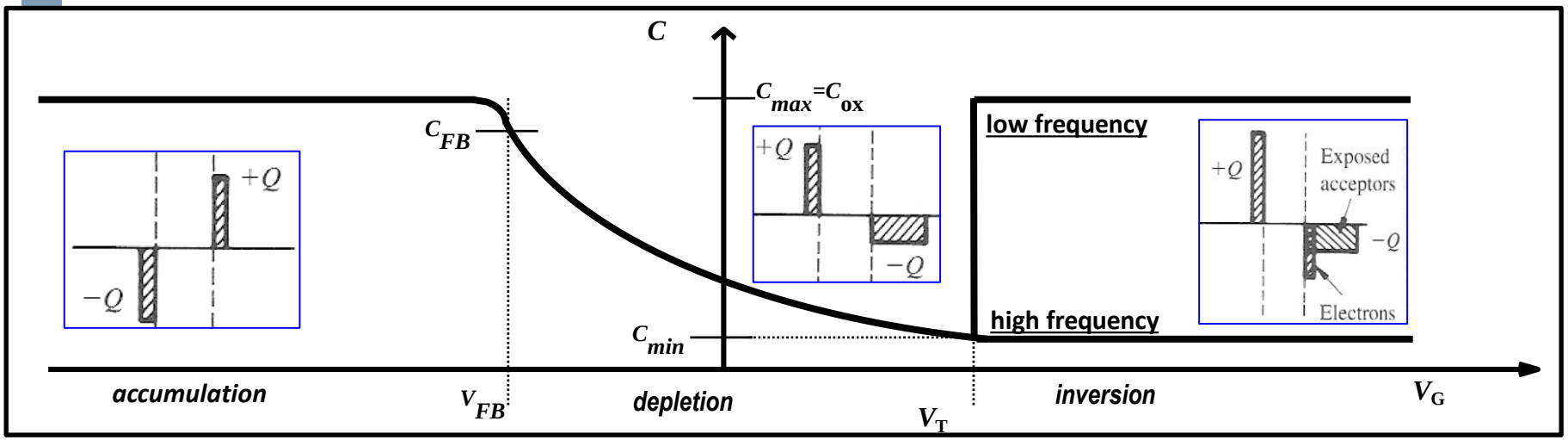
Summary: MOS Capacitor





Refer to Taur & Ning

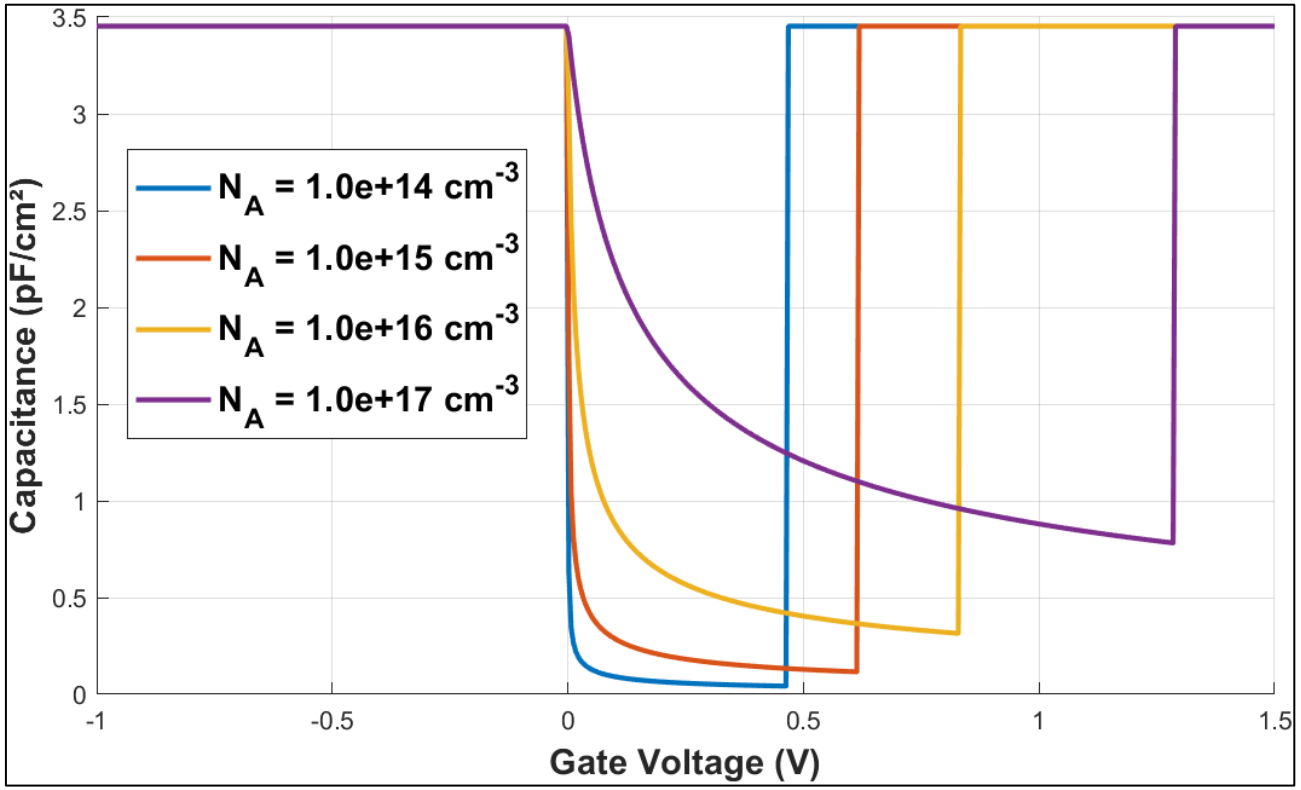


$$V_G = V_{FB} + \phi_s + \frac{\sqrt{2qN_a\varepsilon_{Si}(\phi_s)}}{C_{ox}}$$

$$V_T = V_{FB} + 2\phi_F + \frac{\sqrt{2qN_a\varepsilon_{Si}(2\phi_F)}}{C_{ox}}$$

ϕ_F = equilibrium Fermi level E_f

Impact of Doping on Low Frequency C-V of MOS Capacitor (p-type)



Observation:

1. ↑ N_A ⇒ ↑ V_g range of depletion region.
2. ↑ N_A ⇒ ↑ C in depletion region

Link to the script for calculating capacitance-voltage (C-V): https://core.xjtlu.edu.cn/mod/folder/view.php?id=38872

Depletion Mode: $V_{FB} < V_G < V_T$

Gate voltage (V_G)

$$V_G = V_{FB} + 2\phi_S + \frac{\sqrt{2qN_a\varepsilon_{Si}(\phi_S)}}{C_{ox}}$$

Equilibrium Fermi level (ϕ_F)

$$\phi_F = \frac{kT}{q}\ln\left(\frac{n_i}{p}\right) \approx \frac{kT}{q}\ln\left(\frac{n_i}{N_A}\right)$$

Capacitance (C)

$$C_{dep} = \frac{\varepsilon_s}{x_d}$$

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}}$$

Threshold voltage (V_T)

$$V_T = V_{FB} + 2\phi_F + \frac{\sqrt{2qN_a\varepsilon_{Si}(2\phi_F)}}{C_{ox}}$$

Depletion width (X_d)

$$x_d = \sqrt{\frac{2\varepsilon_{Si}|\phi_s|}{qN_a}}$$