Integrated Electronics & Design

IC Fabrication Techniques

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Reading: Chapter 4.0, 4.2, 4.3.1

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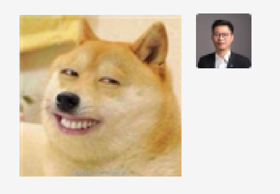
https://www.xjtlu.edu.cn/en/departments/academic-departments/electrical-and-electronic-engineering/staff/chun-zhao

IC Fab. Tech. OUTLINE

- Thin Film Formation
- Photolithography and Etching
- Doping
- IC Resistor
- Sheet Resistance
- Diode
- nMOSFET: Process Flow
- nMOSFET: Fab. and Layout
- nMOSFET: Layout Rules

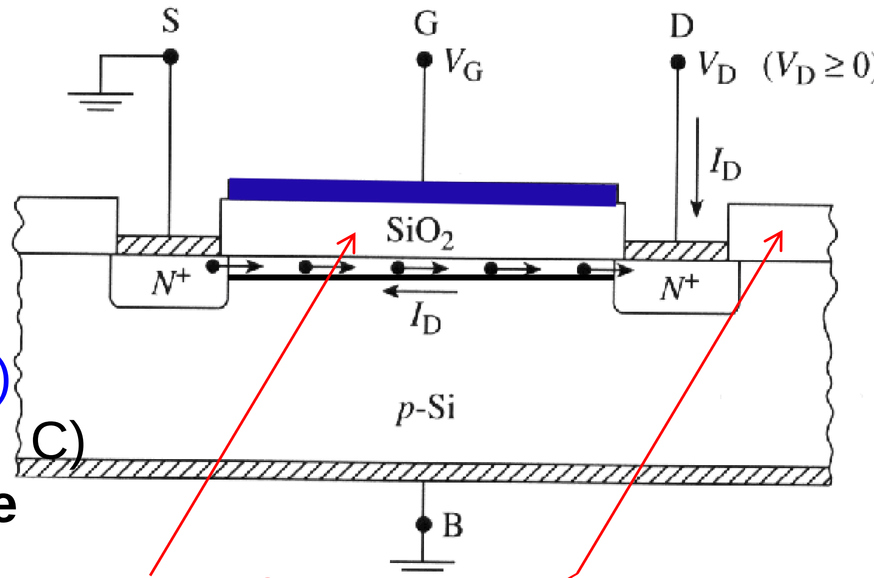


Thin film formation

- Thermal oxidation
- CVD
- PVD

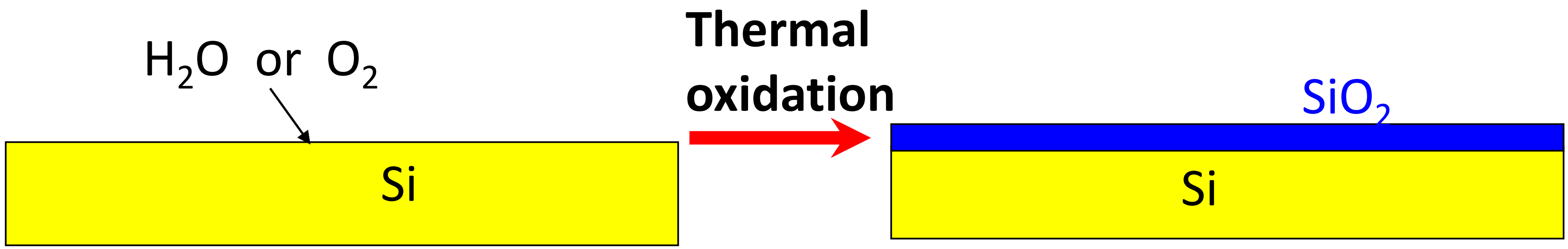
Thermal oxidation

- **Dry oxidation**
  - $Si + O_2 \rightarrow SiO_2$ (900-1200° C)
  - 700nm oxide: 10 hours (1200° C)
  - Good oxide quality: **gate oxide**
- **Wet oxidation**
  - $Si + H_2O \rightarrow SiO_2 + 2H_2$ (900-1200° C)
  - 700nm oxide: 0. 65 hours (1200° C)
  - Poor oxide quality: **field oxide/diffusion barrier** (diffusion mask)

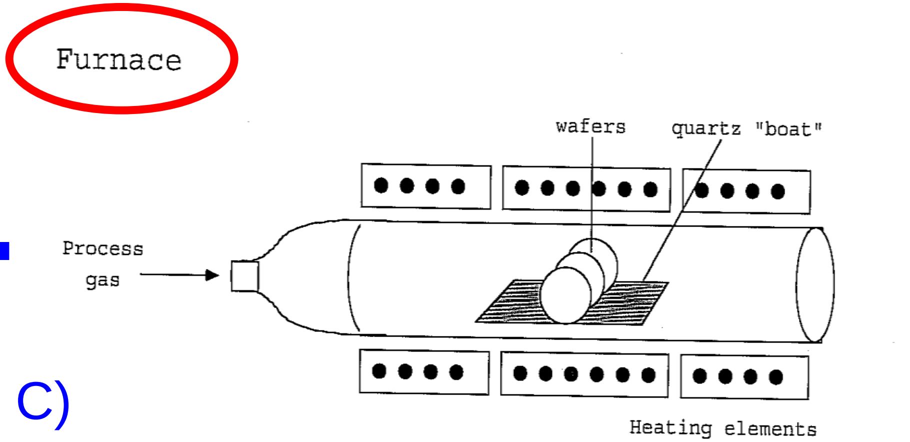


Gate oxide

Field oxide



Thermal oxidation



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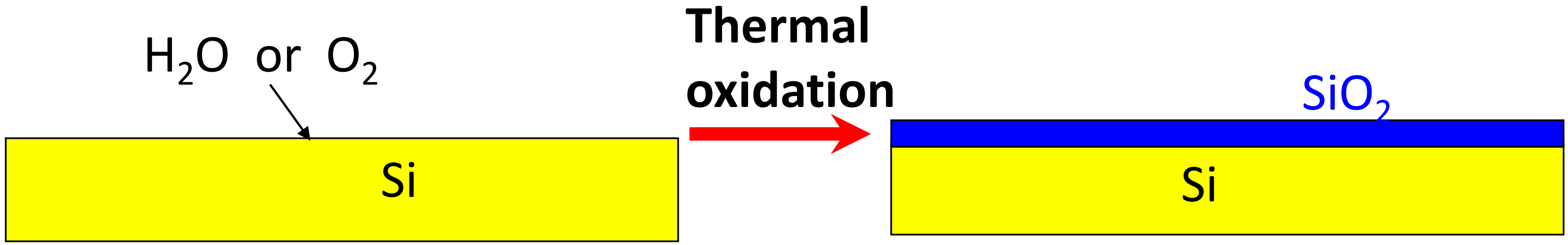
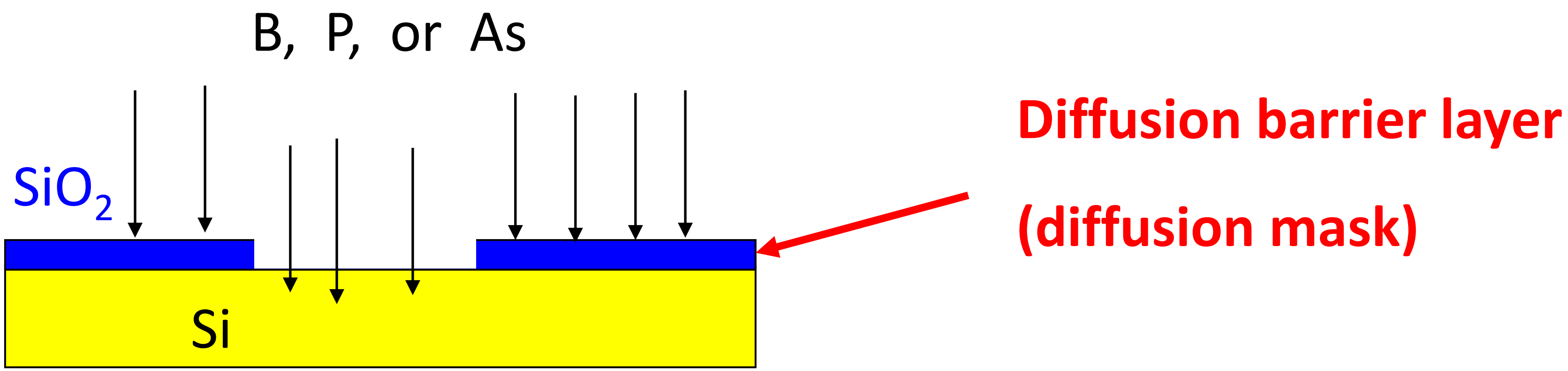
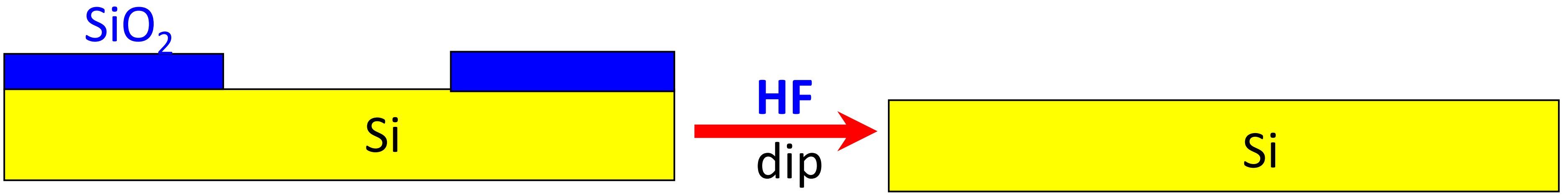


Thermal SiO_2 Properties

- (1) SiO_2 is a good diffusion mask for common dopants



- (2) Very good etching selectivity between Si and SiO_2.



Thin film formation

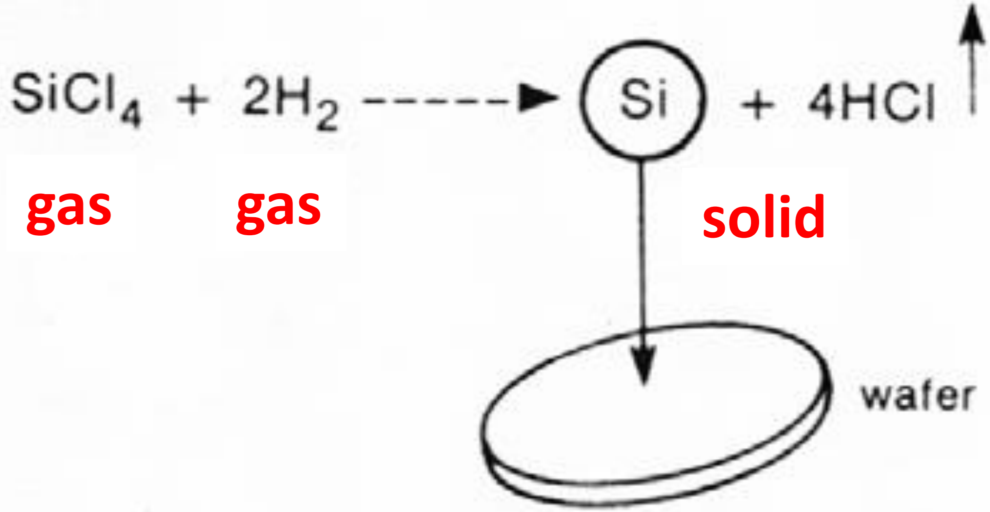
- Thermal oxidation
- CVD
- PVD

Chemical Vapor Deposition (CVD)

- Thin film formation from **vapor phase reactants**. Deposited films range from metals to semiconductors to insulators.

- An **essential process step** in the manufacturing of microelectronic devices. High temperatures and low pressures are the most common process conditions, but are not necessary.

- All CVD involves using an energy source to break reactant gases into reactive species for deposition.



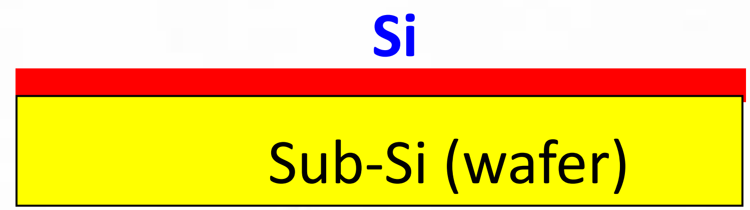


Figure 12.4 Chemical vapor deposition of silicon from silicon tetrachloride.

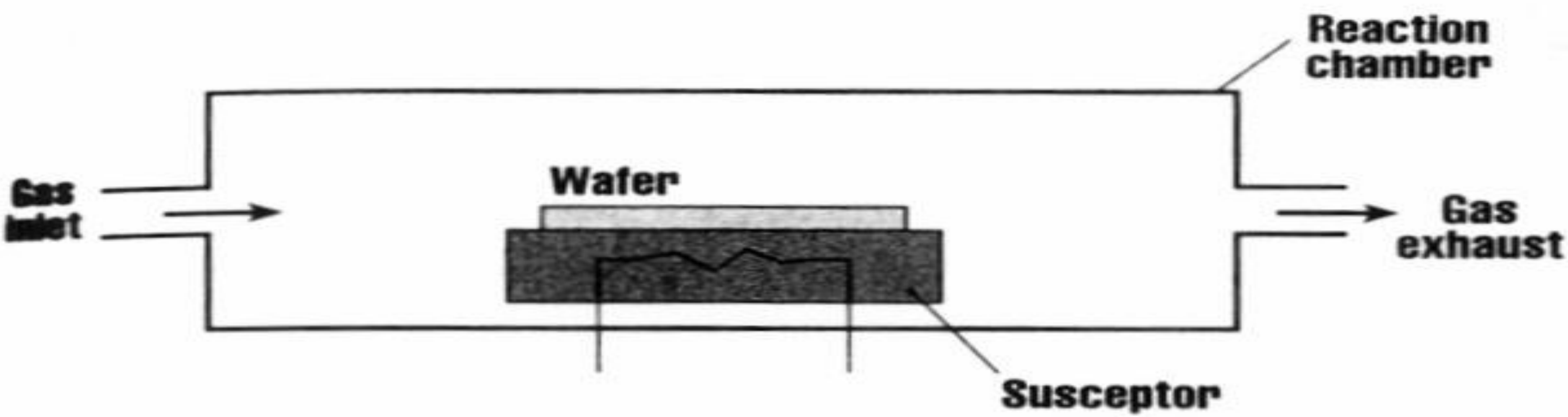
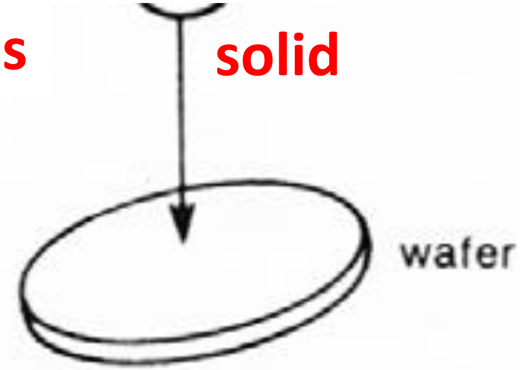


Figure 13-1 A simple prototype thermal CVD reactor.

$SiH_4 + O_2 \rightarrow SiO_2 + 2H_2$

gas gas solid



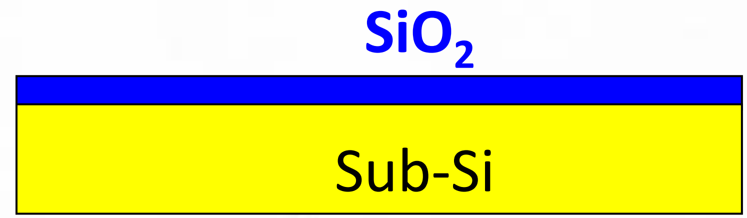


Figure Chemical vapor deposition of silicon from silicon tetrachloride.

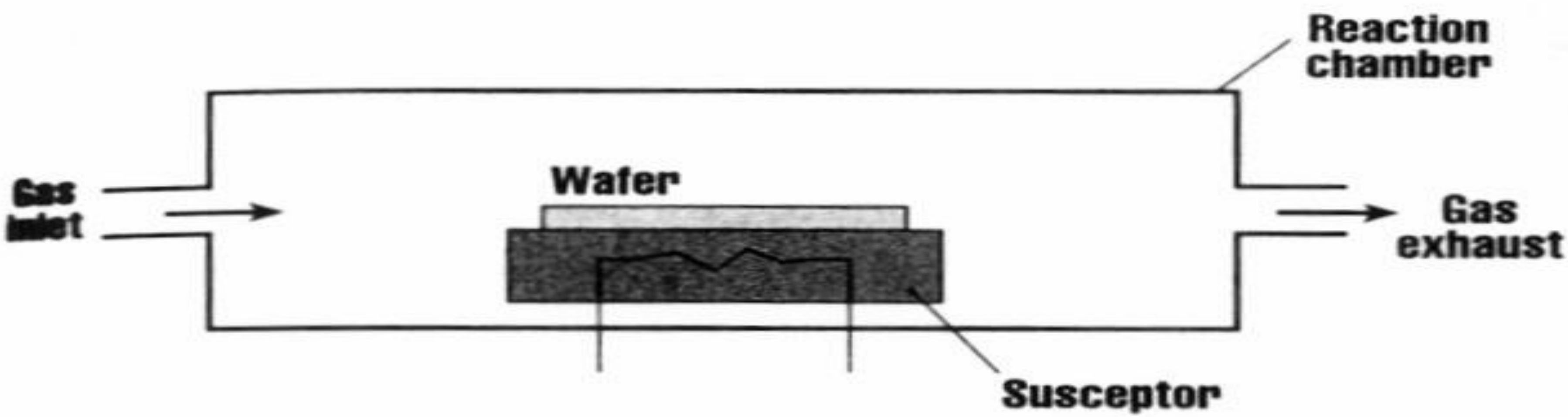


Figure A simple prototype thermal CVD reactor.

Examples of CVD

- Metals/Conductors – W, Al, Cu, doped **poly-Si**
- Insulators (dielectrics) – BPSG, Si_3N_4, **SiO_2**
- Semiconductors – **Si**, Ge, InP, GaAsP

$$\boxed{SiCl_4 + 2H_2 \rightarrow Si + 4HCl}$$

$$\boxed{SiH_4 + O_2 \rightarrow SiO_2 + 2H_2}$$

Thin film formation

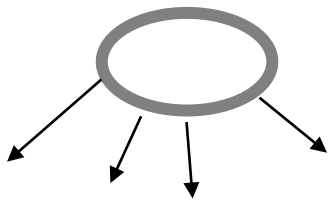
- **Thermal oxidation**
- **CVD**
- **PVD**

Physical Vapor Deposition (PVD)

- No chemical reaction involved
  - Evaporation
  - Sputtering
  - …
- Used to form metal films or metal oxide films, such as
  - Al
  - HfO_2
  - …

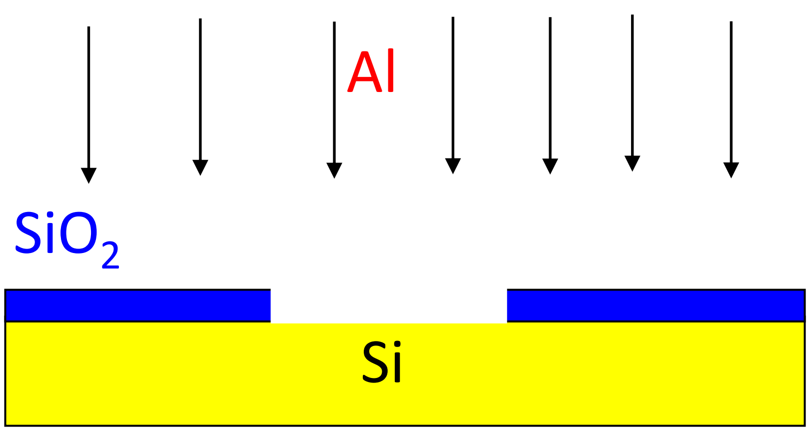
Physical Vapor Deposition - Evaporation

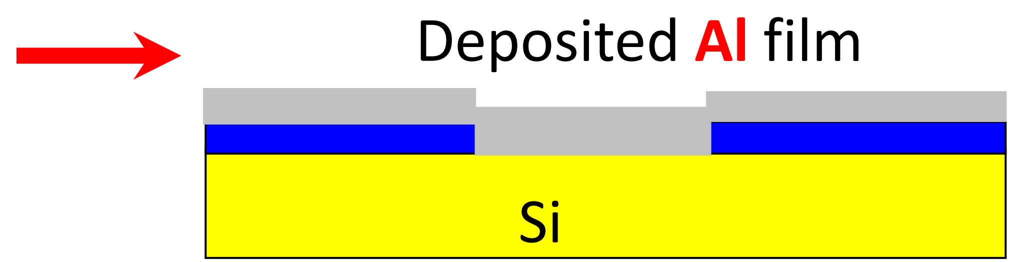
Al ring



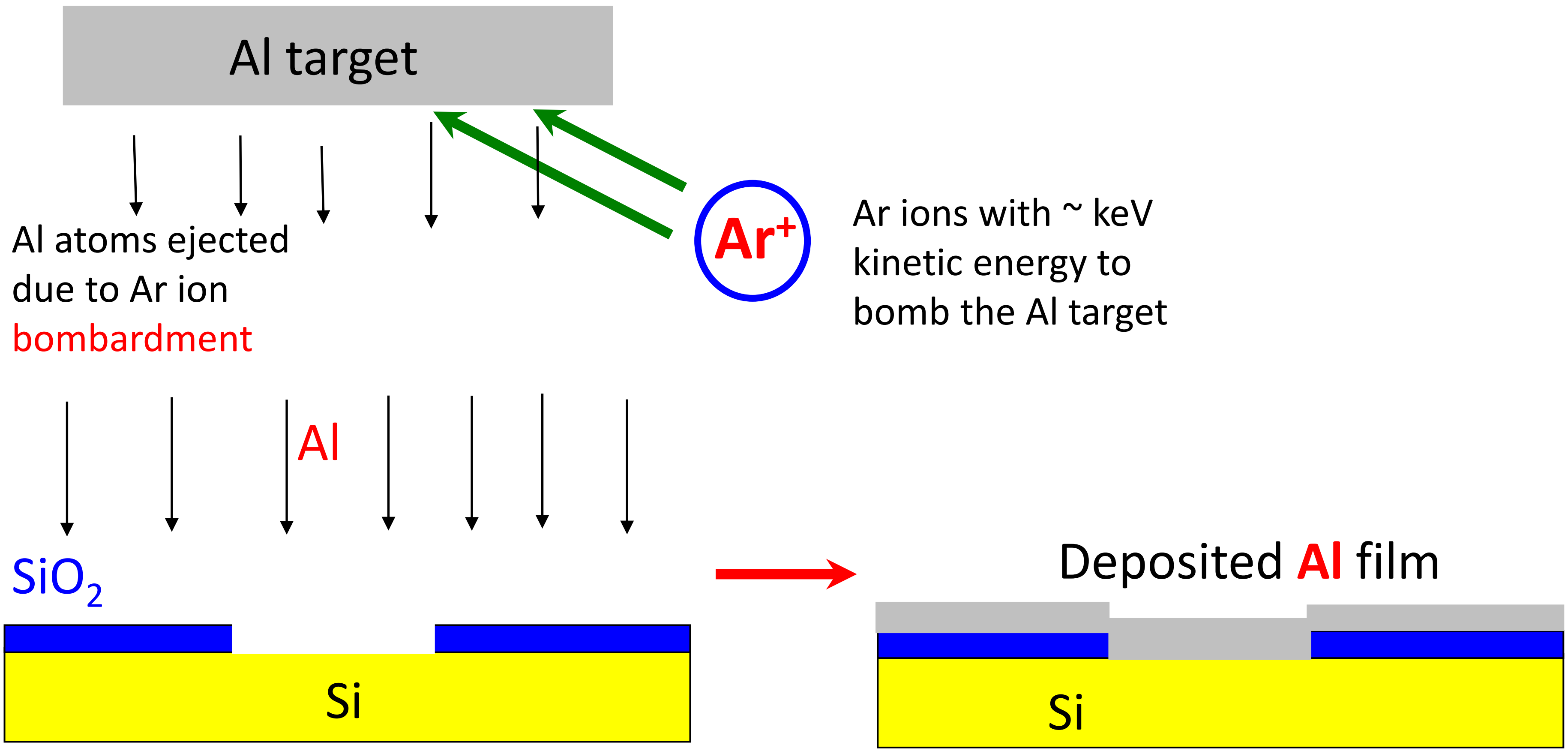
Evaporation Al
(T_{source} >>$T_{boiling}$ of Al , 700^{O}C)

Boiling point
H_2O: 100^{o}C
Al: 660^{o}C

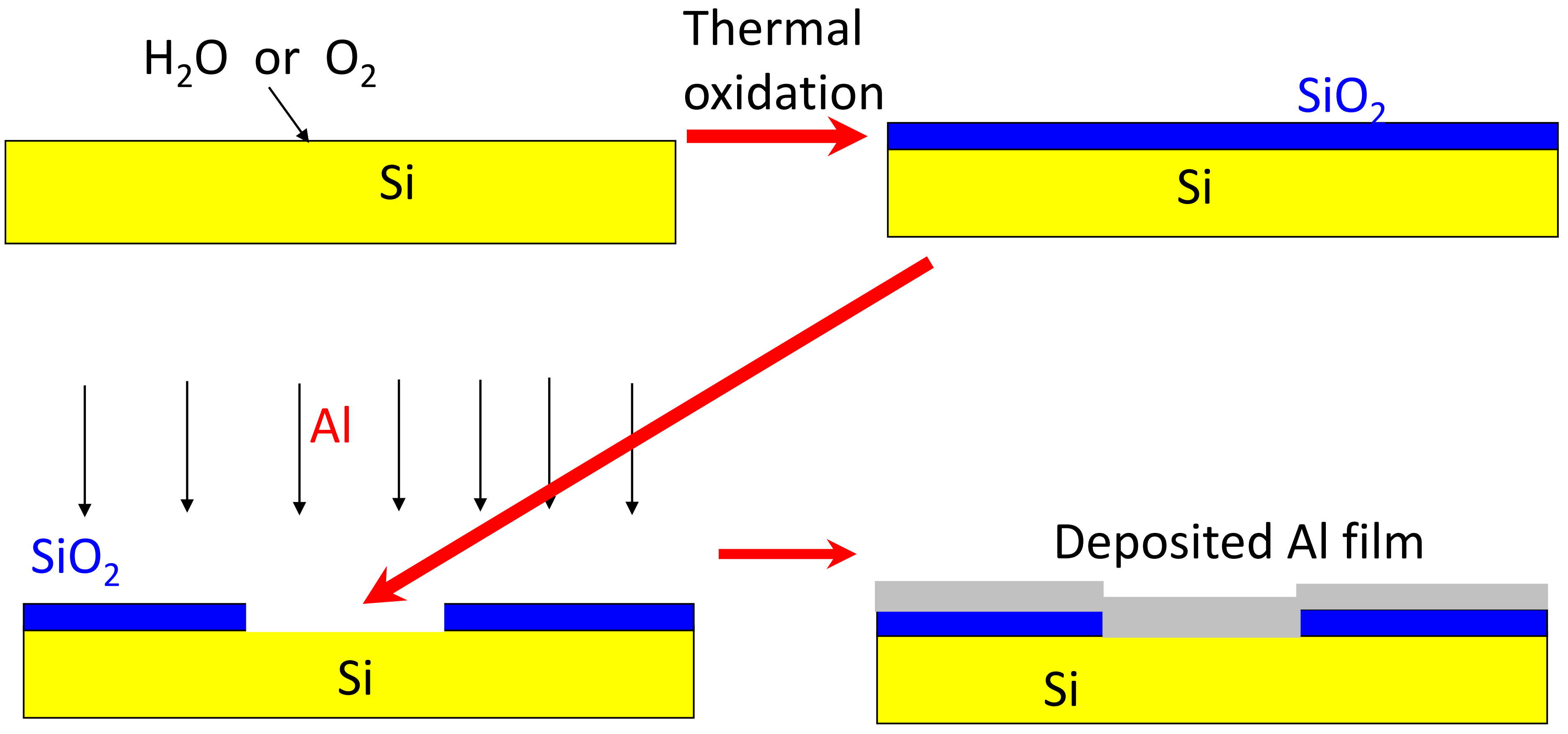




Physical Vapor Deposition - Sputtering



Physical Vapor Deposition - Sputtering



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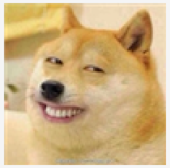
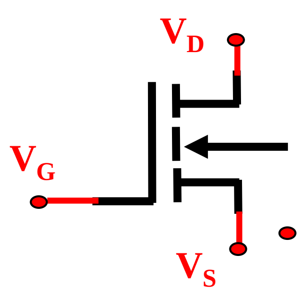
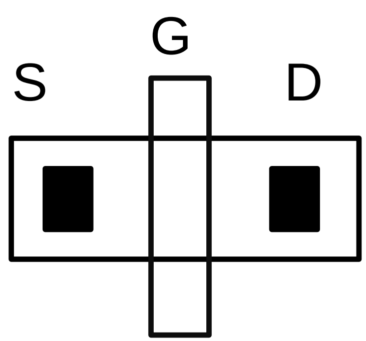



Photolithography & Etching

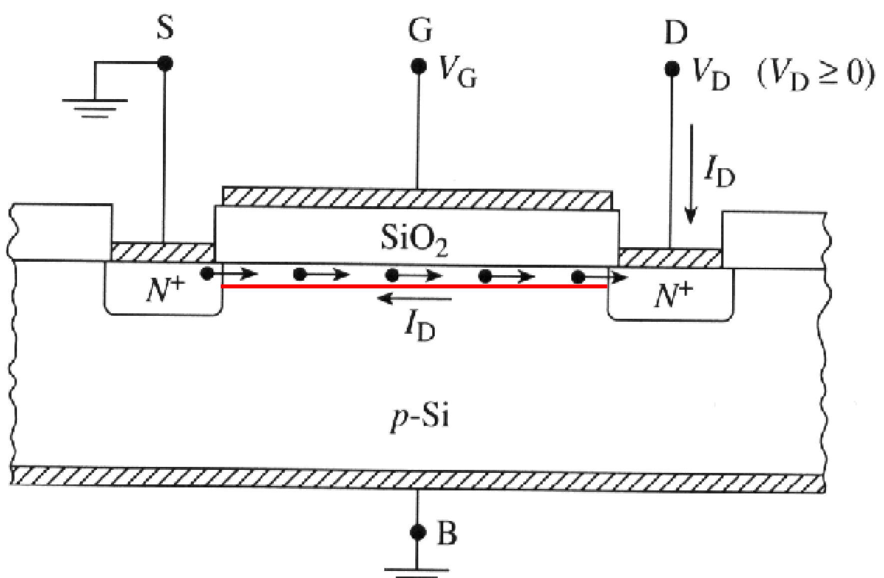
- **1: Glass photomask (mask)**
- 2: Apply photoresist (coating)
- 3: UV exposure
- 4: Development
- 5: Etching



Circuit(电路符号)



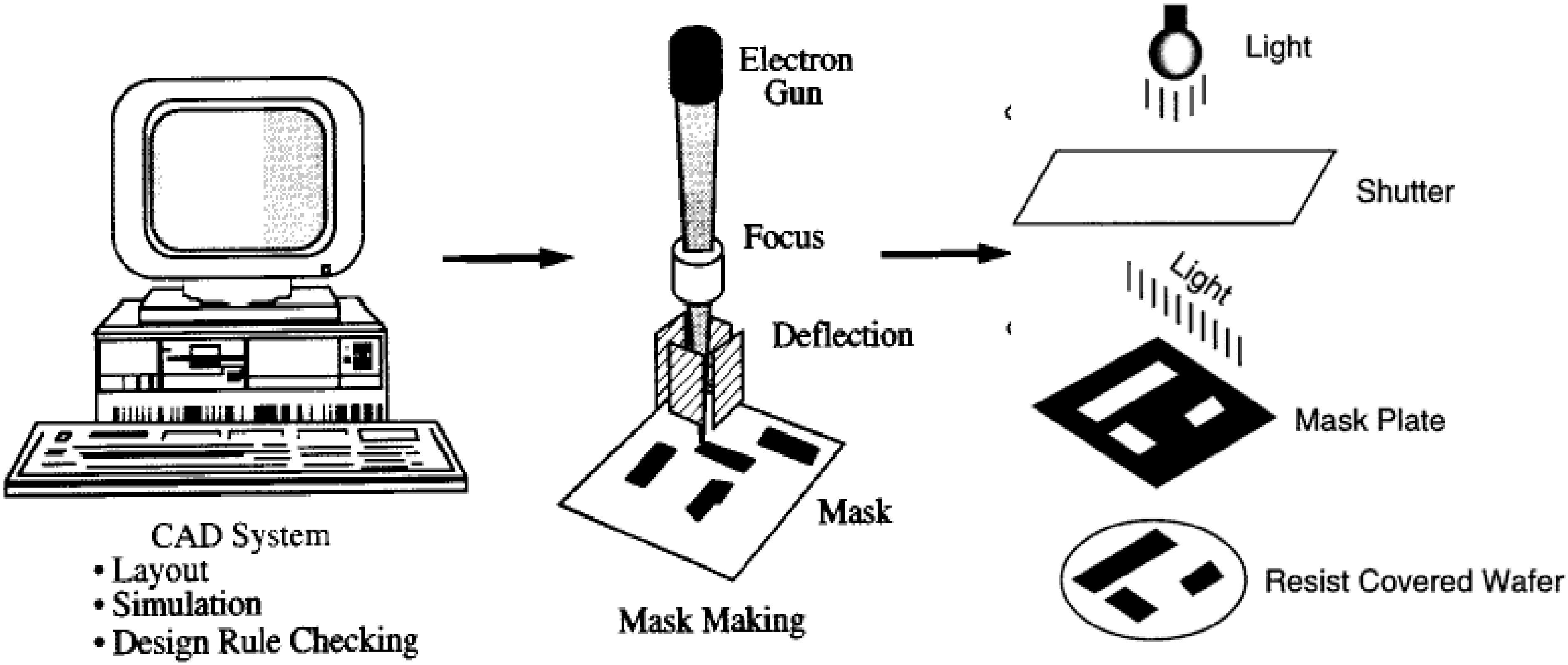
Layout(版图)



Photolithographic process

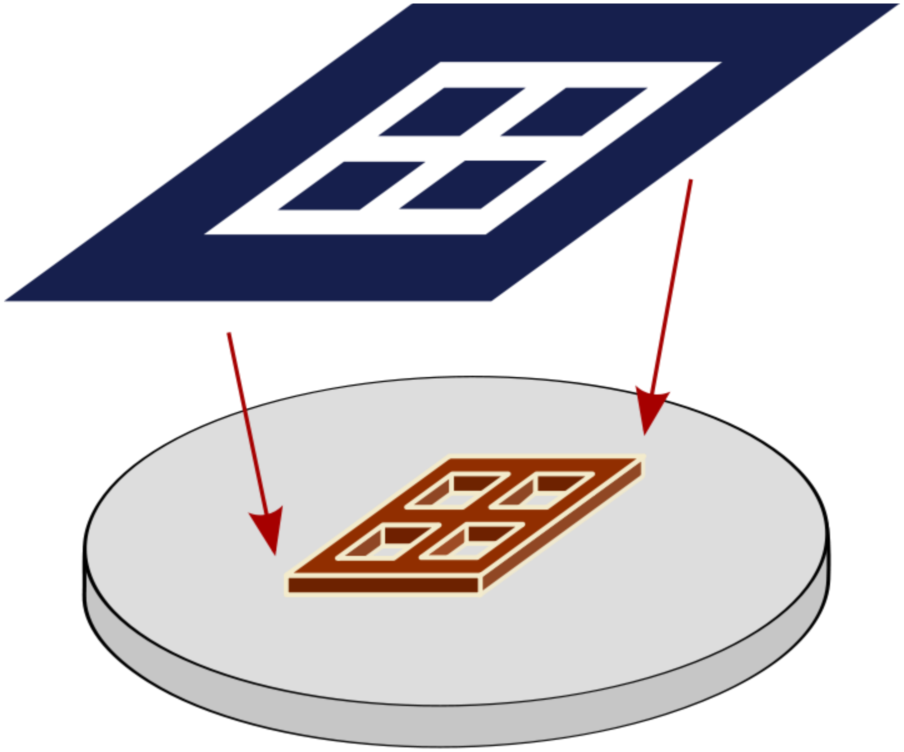
Design => Mask => Wafer

The process of using UV (Ultraviolet) light to transfer patterns from a glass mask onto a surface of the Si wafer.

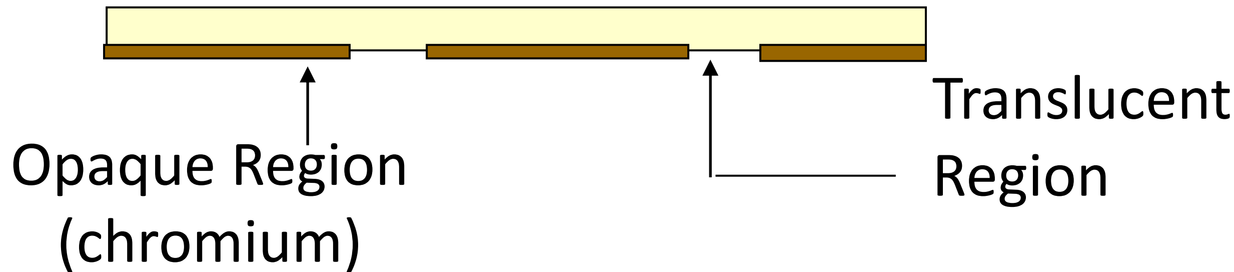


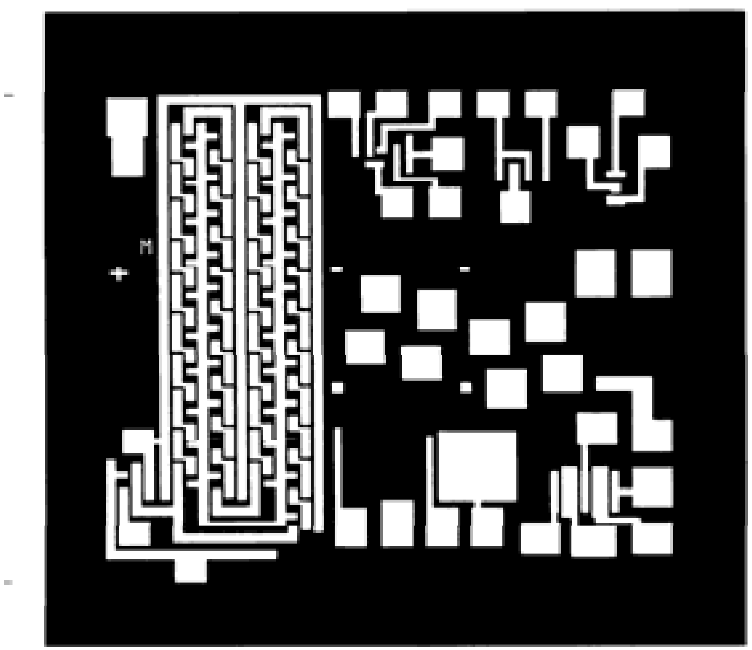
The photolithographic process

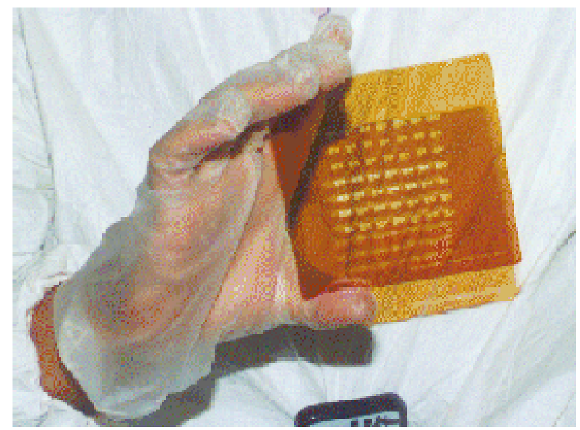
- The process of using UV (Ultraviolet) light to transfer patterns from a glass mask onto a surface of the Si wafer.



1. Glass Photomask (mask)







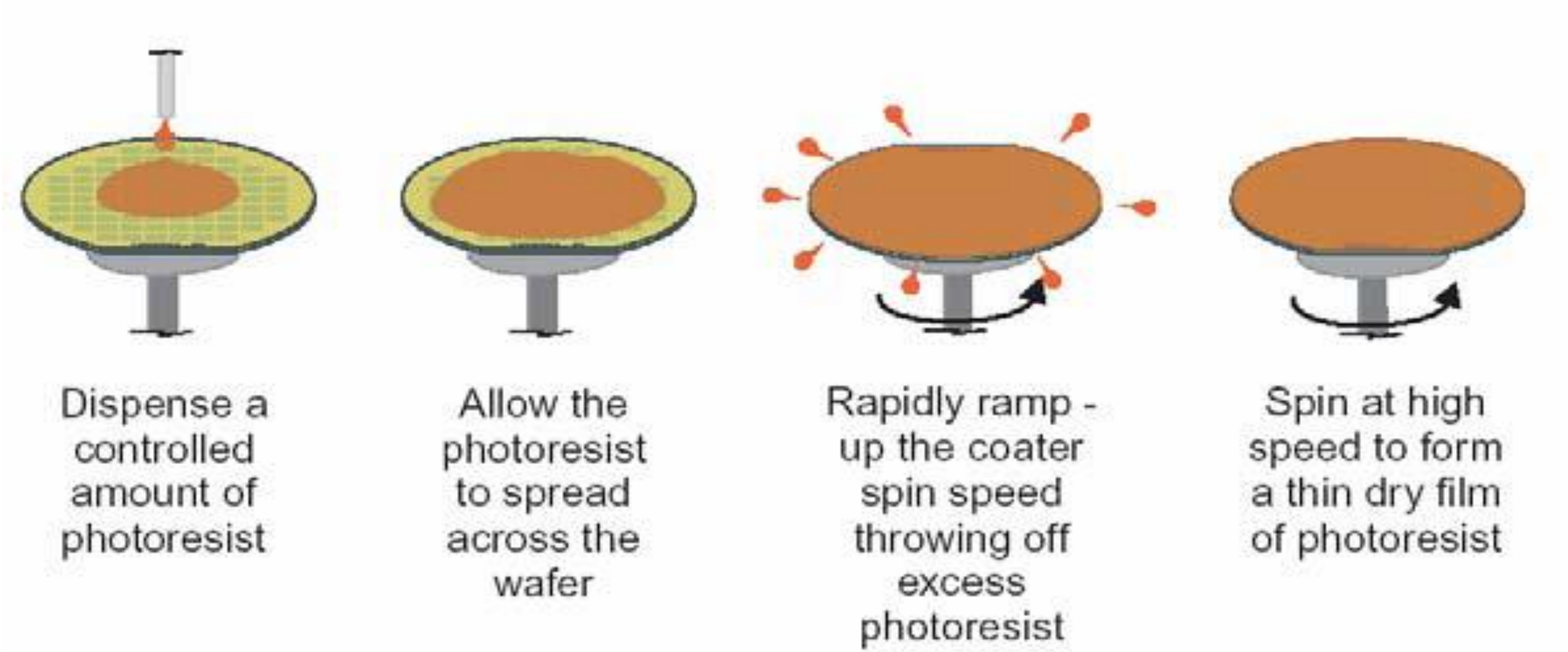
- One mask for each lithography level in process

Photolithography & Etching

- 1: Glass photomask (mask)
- **2: Apply photoresist (coating)**
- 3: UV exposure
- 4: Development
- 5: Etching

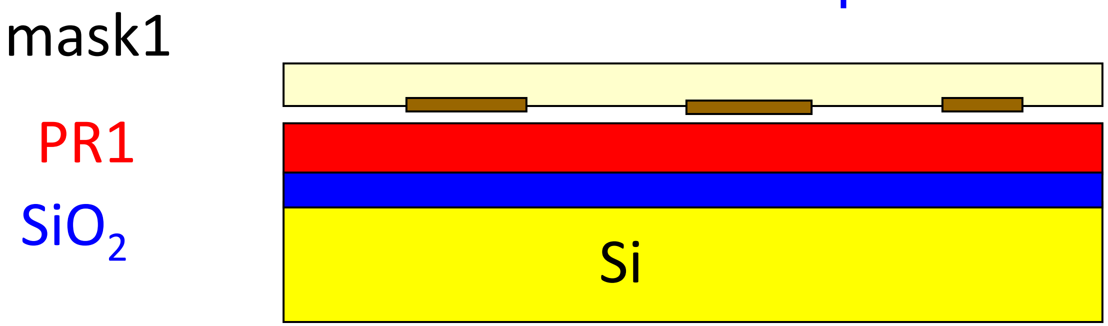
2. Coating

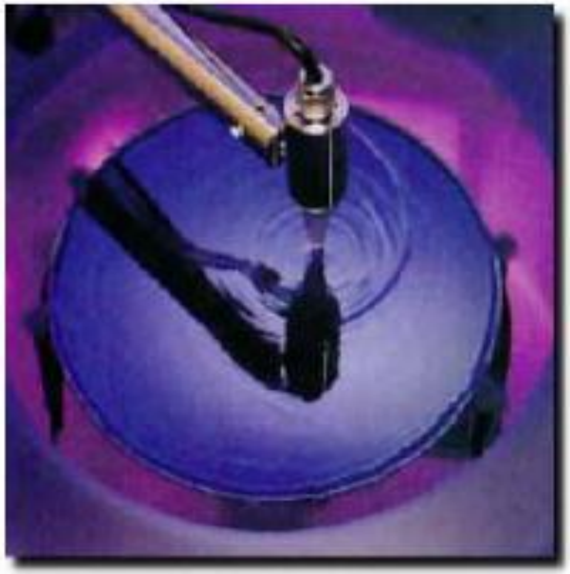
- Spin coating process:
  - A controlled volume of photoresist is dispensed onto a wafer
  - The wafer is spun at high speed to produce a uniform photoresist film.



Using the mask

- Preparing the surface:
  - Grow a thin layer of SiO_2
  - Apply on top of the SiO_2 layer a negative photoresist (PR1); thickness around 1 µm





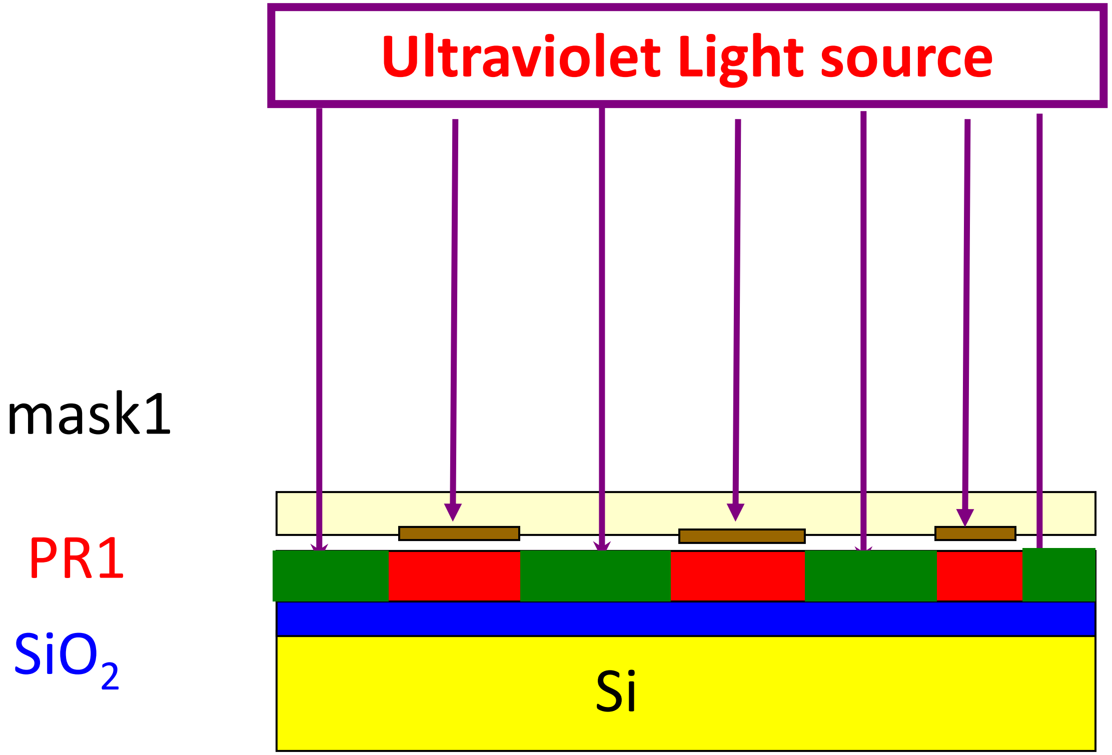
Spin photoresist

- Place a mask (M1) in close proximity of the wafer

Photolithography & Etching

- 1: Glass photomask (mask)
- 2: Apply photoresist (coating)
- 3**: UV exposure**
- 4: Development
- 5: Etching

3. UV exposure



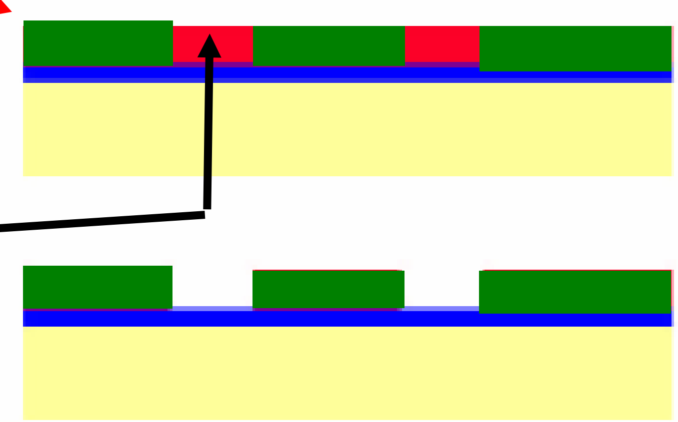
- After placing M1 in close proximity of the wafer, an project UV light through the mask into PR1;
- Induce changes in the polymer structure and these regions will be insoluble to an organic solvent.
- The regions where the mask was opaque will not be exposed.

Photolithography & Etching

- 1: Glass photomask (mask)
- 2: Apply photoresist (coating)
- 3: UV exposure
- 4: **Development**
- 5: Etching

4. Development (negative resist)

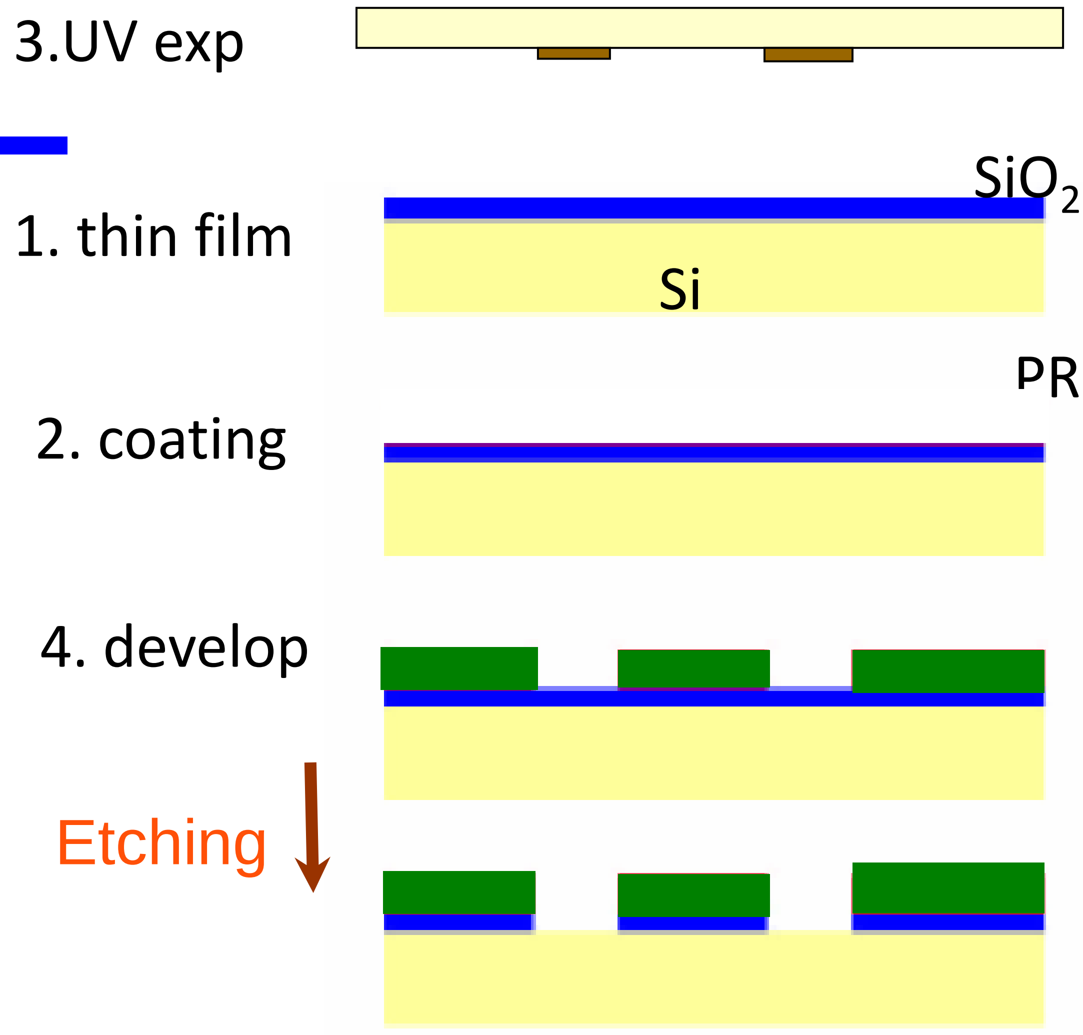
The exposed regions will be insoluble to an organic solvent.



The regions, which is not exposed, will be soluble to an organic solvent

Process of Development

Process steps

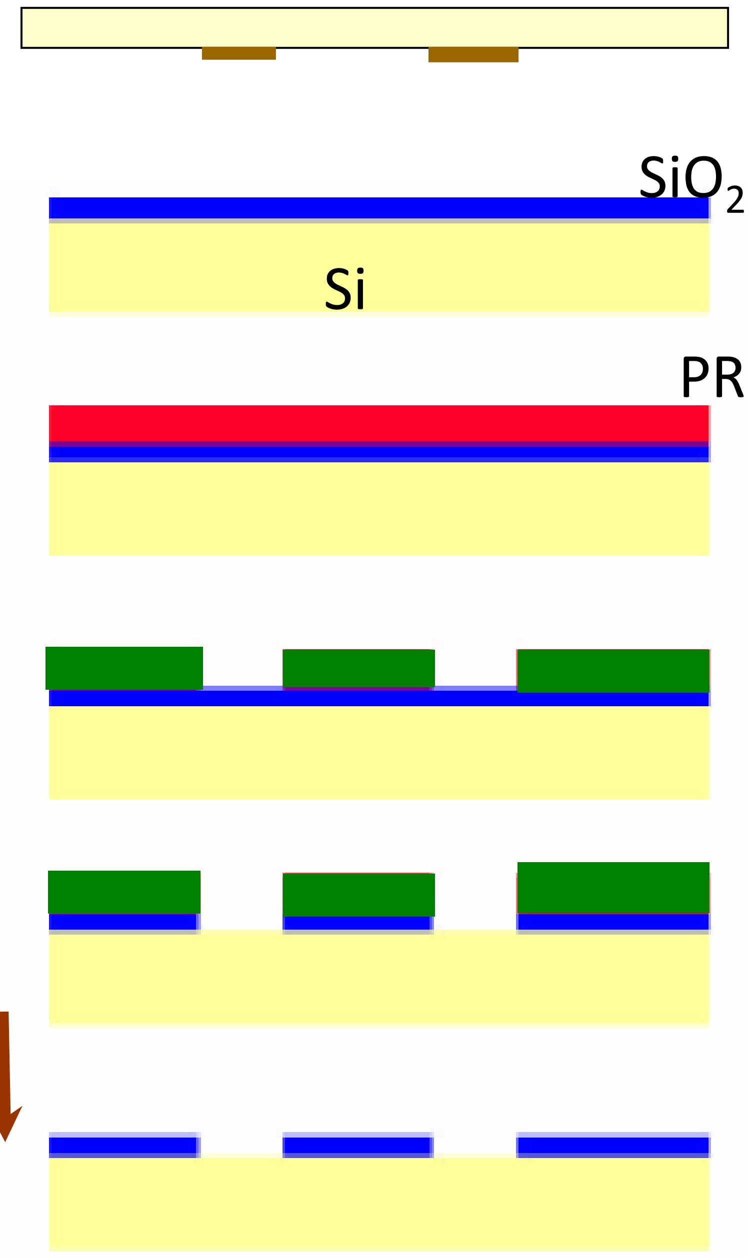


Photolithography & Etching

- 1: Glass photomask (mask)
- 2: Apply photoresist (coating)
- 3: UV exposure
- 4: Development
- **5: Etching**

5. Etching

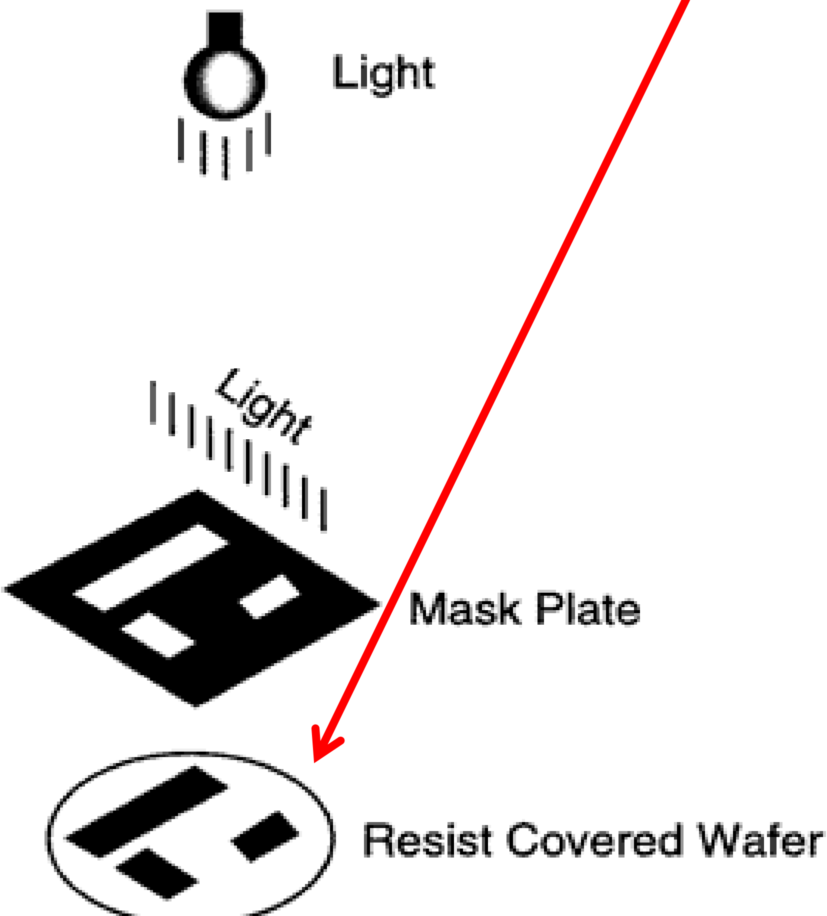
- **Wet Etching**
  - $SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O$ (acid solution)
- **Dry Etching**
  - **REI (e.g. CF_4 plasma)**

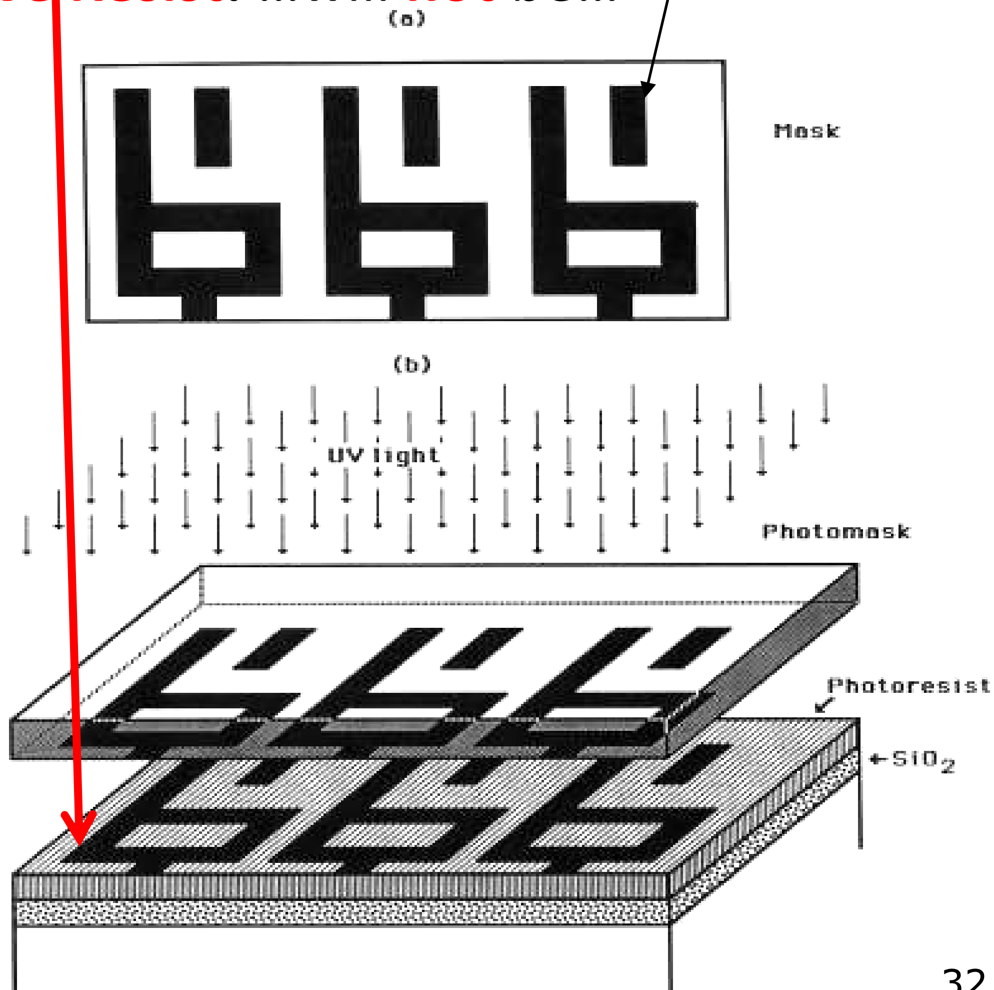


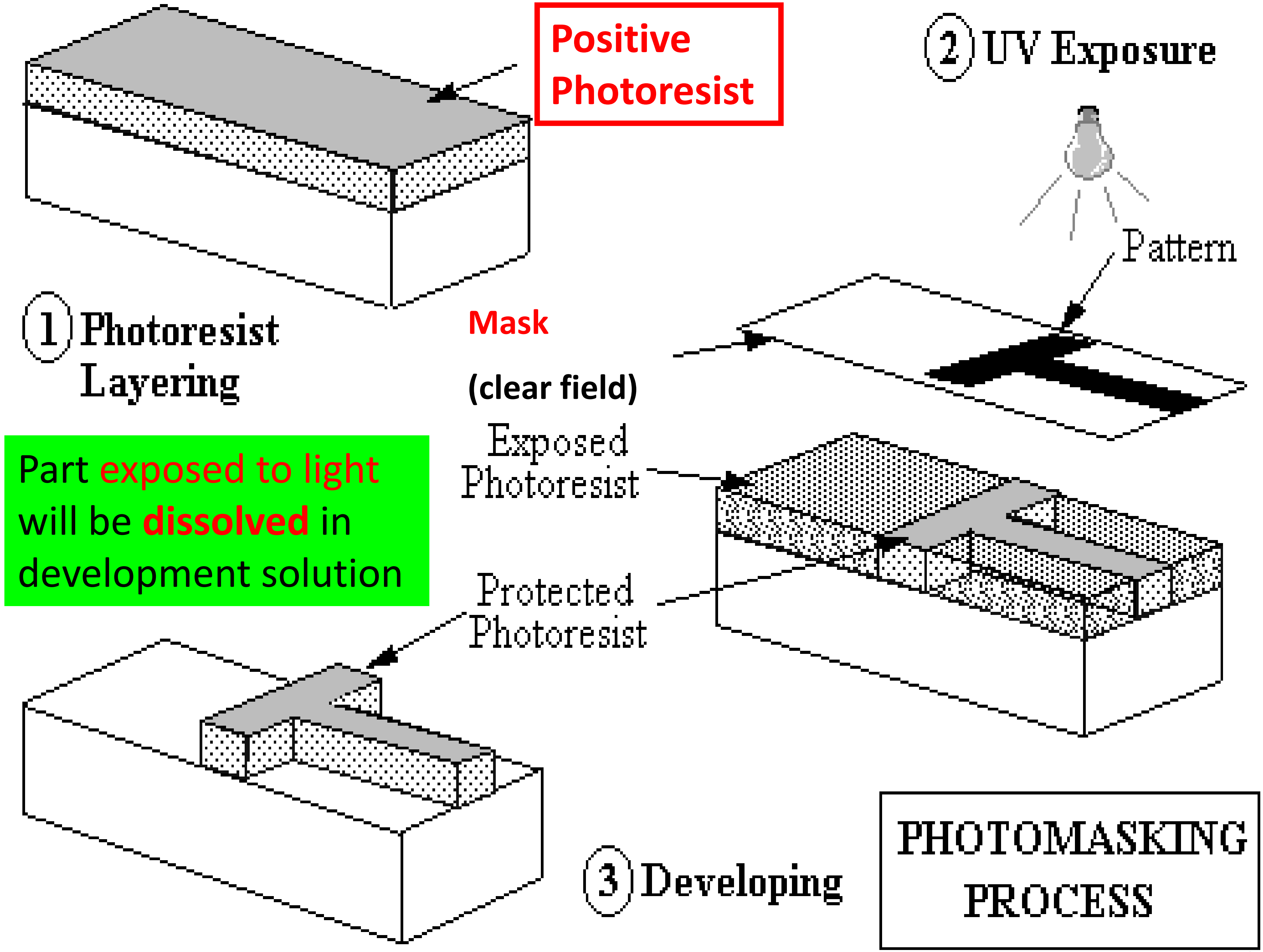
Photoresist

chromium

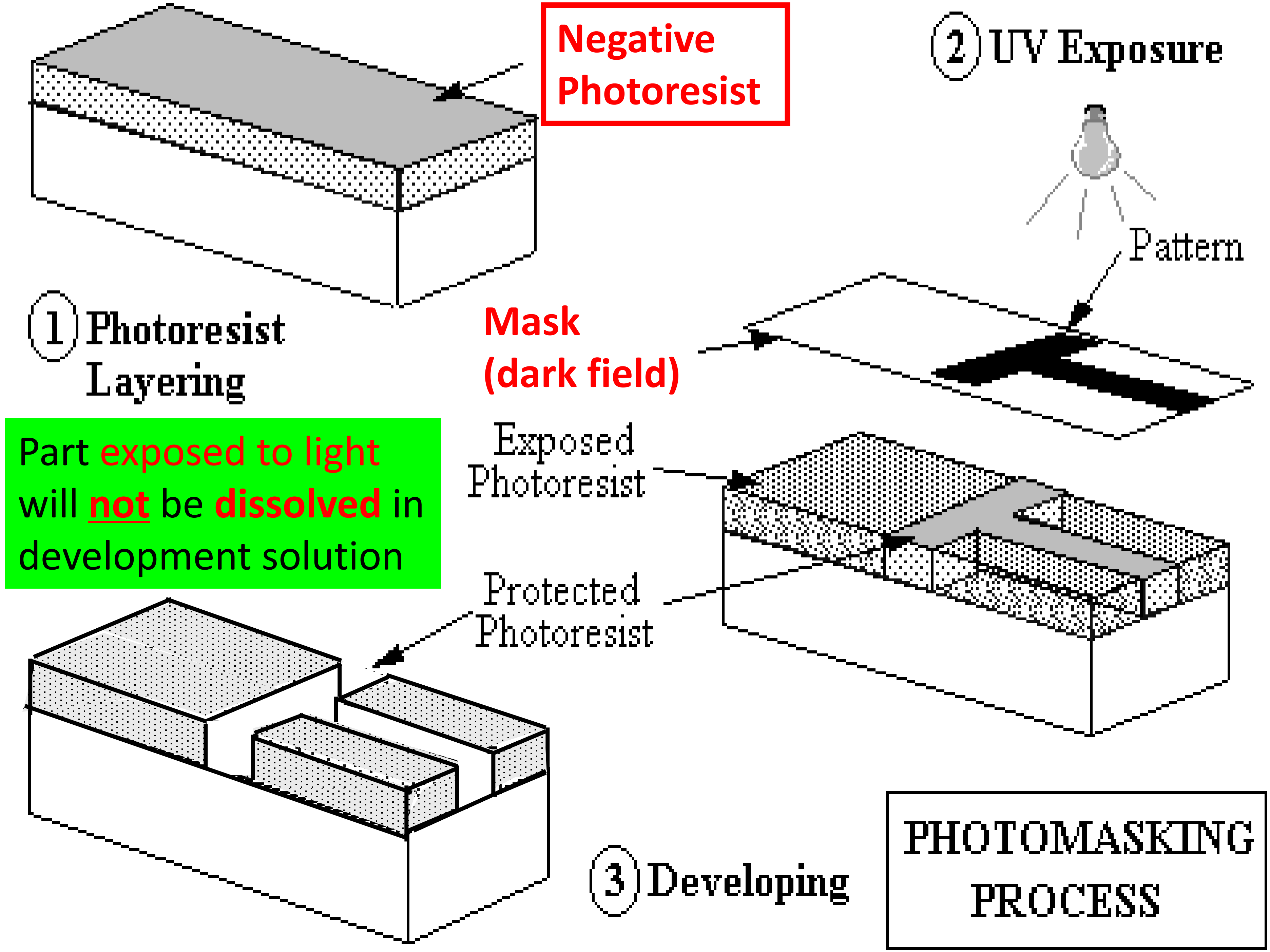
Positive Resist: Part exposed to light will be **dissolved** in development solution. **Negative Resist:** …will **not** be…





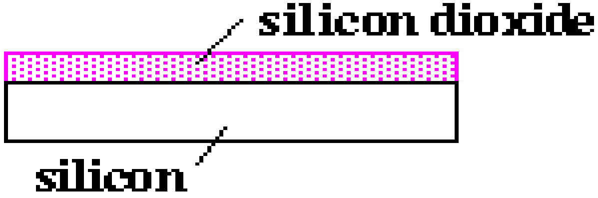


Positive
Photoresist
(2) UV Exposure
Pattern
(1) Photoresist
Layering
Mask
(clear field)
Exposed
Photoresist
Part exposed to light will be dissolved in development solution
Protected
Photoresist
(3) Developing
PHOTOMASKING
PROCESS

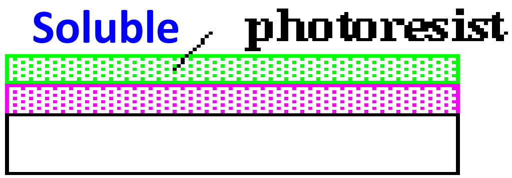

Negative Photoresist
2 UV Exposure
Pattern
1 Photoresist Layering
Mask (dark field)
Part exposed to light will not be dissolved in development solution
Exposed Photoresist
Protected Photoresist
3 Developing
PHOTOMASKING PROCESS

Example 1: negative photoresist

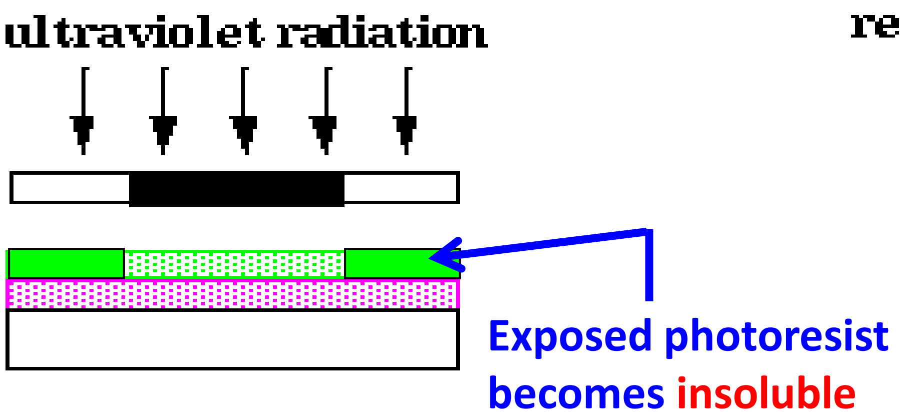
1. Wafer is oxidized.



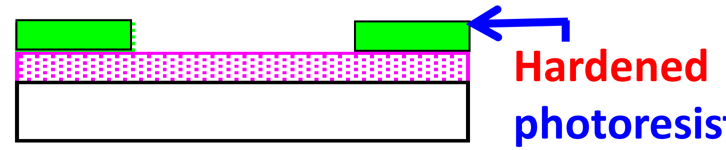
2. Oxidized wafer is covered with photoresist.



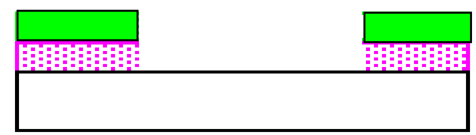
3. Wafer is exposed to UV light through a photomask.



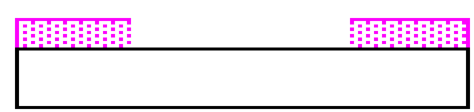
4. Unexposed photoresist is dissolved in developer solution.



5. Oxide now unprotected by photoresist is etched away in hydrofluoric acid. HF



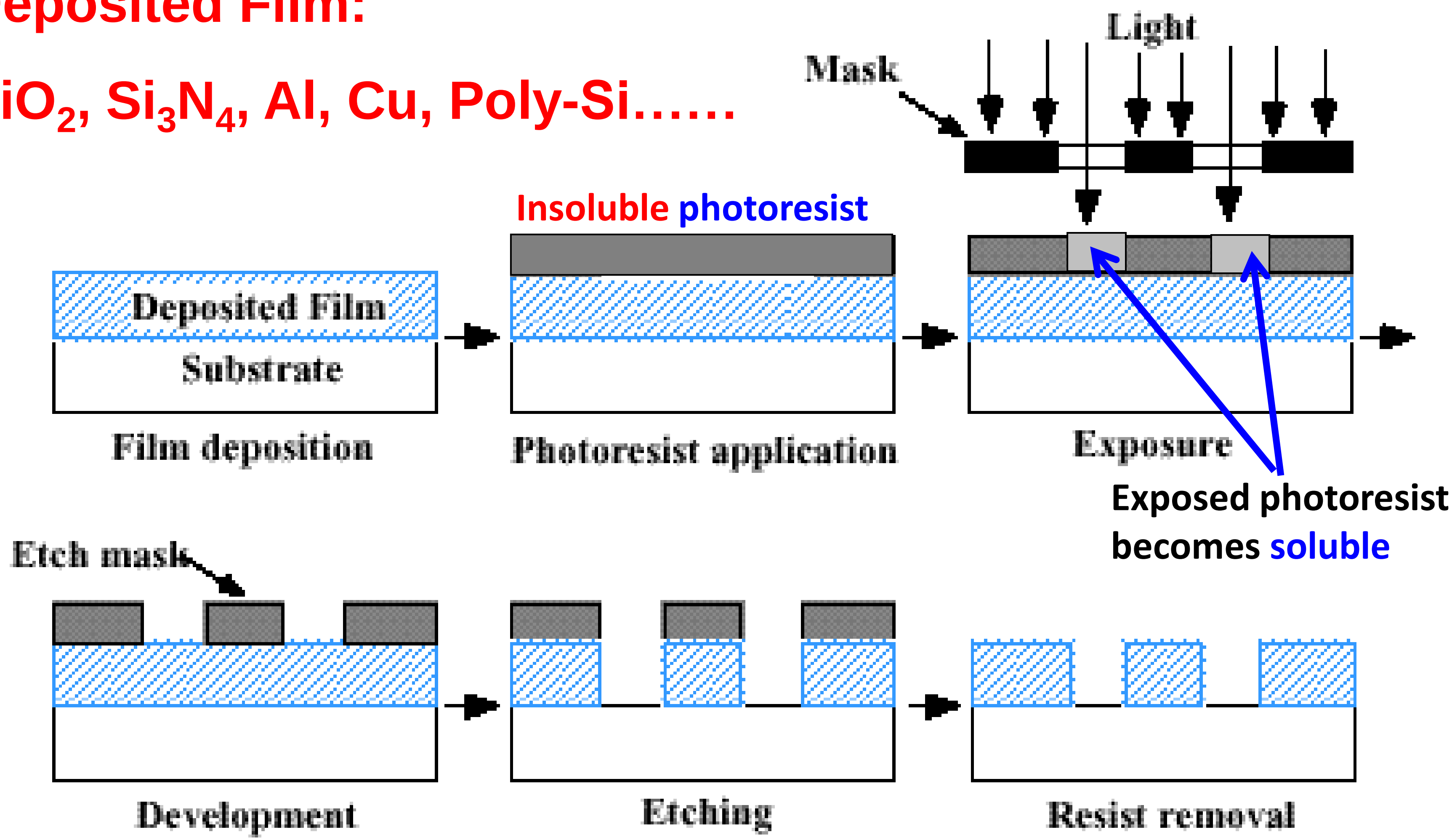
6. The rest of the photoresist is removed. Wafer is now ready for doping.



Example 2: positive photoresist

Deposited Film:

SiO_2, Si_3N_4, Al, Cu, Poly-Si……



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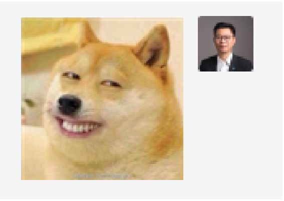


Doping

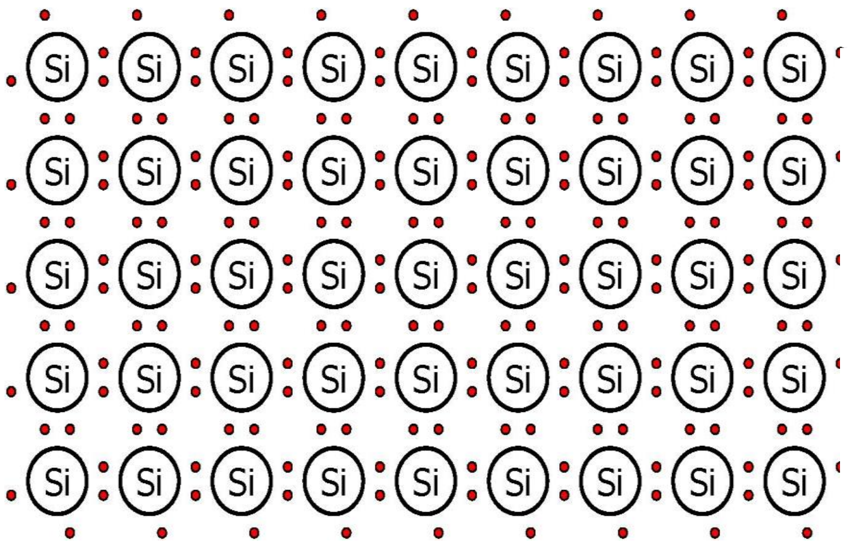
- **Thermal Diffusion**
- **Ion Implantation**

Intrinsic Semiconductor

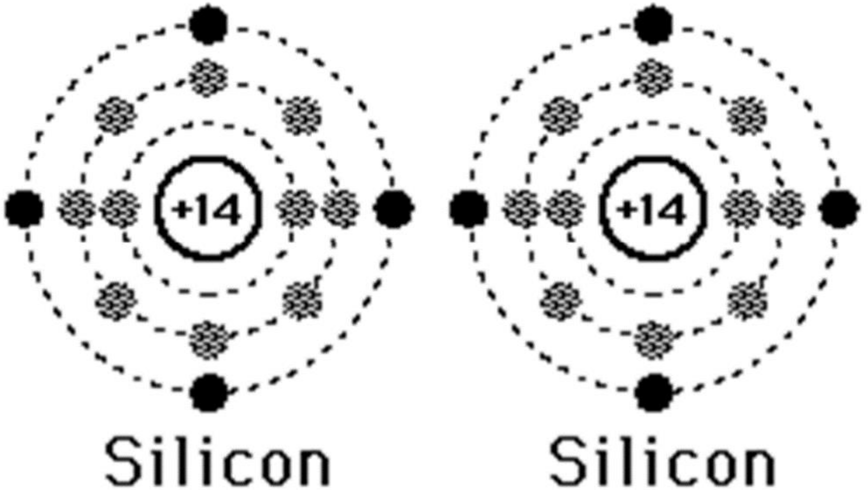
Lecture 3

Silicon has four valence electrons

- It covalently bonds with 4 adjacent atoms in the crystal lattice
- Increasing Temperature Causes Creation of Free Carriers. $10^{10}cm^{-3}$ free carriers at $23^{o}C$ (out of $2x10^{23}cm^{-3}$): Intrinsic Conductivity.

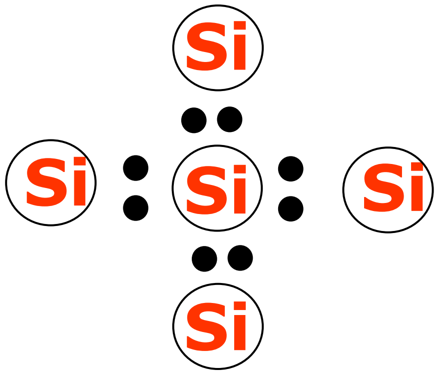


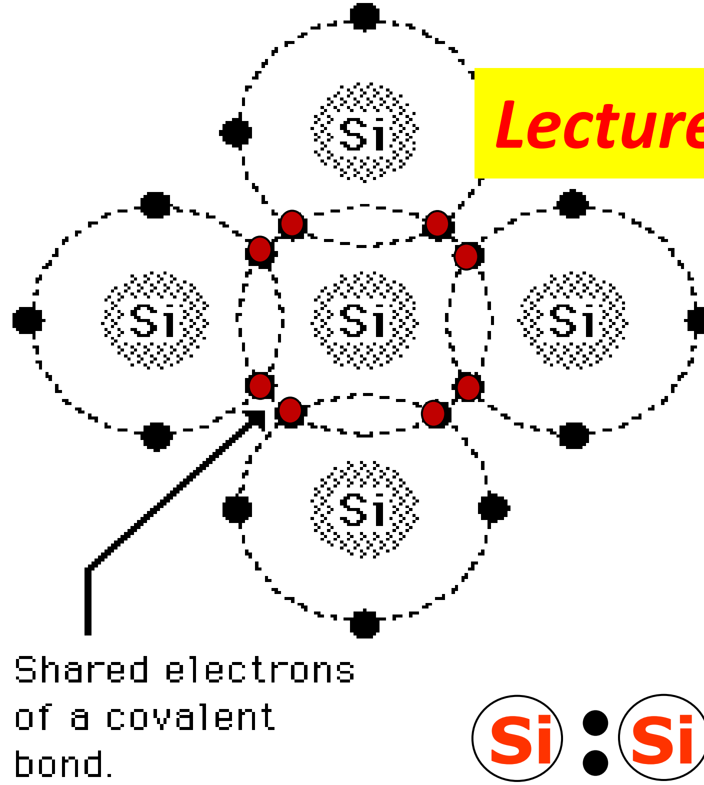
outmost orbit: **4 valence electrons**

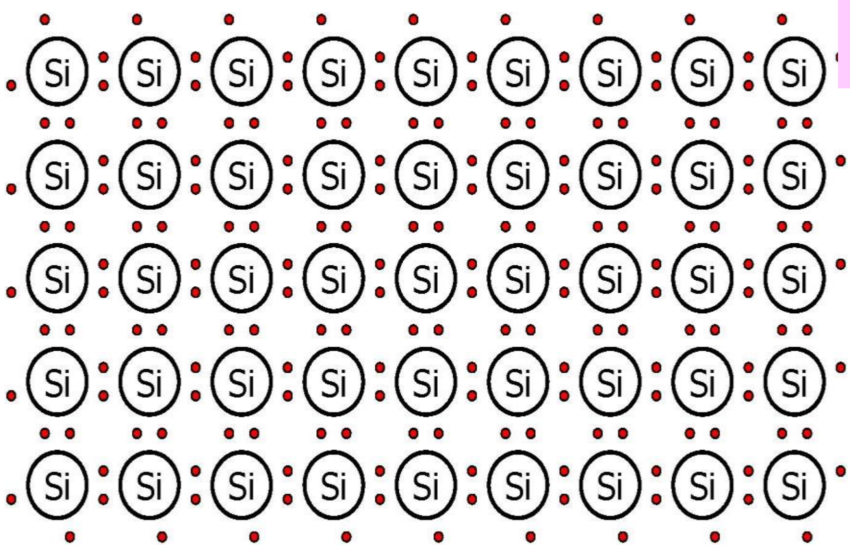


Intrinsic Semicon

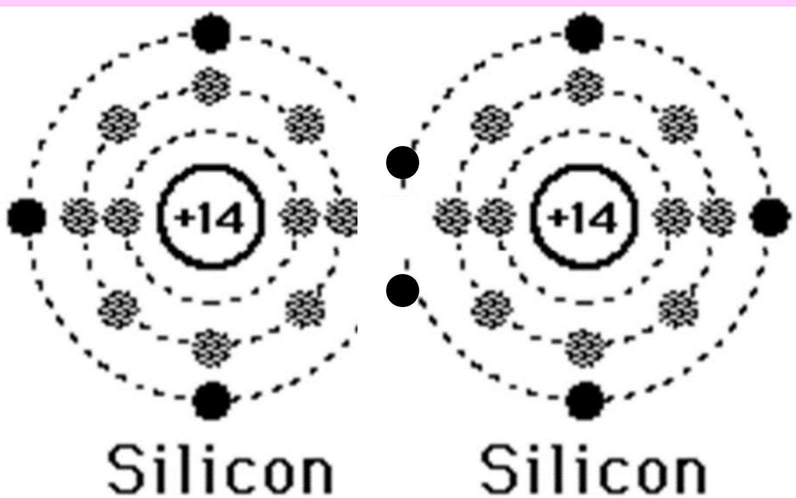
Lecture 3







Covalent Bond : shared electrons



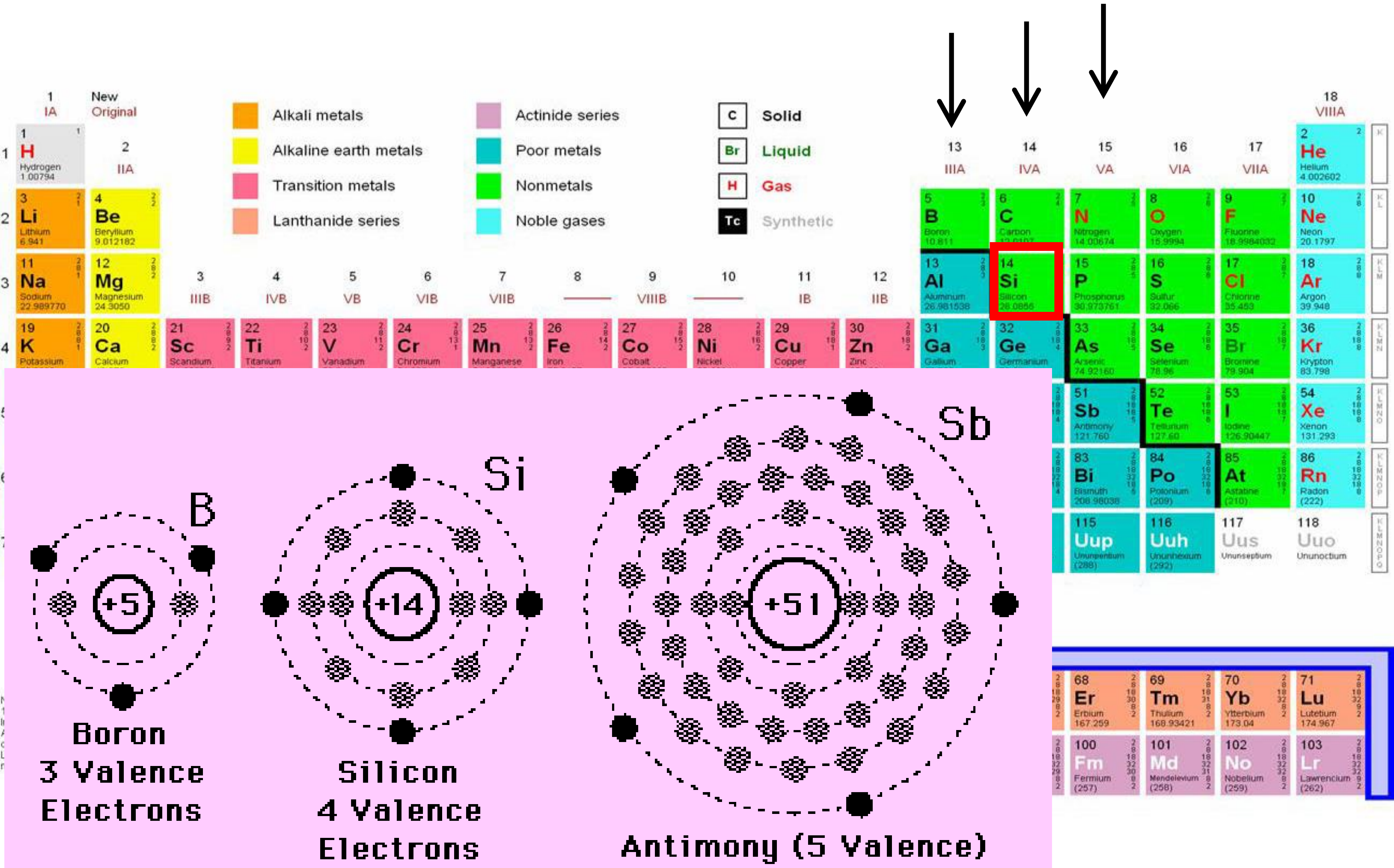
The Doping

Lecture 3

- The addition of a **small** percentage of **foreign atoms** in the regular crystal lattice of silicon or germanium produces dramatic changes in their electrical properties, producing **n-type** and **p-type** semiconductors.

Element periodic table

Lecture 3



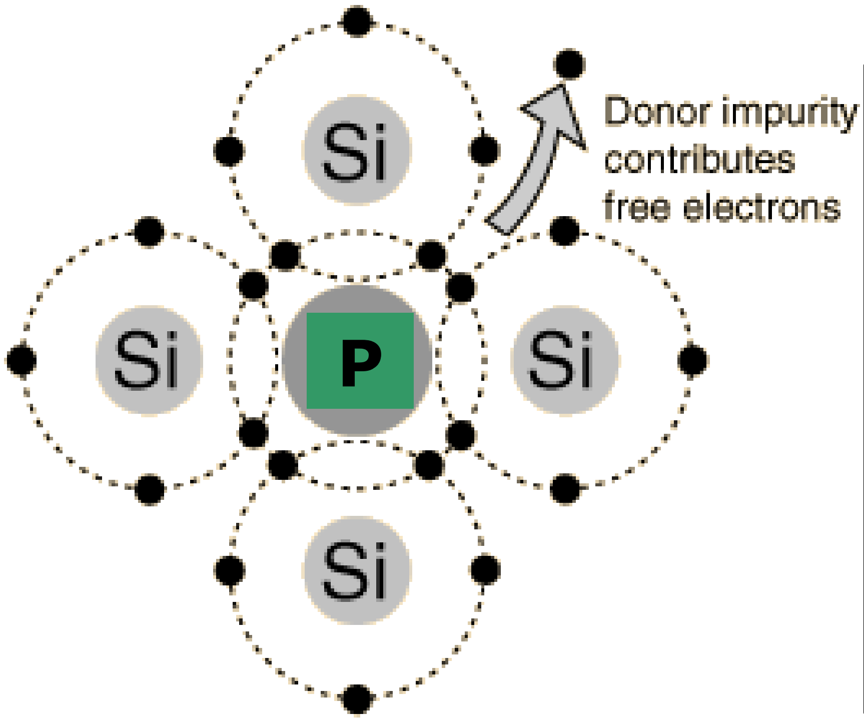
Doping (N type)

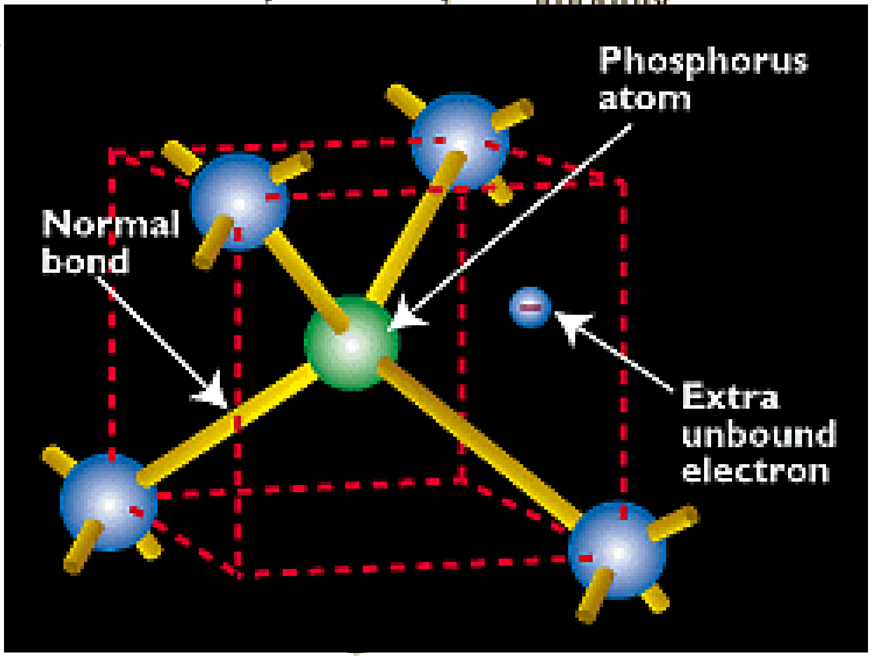
Column V elements are donors, e.g. P, As, Sb

By <u>substituting</u> a Si atom with a special impurity atom (Column V element), a conduction electron is created.

Lecture 3

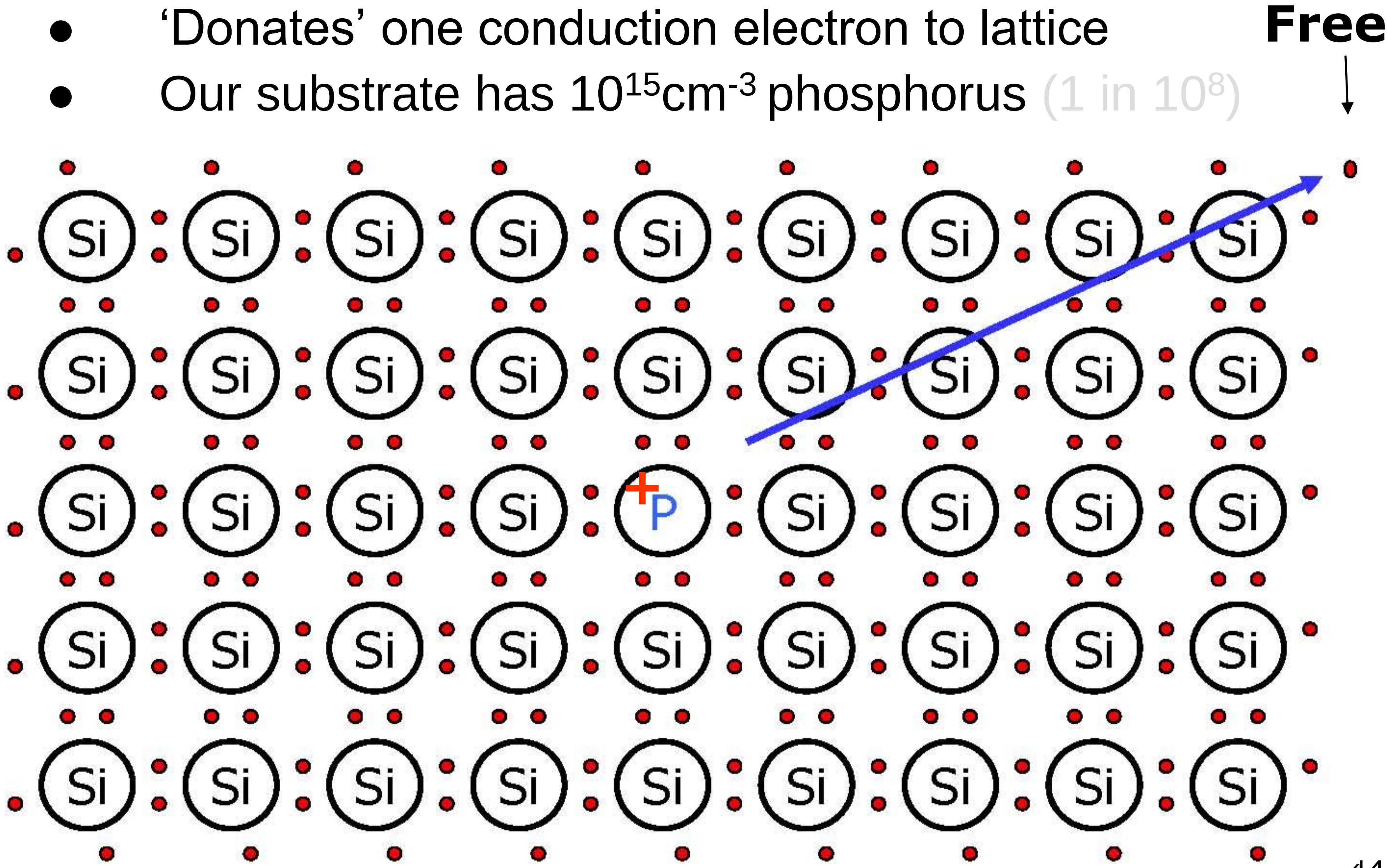
<u>Donors</u>: P, As, Sb





Phosphorus has 5 valence electrons

- 'Donates' one conduction electron to lattice
- Our substrate has $10^{15}cm^{-3}$ phosphorus (1 in 10^8)



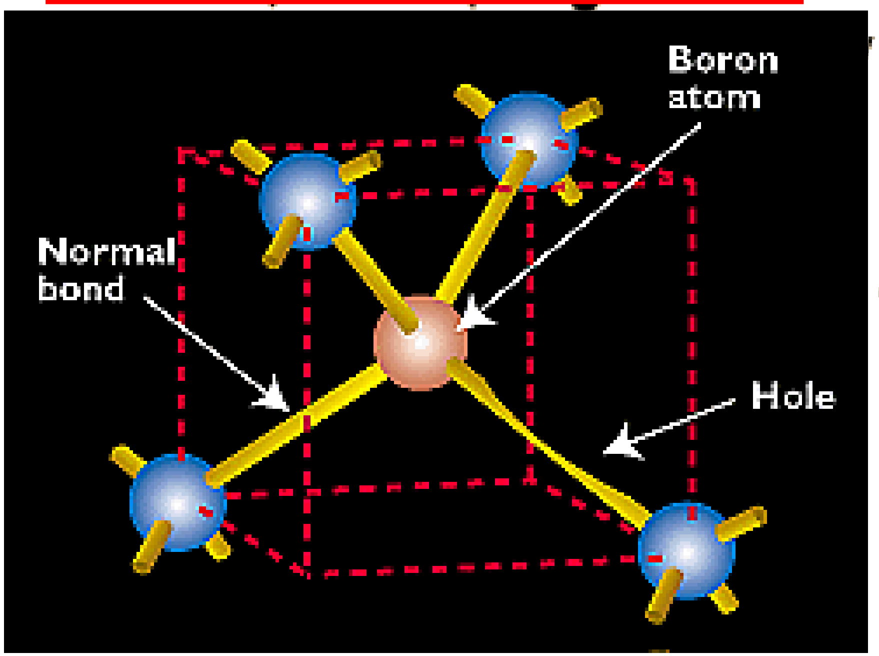
Doping (P type)

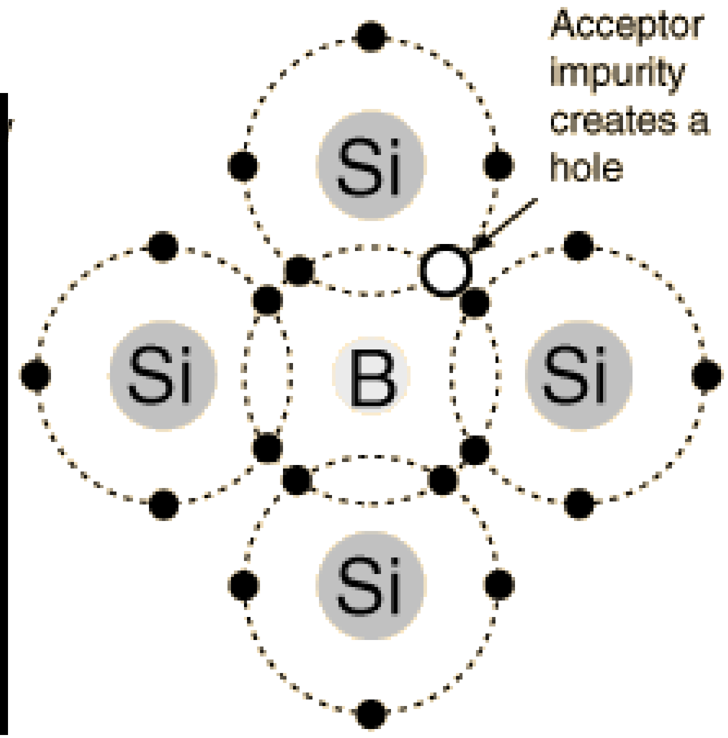
Column III elements are acceptors, e.g. B, Al, Ga

By substituting a Si atom with a special impurity atom (Column III element), a conduction hole is created.

Lecture 3

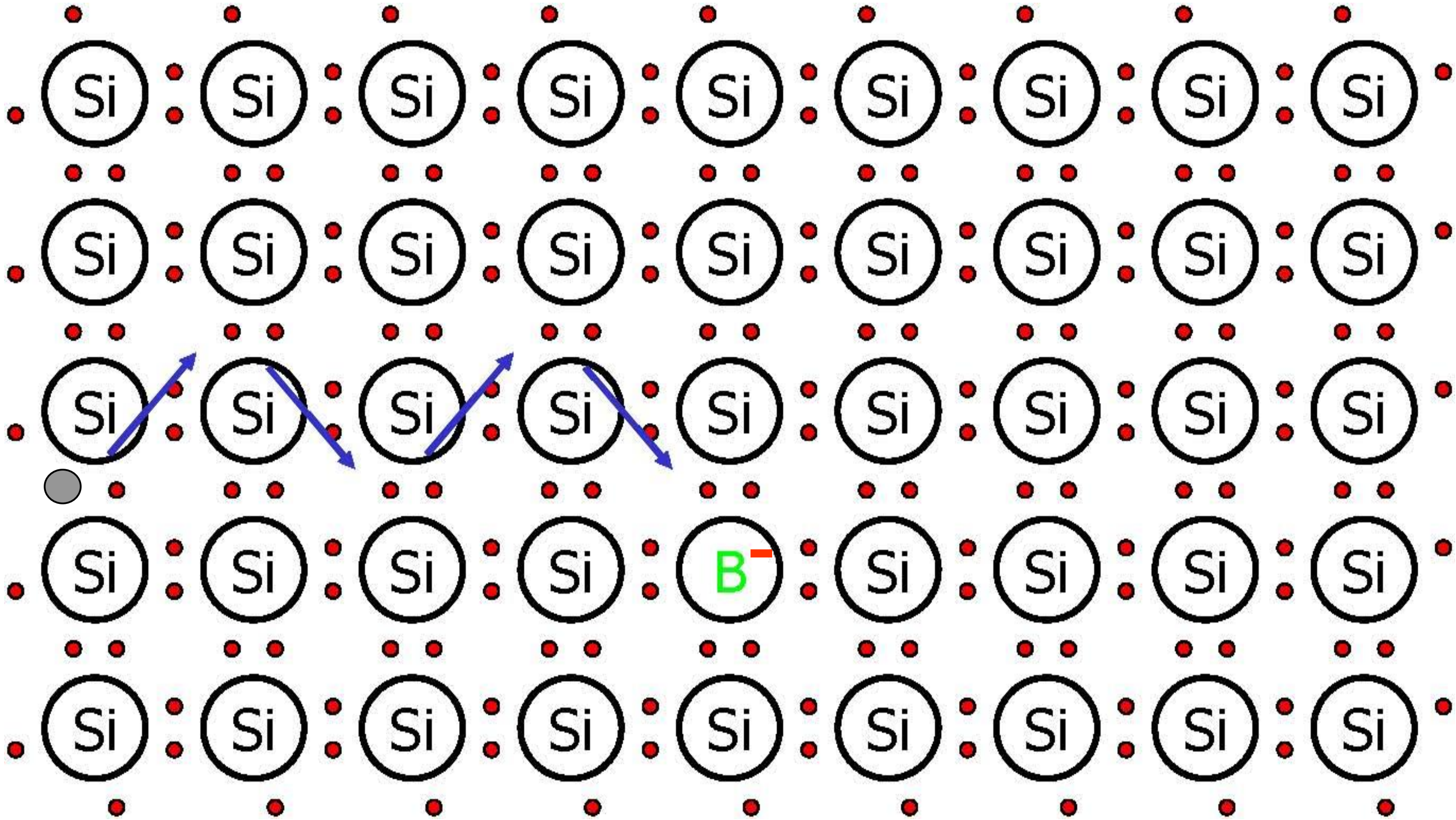
Acceptors: B, Al, Ga, In



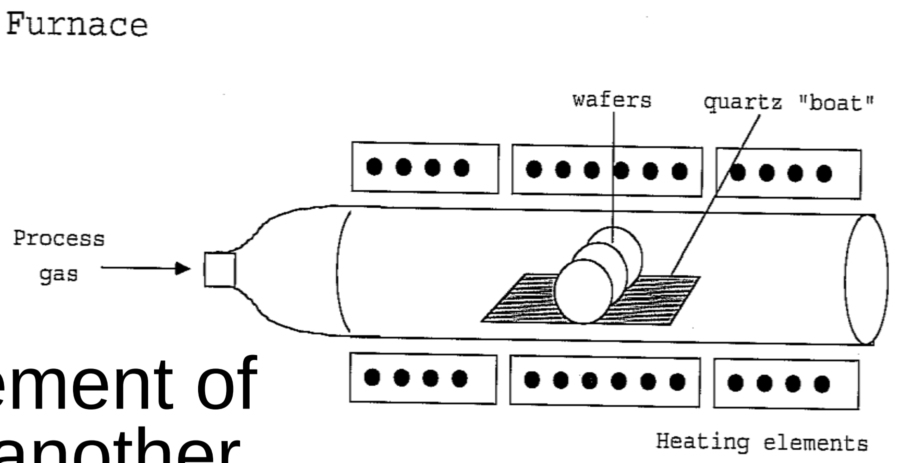


Boron has 3 valence electrons

- 'Accepts' one electron from lattice
- Creates a 'hole'



Diffusion

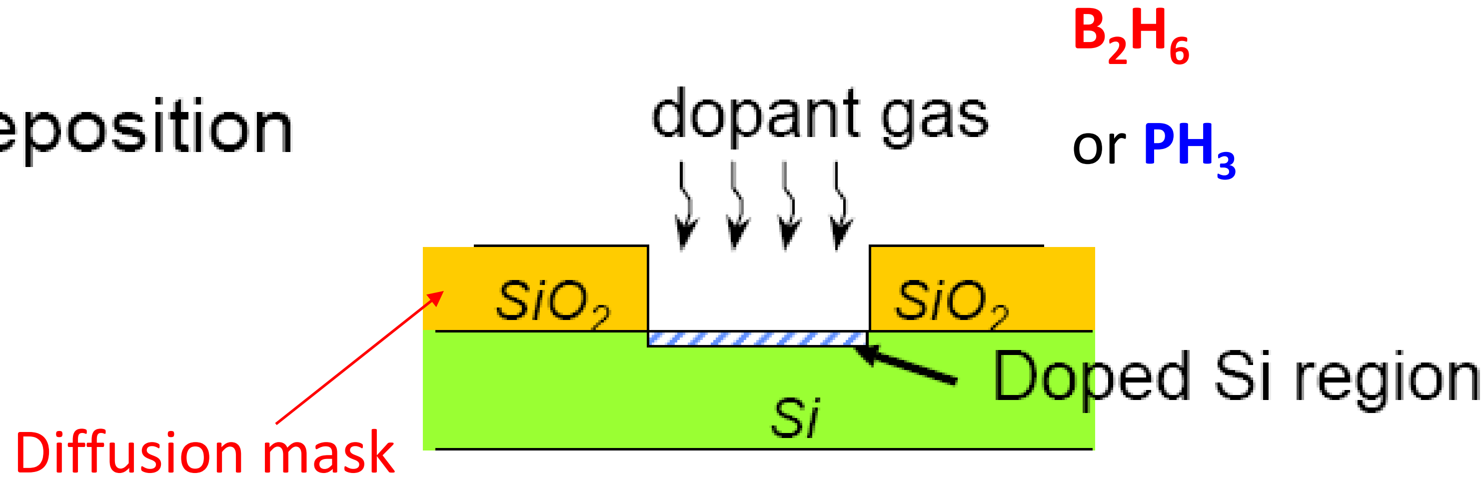


- **Diffusion** is the movement of one material through another from a region of relatively higher concentration into a region of lower concentration. There are two steps to thermal diffusion:
  - **Pre-deposition**
  - **Drive-in**

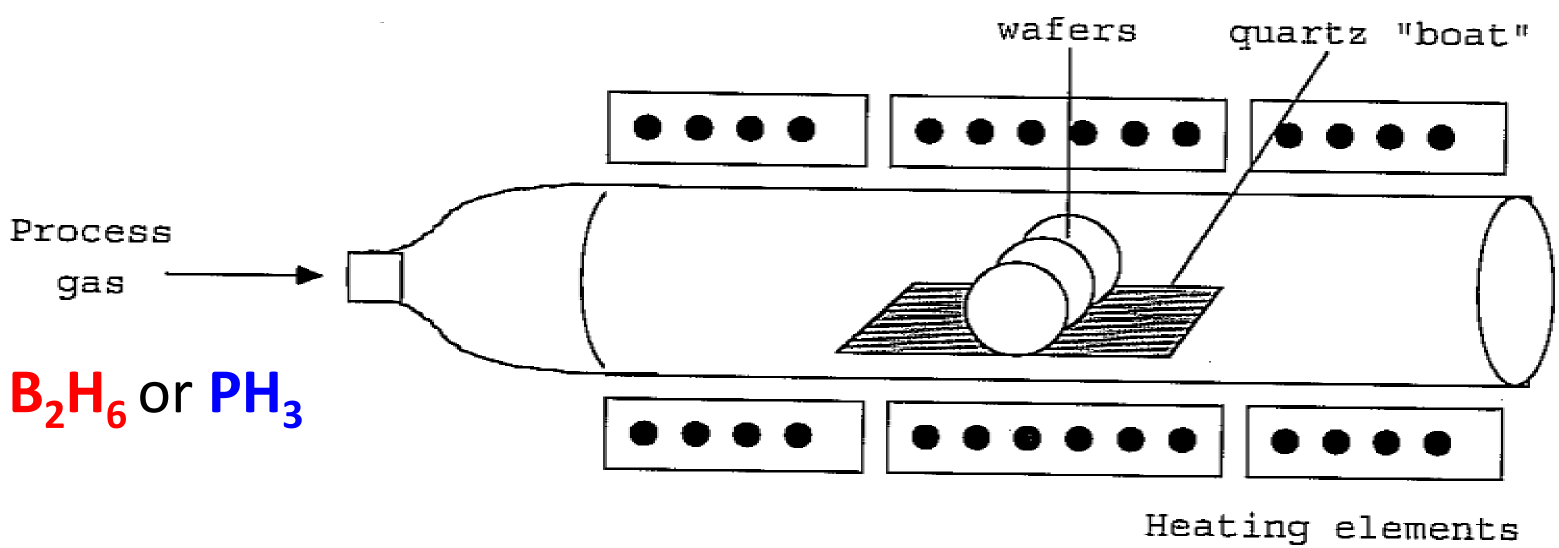
- **Dopant Diffusion Sources**
  - Gas Source: AsH_3, PH_3, B_2H_6

Dopant Diffusion

(1) Predeposition

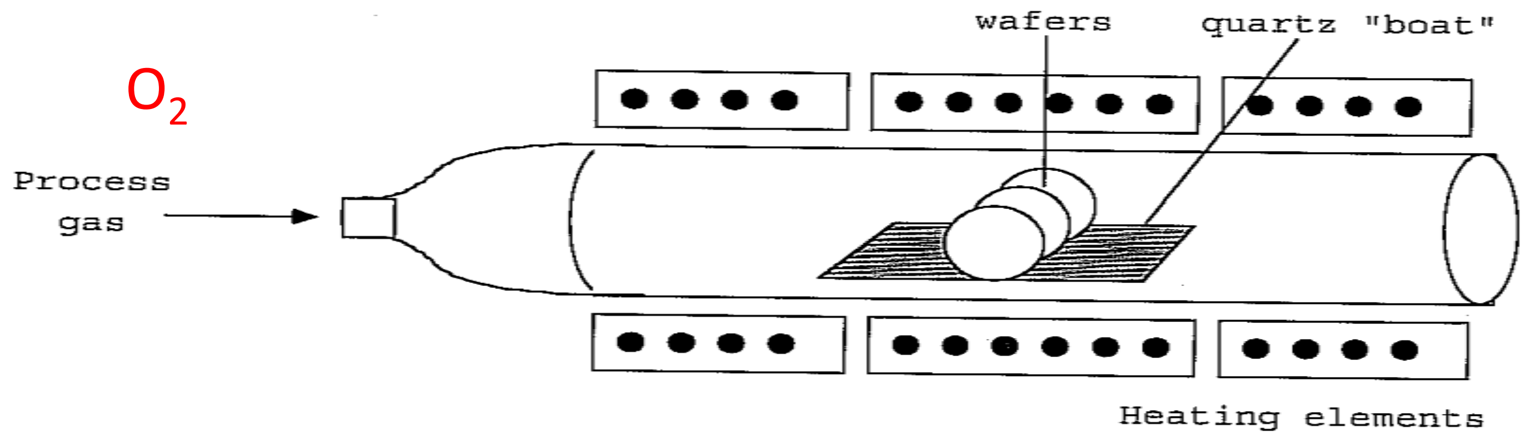


Furnace



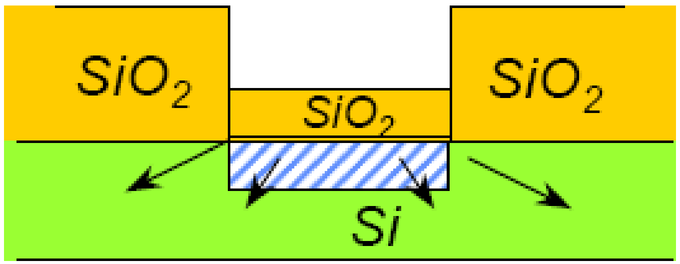
Dopant Diffusion

Furnace



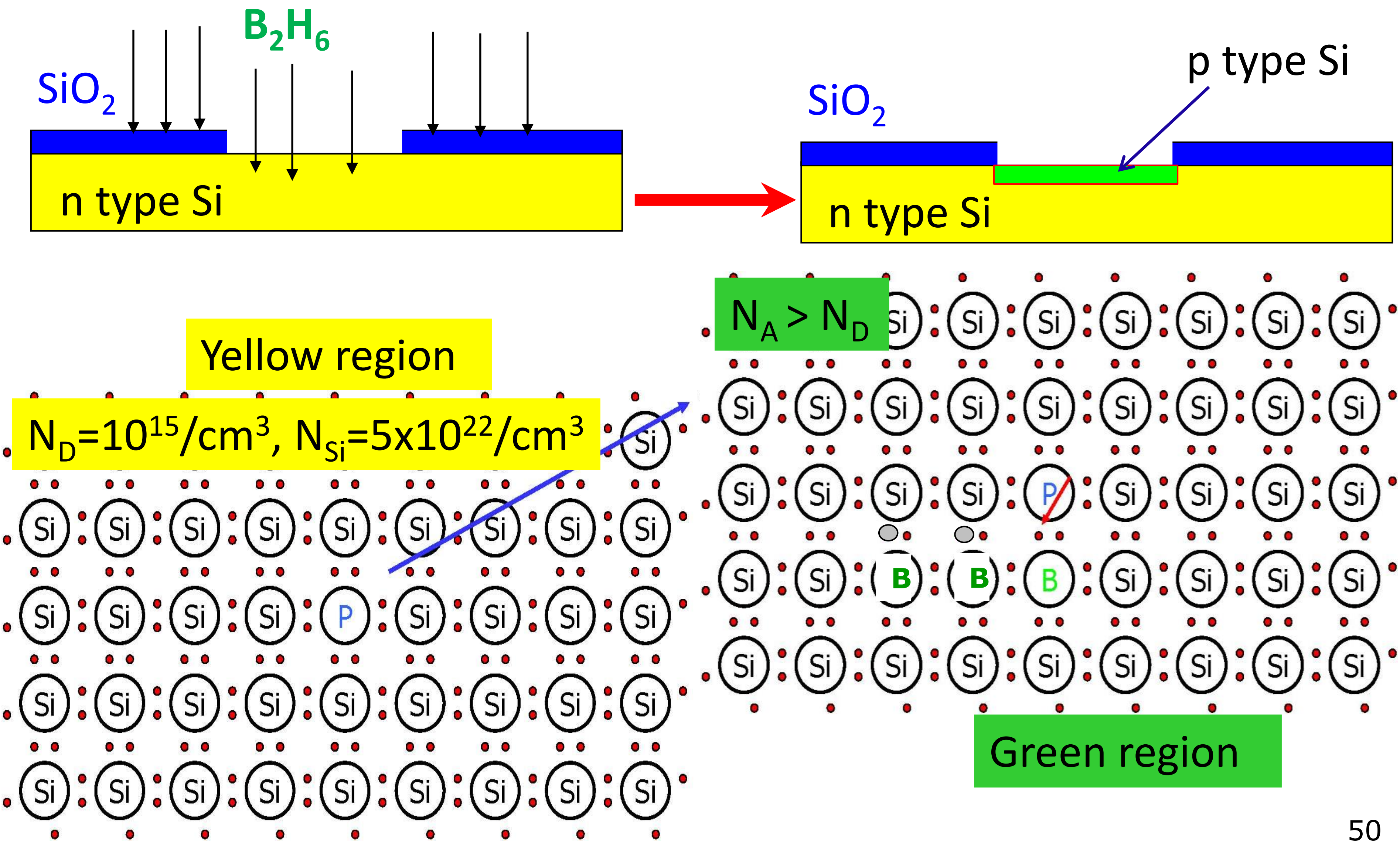
(2) Drive-in

Turn off dopant gas
or seal surface with oxide

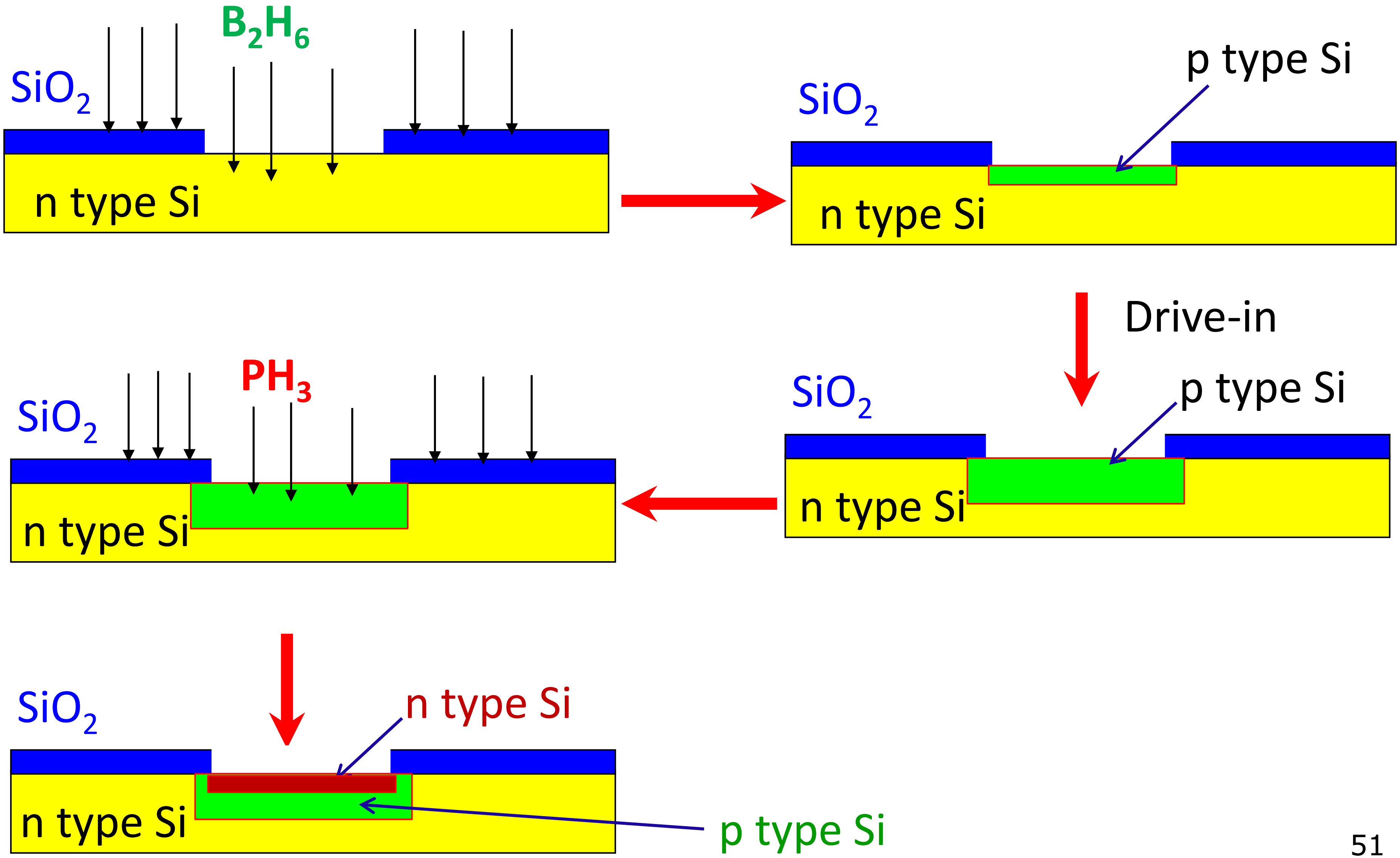


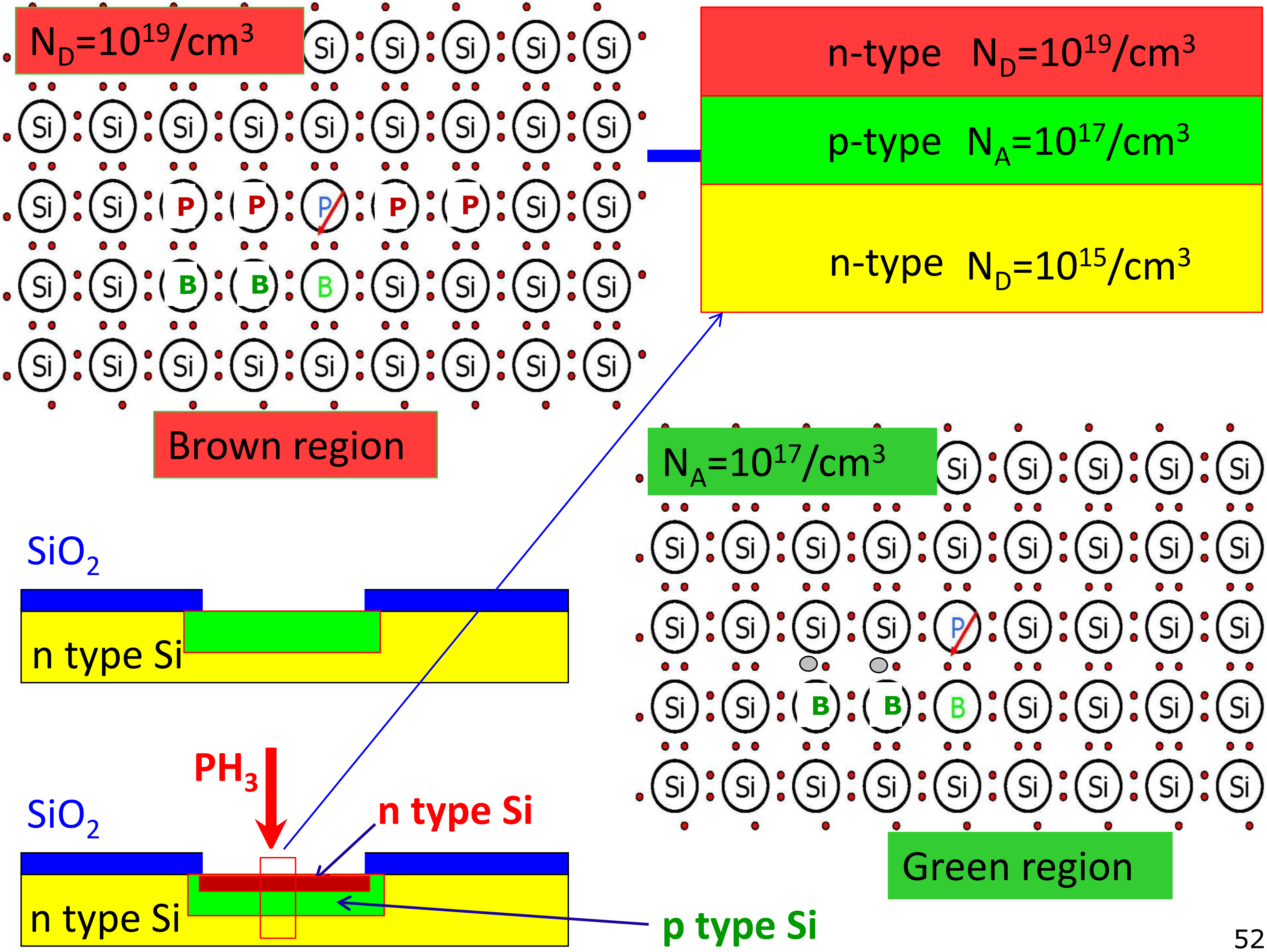
Note: Predeposition by diffusion can also be replaced by a shallow implantation step.

Thermal Diffusion Example



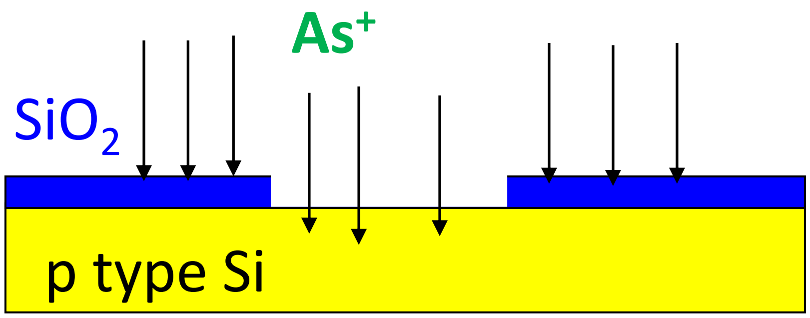
Thermal Diffusion Example



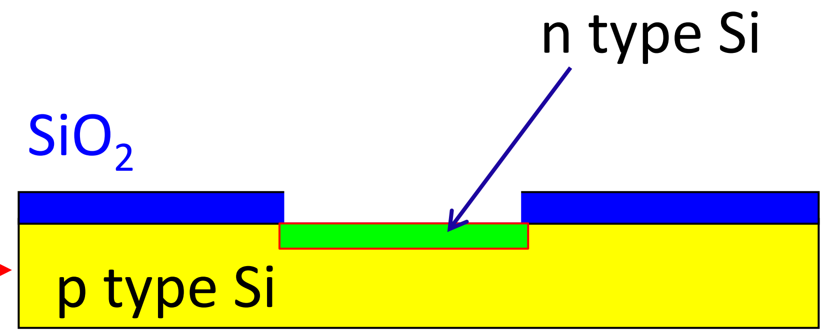


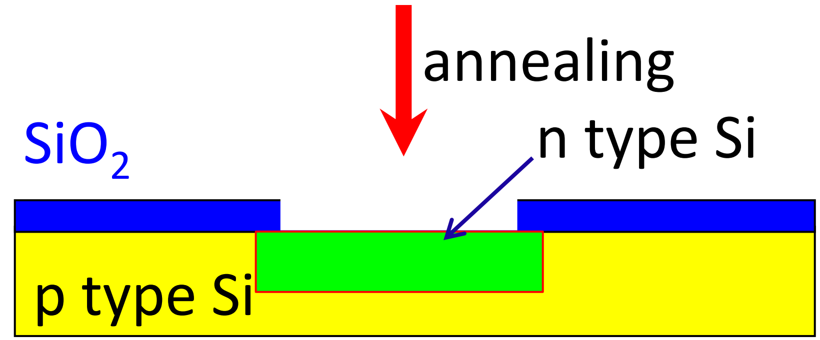
N_D=10^19/cm^3
Brown region
n-type N_D=10^19/cm^3
p-type N_A=10^17/cm^3
n-type N_D=10^15/cm^3
N_A=10^17/cm^3
Green region
SiO2
n type Si
SiO2
PH3
n type Si
n type Si
p type Si
Si
P
B

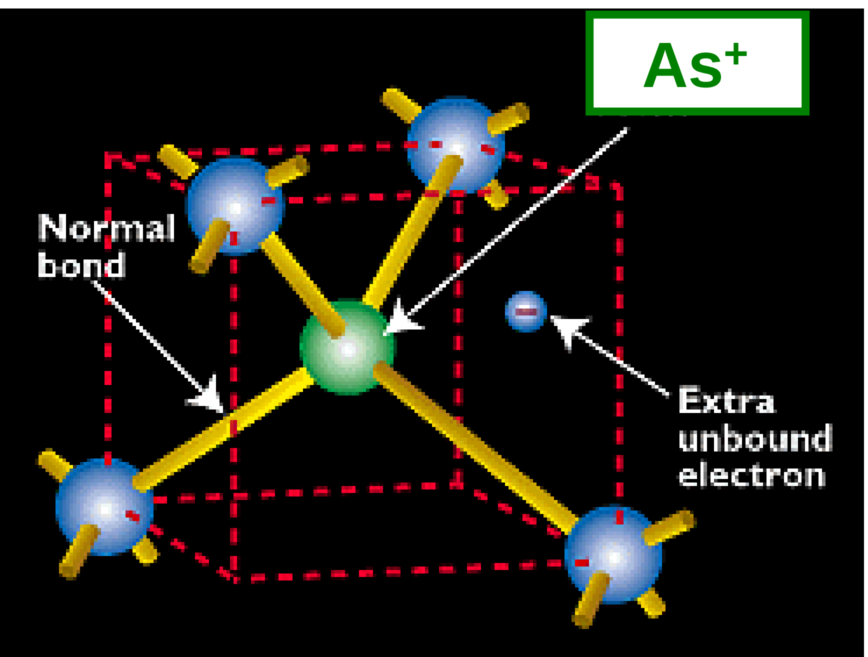
Ion Implantation



As^+ with kinetic energy







Implantation causes

(1) damaged region

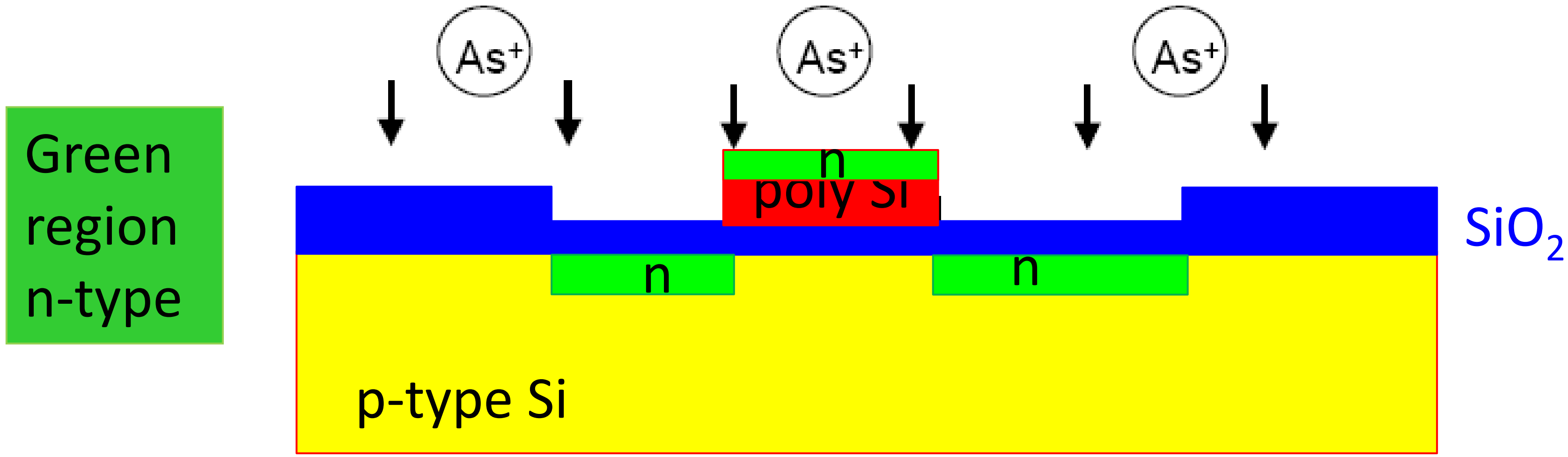
(2) non-substitutional location

Advantages of Ion Implantation

- Precise control of <u>dose</u> and <u>depth</u> profile
- Low-temp. process (can use photoresist as mask)
- Wide selection of masking materials

  e.g. photoresist, oxide, poly-Si, metal
- Less sensitive to surface cleaning procedures
- Excellent lateral dose uniformity (< 1% variation across 12" wafer)

<u>Application example</u>: self-aligned MOSFET source/drain regions



Annealing (Drive-in)

Implantation causes

(1) damaged region and disorder cluster

(2) non-substitutional location

To activate the implanted ions and to restore material properties, the semiconductor must be **annealed**.

Next week:

Fab. Tech. examples