Suggestions & Guidelines for Writing IC Layout Design Report

In the CMOS IC layout design project of EEE201, a formal written report is to be submitted after completing the IC layout drawn by hand on paper. The report carries half of the marks of the whole project. Students are required to write the report in clear English to show and explain the design. Discussions of related semiconductor electronics, circuit principles, design considerations and even engineering practice can be included in relevant sections. Use of essential equations, illustrations with figures or diagrams, images are much encouraged for clear explanations of concepts or ideas so that ordinary readers of the electrical and electronic engineering field can understand the technical contents. The report writing is expected to help student *reflect on* the **engineering design** (including the process itself) of the digital IC layout, consolidating the learning through lectures and self-studies.

Here below is a suggested format of the design report:

- **Title** of the report (descriptive but concise)
- **Author** of the report (student's full name & other key details)
- An abstract of the report (*optional*)
- **Main body**: 1. Introduction
  2. **Circuit Design at Schematic Level**
  3. **IC Layout Design**
  4. CMOS Process for Fabricating the IC (*optional*)
  5. Summary & Conclusion
  6. References
- Appendices: A. Extra contents of schematic circuit design (*optional*)
  B. Extra contents of IC layout design (*optional*)
  C. Extra information about commercial CMOS processes (*optional*)
  D. Layout editing using electronic design automation (EDA) software (*optional*)
  E. Any other extra contents (e.g. learning experience in this design project) (*optional*)

The submitted report is expected to be in legible format (e.g. proper font size and preferably with at 1.5 spacing). While there is no rigid restriction on the number of pages or words for the project report, five pages (excluding any appendices) are expected to be good enough to give a *concise* report of the CMOS IC layout design for readers of ordinary undergraduate students to understand.

Further specific suggestions and guidelines in writing the main body are as follows:

In the **introduction** section, according to your understanding, give an overview of CMOS digital ICs in terms of their importance, applications, economic and technology impact. Then describe the place (or role of any importance) of the **NOR logic gate**[1] in the context of CMOS digital ICs. At the

[1] You can give one or more examples of digital circuits that the NOR logic gate (not necessarily the two-input one) has an essential role, as you learned in the module EEE104 Digital Electronics I.

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end of this section, state explicitly at least one **design goal**[2] based on your understanding of this CMOS IC layout design project. You can also include optionally a couple of additional design goals according to your ambition. This section can be written in just several sentences. It should occupy no more than half a page.

In the section on **Circuit Design at Schematic Level**, give detailed explanations of your design consideration, presumably with a labelled circuit diagram included:

(1). How did you determine the sizes of the NMOS and PMOS transistors? Any consideration of the channel width and length for drawing the IC layout? What is the resulted design?

(2). How is the size determination related to the operation of the CMOS NOR gate?

(3). What performance trade-off have you considered in making your design decisions?

(4). Is your design resulted from much consideration a ***perfect*** one? Why or why not?

(5). What are other alternative circuits to implement the NOR logic gate if not using the CMOS approach? What are the advantages or disadvantages of such implementation compared with the CMOS counterpart?

This section should be about one page. Only one alternative circuit (with a circuit diagram) in Q(5) above is needed in this section. Additional alternatives can be included as appendix A.

In the section on **IC Layout Design**, give detailed explanations of your IC layout design consideration and the resulted IC layout, presumably with examples with images showing part of the layout:

(1). What overall layout optimisations have you adopted (if any)?

(2). What specific layout optimisations have you adopted for minimising the chip area or for increasing the performance (e.g. speed, power consumption)?

(3). What specific layout design consideration (e.g. use of substrate contacts) have you made in reducing the parasitic capacitance, resistance or even inductance? This can be related to Q(2) above.

(4). What layout design rules have you particularly paid attention to when creating your IC layout?

(5). What performance trade-off have you considered in making your layout design decisions?

(6). When attempting to draw the IC layout, did you make any changes to your schematic circuit design decisions? What were those changes? Why?

(7). Is your IC layout resulted from much consideration and optimisation a ***perfect*** one? Why or why not? Is there *one and only unique* ***perfect*** layout for the CMOS NOR gate? Why or why not? How about CMOS digital IC layout in general?

This section should be about three pages, including an image/photo of your hand-drawn IC layout. Examples related to Q(1) to Q(3) should be limited to three while examples related to the layout design rules Q(4) should be no more than five. Any additional examples can be included as appendix B. In total, there should not be more than 10 examples (*representative*/*significant* enough) for illustrating your layout design consideration.

In the ***optional*** section on **CMOS Process for Fabricating the IC**, you can search information about commercial CMOS processes [1]-[4] for making your IC layout into a chip. Based on your information search, describe only several key details of one chosen CMOS process, especially those

[2] One straightforward design goal is to create a CMOS IC layout of the NOR gate compliant to the scalable CMOS design rules and working properly in its circuit operation while occupying a minimum chip area.

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related to the IC layout design consideration (including the transistor sizes determined at the schematic circuit level):

(1). What is the minimum feature size of the CMOS process? What would be resulted minimum channel width and length of the MOS transistors?

(2). Any information about the threshold voltages of the nMOSFETs and the pMOSFETs? Are the voltages the same in magnitude?

(3). Any information about typical or maximum supply voltage (V_{DD}) for the CMOS circuits fabricated using the CMOS process?

(4). How many metal layers available in the CMOS process? Any information about the metal material (e.g. aluminium, copper)?

(5). Why would you choose the CMOS process for fabricating digital circuits of your layout design? Or why not?

(6). What would be the sizes of your overall IC layout of the NOR gate if choosing this CMOS process?

This section should be no more than one page and key details can be included in the form of a table. Any other less important details or information about other commercial CMOS processes can be included as appendix C.

In the **summary and conclusion** section, sum up concisely your IC layout design, particularly a couple of highlights in your design consideration to reach the final design. ***Conclude*** the **design goal**(s) achieved (or failed) in your layout design. This section can be written in just several sentences.

As usual in most technical reports, in the **references** section, list books, papers or websites from which information is taken for writing the reports.

References:

[1]. Semiconductor Manufacturing International Corporation (SMIC), "Mature Logic Technology: 90nm, 0.13/0.11µm, 0.15µm, 0.18µm, 0.25µm, 0.35µm". [online]. Available: https://www.smics.com/en/site/mature_logic. Accessed: 14th November 2020.

[2]. GlobalFoundries, "Mainstream CMOS technologies". [online]. Available: https://www.globalfoundries.com/technology-solutions/cmos/mainstream. Accessed: 14th November 2020.

[3]. Taiwan Semiconductor Manufacturing Company (TSMC), "Logic technology". [online]. Available: https://www.tsmc.com/english/dedicatedFoundry/technology/logic. Accessed: 14th November 2020.

[4]. ON Semiconductor (OnSemi), "Manufacturing Processes". [online]. Available: https://www.onsemi.com/products/product-taxonomy/custom-foundry-services/manufacturing-processes. Accessed: 22nd November 2021.

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