Lecture 10a

of

EEE201

CMOS Digital Integrated Circuits

Department of Electrical & Electronic Engineering

Xi'an Jiaotong-Liverpool University (XJTLU)

Monday, 11th November 2024

- **Logic Inverter VTC**
  - ideal logic inverter
  - voltage transfer characteristics
  - with a resistive load
  - graphical method

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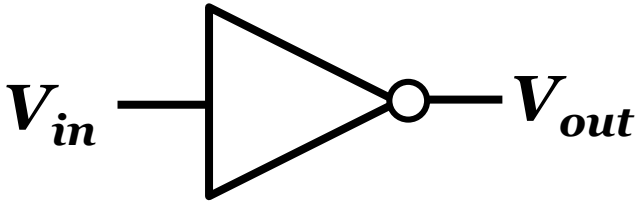
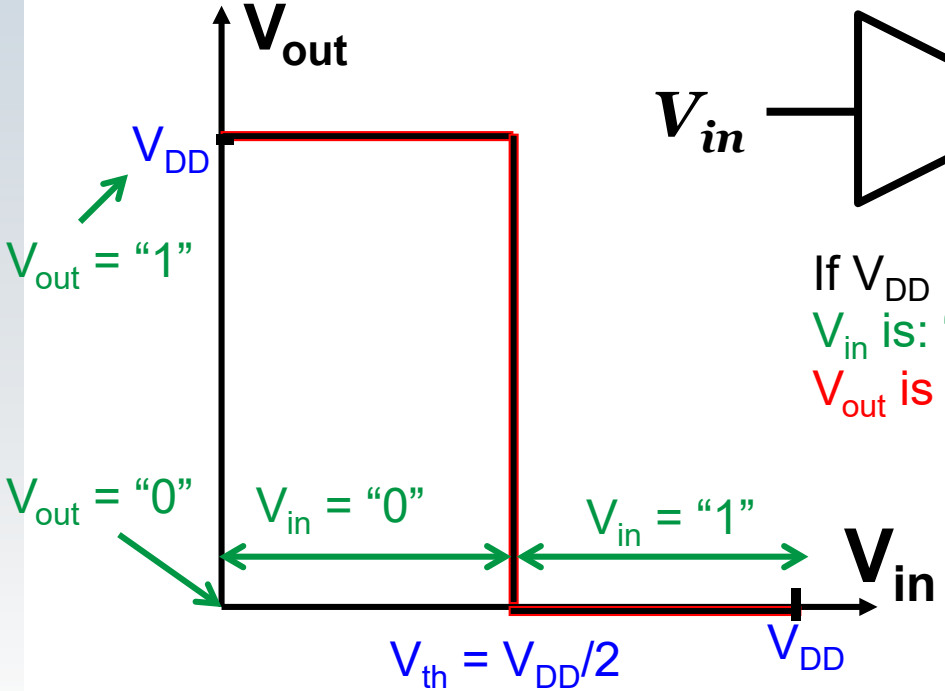
Input-Output Voltage Relation

(ideal logic inverter)

- In *ideal* digital circuits, the logic states "0" and "1" are represented by only two fixed voltages (e.g. 0 V and V_{DD}).
  - In such *ideal* situation, the **input-output voltage relationship** is simple (e.g. in a logic inverter):

V_{in}	V_{out}
0 V	V_{DD}
V_{DD}	0 V





If V_{DD} = 5V, V_{in} = 2V, then

V_{in} is: "0" [redacted]

V_{out} is : "1" [redacted]

nMOSFET: V_{Tn}

pMOSFET: V_{Tp}

inverter: V_{th}

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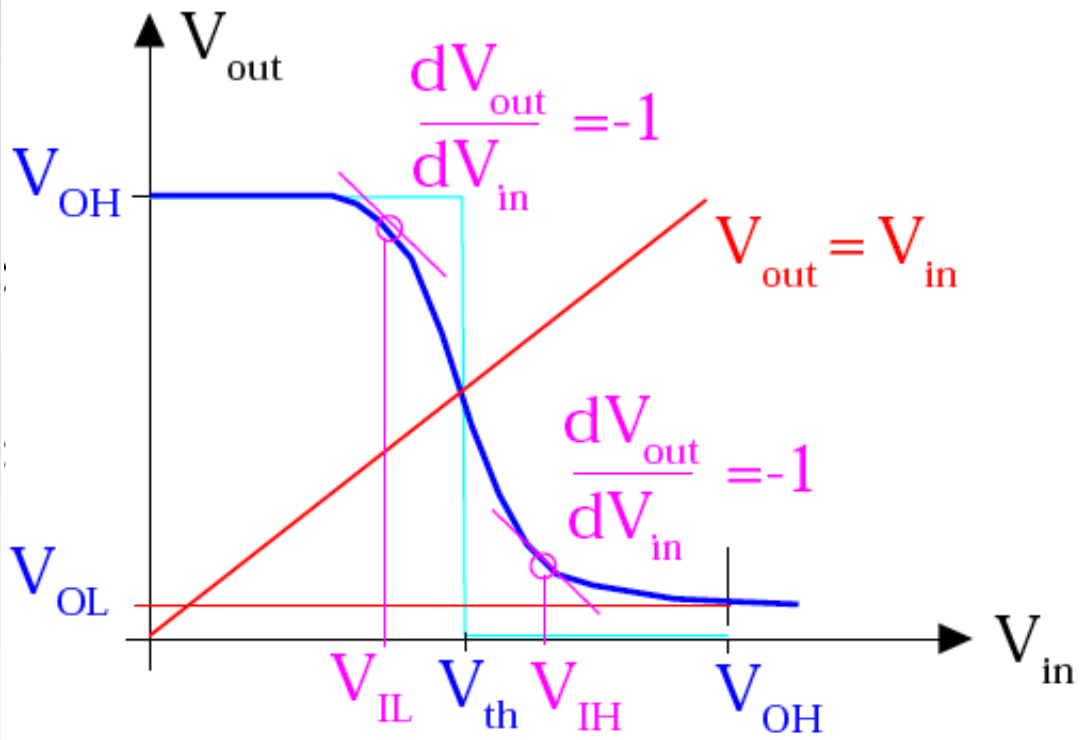
Input-Output Voltage Relation

(real logic inverter)

- In ***real*** digital circuits, there is a ***continuous*** range of voltages for the logic states "0" and "1". And MOS transistors are not ideal **switches**.



- The **input-output voltage relationship** will fall short of the ideal.
- representative case of the logic inverter: **voltage transfer characteristics**

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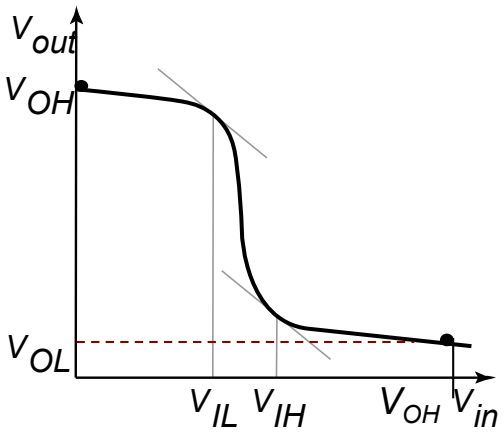
Voltage Transfer Characteristics

(key voltage quantities)

- To specify clearly the **voltage transfer characteristics** (**VTC**), several key voltage quantities need to be defined:
  - V_{OH}: max output voltage when output is logic "1"
  - V_{OL}: min output voltage when output is logic "0"
  - V_{IL}: max input voltage which can be interpreted as "0"
  - V_{IH}: min input voltage which can be interpreted as "1"



- The definitions apply to not only the logic inverter but also other logic gates.
- Note the **threshold voltage V_{th}** of the logic inverter in the transition region of the VTC.

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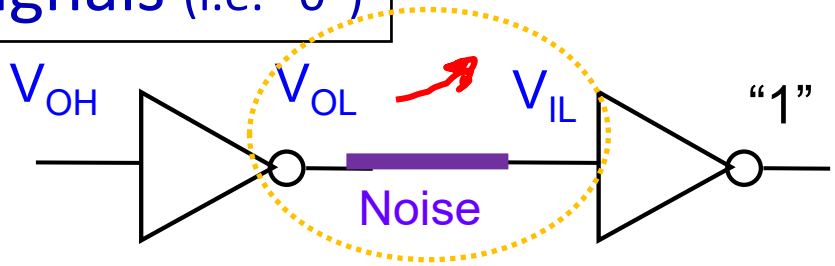
Noise Margins in Logic Voltages

(for logic "0" & "1")

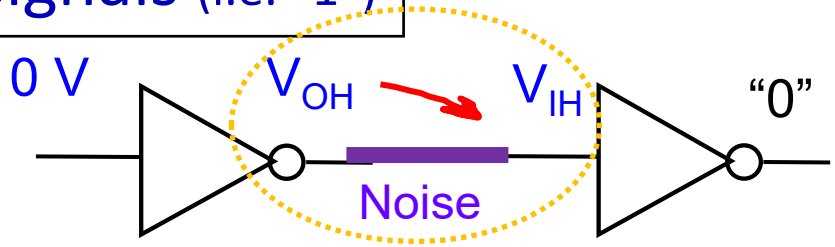
noise margin for "low" signals (i.e. "0")

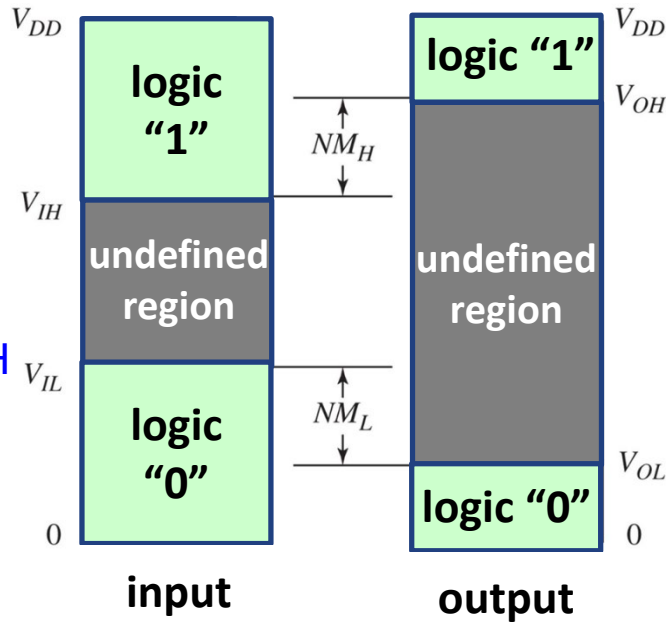
$NM_L = V_{IL} - V_{OL}$



noise margin for "high" signals (i.e. "1")

$NM_H = V_{OH} - V_{IH}$





The **noise margins** (and the key voltages) are part of the **design consideration**.

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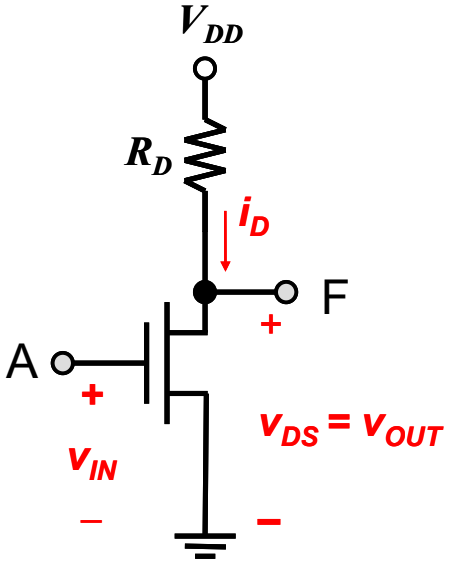
VTC of Logic Inverter

(nMOSFET with a resistor load)

- To determine the VTC of the logic inverter, we will use the simple implementation of an nMOSFET with a resistor load to illustrate the techniques:
  - graphical method & solving simultaneous equations
  - In the CMOS logic inverter, the circuit analysis is more complicated.



- One key step is to understand the three major operation modes of the MOSFET: cut-off, triode (linear), and saturation.
- The resistor load has only one "mode": one equation to define the voltage and current. (What is that "mode"?)

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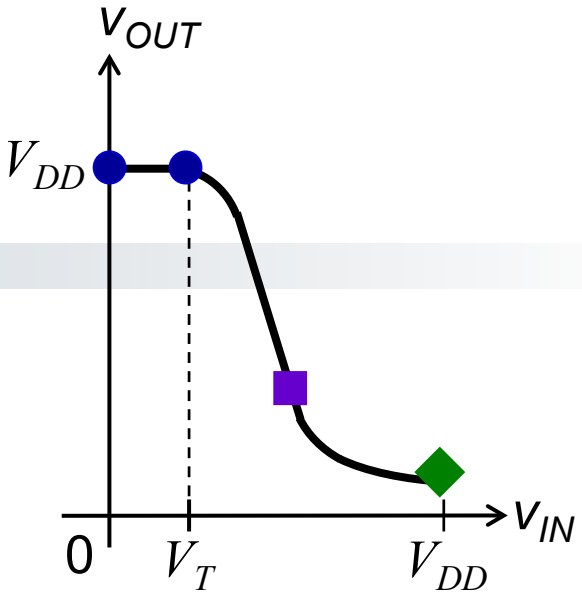
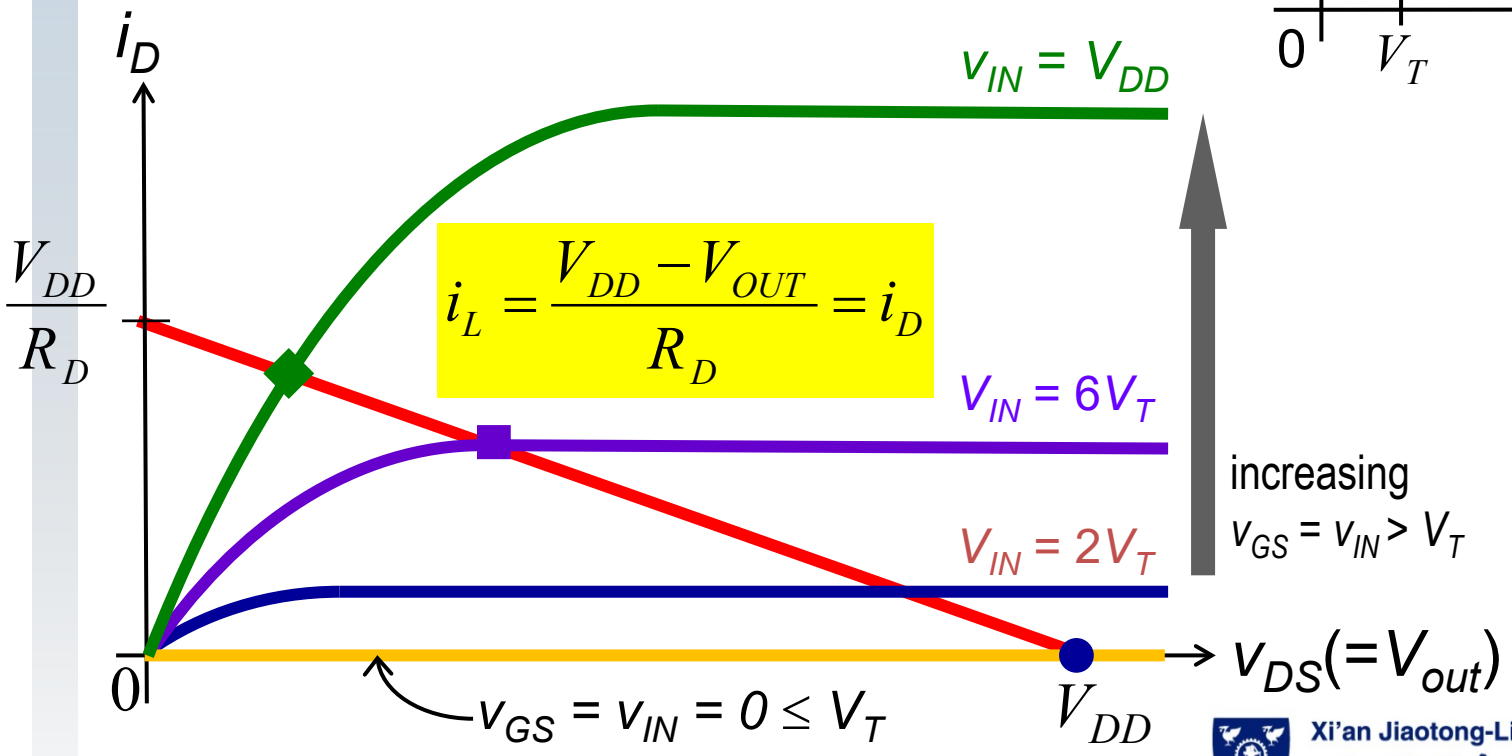
VTC of Logic Inverter

(graphical method)



- Resistor's I-V curves & nMOSFET's
  - intersection points of the VTC



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