Am25LS2516

Eight-Bit by Eight-Bit Serial/Parallel Multiplier with Accumulator

DISTINCTIVE CHARACTERISTICS

- Two's complement, two-bit lookahead carry-save arithmetic
- Microprogrammable — four-bit instruction code for load, multiply, and read operations
- Cascadable, two devices perform full 16-bit multiplication without additional hardware
- Eight-bit byte parallel, bidirectional, bussed I/O
- On-chip registers and double length accumulator
- Overflow indicator
- Three-state shared bus input/output lines
- High-speed architecture provides clock rates of 20MHz (Typ)

RELATED PRODUCTS

Part No.	Description	Page
Am25S05		
Am25LS14A		
Am25S557/8		
Am29516/7		

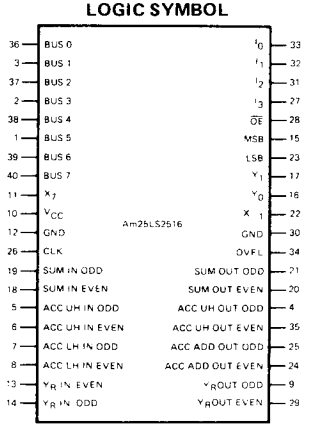
FUNCTIONAL DESCRIPTION

The Am25LS2516 is an eight-bit by eight-bit multiplier and accumulator employing serial/parallel, two's complement, carry-save arithmetic to deliver a 16-bit product in eight clock cycles. The device is fully cascadable for use in high-speed, real-time, digital signal processing applications.

The device includes an eight-bit X Register prior to the X latch providing X hold for chain or overlapping calculations. The X and Y registers are loaded by clocking prior to the beginning of a multiply cycle, the data supplied by the bidirectional bus or the accumulator register. The double length, 16-bit output is multiplexed onto the eight-bit bus; either the upper or lower halves of the result can be read at any one time.

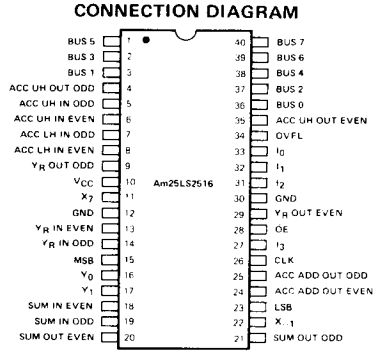
The accumulator and the Y register are both organized as dual-rank shift registers, allowing them to shift two bits at a time. The serial inputs and outputs of the Y register, the low and high order halves of the accumulator and the two-bit serial accumulator adder output, both serially and in parallel, are all available at external pins to provide cascadability.

LOGIC SYMBOL



MPR-336

CONNECTION DIAGRAM



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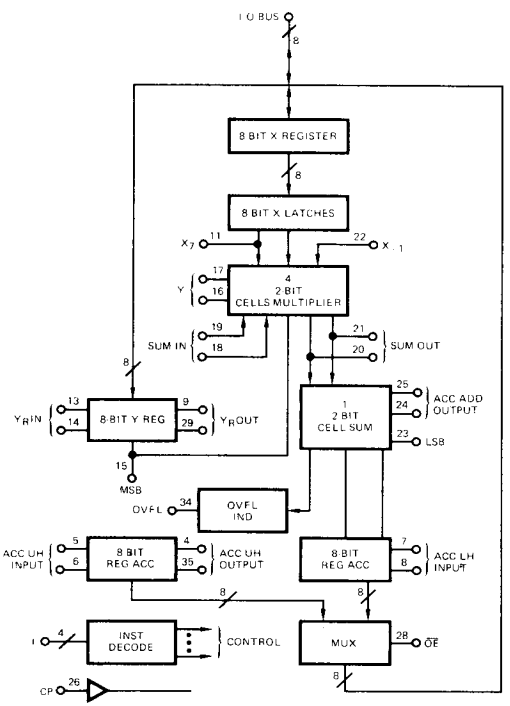
LOGIC DIAGRAM



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ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L	T_A = 0°C to +70°C	V_{CC} = 5.0V ±5%	MIN. = 4.75V	MAX. = 5.25V
MIL	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%	MIN. = 4.50V	MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

(Bus Inputs/Outputs)

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1.0mA	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA			0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V				−0.8	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				60	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				0.2	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−30		−100	mA
I_{OZ}	Off-State (HIGH Impedance) Output Current	V_{CC} = MAX.	V_O = 2.4V			60	μA
			V_O = 0.4V			−800	

Non-Bus Inputs/Outputs

V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −440μA	MIL	2.5			Volts
				COM'L	2.7			
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	Y_R OUT, I_{OL} = 15mA				0.5	Volts
			Others I_{OL} = 4.0mA				0.4	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	Y_0, Y_1				0.8	Volts
			Others, MIL				0.7	
			Others, COM'L				0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V			See Table 1			mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V			See Table 1			μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V			See Table 1			mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−85		mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.			285	390		mA

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Pins 28 and 31 HIGH, all other inputs at GND. Test after one full clock cycle of LOW-HIGH-LOW.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Case) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +6.3V
DC Voltage Applied to Outputs for High Output State	−0.5V to + V_{CC} max.
DC Input Voltage (Pins 5, 6, 7, 8, 18, 19, 26)	−0.5V to +5.5V
DC Input Voltage (Other pins)	−0.5V to +7.0V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

TABLE I.

Terminals	I_{IL}	I_{IH}	I_I
Y IN	−.3mA	20μA	.1mA
I_0, I_1, I_3, OE	−.45mA	20μA	.1mA
Bus 0-7	−.6mA	90μA	.3mA
CP	−.8mA	80μA	.4mA
I_2, X_{-1}	−.9mA	40μA	.1mA
SUM IN	−1.4mA	80μA	.5mA
LSB	−1.6mA	80μA	.4mA
ACC IN all	−2mA	50μA	1mA
MSB	−3mA	150μA	1.5mA
Y_0, Y_1	−7.5mA	200μA	2mA

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	0°C to +70°C	AM25LS2516DC
	−55°C to +125°C	AM25LS2516DM (Note 1)

Note 1. Military temperature range product in development.

SWITCHING CHARACTERISTICS

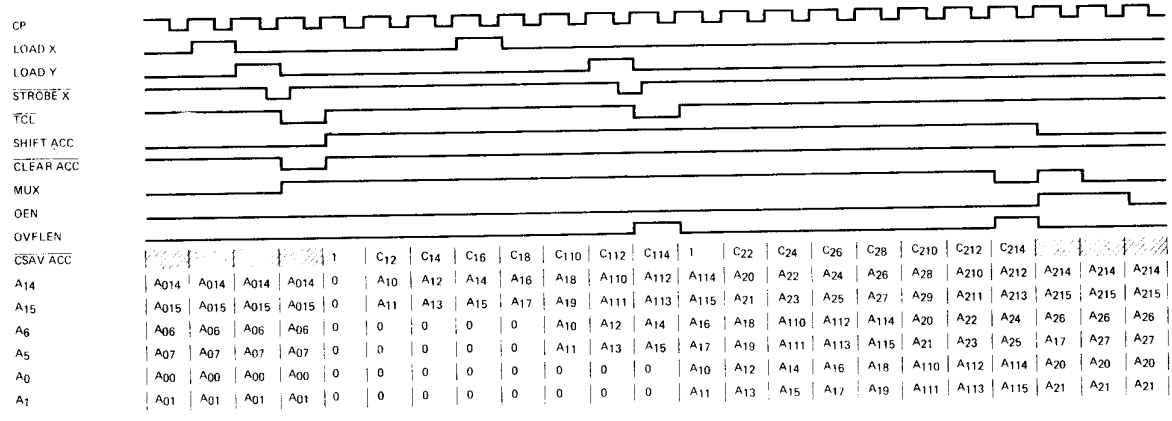
(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	Y_R Register OUT		12	18	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}			15	23		
t_{PLH}	SUM OUT		13	20	ns	
t_{PHL}			15	23		
t_{PLH}	ACC ADDER OUT		27	41	ns	
t_{PHL}			27	41		
t_{PLH}	ACC UH OUT		11	17	ns	
t_{PHL}			13	20		
t_{PLH}	ACC Bus		23	34	ns	
t_{PHL}			17	26		
t_{PLH}	$\overline{OVFL}$		12	18	ns	
t_{PHL}			15	23		
t_{PLH}	X_7		13	20	ns	
t_{PHL}			17	26		
t_{ZH}	$\overline{OE}$ to Bus		12	18	ns	
t_{ZL}			9	14		
t_{HZ}			24	36	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}			12	18		
t_s	X Register (Bus)	20			ns	C_L = 15pF, R_L = 2.0kΩ
t_s	Y Register (Bus)	15			ns	
t_s	X_{-1}	35			ns	
t_s	SUM IN	37			ns	
t_s	Y Register (Serial)	20			ns	
t_s	ACC LH or UH IN	8			ns	
t_s	Multiplier Y_0 and Y_1	33			ns	
t_s	Instruction	25			ns	
t_h	SUM IN, X_{-1}, Multiplier Y_0 and Y_1	0			ns	
t_h	I_{0-3} Hold Time	10			ns	
t_h	Hold Time on All Other Inputs	5			ns	
f_{max} (Note 1)	Maximum Clock Frequency	17			MHz	

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

TIMING DIAGRAMS

	HOLD			SHIFT								SHIFT								HOLD			
FUNCTION	NOP	LDX	LDY CLA	MPY	MPY	MPY	MPY	MPY	LDX	MPY	LDY	MPY	MPY	MPY	MPY	MPY	MPY	MPY	MPY	NOP	RUH	RLH	NOP
CP	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
I_3																							
I_2																							
I_1																							
I_0																							
BUS	Z	X_1	Y_1	Z	Z	Z	Z	Z	X_2	Z	Y_2	Z	Z	Z	Z	Z	Z	Z	Z	Z	A_U	A_L	Z
X_7	X_{07}	X_{07}	X_{07}	X_{17}	X_{17}	X_{17}	X_{17}	X_{17}	X_{17}	X_{17}	X_{17}	X_{27}	X_{27}	X_{27}	X_{27}	X_{27}	X_{27}	X_{27}	X_{27}	X_{27}	X_{27}	X_{27}	X_{27}
Y OUT EVEN	Y_{07}	Y_{07}	Y_{07}	Y_{10}	Y_{12}	Y_{14}	Y_{16}	Y_{17}	Y_{17}	Y_{17}	Y_{17}	Y_{20}	Y_{22}	Y_{24}	Y_{26}	Y_{27}	Y_{27}	Y_{27}	Y_{27}	Y_{27}	Y_{27}	Y_{27}	Y_{27}
Y OUT ODD	Y_{07}	Y_{07}	Y_{07}	Y_{11}	Y_{13}	Y_{15}	Y_{17}	Y_{17}	Y_{17}	Y_{17}	Y_{17}	Y_{21}	Y_{23}	Y_{25}	Y_{27}	Y_{27}	Y_{27}	Y_{27}	Y_{27}	Y_{27}	Y_{27}	Y_{27}	Y_{27}
SUM OUT EVEN					P_{10}	P_{12}	P_{14}	P_{16}	P_{18}	P_{110}	P_{112}	P_{114}	P_{20}	P_{22}	P_{24}	P_{26}	P_{28}	P_{210}	P_{212}	P_{214}				
SUM OUT ODD					P_{11}	P_{13}	P_{15}	P_{17}	P_{19}	P_{111}	P_{113}	P_{115}	P_{21}	P_{23}	P_{25}	P_{27}	P_{29}	P_{211}	P_{213}	P_{215}				
ACC ADD OUT EVEN					A_{10}	A_{12}	A_{14}	A_{16}	A_{18}	A_{110}	A_{112}	A_{114}	A_{20}	A_{22}	A_{24}	A_{26}	A_{28}	A_{210}	A_{212}	A_{214}				
ACC ADD OUT ODD					A_{11}	A_{13}	A_{15}	A_{17}	A_{19}	A_{111}	A_{113}	A_{115}	A_{21}	A_{23}	A_{25}	A_{27}	A_{29}	A_{211}	A_{213}	A_{215}				
ACC UH OUT EVEN	A_{08}	A_{08}	A_{08}	A_{08}	0	0	0	0	A_{10}	A_{12}	A_{14}	A_{16}	A_{18}	A_{110}	A_{112}	A_{114}	A_{20}	A_{22}	A_{24}	A_{26}	A_{28}	A_{28}	A_{28}
ACC UH OUT ODD	A_{09}	A_{09}	A_{09}	A_{09}	0	0	0	0	A_{11}	A_{13}	A_{15}	A_{17}	A_{19}	A_{111}	A_{113}	A_{115}	A_{21}	A_{23}	A_{25}	A_{27}	A_{29}	A_{29}	A_{29}
$\overline{OVFL}$	F_0	F_0	F_0	F_0	0	0	0	0	0	0	0	0	F_1	F_1	F_1	F_1	F_1	F_1	F_1	F_1	F_2	F_2	F_2



$\overline{CSAV\ ACC}$					1	C_{12}	C_{14}	C_{16}	C_{18}	C_{110}	C_{112}	C_{114}	1	C_{22}	C_{24}	C_{26}	C_{28}	C_{210}	C_{212}	C_{214}				
A_{14}	A_{014}	A_{014}	A_{014}	A_{014}	0	A_{10}	A_{12}	A_{14}	A_{16}	A_{18}	A_{110}	A_{112}	A_{114}	A_{20}	A_{22}	A_{24}	A_{26}	A_{28}	A_{210}	A_{212}	A_{214}	A_{214}	A_{214}
A_{15}	A_{015}	A_{015}	A_{015}	A_{015}	0	A_{11}	A_{13}	A_{15}	A_{17}	A_{19}	A_{111}	A_{113}	A_{115}	A_{21}	A_{23}	A_{25}	A_{27}	A_{29}	A_{211}	A_{213}	A_{215}	A_{215}	A_{215}
A_6	A_{06}	A_{06}	A_{06}	A_{06}	0	0	0	0	0	A_{10}	A_{12}	A_{14}	A_{16}	A_{18}	A_{110}	A_{112}	A_{114}	A_{20}	A_{22}	A_{24}	A_{26}	A_{26}	A_{26}
A_5	A_{07}	A_{07}	A_{07}	A_{07}	0	0	0	0	0	A_{11}	A_{13}	A_{15}	A_{17}	A_{19}	A_{111}	A_{113}	A_{115}	A_{21}	A_{23}	A_{25}	A_{17}	A_{27}	A_{27}
A_0	A_{00}	A_{00}	A_{00}	A_{00}	0	0	0	0	0	0	0	0	A_{10}	A_{12}	A_{14}	A_{16}	A_{18}	A_{110}	A_{112}	A_{114}	A_{20}	A_{20}	A_{20}
A_1	A_{01}	A_{01}	A_{01}	A_{01}	0	0	0	0	0	0	0	0	A_{11}	A_{13}	A_{15}	A_{17}	A_{19}	A_{111}	A_{113}	A_{115}	A_{21}	A_{21}	A_{21}

KEY:
////// Data invalid

Note: Variables shown are general.
For this example:

$P_1 = X_1Y_1 \quad A_1 = P_1 \quad F_1 = 0$
$P_2 = X_2Y_2 \quad A_2 = P_1 + P_2$

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Am25LS COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ±5% Min.	Am25LS COM'L Max.	Am25LS MIL T_A = −55°C to +125°C V_{CC} = 5.0V ±10% Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	YR Register OUT		24		26	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}			33		37		
t_{PLH}	SUM OUT		27		27	ns	
t_{PHL}			34		34		
t_{PLH}	ACC ADDER OUT		50		52	ns	
t_{PHL}			57		60		
t_{PLH}	ACC UH OUT		23		23	ns	
t_{PHL}			30		30		
t_{PLH}	ACC Bus		42		45	ns	
t_{PHL}			38		39		
t_{PLH}	$\overline{OVFL}$		26		26	ns	
t_{PHL}			33		33		
t_{PLH}	X_7		30		33	ns	
t_{PHL}			39		42		
t_{ZH}	$\overline{OE}$ to Bus		30		33	ns	C_L = 50pF, R_L = 2.0kΩ
t_{ZL}			21		23	ns	
t_{HZ}			45		55	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}			21		30	ns	
t_S	X Register (Bus)	20		22		ns	C_L = 50pF, R_L = 2.0kΩ
t_S	Y Register (Bus)	15		17		ns	
t_S	X_{-1}	45		51		ns	
t_S	SUM IN	52		62		ns	
t_S	Y Register (Serial)	20		20		ns	
t_S	ACC LH or UH IN	10		14		ns	
t_S	Multiplier Y_0 and Y_1	44		51		ns	
t_S	Instruction	27		30		ns	
t_H	SUM IN, X_{-1}, Multiplier and Y_1	0		0		ns	
t_H	I_{0-3} Hold Time	10		10		ns	
t_H	All Other Inputs	5		5		ns	
f_{max} (Note 1)	Maximum Clock Frequency	15.5		10		MHz	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

The following table provides a guide to the improvement in performance which may be obtained by control of the V_{CC} power supply.

	V_{CC} = 5.0V	V_{CC} = 5.0V ±5%	V_{CC} = 5.0V ±10%
T_A = 25°C	17MHz	16MHz	15MHz
T_A = 0°C to +70°C	16MHz	15.5MHz	–
T_C = −55°C to +125°C	12MHz	–	10MHz

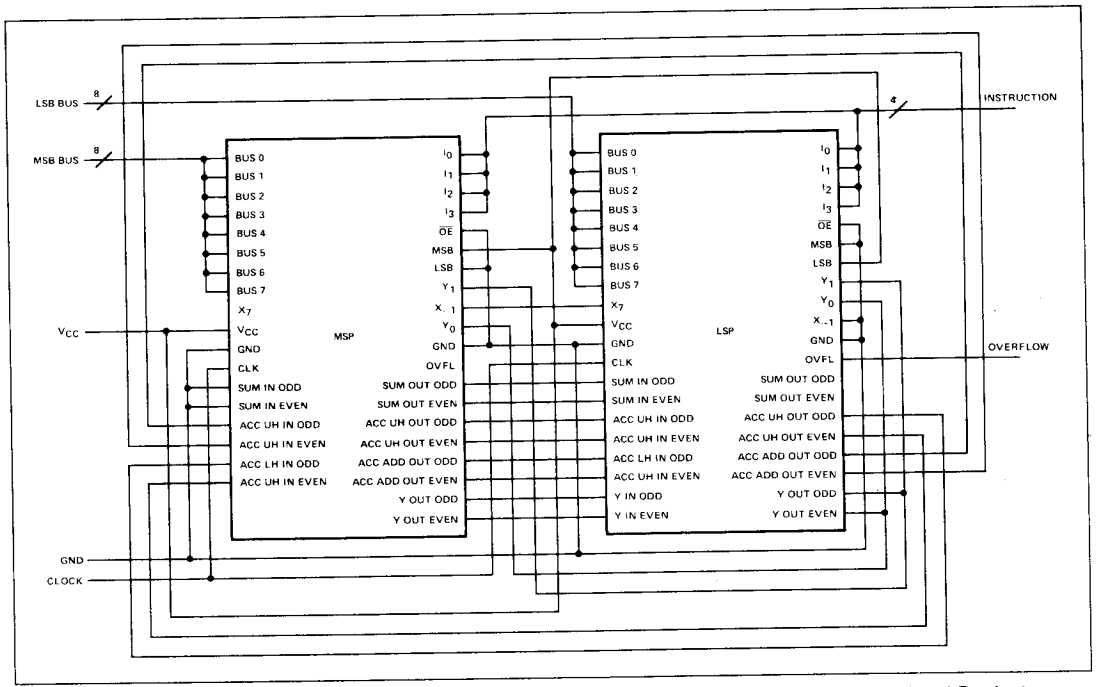


Figure 5b. Two Devices Cascaded in 16-Bit by 16-Bit Multiplier Application with 32-Bit Accumulated Product.

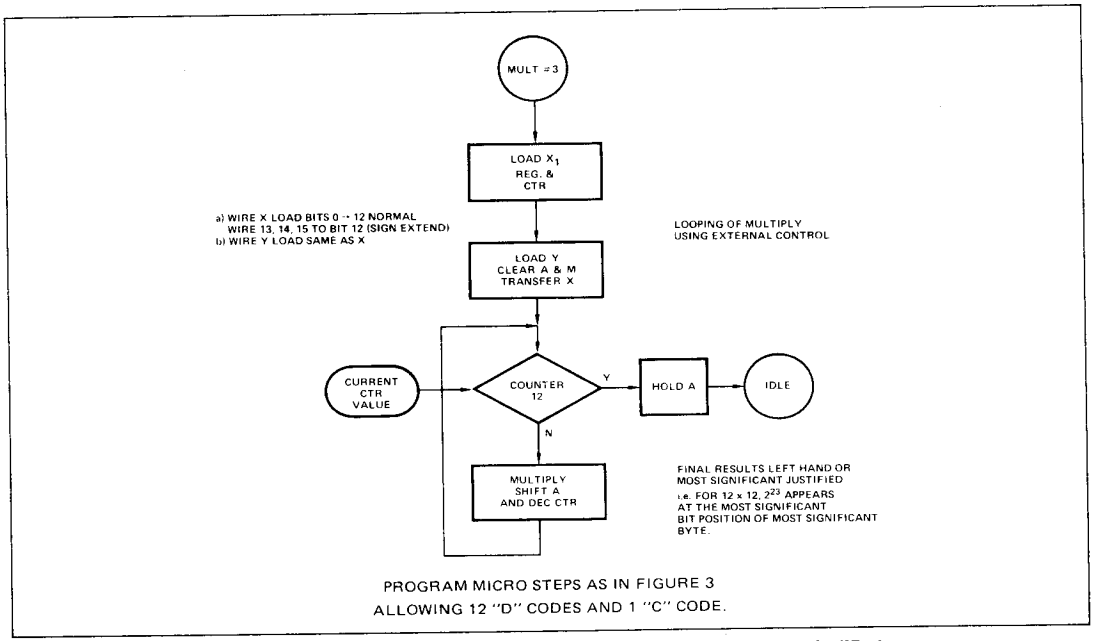


Figure 6. 16 Bit Two's Complement Multiply without Accumulate Modified to 12 x 12 (Using Two Am25LS2516 Devices Interconnected).

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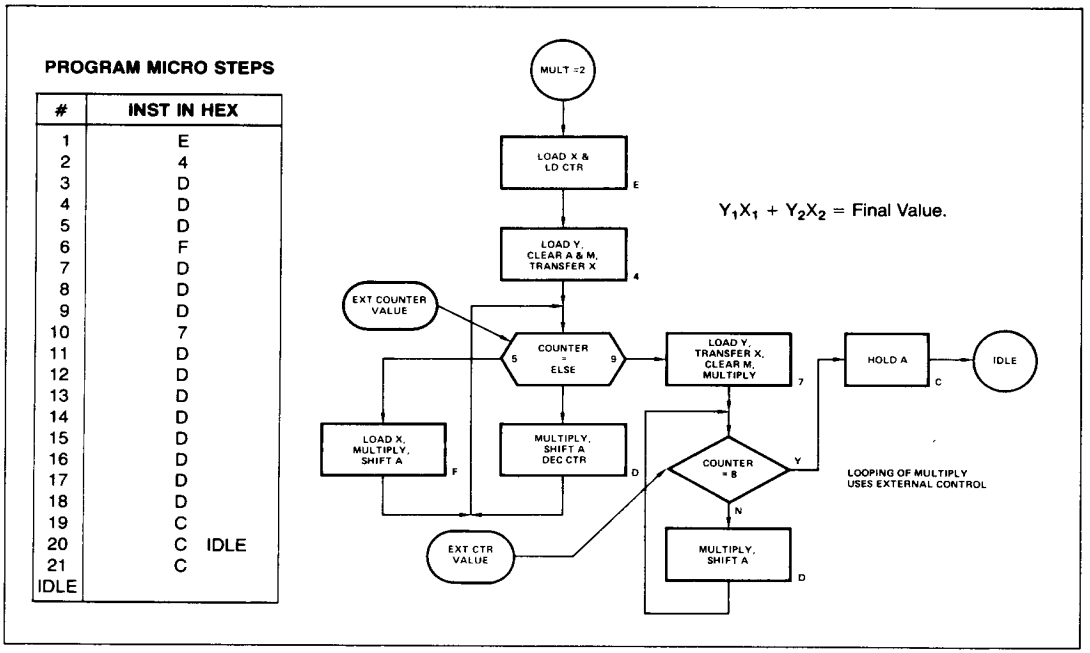

Figure 4. 8-Bit Two's Complement Multiply with Accumulate, Intermediate Load and Chain Calculations.

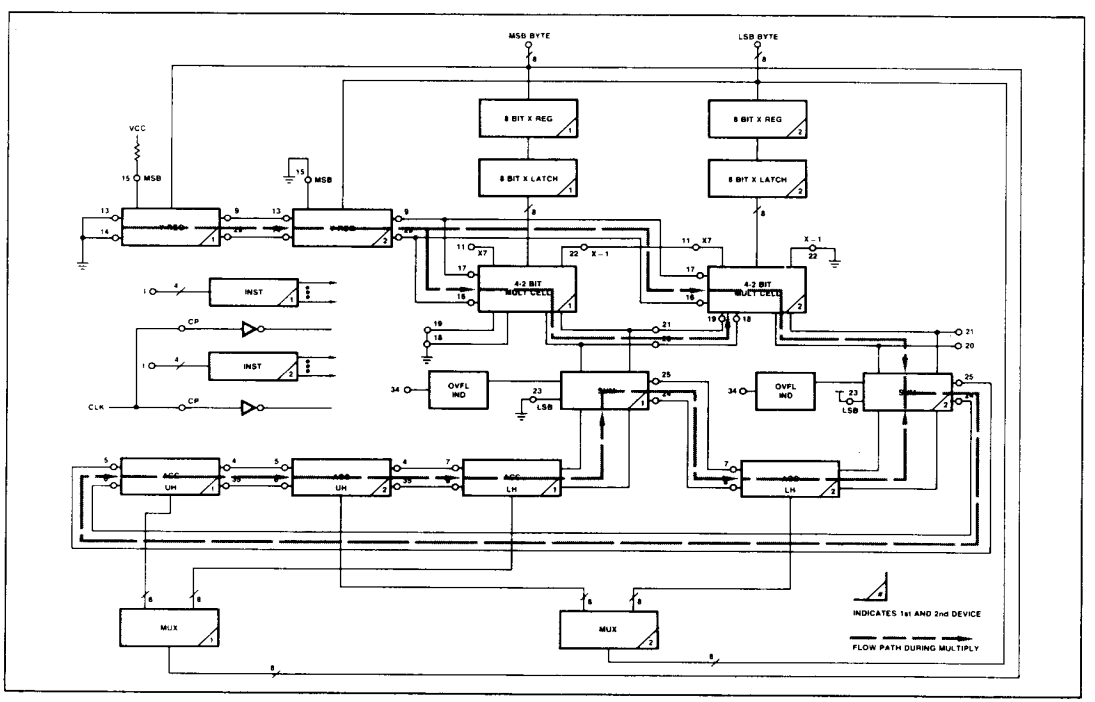

Figure 5a. Interconnection of Two Am25LS2516 (8 x 8 Multiplier) Devices to Execute a 16 x 16 Multiply.

FUNCTION TABLE

Mnemonic	I_3 I_2 I_1 I_0	Function	CLR M	LOAD X	LOAD Y	XFER X	CLR A*	SHFT A	MUX	OE	Remarks
YLHC	0 0 0 0	LHA → Y, XFER X, CLR A CLR M, READ OVFL	1	0	1	1	0	0	0	1	
YUHC	0 0 0 1	UHA → Y, XFER X, CLR A CLR M, READ OVFL	1	0	1	1	0	0	1	1	
YLHA	0 0 1 0	LHA → Y, XFER X CLR M, READ OVFL	1	0	1	1	1	0	0	1	
YUHA	0 0 1 1	UHA → Y, XFER X CLR M, READ OVFL	1	0	1	1	1	0	1	1	
LYCA	0 1 0 0	LOAD Y, XFER X, CLR A, CLR M	1	0	1	1	0	0	0	0	Same Func. as 0101
LYCA	0 1 0 1	CLR A LOAD Y, XFER X, CLR M	1	0	1	1	0	1	1	0	Same Func. as 0100
LYHA	0 1 1 0	LOAD Y, XFER X, HOLD A, CLR M	1	0	1	1	1	0	0	0	
LYSA	0 1 1 1	LOAD Y, XFER X, SHIFT A CLR M, MULTIPLY	1	0	1	1	1	1	1	0	OVFLEN in Next State
RLHA	1 0 0 0	READ LHA READ OVFL	0	0	0	0	1	0	0	1	
RUHA	1 0 0 1	READ UHA READ OVFL	0	0	0	0	1	0	1	1	
XLHA	1 0 1 0	LHA → X READ OVFL	0	1	0	0	1	0	0	1	
XUHA	1 0 1 1	UHA → X READ OVFL	0	1	0	0	1	0	1	1	
HLDA	1 1 0 0	HOLD A OVFLEN AFTER MULT	0	0	0	0	1	0	0	0	Must Prc'd Any Output
MULT	1 1 0 1	MULTIPLY SHIFT A	0	0	0	0	1	1	1	0	
LXHA	1 1 1 0	LOAD X, HOLD A	0	1	0	0	1	0	0	0	
LXSA	1 1 1 1	LOAD X, SHIFT A MULTIPLY	0	1	0	0	1	1	1	0	

*Active LOW

Am25LS
LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

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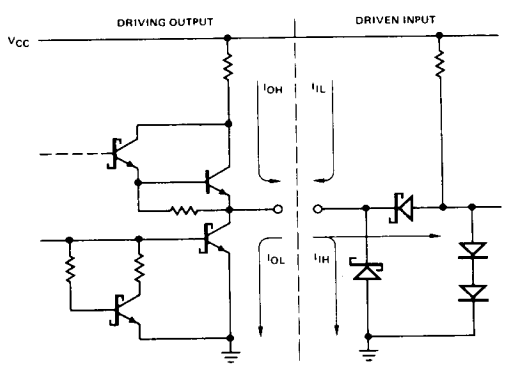
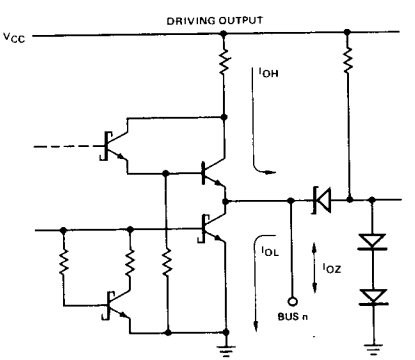
Other Outputs



Bus Outputs



Note: Actual current flow direction shown

DEFINITION OF FUNCTIONAL TERMS

Bus 0-Bus 7 – Bi-directional 8-bit data bus.

X_7 – Interconnection link to more significant byte if cascading (output).

X_{-1} – Interconnecting link between devices to least significant byte if cascading (input) link X7 to X1 to cascade – must be ground if not used.

Accum Upper Half out, even – Accumulator output upper byte, even bit.

Accum Upper Half out, odd – Accumulator output upper byte, odd bit.

Accum Upper Half input even – Accumulator input, upper byte, even bit.

Accum Upper Half input odd – Accumulator input, upper byte, odd bit.

Accum Lower Half input even – Accumulator input, lower byte, even bit.

Accum Lower Half input odd – Accumulator input, lower byte, odd bit.

YR out even – "Y" register output, even (link to "Y0").

YR out odd – "Y" register output, odd (link to "Y1").

YR in even – "Y" register input, even (link for cascading) ground when not used.

YR in odd – "Y" register input, odd (link for cascading) ground when not used.

Y_1 – Multiplier odd input (link to Y register odd).

Y_0 – Multiplier even input (link to Y register even).

Sum in even – Multiplier input even for cascading link to more significant byte, for standalone, ground.

Sum in odd – Multiplier input odd for cascading link to more significant byte, for standalone, ground.

Sum out even – Multiplier output even (link to sum in even for cascading) can be used directly.

Sum out odd – Multiplier output odd (link to sum output odd for cascading) can be used directly.

Acc Add out, even – Adder output even, for LSB (Hi) output equal sum of Accum and multiplier, for LSB (low) output equal sum of accumulator and zero.

Acc Add out, odd – Same as above except odd bit instead of even.

LSB – Control for summing adder – See Accumulator Add outputs for definition.

I_0-I_3 – 4-bit instruction field – provide cycle for cycle control of device function.

OVFL – Stored overflow indicator used only on least significant byte. Requires proper execution of instruction to operate.

MSB – Control for "Y" reg. and multiplier to indicate Most Significant Byte – Activates sign extension and negative waiting for 2's compliment – Low for lesser significant bytes and High for Most Significant Byte only.

CP – Clock Pulse.

$\overline{OE}$ – 3 state enable for Bus 0-Bus 7 outputs.