MOSTEK®

16K-BIT READ ONLY MEMORY

MK34000(P/J/N)-3

FEATURES

- ☐ 2K x 8 organization with static interface
- ☐ 350ns max access time
- ☐ Single +5V ±10% power supply
- ☐ 330mW max power dissipation
- ☐ Contact programmed for fast turn-around
- ☐ Three programmable chip selects
- ☐ Inputs and three-state outputs — TTL compatible
- ☐ Outputs drive 2 TTL loads and 100pF
- ☐ RAM/EPROM pin compatible
- ☐ Pin compatible with Mostek's BYTEWYDE™ Memory Family

ROMS

DESCRIPTION

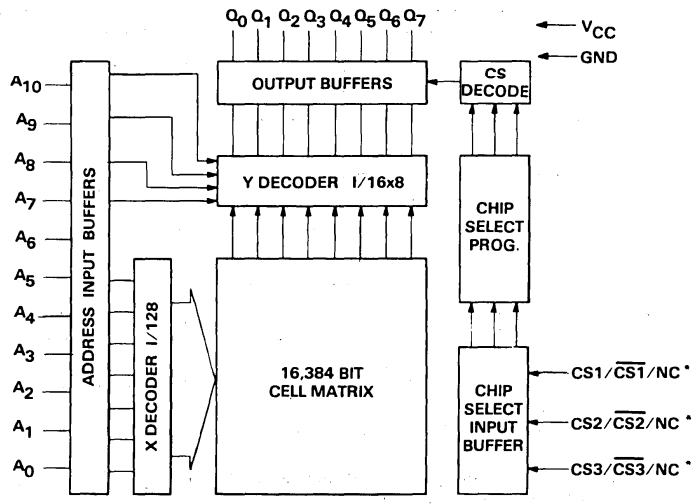
The MK34000 is a new generation N-channel silicon gate MOS Read Only Memory circuit organized as 2048 words by 8 bits. As a state-of-the-art device, the MK34000 incorporates advanced circuit techniques designed to provide maximum circuit density and reliability with highest possible performance, while maintaining low power dissipation and wide operating margins.

The MK34000 requires a single +5 volt (±10% tolerance) power supply and has complete TTL compatibility at all inputs and outputs (a feature made possible by Mostek's Ion-implantation technique). The three chip select inputs can be programmed for any desired combination of active high's or low's or even an optional "DON'T CARE" state. The convenient static operation of the MK34000 coupled with the programmable chip select inputs and three-state TTL compatible outputs results in extremely simple interface requirements.

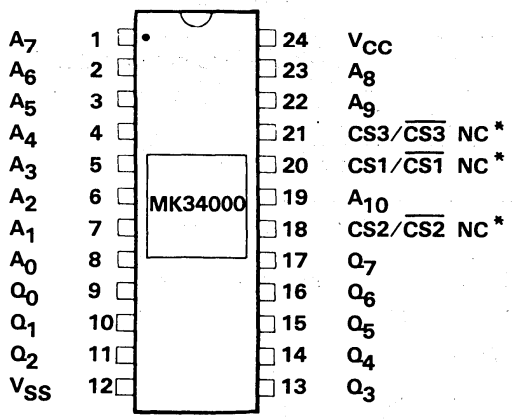
An outstanding feature of the MK34000 is the use of contact programming over gate mask programming. Since the contact mask is applied at a later processing stage, wafers can be partially processed and stored. When an order is received, a contact mask, which represents the desired bit pattern, is generated and applied to the wafers. Only a few processing steps are left to complete the part. Therefore, the use of contact programming reduces the turnaround time for a custom ROM.

Any application requiring a high performance, high bit density ROM can be satisfied by this device. The MK34000 is ideally suited for 8-bit microprocessor systems such as those which utilize the Z80 or F8. The MK34000 also provides significant cost advantages over PROM.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



*Programmable Chip Selects

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Terminal Relative to V_{SS} ..... -0.5V to +7V
Operating Temperature T_A (Ambient) ..... 0°C to +70°C
Storage Temperature - Ceramic (Ambient) ..... -65°C to +150°C
Storage Temperature - Plastic (Ambient) ..... -55°C to +125°C
Power Dissipation ..... 1 Watt

*Stresses greater than these listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(V_{CC} = 5V ±10%; 0°C ≤ T_A ≤ +70°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V	6
V_{IL}	Input Logic 0 Voltage	-0.5		0.8	V	
V_{IH}	Input Logic 1 Voltage	2.0		V_{CC}	V	

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%; 0°C ≤ T_A ≤ +70°C) [6]

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC}	V_{CC} Power Supply Current		60	mA	1
$I_{I(L)}$	Input Leakage Current		10	μA	2
$I_{O(L)}$	Output Leakage Current		10	μA	3
V_{OL}	Output Logic 0 Voltage @ I_{OUT} = 3.3mA		0.4	V	
V_{OH}	Output Logic 1 Voltage @ I_{OUT} = -220 μA	2.4	V_{CC}	V	

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%; 0°C ≤ T_A ≤ +70°C) [6]

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{ACC}	Address to output delay time		350	ns	4
t_{CS}	Chip select to output delay time		175	ns	4
t_{CD}	Chip deselect to output delay time		150	ns	4

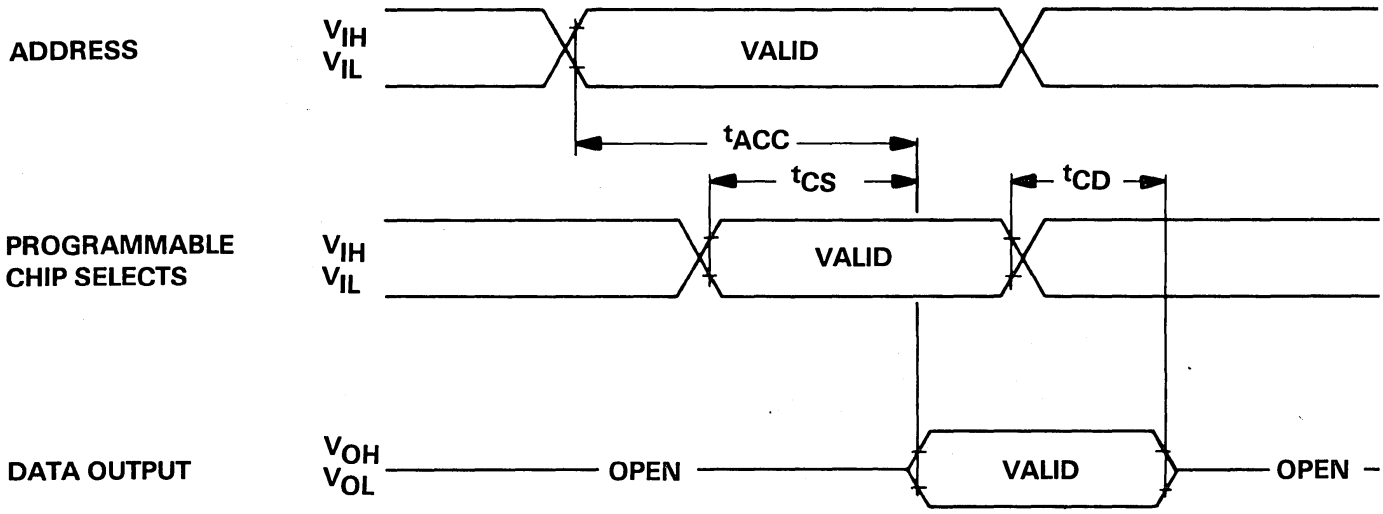
CAPACITANCE

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_{IN}	Input Capacitance	6	8	pF	5
C_{OUT}	Output Capacitance	10	15	pF	5

NOTES:

1. All inputs 5.5V; Data Outputs open.
2. V_{IN} = 0V to 5.5V (V_{CC} = 5V)
3. Device unselected; V_{OUT} = 0V to 5.5V.
4. Measured with 2 TTL loads and 100pF, transition times = 20ns.
5. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation:
   $C = \frac{I\Delta t}{\Delta V}$ with current equal to a constant 20mA.
6. A minimum 2ms time delay is required after the application of V_{CC} (+5) before proper device operation is achieved.

TIMING DIAGRAM



*The chip select inputs can be user programmed so that either the input is enabled by a Logic 0 voltage (V_{IL}), a Logic 1 voltage (V_{IH}), or the input is always enabled (regardless of the state of the input). See chart below for programming instructions.

ROMS

MOSTEK 34000 ROM PUNCHED CARD CODING FORMAT (1)

FIRST CARD

COLS	INFORMATION FIELD
1-30	Customer
31-50	Customer Part Number
60-72	Mostek Part Number (2)

SECOND CARD

1-30	Engineer at Customer Site
31-50	Direct Phone Number for Engineer

THIRD CARD

1-5	Mostek Part Number (2)
33	Chip Select One "1" = CS_1 or "0" = $\overline{CS_1}$ or "2" = Don't Care
35	Chip Select Two "1" = CS_2 or "0" = $\overline{CS_2}$ or "2" = Don't Care
37	Chip Select Three "1" = CS_3 or "0" = $\overline{CS_3}$ or "2" = Don't Care

FOURTH CARD

1-9	Data Format (3)
15-28	Logic - ("Positive Logic" or "Negative Logic")
35-57	Verification Code (4)

DATA FORMAT

128 data cards (16 data words/card) with the following format:

COLS	INFORMATION FIELD
1-4	Four digit octal address of first output word on card
5-7	Three digit octal output word specified by address in column 1-4
8-52	Next fifteen output words, each word consists of three octal digits.

NOTES:

1. Positive or negative logic formats are accepted as noted in the fourth card.
2. Assigned by Mostek; may be left blank.
3. Mostek punched card coding format should be used. Punch "Mostek" starting in column one.
4. Punches as: (a) VERIFICATION HOLD - i.e. customer verification of the data as reproduced by Mostek is required prior to production of the ROM. To accomplish this Mostek supplies a copy of its Customer Verification Data Sheet (CVDS) to the customer.
   (b) VERIFICATION PROCESS - i.e. the customer will receive a CVDS but production will begin prior to receipt of customer verification; (c) VERIFICATION NOT NEEDED -i.e. the customer will not receive a CVDS and production will begin immediately.