Module 1 Logic Gates : AND, OR, NOT, NAND, NOR, Exclusive -OR, and Exclusive - NOR. Implementation of logic functions using gates. NAND - NOR implementations.

Logic Gates :-

1. It is a circuit that has one, two or more input signals and only one output signal.

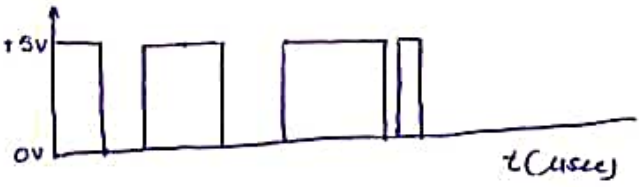
The input is a voltage level. The voltage level could be +5V and 0V
-5V and 0V
+6V and 0V
-6V and 0V and so on.

These levels may be related to binary condition of 1 and 0.

1 represents ON / high (H) / true. (T)
0 represents OFF / low (L) / false (F)

Ideal Digital Signal

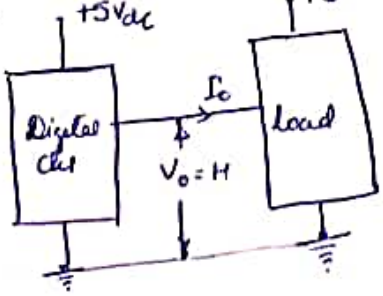
- The signal have either value of 5V level or 0V.



- The level changes or switching takes place in zero time. The modern digital signals approach this level/ behaviour but do not attain it

DIGITAL WAVEFORM

voltage levels. V_o is high



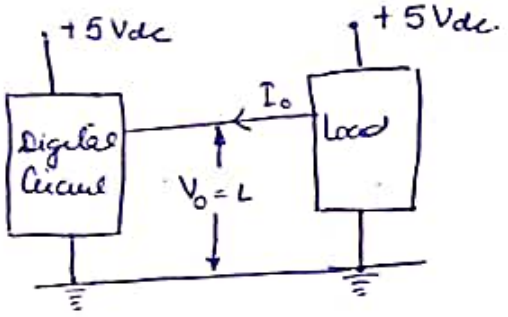
When V_o is high. V_o should be 5V
- ckt acts as a current source and I_o → current is delivered to load
also the output voltage should be close to 5 volts

voltage of any level between 5V and $V_{OH,min}$ is defined as H = 1 = T

$V_{OH,min}$ means min value of o/p voltage when high

example: Transistor - Transistor Logic (TTL) family of ckts which have. $V_{OH,min} = +3.5\ V_{dc}$. Thus H = 1 when V_o lies between +5V dc to +3.5 V dc.

V_o is low



When V_o is low then its value should be 0V.

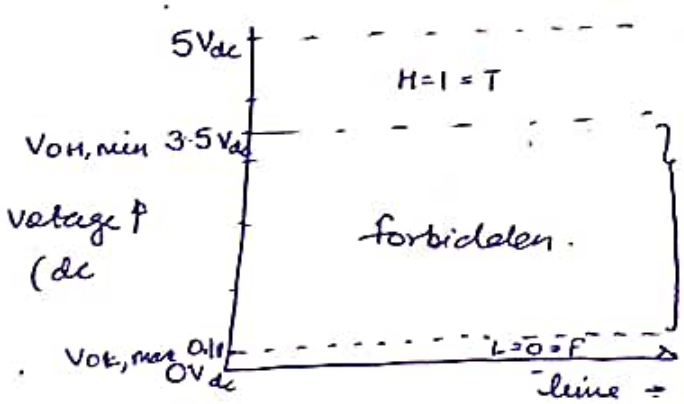
- The circuit acts as a current sink
- It takes current I_o from the load and delivers it to the ground.

The output voltage is close to 0V. and $V_{OL,max}$ is defined as L = 0 = F

$V_{OL,max}$ means maximum value of output voltage when low.

example: T-T Logic allows a $V_{OL,max} = 0 + 0.1\ V_{dc}$.

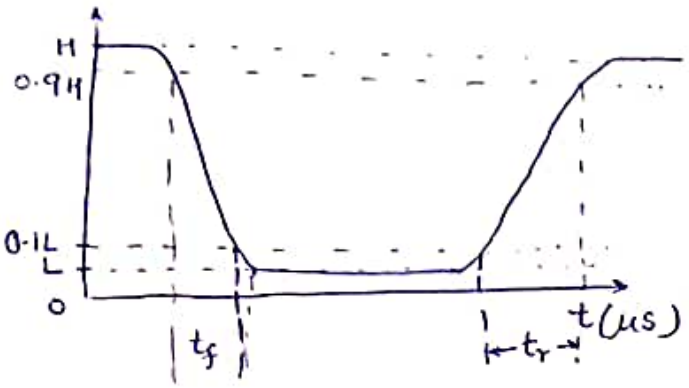
Thus L = 0 when voltage lies between +0.1 V dc to 0 V dc.



for TTL logic

← no voltage levels are permitted in the circuit.

Switching time : The ideal circuit has zero time to change its level. Thus there is never a value of output voltage which has a value that lies between in the forbidden zone / region



when switching is not taking place V_0 remain within the high or the low band.

"t_f" is fall time. it is the time required for transition from high level to low level

"t_r" is rise time. It is the time required for transion from low level to high level.

In the above figure t_f is time needed / take to change from. 0.9H to 1.1L. and tr is the time needed / taken to change from 1.1L to 0.9H.

Period and Frequency : Period(T) is the time after which the signal repeats its self.

frequency is the reciprocal of time period

$$f = \frac{1}{T}$$

Duty Cycle : the duty cycle is a measure of how symmetrical or unsymmetrical a waveform is. It may be presented in % form. If the duty cycle is symmetrical, then

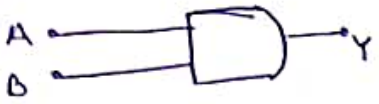
Duty cycle high (H) = Duty Cycle Low (L) = $\frac{T/2}{T} = 0.5$ or 50%

AND Gate

(a) This gate has two or more input and one output

(b) It has high output when both or all the inputs are high

(c) Symbol is



Y = A AND B

Y = A.B

"." is the symbol of logic operation of AND and not the multiplication of decimal numbers

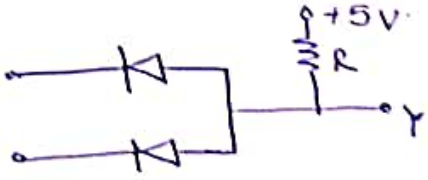
Y = 0.0 = 0
= 0.1 = 0
= 1.0 = 0
= 1.1 = 1

(d) The truth table

Input A	Input B	Output Y
0	0	0
0	1	0
1	0	0
1	1	1

(e) The electric circuit

(f) The diode circuit



- When both the inputs are low, both the diodes will conduct. This will result in high current flowing in the resistance R and the voltage at the output point x will be low due to 5V being dropped to low value due to R.
- When ~~both~~ one of the input is low and the other input is high, the diode with

low input conducts and this pulls the output voltage to a low value.

. When both the inputs are high both the diodes will be in cut-off position so no current flows through R, the supply voltage +5V ~~is~~ is available at the output.

(g) The AND operation is logical multiplication or intersection $\cap$ or $\wedge$

$Y = A \text{ AND } B.$

$= A \cdot B = AB.$

(h) The ~~and~~ AND operation is both commutative and associative

$AB = BA$

$(AB)C = A(BC)$

(i) Application : It is used to block or transmit data in digital systems.

OR Gate

(a) This gate has two or more input and one output.

(b) It is called an OR gate because the output is high if any or all the input voltages are high

(c) Symbol is

Y = A or B

Y = A + B

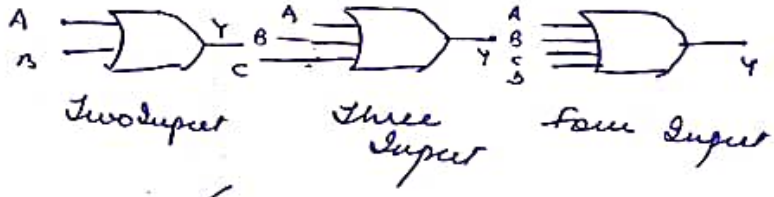
(d) Truth table.

Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

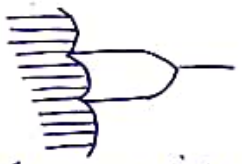
Binary addition

0+0 = 0
0+1 = 1
1+0 = 1
1+1 = 10

(e) Symbol for multiple inputs

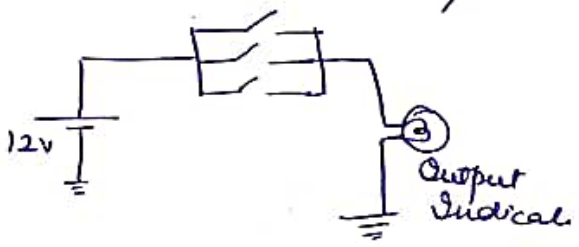


Two input Three input four input

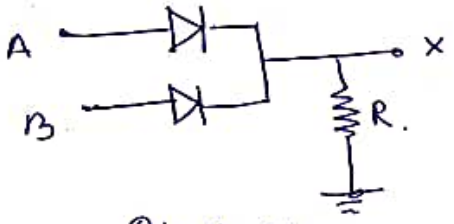


Twelve input

(f)



Electric ckt



Diode ckt

(g) The OR operation is both commutative and associative.

Thus $A + B = B + A$

$(A+B) + C = A + (B+C)$

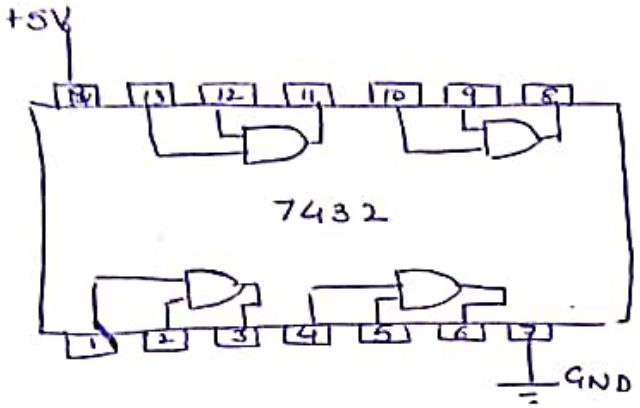
(h) Truth table for 3 input and 4 input can be made easily using binary addition

(i) TTL OR gate, 7432, is a TTL quad-2-input OR gate. It is an IC having 14 pins that contain four OR gates.

Pin diagram of 7432 OR gate

Pin 14 - Supply voltage +5 Volt

Pin 7 - Ground.



NOT gate / Inverter / 7404

(a) 

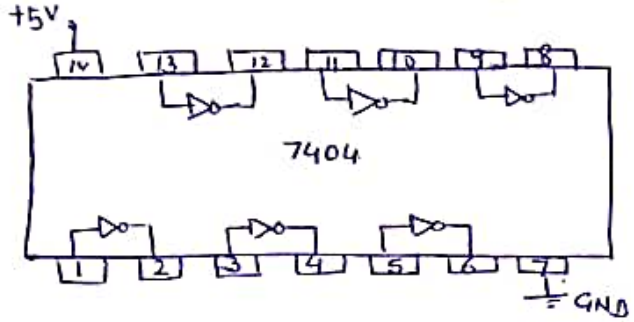
Symbol.

(e) Truth table

A	Y
0	1
1	0

(b) It has a two state operation

(c) 7404 is an hex Inverter. It is an IC which contains six inverters.



Pindiagram of IC 7404

Pin 14 — supply voltage +5V dc.

Pin 7 — ground.

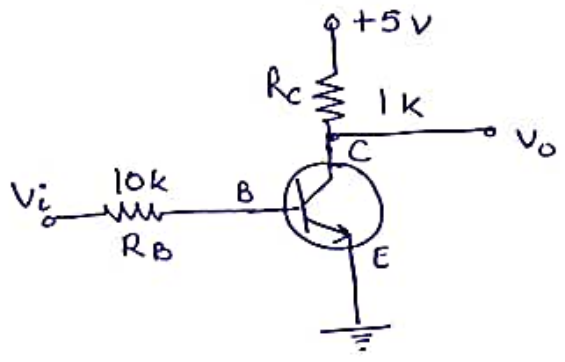
The six inverters can be connected to TTL Devices.

(d) The output of NOT gate is the complement of input

Y = not A

Y = A' or $\bar{A}$

(f) A transistor can be employed as an inverter

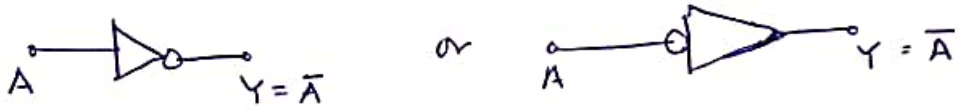


When
V_i = Low (0V)
the transistor cuts out and then
V_o = High (≈ 5V)

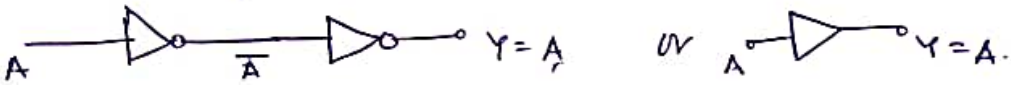
When
V_i = High (5V)
the transistor saturates and forces V_o to be low.
V_o = 0V

(g) Inverter has an output which is the complement of the input.

(h) The bubble of the inverter may be placed on the output or the input



(i) Connecting two inverters in cascade



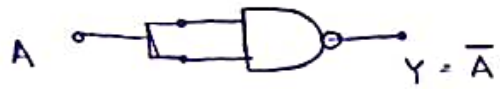
This application is called as buffering or isolating two circuits.

NAND - NOR Implementation or / UNIVERSAL GATES

NAND and NOR as Universal Gates

(A) NAND as a universal gate

1. NAND as NOT gate

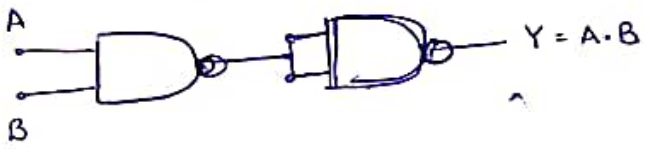


Truth table of NOT Gate

I/p A	B	O/p Y
0		1
1		0

symbol

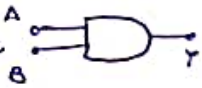
2. NAND as AND GATE



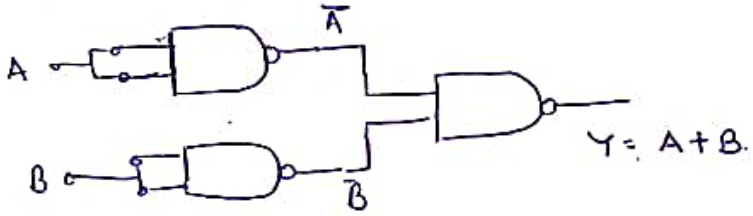
Truth table of ~~and~~ AND gate

Input A	B	Output Y
0	0	0
0	1	0
1	0	0
1	1	1

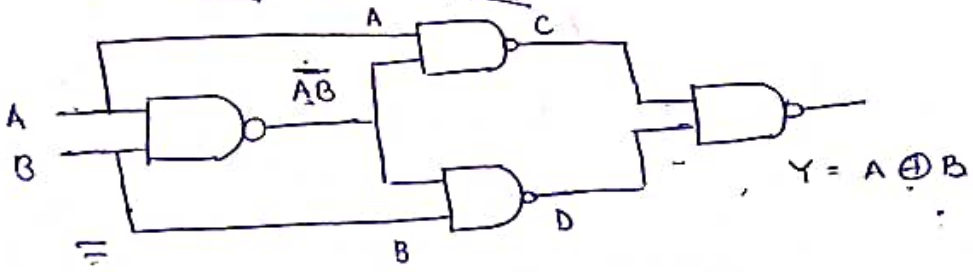
symbol



3. NAND gate forms OR gate



4. NAND as ~~XOR~~ XOR Gate



Truth table for XOR gate

Input A	B	O/p Y
0	0	0
0	1	1
1	0	1
1	1	0

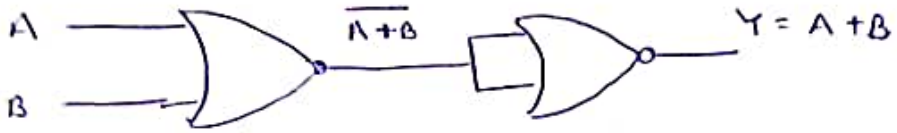
(B) NOR as a Universal Gate

(1) NOR gate as a NOT gate

$\overline{A+A} = \bar{A}\cdot\bar{A} = \bar{A}$

$Y = \bar{A}$

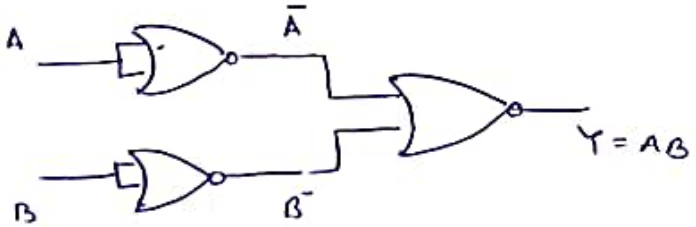
(2) NOR as OR gate



A NOR B = $\overline{A+B}$

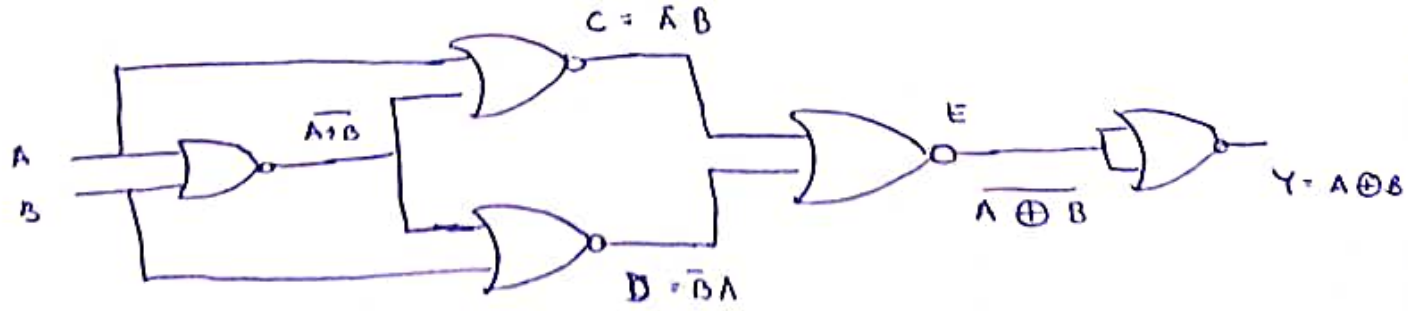
and $\overline{\overline{A+B}} = A+B \Rightarrow Y = A+B$

(3) NOR as ~~AND~~ Gate



as $\bar{A}$ NOR $\bar{B} = \overline{\bar{A}+\bar{B}} = \bar{\bar{A}}\cdot\bar{\bar{B}} = A\cdot B$ (De Morgan's 1st Th.)

4. NOR as XOR Gate



$$C = \overline{[A + (\overline{A+B})]}$$

$$= \bar{A} \cdot (A+B) = \bar{A} \cdot A + \bar{A} \cdot B \cdot \bar{A}B \qquad (\because \bar{A} \cdot A = 0)$$

$$D = \overline{[B + \overline{A+B}]}$$

$$= \bar{B} \cdot (A+B) = \bar{B} \cdot A + \bar{B} \cdot B = \bar{B} \cdot A \qquad (\because \bar{B}B = 0)$$

$$E = \overline{[\bar{A} \cdot B + \bar{B} \cdot A]} = \overline{A+B}$$

and $Y = \overline{\overline{A \oplus B}} = \overline{A+B}$

$\therefore Y = A + B$

Learning Technique

	WAND	NOR
NOT	1	1
AND	2	3
OR	3	2
EOR	4	5
X-NOR	5	4

4.