EG3113 chip user manual

High power MOS tube, IGBT tube gate driver chip

Version change history

Version number	date	description
V1.0	October 22, 2016	First draft of EG3113 data sheet
V1.1	Added DFN8 package on July 20, 2017	
V1.2	Output current capability modified on August 19, 2017	

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EG3113 chip data manual V1.0

1.Characteristics _

7 _ _ Dead zone control circuit ÿ Comes with a latch function to completely
prevent the upper and lower tube outputs from
being turned on at the same time ÿ HIN
input channel is active at high level, controlling the
high-end HO output ÿ LIN input channel is active at low
level, controlling the low-end LO
output ÿ Peripheral devices Less ÿ Quiescent current is less than 5uA, very suitable for
battery applications ÿ Package form: SOP8, DFN8

2.Description _

EG3113 is a cost-effective high-power MOS tube and IGBT tube gate drive chip, which integrates a logic signal input processing circuit.
circuit, dead zone control circuit, latch circuit, level shift circuit, pulse filter circuit and output drive circuit, dedicated to brushless motor controllers
in the drive circuit.

The high-end operating voltage of EG3113 can reach 600V, the low-end Vcc power supply voltage range is wide from 2.8V to 20V, and the static power consumption is less than 5uA. The core
The chip has a latch function to prevent the output power tubes from turning on at the same time. The input channel HIN has a built-in 200K pull-down resistor, and LIN has a built-in pull-up 5V.
High potential, when the input is floating, the upper and lower power MOS tubes are in a closed state, the output current capacity is IO+/- 2/2.5A, and it is packaged in SOP8.

3.Application fields

ÿ Mobile power supply, high voltage fast charging switching
power supply ÿ Variable frequency water
pump controller ÿ 600V step-down switching power supply
ÿ Electric vehicle controller ÿ
Brushless motor driver ÿ High
voltage Class-D amplifier

4. Pin

4.1 Pin definition

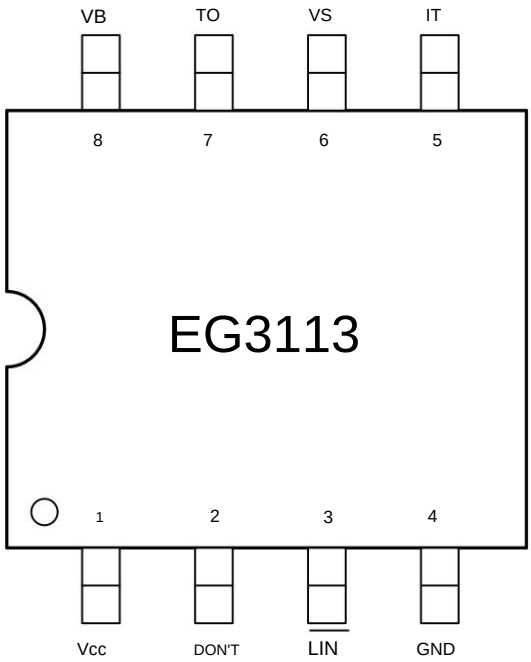


Figure 4-1. EG3113 pin definition

4.2 Pin description

Pin number	Pin name	I/O	describe
1	Vcc	Power	Chip working power input terminal, voltage range 2.8V-20V, connected to an external high-frequency 0.1uF Circuit capacitance can reduce high-frequency noise at the input end of the chip
2	DON'T	I	The logic input control signal is active at high level and controls the conduction and interception of the high-end power MOS tube. end "0" is to turn off the power MOS tube "1" is to turn on the power MOS tube
3	$\overline{\text{LIN}}$	I	The logic input control signal is active at low level and controls the conduction and interception of the low-end power MOS tube. end "1" is to turn off the power MOS tube "0" is to turn on the power MOS tube
4	GND	GND	The ground terminal of the chip.
5	IT	O	output controls the on and off of the low-end MOS power tube
6	VS	O	High-end suspended ground terminal
7	TO	O	output controls the on and off of the high-end MOS power tube
8	VB	Power	high-end floating power supply

5. Structure diagram

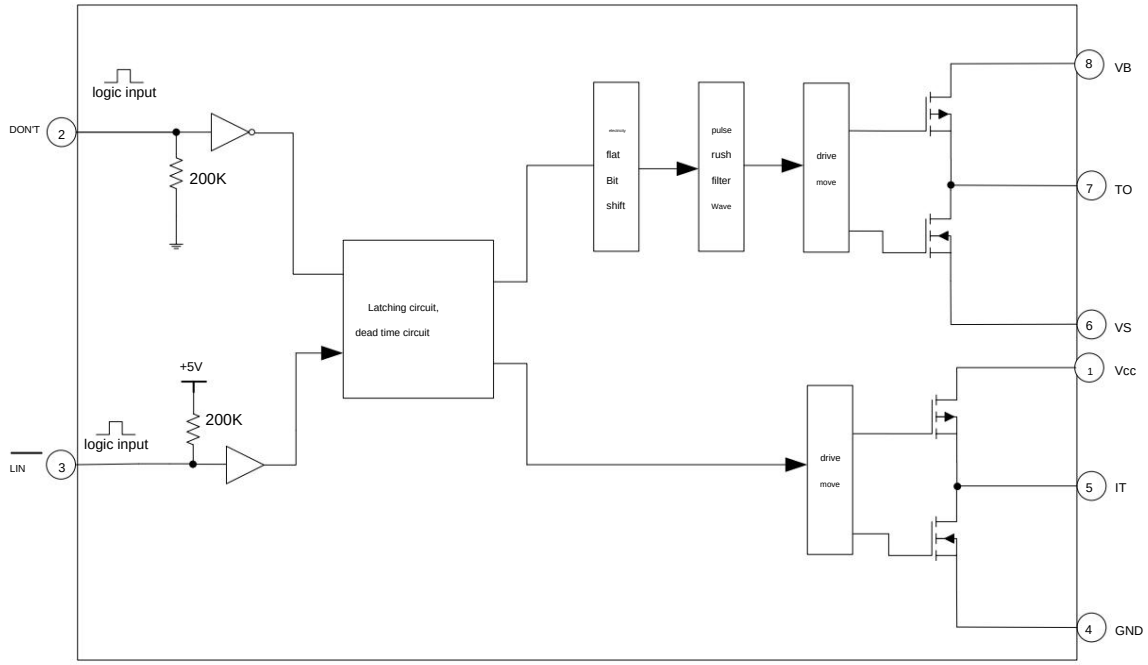


Figure 5-1. EG3113 internal circuit diagram

6.Typical application circuit

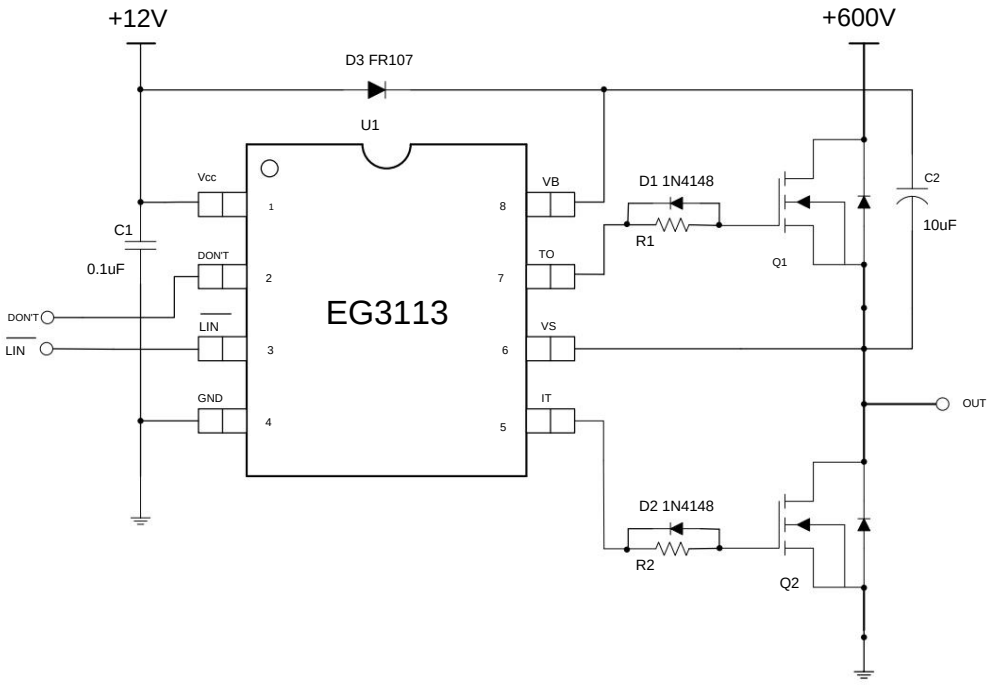


Figure 6-1. EG3113 typical application circuit diagram

7. Electrical characteristics

7.1 Limit parameters

No other instructions, under the condition of TA=25ÿ

Symbol Parameter Name Bootstrap High Side VB Power		Test conditions minimum and maximum units			
Supply	VB		-0.3	600	IN
High-end suspended ground terminal	VS		VB-20 VB+0.3		IN
high end output	TO		VS-0.3 VB+0.3		IN
low end output	IT		-0.3 VCC+0.3		IN
Power	VCC		-0.3	20	IN
high channel logic signals Input level low	DON'T		-0.3 VCC+0.3		IN
channel logic signal Input level	$\overline{\text{LIN}}$		-0.3	6	IN
FACING	ambient temperature		-45	125	ÿ
Tstr	Storage temperature		-55	150	ÿ
TL	Welding temperature	T=10S		300	ÿ

Note: Exceeding the listed extreme parameters may cause permanent damage to the chip internally, and running under extreme conditions for a long time will affect the reliability of the chip.

7.2 Typical parameters

No other instructions, under the conditions of TA=25ÿ, Vcc=12V, load capacitance CL=10nF

Parameter Name Symbol Power		Test Conditions Minimum Typical Maximum Units				
	Vcc		2.8	12	20	IN
Quiescent	Icc input is floating, Vcc=12V -				30	uA
current input logic signal high Potential	Vin(H) All input control signals 2.5					IN
input logic signal low Potential	Vin(L) all input control signals-0.3			0	1.0	IN
input logic signal high The level of the	Iin(H)	Vin=5V			20	uA
current input logic signal is low level of current	Iin(L)	Vin=0V	-20			uA
Low-side output LO switching time characteristics						
On delay	Ton	See Figure 7-1		280	400	nS
off delay	Toff	See Figure 7-1		125	300	nS
Rise Time	Tr	See Figure 7-1		120	200	nS
Fall time	Tf	See Figure 7-1		80	100	nS
High-end output HO switching time characteristics						
On delay	Ton	See Figure 7-2		250	400	nS
off delay	Toff	See Figure 7-2		180	400	nS
Rise Time	Tr	See Figure 7-2		120	200	nS
Fall time	Tf	See Figure 7-2		80	100	nS
Dead time characteristics						
dead time	DT	See Figure 7-3, No load capacitance CL=0	50	100	300	nS
IO output maximum drive capability						
IO output source current IO+		Vo=0V, VIN=VIH PWÿ10uS	1.8	2		A
IO output sink current IO-		Vo=12V, VIN=VIL PWÿ10uS	2	2.5		A

7.3 Switching time characteristics and dead time waveform diagram

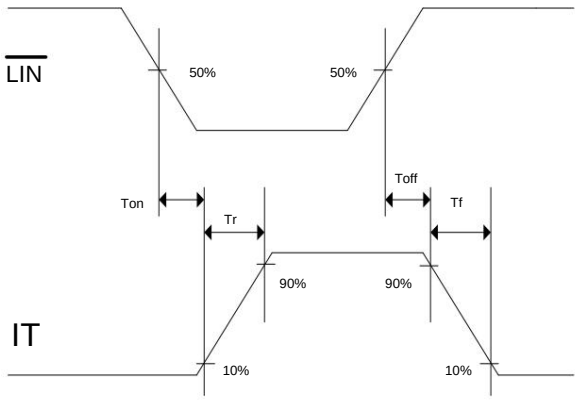
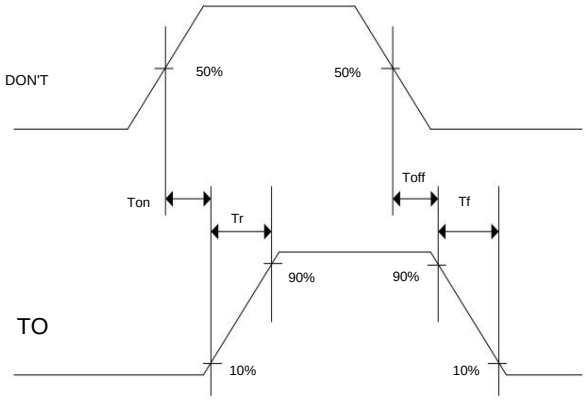


Figure 7-1. Low-side output LO switching time waveform diagram



7-2. High-end output HO switching time waveform diagram

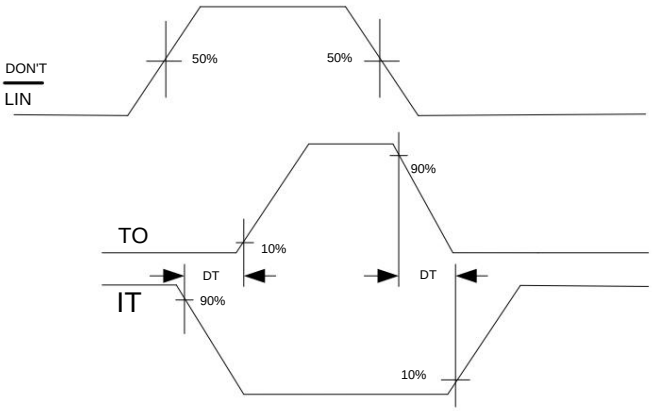


Figure 7-3. Dead time waveform diagram

8. Application design

8.1 Vcc terminal power supply voltage

For different MOS tubes, choose different driving voltages. The recommended power supply Vcc working voltage for high-voltage turning on MOS tubes is typically 10V-15V;

The recommended power supply VCC working voltage for low-voltage turn-on MOS tubes is 2.8V-10V.

8.2 Input logic signal requirements and output driver characteristics

The main functions of EG3113 include logic signal input processing, dead time control, level conversion function, suspended bootstrap power supply structure and upper and lower bridges

Totem pole output. The high-level threshold of the logic signal input terminal is above 2.5V, and the low-level threshold is below 1.0V. The output of the logic signal is required.

The current is small, and the MCU output logic signal can be directly connected to the input channel of EG3113.

The high-side high-side and low-side low-side output drivers can sink up to 2.5A and output current up to 2A, high-side high-side channel

It can withstand a voltage of 600V, and the conduction delay between the input logic signal and the output control signal is small. The low-end output turn-on conduction delay is 280nS.

The turn-off conduction delay is 125nS, the high-end output turn-on conduction delay is 250nS, and the turn-off conduction delay is 180nS. Rise time of low-side output turn-on

is 110nS, the turn-off fall time is 50nS, the high-side output turn-on rise time is 110nS, and the turn-off fall time is 50nS.

The input signal and output signal logic function diagram is shown in Figure 8-2:

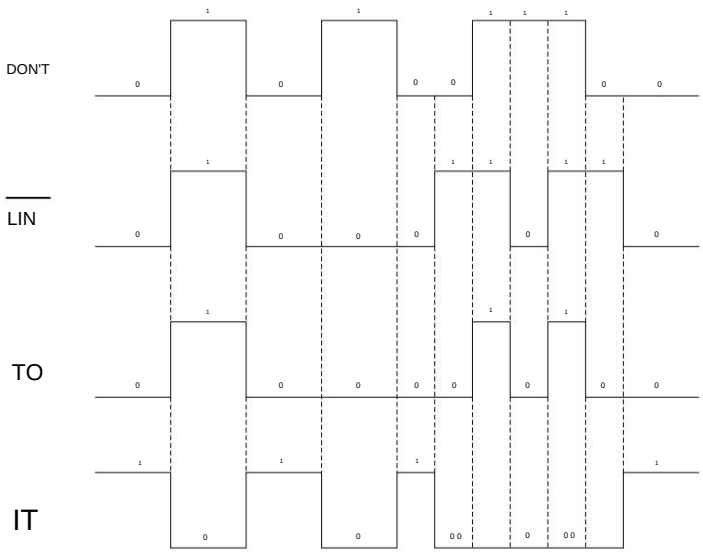


Figure 8-2. Input signal and output signal logic function diagram

Logic truth table for input and output signals:

enter		output	
Input and output logic			
HIN (pull leg 4)	LINÿÿÿÿÿ (Pin 3) HO (Pin 7		LO (pull leg 5)
0	**0**	0	**1**
0	1	0	0
1	0	0	0
1	**1**	**1**	0

It can be seen from the truth table that when the input logic signals HIN and LINÿÿÿÿÿ are "0" at the same time and "1" at different times, the driver controls the output

HO and LO are "0" at the same time. The upper and lower power tubes are turned off at the same time; when the input logic signals HIN and LINÿÿÿÿÿ are "0" at the same time, the driver controls the output HO.

When LO is "0", the upper side is turned off, and when LO is "1", the lower side is turned on; when the input logic signals HIN and LINÿÿÿÿÿ are both "1", the driver control output HO is

"1" means the upper tube is turned on, and "LO" means "0" means the lower tube is turned off; the internal logic processor prevents the controller output from the upper and lower power tubes being turned on at the same time.

Locking function.

8.3 Bootstrap circuit

EG3113 adopts a bootstrap suspension drive power supply structure, which greatly simplifies the drive power supply design. It only uses one power supply voltage VCC to complete the high-end

The driving of two power switching devices, N-channel MOS transistors and low-end N-channel MOS transistors, brings great convenience to practical applications. EG3113 Yes

Use an external bootstrap diode as shown in Figure 8-3 and a bootstrap capacitor to automatically complete the bootstrap boost function. It is assumed that during the period when the lower tube is turned on and the upper tube is turned off.

The C bootstrap capacitor has been charged to a sufficient voltage (Vc=VCC). When HO outputs a high level, the upper tube is turned on and the lower tube is turned off. The voltage on the VC bootstrap capacitor

The voltage will be equivalent to a voltage source as the power supply of the internal driver VB and VS to complete the driving of the high-end N-channel MOS transistor.

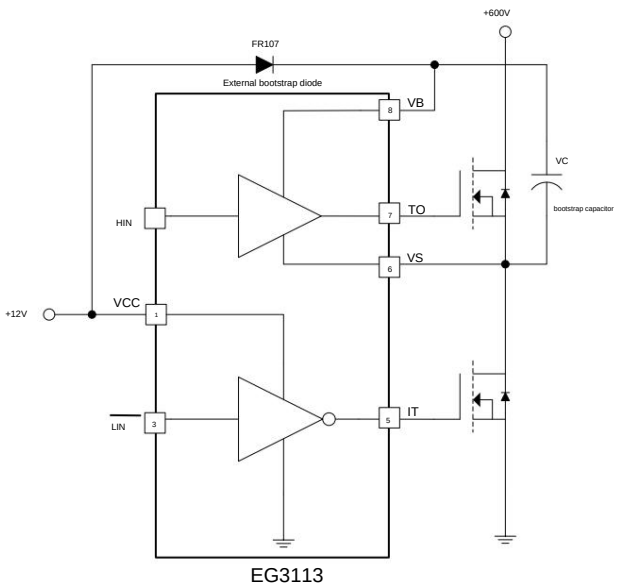
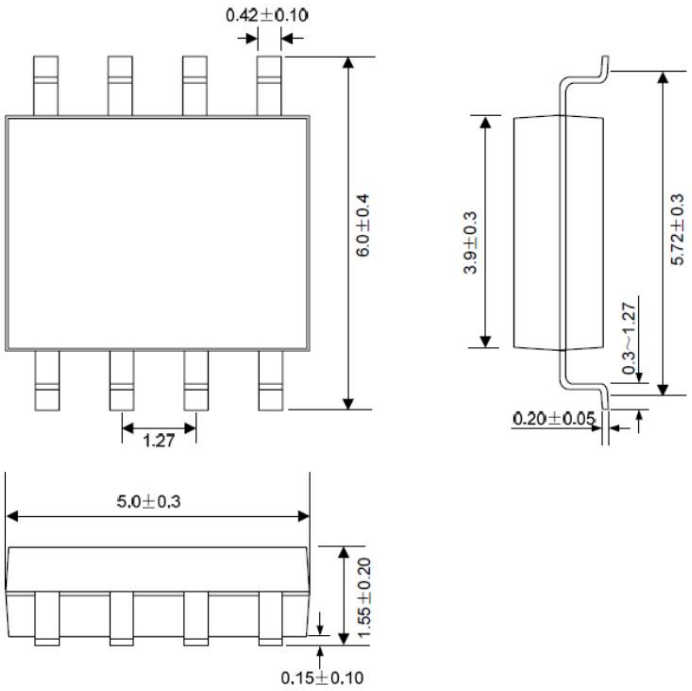


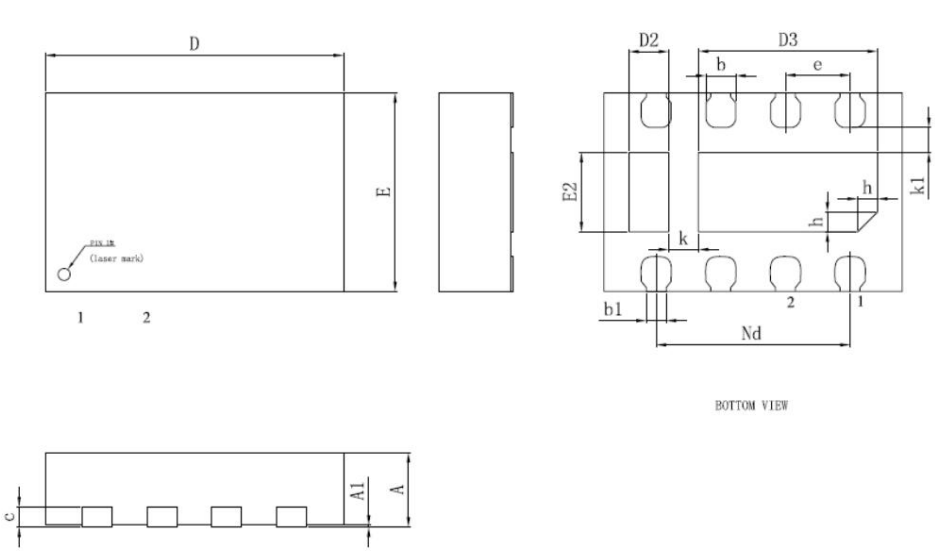
Figure 8-3. EG3113 bootstrap circuit structure

9.Package size

9.1 SOP8 package size



9.2 DFN8 package size



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.25	0.30	0.35
b1	0.15	0.20	0.25
c	0.15	0.20	0.25
D	2.90	3.00	3.10
D2	0.30	0.40	0.50
D3	1.70	1.80	1.90
e	0.65BSC		
Nd	1.95BSC		
E	1.90	2.00	2.10
E2	0.70	0.80	0.90
L	0.30	0.35	0.40
h	0.15	0.20	0.25
k	0.25	0.30	0.35
k1	0.20	—	—