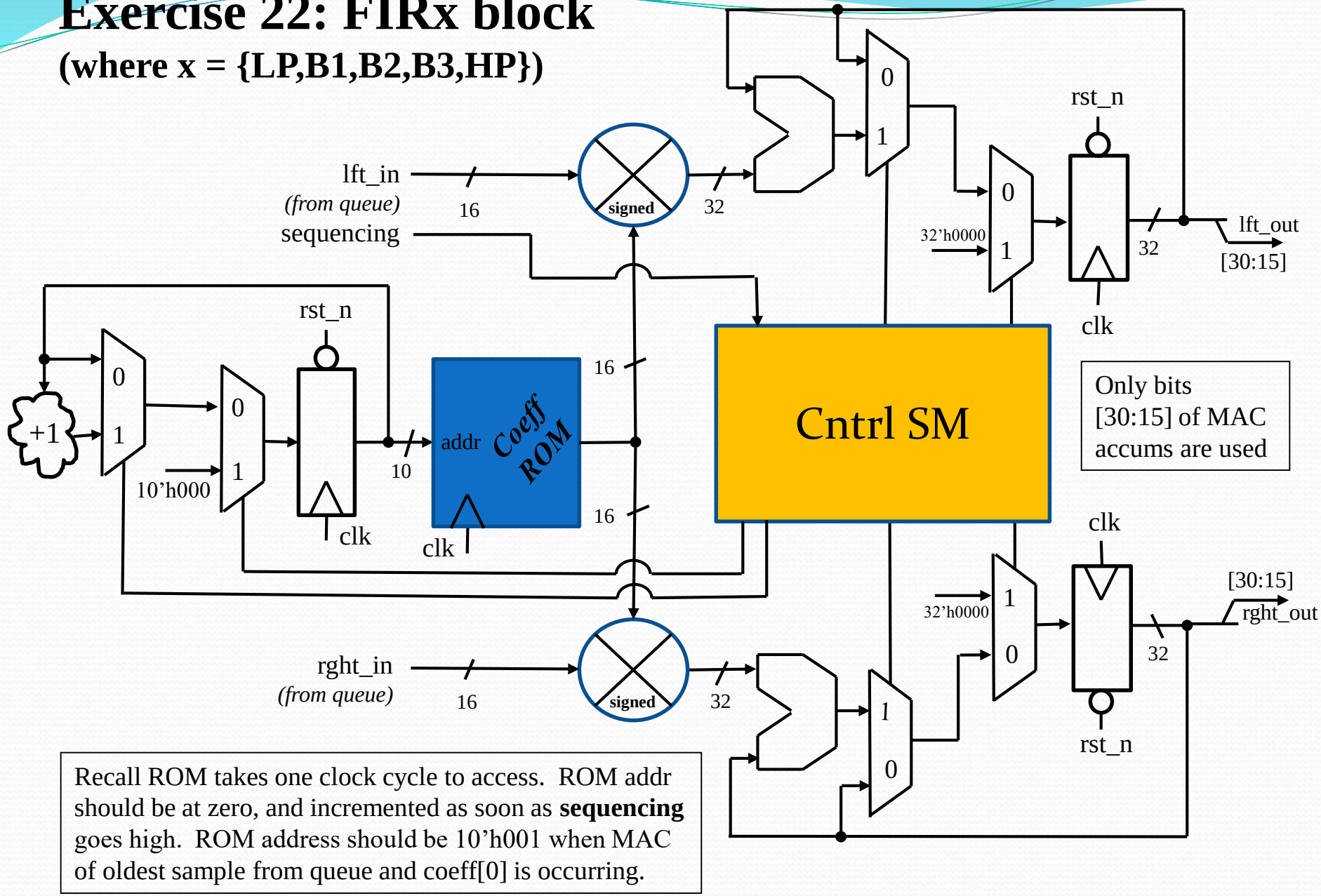
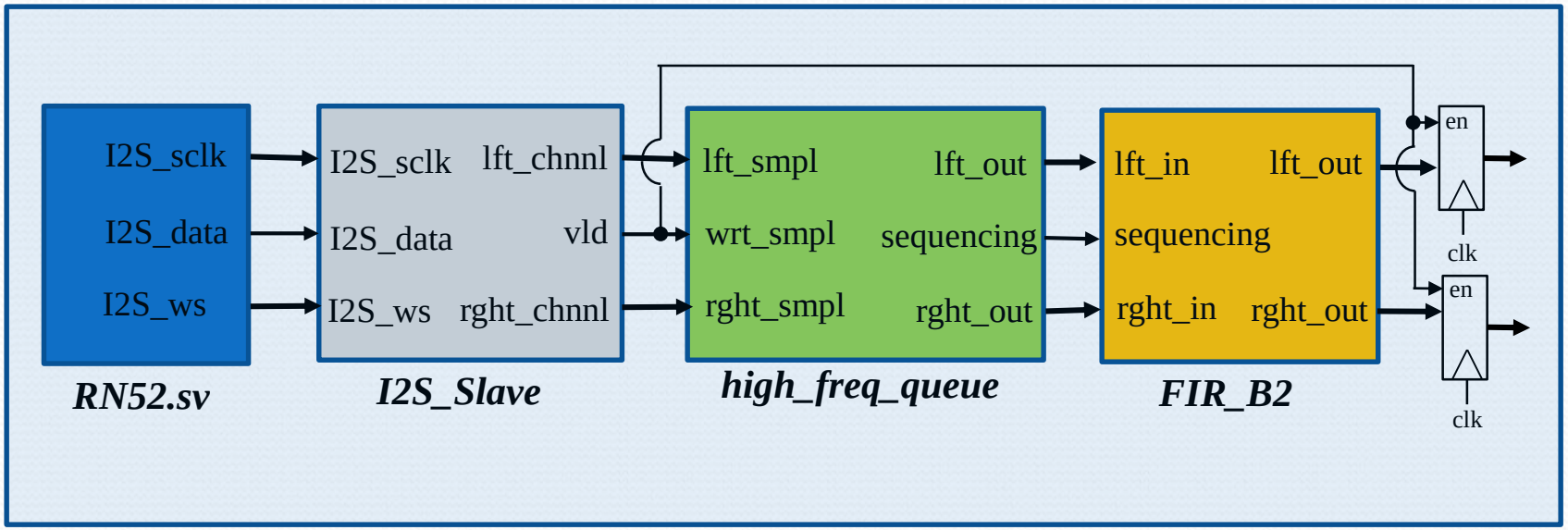
Exercise 22: FIRx block

(where x = {LP,B1,B2,B3,HP})



Recall ROM takes one clock cycle to access. ROM addr should be at zero, and incremented as soon as **sequencing** goes high. ROM address should be 10'h001 when MAC of oldest sample from queue and coeff[0] is occurring.

Exercise 22: FIRx block Testing



This might be a good way of testing your equalizer path

(**RN52.sv**, **ROM_B2.v**, and the **tone_hex_*.txt** files should be coming from the **ProjectProvidedFiles.zip** under the project area of the Canvas page)