Exercise 1 (Ability to run ModelSim From Home):

- To perform homeworks and work on the project you may find it handy to have ModelSim installed on your own machine.
- Windows users can run the Student Edition of ModelSim
- MAC Users will have to be able to remote shell to CAE machines
  - Icarus verilog is not an option
  - We are using system verilog, Icarus does not support SV
- It is strongly encouraged for you to have ModelSim capability from home. The next slide discusses installing the student edition on a windows machine.

Installing ModelSim Student Edition:

- Download from:

http://www.mentor.com/company/higher_ed/modelsim-student-edition

- Once the setup executable is downloaded run as administrator (right click “run as administrator”).

- At the end of the installation process it will kick off your browser to a URL for you to register for the free license. It is important that this part work. Seems to work best with Chrome.

- You will then get an license file mailed to you. Download this file and place it in the executable directory that modelsim is installed in. C:\Modeltech_pe_edu_10.4c.

- This license file is nodelocked to the serial number of your hard drive, so it will not work for your friend. Everyone needs to complete this process individually.

Creating a ModelSim Project, Compiling, & Simulating:

- On the class webpage under the Exercise1 folder download the files ***counter.sv*** and ***counter_tb.v*** to your I: drive.

- Look over the code for ***counter.sv***. This is your DUT (Device Under Test). It is a simple 8-bit counter that can be enabled, and can count either up or down. It uses some system verilog constructs and thus ends with the .sv extension.

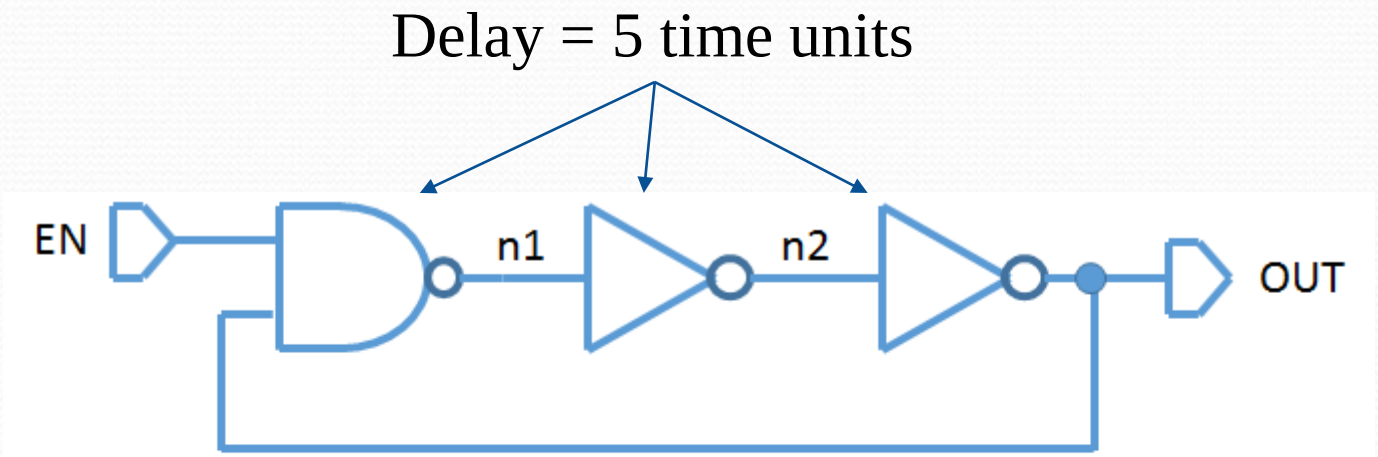
- ***counter_tb.v*** is the test bench for this DUT. It instantiate the DUT, and applies some stimulus to its inputs. Look over the code.

Creating a ModelSim Project, Compiling, & Simulating:

- Launch ModelSim and create a new project in your I: drive area.
- Add the two downloaded files for this exercise to the project.
- Compile the code. Note there is a syntax error in counter.sv. Discover what it is and fix it and compile again.
- Start simulation on ***counter_tb.v***.
- Add waves to the waveform viewer, and run the simulation.
- Perform a screen capture of the waveforms and submit the image to the dropbox for Exercise1

(Stretch Goal on next page)

Ring Oscillator



- What does this circuit do when you raise EN?
- Implement it in structural Verilog
- Create a test bench to instantiate and test it.
  - EN should be low for 15 time units then raised