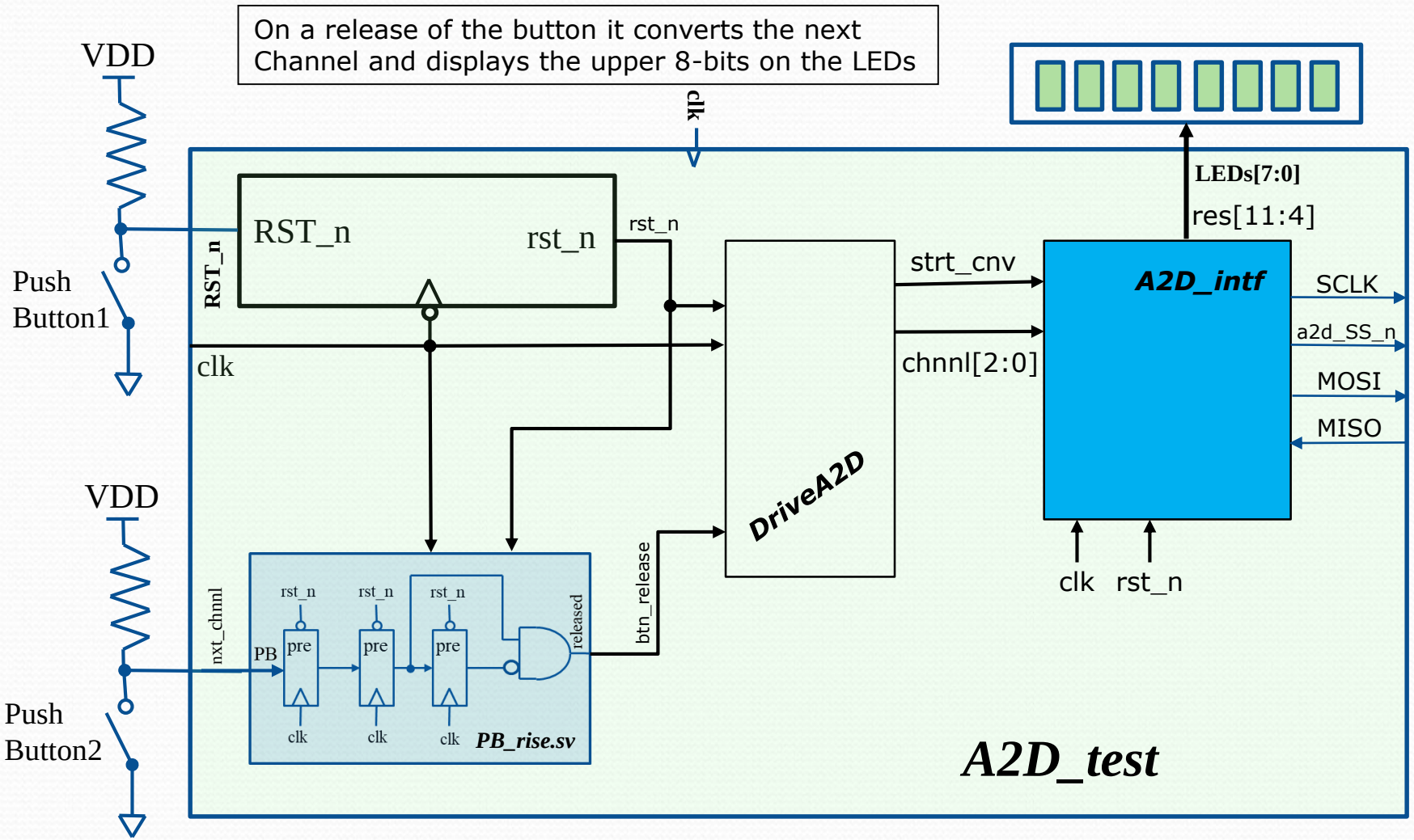
Exercise 12: Mapping A2D_intf to DE0-Nano

- A Quartus settings file (**A2D_test.qsf**) can be downloaded from the webpage.
- A Verilog template file (**A2D_test.sv**) can be downloaded from the webpage.
  - It will instantiate your reset synchronizer from Exercise09.
  - It will instantiate your PB_rise from Exercise09.
  - It also instantiates your A2D_intf from Exercise11.
- Code a simple sequencer block (*DriveA2D* in block diagram) into A2D_test that increments the channel, and asserts ***strt_cnv*** for one clock cycle every time it detects a rise edge on the push button. (you can code flat at A2D_test level of hierarchy if you like…you do not need a block called DriveA2D)
- The most significant 8-bits from the A2D result will drive ***LEDs***.

Exercise 12: Testing Your A2D_intf on DE0-nano

Demo your A2D_intf on DE0_nano to Hoffman/Fego



Exercise 12: Testing Your A2D_intf on DE0-nano

- A Quartus settings file (A2D_test.qsf) that maps the signal names of **A2D_test.sv** to pins of the Altera FPGA exists on the webpage. Download it.
- A Quartus project file (**A2D_test.qpf**) also exists. Download that as well.
- When you have it all mapped and working call either Eric or Fego over and demo its proper operation.

What is working? The lower 3-bits of the LED should reflect The channel you are converting. The upper 4-bit will look somewhat random and should vary as you run your finger along the A2D pins (bottom right corner pins). When you call us over we will put on a board that actually drives the A2D pins to known analog values, so the results will make more sense.