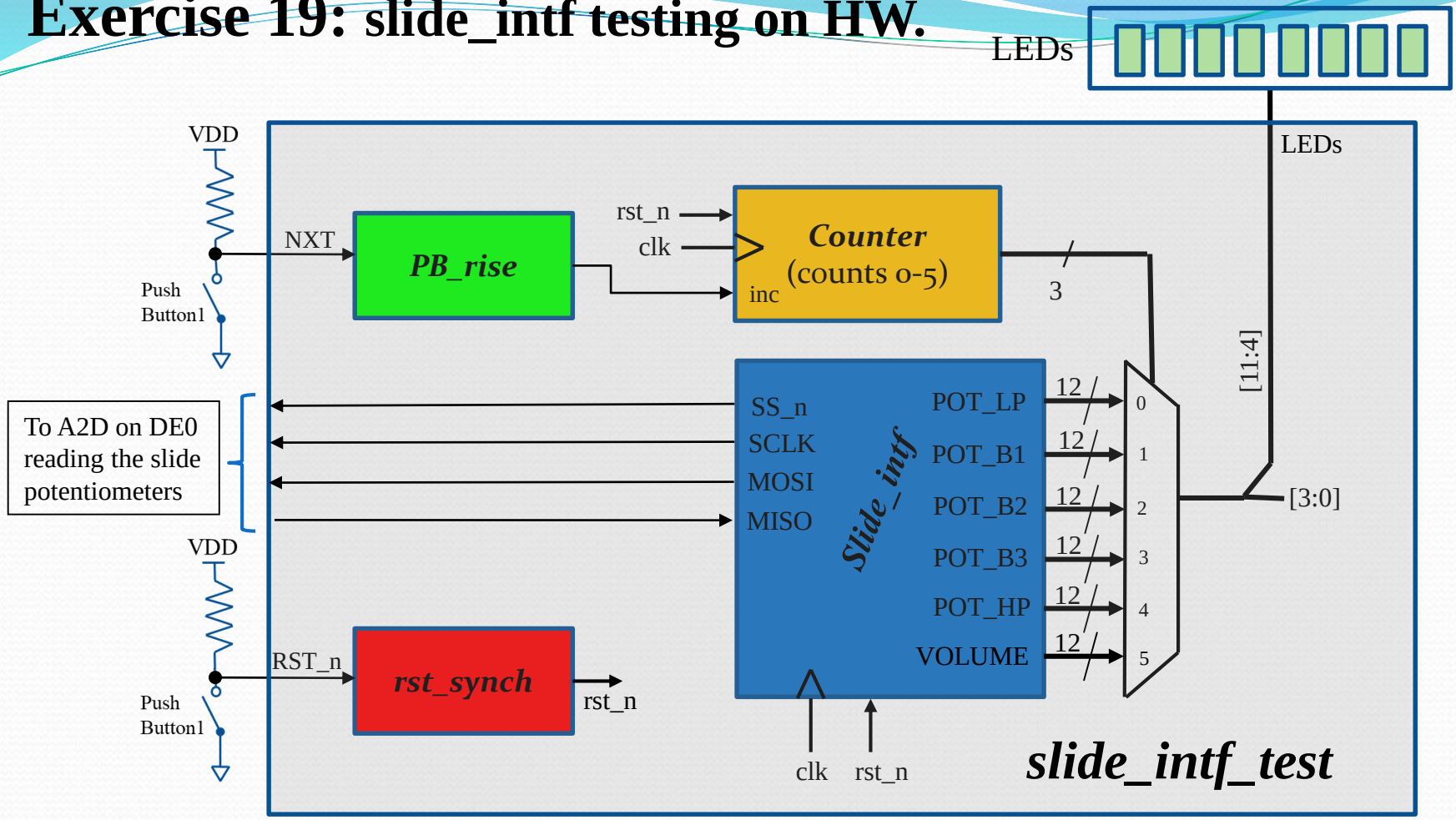
Exercise 19: slide_intf testing on HW.

You have built and tested **slide_intf.sv** in ModelSim, now you will test it on the HW test platform.

Signal:	Dir:	Description:
clk	in	50MHz clock
RST_n	in	From push button. Goes to ***rst_synch*** to produce rst_n
NXT	in	Connected to push button. When button released will move to displaying the next slider
SS_n, SCLK, MOSI	out	SPI interface to A2D on board that is reading the slide potentiometers
MISO	in	SPI serial in from A2D
LEDs[7:0]	out	Used to display the upper 8-bits of selected slide pot

Interface of **slide_intf_test.sv**

Exercise 19: slide_intf testing on HW.



- Produce **slide_intf_test.sv**.
- Copy over sub-modules and compile in Quartus (.qsf & .qpf files available on Canvas page)

Exercise 19: slide_intf testing on HW.

- After successfully compiling in Quartus program your board.
- How do you know it works?
  - What is driving the analog inputs on your board?
  - Yeah…nothing, so it might look kind of random.
  - Call Fego, Eric, or Christian over to test on the HW test platform.
- Once you have checked off with us you are done.