

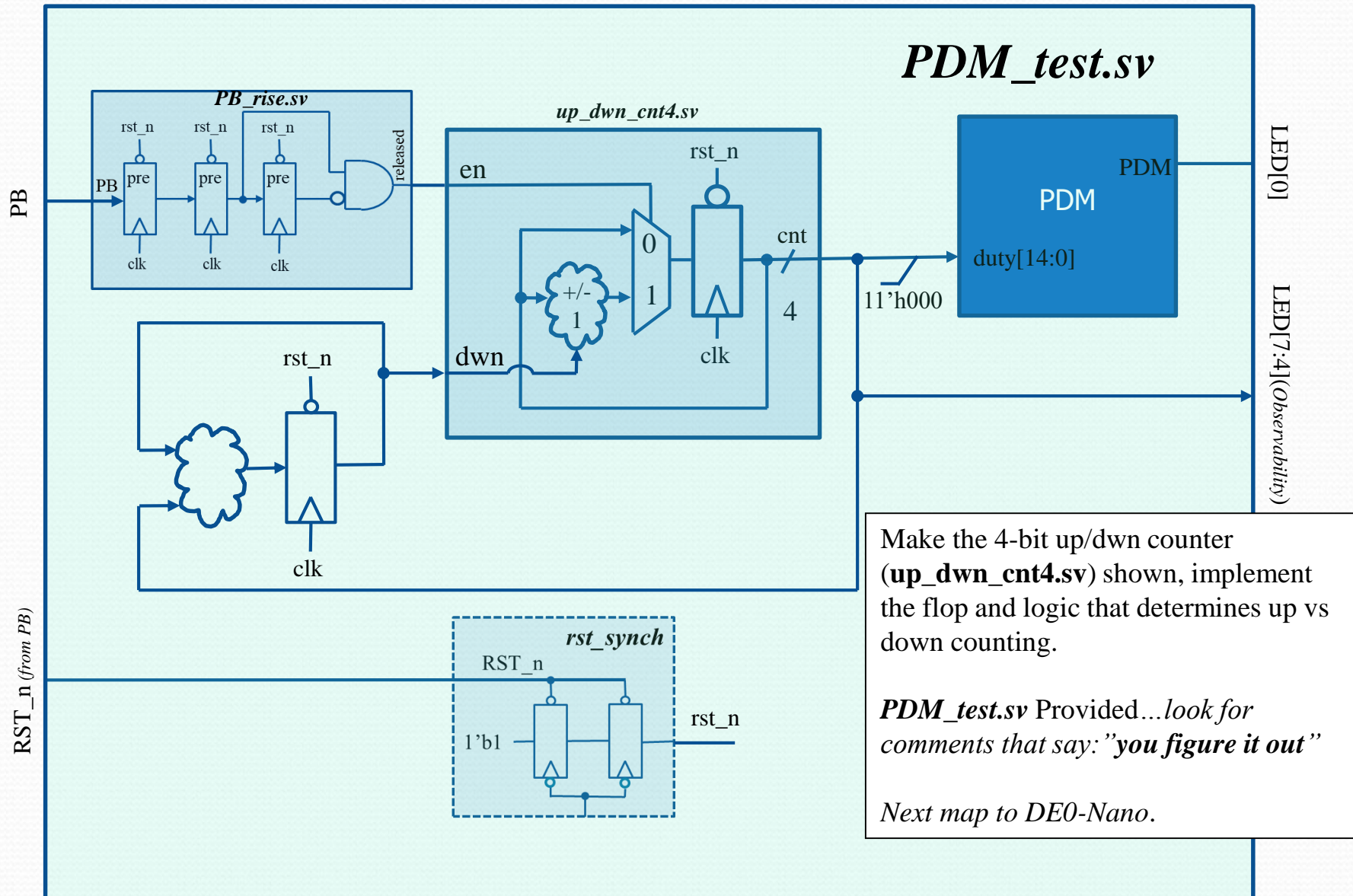
Exercise 10: Testing of PDM on DE0

- In Exercise07 you coded **PDM.sv** which has the interface shown below.

Signal:	Dir:	Description:
clk	in	50MHz clock
rst_n	in	Active low asynch reset
duty[14:0]	in	Duty cycle (from equalizer indicating drive level to speaker)
PDM	Out	Output to the H-bridge to control speaker drive

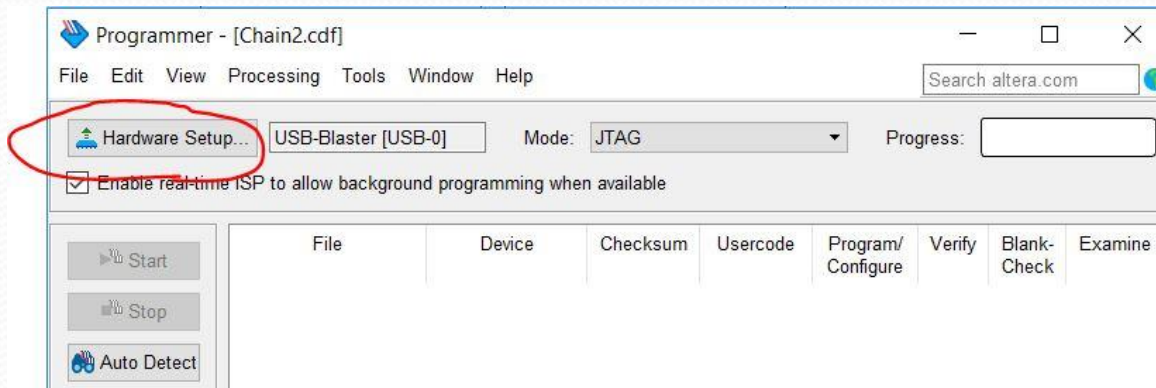
- Now you are going to build a test wrapper (**PDM_test.sv**) for this that will be mapped to your DE0-Nano board and used to test it.
- The test wrapper (**PDM_test.sv**) will contain a 4-bit up/down counter that is enabled by the signal from **PB_rise.sv** (which you just made in Ex09).
- The 4-bit counter is connected to bits [14:11] of **duty[14:0]**. Bits [10:0] being 0.
- The counter will start at 0000 and initially count up with every push of a button (coming from **PB_rise.sv**) and when it hits its full value (1111) it will toggle a flop and then start counting down.

Exercise 10 (Testing of PDM):



Exercise 10 (Testing of PDM) (Mapping to DE0):

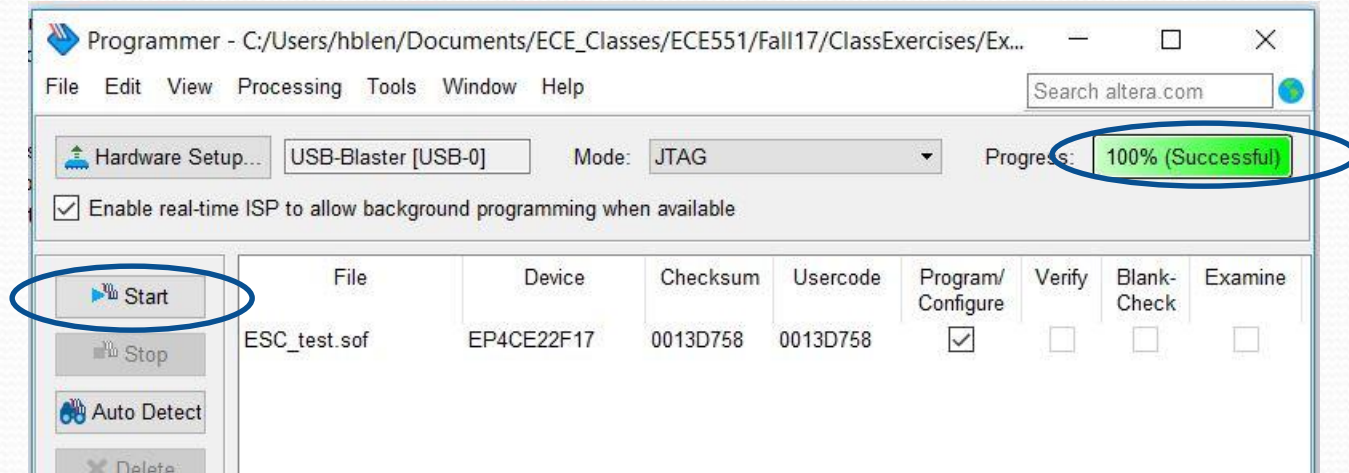
- Download **PDM_test.qpf** (Quartus Project File) and **PDM_test.qsf** (Quartus Settings File) from the website and store in your Exercise10 directory
- Open up Quartus
 - Do a: **File → Open Project** and open up the **PDM_test.qpf**
 - Compile the design and fix any errors
 - Plug in your DE0-Nano Board.
 - Do a: **Tools → Programmer** and check that the USB Blaster shows up (see below) (you may have to wait a while on these CAE machines for it to enumerate)



Might have to go under
“Hardware Setup” to get
it to choose USB-Blaster

Exercise 10 (Testing of PDM) (Mapping to DE0):

- Program the DE0-Nano



- Hit “Start” and look for 100% Success
- See next page for mapping of functions to DE0-Nano

Exercise 10 (Testing of PDM) (Mapping to DE0):

