Computer Sciences Department
University of Wisconsin-Madison
CS/ECE 552 – Introduction to Computer Architecture
In-Class Exercise (03/26)

Answers to all questions should be uploaded on Canvas.

1. [1 point] Consider a virtual memory system with the following parameters:

- 64-bit virtual addresses
- 47-bit physical addresses
- 4KB pages
- 16B cache blocks
- Byte-addressing

How many bits are needed for the page offset, virtual page number, and physical page number?

Offset: 12

PPN: 35

VPN: 52

2. [1 point] For the system in problem 1, assume that the processor has a fully-associative TLB with a hit rate of 95% and a hit time of 1 cycle. How long do address translations take on average, assuming the miss penalty is 100 cycles? What is the speedup over the system without a TLB? Assume that all pages reside in memory and there are no page faults.

3. [4 points] Assume 8KB pages and a 3-way set-associative TLB with 48 entries in total and LRU replacement. Consider the following code segment running on the processor:

```
for (int i = 0; i < 16384; i++)
      C[i] = A[i] + B[i];
```

When each loop iteration executes, it reads A[i] first, then B[i] and finally writes to C[i]. Assume each array element is four bytes. The starting virtual addresses of arrays A, B and C are 0x10000, 0x20000 and 0x30000, respectively.

Assuming that initially none of the array pages are allocated in memory, report the following after all loop iterations have executed.

Total TLB accesses: 49125

Total TLB misses: 27

Total page table accesses: 49152

Total page faults: 0

4. [4 points] Assume a system with 32-bit virtual addresses, total physical memory of 1GB, and page size of 64KB. Each page table entry (PTE) contains a virtual page number (VPN), physical page number (PPN) and one bit each for v/d/ref/read/w/x. Assume a 3-level forward page table. Here, the 16-bit VPN is divided into three fields: the most significant 4 bits are used to index the first-level page table, the next 4 bits are used to index the second-level page table, and the remaining 8 bits are used to index the third-level page table.

Assume a program has been running for a while, and it is accessing memory in the heap, stack and code segments as follows (assume all virtual addresses within the bounds shown are being accessed):

Code segment: 0x00000000 to 0x00001000
Stack segment: 0x10000000 to 0x100100F0
Heap segment: 0x20000000 to 0x320100A0

For the heap segment only, compute the following:

The heap segment occupies _____2_____ total entries in the first level page table

The heap segment occupies _____4_____ total entries in **all** second level page tables.

The heap segment occupies _____6_____ total entries in **all** third level page tables.