Computer Sciences Department
University of Wisconsin-Madison
CS/ECE 552 – Introduction to Computer Architecture
In-Class Exercise (04/21)

Answers to all questions should be uploaded on Canvas.

1. [2 points] From the textbook:
    a. [1 point] (Twist on Check Yourself 6.4) True or False: Both multithreading and multicore rely on parallelism to get more efficiency from a chip.

       Given that the answer is true, what is the difference in the kind of parallelism each is exploiting?

Multithreading: shared data within the core
Multicore: shared data between each core

    b. [1 point] (Twist Check Yourself 6.4) True or False: *Simultaneous Multithreading* (SMT) uses threads to improve resource utilization of a dynamically scheduled, out-of-order processor.

       Given that the answer is true, would SMT also be able to improve resource utilization for in-order processors?
       No.

2. [8 points] Consider four threads running on the same R10K-like processor:

```
     # thread A
A1:  add  $t1, $s5, $t1
A2:  or   $t1, $t1, $s0
A3:  addi $t1, $t1, 4
A4:  beq  $t1, $zero, A1

     # thread B
B1:  addi $s1, $s1, 4
B2:  and  $s2, $s1, $t3
B3:  sub  $s1, $t0, $s2
B4:  bne  $s1, $s4, B1

     # thread C
C1:  and  $t0, $t1, $s0
C2:  sub  $t3, $s4, $t0
C3:  slt  $t1, $t3, $s2
C4:  bne  $t1, $zero, C1

     # thread D
D1:  and  $s0, $t0, $t1
D2:  or   $t0, $t5, $s0
D3:  addi $t0, $t0, 4
D4:  beq  $t0, $zero, D1
```

The processor is **four-wide superscalar** and can fetch (F), decode (De), dispatch (Di) and retire (R) up to four instructions in any given cycle. Assume that all instructions (add, addi, and, beq, bne, or, slt, sub) use the **same type of functional unit** and take one cycle in the X stage. Also assume that there are infinitely many reservation stations, physical registers and reorder buffer entries.

All four threads are running on the same processor. Assume that their loops run indefinitely and that the branch instructions are always taken and predicted perfectly in the F stage.

(a) [4 points] You enable **fine-grained multithreading**. In the first cycle, the processor fetches four instructions from thread A, then four instructions from thread B in the next cycle, then four from thread C, then thread D, back to thread A, and so on. The pipeline diagram for the first eight instructions (i.e., the first two iterations of threads A and B) is shown below. Note that instructions are still retired in the order that they are fetched.

	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
A1	F	De	Di	S	X	C	R							
A2	F	De	Di	S	S	S	X	C	R					
A3	F	De	Di	S	S	S	S	S	X	C	R			
A4	F	De	Di	S	S	S	S	S	S	S	X	C	R	
B1		F	De	Di	S	X	C	R	R	R	R	R	R	
B2		F	De	Di	S	S	S	X	C	R	R	R	R	
B3		F	De	Di	S	S	S	S	S	X	C	R	R	
B4		F	De	Di	S	S	S	S	S	S	S	X	C	R

With fine-grained multithreading of these four threads, what is the **minimum number of functional units** that this processor needs such that no instruction ever needs to wait for a free functional unit?

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	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A1	F	De	Di	S	X	C	R																	
A2	F	De	Di	S	S	S	X	C	R															
A3	F	De	Di	S	S	S	S	S	X	C	R													
A4	F	De	Di	S	S	S	S	S	S	S	X	C	R											
B1		F	De	Di	S	X	C	R	R	R	R	R	R											
B2		F	De	Di	S	S	S	X	C	R	R	R	R											
B3		F	De	Di	S	S	S	S	S	X	C	R	R											
B4		F	De	Di	S	S	S	S	S	S	S	X	C	R										
C1			F	De	Di	S	S	S	S	S	S	S	X	C	R									
C2			F	De	Di	S	S	S	S	S	S	S	S	S	X	C	R							
C3			F	De	Di	S	S	S	S	S	S	S	S	S	S	S	X	C	R					
C4			F	De	Di	S	S	S	S	S	S	S	**S**	S	S	S	S	S	X	C	R			
D1				F	De	Di	S	S	S	S	S	S	S	X	C	R	R	R	R	R	R			
D2				F	De	Di	S	S	S	S	S	S	S	S	S	X	C	R	R	R	R			
D3				F	De	Di	S	S	S	S	S	S	S	S	S	S	S	X	C	R	R			
D4				F	De	Di	S	S	S	SS	S	S	S	SS	S	S	S	S	S	X	C	R		
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(b) [4 points] You enable **simultaneous multithreading**. In each cycle, the processor fetches one instruction each from thread A, B, C and D (in that order). The pipeline diagram for the first four instructions is shown below. Note that instructions are still retired in the order that they are fetched.

	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
A1	F	De	Di	S	X	C	R							
B1	F	De	Di	S	X	C	R							
C1	F	De	Di	S	X	C	R							
D1	F	De	Di	S	X	C	R							

With simultaneous multithreading of these four threads, what is the **minimum number of functional units** that this processor needs such that no instruction ever needs to wait for a free functional unit?

4

Spring 2020, Sinclair

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A1	F	De	Di	S	X	C	R																	
B1	F	De	Di	S	X	C	R																	
C1	F	De	Di	S	X	C	R																	
D1	F	De	Di	S	X	C	R																	
A2		F	De	Di	S	X	C	R																
B2		F	De	Di	S	X	C	R																
C2		F	De	Di	S	X	C	R																
D2		F	De	Di	S	X	C	R																
A3			F	De	Di	S	X	C	R															
B3			F	De	Di	S	X	C	R															
C3			F	De	Di	S	X	C	R															
D3			F	De	Di	S	X	C	R															
A4				F	De	Di	S	X	C	R														
B4				F	De	Di	S	X	C	R														
C4				F	De	Di	S	X	C	R														
D4				F	De	Di	S	X	C	R														
A1																								
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