CS/ECE 552
Spring 2020
Homework 5
Due 11:59 PM Central Time on Friday, April 10th, 2020

You should work both problems with your project groupmate and submit a single solution per group. See *Hand in* directions for additional details. Your group should do this assignment on your own, although you are encouraged to talk with classmates in person or on Piazza about any issues you may have encountered. You group is expected to design your own FSMs and schematics though. If you take an FSM from another group, your group will be penalized according to the UW Student Code of Conduct, as laid out in the syllabus.

The standard late assignment policy applies: you may submit up to 2 days late with a 10% penalty for each late day.

Total Points: 16

The goal of this assignment is to develop the a) schematic and b) state machine diagram for the caches you'll be implementing in your project in Phase 2.3. All of the cache details are listed on the Cache Design Canvas page. **Read it carefully before starting**!

As explained there, you will need to determine how your cache is arranged and functions before starting implementation. Draw out the state machine for your cache controller as this will be required to get it working correctly. You may implement either a Mealy or Moore machine though a Moore machine is recommended as it will likely be easier. Be forewarned that the **resulting state machine will be relatively large so it is best to start early**.

If we have concerns about your design, we will ask you to setup an appointment to talk about your FSM design before the Phase 2.3 due date.

Problem 1 [8 points]

Create the schematic and state machine diagram for the direct-mapped caches you will initially be using in Phase 2.3. As explained above, your memory system schematic should show how the direct-mapped cache, cache controller, and four-bank memory modules are connected (NOTE: these are the modules you will eventually use inside mem_system.v in Phase 2.3). And the state machine diagram should show the various states necessary to correctly operate your cache and the transitions between those states.

Problem 2 [8 points]

Next, we will make our caches two-way set associative. Create the schematic and state machine diagram for a two-way set associative cache. If you do not need any changes to your state machine diagram from Problem 1, please submit the same state machine diagram for both problems.

What to Hand In

To submit this assignment, zip or tar your files together and submit them as a **single file named <netID>-hw5.tgz or <netID>-hw5.zip** on Canvas. Inside this tarball/zip, should be a top-level directory (e.g., hw5), which contains hw5_1/, hw5_2/, and partners.txt; all files for problem 1 should be a folder called hw5_1 and all files for problem 2 should be inside hw5_2 – you must keep this directory structure. **If you need the same file for multiple problems (e.g., problem 1 and problem 2), you should have a copy of that file in each part**. For example, my Net ID is msinclair, so my submission would be called msinclair-hw5.tgz (or msinclair-hw5.zip) and in it would be hw5_1/, hw5_2/, and partners.txt. Note that net ID should be the name of the group member who uploads the submission. If you don't have experience with tar, I recommend consulting tutorials such as this one. *You should work on both problems with your project partner and submit a single solution per group. Names must be included in the partners.txt file*. Note that there are no provided files for this assignment, since everything (besides parterns.txt) is a PDF your group will be creating. However, we encourage you to consult the cache (Phase 2.3) files in (`/u/s/i/sinclair/public/html/courses/cs552/spring2020/handouts/verilog_code/project/project.tgz`) or Github Classroom when designing your FSMs and schematics.

Your single zip/tar per group on Canvas should contain the following files/directories:

1. hw5_1/
    a. **schematic.pdf**: A schematic of your memory system with a direct-mapped cache that should show how the direct mapped cache, cache controller, and four-bank memory modules are connected (NOTE: these are the modules you will eventually use inside mem_system.v in Phase 2.3).
    b. **cacheFSM.pdf**: A state machine diagram for your cache controller for the direct-mapped cache.
2. hw5_2/
    a. **schematic.pdf**: A schematic of your memory system with a two-way set associative cache that should show how the two-way set associative cache, cache controller, and four-bank memory modules are connected (NOTE: these are the modules you will eventually use inside mem_system.v in Phase 2.3).
    b. **cacheFSM.pdf**: A state machine diagram for your cache controller for the two-way set associative cache.
3. **partners.txt** *Names must be included in the partners.txt file, as with other assignments*.

All PDFs may be hand drawn, as long as they are legible. If the schematic or diagram is missing, you will automatically get **zero points** for that component of that problem.

Verifying Your Handin

We have also created a script to check that your submission correctly follows the format, located at:

```
/u/s/i/sinclair/public/html/courses/cs552/spring2020/handouts/scripts/hw5/verify_submission_format.sh <netID>-hw5.tgz
```

You should run this script before submitting in order to ensure that you don't lose points for incorrectly formatting your submission! Additional details about the handin script, including how to run and examples, are available here.

Note that this version of the script does not run anything, it only checks to make sure your PDFs are in the right place.