Computer Sciences Department
University of Wisconsin-Madison
CS/ECE 552 – Introduction to Computer Architecture
In-Class Exercise (03/31)

Answers to all questions should be uploaded on Canvas.

1. [2 points] Recall that the page table resides in main memory. Suppose that the TLB access delay is 1 cycle, the data cache access delay is 2 cycles, and main memory access delay is 10 cycles. In your program, the TLB miss rate is 0.01% and the cache miss rate is 1% on average. Assume there are no page faults, page table entries are not cached in the data cache, and the cache is both indexed and tagged by physical address.

(a) [1 point] What is the average data access latency (in cycles) without a TLB?

0.99*2+0.01*12 = 2.1

(b) [1 point] What is the average data access latency (in cycles) with a TLB?

99.99%+0.01%*2+0.01%*1%*12 = 1.000112

2. [2 points] Assume a **two-level page table** that resides in main memory. Suppose that the TLB access delay is 1 cycle, the data cache access delay is 2 cycles, and main memory access delay is 25 cycles. Assume that the 1-cycle delay is incurred only once per TLB miss and that the 2-cycle delay is incurred only once per cache miss. In your program, the TLB miss rate is 0.01% on average. Assume that there are no page faults and that page table entries are not cached in the data cache.

(a) [1 point] You decide to implement the data cache as **physically indexed and physically tagged**. This yields a **cache miss rate of 3%** on average. What is the average data access latency (in cycles) with your physical cache?

（99.99%）+0.01%*2）*（97%*2+3%*（4+25））= 2.810281

(b) [1 point] You decide to implement the data cache as **virtually indexed and virtually tagged**. This yields a **new cache miss rate of 2%** on average. What is the average data access latency (in cycles) with your virtual cache?

98%*2+2%*4*（99.99%+0.01%*2）*25 = 3.9602

3. [6 points] Consider a virtual memory system with the following parameters.

- 64-bit virtual addresses
- 48-bit physical addresses
- 4KB pages
- 16B cache blocks
- Byte-addressing

Furthermore, it takes 120 cycles for an access to return from main memory.

(a) [1 point] How many bits are needed for the page offset, virtual page number, and physical page number?

Page offset 12 bits

PPN 36

VPN 52

(b) [1 point] What is the minimum size of a page table entry? Ignore bits to guide the replacement policy, but ensure you account for all other necessary bits. Assume a valid page can have every combination of read, write, and execute permissions.

PPN +3 = 39

(c) [2 points] What is the minimum size of an entry in a fully-associative TLB? Again, ignore bits for the replacement policy.

PPPN+VPN +3 = 91

(d) [2 points] Now assume that the processor has a fully-associative TLB with a hit rate of 97% and a hit time of 1 cycle. How long do address translations take now, on average? What is the speedup over the system without a TLB? Again, assume that all pages reside in memory and there are no page faults.

0.97*1+0.03*120 = 4.57

120/4.57 = 260.258%