## **Computer Sciences Department**

## **University of Wisconsin-Madison**

## **CS/ECE 552 – Introduction to Computer Architecture**

## **In-Class Exercise (03/10)**

**Answers to all questions should be uploaded on Canvas.**

1. [1 point] (Twist on Check Yourself 5.9) Which of the following statements (if any) are generally true?

1. There is no way to reduce compulsory misses.
2. Fully associative caches have no conflict misses.
3. In reducing misses, associativity is more important than capacity.

Given that 2 is right, why is 3 wrong?

**Bigger capacity can hold more blocks and data so therefore reduce miss**

2. [2 points] Assume a 4-way set-associative cache uses a 16-bit set index and has 12-bit tags for 32-bit memory addresses.

1. [1 point] What is the block size?

**2^4 = 16 bytes**

1. [1 point] What is the cache capacity?

64 kb

3. [3 points] Show how a 1MB 16-way set-associative cache with 128-byte blocks will be indexed given a 32-bit memory address. In the table below, specify which bits will be used for the tag (**T**), set (**S**) and offset (**O**).

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Bit Index** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3  1 | 3  0 | 2  9 | 2  8 | 2  7 | 2  6 | 2  5 | 2  4 | 2  3 | 2  2 | 2  1 | 2  0 | 1  9 | 1  8 | 1  7 | 1  6 | 1  5 | 1  4 | 1  3 | 1  2 | 1  1 | 1  0 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| T | T | T | T | T | T | T | T | T | T | T | T | T | T | T | T | T | T | T | T | T | S | S | S | S | O | O | O | O | O | O | O |

4. [4 points] Consider the following sequence of accesses to memory blocks in one set of a 4-way set-associative cache.

1. [3 points] Fill in the table below assuming LRU replacement. When there are unpopulated ways, assume they get filled in from left to right.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Block** | **Way Contents Before** | **Way Contents After** | **LRU Before** | **LRU After** |
| A | [-, -, -, -] | [A, -, -, -] | -- | -- |
| B | [A, -, -, -] | [A, B, -, -] | - | - |
| C | [A, B, -, -] | [A, B, C, -] | - | - |
| D | [A, B, C, -] | [A, B, C, D] | - | A |
| C | [A, B, C, D] | [A, B, D, C] | A | A |
| E | [A, B, D, C] | [B, D, C, E] | A | B |
| A | [B, D, C, E] | [D, C, E, A] | B | D |
| C | [D, C, E, A] | [D, E, A, C] | D | D |
| D | [D, E, A, C] | [E, A, C, D] | D | E |
| B | [E, A, C, D] | [A, C, D, B] | E | A |
| E | [A, C, D, B] | [C, D, B, E] | A | C |
| A | [C, D, B, E] | [D, B, E, A] | C | D |
| C | [D, B, E, A] | [B, E, A, C] | D | B |

1. [1 point] What is the miss rate?

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