MT7905DAN Datasheet

802.11ax Wi-Fi 2x2 Dual-band Con-current Baseband Chip

Version: 1.3
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Specifications are subject to change without notice.

Document Revision History

Revision	Date	Author	Description
1.0	2020-03-17	CH Hung	Formal version
1.1	2020-03-26	CH Hung	1. Update 1.1 General Description 2. Update 1.3 Block Diagram 3. Update 4.1 Pin Layout
1.2	2020-04-17	CH Hung	1. Update 4.1/4.2 Pin layout/description
1.3	2020-06-08	CH Hung	1. Update 2.2.2 Chip power on sequence 2. Update 3.1 / 3.2 and 4.3

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1 System overview

1.1 General Description

The MT7905DAN is a highly integrated Wi-Fi A/D chip which supports 573+1201 Mbps PHY rate. It fully complies with IEEE 802.11ax and backward compatible with IEEE 802.11 a/b/g/n/ac standards, offering feature-rich wireless connectivity at high standards, and delivering reliable, cost-effective throughput from an extended distance.
Optimized RF architecture and baseband algorithms provide superb performance and low power consumption. Intelligent MAC design deploys a high efficient offload engine and hardware data processing accelerators which fully offloads WiFi task of the host processor. The MT7905DAN is designed to support standard based features in the areas of security, quality of service and international regulations, giving end users the greatest performance any time and in any circumstance.

1.2 Features

1.2.1 Technology and package

- 12x12 DR-QFN 164 pins package

1.2.2 Power management and clock source

- MT7905DAN support 40MHz crystal clock with low power operation in idle mode

1.2.3 Platform

- 32-bit RISC MCU for Wi-Fi protocols
- Embedded SRAM/ROM
- UART interface with hardware flow control
- PCIe device fully compliant to PCIe v2.1 specification

1.2.4 WLAN

- IEEE 802.11 a/b/g/n/ac/ax compliant
- Support 20/40M bandwidth in 2.4G band and 20/40/80M bandwidth in 5G band
- 2T2R in 2.4G+2T2R in 5G with support of up to 573+1201Mbps PHY rate
- Support MU-MIMO TX/RX
- Support MU-OFDMA TX/RX
- Support STBC, LDPC, TX Beamformer and RX Beamformee
- Greenfield, mixed mode, legacy modes support
- Security support for WFA WPA/WPA2/WPA3 personal, WPS2.0, WAPI
- QoS support of WFA WMM, WMM PS
- Integrated LNA, PA, and T/R switch
- Optional external LNA and PA support.

1.2.5 Miscellaneous

- Integrate 4096bits efuse to store device specific information.

1.3 Block Diagram

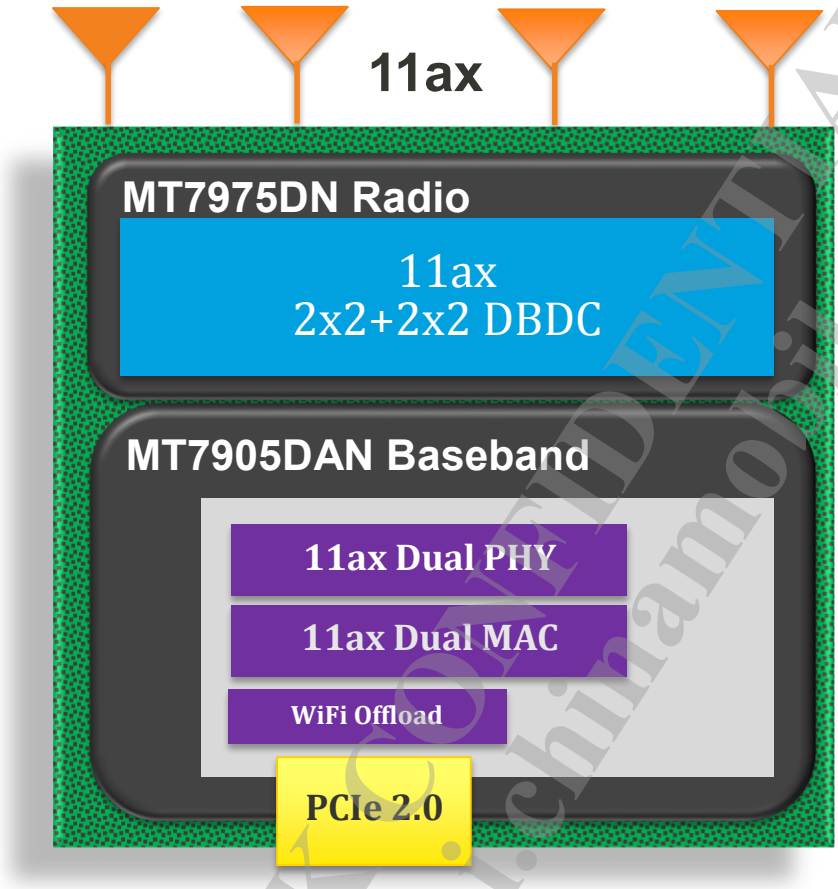


Figure 1 MT7905DAN block diagram

2 Functional Description

2.1 Overview

MT7905DAN is designed to support high data throughput over Wi-Fi. The host interface PCIe are integrated to provide stable bandwidth between the host platform and MT7905DAN. The clock rate of the internal bus fabric can also support the throughput the requirement. The clock rate of MCU is also configurable for different kinds of scenarios.

MT7905DAN supports low power requirement. Multiple power domains are implemented on chip. It defines a deep sleep mode, in which only the AON domain is powered on, while other OFF domains are shut off by the power switches integrated on chip. In deep sleep mode, the PMU could be further configured to be in a low power state to save the power consumption. The power, clock, and reset schemes of MT7905DAN are described in 2.2.

MT7905DAN has a 32-bit RISC MCU subsystem. The CPU has its local memory. They also have common memory space for MEMORY and memory-mapped hardware engine. There are several options of clock frequency to provide the optimal performance with the best power consumption. The 32-bit RISC MCU is used to do clock control, power management, and host interface configuration and also handle Wi-Fi MAC operations,. PDMA (packet DMA) engines are integrated to support on-the-fly data buffer management. The architecture of 32-bit RISC MCU subsystem is described in 2.3.

MT7905DAN features PCIe2.1 for the host interface. The configuration and the feature set of the interface are described in 2.4.

MT7905DAN has the Wi-Fi MAC and BBP subsystem and use with MT7975DN together, which provide the best-in-class radio and low power performance. The architecture of Wi-Fi subsystem is described in 2.5.

2.2 Chip architecture

The section describes the power, clock, and reset schemes in MT7905DAN.

2.2.1 Chip power plan

The external power source can be directly supplied to the Power Management Unit, digital IOs, PCIe PHY and digital circuit on MT7905DAN. The on-chip Power Management Unit contains a number of LDOs. It converts the 3.3V input to other power rails.
PMU:

- 3.3V to 1.05V by PHYLDO for PCIe PHY circuit.
- 3.3V to lower voltage by ELDO for EFuse write operation.

2.2.2 Chip power on sequence

The figure below shows the chip power on sequence.

DVDD power can be ready prior to AVDD33* (refer to timing spec of case1) or between AVDD33* and AVDD18* (refer to timing spec of case2).

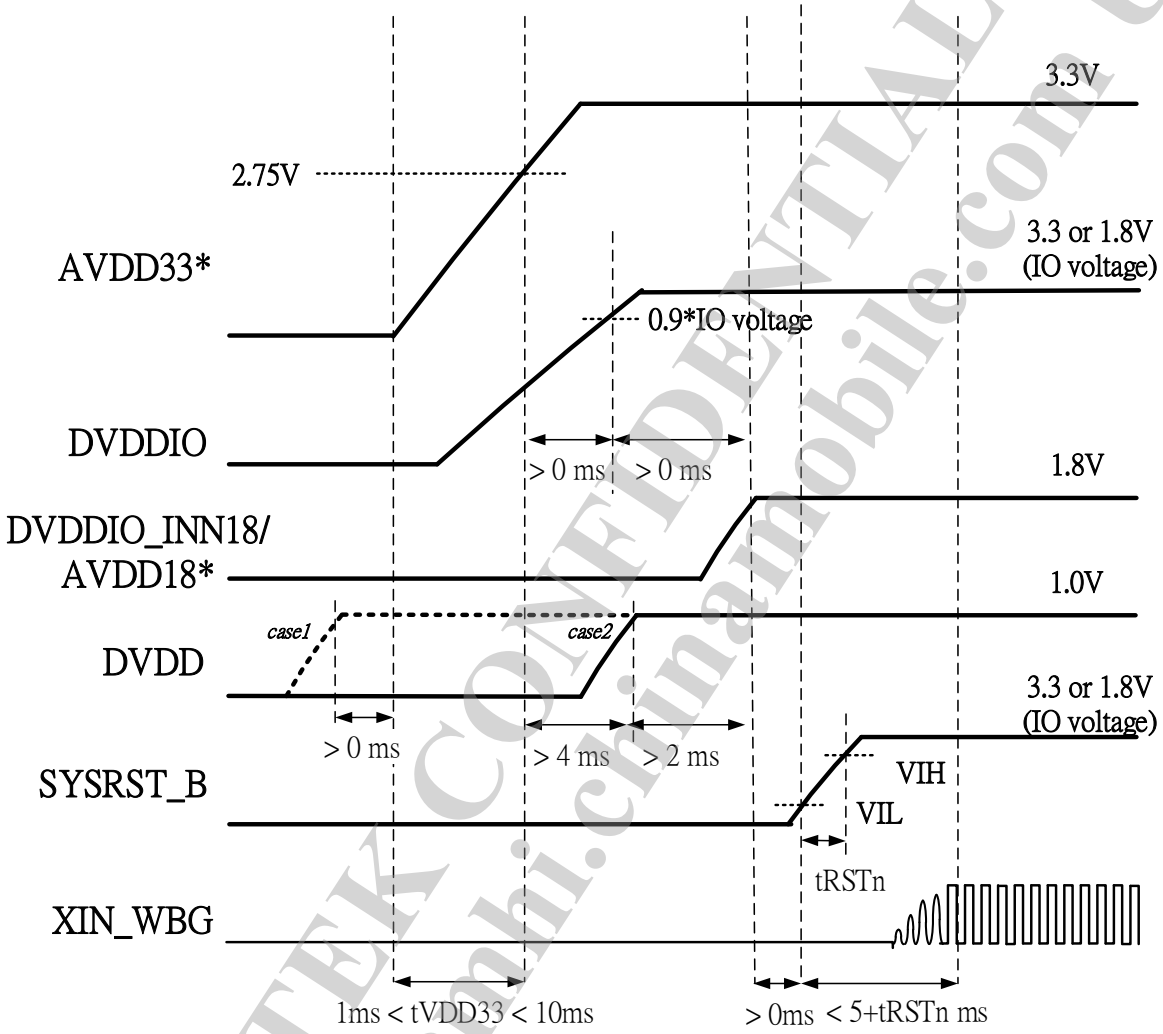


Figure 2 Chip power on sequence

2.2.3 Digital power domain

The digital circuit is separated into AON (always-on), MCU, Wi-Fi MAC, Wi-Fi baseband, and PCIE power domains. Except AON, each power domain can be turned off individually for different sleep scenarios.

2.2.4 Clock

2.2.4.1 Clock scheme

MT7905DAN use external clock source from MT7975DN as the single clock source of the whole system. MT7905DAN clock source only support 40MHz only.
There are 2 major PLLs, MCU PLL, and WF PLL that generate the clocks for the digital circuit. The clocks can be gated to save power when it's not used.

2.2.5 Reset

2.2.5.1 Global reset

MT7905DAN has 2 global resets as follows:

- Cold reset by AVDD33_PMU, AVDD33_PHYLDO — Whole chip reset.
- System reset by SYSRST_B – Reset digital circuit, include strapping and XTAL controller.

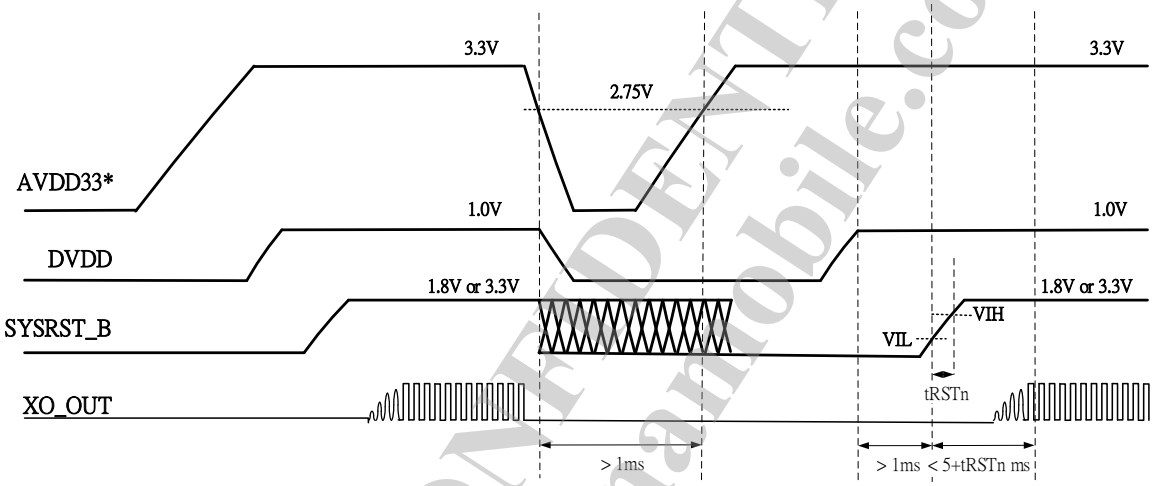


Figure 3 Cold reset sequence

2.3 32-bit RISC MCU subsystem

2.3.1 WiFi MCU subsystem

The WiFi MCU subsystem is built upon a multi-layer AXI bus fabric infrastructure. There is 256KB ROM and 640KB RAM in local memory.

2.4 Host interface subsystem

2.4.1 PCIe interface

MT7905DAN supports PCI Express End Point which is fully compliant with the PCI Express Base Specification Revision 2.0. It supports PCI Express Gen1 (2.5Gbps) and PCIE Express Gen2 (5.0Gbps) differential bus speed.
MT7905DAN supports PCI Express low power operations such as ASPM L1.0, ASPM L1.CLK_PM, ASPM L1.SS (L1.1 and L1.2), and PCI PM L2 state. It also supports WAKE_N for device wakeup host scenario, as well as remote wake-up signaling.
The PCI Express interface is only used for Wi-Fi operations. The DMA ring and the data structure are controlled by the descriptor-based PDMA engine over PCI Express interface.

2.4.1.1 PERST_N

Fundamental reset is triggered when PERST_N is asserted with power already applied to the device and SYSRST_B have been asserted.

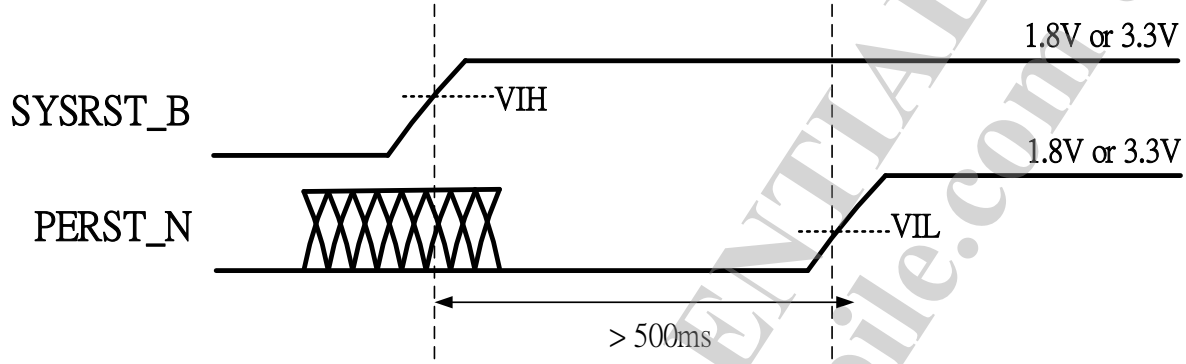


Figure 4 PERST_N sequence

2.5 Wi-Fi subsystem

2.5.1 Wi-Fi MAC

2.5.1.1 Features

Wi-Fi MAC supports the following features:

- Support all date rates of 802.11a/g including 6, 9, 12, 18, 24, 36, 48, and 54Mbps
- Support short GI and all data rates of 802.11n including MCS0 to MCS7
- Support 802.11ac MCS0 to MCS9
- Support 802.11ax MCS0 to MCS11
- AMPDU/AMSDU RX (de-aggregation) and TX (aggregation) support
- TX beamformer and RX beamformee
- TX rate adaptation
- TX power control
- Security
  - 64-bit WEP (WEP-40) and 128-bit WEP (WEP-104) encryption with hardware TKIP and CKIP processing
  - AES-CCMP hardware processing
  - GCMP hardware processing
  - SMS4-WPI (WAPI) hardware processing
- Low power beacon filtering
- Management/control frame filtering

2.5.2 WLAN Baseband

2.5.2.1 Features

Wi-Fi baseband supports the following features:

- 20/40/80 MHz channels
- HE MCS0-11 BW20/40/80MHz with Nss=1~2
- Short Guard Interval
- Space-time block code (STBC)
- Low Density Parity check (LDPC)
- Support digital pre-distortion to enhance PA performance
- Smoothing (channel estimation) extension to MIMO case
- DFS radar detection
- Beamformer (explicit/implicit)
  - Decoded BW20/40/80 up to 2x2 BF matrix apply
- Beamformee
  - Decoded BW20/40/80 up to 4x2 MU matrix feedback
- MU-MIMO RX

3 Electrical Characteristics

3.1 Absolute maximum rating

Symbol	Parameters	Maximum rating	Unit
VDD33	3.3V Supply Voltage	-0.3 to 3.63	V
VDD18	1.8V Supply Voltage	-0.3 to 1.98	V
DVDD	1.0V Supply Voltage	-0.3 to 1.1	V
T_{STG}	Storage Temperature	-40 to +125	°C
VESD	ESD protection (HBM)	2000	V

Table 1 Absolute maximum rating

3.2 Recommended operating range

Symbol	Rating	MIN	TYP	MAX	Unit
VDD33	3.3V Supply Voltage	3	3.3	3.6	V
VDD18	1.8V Supply voltage	1.71	1.8	1.89	V
DVDD	1.0V Supply voltage	0.9	1.0	1.1	V
$T_{AMBIENT}$	Ambient Temperature	-10	-	70	°C

Table 2 Recommended operating range

3.3 DC characteristics

The digital IO supports VDD33 or VDD18 application.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V_{IL}	Input Low Voltage	Input voltage • VDD33 • VDD18	 -0.3 -0.3	-	 0.8 0.58	V
V_{IH}	Input High Voltage	Input voltage • VDD33 • VDD18	 2.0 1.27	-	 VDD33+0.3 VDD18+0.3	V
V_{OL}	Output Low Voltage	Input voltage • VDD33 • VDD18 $\|I_{OL}\|$ = 4~16 mA	 -0.3 -0.3	-	 0.4 0.2	V
V_{OH}	Output High Voltage	Input voltage • VDD33 • VDD18 $\|I_{OH}\|$ = 4~16 mA	 VDD33-0.4 VDD18-0.2	-	 VDD33+0.3 VDD18+0.3	V
R_{PU}	Input Pull-Up Resistance	Input voltage • VDD33 • VDD18 PU=high, PD=low	 40 10	75 50	190 100	KΩ
R_{PD}	Input Pull-Down Resistance	Input voltage • VDD33 • VDD18 PU=low, PD=high	 40 10	75 50	190 100	KΩ

Table 3 DC characteristics of 3.3V application

3.4 XTAL oscillator

The table below lists the requirement for the XTAL.

Parameter	Value
Frequency	40MHz
Frequency stability	±10 ppm @ 25℃

Table 4 XTAL oscillator requirement

3.5 PMU Characteristics

PARAMETER	CONDITIONS	PERFORMANCE			
		MIN	TYP	MAX	Unit
PHY LDO					
Input voltage		2.97	3.3	3.63	V
Output voltage			1.05		V
Output current		-	-	60	mA
Quiescent current		-	40	50	uA

Table 5 PMU electrical characteristic

3.6 Thermal characteristics

Θ_{JC} assumes that all the heat is dissipated through the top of the package, while Ψ_{Jt} assumes that the heat is dissipated through the top, sides, and the bottom of the package. Thus it's suggested to use Ψ_{Jt} to estimate the junction temperature.

Symbol	Description	Performance	
		Typical	Unit
T_J	Maximum Junction Temperature (Plastic Package)	125	°C
Θ_{JA}	Junction to ambient temperature thermal resistance	16.7	°C/W
Θ_{JC}	Junction to case temperature thermal resistance	4.39	°C/W
Ψ_{Jt}	Junction to the package thermal resistance	0.95	°C/W

Note: JEDEC 51-7 system FR4 PCB size: 76.2x114.3mm (3"x4.5"), 4 layer.

Table 6 Thermal characteristics

4 Package specification

4.1 Pin Layout

MT7905DAN uses DR-QFN package of with 12mm x 12mm dimension.

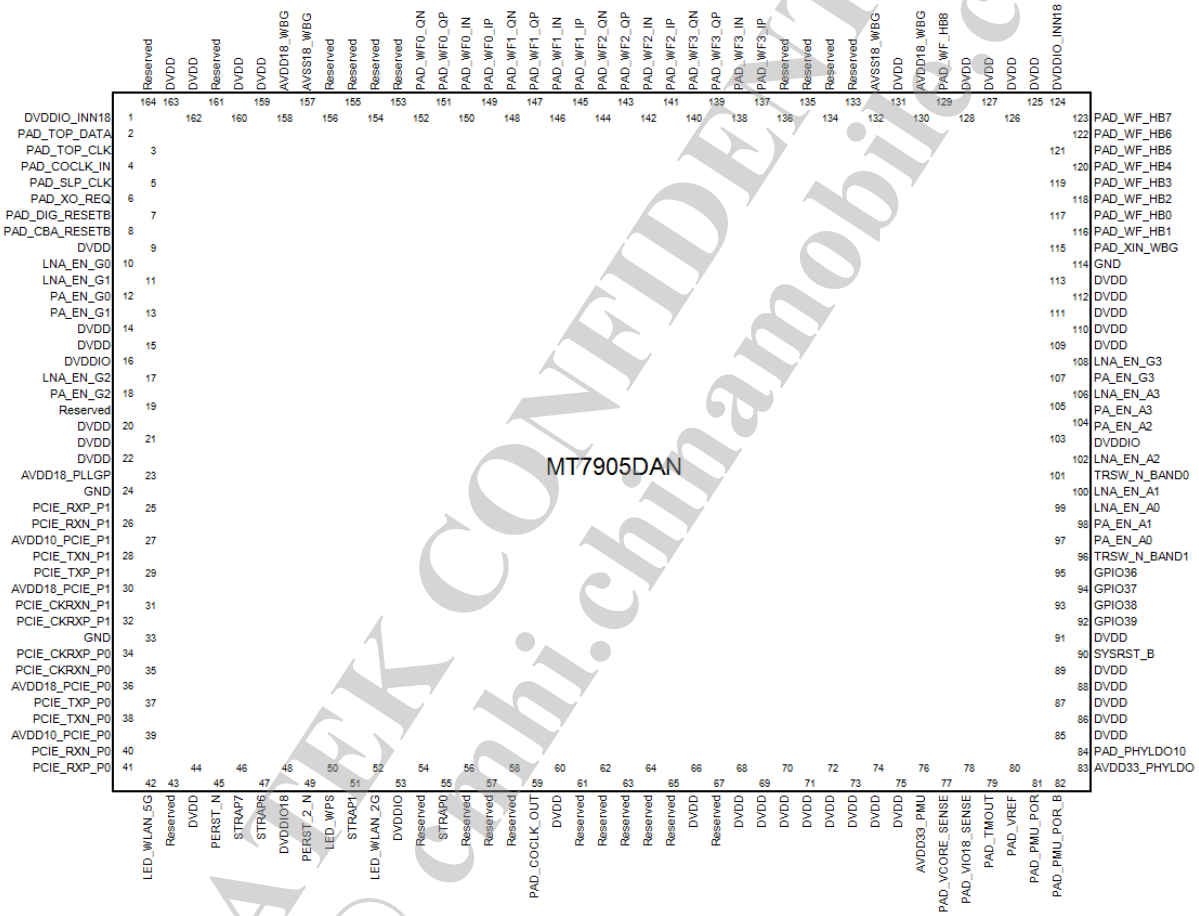


***Figure** 5 MT7905DAN Pin Layout*

4.2 Pin Description

The section describes the pin functionality of MT7905DAN chip.

QFN	Pin Name	Pin description	PU/PD	I/O	Supply domain
Reset and clocks					
90	SYSRST_B	External system reset active low	PU	Input	DVDDIO
115	PAD_XIN_WBG	40MHz Clock input	N/A	Input	
4	PAD_COCLK_IN	Co-Clock input	N/A	Input	

59	PAD_COCLK_OUT	Co-Clock output	N/A	Output	
To RF-Die Digital Interface					
2	PAD_TOP_DATA		PU/PD	In/out	DVDDIO_INN18
3	PAD_TOP_CLK		PU/PD	In/out	DVDDIO_INN18
5	PAD_SLP_CLK		PU/PD	In/out	DVDDIO_INN18
6	PAD_XO_REQ		PU/PD	In/out	DVDDIO_INN18
7	PAD_DIG_RESETB		PU/PD	In/out	DVDDIO_INN18
8	PAD_CBA_RESETB		PU/PD	In/out	DVDDIO_INN18
116	PAD_WF_HB1		PU/PD	In/out	DVDDIO_INN18
117	PAD_WF_HB0		PU/PD	In/out	DVDDIO_INN18
118	PAD_WF_HB2		PU/PD	In/out	DVDDIO_INN18
119	PAD_WF_HB3		PU/PD	In/out	DVDDIO_INN18
120	PAD_WF_HB4		PU/PD	In/out	DVDDIO_INN18
121	PAD_WF_HB5		PU/PD	In/out	DVDDIO_INN18
122	PAD_WF_HB6		PU/PD	In/out	DVDDIO_INN18
123	PAD_WF_HB7		PU/PD	In/out	DVDDIO_INN18
129	PAD_WF_HB8		PU/PD	In/out	DVDDIO_INN18
161	Reserved	Reserved Pin	PU/PD	In/out	DVDDIO_INN18
164	Reserved	Reserved Pin	PU/PD	In/out	DVDDIO_INN18
To RF-Die Analog Interface					
133	Reserved		N/A	Analog	
134	Reserved		N/A	Analog	
135	Reserved		N/A	Analog	
136	Reserved		N/A	Analog	
137	PAD_WF3_IP		N/A	Analog	
138	PAD_WF3_IN		N/A	Analog	
139	PAD_WF3_QP		N/A	Analog	
140	PAD_WF3_QN		N/A	Analog	
141	PAD_WF2_IP		N/A	Analog	
142	PAD_WF2_IN		N/A	Analog	
143	PAD_WF2_QP		N/A	Analog	
144	PAD_WF2_QN		N/A	Analog	
145	PAD_WF1_IP		N/A	Analog	
146	PAD_WF1_IN		N/A	Analog	
147	PAD_WF1_QP		N/A	Analog	
148	PAD_WF1_QN		N/A	Analog	
149	PAD_WF0_IP		N/A	Analog	

150	PAD_WF0_IN		N/A	Analog	
151	PAD_WF0_QP		N/A	Analog	
152	PAD_WF0_QN		N/A	Analog	
153	Reserved		N/A	Analog	
154	Reserved		N/A	Analog	
155	Reserved		N/A	Analog	
156	Reserved		N/A	Analog	
PMU					
76	AVDD33_PMU	PMU 3.3V supply	N/A	Input	
77	PAD_VCORE_SENSE	DVDD 1.0V voltage sense	N/A	Input	
78	PAD_VIO18_SENSE	DVDDIO18 1.8V voltage sense	N/A	Input	
79	PAD_TMOUT	PMU monitor	N/A	Output	
80	PAD_VREF		N/A	Output	
81	PAD_PMU_POR	Power ready indicator	N/A	Output	
82	PAD_PMU_POR_B	Power ready indicator	N/A	Output	
83	AVDD33_PHYLDO	PHY LDO 3.3V supply	N/A	Input	
84	PAD_PHYLDO10	PHY LDO 1.05V output	N/A	Output	
Miscellaneous					
108	LNA_EN_G3	External component control	N/A	Output	DVDDIO
107	PA_EN_G3	External component control	N/A	Output	DVDDIO
106	LNA_EN_A3	External component control	N/A	Output	DVDDIO
105	PA_EN_A3	External component control	N/A	Output	DVDDIO
104	PA_EN_A2	External component control	N/A	Output	DVDDIO
102	LNA_EN_A2	External component control	N/A	Output	DVDDIO
101	TRSW_N_BAND0	External component control	N/A	Output	DVDDIO
100	LNA_EN_A1	External component control	N/A	Output	DVDDIO
99	LNA_EN_A0	External component control	N/A	Output	DVDDIO
98	PA_EN_A1	External component control	N/A	Output	DVDDIO
97	PA_EN_A0	External component control	N/A	Output	DVDDIO
96	TRSW_N_BAND1	External component control	N/A	Output	DVDDIO
61	Reserved	Reserved Pin	N/A	Output	DVDDIO
58	Reserved	Reserved Pin	N/A	Output	DVDDIO
57	Reserved	Reserved Pin	N/A	Output	DVDDIO
56	Reserved	Reserved Pin	N/A	Output	DVDDIO
55	STRAP0	Bootstrap Pin	N/A	Output	DVDDIO
54	Reserved	Reserved Pin	N/A	Output	DVDDIO
52	LED_WLAN_2G	LED control	N/A	Output	DVDDIO

51	STRAP1	Bootstrap Pin	N/A	Output	DVDDIO
50	LED_WPS	LED control	N/A	Output	DVDDIO
49	PERST_2_N	PCIe 2 functional reset	N/A	Output	DVDDIO
47	STRAP6	Bootstrap Pin	N/A	Output	DVDDIO
46	STRAP7	Bootstrap Pin	N/A	Output	DVDDIO
45	PERST_N	PCIe functional reset	PU	Input	DVDDIO
43	Reserved	Reserved Pin	N/A	Output	DVDDIO
42	LED_WLAN_5G	LED control	N/A	Output	DVDDIO
10	LNA_EN_G0	External component control	N/A	Output	DVDDIO
11	LNA_EN_G1	External component control	N/A	Output	DVDDIO
12	PA_EN_G0	External component control	N/A	Output	DVDDIO
13	PA_EN_G1	External component control	N/A	Output	DVDDIO
17	LNA_EN_G2	External component control	N/A	Output	DVDDIO
18	PA_EN_G2	External component control	N/A	Output	DVDDIO
19	Reserved	Reserved Pin	N/A	Output	DVDDIO
95	GPIO36	SW ANT diversity control	N/A	Output	DVDDIO
94	GPIO37	SW ANT diversity control	N/A	Output	DVDDIO
93	GPIO38	SW ANT diversity control	N/A	Output	DVDDIO
92	GPIO39	SW ANT diversity control	N/A	Output	DVDDIO
65	Reserved	Reserved Pin	N/A	Output	DVDDIO
64	Reserved	Reserved Pin	N/A	Output	DVDDIO
63	Reserved	Reserved Pin	N/A	Output	DVDDIO
62	Reserved	Reserved Pin	N/A	Output	DVDDIO
67	Reserved	Reserved Pin	PD	Input	DVDDIO
power supplies					
16,53,103	DVDDIO	Digital IO power input	N/A	Power	
1,124	DVDDIO_INN18	Digital A/D-Die IO power input	N/A	Power	
48	DVDDIO18	Digital IO power input	N/A	Power	
9,14,15,20,21,22,44,60,66,68-75,85-89,91,109-113,125-128,131,159,160,162,163	DVDD	Digital CORE power input	N/A	Power	
24,33,114	GND	Ground	N/A	Ground	
23	AVDD18_PLLGP	MCU PLL power supply	N/A	Power	
130,158	AVDD18_WBG	ADC/DAC power supply	N/A	Power	
132,157	AVSS18_WBG	ADC/DAC ground	N/A	Ground	

PCIE interface					
34	PCIE_CKRXP_P0	PCIe differential reference clock	N/A	Analog	
35	PCIE_CKRXN_P0	PCIe differential reference clock	N/A	Analog	
36	AVDD18_PCIE_P0	PCIe 1.8V power supply	N/A	Power	
37	PCIE_TXP_P0	PCIe transmit differential pair	N/A	Analog	
38	PCIE_TXN_P0	PCIe transmit differential pair	N/A	Analog	
39	AVDD10_PCIE_P0	PCIe 1.05V power supply	N/A	Power	
40	PCIE_RXN_P0	PCIe receive differential pair	N/A	Analog	
41	PCIE_RXP_P0	PCIe receive differential pair	N/A	Analog	
32	PCIE_CKRXP_P1	PCIe differential reference clock	N/A	Analog	
31	PCIE_CKRXN_P1	PCIe differential reference clock	N/A	Analog	
30	AVDD18_PCIE_P1	PCIe 1.8V power supply	N/A	Power	
29	PCIE_TXP_P1	PCIe transmit differential pair	N/A	Analog	
28	PCIE_TXN_P1	PCIe transmit differential pair	N/A	Analog	
27	AVDD10_PCIE_P1	PCIe 1.05V power supply	N/A	Power	
26	PCIE_RXN_P1	PCIe receive differential pair	N/A	Analog	
25	PCIE_RXP_P1	PCIe receive differential pair	N/A	Analog	

Table 7 MT7905DAN pin descriptions

4.3 Bootstrap

The section describes the bootstrap function. The chip modes are sensed from the device pin during power up. After chip reset, the pull configuration are stored in a register and determine the device operation mode.

XTAL mode	STRAP7	STRAP6	STRAP1	XO_IN	XO_out_A	XO_out_B	Description
OSC	Pull-up	Pull-down	Pull-down	40MHz	40MHz	40MHz	Uses 40M XTAL
Buffer	Pull-up	Pull-down	Pull-up	40MHz	40MHz	40MHz	From other MT7975
OSC	Pull-up	Pull-up	Pull-down	40MHz	40MHz	80MHz	Uses 40M XTAL
Buffer	Pull-up	Pull-up	Pull-up	80MHz	40MHz	40MHz	From other MT7975

Note: XTAL mode is defined for MT7975DN RF chip

Table 8 Bootstrap option – XTAL clock mode

Chip mode	STRAP0	Description
Normal mode	Pull-down	Chip operates in normal mode.

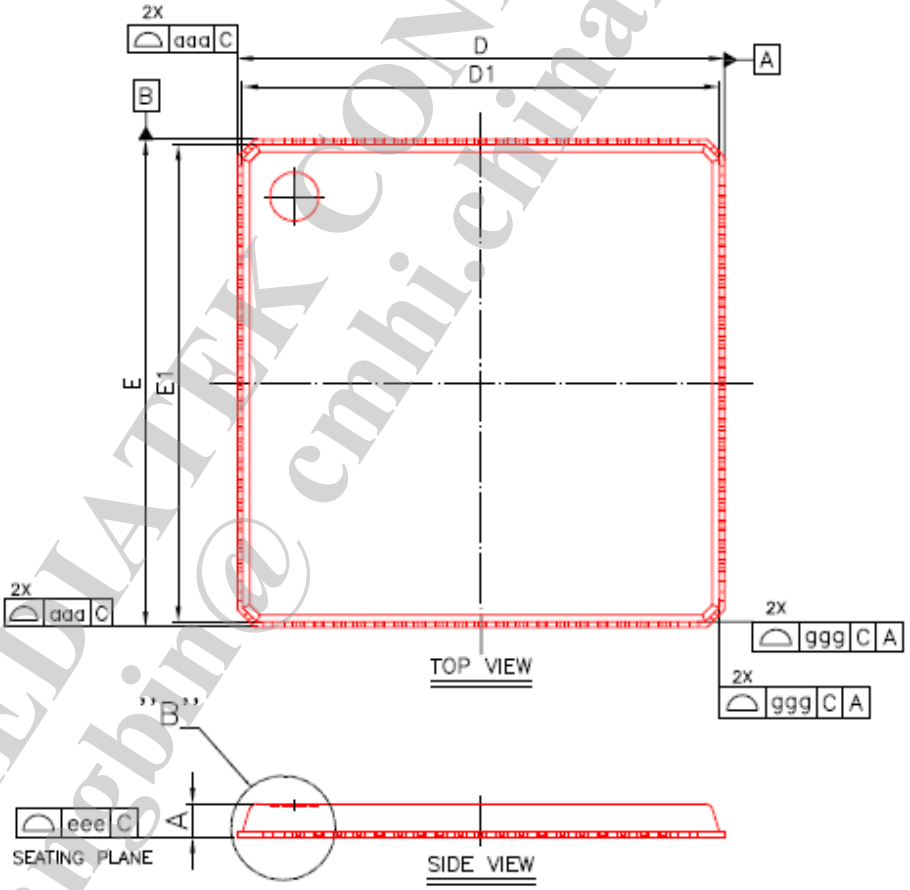
Chip mode	STRAP0	Description
Test mode	Pull-up	Chip operates in test mode.

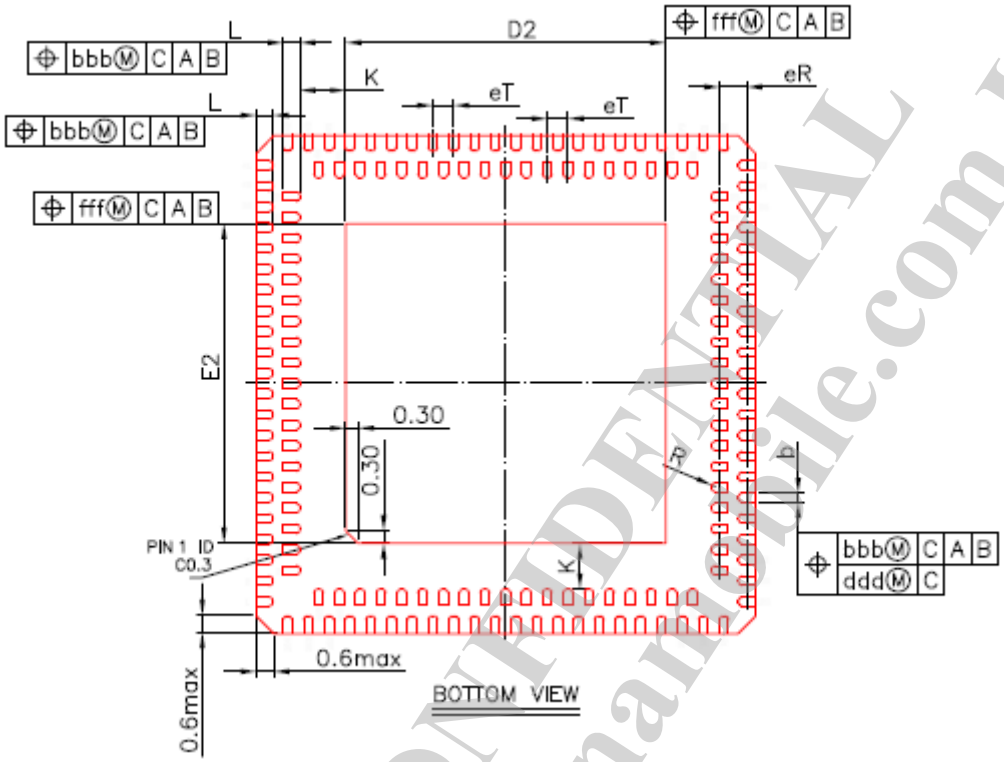
Table 9 Bootstrap option – Chip mode

Pins STRAP0, STRAP1, STRAP6 and STRAP7 are used for bootstrap. The system design should follow the following guideline:

- Those pins shall not be used as input functions because the signals from other device might affect the values sensed.
- Those pins shall not be used as an open-drain function because the pull-up resistor would affect the values sensed.

4.4 Package information





Item	SYMBOL	MIN.	NOM.	MAX.
TOTAL THICKNESS	A	0.80	0.85	0.90
LEAD STAND OFF.	A1	0.00	0.02	0.05
MOLD THICKNESS	A2	0.65	0.70	0.75
L/F THICKNESS	A3		0.15 REF.	
LEAD WIDTH	b	0.18	0.22	0.30
PACKAGE SIZE	D	11.90	12.00	12.10
	E			
Mold Edge size	D1		11.75 BSC	
	E1		11.75 BSC	
E-PAD size	D2	7.60	7.70	7.80
	E2	7.60	7.70	7.80
LEAD LENGTH	L	0.30	0.40	0.50
LEAD PITCH (BSC.)	eT		0.50 BSC	
LEAD PITCH (BSC.)	eR		0.65 BSC	
ANGLE	θ1	5°	---	15°
LEAD ARC	R	0.09	---	0.14
Lead to E-PAD Toler-ance	K	0.20	---	---
PKG EDGE TOLER-ANCE	aaa		0.10	
PACKAGE PROFILE OF A SURFACE	bbb		0.10	
LEAD PROFILE OF A SURFACE	ccc		0.10	
LEAD POSITION	ddd		0.05	
LEAD PROFILE OF A SURFACE	eee		0.08	
EPAD POSTION	fff		0.10	
Mold edge OF A & C SURFACE	ggg		0.20	

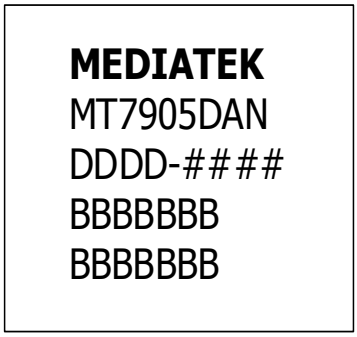
Figure 6 Package outline drawing

4.5 Ordering Information

Part number	Package	Operational temperature range
MT7905DAN	12x12x0.9 mm 164L DR-QFN	-10~70°C

Table 10 Ordering information

4.6 Top marking




```
MT7905DAN : Part number
DDDD      : Date code
####      : Internal control code
BBBBBBB   : Lot number
```

Figure 7 MT7905DAN Top Marking

ESD CAUTION

MT7905DAN is ESD (electrostatic discharge) sensitive device and may be damaged with ESD or spike voltage. Although MT7905DAN is with built-in ESD protection circuitry, please handle with care to avoid the permanent malfunction or the performance degradation.