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MT7620
Format V1.7

Update history

Version	Date	Description	Modified by
1.0	2012/03/01	Initial version	Kim
1.1	2012/08/13	Modify TX power compensation, and data rate offset format.	Kim
1.2	2012/10/02	Modify TX power compensation of TSSI and temperature	Kim
1.3	2012/11/01	To correct TX0/1 power setting, the1 step=0.5dBm.	Kim
1.4	2012/11/06	1.Tx Power Compensation Parameter, 0x76h and 0x77 default setting are 0x00 2. TX rate power configuration (DEh~EFh) table without single sku table.	Kim
1.5	2012/11/14	Add 0x42 bit 15 to decide PA mode value: 0: set PA mode=0 for all mode 1: Keep original value(default setting)	Kim
1.6	2012/11/19	1. Add Temperature sensor -- 25°C Reference code D0h[15:8]. 2. Add 0x42h[11] 25CTemper calibration value disable bit. 3. Modify Temperature power compensation 0x6E~0x7E table.	Kim
1.7	2013/01/03	1. Modify Temperature power compensation 0x76~0x77 table. 2. Modify 20M/40M BW Power Delta (0x50h) step from 1dBm to 0.5dBm	Kim

Contents

1. General Description

This Document specify every field for MT7620 EEPROM layout.

There are application usage for MT7620, the other is as an intelligent NIC(iNIC). The EEPROM definition will be different for these two applications.

2. RT7620 EEPROM Layout

2.1 EEPROM for iNIC application

Offset	Default (hex)	b15 ~b8	b7 ~ b0
00h	7620	Chip ID	
02h	0000	EEPROM Version	
04h		WLAN Mac Address [47:32]	
06h		WLAN Mac Address [31:16]	
08h		WLAN Mac Address [15:0]	
0Ah	7620	USB Device ID	
0Ch	148F	USB Vender ID (148Fh for Ralink)	
0Eh	FFFF	**Reserved**	
10h	FFFF	**Reserved**	
12h	FFFF	**Reserved**	
14h	FFFF	**Reserved**	
16h	FFFF	**Reserved**	**Reserved**
18h	FFFF	**Reserved**	
1Ah	FFFF	Magic number of DRAM setting (0x5a)	DRAM setting
1Ch	FFFF	Reserved	
1Eh	FFFF	Reserved	
20h	FFFF	Reserved	
22h	FFFF	Reserved	
24h	FFFF	Low half word of Magic number (0x5244)	
26h	FFFF	High half word of Magic number (0x4D41)	
28h	FFFF	[SDR] Low half word of SDRAM CFG0	
		[DDR] DDR_CFG3 ODT	[DDR] SYSCFG1[25:20]
2Ah	FFFF	[SDR] High half word of SDRAM CFG0	
		Reserved	
2Ch	FFFF	[SDR] Low half word of SDRAM CFG1	
		Reserved	
2Eh	FFFF	[SDR] High half word of SDRAM CFG1	
		Reserved	
30h	FFFF	Source Address of in-band frame (0 for 00:0c:43:00:00:00) (FFFF for broadcast address)	

Offset		Default (hex)	b15 ~b8	b7 ~ b0
32h		FFFF	Protocol of in-band frame	
34h		FFFF	NIC Configuration 0	
36h		FFFF	NIC Configuration 1	
38h		FFFF	Country Region 2.4G band	**Reserved**
3Ah		FFFF	LED Mode	Frequency offset
3Ch		FFFF	Reserved	
3Eh		FFFF	LED ACT Configuration	
40h		FFFF	LED ACT Polarity	
42h		FFFF	NIC Configuration 2, bit 11 25CTemper calibration value disable bit.	
44h		FFFF	**Reserved**	External LNA gain for 2.4G Band
46h		0000	2.4G RSSI1 offset	2.4G RSSI0 offset
48h		0000	**Reserved**	Reserved
4Ah		0000	**Reserved**	**Reserved**
4Ch		0000	**Reserved**	**Reserved**
4Eh		FFFF	**Reserved**	**Reserved**
50h		FFFF	**Reserved**	20M/40M BW Power delta for 2.4G band
52h		FFFF	Channel 2 TX0 power	Channel 1 TX0 power
54h		FFFF	Channel 4 TX0 power	Channel 3 TX0 power
56h		FFFF	Channel 6 TX0 power	Channel 5 TX0 power
58h		FFFF	Channel 8 TX0 power	Channel 7 TX0 power
5Ah		FFFF	Channel 10 TX0 power	Channel 9 TX0 power
5Ch		FFFF	Channel 12 TX0 power	Channel 11 TX0 power
5Eh		FFFF	Channel 14 TX0 power	Channel 13 TX0 power
60h		FFFF	Channel 2 TX1power	Channel 1 TX1 power
62h		FFFF	Channel 4 TX1 power	Channel 3 TX1 power
64h		FFFF	Channel 6 TX1 power	Channel 5 TX1 power
66h		FFFF	Channel 8 TX1 power	Channel 7 TX1 power
68h		FFFF	Channel 10 TX1 power	Channel 9 TX1 power
6Ah		FFFF	Channel 12 TX1 power	Channel 11 TX1 power
6Ch		FFFF	Channel 14 TX1 power	Channel 13 TX1 power
6Eh	TSSI	FFFF	TSSI offset for Ant 0, 2.4G group 1 (channel 1~4)	TSSI slope for ant0
	Temper	FFFF	2.4G TX power –6 boundary	2.4G TX power –7 boundary
70h	TSSI	FFFF	TSSI offset for Ant 0, 2.4G group 3 (channel 9~14)	TSSI offset for Ant 0, 2.4G group 2 (channel 5~8)
	Temper	FFFF	2.4G TX power –4 boundary	2.4G TX power –5 boundary

Offset		Default (hex)	b15 ~b8	b7 ~ b0
72h	TSSI	FFFF	TSSI offset for Ant 1, 2.4G group 1 (channel 1~4)	TSSI slope for ant1
	Temper	FFFF	2.4G TX power –2 boundary	2.4G TX power –3 boundary
74h	TSSI	FFFF	TSSI offset for Ant 1, 2.4G group 3 (channel 9~14)	TSSI offset for Ant 1, 2.4G group 2 (channel 5~8)
	Temper	FFFF	2.4G TX power –0 boundary	2.4G TX power –1 boundary
76h	TSSI	0000	Ant1 TSSI offset(0.125 dB)	Ant0 TSSI offset(0.125 dB)
	Temper	FFFF	2.4G reference temp	2.4G reference step
78h	Temper	FFFF	2.4G TX power +2 boundary	2.4G TX power +1 boundary
7Ah	Temper	FFFF	2.4G TX power +4 boundary	2.4G TX power +3 boundary
7Ch	Temper	FFFF	2.4G TX power +6 boundary	2.4G TX power +5 boundary
7Eh	Temper	FFFF	**Reserved**	2.4G TX power +7 boundary
80h		FFFF	**Reserved**	**Reserved**
82h		FFFF	**Reserved**	**Reserved**
84h		FFFF	**Reserved**	**Reserved**
86h		FFFF	**Reserved**	**Reserved**
88h		FFFF	**Reserved**	**Reserved**
8Ah		FFFF	**Reserved**	**Reserved**
8Ch		FFFF	**Reserved**	**Reserved**
8Eh		FFFF	**Reserved**	**Reserved**
90h		FFFF	**Reserved**	**Reserved**
92h		FFFF	**Reserved**	**Reserved**
94h		FFFF	**Reserved**	**Reserved**
96h		FFFF	**Reserved**	**Reserved**
98h		FFFF	**Reserved**	**Reserved**
9Ah		FFFF	Reserved	**Reserved**
9Ch		FFFF	Reserved	Reserved
9Eh		FFFF	Reserved	Reserved
A0h		FFFF	Reserved	Reserved
A2h		FFFF	Reserved	Reserved
A4h		FFFF	Reserved	Reserved
A6h		FFFF	**Reserved**	**Reserved**
A8h		FFFF	**Reserved**	**Reserved**
AAh		FFFF	**Reserved**	**Reserved**
ACh		FFFF	**Reserved**	**Reserved**
AEh		FFFF	**Reserved**	**Reserved**
B0h		FFFF	**Reserved**	**Reserved**

Offset	Default (hex)	b15 ~b8	b7 ~ b0
B2h	FFFF	**Reserved**	**Reserved**
B4h	FFFF	**Reserved**	**Reserved**
B6h	FFFF	**Reserved**	**Reserved**
B8h	FFFF	**Reserved**	**Reserved**
BAh	FFFF	**Reserved**	**Reserved**
BCh	FFFF	**Reserved**	**Reserved**
BEh	FFFF	**Reserved**	**Reserved**
C0h	FFFF	**Reserved**	**Reserved**
C2h	FFFF	**Reserved**	**Reserved**
C4h	FFFF	**Reserved**	**Reserved**
C6h	FFFF	**Reserved**	**Reserved**
C8h	FFFF	Reserved	**Reserved**
CAh	FFFF	Reserved	Reserved
CCh	FFFF	Reserved	Reserved
CEh	FFFF	Reserved	Reserved
D0h	801E	Temperature sensor -- 25°C Reference code	OFDM 54 M target power for 2.4GHz
D2h	FFFF	Reserved	Reserved
D4h	FFFF	**Reserved**	**Reserved**
D6h	FFFF	**Reserved**	**Reserved**
D8h	FFFF	**Reserved**	**Reserved**
DAh	FFFF	**Reserved**	**Reserved**
DCh	FFFF	**Reserved**	**Reserved**
DEh	0808	TX power for CCK 5.5M/11M	TX power for CCK 1M/2M
E0h	0808	TX power for OFDM 12M/18M	TX power for OFDM 6M/9M
E2h	0004	TX power for OFDM 48M/54M	TX power for OFDM 24M/36M
E4h	0707	TX power for HT MCS=2,3	TX power for HT MCS=0,1
E6h	0004	TX power for HT MCS=6,7	TX power for HT MCS=4,5
E8h	0808	TX power for HT MCS=10,11	TX power for HT MCS=8,9
EAh	0004	TX power for HT MCS=14,15	TX power for HT MCS=12,13
ECh	0707	TX power for STBC MCS=2,3	TX power for STBC MCS=0,1
EEh	0004	TX power for STBC MCS=6,7	TX power for STBC MCS=4,5
F0h	FFFF	Reserved	Reserved
F2h	FFFF	Reserved	Reserved
F4h	FFFF	Reserved	Reserved
F6h	FFFF	Reserved	Reserved
F8h	FFFF	Reserved	Reserved

Offset	Default (hex)	b15 ~b8	b7 ~ b0
FAh	FFFF	Reserved	Reserved
FCh	FFFF	Reserved	Reserved
FEh	FFFF	Reserved	Reserved
….	….	….	….

2.2 EEPROM for Standalone router application

Offset	Default (hex)	b15 ~b8	b7 ~ b0
00h	7620	Chip ID	
02h	0000	EEPROM Version	
04h		WLAN Mac Address [47:32]	
06h		WLAN Mac Address [31:16]	
08h		WLAN Mac Address [15:0]	
0Ah	FFFF	**Reserved**	
0Ch	FFFF	**Reserved**	
0Eh	FFFF	**Reserved**	
10h	FFFF	**Reserved**	
12h	FFFF	**Reserved**	
14h	FFFF	**Reserved**	
16h	FFFF	**Reserved**	**Reserved**
18h	FFFF	**Reserved**	
1Ah	FFFF	**Reserved**	
1Ch	FFFF	**Reserved**	
1Eh	FFFF	Reserved	
20h	FFFF	Reserved	
22h	FFFF	Reserved	
24h	FFFF	Reserved	
26h	FFFF	Reserved	
28h		MAC0 MAC address [47:32]	
2Ah		MAC0 MAC address [31:16]	
2Ch		MAC0 MAC address [15:0]	
2Eh		MAC1 MAC address [47:32]	
30h		MAC1 MAC address [31:16]	
32h		MAC1 MAC address [15:0]	
34h	FFFF	NIC Configuration 0	
36h	FFFF	NIC Configuration 1	
38h	FFFF	Country Region 2.4G band	**Reserved**
3Ah	FFFF	LED Mode	Frequency offset
3Ch	FFFF	Reserved	
3Eh	FFFF	LED ACT Configuration	
40h	FFFF	LED ACT Polarity	
42h	FFFF	NIC Configuration 2, bit 11 25CTemper calibration value disable bit.	
44h	FFFF	**Reserved**	External LNA gain for 2.4G Band

Offset		Default (hex)	b15 ~b8	b7 ~ b0
46h		0000	2.4G RSSI1 offset	2.4G RSSI0 offset
48h		0000	**Reserved**	2.4G RSSI2 offset
4Ah		0000	**Reserved**	**Reserved**
4Ch		0000	**Reserved**	**Reserved**
4Eh		FFFF	**Reserved**	**Reserved**
50h		FFFF	**Reserved**	20M/40M BW Power delta for 2.4G band
52h		FFFF	Channel 2 TX0 power	Channel 1 TX0 power
54h		FFFF	Channel 4 TX0 power	Channel 3 TX0 power
56h		FFFF	Channel 6 TX0 power	Channel 5 TX0 power
58h		FFFF	Channel 8 TX0 power	Channel 7 TX0 power
5Ah		FFFF	Channel 10 TX0 power	Channel 9 TX0 power
5Ch		FFFF	Channel 12 TX0 power	Channel 11 TX0 power
5Eh		FFFF	Channel 14 TX0 power	Channel 13 TX0 power
60h		FFFF	Channel 2 TX1power	Channel 1 TX1 power
62h		FFFF	Channel 4 TX1 power	Channel 3 TX1 power
64h		FFFF	Channel 6 TX1 power	Channel 5 TX1 power
66h		FFFF	Channel 8 TX1 power	Channel 7 TX1 power
68h		FFFF	Channel 10 TX1 power	Channel 9 TX1 power
6Ah		FFFF	Channel 12 TX1 power	Channel 11 TX1 power
6Ch		FFFF	Channel 14 TX1 power	Channel 13 TX1 power
6Eh	TSSI	FFFF	TSSI offset for Ant 0, 2.4G group 1 (channel 1~4)	TSSI slope for ant0
	Temper	FFFF	2.4G TX power –6 boundary	2.4G TX power –7 boundary
70h	TSSI	FFFF	TSSI offset for Ant 0, 2.4G group 3 (channel 9~14)	TSSI offset for Ant 0, 2.4G group 2 (channel 5~8)
	Temper	FFFF	2.4G TX power –4 boundary	2.4G TX power –5 boundary
72h	TSSI	FFFF	TSSI offset for Ant 1, 2.4G group 1 (channel 1~4)	TSSI slope for ant1
	Temper	FFFF	2.4G TX power –2 boundary	2.4G TX power –3 boundary
74h	TSSI	FFFF	TSSI offset for Ant 1, 2.4G group 3 (channel 9~14)	TSSI offset for Ant 1, 2.4G group 2 (channel 5~8)
	Temper	FFFF	2.4G TX power –0 boundary	2.4G TX power –1 boundary
76h	TSSI	FFFF	Ant1 TSSI offset(0.125 dB)	Ant0 TSSI offset(0.125 dB)
	Temper	FFFF	2.4G reference temp	2.4G reference step
78h	Temper	FFFF	2.4G TX power +2 boundary	2.4G TX power +1 boundary
7Ah	Temper	FFFF	2.4G TX power +4 boundary	2.4G TX power +3 boundary
7Ch	Temper	FFFF	2.4G TX power +6 boundary	2.4G TX power +5 boundary
7Eh	Temper	FFFF	**Reserved**	2.4G TX power +7 boundary
80h		FFFF	**Reserved**	**Reserved**

Offset	Default (hex)	b15 ~b8	b7 ~ b0
82h	FFFF	**Reserved**	**Reserved**
84h	FFFF	**Reserved**	**Reserved**
86h	FFFF	**Reserved**	**Reserved**
88h	FFFF	**Reserved**	**Reserved**
8Ah	FFFF	**Reserved**	**Reserved**
8Ch	FFFF	**Reserved**	**Reserved**
8Eh	FFFF	**Reserved**	**Reserved**
90h	FFFF	**Reserved**	**Reserved**
92h	FFFF	**Reserved**	**Reserved**
94h	FFFF	**Reserved**	**Reserved**
96h	FFFF	**Reserved**	**Reserved**
98h	FFFF	**Reserved**	**Reserved**
9Ah	FFFF	**Reserved**	**Reserved**
9Ch	FFFF	**Reserved**	**Reserved**
9Eh	FFFF	**Reserved**	**Reserved**
A0h	FFFF	**Reserved**	**Reserved**
A2h	FFFF	**Reserved**	**Reserved**
A4h	FFFF	**Reserved**	**Reserved**
A6h	FFFF	**Reserved**	**Reserved**
A8h	FFFF	**Reserved**	**Reserved**
AAh	FFFF	**Reserved**	**Reserved**
ACh	FFFF	**Reserved**	**Reserved**
AEh	FFFF	**Reserved**	**Reserved**
B0h	FFFF	**Reserved**	**Reserved**
B2h	FFFF	**Reserved**	**Reserved**
B4h	FFFF	**Reserved**	**Reserved**
B6h	FFFF	**Reserved**	**Reserved**
B8h	FFFF	**Reserved**	**Reserved**
BAh	FFFF	**Reserved**	**Reserved**
BCh	FFFF	**Reserved**	**Reserved**
BEh	FFFF	**Reserved**	**Reserved**
C0h	FFFF	**Reserved**	**Reserved**
C2h	FFFF	**Reserved**	**Reserved**
C4h	FFFF	**Reserved**	**Reserved**
C6h	FFFF	**Reserved**	**Reserved**
C8h	FFFF	**Reserved**	**Reserved**

Offset	Default (hex)	b15 ~b8	b7 ~ b0
CAh	FFFF	**Reserved**	**Reserved**
CCh	FFFF	**Reserved**	**Reserved**
CEh	FFFF	**Reserved**	**Reserved**
D0h	801E	Temperature sensor -- 25°C Reference code	OFDM 54 M target power for 2.4GHz
D2h	FFFF	**Reserved**	**Reserved**
D4h	FFFF	**Reserved**	**Reserved**
D6h	FFFF	**Reserved**	**Reserved**
D8h	FFFF	**Reserved**	**Reserved**
DAh	FFFF	**Reserved**	**Reserved**
DCh	FFFF	**Reserved**	**Reserved**
DEh	0808	TX power for CCK 5.5M/11M	TX power for CCK 1M/2M
E0h	0808	TX power for OFDM 12M/18M	TX power for OFDM 6M/9M
E2h	0004	TX power for OFDM 48M/54M	TX power for OFDM 24M/36M
E4h	0707	TX power for HT MCS=2,3	TX power for HT MCS=0,1
E6h	0004	TX power for HT MCS=6,7	TX power for HT MCS=4,5
E8h	0808	TX power for HT MCS=10,11	TX power for HT MCS=8,9
EAh	0004	TX power for HT MCS=14,15	TX power for HT MCS=12,13
ECh	0707	TX power for STBC MCS=2,3	TX power for STBC MCS=0,1
EEh	0004	TX power for STBC MCS=6,7	TX power for STBC MCS=4,5
F0h	FFFF	Reserved	Reserved
F2h	FFFF	Reserved	Reserved
F4h	FFFF	Reserved	Reserved
F6h	FFFF	Reserved	Reserved
F8h	FFFF	Reserved	Reserved
FAh	FFFF	Reserved	Reserved
FCh	FFFF	Reserved	Reserved
FEh	FFFF	Reserved	Reserved
…	…	…	…

3. EEPROM Contents

3.1 E2PROM layout version # (02h)

Offset	Value	Description
02h	0	Version 0.
	1 ~ 255	Invalid version. Treat as version 0.

3.2 ASIC Boot-Rom Config(1Ah ~ 33h)

3.2.1 RT3x5x reserved fields for RGMII device mode (iNIC)

Offset	Default (hex)	b15 ~b8	b7 ~ b0
1Ah	FFFF	Magic number of DRAM setting (0x5a)	DRAM Setting
1Ch	FFFF	Reserved	
1Eh	FFFF	Reserved	
20h	FFFF	Reserved	
22h	FFFF	Reserved	
24h	FFFF	Low half word of Magic number (0x5244)	
26h	FFFF	High half word of Magic number (0x4D41)	
28h	FFFF	[SDR] Low half word of SDRAM CFG0	
		[DDR] DDR_CFG3 ODT	[DDR] SYSCFG1[25:20]
2Ah	FFFF	[SDR] High half word of SDRAM CFG0	
2Ch	FFFF	[SDR] Low half word of SDRAM CFG1	
2Eh	FFFF	[SDR] High half word of SDRAM CFG1	
30h	FFFF	Source Address of in-band frame (0 for 00:0c:43:00:00:00) (FFFF for broadcast address)	
32h	FFFF	Protocol of in-band frame	

For iNIC, there are two interface to be used between MT7620 and the main system(main CPU), one is through USB interface(or said “boot from USB”), the other is through MII(or said “boot from MII”). Fields 0x24 ~ 0x32 is the same definition for both interface, fields 0x1e ~ 0x22 is only used for MII interface.

For MII interface, there are MDIO_CFG setting to be set before boot-up, if MDIO_CFG need to be configured, field 0x1e shield be written as the magic number 0xA96b, and MDIO_CFG should be written to 0x20 ~ 0x22.

For both interface(no matter boot from PCI or MII), fields 0x24 ~ 0x26 is the magic number for iNIC bootrom, if the magic number is correctly configured(written 0x5244 and 0x4d41), then

If the System configuration register bit 28(INIC_EE_SDRAM) is 1, then iNIC bootrom will read 0x28 ~ 0x2A, and use it’s value for SDRAM_CFG0, and also read 0x2C ~ 0x2E, and use it’s value for SDRAM_CFG1. If

INIC_EE_SDRAM bit is 0, 0x28 ~ 0x2E is ignored.

If 0x30 is default value 0xFFFF, the bootrom will send bootstap frames using broadcast address as source address, if it's value is 0x0, it will use source address 00:0c:43:00:00:00

If 0x32 is default value 0xFFFF, then the Ethernet protocol filed for bootstrap frame will be 0xFFFF, and if it is other value, the Ethernet protocol will be that value.

3.2.2 DRAM setting (0x1A)

Offset	Field	Description
1Ah	0	**DRAM_WIDTH(one dram cell)** DRAM(DDR) 0: 16 (8) 1: 32 (16)
	3:1	**DRAM_SIZE(one dram cell)** 0: 2MB 1: 8MB 2: 16MB 3: 32MB 4: 64MB 5: 128MB 6: 256MB
	4	**DRAM_TOTAL_WIDTH** 0: 16 1: 32
	5	**DRAM_TYPE** 0: SDRAM 1: DDR
	7:6	**reserved**

3.2.3 [DDR] SYSCFG1[25:20] (0x28)

Offset	Field	Description
28h	5:0	**SYSCFG1[25:20]**
	7:6	**reserved**

3.2.4 [DDR] DDR_CFG3 ODT (0x29)

Offset	Field	Description
29h	0	**DDR_CFG3[2]**
	1	**DDR_CFG3[6]**
	7:2	**reserved**

3.2.5 RT305x reserved fields for standalone router

Offset	Default (hex)	b15 ~b8	b7 ~ b0
1Eh	FFFF	reserved	
20h	FFFF	reserved	
22h	FFFF	reserved	
24h	FFFF	reserved	

Offset	Default (hex)	b15 ~b8	b7 ~ b0
26h	FFFF	reserved	
28h		MAC0 MAC address [15:0]	
2Ah		MAC0 MAC address [31:16]	
2Ch		MAC0 MAC address [47:32]	
2Eh		MAC1 MAC address [15:0]	
30h		MAC1 MAC address [31:16]	
32h		MAC1 MAC address [47:32]	

3.3 NIC Configuration 0 (0x34)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				RFIC Type				TX Path setting				RX Path setting			
Reserved								1: 1TX 2: 2TX				1: 1RX 2: 2RX			

NIC Configuration 0 Register Bit Fields Description

Offset	Field	Description
34h	3:0	These fields are to provide the RX front-end architecture in the system. 0 (0000): Reserved. 1 (0001): 1 RX front-end in the system. 2 (0010): 2 RX front-end in the system. 3 ~ F (0011 ~ 1111): Reserved.
	7:4	These fields are to provide the TX front-end architecture in the system. 0 (0000): Reserved. 1 (0001): 1 TX front-end in the system. 2 (0010): 2 TX front-end in the system. 3 ~ F (0011 ~ 1111): Reserved.
35h	11:8	
	15:12	Reserved.

3.4 NIC Configuration 1 (0x36)

Bit[7:0] = 0xFF will be treated as INVALID and used Default Value
Bit[15:8] = 0xFF will be treated as INVALID and used Default Value

7	6	5	4	3	2	1	0
WPS PBC	**Reserved**	2.4G side band for 40M BW	Proprietary Test bit	**Reserved**	EXT LNA 2.4G	External TX ALC	**Reserved**
0: off (D) 1: on		0: off(D) 1: on	0: off(D) 1: on		0: off(D) 1: on	0: off(D) 1: on	

15 ~ 14	13	12	11	10	9	8
PA Setting<TX1:TX0>	Internal TX ALC	Reserved	Reserved	Broadband EXT LNA	**Reserved**	40M BW in 2.4G band
0: internal PA 1: external PA	0: off(D) 1: on			0: off 1: on		0: on (D) 1: off

NIC Configuration 1 Register Bit Fields Description

Offset	Field	Definition	Description	
36h	0	Reserved	Reserve.	
	1	External TX ALC	The default value is 0. When the TX auto-level-calibration control is enabled (=1), the driver will automatic compensate TX power varied due to temperature variation.	
			0	Default value. Disable TX auto-level-calibration control.
			1	Enable TX auto-level-calibration control.
	2	External LNA for 11g (2.4 GHz) band	0	Board without external LNA must set this bit to 0.
			1	Default value. Board with external LNA.
	3	**Reserved**	**Reserved**	
	4	Proprietary TEST BIT#1	For debug purpose.	
	5	2.4G side band for 40M BW	For debug purpose.	
	6	**Reserved**	**Reserved**	
	7	WPS PBC	WPS Push Button Configuration control.	
			0	OFF: Disable WPS PBC function.
			1	ON: Enable WPS PBC function,
37h	8	40M BW in 2.4G	0	Enable 11g 40M bandwidth.

Offset	Field	Definition	Description	
		band	1	Disable 11g 40M bandwidth.
	9	**Reserved**	**Reserved**	
	10	Broadband EXT LNA	0	Board without external LNA must set this bit to 0.
			1	Board with external LNA must set this bit to 1.
	11	**Reserved**	**Reserved**	
	12	Reserved	Reserved	
	13	Internal TX ALC	Internal TX auto level control 0: disable internal TX ALC function (default value). 1: enable internal TX ALC function When the internal TX ALC function is enabled (=1), the driver will use the internal TX ALC function to automatic compensate TX power varied due to temperature variation. It also needs to fill the register “2.4G internal/external step value (77h)” for the TX ALC function.	
	15:14	PA setting <TX1:TX0>	Select to use internal or external PA 00: internal PA for TX0 &TX1 01: internal PA for TX1, external PA for TX0 10: internal PA for TX0, external PA for TX1 11: external PA for TX0 &TX1	

3.5 NIC Configuration 2 (0x42)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				25CTemper calibration value disable bit. 0: Enable(default setting) 1: disable	Reserved			TX Stream 1: 1 Stream 2: 2 Stream				RX Stream 1: 1 Stream 2: 2 Stream			

Note:Need to do temperature calibration, and calibration result will be written into EEPROM 0xD0[15:8].

NIC Configuration 0 Register Bit Fields Description

Offset	Field	Description
42h	3:0	These fields are to define the support RX stream number in the system. 0 (0000): Reserved. 1 (0001): 1 RX stream in the system. 2 (0010): 2 RX streams in the system. 3 ~ F (0011 ~ 1111): Reserved.
	7:4	These fields are to define the support TX stream number in the system. 0 (0000): Reserved. 1 (0001): 1 TX stream in the system. 2 (0010): 2 TX streams in the system. 3 ~ F (0011 ~ 1111): Reserved.
43h	14:8	Reserved.
43h	15	Decide PA mode value: 0: set PA mode=0 for all mode 1: Keep original value(default setting)

Note:

1. Stream vs. data rate.

# Stream	Data rate
1 stream	MCS0~MCS7
2 stream	MCS0~MCS15.

2. Stream setting should be equal or less than front-end path setting (offset 0x34h).
3. Default=0xFF means that based on the front-end path setting (0x34h) for maximum capability.

3.6 Country Region Code for 2.4G band (0x39)

7	6	5	4	3	2	1	0
2.4GHz band country region code							

Default value = FFh, which means read from INF and registry, more flexible than reading from EEPROM, this is our current InstallShield CCS implementation. We do not recommend customers to read SKU from EEPROM. Value FFh is the default value.
CountryCode— Specify the domain code, can be FFh or one of the followings,

Index	Support Channels
0	CH1 – 11
1	CH1 – 13
2	CH10 – 11
3	CH10 – 13
4	CH14
5	CH1 – 14
6	CH3 – 9
7	CH5 – 13

Notes: If set to read SKU from EEPROM, only available if both 5GHz and 2.4GHz Country Region code registers are programmed.

3.7 Frequency offset (0x3A)

7	6	5	4	3	2	1	0
Frequency calibration							

For crystal frequency calibration purpose.

3.8 LED Mode Setting (0x3B)

7	6	5	4	3	2	1	0
GPIO Polarity	LED control modes						

Offset	Field	LED Mode		Description
3Bh	[6:0]	0	HW control	The default mode. Driver sets MAC register and MAC controls LED.
		1	FW default mode	The firmware controls how LED blinks.
		2	8sec scan	Same as LED mode 1 except that fast blink for 8sec when doing scanning.
		3-63	-	Reserved.
		64	Reserved	Reserved.
	7	GPIO Polarity		0: Negative polarity 1: Positive polarity

3.9 LED Configuration: (in EEPROM Byte 3Eh~3Fh)

7	6	5	4	3	2	1	0
Radio on and link down				Radio off			

15	14	13	12	11	10	9	8
Reserved				Radio on and link to G			

Offset	States	Field	RT3052 WLAN_LED behavior
3Eh	Radio off	[1:0]	00: Reserved 01: Solid on 10: Blink when transmitting data and management packet 11: Blink when transmitting data, management packet and beacon
		2	0: Solid on when no traffic 1: Slow blink when no traffic
		3	Reserved
	Radio on but link down	[5:4]	00: Reserved 01: Solid on 10: Blink when transmitting data and management packet 11: Blink when transmitting data, management packet and beacon
		6	0: Solid on when no traffic 1: Slow blink when no traffic
		7	Reserved
3Fh	Radio on and link to G	[9:8]	00: Reserved 01: Solid on 10: Blink when transmitting data and management packet 11: Blink when transmitting data, management packet and beacon
		10	0: Solid on when no traffic 1: Slow blink when no traffic
		11	Reserved
	Reserved	[15:12]	Reserved

3.10 LED Polarity: (in EEPROM Byte 40h~41h)

7	6	5	4	3	2	1	0
Reserved	LED ACT	Reserved	Reserved	Reserved	LED ACT	Reserved	Reserved
Radio on and link down				Radio off			

15	14	13	12	11	10	9	8
Reserved	Reserved	Reserved	Reserved	Reserved	LED ACT	Reserved	Reserved
Reserved				Radio on and link to G			

Offset	States	Field	LED behavior	
40h	Radio off	0	Reserved	1: Positive polarity 0: Negative polarity
		1	Reserved	
		2	LED ACT	
		3	Reserved	Reserved and must be filled as 1.
	Radio on but link down	4	Reserved	1: Positive polarity 0: Negative polarity
		5	Reserved	
		6	LED ACT	
		7	Reserved	Reserved and must be filled as 1.
41h	Radio on and link to G	8	Reserved	1: Positive polarity 0: Negative polarity
		9	Reserved	
		10	LED ACT	
		11	Reserved	Reserved and must be filled as 1.
	Reserved	12	Reserved	Reserved and must be filled as 1.
		13	Reserved	
		14	Reserved	
		15	Reserved	

3.11 External LNA gain for 2.4GHz Band (44h)

External LNA gain for 2.4GHz Band Register Bit Fields Description

Offset	Field	Description
44h	7:0	External LNA gain for 2.4GHz Band. 1 step = 1 dB Example:

Value	LNA gain (dB)
0000 0000	0
0000 0001	1
0000 1010	10

3.12 EIRP TX Power for 2.4GHz band (4Eh) Reserved

The register is intend to limit the TX power for different countries in one SKU.

EIRP TX Power for 2.4GHz band Register Bit Fields Description

Offset	Field	Description
4Eh	7:0	2.4GHz maximum TX power. The register value is the board's EIRP value. The driver will compare the board's EIRP with each country allow TX power automatically if this function is enabled. FF (1111 1111): disable the maximum TX power comparison function. Ex: 08 (0000 1000): Board's EIRP is 8dBm 10 (0001 0000): Board's EIRP is 16dBm 12 (0001 0010): Board's EIRP is 18dBm
4Fh	15:8	Reserved

Example:

If antenna gain is 3dBi, board's maximum TX power is 17dBm. The Equivalent isotropically radiated power (EIRP) is 17+3=20dBm. The value of offset 4Eh is 14 (0001 0100).

Following table is based on the maximum TX power comparison function is enabled.

Country	Allowed TX power of the country (dBm)	Offset 4Eh = 14	Exact maximum EIRP (dBm)
A	20	20	20
B	16	20	16
C	18	20	18
D	23	20	20

Note:

If allowed country power is greater than the TX power setting of offset 4Eh, then the board maximum EIRP is the TX power setting of offset 4Eh.

If allowed country power is less than the TX power setting of offset 4Eh, then the board maximum EIRP is the country's allowed TX power.

3.13 20M/40M BW Power Delta for 2.4GHz band (50h)

This register is for driver compensates the TX power value of 40M BW with the configured delta value.

TX power delta configuration Register Bit Fields Description

Field	Description
5:0	40M BW TX power delta value (MAX=4dBm). 000001: 0.5dBm 000010: 1dBm 000011: 1.5dBm 000100: 2dBm 000101:2.5dBm 000110:3dBm 000111:3.5dBm 001000:4dBm
6	1: increase 40M BW TX power with the delta value. 0: decrease 40M BW TX power with the delta value.
7	1: enable TX power compensation.

Example:

The default calibrated TX power is as followings with the TX power delta configuration is not enabled.

- 40M BW TX power= 14dBm and 20M BW TX power = 14dBm

If want keep 20M BW TX power in 14dBm while to reduce 40M BW TX power to 10dBm (delta=4dBm),

Apply following settings can meet the requirement.

- Set 50h = 88h (1000 1000)

3.14 2.4G band TX0 & TX1 Power (52h~6Dh)

Both the calibrated 2.4GHz TX0 & TX1 power values are saved in these registers.
To prevent reading from EMPTY E2PROM, driver treats these “Channel xx Tx Power” value 0 and any value > =0x20 as invalid. That is, only bit [0..4] in each byte contains valid data, [bit 5..7] MUST be 0.

Offset	b15 ~b8	b7 ~ b0
52h	Channel 2 TX0 power	Channel 1 TX0 power
54h	Channel 4 TX0 power	Channel 3 TX0 power
56h	Channel 6 TX0 power	Channel 5 TX0 power
58h	Channel 8 TX0 power	Channel 7 TX0 power
5Ah	Channel 10 TX0 power	Channel 9 TX0 power
5Ch	Channel 12 TX0 power	Channel 11 TX0 power
5Eh	Channel 14 TX0 power	Channel 13 TX0 power
60h	Channel 2 TX1power	Channel 1 TX1 power
62h	Channel 4 TX1 power	Channel 3 TX1 power
64h	Channel 6 TX1 power	Channel 5 TX1 power
66h	Channel 8 TX1 power	Channel 7 TX1 power
68h	Channel 10 TX1 power	Channel 9 TX1 power
6Ah	Channel 12 TX1 power	Channel 11 TX1 power
6Ch	Channel 14 TX1 power	Channel 13 TX1 power

3.15 Tx Power Compensation Parameter (6Eh ~ 76h)

Driver compares current TSSI value (from BBP R49) with this TSSI reference value as a base to decide if real-time TX power compensation is required. 0xFF will be treated as invalid value. This function is controlled by ‘external TX ALC’ bit in NIC configuration1 bit1 or ‘internal TX ALC ‘ bit in NIC configuration1 bit13. 0x76h and 0x77 default setting are 0x00

6Eh	TSSI offset for Ant 0, 2.4G group 1 (channel 1~4)	TSSI slope for ant0
70h	TSSI offset for Ant 0, 2.4G group 3 (channel 9~14)	TSSI offset for Ant 0, 2.4G group 2 (channel 5~8)
72h	TSSI offset for Ant 1, 2.4G group 1 (channel 1~4)	TSSI slope for ant1
74h	TSSI offset for Ant 1, 2.4G group 3 (channel 9~14)	TSSI offset for Ant 1, 2.4G group 2 (channel 5~8)
76h	Ant1 TSSI offset(0.125 dB)	Ant0 TSSI offset(0.125 dB)

3.16 Temperature Tx ALC definition for 2.4GHz & 5GHz (6Eh ~ 77h)

Temperature Tx ALC will compensate Tx power level based on temperature reading. During calibration, the reference temperature will be stored into EEPROM 0x77 for 2.4G. This function is controlled by ‘Temperature TX ALC ‘ bit in NIC configuration1 bit1.

2.4GHz Tx Power delta Temperature Boundary

	Temperature compensation EEPROM 0x36 bit 1 = 1	
Offset	**B15 ~ b8**	**B7 ~ b0**
6Eh	-6 step number	-7 step number
70h	-4 step number	-5 step number
72h	-2 step number	-3 step number
74h	0 step number	-1 step number
76h	2.4G reference temp	2.4G reference step
78h	+2 step number	+1 step number
7Ah	+4 step number	+3 step number
7Ch	+6 step number	+5 step number
7Eh	Reserved	+7 step number

3.17 OFDM 54 M target power for 2.4GHz (D0h[7:0]) with E3h=0

D0h is OFDM 54 M target power. Unit is 0.5 dBm.
e.g. For target power 16 dBm, set D0h as 0x20

3.18 Temperature sensor -- 25˚C Reference Code (D0h[15:8])

D0h[15:8] is Temperature sensor -- 25˚C Reference code.
The unit is 1.9 degree.

	b15~b8	b7~b0
D0h	Temperature sensor -- 25˚C Reference Code	OFDM 54M target Power for 2.4 GHz(E2 b15~b8 = 0)

Note: that is depend on 0x42[11] to enable this function.

3.19 TX rate power configuration (DEh~EFh)

The default value=0x00, Bit [5:0] for TX0/1 power setting
The 1 step=0.5dBm.

Offset	Default Value	Description	Bit [5:0]
DEh	08	TX0/1 power for CCK 1M/2M	TX power setting
DFh	08	TX0/1 power for CCK 5.5M/11M	TX power setting
E0h	08	TX0/1 power for OFDM 6M/9M	TX power setting
E1h	08	TX0/1 power for OFDM 12M/18M	TX power setting
E2h	04	TX0/1 power for OFDM 24M/36M	TX power setting
E3h	00	TX0/1 power for OFDM 48M/54M	TX power setting
E4h	07	TX0/1 power for HT MCS=0,1	TX power setting
E5h	07	TX0/1 power for HT MCS=2,3	TX power setting
E6h	04	TX0/1 power for HT MCS=4,5	TX power setting
E7h	00	TX0/1 power for HT MCS=6,7	TX power setting
E8h	08	TX0/1 power for HT MCS=8,9	TX power setting
E9h	08	TX0/1 power for HT MCS=10,11	TX power setting
EAh	04	TX0/1 power for HT MCS=12,13	TX power setting
EBh	00	TX0/1 power for HT MCS=14,15	TX power setting
ECh	07	TX0/1 power for STBC MCS=0,1	TX power setting
EDh	07	TX0/1 power for STBC MCS=2,3	TX power setting
EEh	04	TX0/1 power for STBC MCS=4,5	TX power setting
EFh	00	TX0/1 power for STBC MCS=6,7	TX power setting

Note:

1. CCK mode power base lower 1dB than OFDM.
2. MCS 0~3 power base higher 0.5dB than MCS4~7.

3.20 Serial Number for Customer (110h ~ 117h)