

# Lab Report #3

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## ① Introduction

In this lab, I implement a SingalCycleCPU by using the components designed in previous lab and test it.

First, we need to connect each data path. I use the figure given by the file "assignment3.pdf" to implement a SingalCycleCPU. Figure 1 is the SingalCycle ARM for lab3.

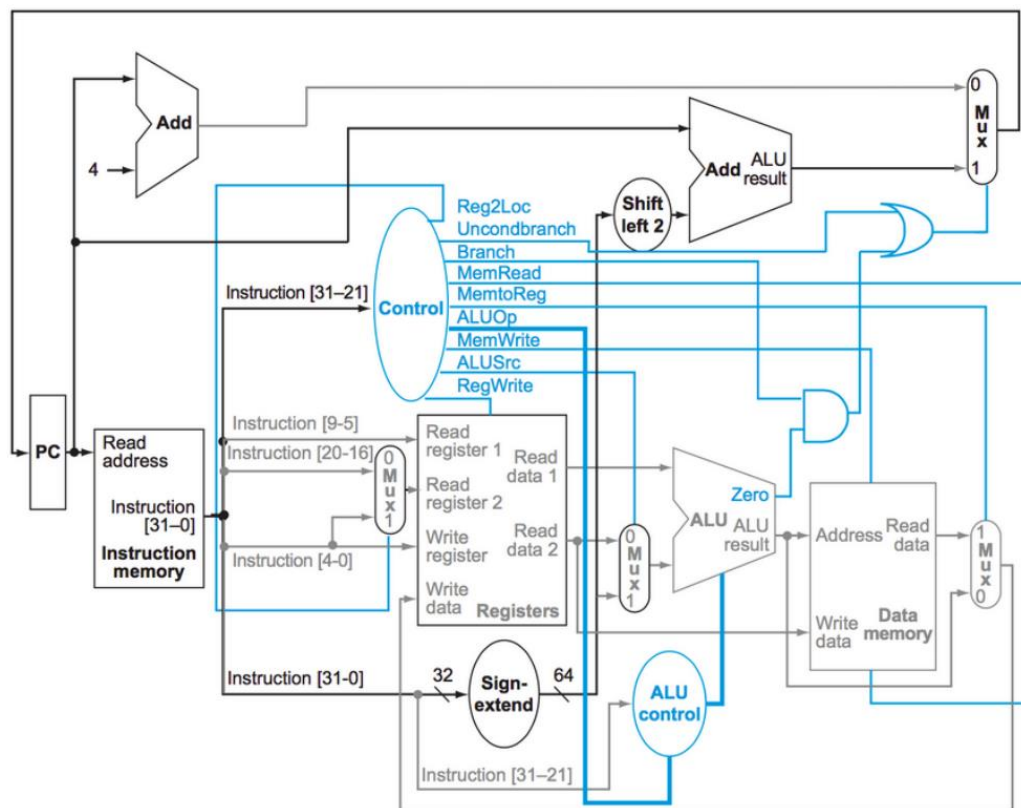


Figure 1: **Single cycle ARM (LEGv8) processor for Lab3.** This is Figure 4-23 in the textbook.

In order to wire different component, we need to create different signals. Below are signal I create.

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Ln#
161 end component;
162 signal MUX64_out_PC : std_logic_vector(63 downto 0);
163 signal MUX64_out_ALU : std_logic_vector(63 downto 0);
164 signal MUX64_out_WD : std_logic_vector(63 downto 0);
165 signal MUX5_out : std_logic_vector(4 downto 0);
166 signal PC_out : std_logic_vector(63 downto 0);
167 signal add_out_PC : std_logic_vector(63 downto 0);
168 signal IMEM_out : std_logic_vector(31 downto 0);
169 signal ReadData01_out : std_logic_vector(63 downto 0);
170 signal ReadData02_out : std_logic_vector(63 downto 0);
171 signal SignExtend_out : std_logic_vector(63 downto 0);
172 signal Shiftleft2_out : std_logic_vector(63 downto 0);
173 signal add_out_shiftleft2 : std_logic_vector(63 downto 0);
174 signal ALU_result : std_logic_vector(63 downto 0);
175 signal ALU_zero : STD_LOGIC;
176 signal ALUControl_out : std_logic_vector(3 downto 0);
177 signal DMEM_out : std_logic_vector(63 downto 0);
178 signal Reg2Loc : STD_LOGIC;
179 signal RegWrite : STD_LOGIC;
180 signal ALUSrc : STD_LOGIC;
181 signal CBranch : STD_LOGIC;
182 signal UBranch : STD_LOGIC;
183 signal ALUOp : std_logic_vector(1 downto 0);
184 signal MemWrite : STD_LOGIC;
185 signal MemRead : STD_LOGIC;
186 signal MemtoReg : STD_LOGIC;
187 signal OR2_out : STD_LOGIC;
188 signal AND2_out : STD_LOGIC;
189 signal DEBUG_TMP_REGS_out : STD_LOGIC_VECTOR(64*4 - 1 downto 0);
190 signal DEBUG_SAVED_REGS_out : STD_LOGIC_VECTOR(64*4 - 1 downto 0);
191 signal DEBUG_MEM_CONTENTS_out : STD_LOGIC_VECTOR(64*4 - 1 downto 0);
192

```

## ② Introduction

However, in the lab3 we cannot simply wire each component. Because before lab3, we create components under simple condition which cannot be directly used for lab3. We need to add some new functionality for some components.

First of all, we need to change the ALU control and CPU control to generate new operation code for the instructions which are not used in the previous lab. For example, I-type, D-type and CBZ instructions.

This is my CPU control for lab3:

```

E:\Modelsim\ee126\lab3\cpucontrol.vhd - Default
Ln#
1  LIBRARY IEEE;
2  USE IEEE.STD_LOGIC_1164.ALL;
3  use IEEE.STD_LOGIC_UNSIGNED.ALL;
4  entity CPUControl is
5  -- Functionality should match the truth table shown in Figure 4.22 of the textbook, including the
6  -- output 'X' values.
7  -- The truth table in Figure 4.22 omits the unconditional branch instruction:
8  -- UBranch = '1'
9  -- MemWrite = RegWrite = '0'
10 -- all other outputs = 'X'
11 port (Opcode : in STD_LOGIC_VECTOR(10 downto 0);
12       Reg2Loc : out STD_LOGIC;
13       CBranch : out STD_LOGIC; --conditional
14       MemRead : out STD_LOGIC;
15       MemtoReg : out STD_LOGIC;
16       MemWrite : out STD_LOGIC;
17       ALUSrc : out STD_LOGIC;
18       RegWrite : out STD_LOGIC;
19       UBranch : out STD_LOGIC; -- This is unconditional
20       ALUOp : out STD_LOGIC_VECTOR(1 downto 0)
21 );
22 end CPUControl;
23
24 ARCHITECTURE Behav1 OF CPUControl IS
25 BEGIN
26     PROCESS (opcode)
27     BEGIN
28         regWrite <= '0';

```

```
E:/Modelism/ee126/lab3/cpucontrol.vhd - Default
Ln#
29  if (Opcode(10 downto 5) = "000101") then
30      Reg2Loc  <= 'X';
31      CBranch  <= 'X';
32      MemRead  <= 'X';
33      MemtoReg <= 'X';
34      MemWrite <= '0';
35      ALUSrc   <= 'X';
36      RegWrite <= '0';
37      UBranch  <= '1';
38      ALUOp    <= "XX";
39
40      ELSif (Opcode(10 downto 0) = "11111000010") then
41          Reg2Loc  <= 'X';
42          CBranch  <= '0';
43          MemRead  <= '1';
44          MemtoReg <= '1';
45          MemWrite <= '0';
46          ALUSrc   <= '1';
47          RegWrite <= '1';
48          UBranch  <= '0';
49          ALUOp    <= "00";
50      ELSif (Opcode(10 downto 0) = "11111000000") then
51          Reg2Loc  <= '1';
52          CBranch  <= '0';
53          MemRead  <= '0';
54          MemtoReg <= 'X';
55          MemWrite <= '1';
56          ALUSrc   <= '1';
57          RegWrite <= '0';
58          UBranch  <= '0';
59          ALUOp    <= "00";
60
61      ELSif (Opcode(10 downto 3) = "10110100") then
62          Reg2Loc  <= '1';
63          CBranch  <= '1';
64          MemRead  <= '0';
65          MemtoReg <= 'X';
66          MemWrite <= '0';
67          ALUSrc   <= '0';
68          RegWrite <= '0';
69          UBranch  <= '0';
70          ALUOp    <= "01";
71      ELSif (Opcode(10 downto 3) = "10110101") then
72          Reg2Loc  <= '1';
73          CBranch  <= '1';
74          MemRead  <= '0';
75          MemtoReg <= 'X';
76          MemWrite <= '0';
77          ALUSrc   <= '0';
78          RegWrite <= '0';
79          UBranch  <= '0';
80          ALUOp    <= "01";
81      ELSif (Opcode(10) = '1' AND Opcode(7 downto 4) = "0101" and Opcode(2 downto 0) = "000") then
82          Reg2Loc  <= '0';
83          CBranch  <= '0';
84          MemRead  <= '0';
85          MemtoReg <= '0';
86          MemWrite <= '0';
87          ALUSrc   <= '0';
88          RegWrite <= '1';
89          UBranch  <= '0';
90          ALUOp    <= "10";
```

```

Ln#
90  ELSif(Opcod(10)='1' AND Opcod(7 downto 5)="100" and Opcod(2 downto 1) ="00")then
91      Reg2Loc <='0';
92      CBranch <='0';
93      MemRead <='0';
94      MemtoReg <='0';
95      MemWrite <='0';
96      ALUSrc <='1';
97      RegWrite <='1';
98      UBranch <='0';
99      ALUOp <="10";
100  ELSif(Opcod(10 downto 2) ="110100110") then
101      Reg2Loc <='0';
102      CBranch <='0';
103      MemRead <='0';
104      MemtoReg <='0';
105      MemWrite <='0';
106      ALUSrc <='1';
107      RegWrite <='1';
108      UBranch <='0';
109      ALUOp <="10";
110  else
111      Reg2Loc <='0';
112      CBranch <='0';
113      MemRead <='0';
114      MemtoReg <='0';
115      MemWrite <='0';
116      ALUSrc <='0';
117      RegWrite <='0';
118      UBranch <='0';
119      ALUOp <="11";
120  end if;
121

```

This is my ALU control for lab3:

```

E:\Modelism\ee126\lab3\alucntrl.vhd - Default
Ln#
11  Opcode : in STD_LOGIC_VECTOR(10 downto 0);
12  Operation : out STD_LOGIC_VECTOR(3 downto 0)
13  );
14  end ALUControl;
15
16  architecture behavl of ALUControl is
17  begin
18  col : process(ALUOp,Opcode)
19  begin
20  if Opcode="10010001000" then
21      operation <= "0010";
22
23  elsif Opcode="10001011000" then
24      operation <= "0010";
25  elsif Opcode = "11010001000" then
26      operation <= "0110";
27  elsif Opcode = "10001010000" then
28      operation <= "0000";
29  elsif Opcode = "10101010000" then
30      operation <= "0001";
31  elsif Opcode = "11111000000" then
32      operation <= "0010";
33  elsif Opcode = "11111000010" then
34      operation <= "0010";
35  elsif Opcode = "11001011000" then
36      operation <= "0110";
37  else
38      operation <= "1111";
39  end if;
40  end process;
41  end behavl;

```

**CORE INSTRUCTION FORMATS**

<b>R</b>	opcode		Rm	shamt		Rn	Rd
	31	21 20	16 15	10 9	5 4	0	
<b>I</b>	opcode		ALU immediate		Rn	Rd	
	31	22 21	10 9	5 4	0		
<b>D</b>	opcode		DT address		op	Rn	Rt
	31	21 20	12 11	10 9	5 4	0	
<b>B</b>	opcode	BR address					
	31	26 25					0
<b>CB</b>	Opcode	COND BR address				Rt	
	31	24 23	5 4			0	
<b>IW</b>	opcode		MOV immediate			Rd	
	31	21 20	5 4			0	

```
E:\Modelsim\ee126/lab3/signextend.vhd - Default
```

```
Ln#  
13 architecture behv1 of SignExtend is  
14 begin  
15 process(x)  
16 begin  
17     if x(28 downto 22) = "1000100" then  
18         if x(21) = '0' then  
19             y <= x("0000000000000000" & x(21 downto 10);  
20         else  
21             y <= x("FFFFFFFFFFFFFF" & x(21 downto 10);  
22         end if;  
23     elsif x(31 downto 27) = "11111" then  
24  
25         if x(20) = '0' then  
26             y <= "000000000000000000000000000000000000000000000000000" & x(20 downto 12);  
27         else  
28             y <= "111111111111111111111111111111111111111111111111111" & x(20 downto 12);  
29         end if;  
30     elsif x(31 downto 24) = "10110100" then  
31  
32         if x(23) = '0' then  
33             y <= "000000000000000000000000000000000000000000000" & x(23 downto 5);  
34         ELSE  
35             y <= "111111111111111111111111111111111111111111111" & x(23 downto 5);  
36         end if;  
37  
38     elsif (x(31 downto 26) = "000101") then  
39  
40         if x(25) = '0' then  
41             y <= "00000000000000000000000000000000000000000000" & x(25 downto 0);  
42         ELSE  
43             y <= "111111111111111111111111111111111111111111111" & x(25 downto 0);  
44         end if;  
45  
46         y <= "111111111111111111111111111111111111111111111" & x(25 downto 0);  
47     end if;  
48 else  
49         y <= x("0000_0000_0000_0001");  
end if;  
end process;  
end behv1;
```

For the test part, we need to write the testbench, for this lab we use one test bench to finish all three test, but we use three different IMEM which have different group of instructions. Blew is my test bench for the lab3:

```

E:/Modelism/ee126/lab3/Singlecyclecpu_tb.vhd - Default
Ln#
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3  use IEEE.NUMERIC_STD.ALL;
4
5  entity Singlecyclecpu_tb is
6  end Singlecyclecpu_tb;
7
8  architecture Singlecyclecpu_tb of Singlecyclecpu_tb is
9
10 component SingleCycleCPU
11 port (clk :in STD_LOGIC;
12       rst :in STD_LOGIC;
13       DEBUG_PC : out STD_LOGIC_VECTOR(63 downto 0);
14       DEBUG_INSTRUCTION : out STD_LOGIC_VECTOR(31 downto 0);
15       DEBUG_TMP_REGS : out STD_LOGIC_VECTOR(64*4 - 1 downto 0);
16       DEBUG_SAVED_REGS : out STD_LOGIC_VECTOR(64*4 - 1 downto 0);
17       DEBUG_MEM_CONTENTS : out STD_LOGIC_VECTOR(64*4 - 1 downto 0)
18 );
19 end component;
20 signal rst : std_logic;
21 signal clk : STD_LOGIC:= '0';
22 signal DEBUG_MEM_CONTENTS : std_logic_vector(64*4 - 1 downto 0);
23 signal DEBUG_TMP_REGS : std_logic_vector(64*4 - 1 downto 0);
24 signal DEBUG_PC : STD_LOGIC_VECTOR(63 downto 0);
25 signal DEBUG_INSTRUCTION : STD_LOGIC_VECTOR(31 downto 0);
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```

The complete waveform will be stored separately in the file.





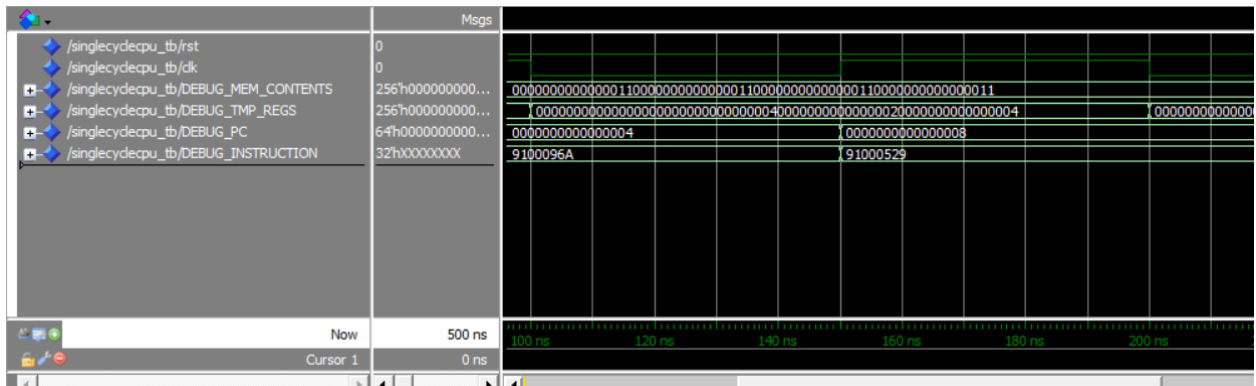


Figure2 computation test (100-200ns)

During this time, the instruction in IMEM = 9100096A is executed, we can see that DEBUG\_TMP\_REGS is changed from

```
sim:/singlecyclecpu_tb/DEBUG_TMP_REGS @ 140 ns
256'h0000000000000000000000000000000030000000000000020000000000000004
```

To

```
sim:/singlecyclecpu_tb/DEBUG_TMP_REGS @ 171 ns
256'h0000000000000000000000000000000400000000000000020000000000000004
```

So X10 is changed to  $4(X11+2)$ .

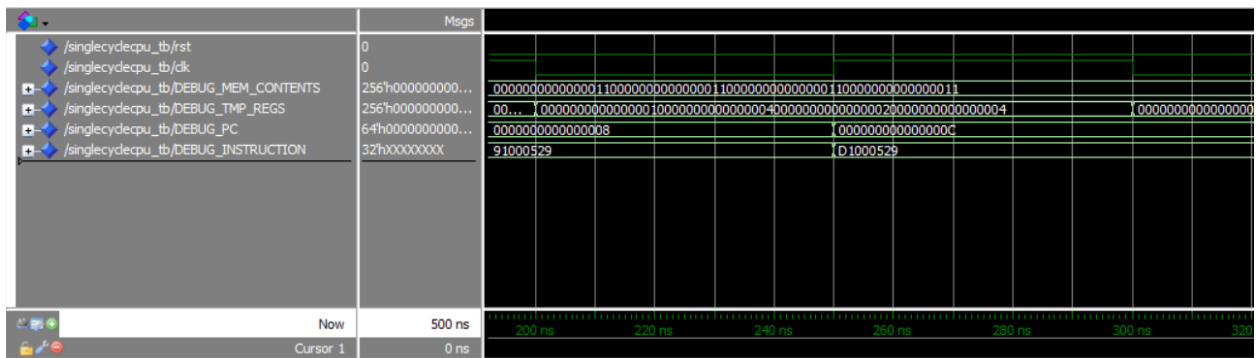


Figure3 computation test (200-300ns)

During this time, the instruction in IMEM = 91000529 is executed, we can see that

DEBUG\_TMP\_REGS is changed from

```
sim:/singlecyclecpu_tb/DEBUG_TMP_REGS @ 233 ns
256'h0000000000000000000000000000000400000000000000020000000000000004
```

To

```
sim:/singlecyclecpu_tb/DEBUG_TMP_REGS @ 287 ns
256'h0000000000000000010000000000000040000000000000020000000000000004
```



So X9 is changed to  $1(X9+1)$ .

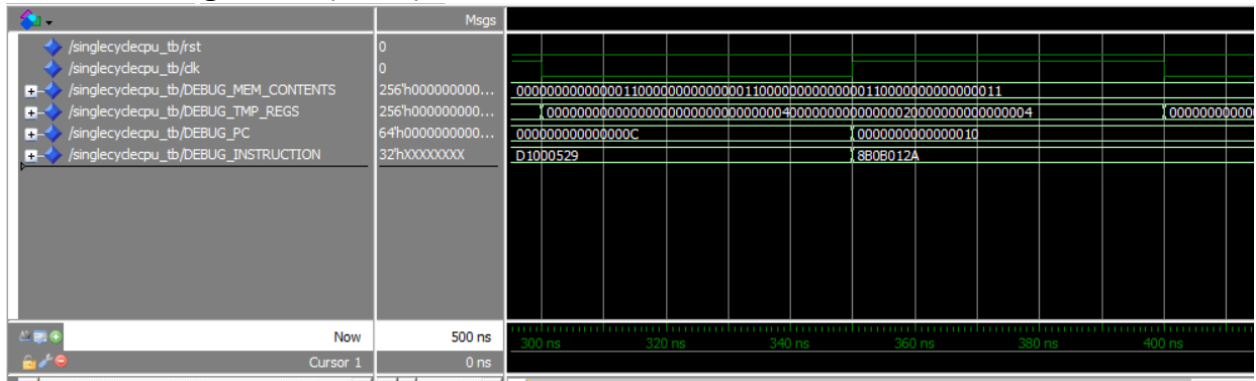


Figure4 computation test (300-400ns)

During this time, the instruction in IMEM = D1000529 is executed, we can see that

DEBUG\_TMP\_REGS is changed from

```
sim:/singlecyclecpu_tb/DEBUG_TMP_REGS @ 330 ns
256'h0000000000000000100000000000000040000000000000020000000000000004
```

To

```
sim:/singlecyclecpu_tb/DEBUG_TMP_REGS @ 380 ns
256'h0000000000000000000000000000000040000000000000020000000000000004
```

So X9 is changed to  $0(X9-1)$ .

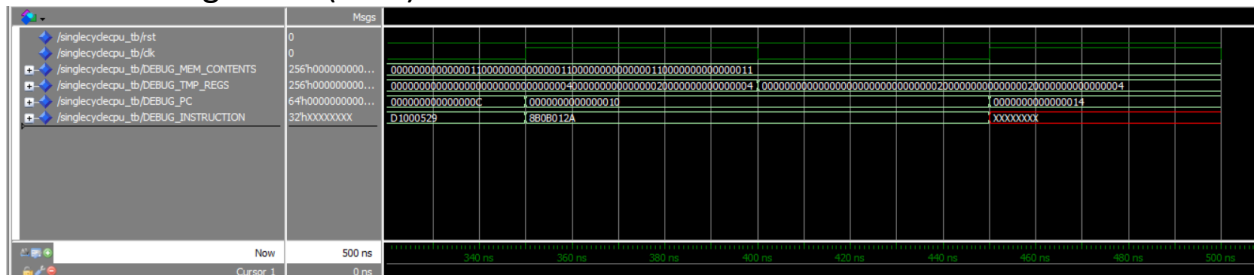


Figure5 computation test (400-500ns)

During this time, the instruction in IMEM = 8B0B012A is executed, we can see that

DEBUG\_TMP\_REGS is changed from

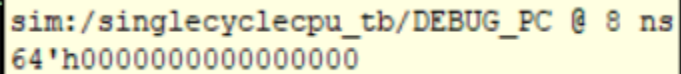
```
sim:/singlecyclecpu_tb/DEBUG_TMP_REGS @ 434 ns
256'h0000000000000000000000000000000040000000000000020000000000000004
```

To

```
sim:/singlecyclecpu_tb/DEBUG_TMP_REGS @ 467 ns
256'h0000000000000000000000000000000020000000000000020000000000000004
```

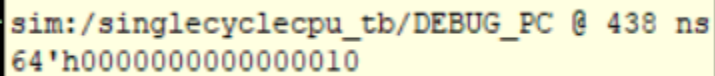
So X10 is changed to  $2(X9+x11)$ .

And during the whole the PC is increasing each cycle, from



```
sim:/singlecyclecpu_tb/DEBUG_PC @ 8 ns  
64'h0000000000000000
```

To



```
sim:/singlecyclecpu_tb/DEBUG_PC @ 438 ns  
64'h0000000000000010
```

Because there is no fifth instruction in the IMEM, so DEBUG\_INSTRUCTION become xxxxxxxx after 450 ns and the result of the test is correct.

## B. Communication Test

Test code:

```
STUR X10, [X11, 0]  
LDUR X10, [X9, 0]  
----- Assembly Trasnlation -----  
16'h0000: out = 32'b111110000000000000000000101101010; // STUR X10, [X11, 0]  
16'h0001: out = 32'b111110000100000000000000100101010; // LDUR X10, [X9, 0]
```

Test result:

The figure below just shows the result of six signals:

Clk,rst,

DEBUG\_MEM\_CONTENTS,

DEBUG\_TMP\_REGS,

DEBUG\_PC,

DEBUG\_INSTRUCTION

The complete waveform will be stored separately in the file.

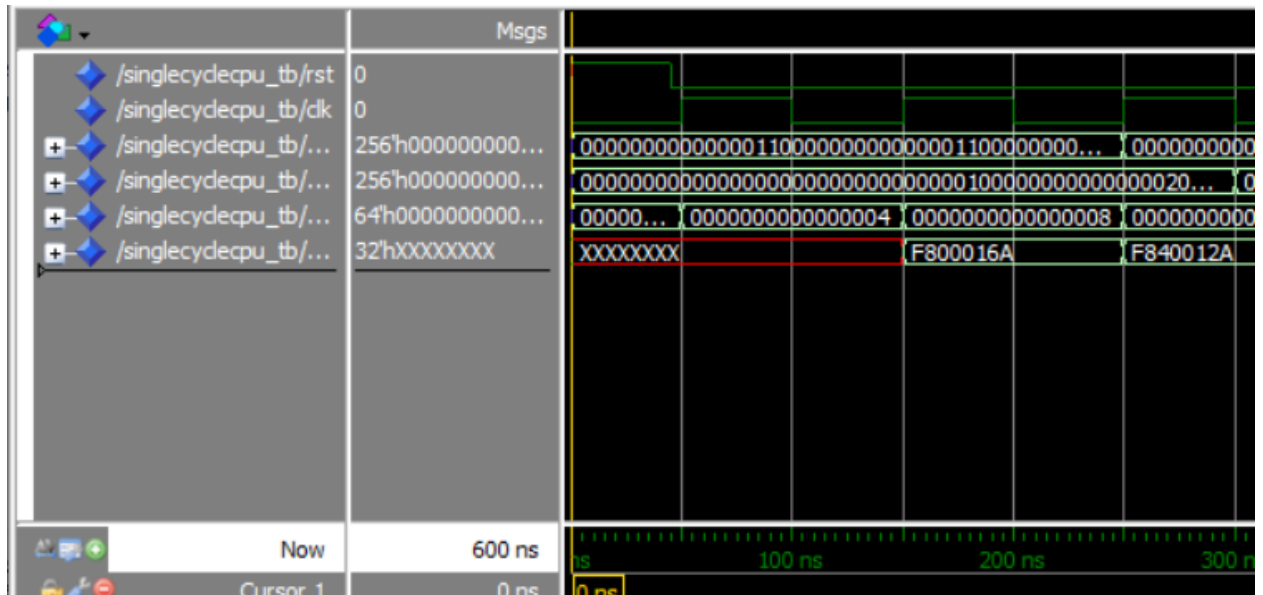


Figure6 communication test(0-250ns)

Because there is no instruction in the IMEM from imemBytes(0) to imemBytes(7):

```

E:\Models\ee126\lab3\imem_dstr.vhd (/singlecyclecpu_tb\aut\IMEM_1) - Default *
Ln#
21 process(Address)
22 variable addr:integer;
23 variable first:boolean:=true;
24 begin
25   if(first) then
26     -- STUR X10, [X11,0]
27     imemBytes(11) <= "11111000";
28     imemBytes(10) <= "00000000";
29     imemBytes(9) <= "00000001";
30     imemBytes(8) <= "01101010";
31
32     -- LDUR X10, [X9, 0]
33
34     imemBytes(15) <= "11111000";
35     imemBytes(14) <= "01000000";
36     imemBytes(13) <= "00000001";
37     imemBytes(12) <= "00101010";
38
39
40
41
42
43

```

So, the DEBUG\_INSTRUCTION is xxxxxxx before 150 ns

During time t=150ns to 200 ns, the instruction in IMEM = F800 016A is executed, we can see that

DEBUG\_MEM\_CONTENTS is changed from

```

sim:/singlecyclecpu_tb/DEBUG_MEM_CONTENTS @ 51 ns
256'h000000000000000011000000000000001100000000000000110000000000000011

```

To

```

sim:/singlecyclecpu_tb/DEBUG_MEM_CONTENTS @ 255 ns
256'h00000000000000001100000000000000110000000000000000000000000010011

```

Because

So we can know `dmemBytes(2)` is changed to 1.



DEBUG\_TMP\_REGS is changed from

[illegible]

### C. Final Test

Test code:

```

    ADDI X9, X9, 1
    ADD  X10,X9,X11
    STUR X10, [X11,0]
    LDUR X12, [X11, 0]
    CBZ  X9, 2
    B 3
    ADD  X9, X10, X11
    ADDI X9, X9, 1
    ADD  X21, X10, X9

```

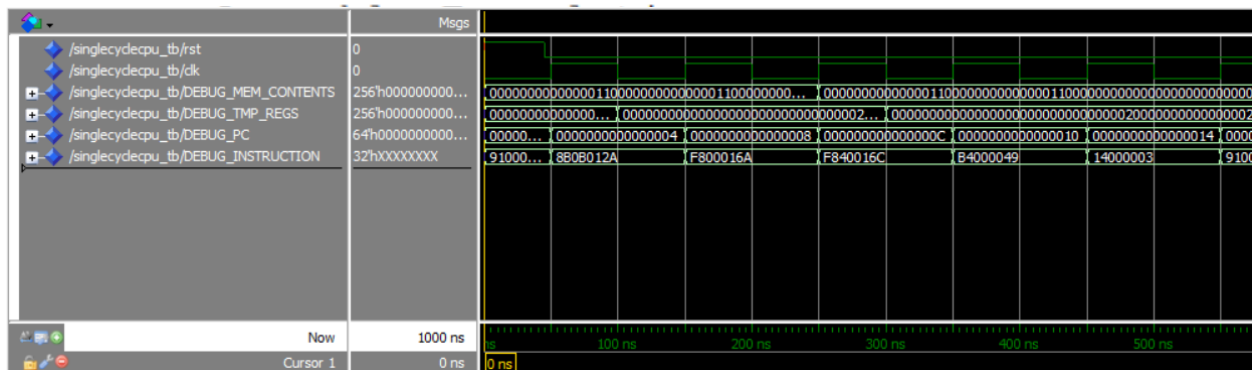


Figure8 final test(0-500ns)

For the 0-500ns, the figure 8 shows the result of final test, Since four of these instructions have already been discussed above, they are not discussed.

But we should notice that address of PC is changed from

```

sim:/singlecyclecpu_tb/DEBUG_PC @ 393 ns
64'h00000000000000010

```

To

```

sim:/singlecyclecpu_tb/DEBUG_PC @ 507 ns
64'h00000000000000014

```

Means not branch by the instruction “CBZ X9,2” because X9 is not equal to 0.

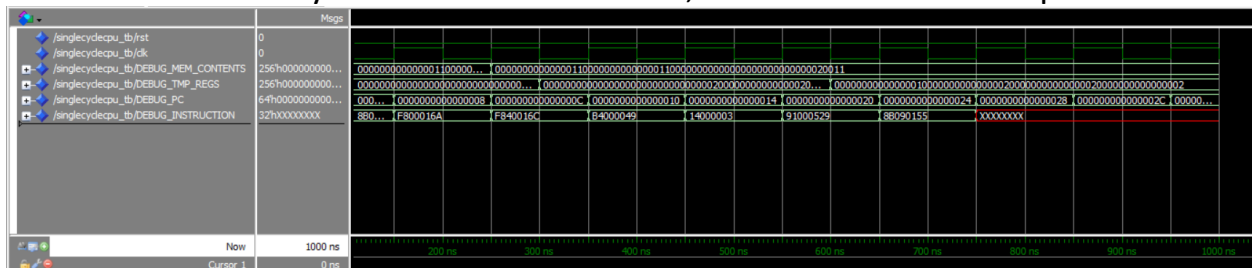


Figure9 final test(500-1000ns)

During this time t=450ns to 550ns, the instruction in IMEM = 1400 0003is executed, we can see that

DEBUG\_PC is changed from

```
sim:/singlecyclecpu_tb/DEBUG_PC @ 515 ns  
64'h0000000000000014
```

To

```
sim:/singlecyclecpu_tb/DEBUG_PC @ 621 ns  
64'h0000000000000020
```

Hex 20 = 32

Hex 14 = 20

So the address is increase 12 not 4. So the instruction "B 3".

And we can see next instruction we execute is 9100 0529 which is

```
E:/Modelism/ee126/lab3/imem_p1.vhd (/singlecyclecpu_tb/uut/IMEM_1) - Default  
Ln#  
62  
63      -- ADD X9, X10, X11  
64      imemBytes(27) <= "10001011";  
65      imemBytes(26) <= "00001011";  
66      imemBytes(25) <= "00000001";  
67      imemBytes(24) <= "01001001";  
68      -- ADD X9, X10, X11  
69      imemBytes(31) <= "10001011";  
70      imemBytes(30) <= "00001011";  
71      imemBytes(29) <= "00000001";  
72      imemBytes(28) <= "01001001";  
73  
74      -- ADDI X9, X9, 1  
75      imemBytes(35) <= "10010001";  
76      imemBytes(34) <= "00000000";  
77      imemBytes(33) <= "00000101";  
78      imemBytes(32) <= "00101001";  
79  
80      -- ADD X21, X10, X9  
81      imemBytes(39) <= "10001011";  
82      imemBytes(38) <= "00001001";  
83      imemBytes(37) <= "00000001";  
84      imemBytes(36) <= "01010101";  
85  
86
```

So we skipped two instructions. The result is correct.

#### ④ Question

If we change X9=-1, then we execute code:



```

STUR X10, [X11, 0]
LDUR X10, [X9, 0]

Registers(8) <= x"0000_0000_0000_0000"; --X8
Registers(9) <= x"ffff_ffff_ffff_ffff"; --X9

```

We

get

```

# time: 250 ns iteration: 5 Process: /singlecyclecpu_tb/uut/DMEM_1/line__2/ file: E:/Modelism/eel26/lab3
# Fatal error in Process line__27 at E:/Modelism/eel26/lab3/dmem_1e.vhd line 93
#
# HDL call sequence:
# Stopped at E:/Modelism/eel26/lab3/dmem_1e.vhd 93 Process line__27
#
VSI22>

```

The test is failed. In the DMEM file we have:

```

Ln#
18 -- Four 64-bit words: DMEM(0) & DMEM(4) & DMEM(8) & DMEM(12)
19 DEBUG_MEM_CONTENTS : out STD_LOGIC_VECTOR(64*4 - 1 downto 0)
20 );
21 end DMEM;
22
23 architecture behavioral of DMEM is
24 type ByteArray is array (0 to NUM_BYTES-1) of STD_LOGIC_VECTOR(7 downto 0);
25 signal dmemBytes:ByteArray;
26 begin
27 process(Clock,MemRead,MemWrite,WriteData,Address) -- Run when any of these inputs change
28 variable addr:integer;
29 variable first:boolean := true; -- Used for /singlecyclecpu_tb/uut/DMEM_1/Address
30 begin
31 -- This part of the process initializes the memory and is only here for simulation purposes
32 -- It does not correspond with actual hardware!
33 if(first) then
34 dmemBytes(0) <= "00010001";
35 dmemBytes(1) <= "00000000";
36 dmemBytes(2) <= "00000000";
37 dmemBytes(3) <= "00000000";
38 dmemBytes(4) <= "00000000";
39 dmemBytes(5) <= "00000000";
40 dmemBytes(6) <= "00000000";

```

The address = "FFFFFFFFFFFFFFFF", I the address is too big to find.