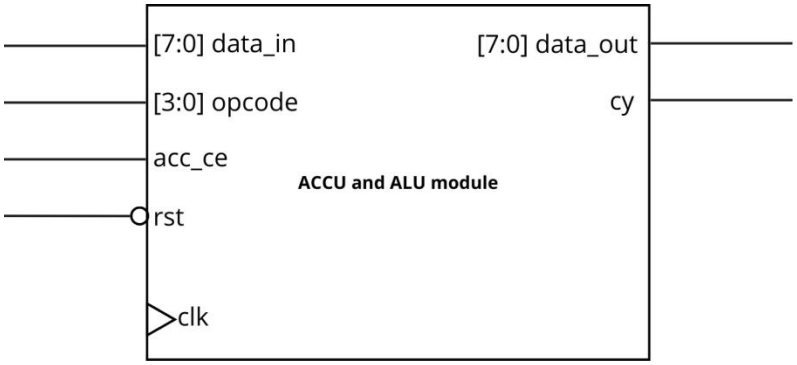
Alu and Accu module requirements

1. Overview.
   Module contain simple units of ALU and accumulator. Its task is to perform operations on 8-bit data words. Logic operations treat data as simple vector, Arithmetic operation treat data as value represented in U2 code.



2. Interface.
   Module ports describes table Tab.1

Signal Name	Signal attributes	description
Module inputs		
clk	1 bit wire	Clock signal input, sensitivity on raising edge.
rst	1 bit wire	Reset signal input, Asynchronous, active by low signal level, sensitivity on falling edge.
data_in	8 bit signed wire	Input data value.
opcode	4 bit wire	Input signal for operation code
acc_ce	1 bit wire	Input signal that controls writing to the accumulator. Active by high signal level.
Module outputs		
data_out	8 bit signed register	Data output value. Takes a value in the range -128 to 127. When the result goes out of range, it wraps around.
cy	1 bit register	Carry out value. Signal corresponded with overflow and underflow of accumulator value for arithmetic operations. Its take a high level when value exceeds 127 of positive value, or -128 of negative value. Its take low signal level for any other operation than arithmetic

3. Operations:

Operations codes. (opcode)		
Mnemonic	Bit code	Description.
LD	4'b0000	Load data to ACC
ST	4'b0001	Do nothing, only put ACC to data_out
ADD	4'b0010	Arithmetic operation, ACC + data_in.
SUB	4'b0011	Arithmetic operation, ACC- data_in.
AND	4'b0100	Logical operation ACC & data_in
OR	4'b0101	Logical operation ACC | data_in
XOR	4'b0110	Logical operation ACC ^ data_in
NOT	4'b0111	Logical operation ACC = ~data_in
NOP	4'b1111	Do nothing

Behaviour:

- LOW level off rst signal reset value of data_out to 0. No operations can be performed.
- HIGH rst signal value is necessary to perfortm any operation.
- All operations are triggered on raising edge of clk signal
- To update value of data_out output, its necessary to set accu_ce signal value to high, before of clk rising edge.