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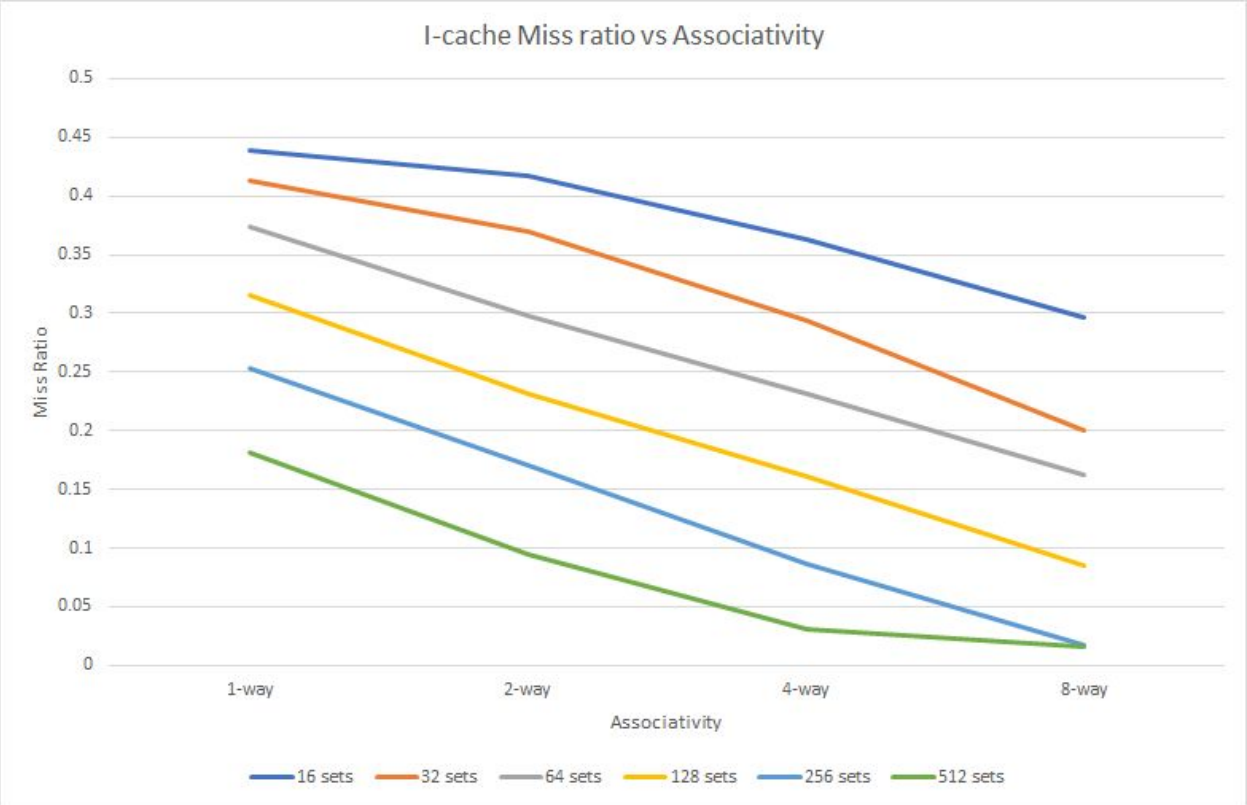
CS 472 Lab

1.

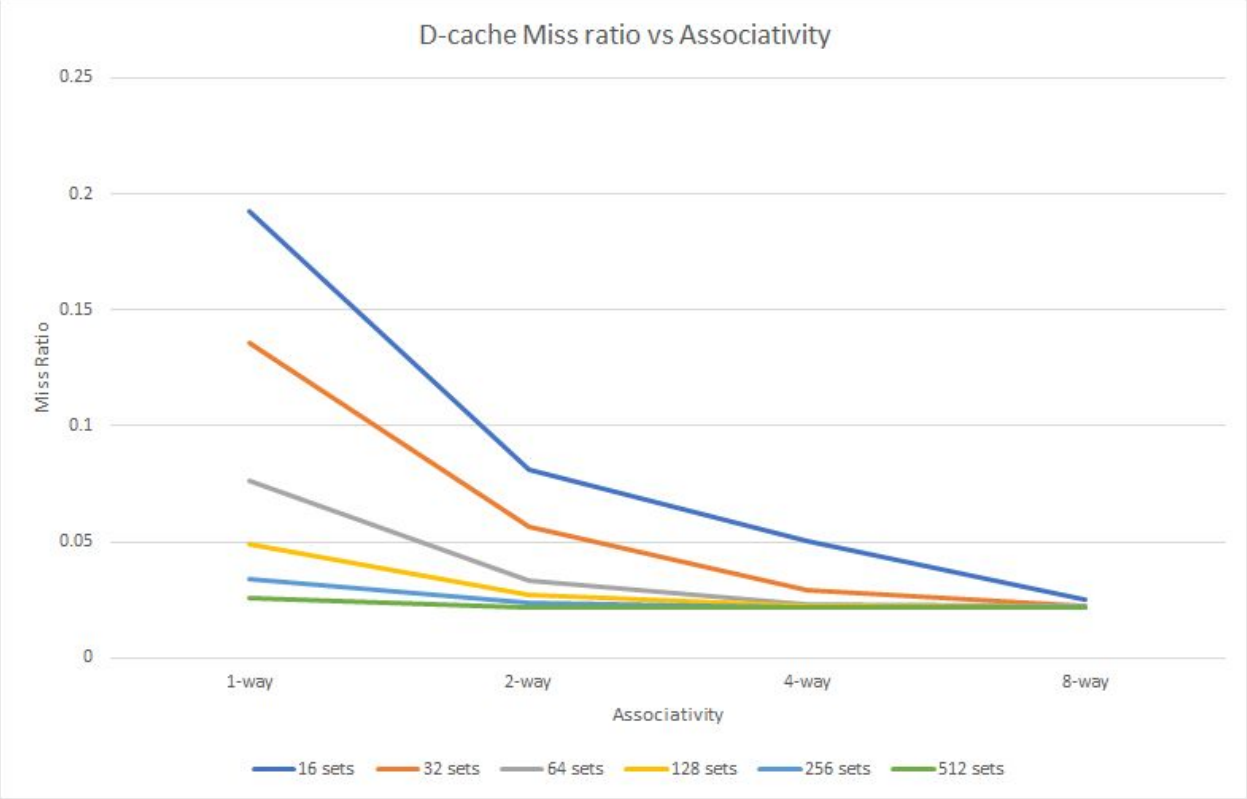
I-cache Miss Ratio by Sets vs Associativity

	1-way	2-way	4-way	8-way
16 sets	0.4388	0.4179	0.3635	0.2971
32 sets	0.4134	0.3695	0.2941	0.1997
64 sets	0.3732	0.2986	0.2313	0.1627
128 sets	0.3155	0.2321	0.1615	0.0851
256 sets	0.253	0.1699	0.086	0.0177
512 sets	0.1816	0.0948	0.031	0.0154



D-cache Miss Ratio by Sets vs Associativity

	1-way	2-way	4-way	8-way
16 sets	0.1925	0.0813	0.0504	0.0249
32 sets	0.1359	0.0568	0.029	0.0226
64 sets	0.0761	0.0336	0.023	0.0223
128 sets	0.0491	0.0273	0.0224	0.0216
256 sets	0.0342	0.0239	0.0216	0.0215
512 sets	0.0256	0.0218	0.0215	0.0215



a) For a given number of sets, what effect does increasing associativity have on the miss ratio?

Increasing associativity tends to decrease the miss ratio for any given set size.

b) For a given associativity, what is the effect of increasing the number of sets?

A larger set size shows a smaller miss ratio for any given associativity.

c) For a given cache size, how does the miss ratio change when going from an associativity of one to two to four? Explain.

For a given cache size, increasing associativity tends to show a minor decrease in miss ratio from 1-way to 2-way associativity. However, there is a minor *increase* in miss ratio from 2-way to 4-way associativity for many (but not all) cases.

d) If you were to design an Instruction cache, limited to a total cache size of 4 Kbytes, which cache organization would you choose, based solely on performance?

Based off of the results and assuming a fixed block size of 16 bytes as was the case in testing, maximum performance can be obtained using 32 sets and 8-way associativity.

e) If you were to design a data cache, limited to a total cache size of 4 Kbytes, which cache organization would you choose, based solely on performance?

Based off of the results and assuming a fixed block size of 16 bytes as was the case in testing, maximum performance can be obtained using 32 sets and 8-way associativity.

2.

Sets / Assoc	I-Cache Miss No. (N/2 sets)	D-Cache Miss No. (N/2 sets)	Total Accesses	Effective Combined Cache Miss Rate	Unified Cache Miss Rate
128 / 1	70679	3668	237599	0.3130	0.2996
128 / 2	56547	1620	237599	0.2448	0.2131
128 / 4	43815	1109	237599	0.1891	0.1474
2048 / 1	21674	1069	237599	0.0957	0.0511
2048 / 2	6501	1035	237599	0.0317	0.0189
2048 / 4	2909	1035	237599	0.0166	0.0166

Note:
I ran split-cache with the following:
./sim-cache -cache:il1 i11:$sets:16:$assoc:l -cache:dl1 d11:$sets:16:$assoc:l -cache:il2 none -cache:dl2 none -tlb:itlb none -tlb:dtlb none tests-pisa/bin.little/test-math

I ran unified-cache with the following:
./sim-cache -cache:il1 dl1 -cache:dl1 d11:$sets:16:$assoc:l -cache:il2 none -cache:dl2 none -tlb:itlb none -tlb:dtlb none tests-pisa/bin.little/test-math