Name: _____ CWID: _____ Date: _____

CALIFORNIA STATE UNIVERSITY, FULLERTON

Computer Engineering

EGCP 180 – Digital Logic and Computer Structures (Fall 2018)

Final Exam (Total Points = 100)

(Time allowed: 2:30 — 4:20 PM)

Academic Dishonesty Policy

In line with University policies, the Computer Engineering program supports a strict and well-defined policy against academic dishonesty. Thus, to assure a fair and equitable testing environment for all students, there will be zero tolerance during exam for any of the following:

- Cheating of any type (looking at or copying another student's answers) or helping another student with answers.
- Use of notes, phones, or other aids (other than that allowed by instructor)
- Talking or texting during exams
- Leaving the classroom during the exam (without permission)

Consequences for violating these policies will be a "zero" on the exam at a minimum, with the possibility of an F in the course.

Only one page of handwritten notes (two side), pens/pencils, erasers, and a calculator (shouldn't be necessary) are allowed with the exam.

Normally, full credit is given only if work is shown when appropriate.

Perfect VHDL syntax is not required, but your code should still be correctly written. Just small syntax errors, like a missing semicolon, will not be penalized.

Name: _____ CWID: _____ Date: _____

1. **(20 Points) Do the following**

BINARY	OCTAL	DECIMAL	HEXADECIMAL
1011110101.01	1365.2	757.25	2F5.4

$2\overline{)757}\,(378$ $\quad 756$ $\quad 1$

$2\overline{)378}\,(189$ $\quad 370$ $\quad 08$

$2\overline{)189}\,(94$ $\quad 188$ $\quad 1$

$2\overline{)94}\,(47$ $\quad 94$ $\quad 00$

$2\overline{)47}\,(23$ $\quad 46$ $\quad 1$

$2\overline{)23}\,(11$ $\quad 22$ $\quad 1$

$2\overline{)11}\,(5$ $\quad 10$ $\quad 1$

$2\overline{)5}\,(2$ $\quad 4$ $\quad 1$

$2\overline{)2}\,(1$ $\quad 2$ $\quad 0$

$0.25\times2=0.5$

$0.5\times2=1$

1011110101.01

1 3 6 5.2

0010 1111 0101.0100

2 F 5.4

b) Find the 1's complement, 2's complement and sign of the number based on the 8-bit signed number shown below. (Show the steps)

Number	1's Complement	2's Complement	Sign
11100110	00011001	00011010	—

11100110

00011001 – 1's Complement

$+\quad 1$

00011010 – 2's Complement

c) Convert to base 6: $3BA.24_{14}$ (do all the arithmetic in decimal).

Base 14 to 10 $\Rightarrow 3\times14^{2}+11\times14+10\times1+2\times14^{-1}+4\times14^{-2}$

$= 752.1632653$

$6\overline{)752}\,(125$ $\quad 750$ $\quad 2$

$6\overline{)125}\,(20$ $\quad 120$ $\quad 5$

$6\overline{)20}\,(3$ $\quad 18$ $\quad 2$

$6\times0.1632653=0.971592$

$6\times0.971592=5.877551$

$6\times0.877551=5.265305$

$6\times0.265305=1.591829$

$(3252.0551)_{6}$ (2/10)

Name: _____ CWID: _____ Date: _____

2. (10 Points) Max and Min term

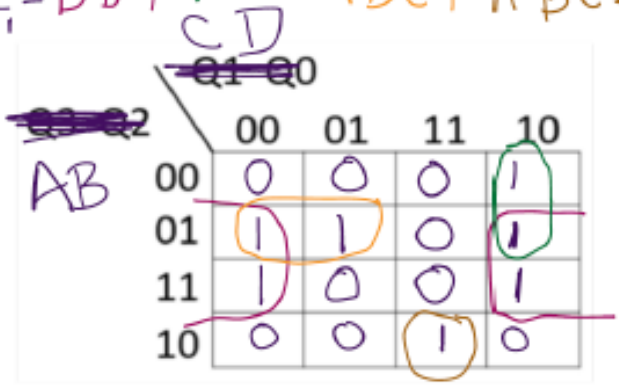
From a 4-bit Instruction Register we have the following Truth Table (instruction decoding). a) Express the Boolean functions using minterms and maxterms representations. b) Provide the Boolean functions using Sum of Products (SOP), and Product of Sums (POS).

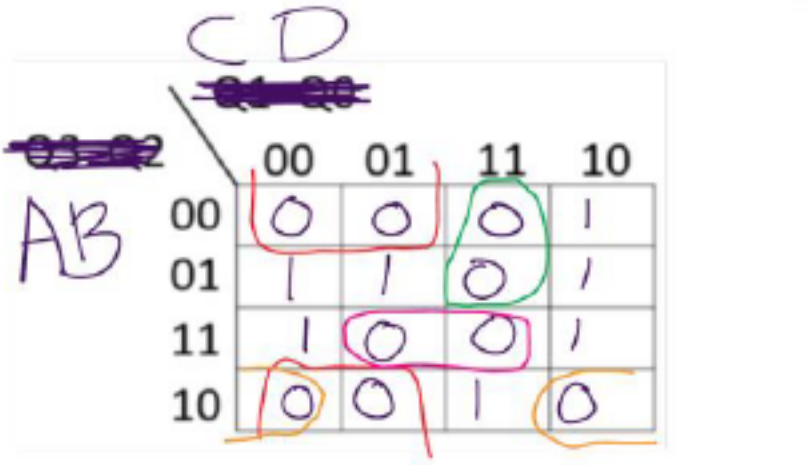
A	B	C	D	F1
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

$F_1 = \Sigma(2,4,5,6,11,12,14)$

$F_1 = \Pi(0,1,3,7,8,9,10,13,15)$

$F_1 = B\bar{D} + \bar{A}C\bar{D} + \bar{A}B\bar{C} + A\bar{B}CD$





$F_1 = (B+C)(\bar{A}+\bar{B}+\bar{D})(A+\bar{C}+\bar{D})(\bar{A}+\bar{B}+D)$

3/10

Name: _____ CWID: _____ Date: _____

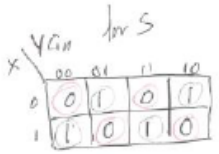
3. (30 Points) Arithmetic Logic Design

Full-Adder verbal description: has three inputs X, Y, and Cin (Carry-in). It has two outputs S (Sum) and Cout (Carry-out). It performs the addition of input numbers X, Y, and Cin. a) Write the truth table for S and Cout. b) Implement the circuits using NAND gates. c) Implement the circuits using NOR gates. d) Implement it with 3 to 8 decoder with active high output (use appropriate logic gate) e) Implement the full adder using 4-to-1 Multiplexer. Connect A and Cin to the control inputs of Mux. Connect 1's, 0's, B or $\bar{B}$ to each data input.

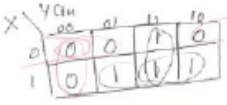
Inputs X, Y, Cin

Outputs S, Cout

X	y	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



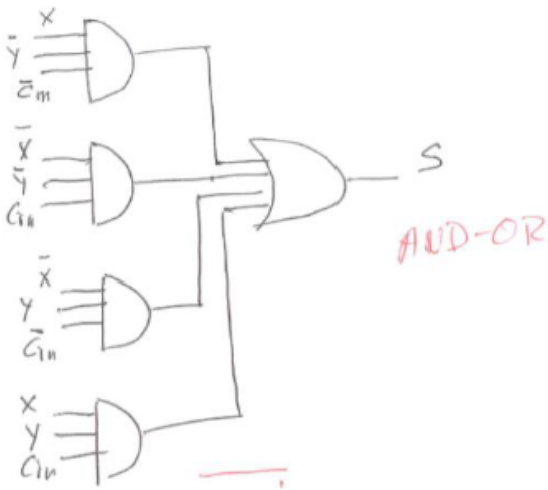
$S = X \oplus Y \oplus Cin$

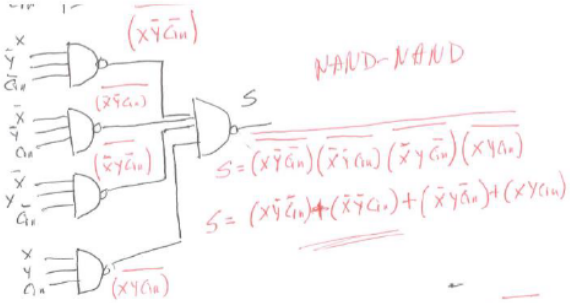


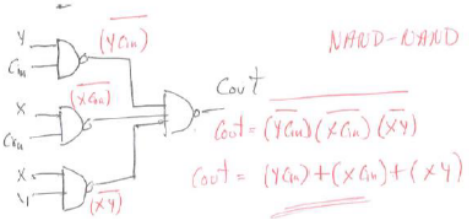
$Cout = YCin + XCin + XY$

$S = X\bar{Y}\bar{Cin} + \bar{X}\bar{Y}Cin + \bar{X}Y\bar{Cin} + XYCin$

$Cout = YCin + XCin + XY$



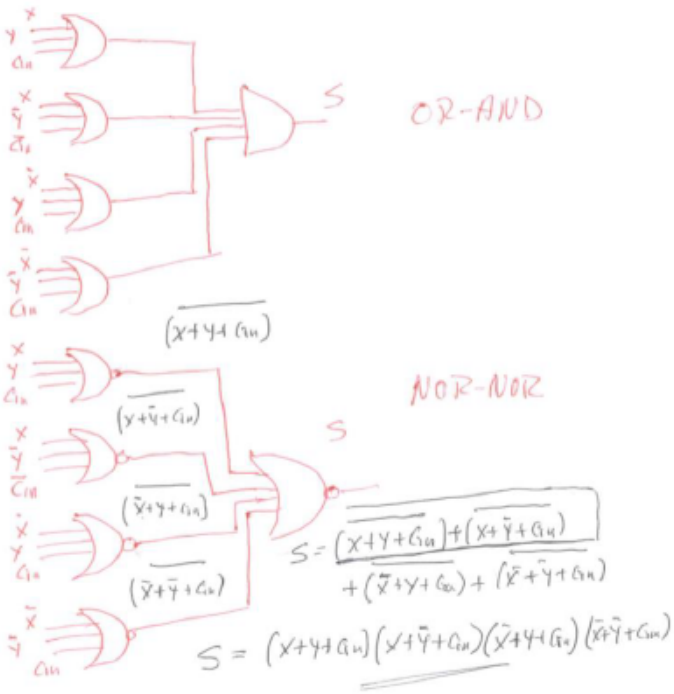


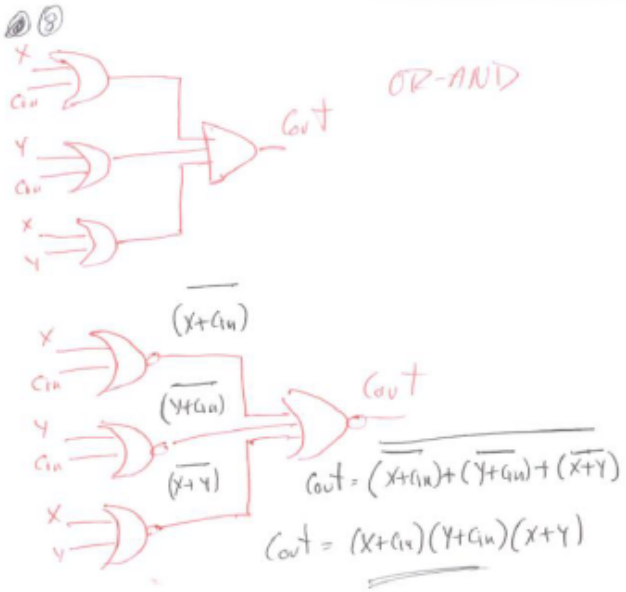


Name: _____ CWID: _____ Date: _____

$S = (X+Y+C_{in})(X+\bar{Y}+\bar{C}_{in})(\bar{X}+Y+C_{in})(\bar{X}+\bar{Y}+C_{in})$

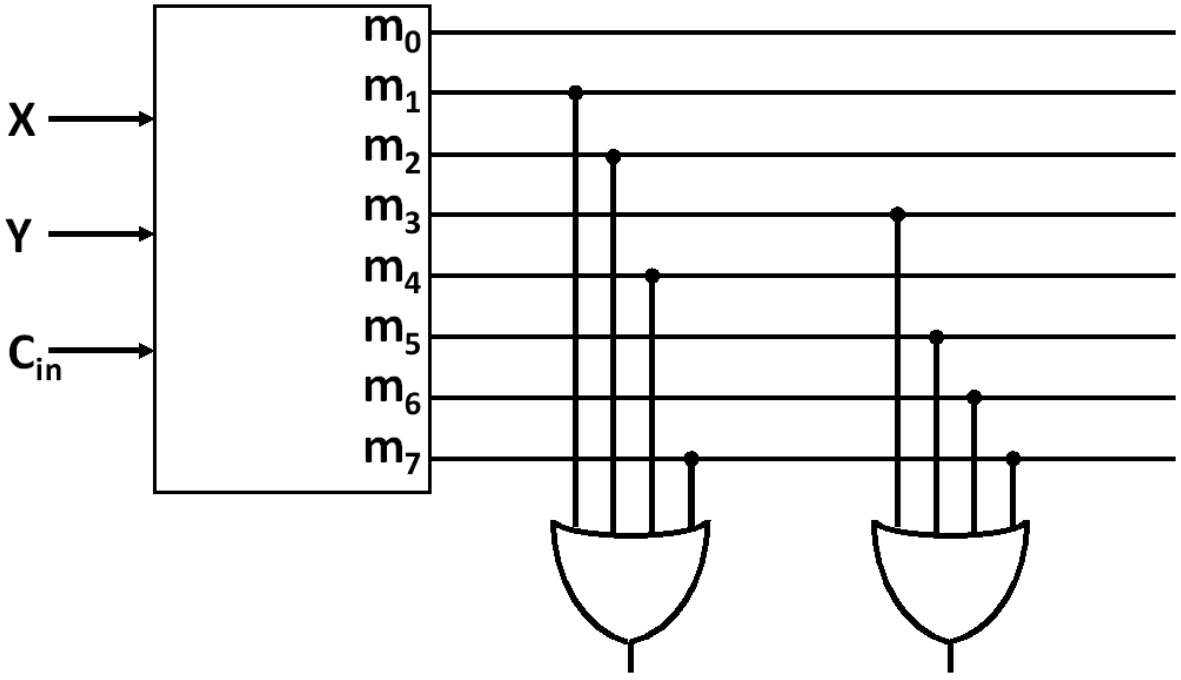
$C_{out} = (X+C_{in})(Y+C_{in})(X+Y)$



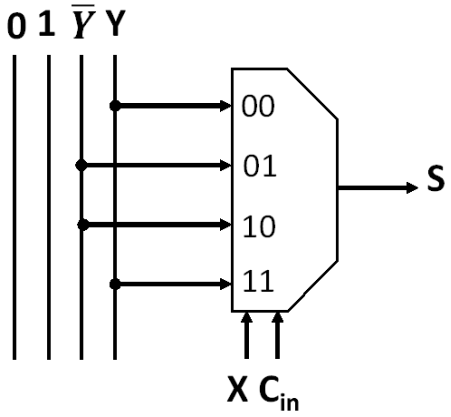


$C_{out} = (\overline{X+C_{in}}) + (\overline{Y+C_{in}}) + (\overline{X+Y})$

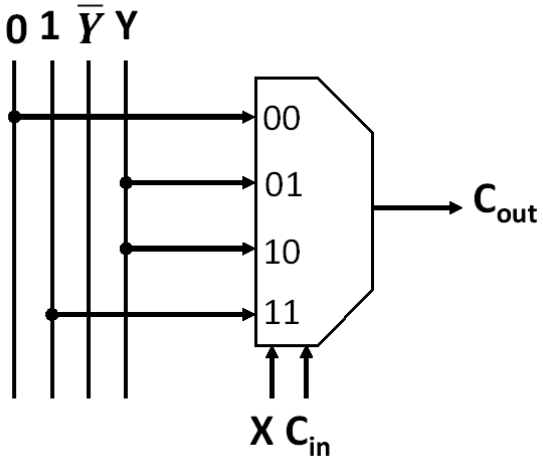
$C_{out} = (X+C_{in})(Y+C_{in})(X+Y)$



		X Cin			
		00	01	10	11
Y	0	0	1	1	0
	1	1	0	0	1



		X Cin			
		00	01	10	11
Y	0	0	0	0	1
	1	0	1	1	1

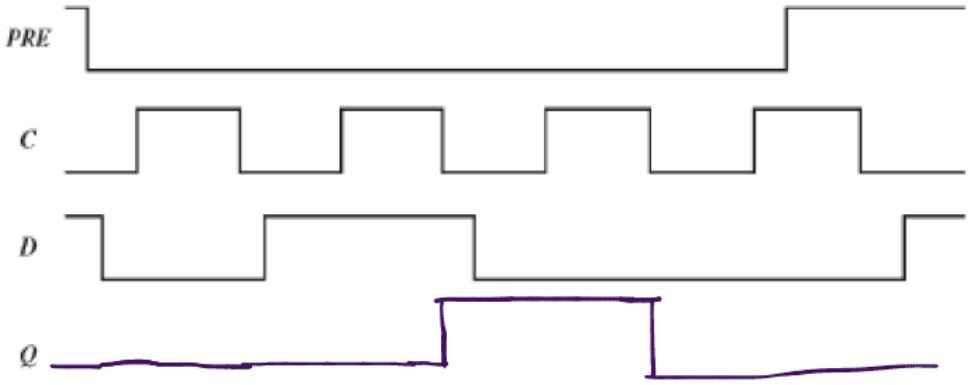


Name: _____ CWID: _____ Date: _____

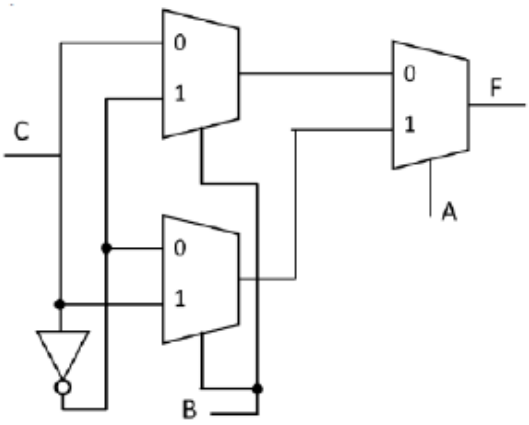
4. (10 points) Latch and Flip Flop

Complete the timing diagram

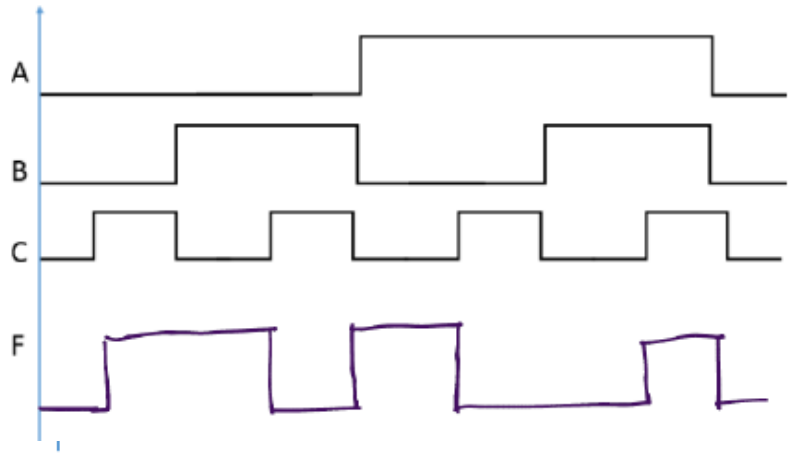
a) Draw the waveform for the Q output for a negative edge-triggered D flip-flop. In the waveform PRE is Reset, C is Clock, D is Input, and Q is Output



b) For the circuit shown below draw the waveform for F based on input A, B and C.



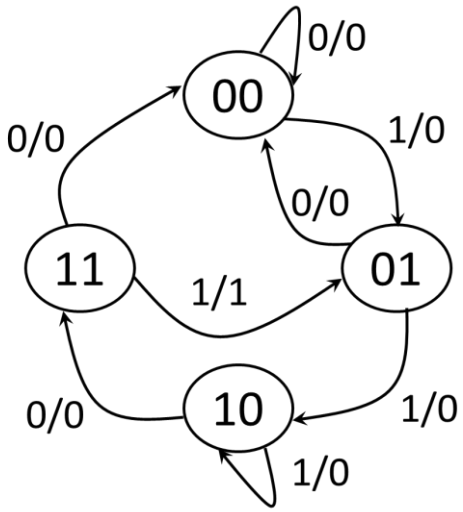
A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1



Name: _____ CWID: _____ Date: _____

5. (30 Points) State Machine Design

The following State Diagram is given.



a) The state table using D - Flip Flops is shown below. Fill it according to the state diagram.

Present State		Input	Next State		Output
A	B	X	A+	B+	Z
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	1	1	0
1	0	1	1	0	0
1	1	0	0	0	0
1	1	1	0	1	1

b) Using K-map drive the characteristic equation of the next state

A+

A\BX	00	01	11	10
0	0	0	1	0
1	1	1	0	0

$$A^+ = A\bar{B} + \bar{A}BX$$

Name: _____ CWID: _____ Date: _____

B+

A\BX	00	01	11	10
0	0	1	0	0
1	1	0	1	0

$$B^{+} = \bar{A}\bar{B}X + A\bar{B}\bar{C} + ABC$$

Z = ABC

c) Draw the logical circuit from b)