CALIFORNIA STATE UNIVERSITY
FULLERTON™

EGEC 180 – Digital Logic and Computer Structures

Spring 2024

Lecture 14: Analysis and Design of Sequential Circuits (3.4)

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Analysis & Design

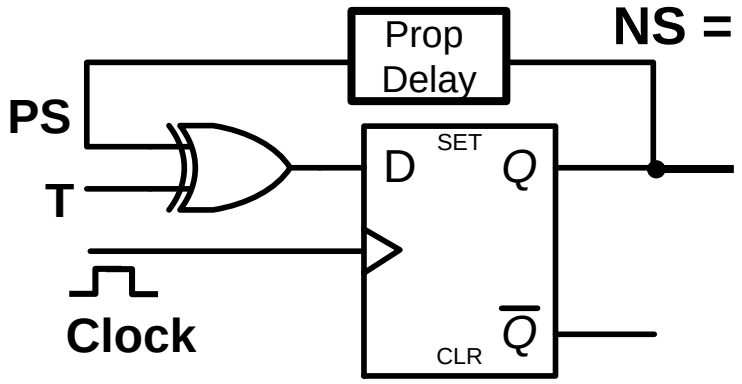
Analysis of Clocked Sequential Circuits

The behavior of a sequential circuit is determined by the inputs, outputs and states of its Flip-Flops (FFs).

Analysis: obtain a suitable description (table or diagram) for the time sequence of inputs, outputs and FF states.

- **Given a circuit**
- **Find the State Table or State Diagram**

Analysis Model: Two-process PS/NS Method



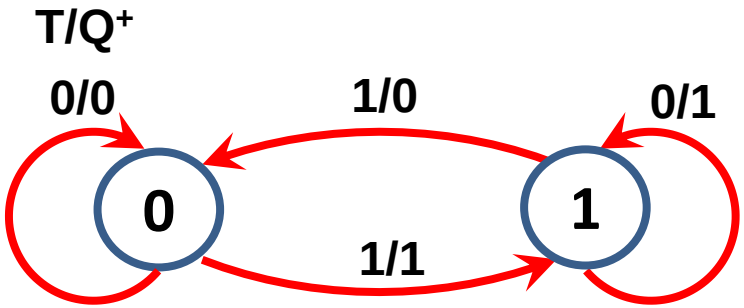
$Q^+ = T'Q + TQ'$

$= Q \oplus T$

	Q' 0	Q 1
T' 0	0	1
T 1	1	0

$Q^+ = \Sigma\, m(1,2)$

T	Q	Q^+
0	0	0
0	1	1
1	0	1
1	1	0

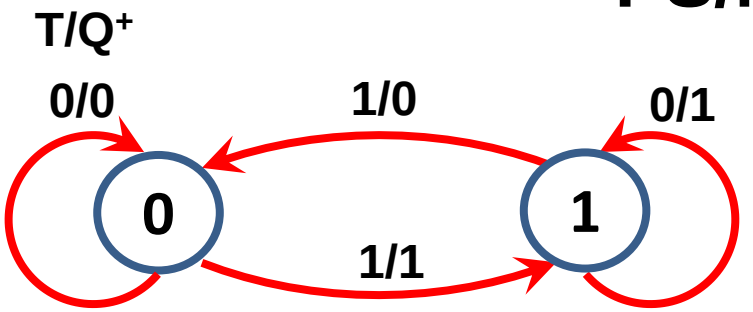


Design of Clocked Sequential Circuits

Design of Sequential Circuit: for its design we need knowledge of the type of FFs used and a list of Boolean functions for the input combinational circuit to the FFs.

- **Determine type of FFs (SR, D, T, JK)**
- **Find combinational circuit connected to input(s) of FFs**

Design Model: Two-process PS/NS Method

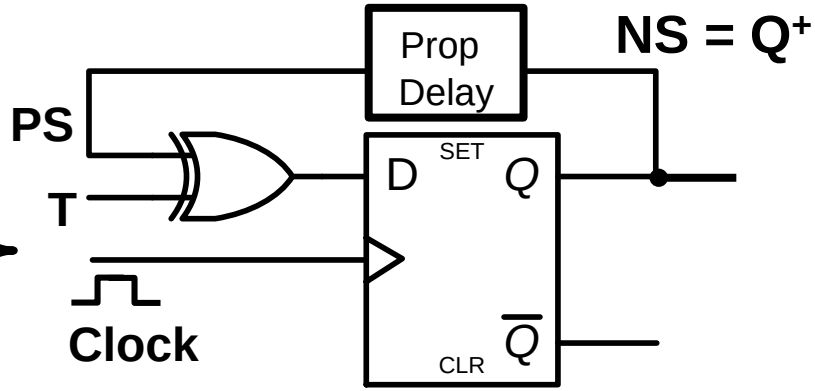


T	Q	Q+
0	0	0
0	1	1
1	0	1
1	1	0

	Q' 0	Q 1
T' 0	0	1
T 1	1	0

$Q^+ = T'Q + TQ'$

$= Q \oplus T$



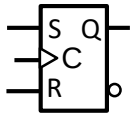
Analysis and Design of Clocked Sequential Circuits

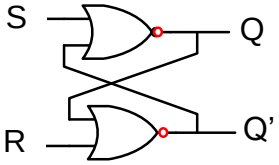
Input equations:

1) **Part of the circuit that generates the signals for the inputs to the FFs, also**
2) **Selecting the type of FFs.**
   - **Time is not specified, it is implied**
   - **Convenient way for specifying the logic diagram also known as state equations**

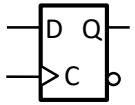
Logic Storage Devices

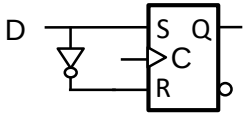
Characteristic Table



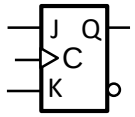


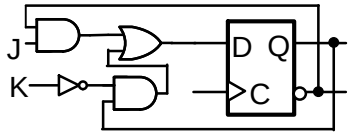
S	R	Q(t+1)	Operation
0	0	Q(t)	Hold
0	1	0	Reset
1	0	1	Set
1	1	?	Undefined



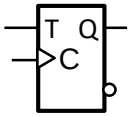


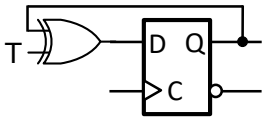
D	Q(t+1)	Operation
0	0	Reset
1	1	Set





J	K	Q(t+1)	Operation
0	0	Q(t)	Hold
0	1	0	Reset
1	0	$\overline{1}$	Set
1	1	Q(t)	Toggle





T	Q(t+1)	Operation
0	Q(t)	No Change
1	$\overline{Q(t)}$	Toggle

Excitation Table

$Q(t+1) = S + R'Q$

Q	Q^+	S	R	Operation
0	0	0	d	Hold
0	1	1	0	Set
1	0	0	1	Reset
1	1	d	0	Hold

$Q(t+1) = D$

Q^+	D	Operation
0	0	Reset
1	1	Set

$Q(t+1) = JQ' + K'Q$

Q	Q^+	J	K	Operation
0	0	0	d	Hold
0	1	0	d	Set
1	0	d	0	Reset
1	1	d	1	Hold

$Q(t+1) = Q \oplus T$

Q^+	T	Operation
Q(t)	0	Hold
$\overline{Q(t)}$	1	Toggle

Analysis and Design of Clocked Sequential Circuits

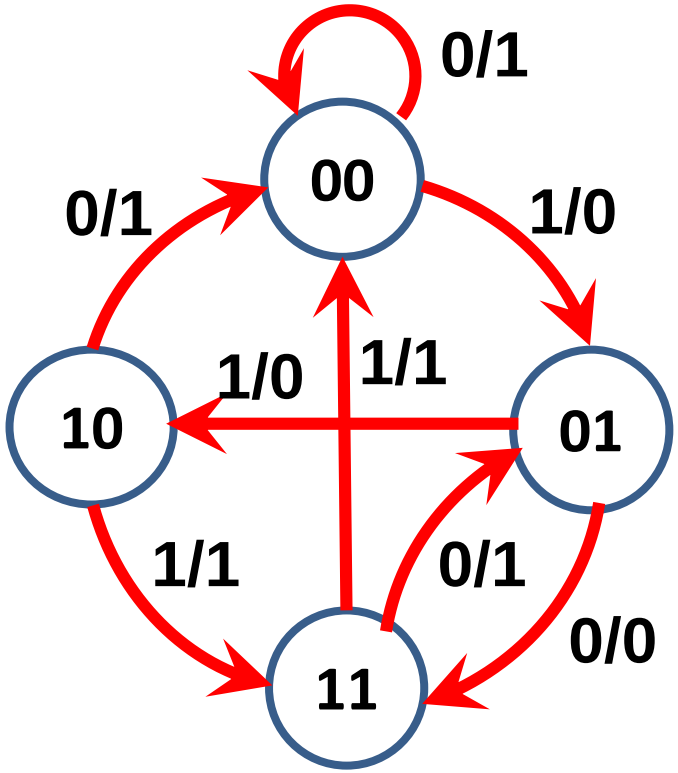
Inputs, outputs, and FF states may be listed in a State Table or drawn in a State Diagram:

State Table:

Present State (before CLK pulse)			Inputs			Next State (after CLK pulse)			Outputs (during present state)		

Lay this out like you would a truth table

Reading A State Diagram



State

Transition

1/0

Input (x) Output(z)

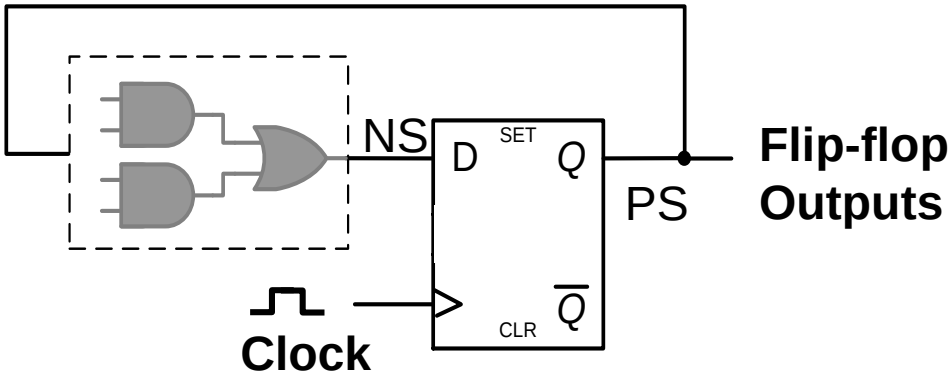
How many Flip-flops do you need?

One per binary digit in a state name
(One per Brain Cell)

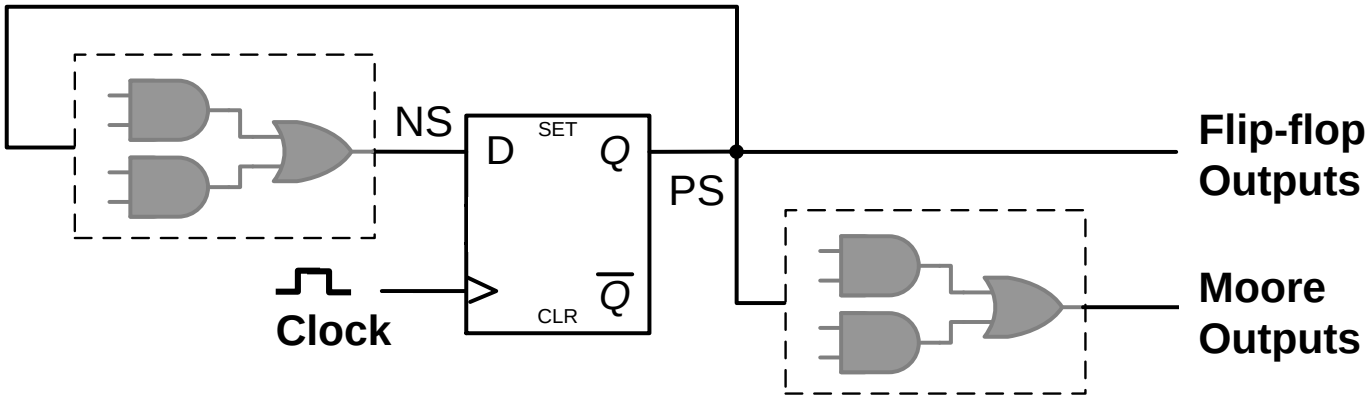
Note: **11/00** Implies 2 Inputs and that every state has 4 (2^2) transitions out.
Also, this means there are 2 outputs with each transition.

Moore Models

Moore Model: Sequential Circuits in which outputs depend on the states, one dimensional column suffices.

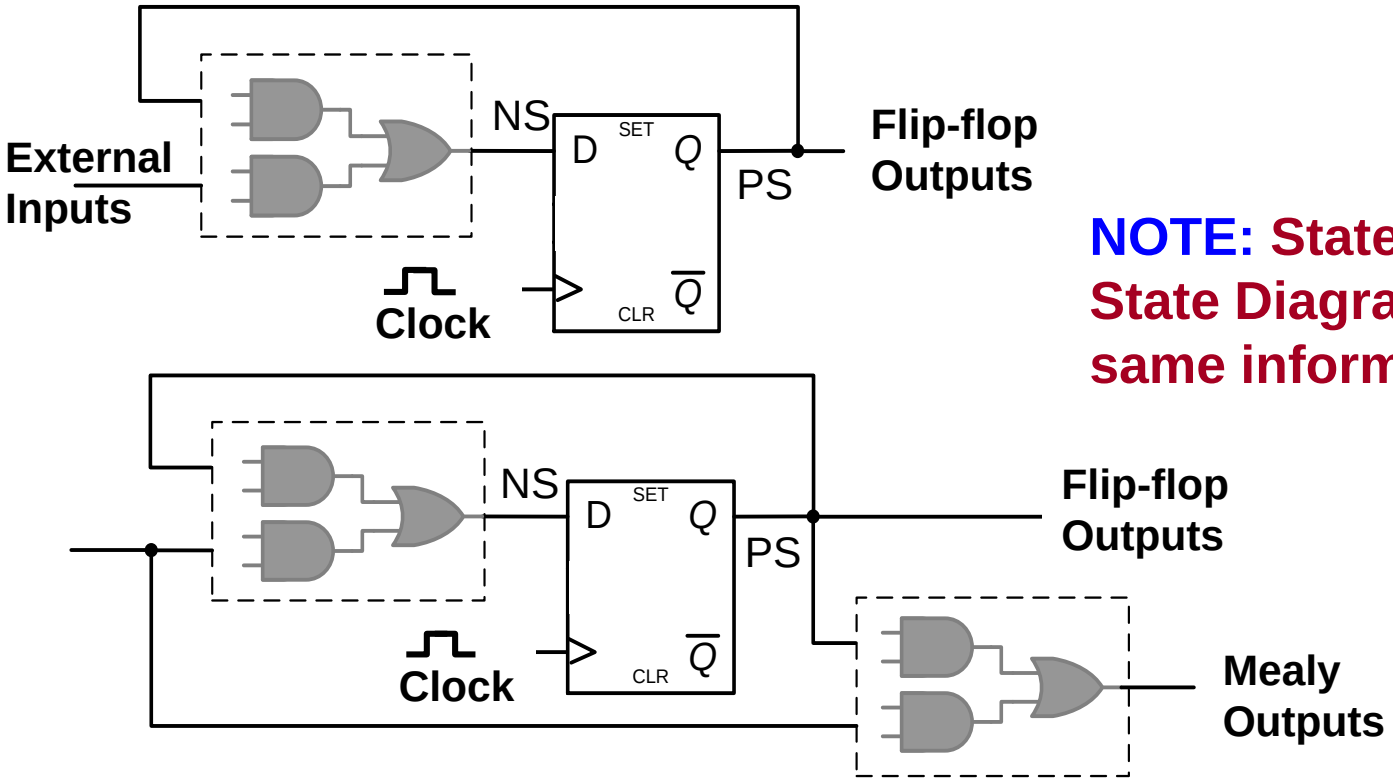


NOTE: State Tables and State Diagrams provide the same information.



Mealy Models

Mealy Model: Sequential Circuits in which outputs depend on the inputs and the states, two dimensional columns.

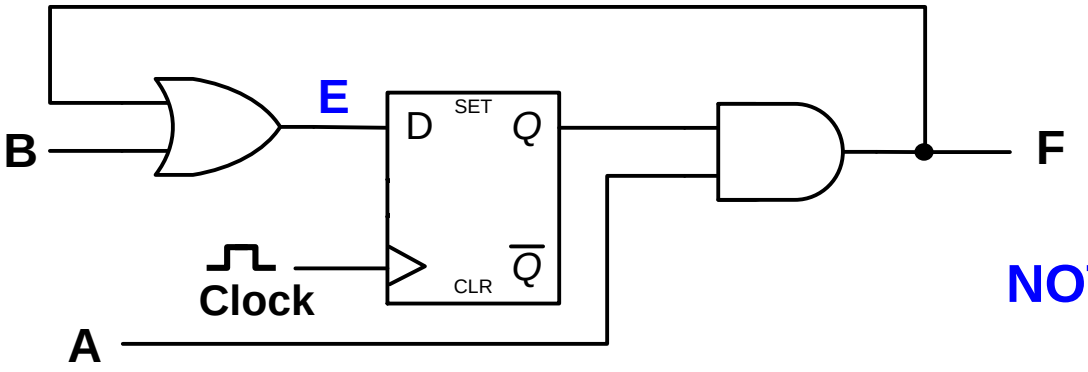


NOTE: State Tables and State Diagrams provide the same information.

Analysis

Analysis of Clocked Sequential Circuits

Starting with the Logic Diagram (circuit)



NOTE: This is a Mealy Model

Step 1) Write the state, input and output equations

Output equations F = Q A

Input equations E = F + B

State equations $Q(t+1) = Q^{+} = Q\,A + B$

NOTE:

- 2 inputs – A and B
- 1 Output - F
- 1 D type FF

Analysis of Clocked Sequential Circuits

Step 2) Complete the State Table

Q	Inputs		QA	Q^+	F
	A	B			
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	0	1	0
1	0	0	0	0	0
1	0	1	0	1	0
1	1	0	1	1	1
1	1	1	1	1	1

$Q(t+1) = Q^+ = Q\,A + B$

$F = Q\,A$

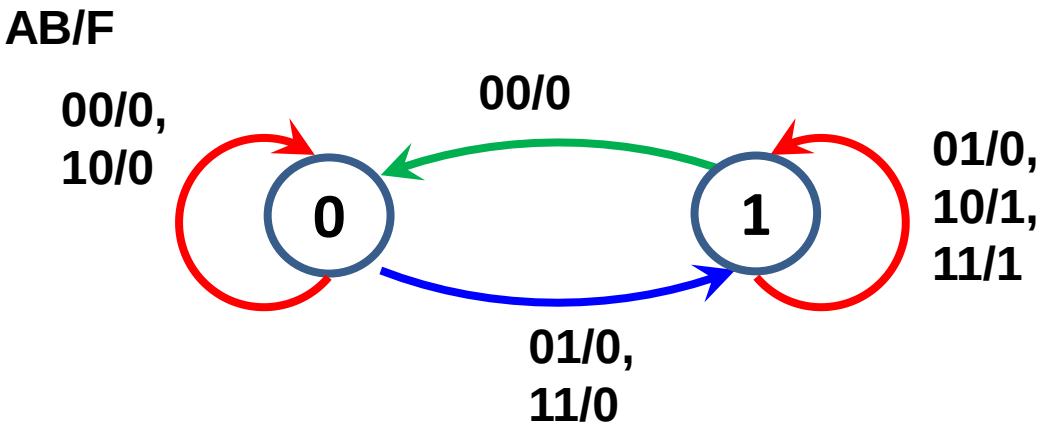
NOTE: The circled states are considered stable states since the state does not change when transitioning or graphically

AB/F

Analysis of Clocked Sequential Circuits

Step 3) Draw the State Diagram

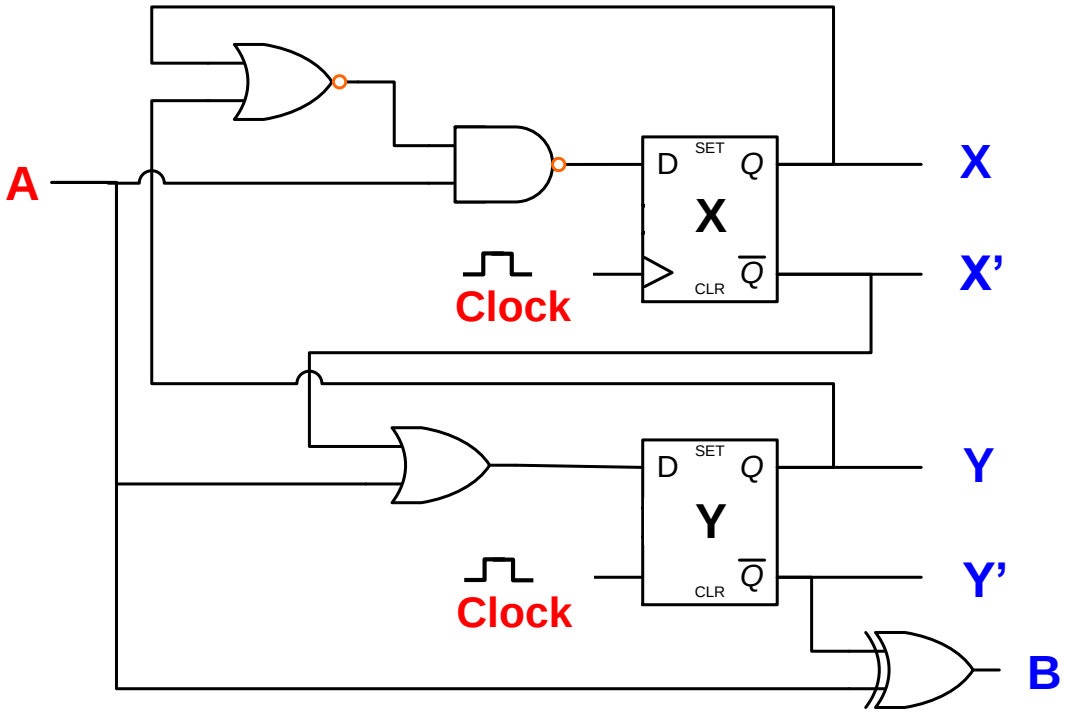
Q	Inputs		QA	Q^+	F
	A	B			
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	0	1	0
1	0	0	0	0	0
1	0	1	0	1	0
1	1	0	1	1	1
1	1	1	1	1	1



NOTE: There are 2 inputs so each state should have 2^2 outputs and there should be a total of 8 transitions in the diagram one for each row of the state table.

Practice Problem #1

Starting with the Logic Diagram (circuit)



NOTE: This is a typical quiz problem

Inputs: A, Clk

Outputs: X, X', Y, Y', B

Step 1) Write the state, input and output equations

Outputs Eq:

$B(A,X,Y) = A \oplus Y'$

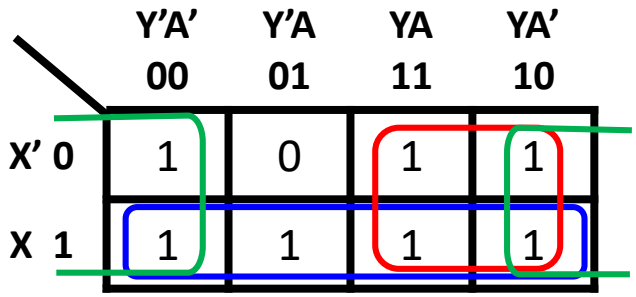
Input Eq:

$Y^{+}(A,X,Y) = A+X'$

$X^{+}(A,X,Y) = (((Y+X)'A)'$

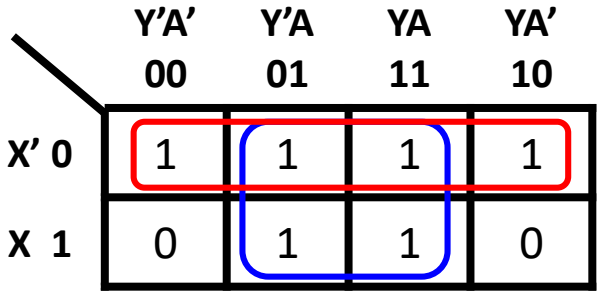
Practice Problem #1
State Table From Equations (1)

$X^+(X,Y,A) = (((Y+X)'A)'$
$= (((Y+X)')' + A'$
$= Y + X + A'$



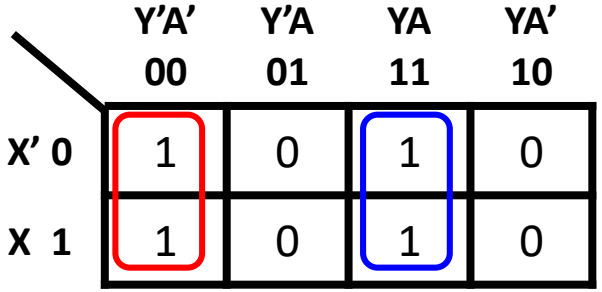
$X^+ = \Sigma\, m(0,2,3,4,5,6,7)$

$Y^+(X,Y,A) = A + X'$



$Y^+ = \Sigma\, m(0,1,2,3,5,7)$

$B^+(X,Y,A) = A \oplus (Y)'$
$= AY + A'Y'$



$B^+ = \Sigma\, m(0,3,4,7)$

Practice Problem #1
State Table From Equations (2)

Step 2) Complete the State Table

Present State		A	Next State		B
X	Y		X	Y	
0	0	0	1	1	1
0	0	1	0	1	0
0	1	0	1	1	0
0	1	1	1	1	1
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	0	0
1	1	1	1	1	1

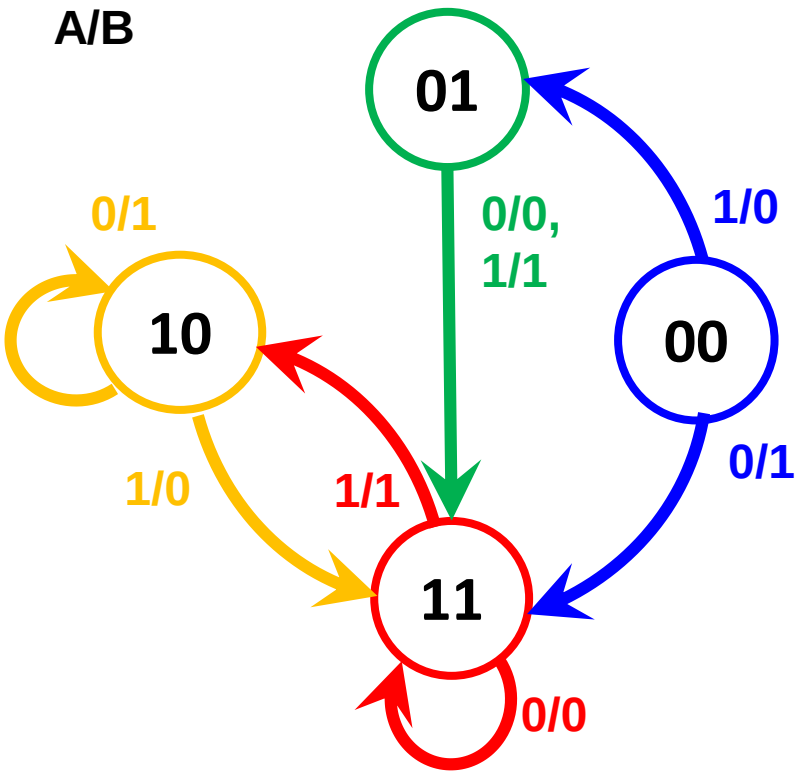
$X^+ = \Sigma\, m(0,2,3,4,5,6,7)$ $B^+ = \Sigma\, m(1,2,5,6)$

$Y^+ = \Sigma\, m(0,1,2,3,5,7)$

NOTE: The circled states are considered stable states since the state does not change when transitioning or graphically

Practice Problem #1
State Table From Equations (3)

Step 3) Draw the State Diagram



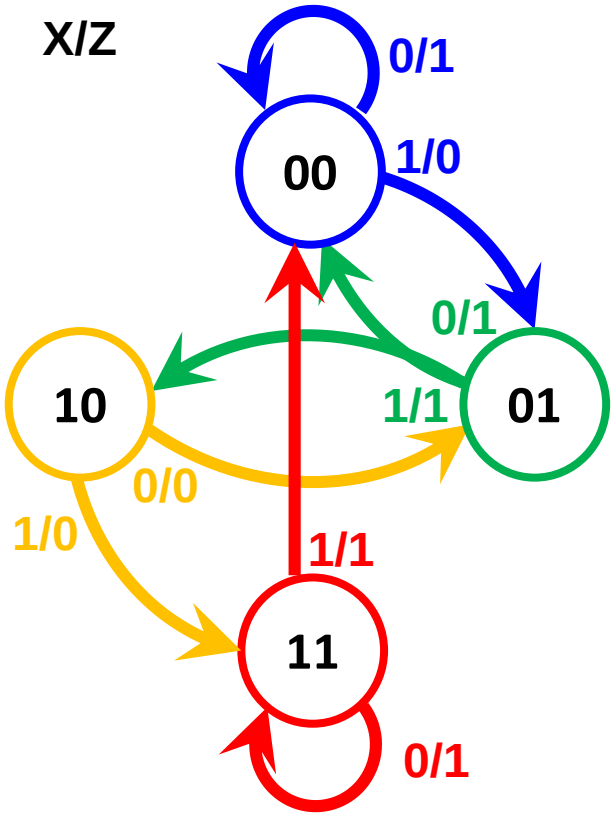
Present State		A	Next State		B
X	Y		X^+	Y^+	
0	0	0	1	1	1
0	0	1	0	1	0
0	1	0	1	1	0
0	1	1	1	1	1
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	0	0
1	1	1	1	1	1

Design

Design of Clocked Sequential Circuits

From verbal or written description use this information to generate (in this case the verbal statement said we need to use D flipflops (FF):

Step 1) Complete State Diagram or State Table



Present State			Next State		
B	A	X	B^+	A^+	Z
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	0	1
1	0	0	0	1	0
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	1

Logic Circuit Design

Step 2) Define the FFs inputs so that the State changes occur as specified by problem description. Two approaches:

1. **Know FF inputs, want to define the next state. Use Characteristic Table of FFs.**

2. **Know the transition, want to find the inputs that cause those transitions. Use Excitation Table (PS/NS) of FFs.**

Note:

A. Choose types of FFs to use

Number of FFs determined by number of states (4 or 2^2 states = 2 FF

Type: JK most flexible; SR or D for data transfer; T when complementing is involved. Most popular is the D FF.

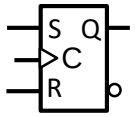
B. Notation to distinguish FF inputs in complex circuits (2 letter designations)

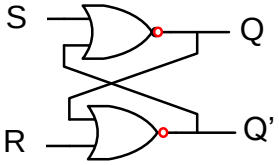
First letter refers to specific FF input (J, K, D, T, S, R)

Second letter refers to a FF identifier (A, B, C, etc)

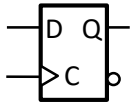
Logic Storage Devices

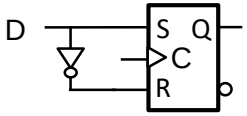
Characteristic Table



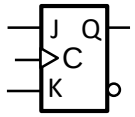


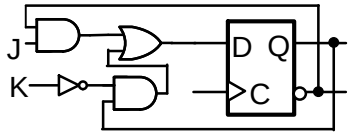
S	R	Q(t+1)	Operation
0	0	Q(t)	Hold
0	1	0	Reset
1	0	1	Set
1	1	?	Undefined



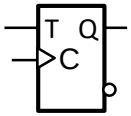


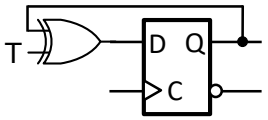
D	Q(t+1)	Operation
0	0	Reset
1	1	Set





J	K	Q(t+1)	Operation
0	0	Q(t)	Hold
0	1	0	Reset
1	0	$\overline{1}$	Set
1	1	Q(t)	Toggle





T	Q(t+1)	Operation
0	Q(t)	No Change
1	$\overline{Q(t)}$	Toggle

Excitation Table

$Q(t+1) = S + R'Q$

Q	Q^+	S	R	Operation
0	0	0	d	Hold
0	1	1	0	Set
1	0	0	1	Reset
1	1	d	0	Hold

$Q(t+1) = D$

Q^+	D	Operation
0	0	Reset
1	1	Set

$Q(t+1) = JQ' + K'Q$

Q	Q^+	J	K	Operation
0	0	0	d	Hold
0	1	0	d	Set
1	0	d	0	Reset
1	1	d	1	Hold

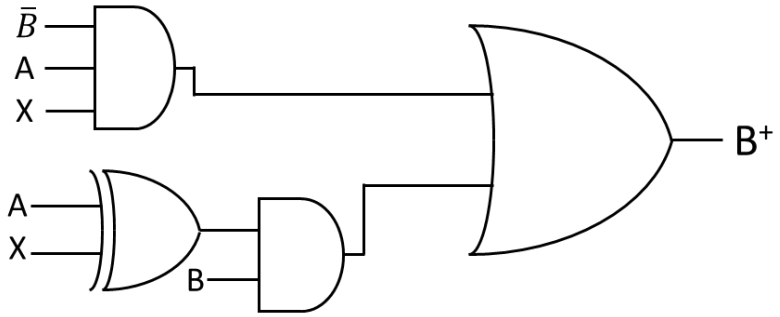
$Q(t+1) = Q \oplus T$

Q^+	T	Operation
Q(t)	0	Hold
$\overline{Q(t)}$	1	Toggle

Developing Flipflop Input Equations For B^+ and A^+

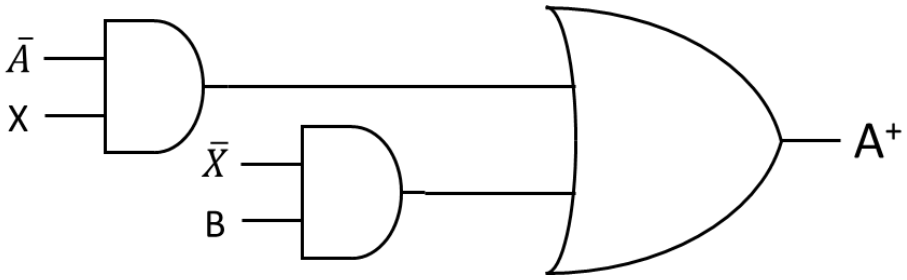
$B^+ = \bar{B}AX + B(\bar{A}X + A\bar{X})$

	AX 00	A'X 01	AX 11	AX' 10
B' 0	0	0	1	0
B 1	0	1	0	1



$A^+ = B\bar{X} + \bar{A}X$

	AX 00	A'X 01	AX 11	AX' 10
B' 0	0	1	0	0
B 1	1	1	0	1



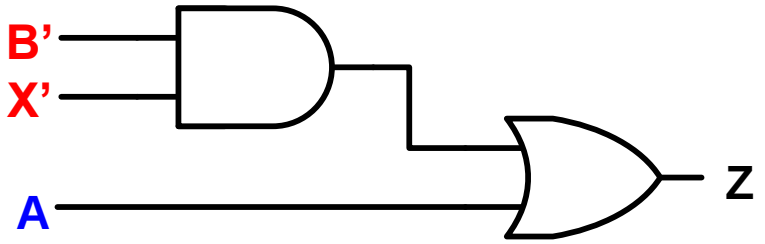
Developing the Output Equation

Present State			Next State		
B	A	X	B	A	Z
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	0	1
1	0	0	0	1	0
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	1

$Z = \Sigma\, m(0,2,3,6,7)$

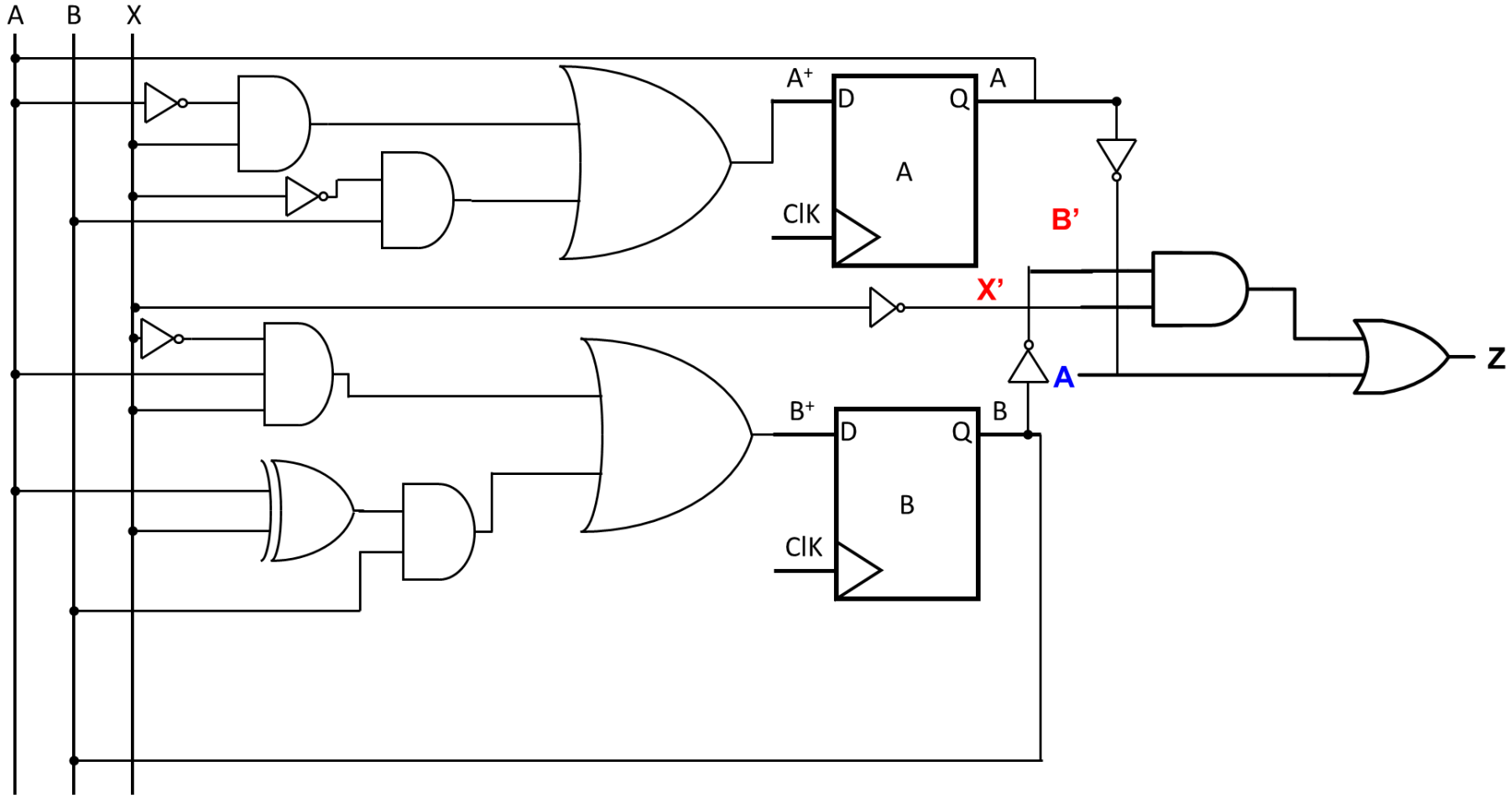
	A'X' 00	A'X 01	AX 11	AX' 10
B' 0	1	0	1	1
B 1	0	0	1	1

$Z = B'X' + A$



Assembling Circuit

Step 3) Draw Logic Diagram



Q&A