Name: _____ CWID: _____ Date: _____

CALIFORNIA STATE UNIVERSITY, FULLERTON

Computer Engineering

EGCP 180 – Digital Logic and Computer Structures (Fall 2017)

Midterm Exam 2(Total Points = 45)

(Time allowed: 9:00 — 11:00 AM)

Academic Dishonesty Policy

In line with University policies, the Computer Engineering program supports a strict and well-defined policy against academic dishonesty. Thus, to assure a fair and equitable testing environment for all students, there will be zero tolerance during exam for any of the following:

- Cheating of any type (looking at or copying another student's answers) or helping another student with answers.
- Use of notes, phones, or other aids (other than that allowed by instructor)
- Talking or texting during exams
- Leaving the classroom during the exam (without permission)

Consequences for violating these policies will be a "zero" on the exam at a minimum, with the possibility of an F in the course.

Only one page of handwritten notes (two side), pens/pencils, erasers, and a calculator (shouldn't be necessary) are allowed with the exam.

Normally, full credit is given only if work is shown when appropriate.

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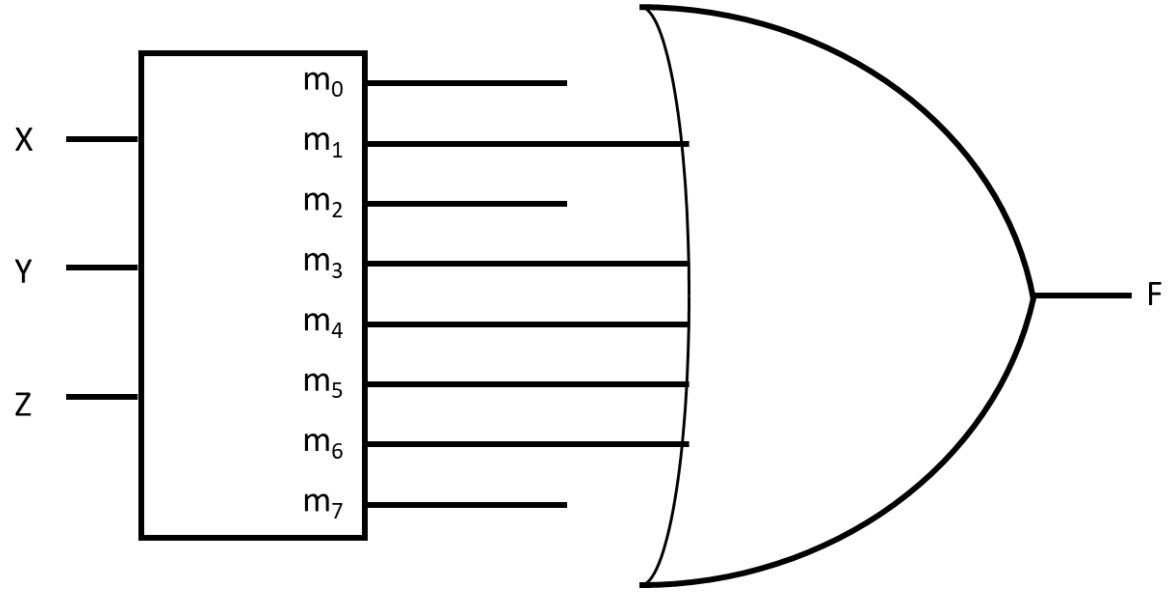
1. **(10 Points) Decoder**
   Design a circuit for the function F(X, Y, Z)= ∏M(0,2,7) with a 3-to-8 decoder with active high outputs.



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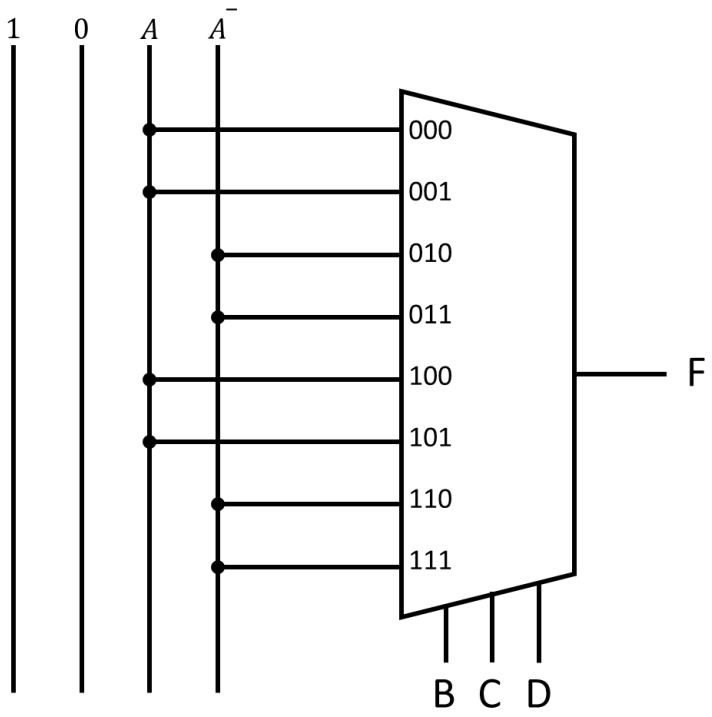
2. (10 Points) Multiplexer

Obtain a MUX design for the F(A, B, C, D) = ∑m (2, 3, 6, 7, 8, 9, 12, 13) such that B, C, and D are connected to the control inputs of Mux. Connect 1's, 0's, A, and $\bar{A}$ to each data inputs. (Show your steps)

A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0



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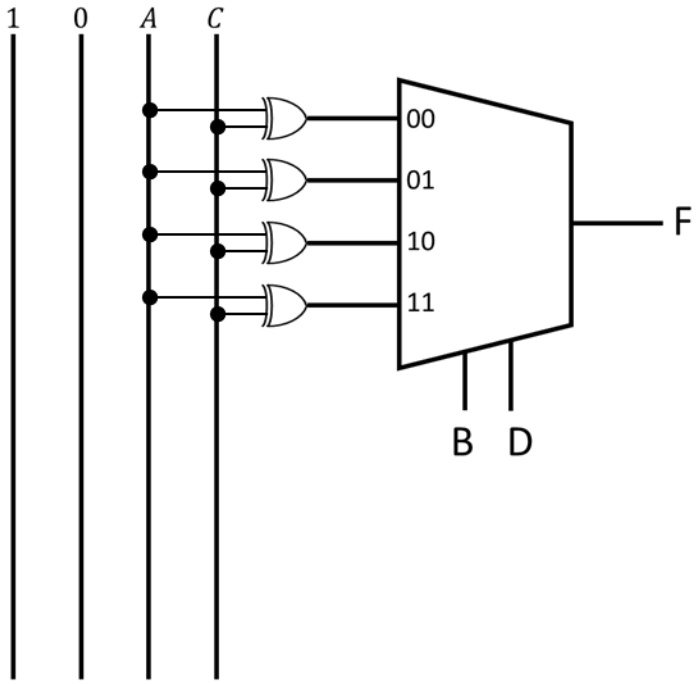
3. **(10 Points) Extra Credit (Optional)**
   Repeat question 2 but this time use technique 2 which uses K-map such that B and D are connected to the control inputs of Mux. Connect 1's, 0's, A and C to each data inputs. (Show your steps)



AC\BD	00	01	10	11
00	0	0	0	0
01	1	1	1	1
10	1	1	1	1
11	0	0	0	0

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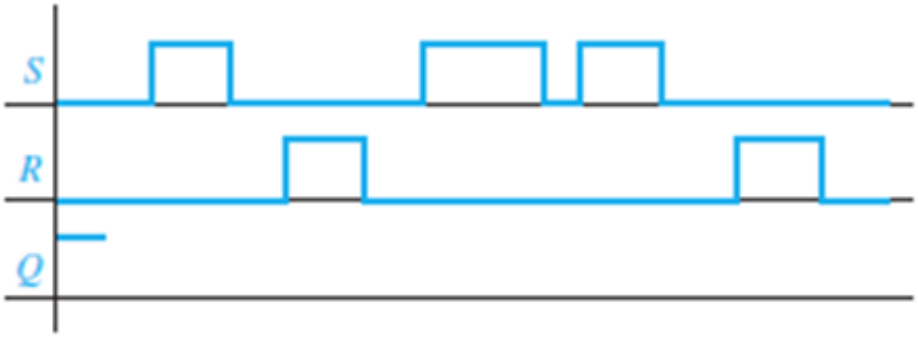
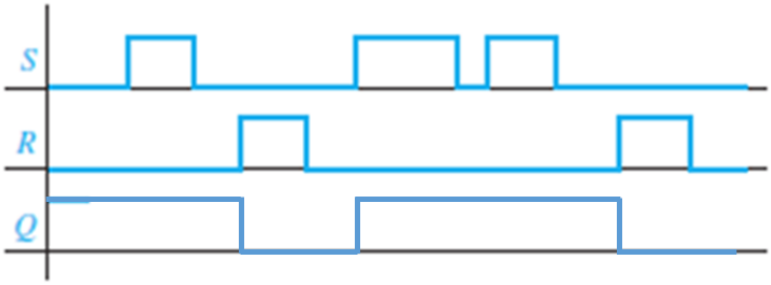
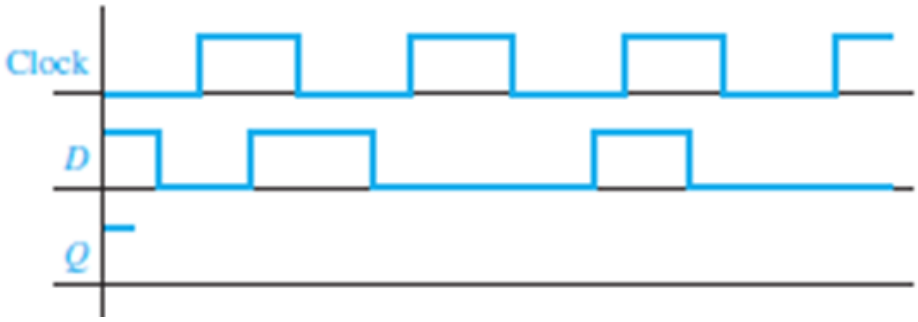
4. (10 Points) Latches and Flip Flop

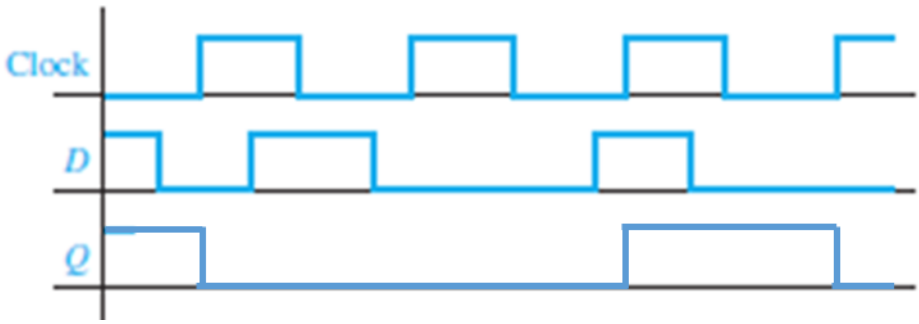
a) Complete the following timing diagram for an NOR based S-R latch. Assume Q begins at 1.





b) Complete the following diagrams for the rising-edge-triggered D flip-flop. Assume Q begins at 1.





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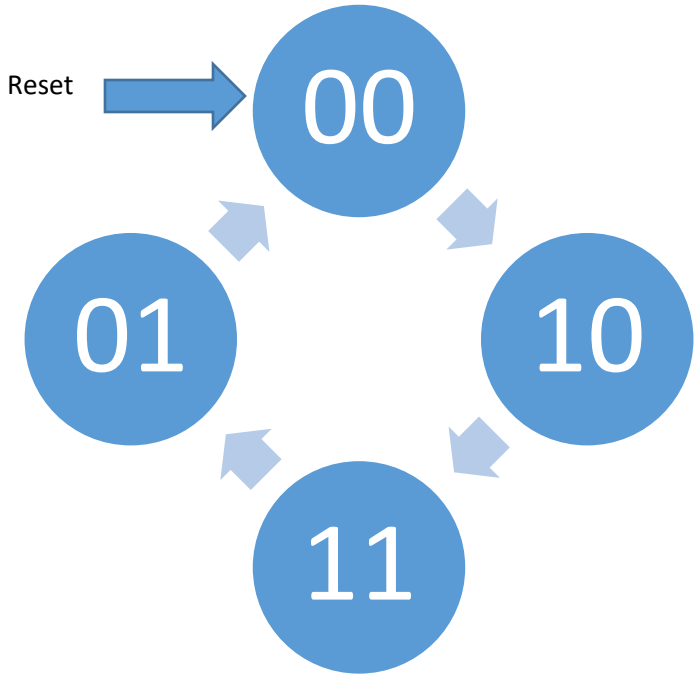
5. (15 Points) Counter Design

Design a two bit counter shown below



a) Fill the state table:

Present State		Next State	
Q1	**Q0**	**$Q1^+$**	**$Q0^+$**
0	0	1	0
0	1	0	0
1	0	1	1
1	1	0	1

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b) Drive the logic equation of

$Q1^+ = \overline{Q0}$

$Q0^+ = Q1$

c) Complete the logic diagram based on the logic equation