CALIFORNIA STATE UNIVERSITY
FULLERTON™

EGEC 281: Designing with VHDL

Fall 2024

Lecture 7: Midterm Exam No 1 Review

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Midterm Exam No 1

Attempts: 27 out of 27

+1

Discrimination Index ?

Midterm Exam No 1 should be held on

_____

October16, 2024	5 respondents	**19 %**	✓
October 23, 2024	22 respondents	81 %	

19% answered correctly

Midterm Exam No 1

- Day: 23 October 2024
- Time: 11:00 AM – 12: 45 pm
- Lecture Slides from 1 to 5
- Bring a cheat-sheet of one page (A4 Size), pen, pencil and calculator.

Conversion

- 8-4-2-1 Code (BCD)
- 6-3-1-1 Code
- Excess-3 Code
- 2-out of 5 Code
- Gray Code
- Binary
- Octal
- Hexadecimal

Arithmetic Operations

- Adding two Binary, Octal, Hexadecimal number
- Subtraction of two Binary, Octal, Hexadecimal number
- Subtraction using 1’s and 2’s Complement
- Multiplication
- Division

Boolean Algebra

- Boolean Functions
- Truth Table
- Logical Circuits
- Minterm
- Maxterm
- K-Map

Data Conversion

1. (20 Points) Do the following

a) Carry out the conversion required to complete the columns. (Show the steps)

BINARY	OCTAL	DECIMAL	HEXADECIMAL
_____	_____	757.25	_____

b) Find the 1's complement, 2's complement and sign of the number based on the 8-bit signed number shown below. (Show the steps)

Number	1's Complement	2's Complement	Sign
11100110.101			
01101100			

c) Convert to base 6: $3BA.24_{14}$ (do all the arithmetic in decimal).

Arithmetic Operation

(25 Points) Arithmetic Operation

Calculate the following. (Show the steps)

a) $(110110)_2$ plus $(11101)_2$

b) $(11110100)_2$ minus $(1000111)_2$ using 1's complement and 2's complement

c) $(1111)_2$ times $(1010)_2$

d) $(101101)_2$ divided by $(110)_2$

Boolean Algebra

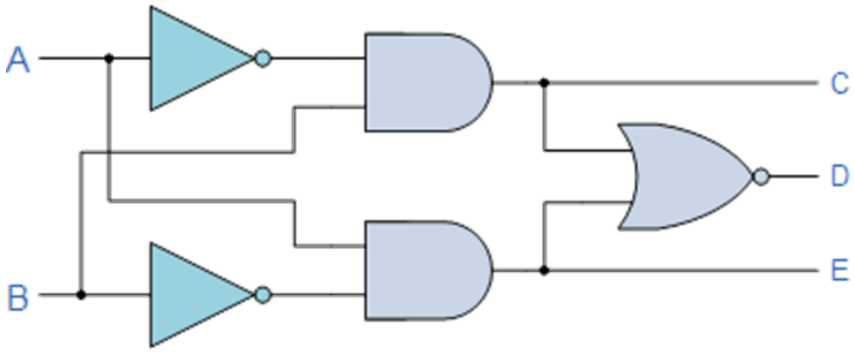
(30 Points) Max and Min term

From a 4-bit Instruction Register we have the following Truth Table (instruction decoding). a) Express the Boolean functions using minterms and maxterms representations. b) Provide the Boolean functions using Sum of Products (SOP), and Product of Sums (POS) using K-map c) Based on the Boolean expression obtained in part b) draw the logic circuit for SOP and POS.

A	B	C	D	F1
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

VHDL

- Designing simple Combination circuit.
- Identifying the waveform
- Note: I will never ask to write testbench in exam




```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity Ques1 is
    Port ( A,B : in  STD_LOGIC;
           C,D, E : out  STD_LOGIC);
end Ques1;

architecture Behavioral of Ques1 is

signal _________________ : _______________ ;

begin

_____________________________________________

_____________________________________________

_____________________________________________


end Behavioral;
```

Q&A