EGEC281 – FALL 2024

LAB 4

MULTIPLEXER

Designing with VHDL
Experiment 4A

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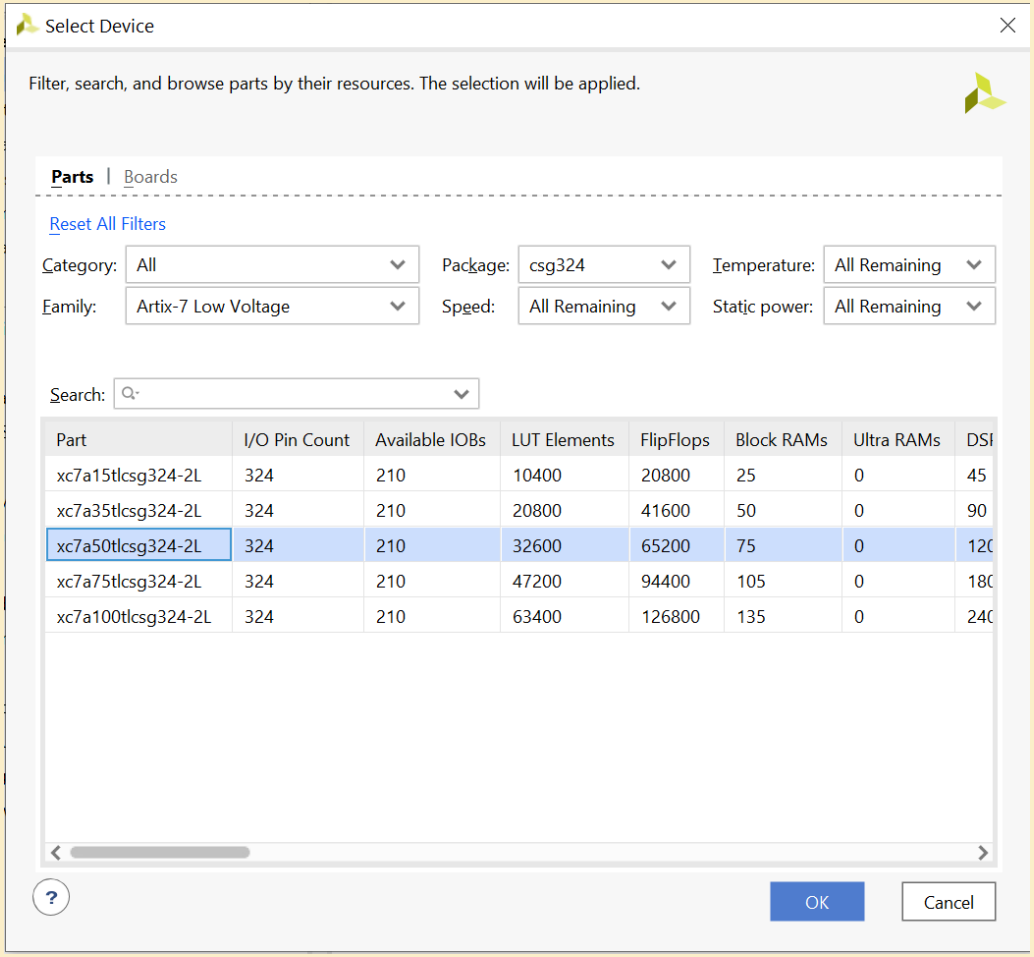
LEARNING OBJECTIVES

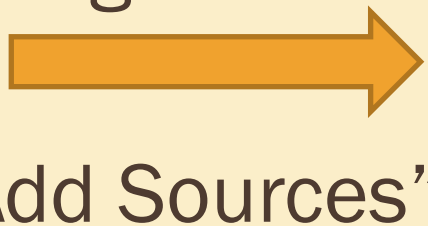
- Project 4A- Implement Binary to Hexadecimal Using a Multiplexer

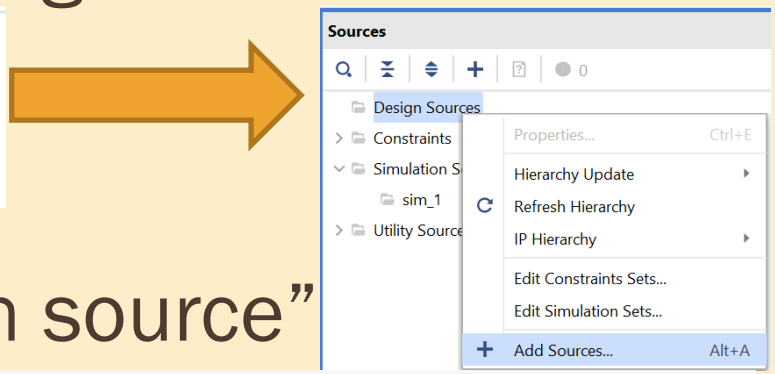
FPGA SETUP IN XILINX VIVALDO



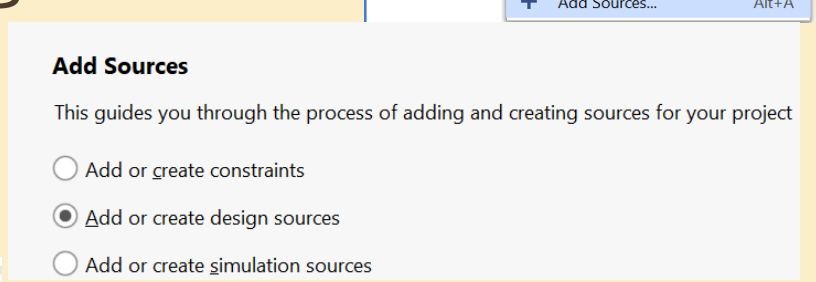
LAB 4 PROJECT B – ADDING FILE IN A PROJECT

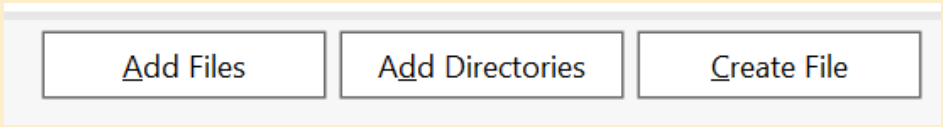
- Select Design Sources and right click on mouse.





- Select “Add Sources”
- Select “Add or create design source”
- Click “Next”
- Click “Add Files”

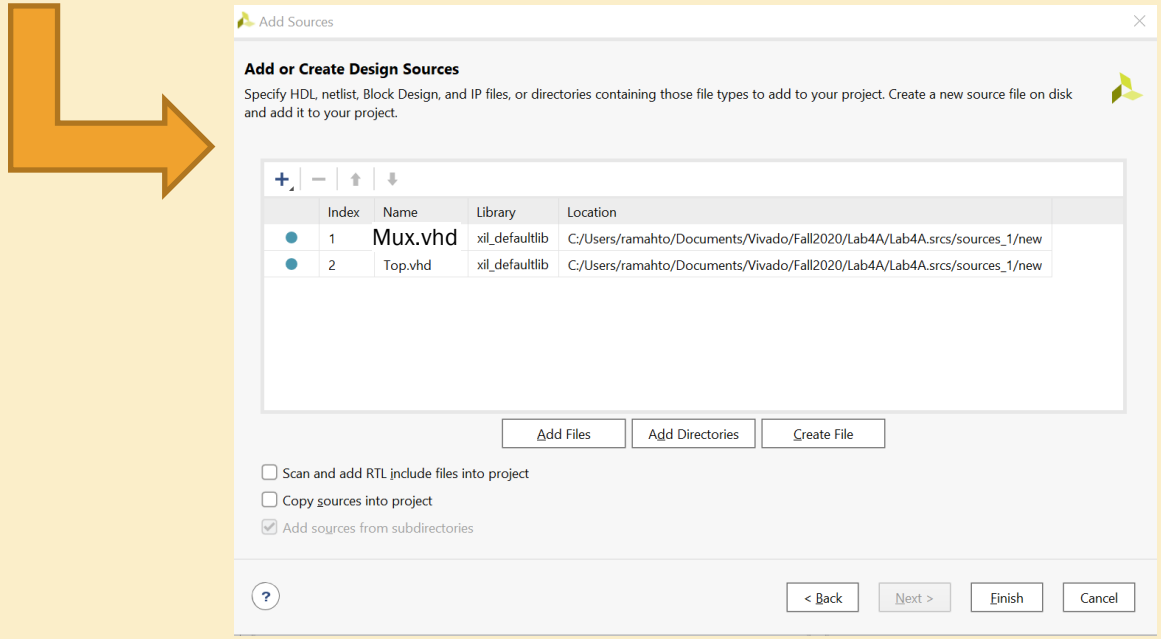




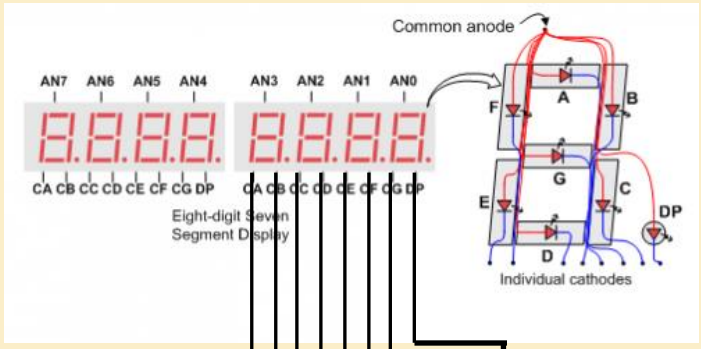
- Select the, “Decoder.vhd” and Top.vhd

LAB 4 PROJECT A – ADDING FILE IN A PROJECT

- Select the, “Mux.vhd” and Top.vhd
- Click “Finish”



LAB 4 PROJECT A – SCHEMATIC



Cath(0)

Cath(1)

Cath(2)

Cath(3)

Cath(4)

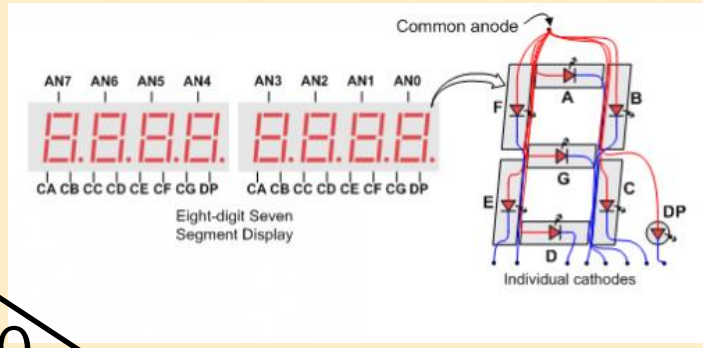
Cath(5)

Cath(6)

Cath(7)

LAB 4 PROJECT A – SCHEMATIC

W	X	Y	Z	A
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0



PROJECT 4A BINARY TO HEXADECIMAL ON 7-SEGMENT DISPLAY USING MULTIPLEXER

- 4 Inputs (Switches), 8 bit Cathode and 8 bit Anode Outputs.
- Based on the 4-bit inputs, the 7-segment display should show the hexadecimal equivalent of the input.

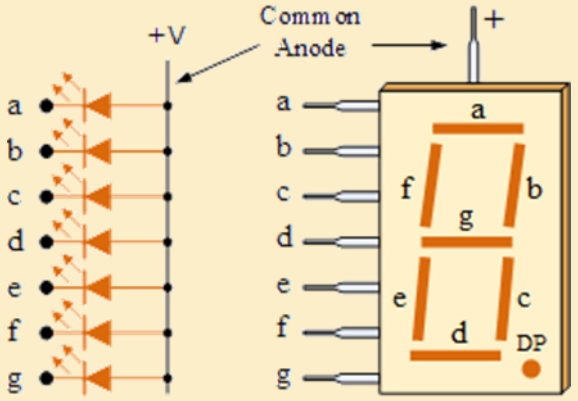
LAB 4 PROJECT A BINARY TO HEXADECIMAL

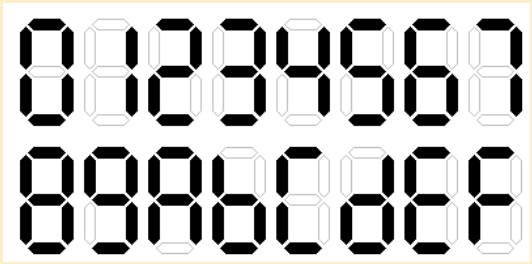
1. Create a new project. Name it Lab4A.
   - Download the VHDL Template files (Top.vhd and Mux.vhd) provided and add them in your project
   - Complete the VHDL for multiplexer in "Mux.vhd" based on either Tech #0, Tech#1, or Tech#2.
2. Add the testbench file, Mux_TB.vhd provided to generate the waveforms.
3. Verify the simulation output.
4. Complete the "Top. Vhd" based on the Tech#0, Tech#1, or Tech#2 used in part 1.
5. Add the testbench file, Mux_TB.vhd provided, to generate the waveforms.
6. Verify the simulation output.
7. Create a XDC for Lab4B; Assign:
   - Input signals W, X, Y and Z: 4 switches
     - Input W ⇨ R15
     - Input X ⇨ M13
     - Input Y ⇨ L16
     - Input Z ⇨ J15
   - Output signals Cath (8 bits) to cathode ports,
   - Output An (8 bits) to anode ports.
8. Generate and download program file (.bit) to FPGA
9. Verify that the hardware works as expected.

An	Loc	Cath	Loc
An(0)	J15	Cath(0)	T10
An(1)	J18	Cath(1)	R10
An(2)	T9	Cath(2)	K16
An(3)	J14	Cath(3)	K13
An(4)	P14	Cath(4)	P15
An(5)	T14	Cath(5)	T11
An(6)	K2	Cath(6)	L18
An(7)	U13	Cath(7)	H15

LAB 4 PROJECT B BINARY TO HEXADECIMAL

W	X	Y	Z	A	B	C	D	E	F	G	DP
0	0	0	0	0	0	0	0	0	0	1	1
0	0	0	1								
0	0	1	0								
0	0	1	1								
0	1	0	0								
0	1	0	1								
0	1	1	0								
0	1	1	1								
1	0	0	0								
1	0	0	1								
1	0	1	0								
1	0	1	1								
1	1	0	0								
1	1	0	1								
1	1	1	0								
1	1	1	1								





Note: Please note Cathode is active low

LAB REPORT

- Cover page:
  - Course Title
  - Lab Number, Letter
  - Team Names
- Project 4A:
  - VHDL (Mux.vhd and Top.vhd)
  - Logic Diagram
  - Truth Table
  - Hand-Calculation
  - Simulation Code (Mux_TB.vhd and Top_TB.vhd), Waveform
  - XDC
  - Picture of Implementation
- Summary paragraph
  - Work completed
  - Any problems
  - Helpful Hints
  - Suggested Improvements