Name: Key _____ CWID: _____ Date: _____

CALIFORNIA STATE UNIVERSITY, FULLERTON

Computer Engineering

EGCP 281 – Designing Using VHDL
(FALL 2017)

Mid-term Exam 1 (Total Points = 85)

Academic Dishonesty Policy

In line with University policies, the Computer Engineering program supports a strict and well-defined policy against academic dishonesty. Thus, to assure a fair and equitable testing environment for all students, there will be zero tolerance during exam for any of the following:

- Cheating of any type (looking at or copying another student's answers) or helping another student with answers.
- Use of notes, phones, or other aids (other than that allowed by instructor)
- Talking or texting during exams
- Leaving the classroom during the exam (without permission)

Consequences for violating these policies will be a "zero" on the exam at a minimum, with the possibility of an F in the course.

Only one page of handwritten notes (two side), pens/pencils, erasers, and a calculator (shouldn't be necessary) are allowed with the exam.

Normally, full credit is given only if work is shown when appropriate.

Perfect VHDL syntax is not required, but your code should still be correctly written. Just small syntax errors, like a missing semicolon, will not be penalized.

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1. (20 Points) Do the following

a) Carry out the conversion required to complete the columns. (Show the steps)

BINARY	OCTAL	DECIMAL	HEXADECIMAL
10111101.01	1365.2	757.25	2F5.4

$2\overline{)757}\,(378,\ -756,\ 1$

$2\overline{)378}\,(189,\ -378,\ 0$

$2\overline{)189}\,(94,\ -188,\ 1$

$2\overline{)94}\,(47,\ -94,\ 0$

$2\overline{)47}\,(23,\ -46,\ 1$

$2\overline{)23}\,(11,\ -22,\ 1$

$2\overline{)11}\,(5,\ -10,\ 1$

$2\overline{)5}\,(2,\ -4,\ 1$

$2\overline{)2}\,(1,\ -2,\ 0$

$2\overline{)1}\,(0,\ 0,\ 1$

$0.25 \times 2 = 0.5$

$0.5 \times 2 = 1.0$

00|011 |10|10|1.010

1 3 6 5.2

00|011 |101|01.0100

2F 5 4

b) Find the 1's complement, 2's complement and sign of the number based on the 8-bit signed number shown below. (Show the steps)

Number	1's Complement	2's Complement	Sign
11100110.101	00011001.010	00011001.011	-ve
01101100			+ve

c) Convert to base 6: $3BA.24_{14}$ (do all the arithmetic in decimal).

$3BA.24_{14} = (752.1633)_{10} = (3252.0513)_6$

$3 \times 14^2 + 11 \times 14 + 10 \times 14^0 + \frac{2}{14} + \frac{4}{14^2}$

$6\overline{)752}\,(125,\ -750,\ 2$

$6\overline{)125}\,(20,\ -120,\ 5$

$6\overline{)20}\,(3,\ -18,\ 2$

$6\overline{)3}\,(0,\ 0,\ 3$

$0.1633 \times 6 = 0.9798$

$0.9798 \times 6 = 5.8788$

$0.8788 \times 6 = 5.2728$

$0.2728 \times 6 = 1.6368$

$0.6368 \times 6 = 3.8208$

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2. (25 Points) Arithmetic Operation

Calculate the following. (Show the steps)

a) $(110110)_2$ plus $(11101)_2$

```
  1 1 1
  1 1 0 1 1 0
+   1 1 1 0 1
-------------
1 0 1 0 0 1 1
```

b) $(11110100)_2$ minus $(1000111)_2$ using 1's complement and 2's complement

01000111 ⇒ 10111000 ⇒ 10111001

1's Complement — 2's Complement

Subtraction using 2's Complement

```
    1 1 1
  1 1 1 1 0 1 0 0
+ 1 0 1 1 1 0 0 1
-----------------
1 0 1 0 1 1 0 1
```

Subtraction using 1's Complement

```
    1 1 1
  1 1 1 1 0 1 0 0
+ 1 0 1 1 1 0 0 0
-----------------
1 0 1 0 1 1 0 0
        +     1
-----------------
  1 0 1 0 1 1 0 1
```

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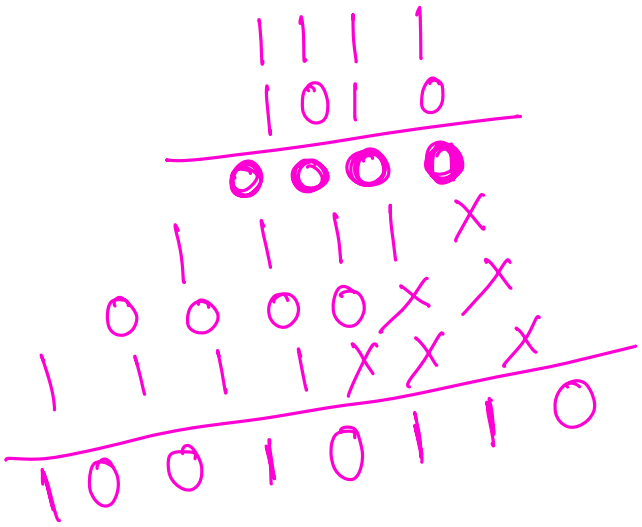
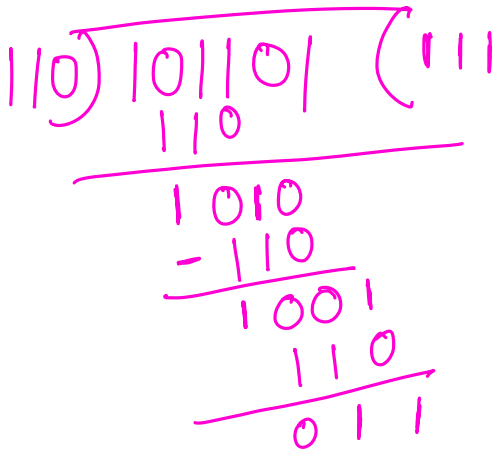
c) $(1111)_2$ times $(1010)_2$



d) $(101101)_2$ divided by $(110)_2$



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3. (30 Points) Max and Min term

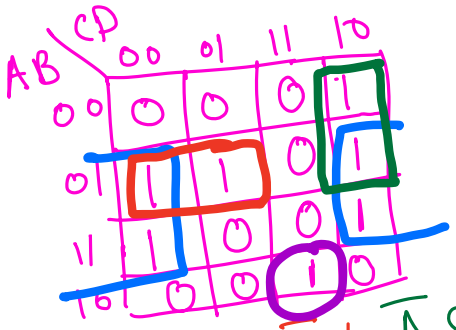
From a 4-bit Instruction Register we have the following Truth Table (instruction decoding). a) Express the Boolean functions using minterms and maxterms representations. b) Provide the Boolean functions using Sum of Products (SOP), and Product of Sums (POS) using K-map c) Based on the Boolean expression obtained in part b) draw the logic circuit for SOP and POS.

A	B	C	D	F1	
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	1	2
0	0	1	1	0	3
0	1	0	0	1	4
0	1	0	1	1	5
0	1	1	0	1	6
0	1	1	1	0	7
1	0	0	0	0	8
1	0	0	1	0	9
1	0	1	0	0	10
1	0	1	1	1	11
1	1	0	0	1	12
1	1	0	1	0	13
1	1	1	0	1	14
1	1	1	1	0	15

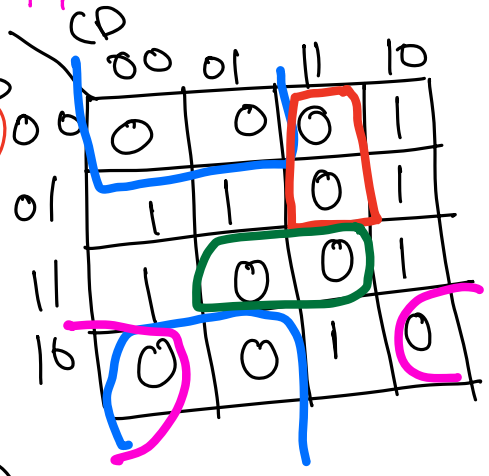
a) $Minterm = \Sigma m(2,4,5,6,11,12,14)$

$Maxterm = \Pi M(0,1,3,7,8,9,10,13,15)$

b)

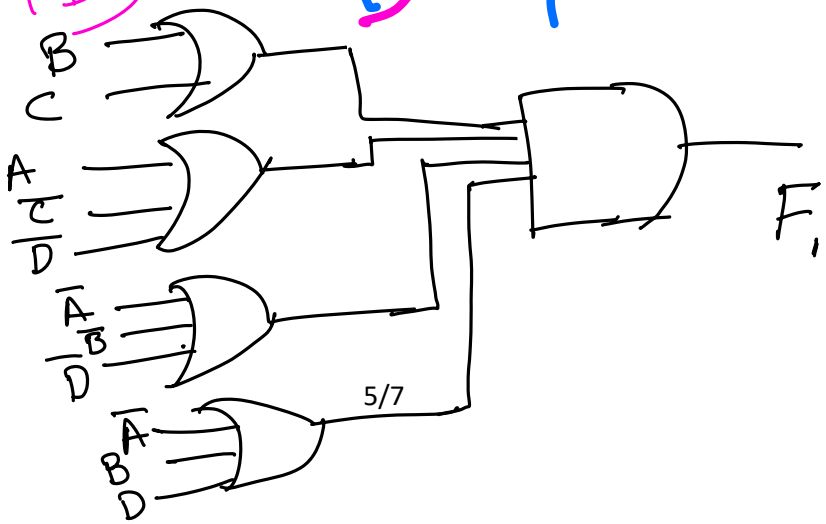


$F_1 = B\bar{D} + \bar{A}B\bar{C} + \bar{A}C\bar{D} + A\bar{B}CD$



$F_1 = (B + C)(A + \bar{C} + \bar{D})(\bar{A} + \bar{B} + \bar{D})(\bar{A} + B + D)$

c) POS



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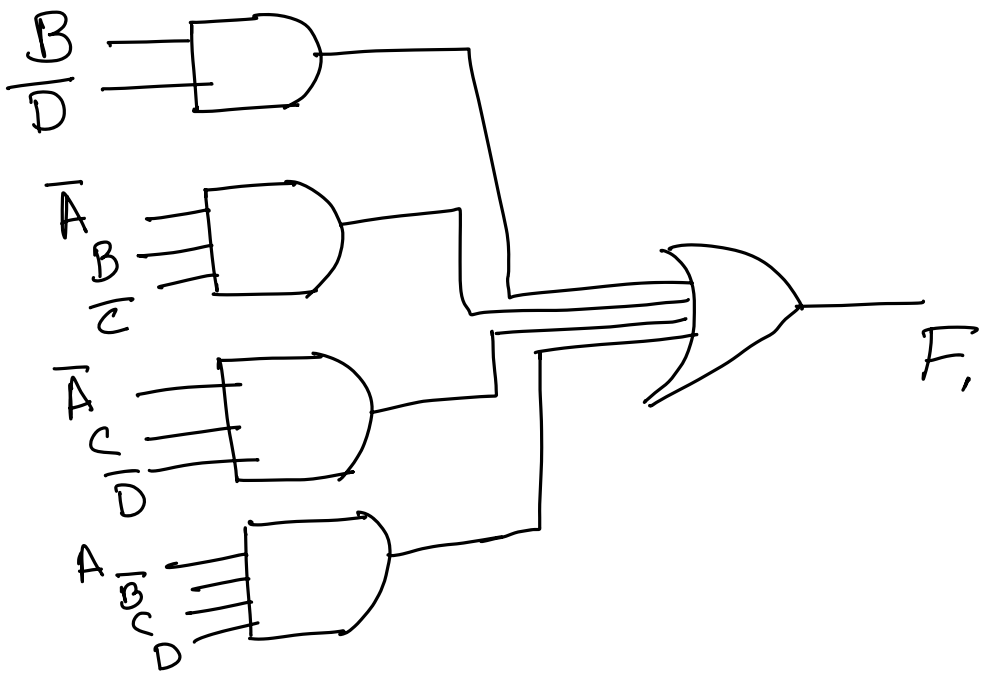

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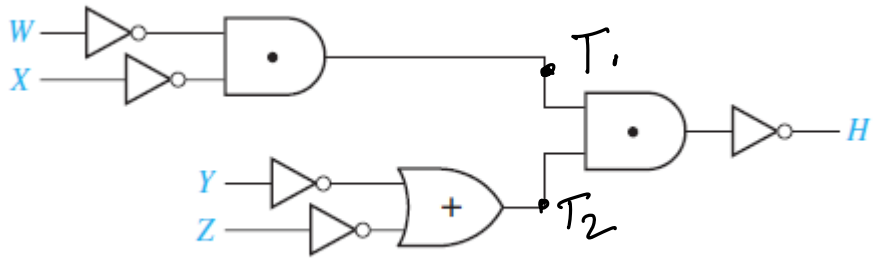
4. (10 Points) Combination Digital Circuit

For the combination circuit shown in the figure below fill the VHDL code




```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity Exam_Q5 is
    Port ( W, X, Y, Z : in std_logic;
           H : out std_logic);
end Exam_Q5;

architecture Behavioral of Exam_Q5 is
Signal T1, T2: std_logic := '0';

begin
T1 <= (not(W) and not(X));
T2 <= (not(Y) or not(Z));
H <= not(T1 and T2);


end Behavioral;
```