CALIFORNIA STATE UNIVERSITY
FULLERTON™

EGCP 281: Designing with VHDL

Fall 2024

Lecture 10: Bistable Memory Devices

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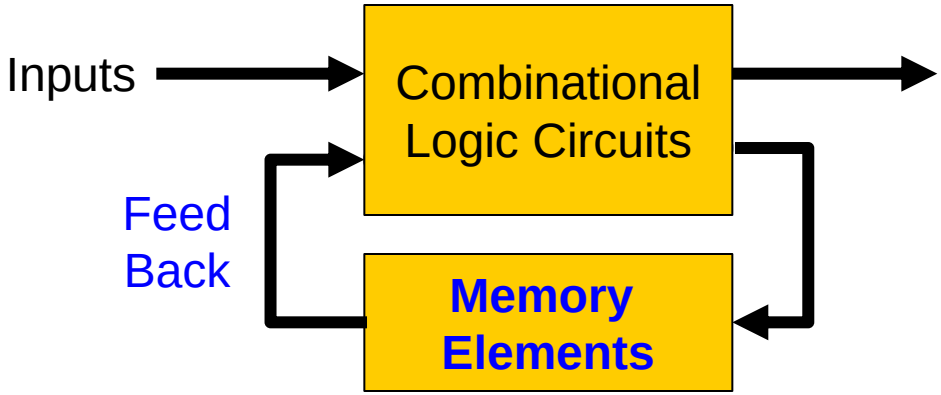
Sequential Circuits and Bistable Memory Devices

Two Types of Logic Circuits: Combinational

1. **Combinational – outputs determined directly from present combination of inputs. Previous inputs do not matter**

2. **Sequential – outputs determined directly from present AND previous inputs inputs. Previous inputs does matter**



Flip-Flops and Latches

We say a circuit has feedback if the output of one of the gates is connected back into the input of another gate in the circuit so as to form a closed loop.

Sequential Circuits

Sequential Circuits are specified by:

- **Inputs**
- **Outputs**
- **Internal states (past output values)**

Two types of sequential circuits:

1)Asynchronous: output can be affected at any point in time by changes in input variables.

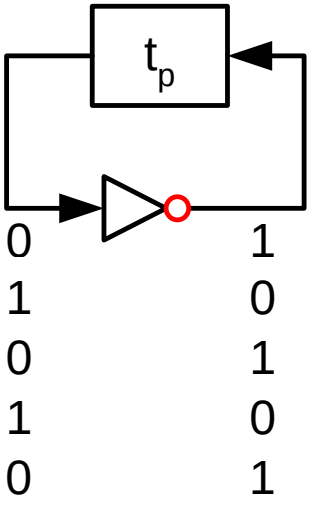
Ex. storage element = time delay device Flip-Flop

2)Synchronous: outputs are changed only at discrete instants of time.

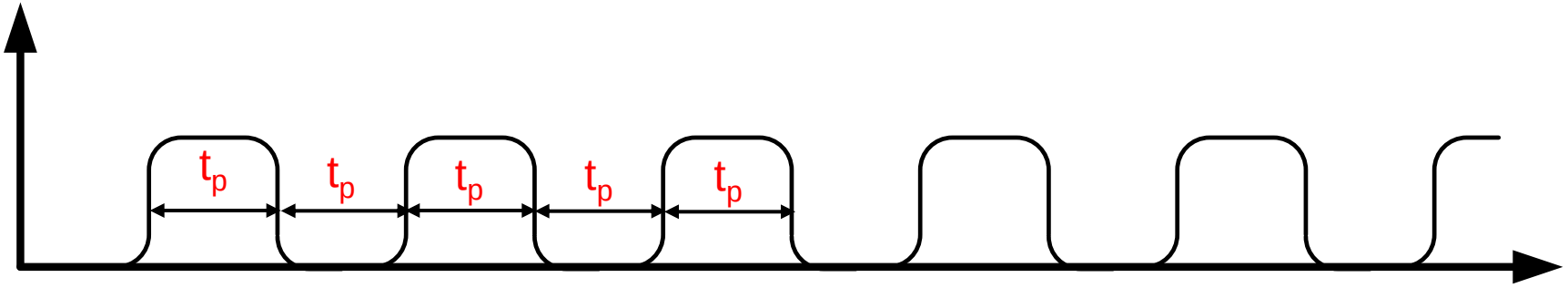
Ex. storage element = clocked Flip-Flop

Concept of Feedback

Example feedback circuit with no stable states.
Oscillator or Clock signal.

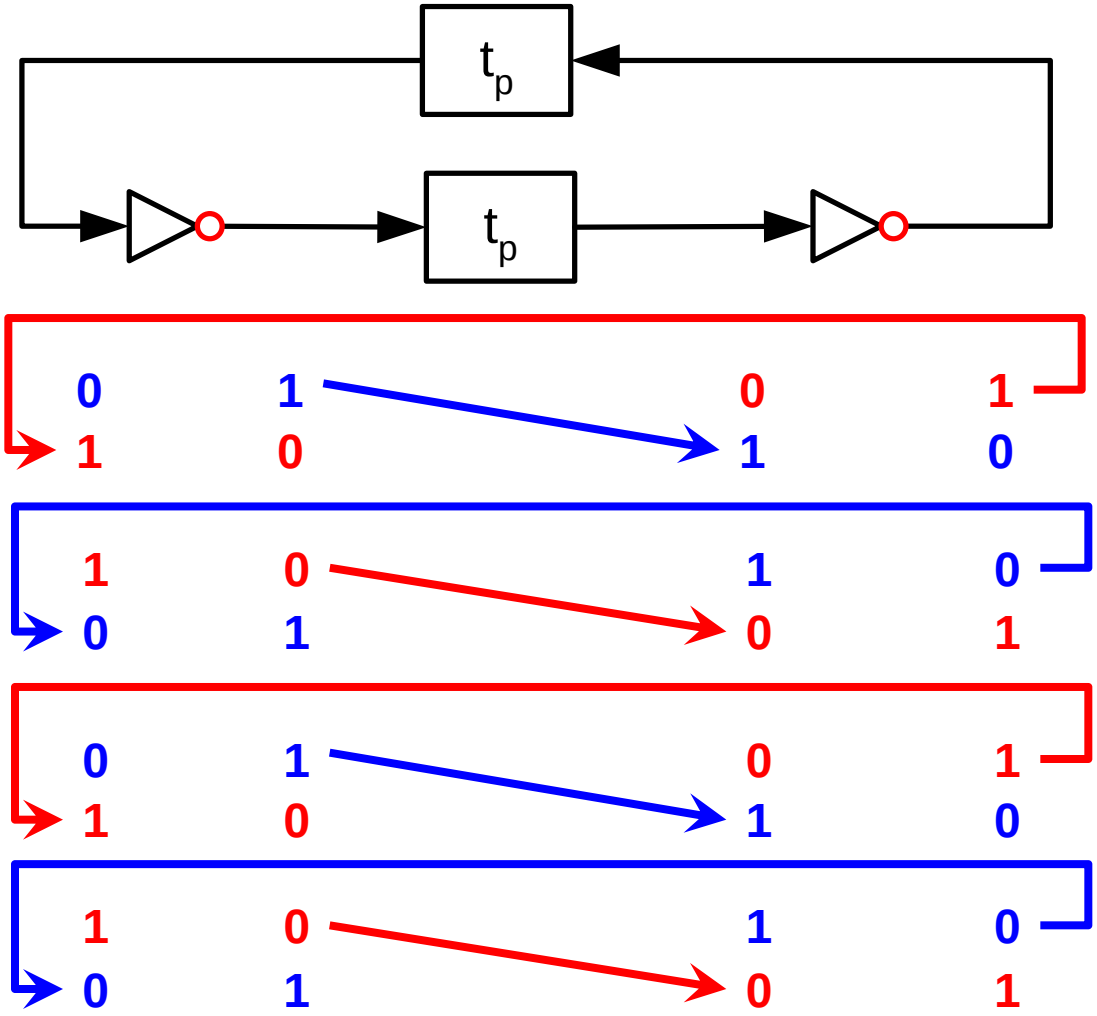


t_p (propagation delay time) = time it takes a signal applied at the its input to travel from the input to the output.



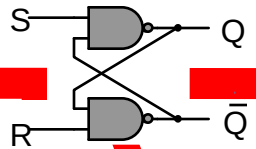
Bistable Feedback

Bistable means that there are two stable states, allowing these devices to store, save, or capture the value for a logic 1 or logic 0.



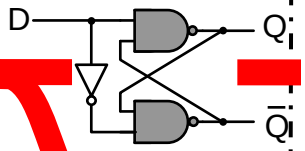
Memory Storage Devices

Allows for data storage



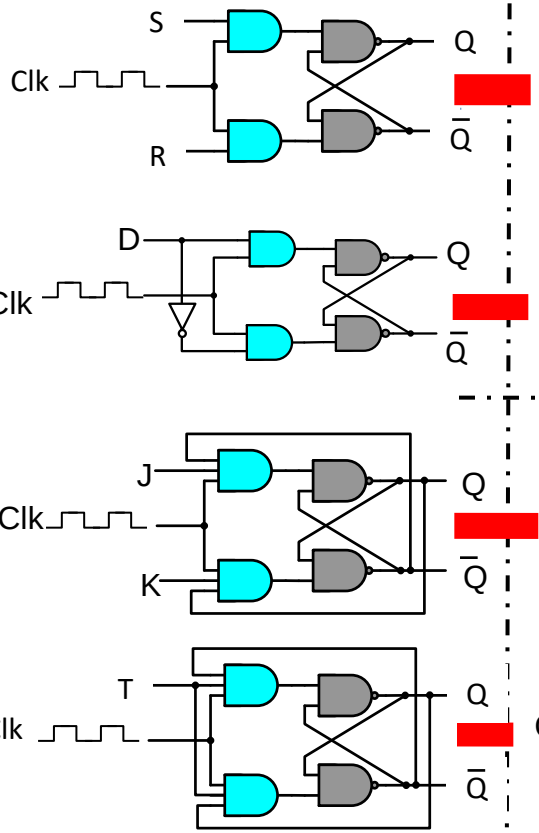
The first attempt problem when S & R are both high

But now there is no reset



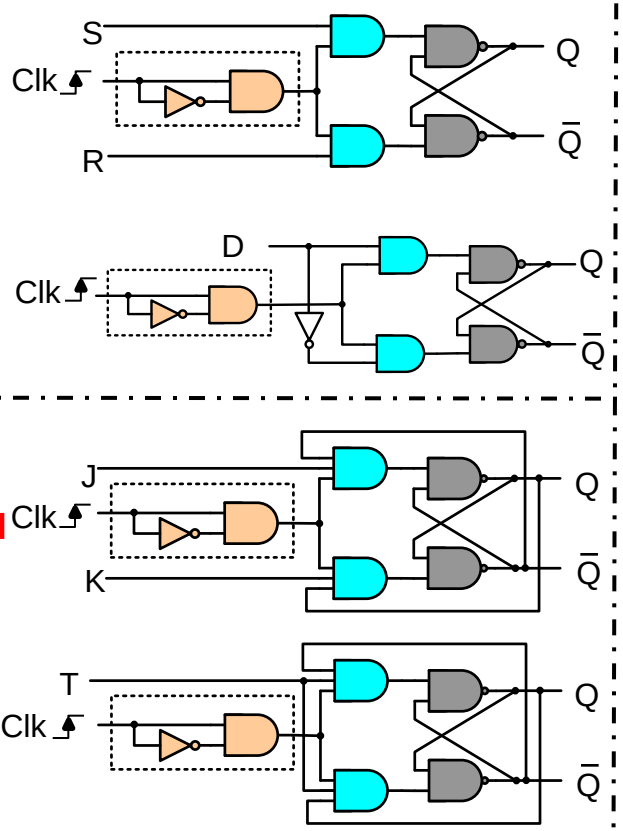
The JK flip-flop augments the behavior of the S-R flip-flop (J=Set, K=Reset) by interpreting the J = K = 1 condition as a "flip" or toggle command.

Use of clock allows for interaction between devices Master/Slave

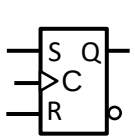


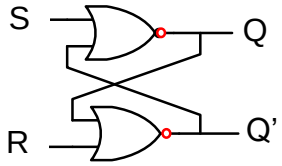
Problem as long as clock is high data can change in middle register reads

Use of rising edge detector circuit solves data fluctuating when being read

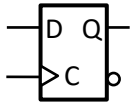


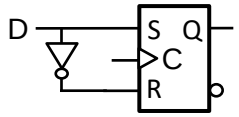
Logic Storage Devices



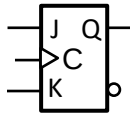


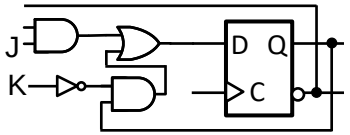
S	R	Q(t+1)	Operation
0	0	Q(t)	Hold
0	1	0	Reset
1	0	1	Set
1	1	?	Undefined



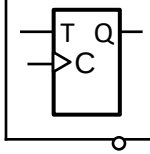


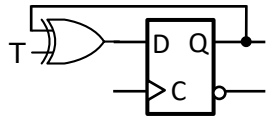
D	Q(t+1)	Operation
0	0	Reset
1	1	Set





J	K	Q(t+1)	Operation
0	0	Q(t)	Hold
0	1	0	Reset
1	0	1	Set
1	1	$\overline{Q}$(t)	Toggle





T	Q(t+1)	Operation
0	Q(t)	No Change
1	$\overline{Q}$(t)	Toggle

Register is a digital component that can temporarily store single or multiple bits.

Circuit Analysis of S-R NOR Latch

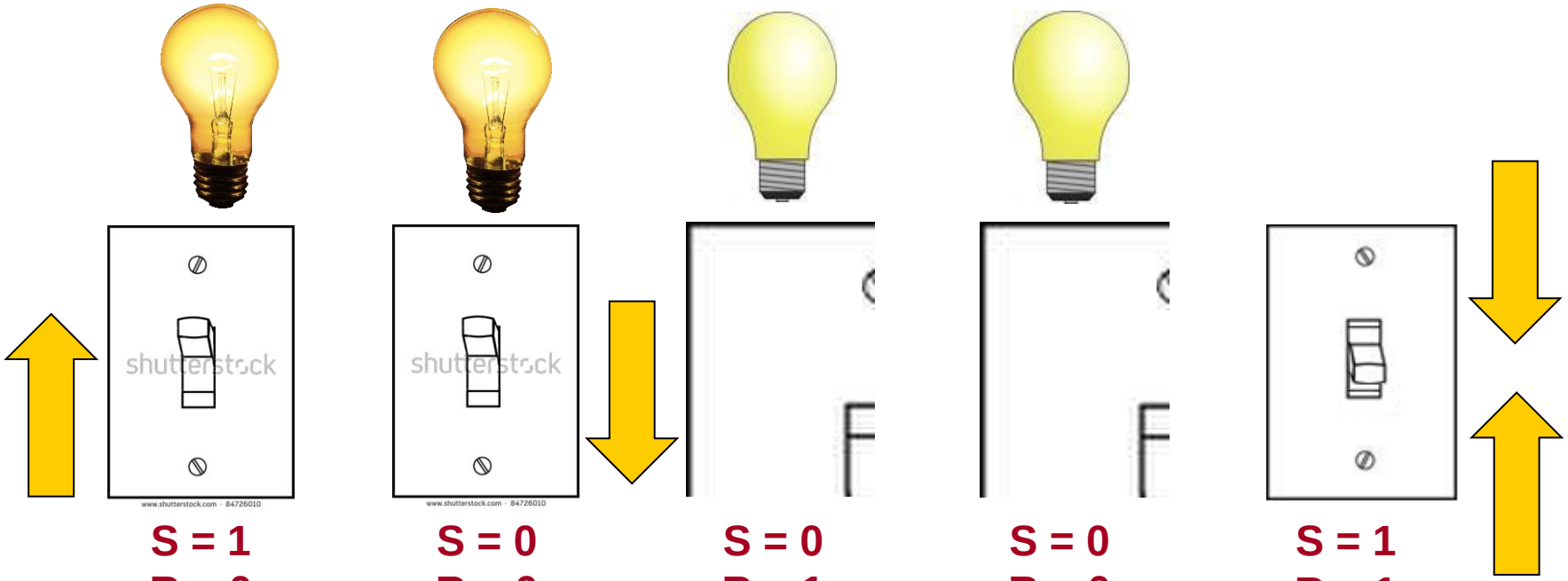
Different Techniques for Analysis

1. Circuit delay model.
2. Characteristic table.
3. Characteristic equation.
4. PS/NS (present-state/next-state) table.
5. Timing diagram.

Circuit Delay Model of S-R NOR Latch

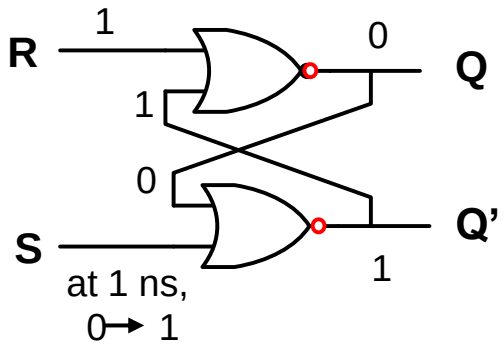
Five Different Conditions for a Light Switch

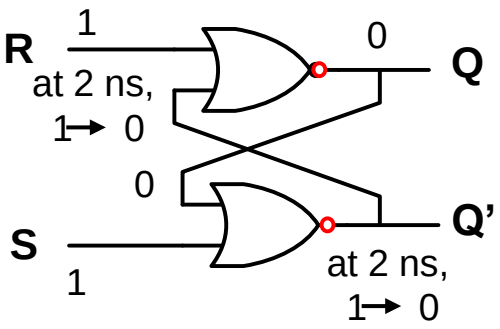
A light switch and a two cross-coupled NOR gates, which is a digital circuit called S-R NOR Latch have similar characteristics.

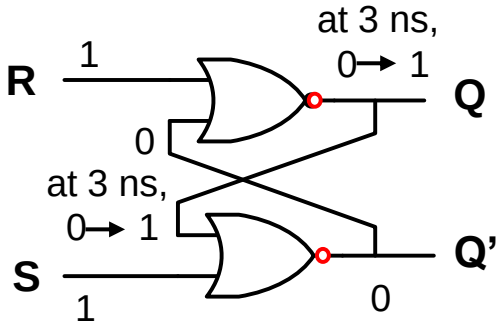


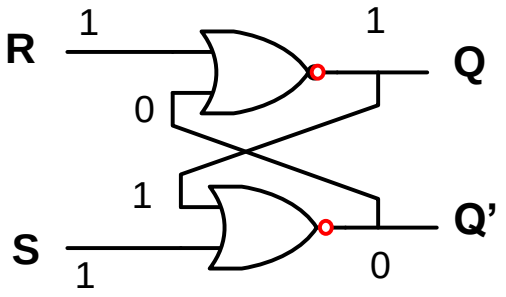
S = 1 R = 0 (push up, don't push down)	S = 0 R = 0 (don't push up, don't push down)	S = 0 R = 1 (don't push up, push down)	S = 0 R = 0 (don't push up, don't push down)	S = 1 R = 1 (push up, push down)
Set	**Hold**	**Reset or Clear**	**Hold**	**Forbidden**

Signal Propagation in a SR-Latch



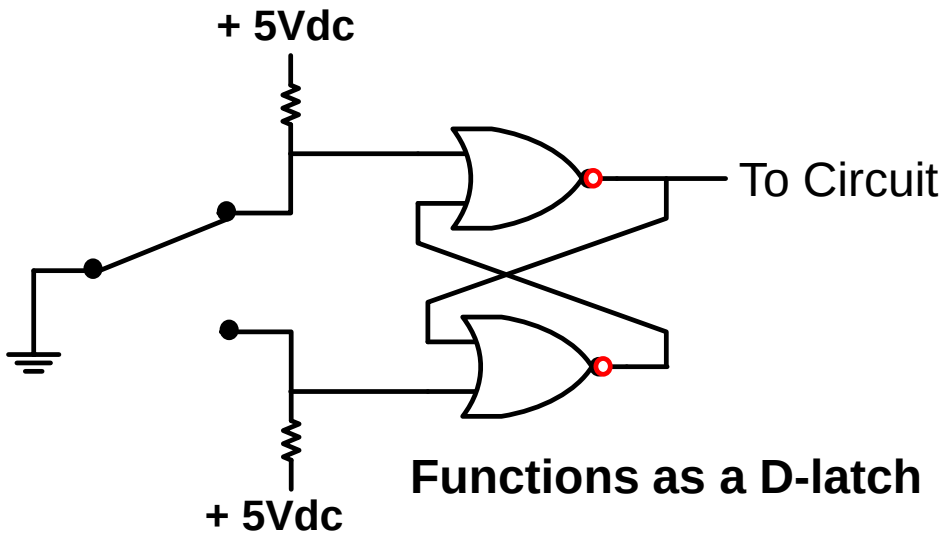






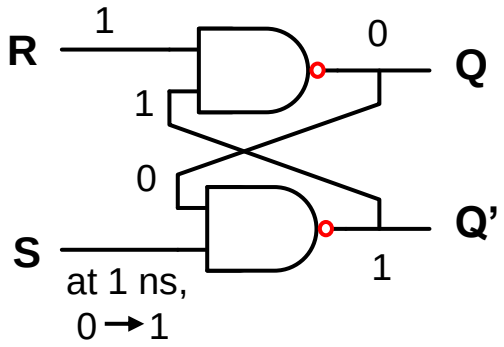
NOR Function

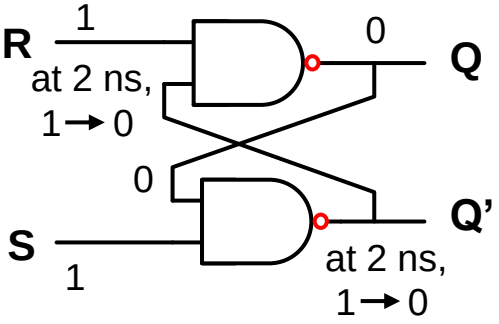
X	Y	F
0	0	1
0	1	0
1	0	0
1	1	0

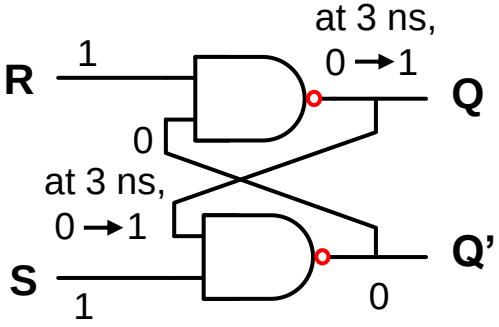


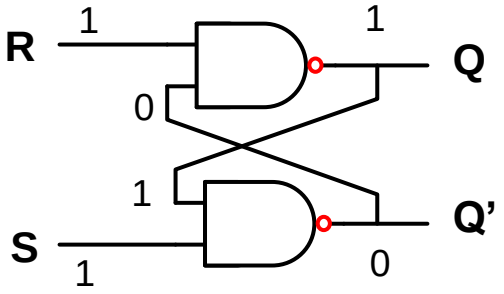
Functions as a D-latch

Signal Propagation in a SR-Latch



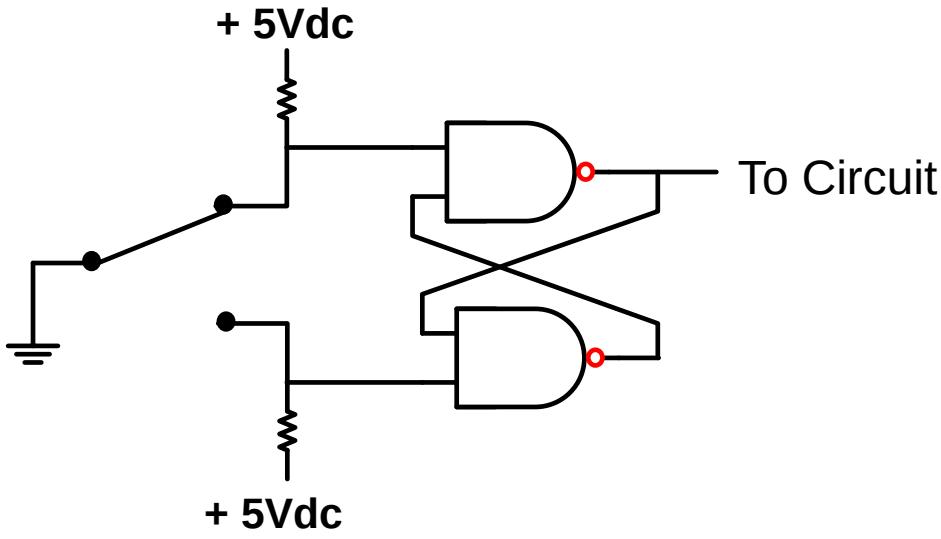






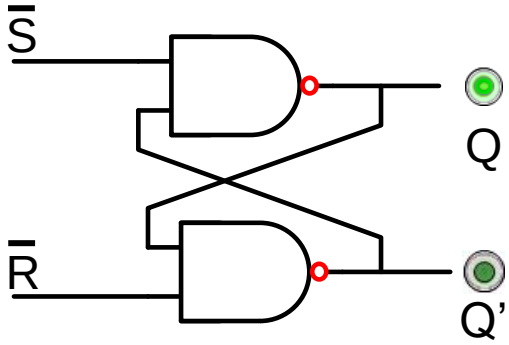
NAND Function

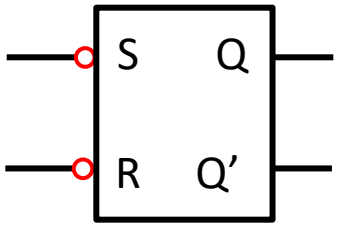
X	Y	F
0	0	1
0	1	1
1	0	1
1	1	0



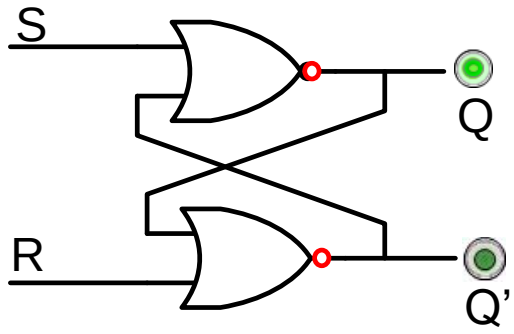
Analyzing an S-R NOR Latch

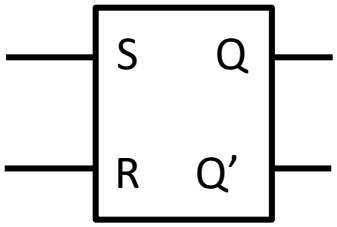
Latch is the simplest circuit form of a single-bit register.





$\overline{S}$	$\overline{R}$	Q	Q^+
1	1	1	1
1	1	0	0
1	0	1	0
1	0	0	0
0	1	1	1
0	1	0	1
0	0	1	Not Allowed
0	0	1	





S	R	Q	Q^+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	1	Not Allowed
1	1	1	

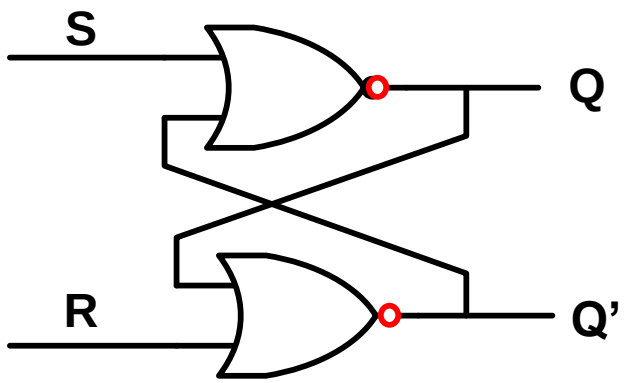
Circuit Delay Model for S-R NOR Latch

t_p=0	SR = 10	Q = 1	Q' = 0	Set
t_p=1	SR = 00	Q = 1	Q' = 0	Hold
t_p=2	SR = 01	Q = 0	Q' = 1	Reset
t_p=3	SR = 11	Q = ?	Q' = ?	Forbidden

NOR Function

X	Y	F
0	0	1
0	1	0
1	0	0
1	1	0

NOTE: Any time one of the inputs X or Y is a 1 the output F is a 0.



Characteristic Table for an S-R NOR Latch

CHARACTERISTIC TABLE

NOR FOR S-R LATCH

S	R	Q(t+1)	Next State	
0	0	Q(t)	Present State (High or Low)	HOLD
0	1	0	Low	RESET
1	0	1	High	SET
1	1	?	Reset dominant (normally not used)	FORBIDDEN

NAND FOR S-R LATCH

S	R	Q(t+1)	Next State	
0	0	?	Reset dominant (normally not used)	FORBIDDEN
0	1	1	High	SET
1	0	0	Low	RESET
1	1	Q(t)	Present State (High or Low)	HOLD

PS/NS Table for an S-R NOR Latch

State Transition Table
S-R NOR Latch

S	R	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	?

S	R	Q	Q^+
0	0	0	Q = 0, Hold
0	0	1	Q = 1, Hold
0	1	0	0, Reset
0	1	1	0, Reset
1	0	0	1, Set
1	0	1	1, Set
1	1	0	?, Invalid
1	1	1	? , Invalid

	R'Q' 00	R'Q 01	RQ 11	RQ' 10
S' 0	0	1	0	0
S 1	1	1	?	?

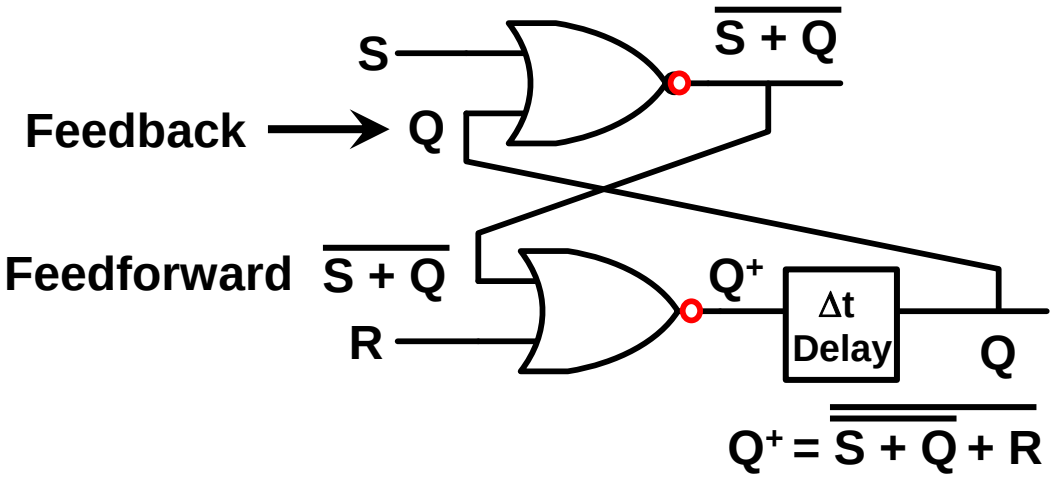
CHARACTERISTIC EQUATION FOR S-R NOR LATCH

	R'Q' 00	R'Q 01	RQ 11	RQ' 10
S' 0	0	1	0	0
S 1	1	1	?	?

Characteristic Equation: S and R cannot be both 1

$Q^+ = SR' + R'Q$ without don't cares

$Q^+ = S + R'Q$ with don't cares



$$Q^+ = \overline{\overline{S+Q}+R}$$
$$= \overline{S}\,\overline{Q} + R$$
$$= (\overline{\overline{S}}\,\overline{Q})\overline{R}$$
$$= (\overline{\overline{S}} + \overline{Q})\overline{R}$$
$$= (S + Q)\overline{R}$$
$$= S\overline{R} + Q\overline{R}$$

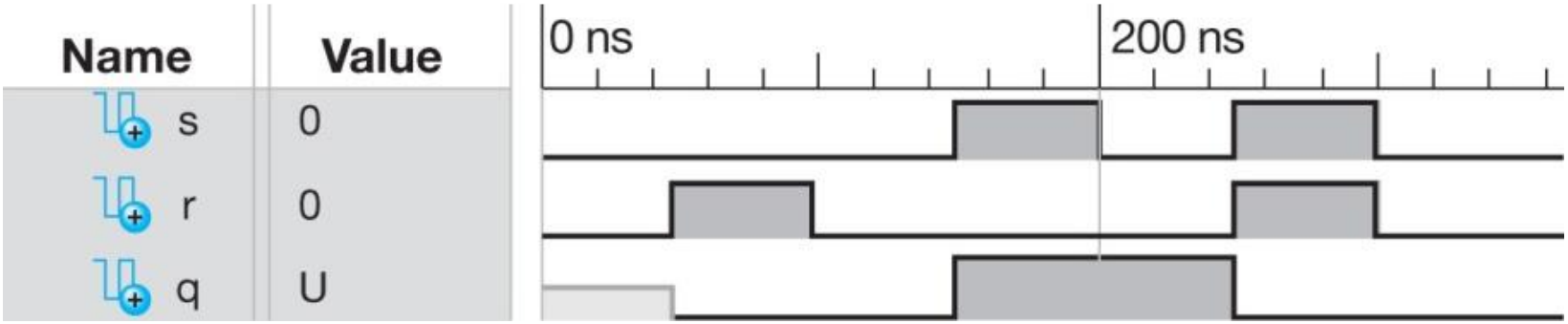
VHDL DESIGN FOR S-R NOR LATCH


```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity S_R_NOR_LATCH is port (
     S, R : in std_logic;
     Q : inout std_logic
     );
end S_R_NOR_LATCH;

architecture dataflow of S_R_NOR_LATCH is
begin
     Q <= (Q and not R) or (S and not R);
end dataflow;
```

$Q^+ = SR' + R'Q$ without don't cares

ALTERNATE DESIGN FOR S-R NOR LATCH


```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity S_R_NOR_LATCH_int is port (
     S, R : in std_logic;
     Q : out std_logic
     );
end S_R_NOR_LATCH_int;

architecture dataflow of S_R_NOR_LATCH_int is
     signal Q_int: std_logic;
begin
     Q_int <= (Q_int and not R) or (S and not R);
     Q <= Q_int;
end dataflow;
```



State Transition Table
S-R NAND Latch

$\overline{S}$	$\overline{R}$	Q(t+1)
1	1	Q(t)
1	0	0
0	1	1
0	0	?

S	R	Q	Q^+
1	1	1	Q = 0, Hold
1	1	0	Q = 1, Hold
1	0	1	0, Reset
1	0	0	0, Reset
0	1	1	1, Set
0	1	0	1, Set
0	0	1	?, Invalid
0	0	0	? , Invalid

	R'Q' 00	R'Q 01	RQ 11	RQ' 10
S' 0	?	?	1	1
S 1	0	0	0	1

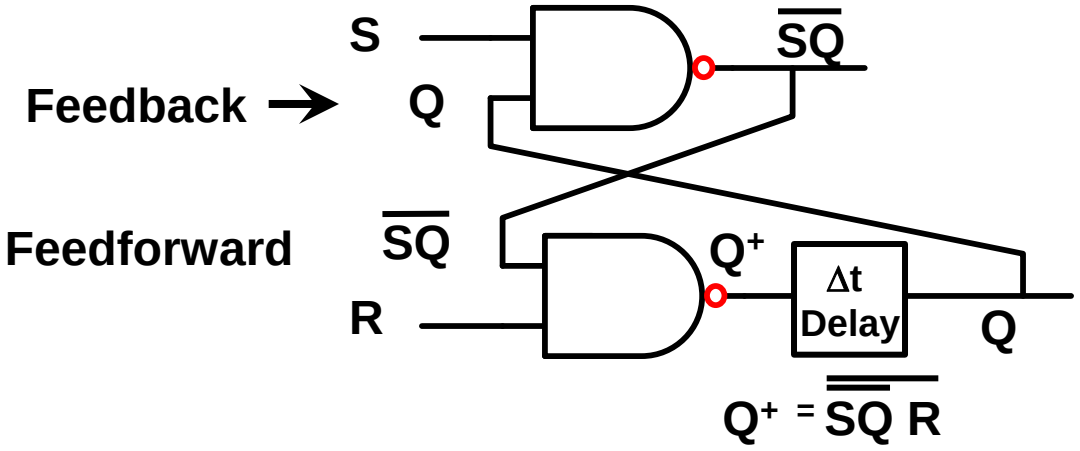
CHARACTERISTIC EQUATION FOR S-R NOR LATCH

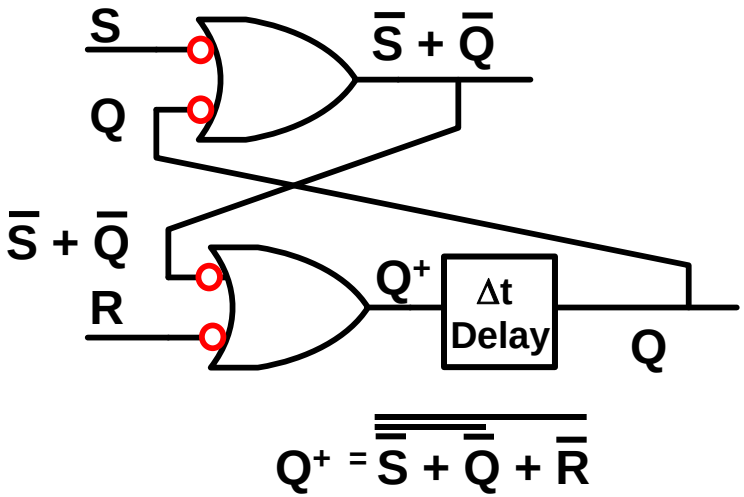
	R'Q' 00	R'Q 01	RQ 11	RQ' 10
S' 0	?	?	1	1
S 1	0	0	0	1

Characteristic Equation: S and R cannot be both 1

$Q^+ = S'R + RQ'$ without don't cares

$Q^+ = S' + RQ'$ with don't cares

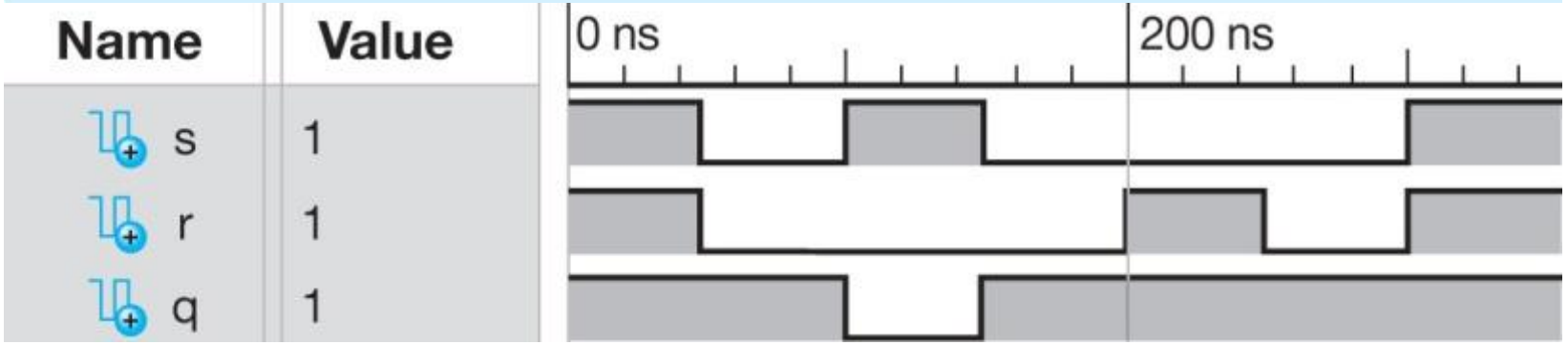




VHDL DESIGN FOR S-R NAND LATCH

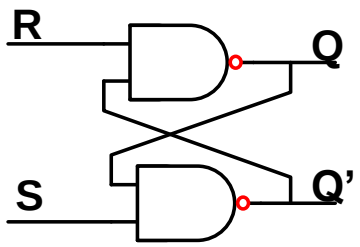

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity S_R_NAND_LATCH is port (
     S, R : in std_logic;
     Q : inout std_logic
     );
end S_R_NAND_LATCH;

architecture dataflow of S_R_NAND_LATCH is
begin
     Q <= (R and Q) or not S;
end dataflow;
```

$Q^+ = S' + RQ'$ with don't cares

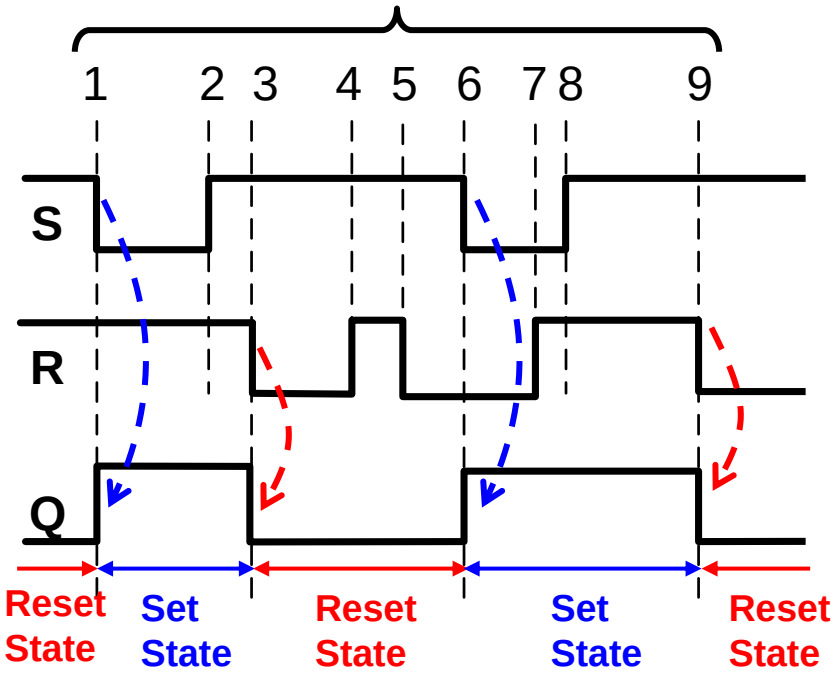


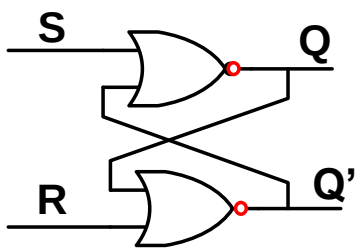
Timing Diagrams

$\overline{S}$	$\overline{R}$	Q(t+1)
1	1	Q(t)
1	0	0
0	1	1
0	0	?



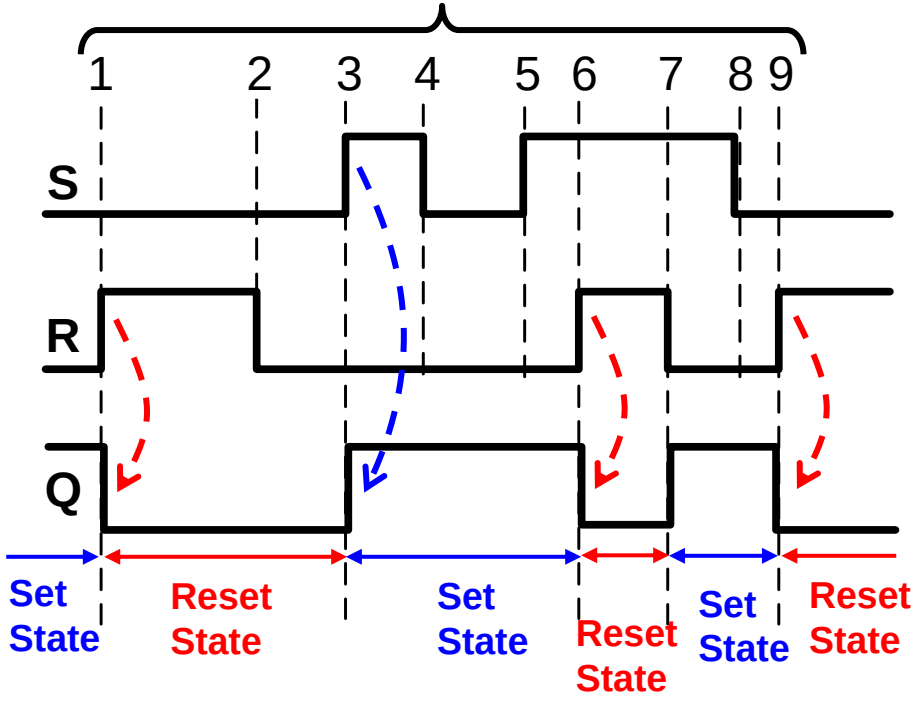
Asynchronous Events
Time between events is not the same



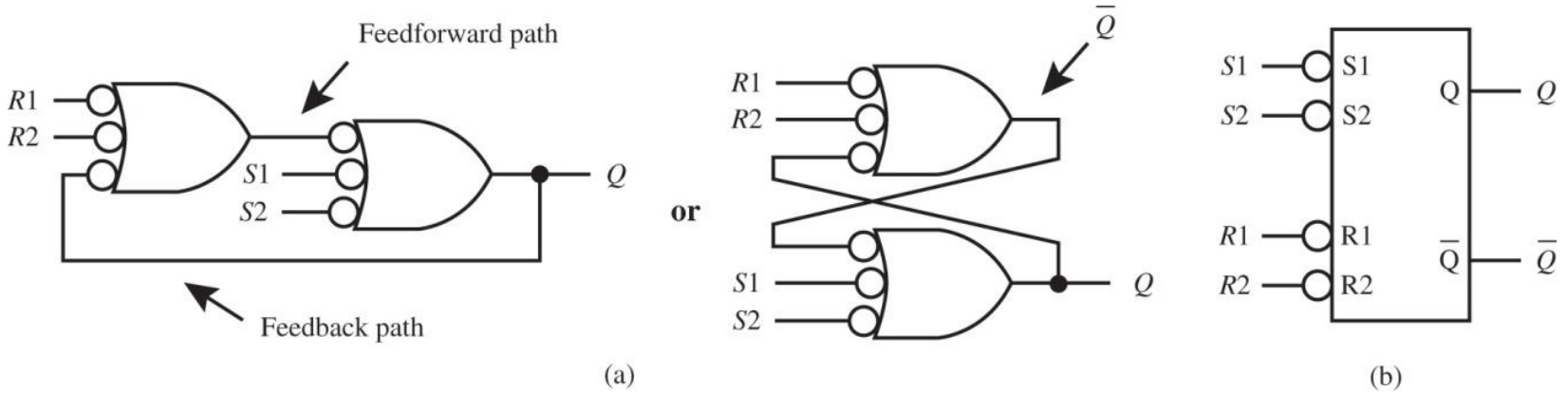


S	R	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	?

Asynchronous Events
Time between events is not the same



Multiple Inputs S-R NAND Latch



We use bubbled input OR gates to represent the NAND gates because these equivalent gate forms help remind us that the inputs to an S-R NAND Latch are active low inputs.

This type of Latch is also referred as and S'-R' NAND Latch.

Basic CLOCK (CLK)

CLOCK (Oscillator)

A clock provides a sequence of pulses at its output.

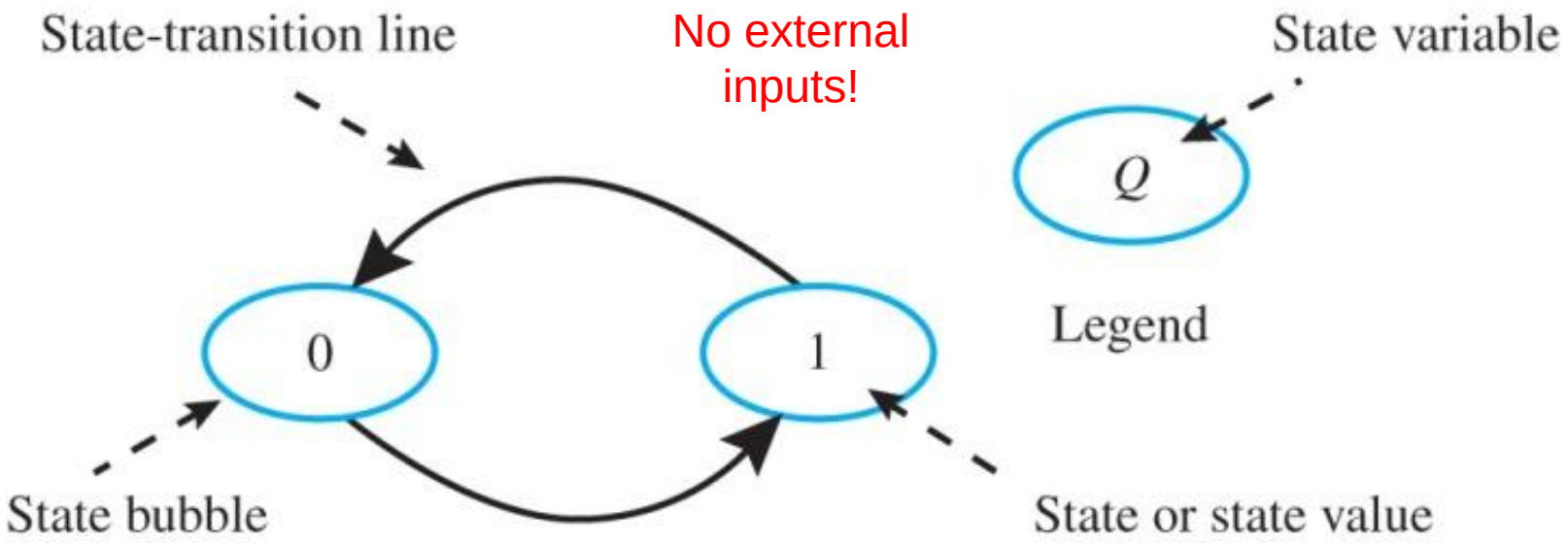
Clocks are used in the design of synchronous sequential circuits.

Crystal Clock Oscillators are much more stable.

EX. your PC, smartphone, tablet, etc.

State Diagram for a CLOCK

- Circle or oval represents each state of the circuit.
- A state transition line is used to represent the flow of the circuit when it changes from one state to the next.
- Four major parts of a state diagram: state bubbles, state-transition lines, state variables, and states or state values.

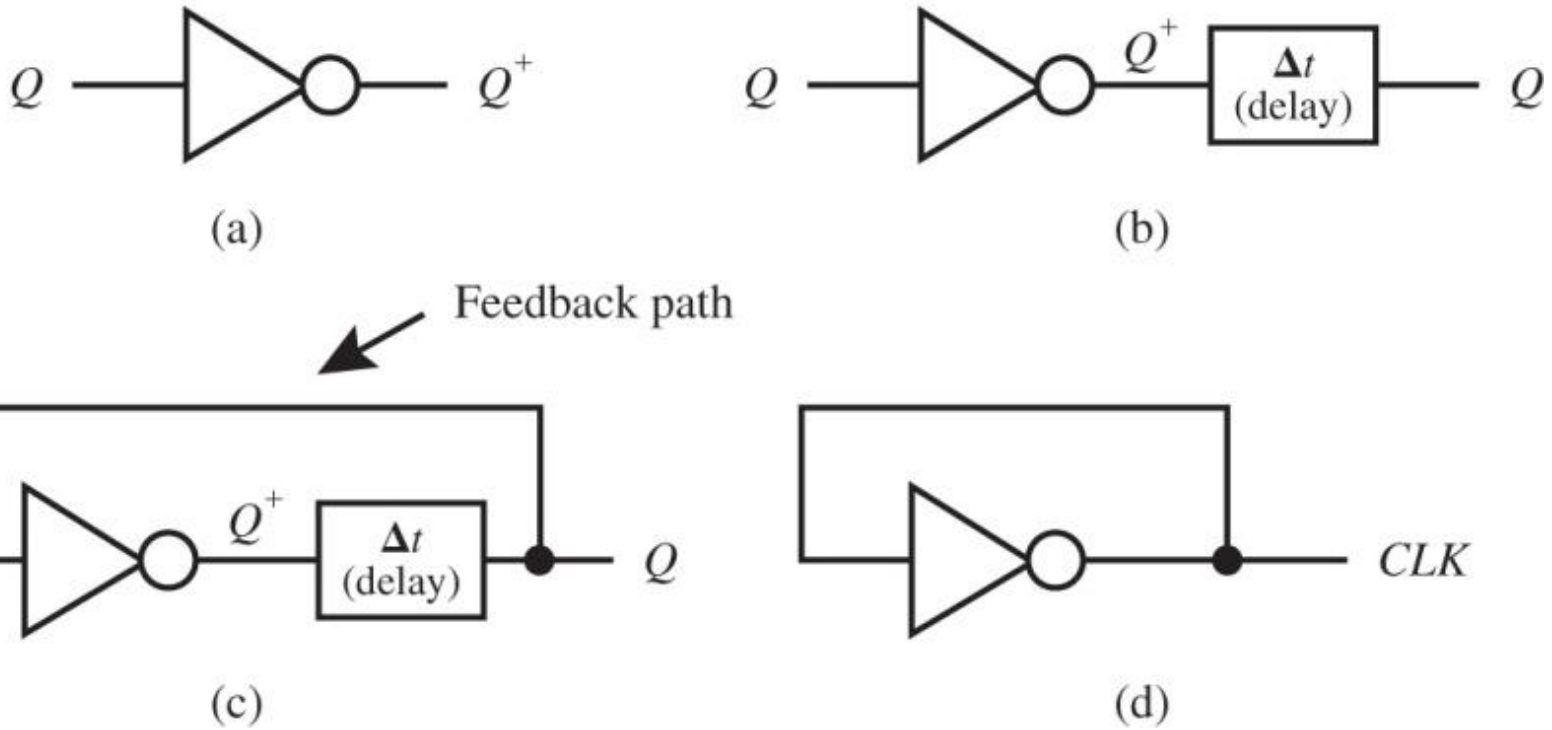


PS/NS Table for CLOCK (Oscillator)

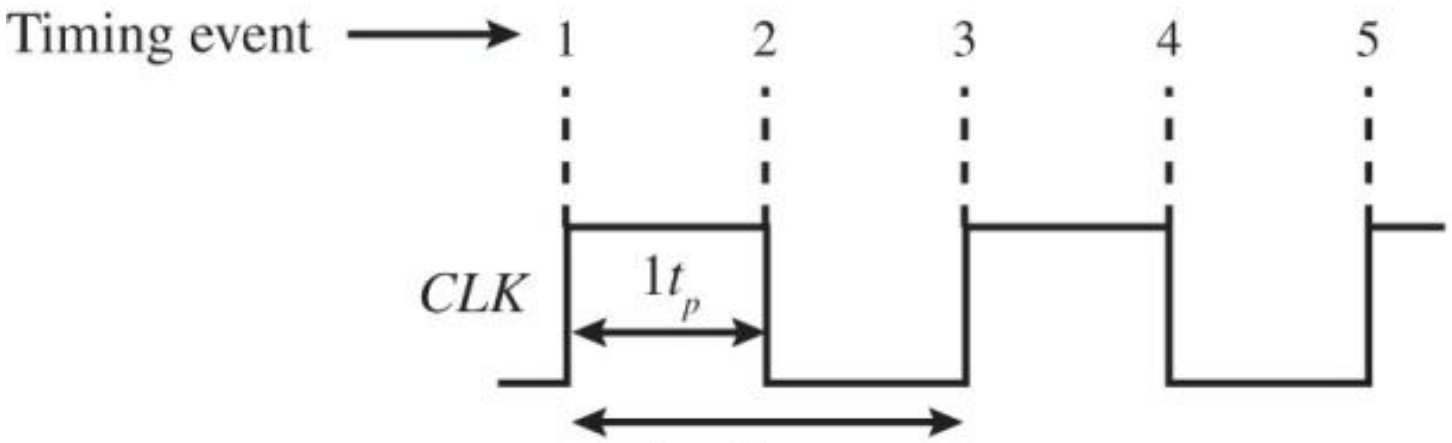
Q	Q^+
0	1
1	0

Characteristic Equation = Σm(0) = m0 - SOM

Gate-level Circuit Design for the CLOCK



Ideal Timing Diagram for CLOCK

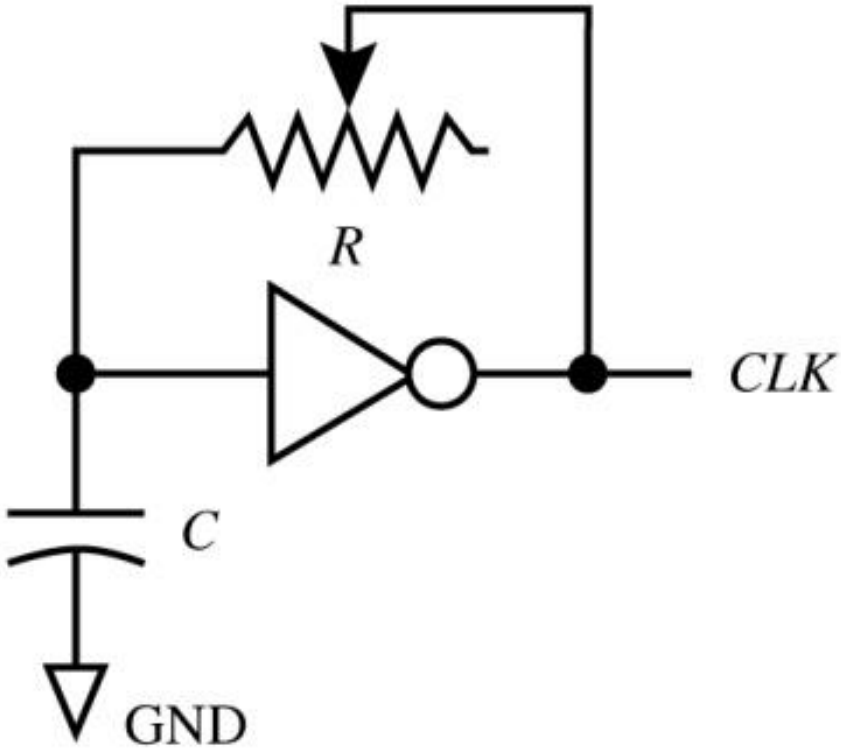


Period $T = 2t_p$

Frequency $f = 1/T = 1/(2t_p)$

Duty cycle $DC = 1t_p/T = 1t_p/(2t_p) = ½ = 0.5 = 50\%$

CLOCK Circuit with RC Circuit Added for Frequency Adjustment



Q&A