EGEC281 – FALL 2024

LAB 3

7 SEGMENT DISPLAY AND DECODER

Designing with VHDL
Experiment 3A, and 3B

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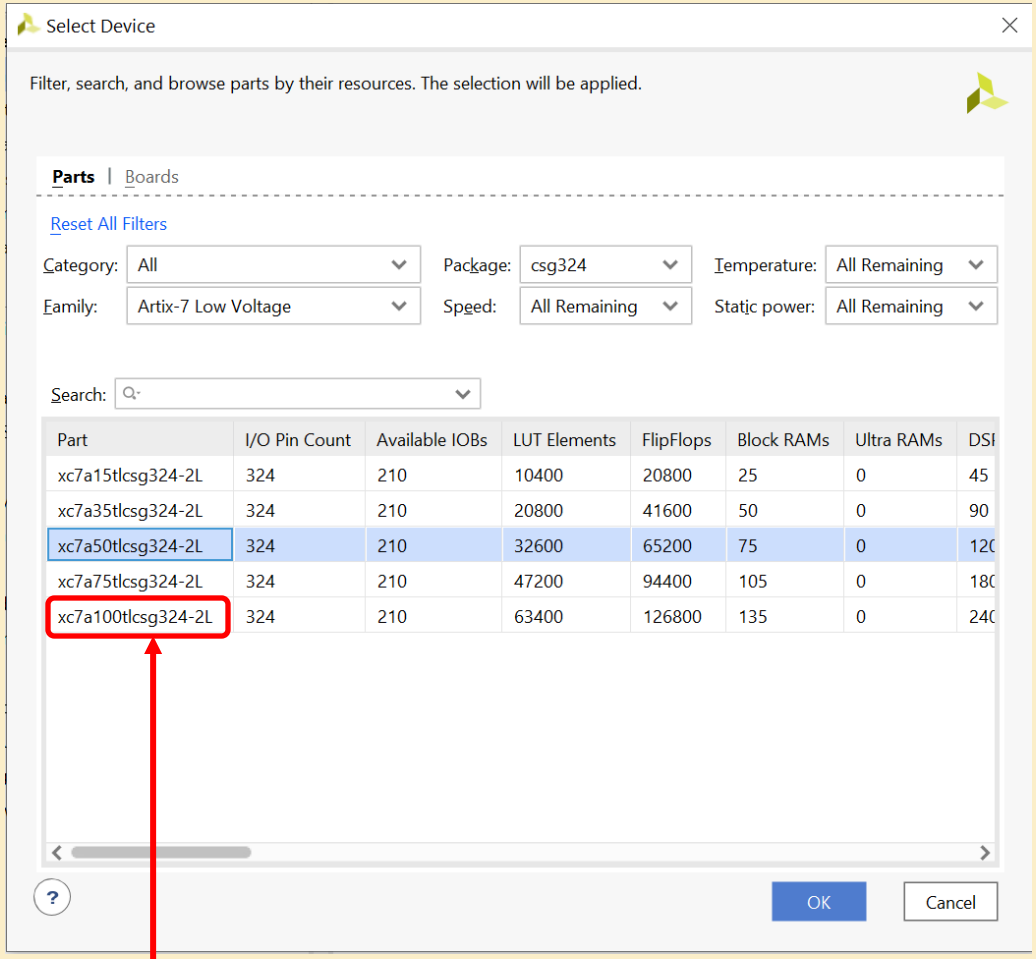
LEARNING OBJECTIVES

- Implement Binary to Decoder.
  - Project 3A – 7-Segment Decoder.
  - Project 3B – Binary to 7-Segment Display.
- K-map into VHDL Code

FPGA SETUP IN XILINX VIVALDO



XC7a100tlcsg324-2L for the board in class

PROJECT 3A

- 2 Inputs (Switches), 4-bit Output An (Anode) and 8-bit Cath (Cathode).
- If both inputs are logic ‘0’, then the 7-segment should display  .
- If the input X is logic ‘0’ and input Y is logic ‘1’ then the then the 7-segment should display  .
- If the input X is logic ‘1’ and input Y is logic ‘0’ then the then the 7-segment should display  .
- If both inputs are logic ‘1’, then the 7-segment should display  .

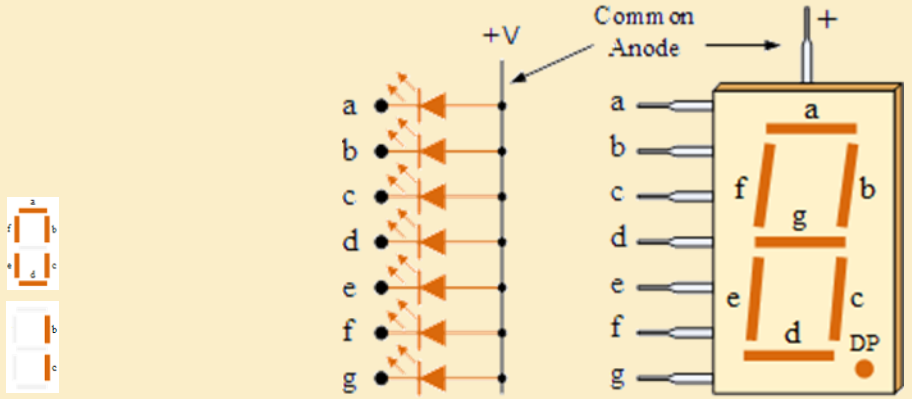
LAB 3 PROJECT A – 2 BIT BCD TO 7-SEGMENT

1. Create a new project. Name it “Lab3A”.
   - Write the VHDL that compares two input values to see if they are the same value.
   - Input signals X and Y
   - Output signals Cath (8 bits), An (8 bits).
2. Based on the table shown on next slide, create a truth table.
3. Write the VHDL code according to the truth table in step 2.
4. Simulate Lab3A. Make stimulus inputs count from 00 – 11, waiting 100 ns between each count.
5. Verify that your truth table corresponds with the simulation output.
6. Create a XDC for Lab3A; Assign:
   - Input signals A and B: 2 switches
     Input X ⇨ L16
     Input Y ⇨ J15
   - Output signals Cath (8 bits) to cathode ports,
   - Output An (8 bits) to anode ports.
7. Generate and download program file (.bit) to FPGA
8. Verify that the hardware works as expected based on your truth table from #3, #4, and #5.

An	Loc	Cath	Loc
An(0)	J15	Cath(0)	T10
An(1)	J18	Cath(1)	R10
An(2)	T9	Cath(2)	K16
An(3)	J14	Cath(3)	K13
An(4)	P14	Cath(4)	P15
An(5)	T14	Cath(5)	T11
An(6)	K2	Cath(6)	L18
An(7)	U13	Cath(7)	H15

LAB 3 PROJECT A – 2 BIT BCD TO 7-SEGMENT

X	Y	A	B	C	D	E	F	G	DP
0	0	0	0	0	0	0	0	1	1
0	1	1	0	0	1	1	1	1	1
1	0								
1	1								



Note: Please note Cathode is active low

PROJECT 3B BINARY TO HEXADECIMAL ON 7-SEGMENT DISPLAY

- 4 Inputs (Switches), 8 bit Cathode and 8 bit Anode Outputs.
- Based on the 4-bit inputs, the 7-segment display should show the hexadecimal equivalent of the input.

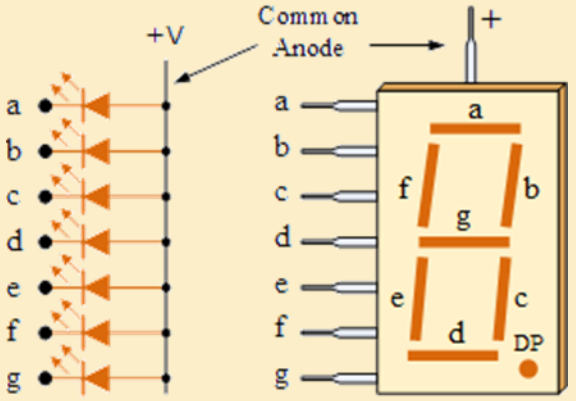
LAB 3 PROJECT B BINARY TO HEXADECIMAL

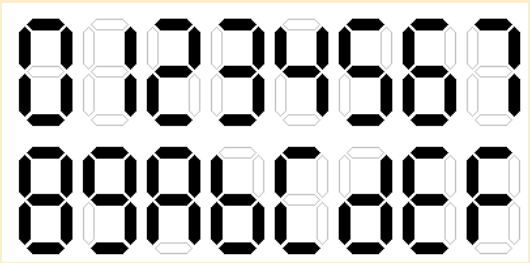
1. Create a new project. Name it Lab3B.
   - Write the VHDL that compares two input values to see if they are the same value.
   - Input signals W, X, Y and Z
   - Output signals Cath (8 bits), An (4 bits).
2. Simulate Lab3B. Make stimulus inputs count from 0000 – 1111, waiting 100 ns between each count.
3. Verify the simulation output.
4. Create a XDC for Lab3B; Assign:
   - Input signals W, X, Y and Z: 4 switches
     - Input W → R15
     - Input X → M13
     - Input Y → L16
     - Input Z → J15
   - Output signals Cath (8 bits) to cathode ports,
   - Output An (8 bits) to anode ports.
5. Generate and download program file (.bit) to FPGA
6. Verify that the hardware works as expected.

An	Loc	Cath	Loc
An(0)	J15	Cath(0)	T10
An(1)	J18	Cath(1)	R10
An(2)	T9	Cath(2)	K16
An(3)	J14	Cath(3)	K13
An(4)	P14	Cath(4)	P15
An(5)	T14	Cath(5)	T11
An(6)	K2	Cath(6)	L18
An(7)	U13	Cath(7)	H15

LAB 3 PROJECT B BINARY TO HEXADECIMAL

W	X	Y	Z	A	B	C	D	E	F	G	DP
0	0	0	0	0	0	0	0	0	0	1	1
0	0	0	1								
0	0	1	0								
0	0	1	1								
0	1	0	0								
0	1	0	1								
0	1	1	0								
0	1	1	1								
1	0	0	0								
1	0	0	1								
1	0	1	0								
1	0	1	1								
1	1	0	0								
1	1	0	1								
1	1	1	0								
1	1	1	1								





Note: Please note Cathode is active low

LAB REPORT

- Cover page:
  - Course Title
  - Lab Number, Letter
  - Team Names
- Project 3A:
  - VHDL
  - Logic Diagram (Schematic)
  - Truth Table
  - Simulation Code, Waveform
  - XDC
  - Picture of Implementation
- Project 3B:
  - VHDL
  - Logic Diagram (Schematic)
  - Truth Table
  - K-Map
  - Simulation Code, Waveform
  - XDC
  - Picture of Implementation
- Summary paragraph
  - Work completed
  - Any problems
  - Helpful Hints
  - Suggested Improvements