1. Drew Sadler
2. No TLB hit
3. Yes TLB hit
4. Class 0
5. 00100000111011 - read
   00110000010101 - write
   01100000100001 - read
6. Spends 30 cycles on a miss, and 1 cycle on a hit (or 300,000 cycles for misses and 90,000 cycles for the hits, making 390,000 total cycles) , spending 31 cycles on a memory access
7. Average cycles taken to access memory is 4.33333333333333333333333333333333
8. 290,000 total cycles, with a average number of cycles per access being 3.22222222222222222222222222222222
9. 129,000 cycles spend on memory access with the average becoming 1.30303030303030303030303030303030303 number of cycles per access
10. The 2nd alternative is better, by 161,000 cycles faster, making a ratio of 2.248062015503875968992248062015 5 times faster