Introduction

The AXI Timebase Watchdog Timer is a 32-bit peripheral that connects to the AXI and provides the controller interface for asynchronous serial data transfer.

Features

- AXI interface is based on AXI 4 lite specificatio

- Connects as a 32-bit slave on AXI

- Watchdog timer (WDT) with selectable timeout period and interrupt

- Configurable WDT enable: enable-once or enable-disable

- One 32-bit free-running timebase counter with rollover interrupt

| LogiCORE IP Facts				
Core Specifics				
Supported Device Family	Virtex®6, Spartan®6			
Resources Used	Slices	LUTs	FFs	Block RAMs
	Refer to the Table 8 and Table 9			0
Special Features	N/A			
Provided with Core				
Documentation	Product Specification			
Design File Formats	VHDL			
Constraints File	N/A			
Verification	N/A			
Instantiation Template	N/A			
Reference Designs /Application Notes	N/A			
Additional Items	N/A			
Design Tool Requirements				
Xilinx Implementation Tools	ISE® 12.2 or later			
Verification	ModelSim SE/EE 6.5b or later			
Simulation	ModelSim SE/EE 6.5b or later			
Synthesis	XST 12.2 or later			
Support				
Provided by Xilinx, Inc.				

Functional Description
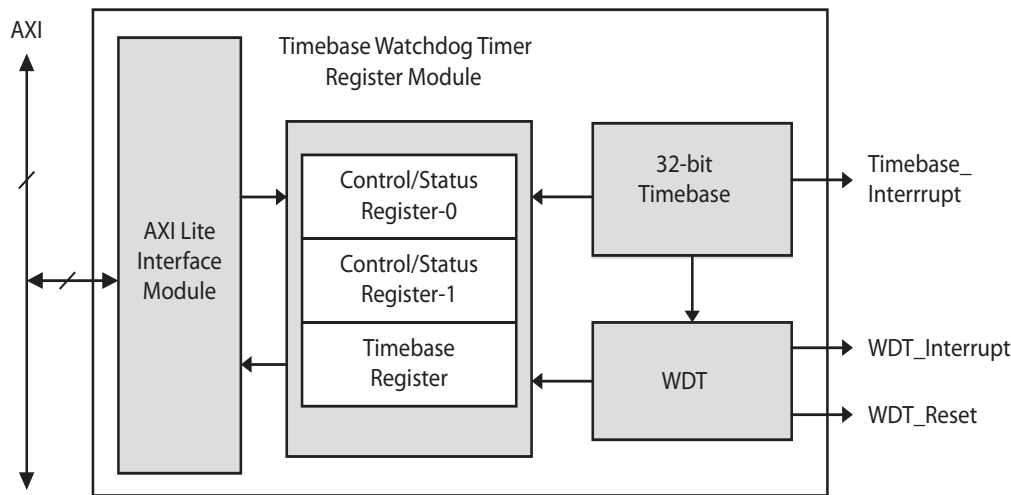
Figure 1: **Block Diagram of AXI Timebase Watchdog Timer**

The AXI Timebase Watchdog Timer modules are described in the sections below.

AXI Lite Interface Module: The AXI Lite Interface Module provides the interface to the AXI. Read and write transactions at the AXI are translated into equivalent IP Interconnect (IPIC) transactions. The register interfaces of the AXI Timebase Watchdog Timer connect to the IPIC. The AXI Lite Interface Module also provides an address decoding service.

Timebase Watchdog Timer Register Module: The Timebase Watchdog Timer Register Module includes all memory mapped registers (as shown in Figure 1). It interfaces to the AXI. It consists of an 32-bit control/status register-0, an 32-bit control/status register-1 and an 32-bit timebase register (TBR).

32-bit Timebase: The 32-bit timebase consists of free-running 32-bit timebase counter.

WDT: The Watchdog Timer (WDT) provides the functionality of timeout.

AXI Timebase Watchdog Timer Characteristics

The AXI Timebase Watchdog Timer has the following characteristics:

- Consists of a free-running 32-bit timebase counter that is used for both the general purpose timing and the WDT facility

- The timebase counter always counts up from system reset and is read-only

- The WDT timeout interval is set by generic C_WDT_INTERVAL, which determines the bit in the timebase to be used as input to the WDT state machine

- The WDT uses a dual-expiration architecture. After one expiration of the timeout interval an interrupt is generated and the WDT state bit is set to one in the status register. If the state bit is not cleared (by writing a '1' to the state bit) before the next expiration of the timeout interval, a WDT reset is generated. A WDT reset, sets the WDT reset status bit in the status register so that the application code can determine if the last system reset was a WDT reset.

- The WDT can only be disabled by writing to two distinct addresses, reducing the possibility of inadvertently disabling the WDT in the application code.

AXI Timebase Watchdog Timer Operation

Timebase Operation

The timebase is a 32-bit up counter that is incremented by one on the rising edge of the clock provided to the Timebase Watchdog Timer. The counter is reset to zero when the reset input is high or when the WDT is enabled. The TBR contains the full timebase count value of 32 bits.

The TWCSR0 contains the most-significant 28 bits of the timebase count, as well as the WDT enable and status bits. The timing resolution from the upper 28 bits of the timebase count is T_{clk} x 16 (T_{clk} is the period of the input clock). As a result, a single access can be used to read the state of the watchdog timer, as well as a reduced resolution version of the timebase.

An interrupt signal is provided that pulses high for one clock period as the counter rolls over from `0xFFFFFFFF` to `0x00000000`. This interrupt can be used by the software to keep track of how many timebase rollovers have occurred.

WDT Operation

The WDT timeout interval is configured by a parameter to be $2^{C\_WDT\_INTERVAL}$ clock cycles, where C_WDT_INTERVAL is any integer from 8 to 31. The WDT interval is set at FPGA configuration time and cannot be modified dynamically through a control register. Figure 2 shows the WDT state diagramThe detailed block diagram of the AXI Timer/Counter is shown in Figure 2.
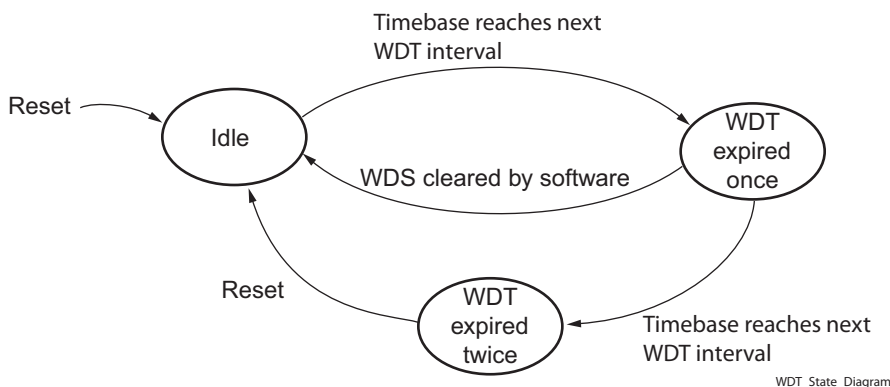

Figure 2: **Timebase Watchdog timer State Diagram**

AXI Timer I/O Signals

The AXI Timebase Watchdog Timer I/O signals are listed and described in Table 1.

Table 1: **AXI Timebase Watchdog Timer I/O Signal Description**

Port	Signal Name	Interface	I/O	Initial State	Description
System Signals					
P1	S_AXI_ACLK	System	I	-	AXI Clock
P2	S_AXI_ARESETN	System	I	-	AXI Reset, active LOW
AXI Write Address Channel Signals					

Table 1: **AXI Timebase Watchdog Timer I/O Signal Description** *(Cont.)*

Port	Signal Name	Interface	I/O	Initial State	Description
P3	S_AXI_AWADDR[C_S_AXI_ADDR_WIDTH-1:0]	AXI	I	-	AXI Write address. The write address bus gives the address of the write transaction.
P4	S_AXI_AWVALID	AXI	I	-	Write address valid. This signal indicates that valid write address is available.
P5	S_AXI_AWREADY	AXI	O	0x0	Write address ready. This signal indicates that the slave is ready to accept an address.
AXI Write Channel Signals					
P6	S_AXI_WDATA[C_S_AXI_DATA_WIDTH-1:0]	AXI	I	-	Write data
P7	S_AXI_WSTB[C_S_AXI_DATA_WIDTH/8-1:0]	AXI	I	-	Write strobes. This signal indicates which byte lanes to update in memory.
P8	S_AXI_WVALID	AXI	I	-	Write valid. This signal indicates that valid write data and strobes are available.
P9	S_AXI_WREADY	AXI	O	0x0	Write ready. This signal indicates that the slave can accept the write data.
AXI Write Response Channel Signals					
P10	S_AXI_BRESP[1:0]	AXI	O	0x0	Write response. This signal indicates the status of the write transaction. "00" - OKAY "10" - SLVERR "11" - DECERR
P11	S_AXI_BVALID	AXI	O	0x0	Write response valid. This signal indicates that a valid write response is available.
P12	S_AXI_BREADY	AXI	I	-	Response ready. This signal indicates that the master can accept the response information.
AXI Read Address Channel Signals					
P13	S_AXI_ARADDR[C_S_AXI_ADDR_WIDTH-1:0]	AXI	I	-	Read address. The read address bus gives the address of a read transaction.

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Table 1: **AXI Timebase Watchdog Timer I/O Signal Description** *(Cont.)*

Port	Signal Name	Interface	I/O	Initial State	Description
P14	S_AXI_ARVALID	AXI	I	-	Read address valid. This signal indicates, when HIGH, that the read address is valid and will remain stable until the address acknowledgement signal, S_AXI_ARREADY, is high.
P15	S_AXI_ARREADY	AXI	O	0x1	Read address ready. This signal indicates that the slave is ready to accept an address.
			AXI Read Data Channel Signals		
P16	S_AXI_RDATA[C_S_AXI_DATA_WIDTH -1:0]	AXI	O	0x0	Read data
P17	S_AXI_RRESP[1:0]	AXI	O	0x0	Read response. This signal indicates the status of the read transfer. "00" - OKAY "10" - SLVERR "11" - DECERR
P18	S_AXI_RVALID	AXI	O	0x0	Read valid. This signal indicates that the required read data is available and the read transfer can complete
P19	S_AXI_RREADY	AXI	I	-	Read ready. This signal indicates that the master can accept the read data and response information
			AXI Timebase Watchdog Timer Signals		
P20	WDT_Reset	Timebase Watchdog Timer	O	0	Asserted upon second expiration of the WDT timeout interval. (Active High = '1').
P21	Timebase_Interrupt	Timebase Watchdog Timer	O	0	Asserted as a one clock period wide pulse upon rollover of the timebase from 0xFFFFFFFF to 0x00000000.
P22	WDT_Interrupt	Timebase Watchdog Timer	O	0	Asserted high and stays high until the WDS bit is cleared in the TWCSR0 register.
P23	Freeze	Timebase Watchdog Timer	I	-	When High the watchdog tier counters will be stalled

AXI Timebase Watchdog Timer Design Parameters

To allow the user to create the AXI Timebase Watchdog Timer that is uniquely tailored for the user's system, certain features can be parameterized. This allows the user to have a design that only utilizes the resources required by the system and operating at the best possible performance. The AXI Timebase Watchdog Timer design parameters are shown in Table 2.

Table 2: **AXI Timebase Watchdog Timer Design Parameters**

Generic	Feature/Description	Parameter Name	Allowable Values	Default Value	VHDL Type
System Parameter					
G1	Target FPGA family	C_FAMILY	virtex6, spartan6	virtex6	string
G2	System clock frequency (in Hz) driving the Timer peripheral	C_S_AXI_ACLK_FREQ	integer (ex. 100000000)	100_000_000	integer
AXI Parameters					
G3	AXI Base Address	C_BASEADDR	Valid Address[1]	None[3]	std_logic_vector
G4	AXI High Address	C_HIGHADDR	Valid Address[2]	None[3]	std_logic_vector
G5	AXI address bus width	C_S_AXI_ADDR_WIDTH	32	32	integer
G6	AXI data bus width	C_S_AXI_DATA_WIDTH	32	32	integer
Timebase Watchdog Timer Parameters					
G7	Indicates the exponent for setting the length of the WDT interval. WDT interval = $2^{C\_WDT\_INTERVAL} \times T_{clk}$	C_WDT_INTERVAL	8 - 31	30	integer
G8	Indicates WDT enable behavior	C_WDT_ENABLE_ONCE	0 = WDT can be repeatedly enabled and disabled via software 1 = WDT can only be enabled once (no disable possible after initial enable)	1	integer

Notes:
1. The user must set the values. The C_BASEADRR must be a multiple of the range, where the range is C_HIGHADDR - C_BASEADDR + 1.
2. C_HIGHADDR - C_BASEADDR must be a power of 2 greater than equal to C_BASEADDR + 0x1000.
3. No default value will be specified to insure that the actual value is set, i.e., if the value is not set, a compiler error will be generated.

Allowable Parameter Combinations

The address range specified by C_BASEADDR and C_HIGHADDR must be a power of 2, and must be at least 0x1000.

For example, if C_BASEADDR = 0xE0000000, C_HIGHADDR must be at least = 0xE00001000.

AXI Timebase Watchdog Timer Parameter - Port Dependencies

The dependencies between the AXI Timebase Watchdog Timer core design parameters and I/O signals are described in Table 3. In addition, when certain features are parameterized out of the design, the related logic will no longer be a part of the design. The unused input signals and related output signals are set to a specified value.

Table 3: **AXI Timebase Watchdog Timer Parameter-Port Dependencies**

Generic or Port	Name	Affects	Depends	Relationship Description
Design Parameters				
G5	C_S_AXI_ADDR_WIDTH	P3, P13	-	Defines the width of the ports
G6	C_S_AXI_DATA_WIDTH	P6, P7, P16	-	Defines the width of the ports
I/O Signals				
P4	S_AXI_AWADDR[C_S_AXI_ADDR_WIDTH-1:0]	-	G5	Port width depends on the generic C_S_AXI_ADDR_WIDTH
P7	S_AXI_WDATA[C_S_AXI_DATA_WIDTH-1:0]	-	G6	Port width depends on the generic C_S_AXI_DATA_WIDTH
P8	S_AXI_WSTB[C_S_AXI_DATA_WIDTH/8-1:0]	-	G6	Port width depends on the generic C_S_AXI_DATA_WIDTH
P14	S_AXI_ARADDR[C_S_AXI_ADDR_WIDTH -1:0]	-	G5	Port width depends on the generic C_S_AXI_ADDR_WIDTH
P17	S_AXI_RDATA[C_S_AXI_DATA_WIDTH -1:0]	-	G6	Port width depends on the generic C_S_AXI_DATA_WIDTH

AXI Timebase Watchdog Timer Register Descriptions

Table 4 shows all the AXI Timebase Watchdog Timer registers and their addresses.

Table 4: **AXI Timer Registers**

Base Address + Offset (hex)	Register Name	Access Type	Reset Value (hex)	Description
TWCSR0	C_BASEADDR + 0x0	Word	0x00000000	Control/Status register-0
TWCSR1	C_BASEADDR + 0x4	Word	0x00000000	Control/Status register-1, state is mirrored in TWCSR0 for read
TBR	C_BASEADDR + 0x08	Word	0x00000000	Timebase register

Control/Status Register - 0 (TWCSR0)

Control/Status Register-0 contains the watchdog timer reset status, watchdog timer state, and watchdog timer enables. The TWCSR0 bit definitions are shown in Figure 3 and explained in Table 5.

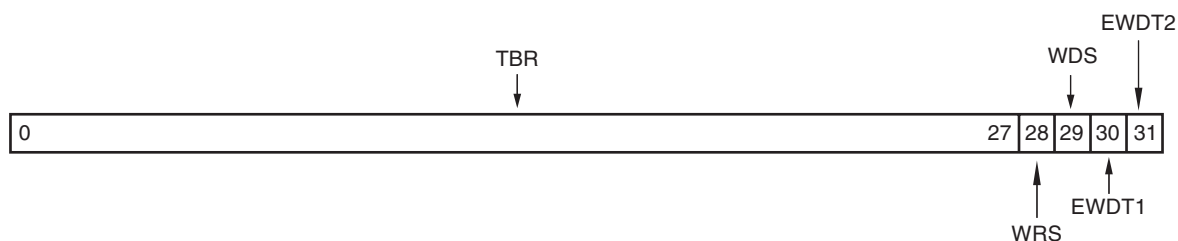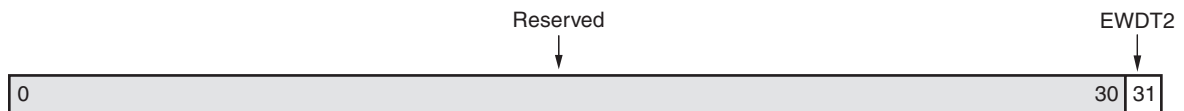*Figure 3:* **Control/Status Register - 0 (TWCSR0)**

Table 5: **Control/Status Register - 0 Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
0 - 27	TBR	Read	0	Timebase Register (Most significant 28 bits): This read-only field contains the most significant 28 bits of the timebase register. The timebase register is mirrored here so that a single read can be used to obtain the count value and the watchdog timer state if the upper 28 bits of the timebase provide sufficient timing resolution.
28	WRS	Read/Write	'0'	Watchdog Reset Status: Indicates the WDT reset signal was asserted. This bit is not cleared by a system reset so that it can be read after a system reset to determine if the reset was caused by a watchdog timeout. Writing a '1' to this bit clears the watchdog reset status bit. Writing a '0' to this bit has no effect. '0' = WDT reset has not occurred '1' = WDT reset has occurred
29	WDS	Read/Write	'0'	Watchdog Timer State: Indicates the WDT period has expired. The WDT_Reset signal will be asserted if the WDT period expires again before this bit is cleared by software. Writing a '1' to this bit clears the watchdog timer state. Writing a '0' to this bit has no effect. '0' = WDT period has not expired '1' = WDT period has expired, reset will occur on next expiration

Table 5: **Control/Status Register - 0 Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
30	EWDT1	Read/Write	'0'	Enable Watchdog Timer (Enable 1): This bit must be used in conjunction with the EWDT2 bit in the TWCSR1 register. Both bits must be 0 to disable the WDT. '0' = Disable WDT function if EWDT2 also equals '0' '1' = Enable WDT function
31	EWDT2	Read	'0'	Enable Watchdog Timer (Enable 2): This bit is read only and is the only place to read back a value written to bit 31 of TWCSR1.

Control/Status Register - 1 (TWCSR1)

Control/Status Register-1 contains the second Watchdog Timer (WDT) enable bit. The WDT enable must be cleared in both TWCSR0 and TWCSR1 to disable the WDT. If the WDT is configured as enable-once, then the WDT cannot be disabled after it has been enabled. The TWCSR1 bit definitions are shown in Figure 4 and explained in Table 6.

Reserved   EWDT2

| 0 | 30 | 31 |

Figure 4: **TControl/Status Register - 1 (TWCSR1)**

Table 6: **Control/Status Register - 1 Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
0 - 30	Reserved	N/A	N/A	Reserved
31	EWDT2	Write<RD Red>[1]	'0'	Enable Watchdog Timer (Enable 2): This bit must be used in conjunction with the EWDT1 bit in the TWCSR0 register to disable the WDT. Both bits must be 0 to disable the WDT. This bit is write-only in this register. The value of EWDT2 can be read back only in TWCSR1. '0' = Disable WDT function if EWDT1 also equals '0' '1' = Enable WDT function

1. Reading of this register returns undefined value.

Timebase Register (TBR)

The TBR bit definitions are shown in Figure 5 and explained in Table 7.

The Timebase Register is the output of a free-running incrementing counter that clocks at the input clock rate (no prescaling of the clock is done for this counter). This register is read-only and is reset by the following:

- A system reset
- Enabling the WDT after power on reset

Enabling the WDT after the WDT has been disabled. (EWDT1 and EWDT2 must both be '0' to disable the WDT.) The WDT is enabled when either EWDT1 or EWDT2 are set to '1'. Note that when the WDT mode is enable-once, the TBR can only be reset when the WDT is first enabled.

TBR

| 0 | 31 |
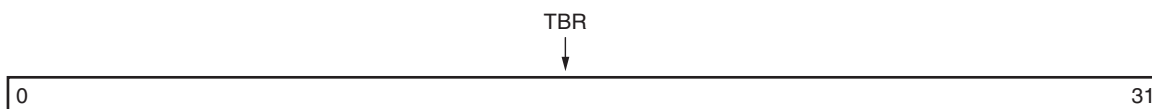
Figure 5: **Timebase Register 0**

Table 7: **Timebase Register Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
0 - 31	TBR	Read[Ref 1]	0	Timebase register: This register indicates the free-running incrementing counter value.

1. Writing into this register has no effect.

AXI Timebase Watchdog Timer Timing Diagrams

Figure 6 shows the WDT Expired Once operation waveform and Figure 7 shows the WDT Expired Twice operation waveform. The state of the WDT is given by the WDS bit in the TWCSR0 register. If the WDT interval expires while the WDS bit is '1', the WDT reset signal is asserted. An interrupt is provided when the WDS bit is set so that the software can clear the bit before the second expiration of the WDT. The WDS bit is cleared by writing a '1' to it. Writing a '0' to the WDS bit has no effect. Figure 6 shows the operation performed where WDS

bit is cleared by the software before the second expiration occurs. Figure 7 shows the operation performed where WDS bit is not cleared and WDT expired twice state is reached.
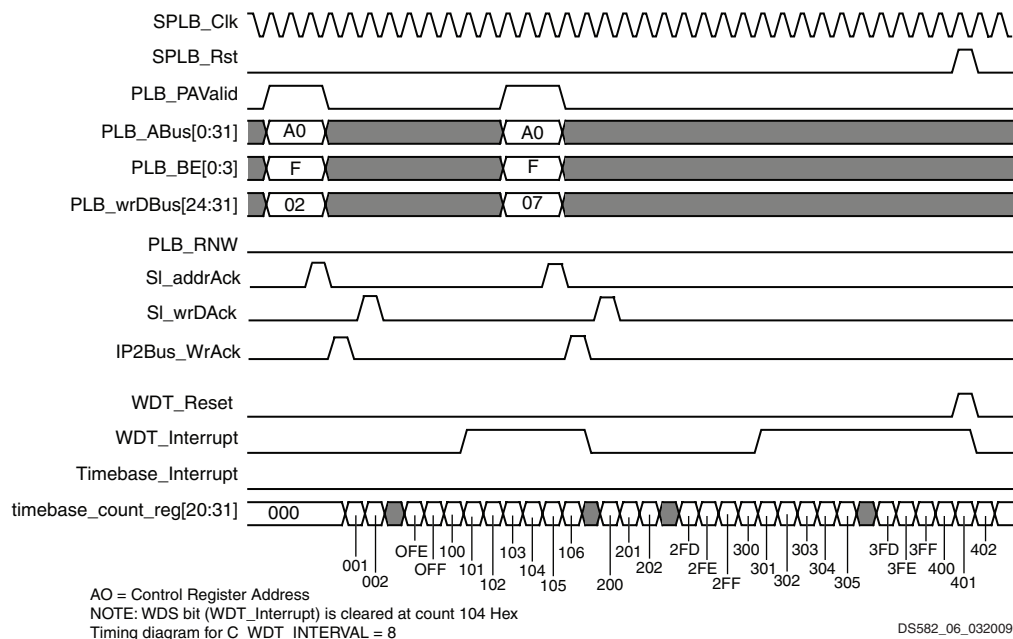

AO = Control Register Address
NOTE: WDS bit (WDT_Interrupt) is cleared at count 104 Hex
Timing diagram for C_WDT_INTERVAL = 8

DS582_06_032009

Figure 6: **Timebase Watchdog timer State Diagram**

AO = Control Register Address
NOTE: WDT Expires twice
Timing diagram for C_WDT_INTERVAL = 8

DS582_07_032009
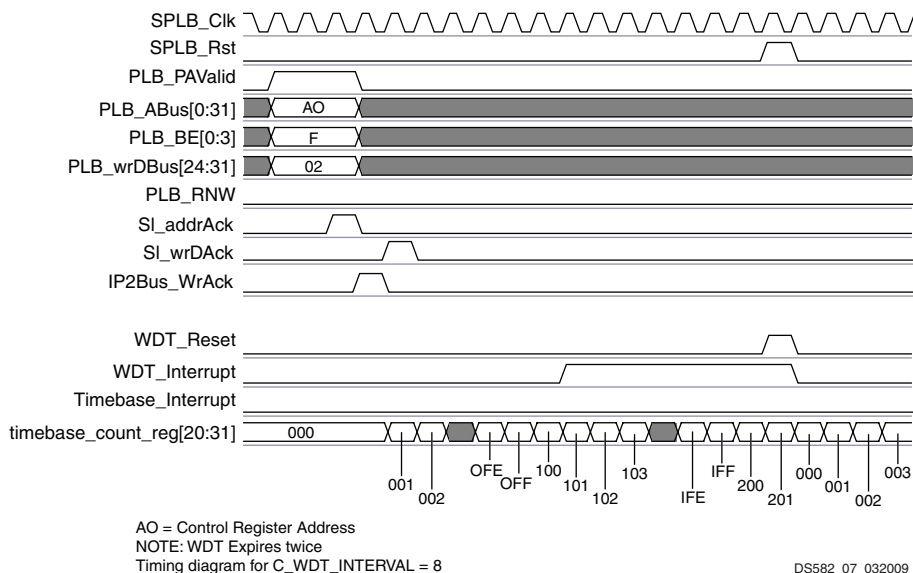
Figure 7: **Timebase Watchdog timer State Diagram**

Design Implementation

Target Technology

The intended target technology is Virtex6 and Spartan6 family FPGAs.

Device Utilization and Performance Benchmarks

Core Performance

Since the AXI Timer core will be used with other design modules in the FPGA, the utilization and timing numbers reported in this section are estimates only. When the AXI Timer core is combined with other designs in the system, the utilization of FPGA resources and timing of the AXI Timer design will vary from the results reported here.

The AXI Timer resource utilization for various parameter combinations measured with Virtex-6 as the target device are detailed in Table 8

Table 8: **Performance and Resource Utilization Benchmarks on Virtex-6 (xc6vlx130t-1-ff1156)**

Parameter Values		Device Resources			Performance
C_WDT_INTERVAL	WDT_ENABLE_ONCE	Slice Flip-Flops	Slices	LUTs	$f_{MAX \ (MHz)}$
8	0				
30	1				
31	1				

The AXI Timer resource utilization for various parameter combinations measured with Virtex-6 as the target device are detailed in Table 9

Table 9: **Performance and Resource Utilization Benchmarks on Spartan-6 (xc6slx45t-2-fgg484)**

Parameter Values		Device Resources			Performance
C_WDT_INTERVAL	WDT_ENABLE_ONCE	Slice Flip-Flops	Slices	LUTs	$f_{MAX \ (MHz)}$
8	0				
30	1				
31	1				

System Performance

To measure the system performance (Fmax) of this core, this core was added to a Virtex-6 system and a Spartan-6 system as the Device Under Test (DUT).

Because the AXI Timer core will be used with other design modules in the FPGA, the utilization and timing numbers reported in this section are estimates only. When this core is combined with other designs in the system, the utilization of FPGA resources and timing of the design will vary from the results reported here.

The target FPGA was then filled with logic to drive the LUT and BRAM utilization to approximately 70% and the I/O utilization to approximately 80%. Using the default tool options and the slowest speed grade for the target FPGA, the resulting target F_{MAX} numbers are shown in Table 10.

Table 10: **AXI Timer System Performance**

Target FPGA	Target F_{MAX} (MHz)
S6	110
V6	150

The target F_{MAX} is influenced by the exact system and is provided for guidance. It is not a guaranteed value across all systems.

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY.*

Reference Documents

- *AMBA AXI Protocol v1.0 Specification*

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
03/18/2010	1.0	Initial Xilinx release.

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