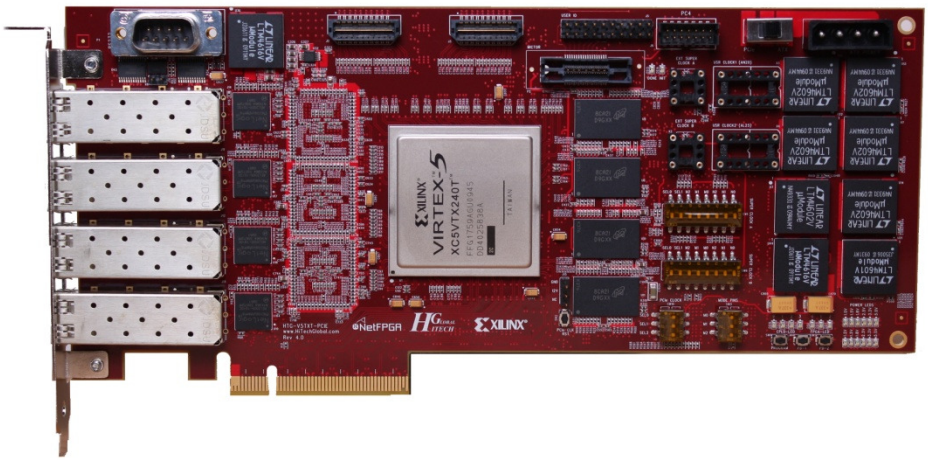
NetFPGA-10G Production Test

October 2010



Version 1.0

Contents

1. Introduction

This document describes the NETFPGA-10G board production test and how to use it. The purpose of the production test is to verify that your board is working. It does this by stressing all board level interfaces simultaneously under heavy load, and checking/reporting the status via PCIe or UART. It is packaged as a Virtex5 FPGA bitfile, corresponding software and this document. The bitfile contains the design for stressing the interfaces, while the software drives and monitors the test. The production test can be run on a board hosted by a Linux server, or operated in standalone mode outside of a server.

Please run this test before you start using the board. If the test outcome is not as described below, return the board to HTG immediately.

2. System requirements and setup

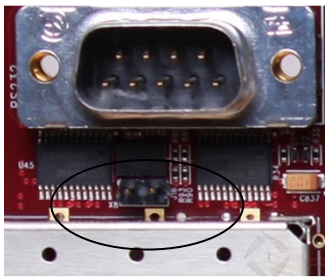
a. Standalone mode

The following items are required to conduct the test:

- NetFPGA-10G board rev4 or higher
- Latest bitstream – please download from www.netfpga.org
- ATX power supply
- JTAG programming cable
- Null-modem (UART) cable
- Any UART terminal (for example a Windows machine with hyperterminal or PuTTY installed or a Linux machine with minicom installed)
- For testing of the expansion interface, the following cable is required which can be ordered from www.samtec.com: HQDP-020-05.00-STL-SBR-2. This is optional.
- For testing the 10G interfaces, we've verified operation with the following cables: This is optional.
  ProCurve 10GbE SFP+ 1m direct attach, model J9281B
  GORE SFP+ Eyeopener+ copper cable, 24 AWG, SFF-8431, 10 meter
  GORE copper cable, 32 AWG, SFF-8431, 1 meter

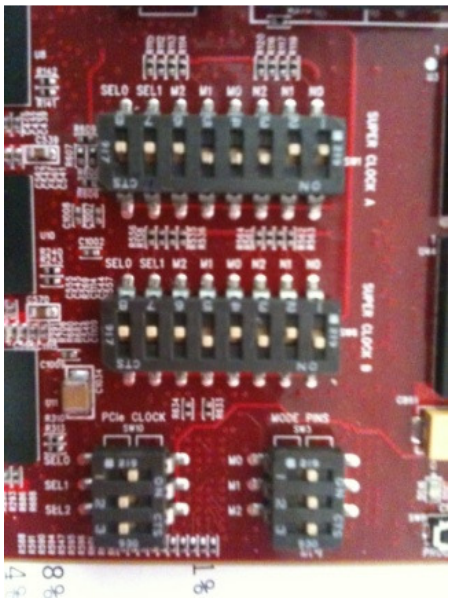
Before running the test please ensure that

- jumper J16 is not populated (location as shown in picture below)

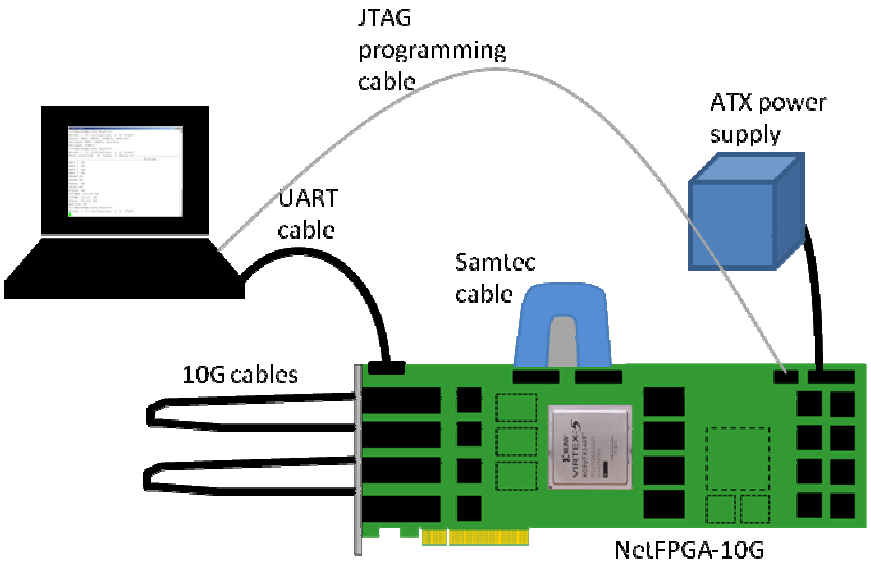


- set SW9 to ATX (make sure the switch is fully in the right position)

- NOTE: On the following switches, the switch pin is in the “on” position when it is set towards the side labeled “on”.
- SW1: SEL0, SEL1, M2, M1, M0, N2, N1, N0 are set to off, off, off, on, on, on, off, off
- SW6: SEL0, SEL1, M2, M1, M0, N2, N1, N0 are set to off, off, off, on, off on, off, on
- SW3: M0, M1, M2 is set to on, on, on
- SW10: SEL0, SEL1, SEL2 are set to on, off, off



The following picture illustrates the exact test set-up: In particular ensure the 10G cables are fitted as indicated.



b. Server mode

The following items are required to conduct the test:

- NetFPGA-10G board rev4 or higher
- Latest bitstream – please download from www.netfpga.org
- Latest production test software – please download from www.netfpga.org
- Linux Server: We've verified the NetFPGA-10G board operation with the following server, however there is no reason why it shouldn't work in similar setups:

NetFPGA-10G PreBuilt Desktop 10G Processor: Intel i7 920 Motherboard: eVGA X58 141-BL-E758 Video Card: ATI 3650 Chipset PCI-Express Operating System: CentOS Installed (free) Memory: 6GB (3x2GB) Corsair Hard Drives: Western Digital 500GB SATA Optical Drive: DVD Reader/Writer (all-in-one) Case: Lian-Li Mid Tower W/ Antec 500W PSU

(This server can be ordered from: Accent Technologies)

- JTAG programming cable
- A null-modem (UART) cable
- For testing of the expansion interface, the following cable is required which can be ordered from www.samtec.com: HQDP-020-05.00-STL-SBR-2. This is optional
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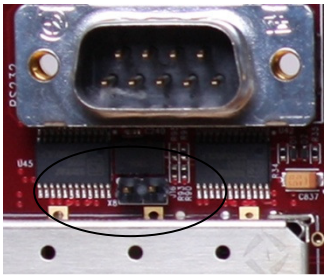
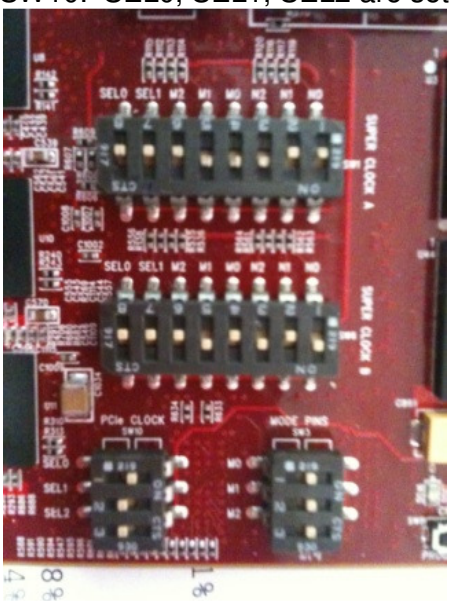
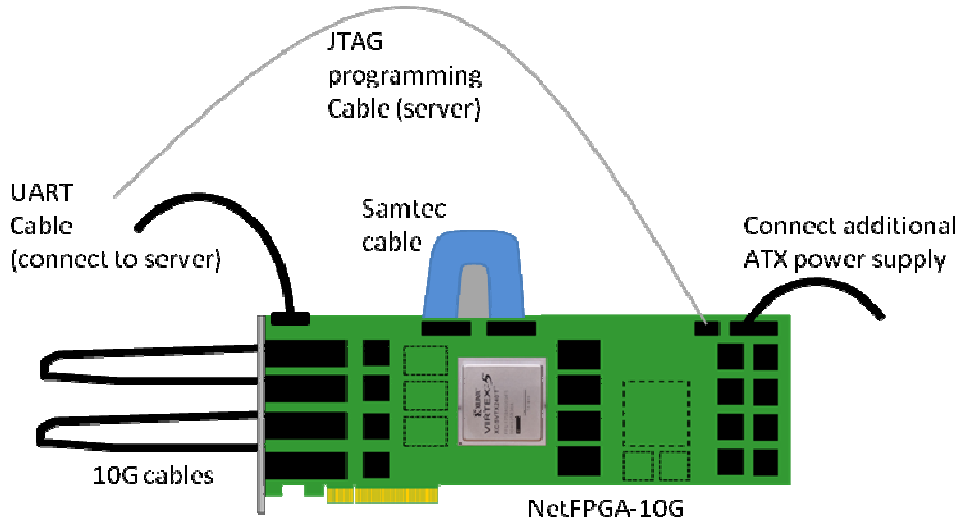


- set SW9 to PCIe (make sure the switch is fully in the left position)

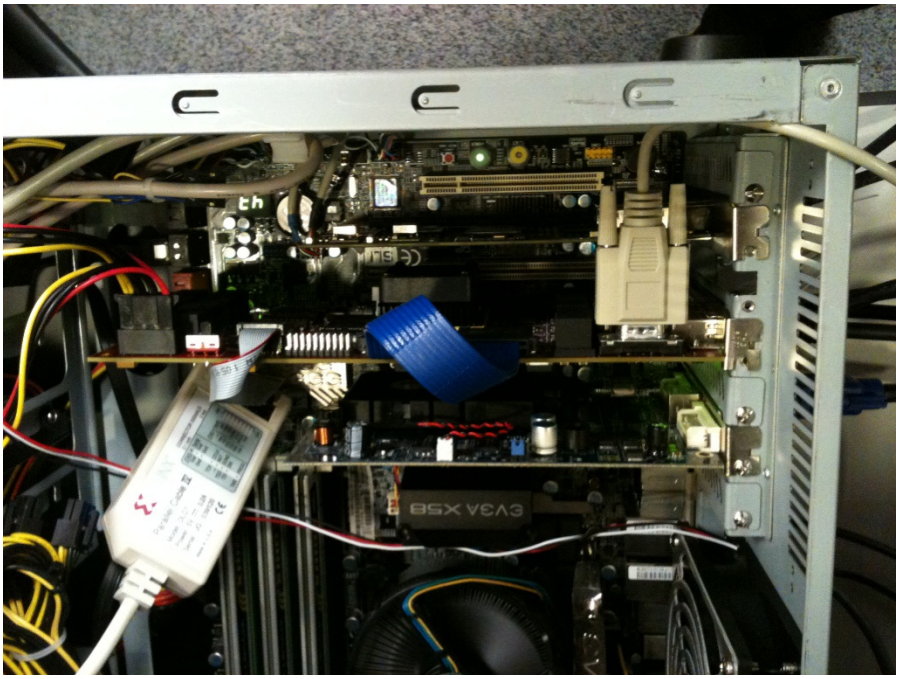
- connect auxiliary power from ATX to the NetFPGA-10G board
- SW1: SEL0, SEL1, M2, M1, M0, N2, N1, N0 are set to off, off, off, on, on, on, off, off
- SW6: SEL0, SEL1, M2, M1, M0, N2, N1, N0 are set to off, off, off, on, off on, off, on
- SW3: M0, M1, M2 is set to on, on, on
- SW10: SEL0, SEL1, SEL2 are set to on, off, off



The picture below indicates the necessary connections to the board once deployed in the server after the card was included.



The picture below shows a card fitted inside the server:



3. Test procedure

a. Standalone mode

Power-up the board and check that all power rails are ok. For this all power LEDs should be illuminated (whereby the brightness does vary) – see picture below:

Then run Xilinx Impact to program FPGA and CPLD:

- cpld.jed for the CPLD component
- prod_test.bit for the V5TX240T FPGA

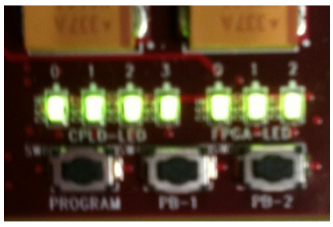
Once the CPLD and FPGA are programmed, the LEDs reflect the following status:

- FPGA LED0: is a heartbeat signal derived from the system clock. If this LED is not flashing, then there is no need to continue any further as it is highly unlikely that the test will run.

- FPGA LED2: When illuminated then this indicates that all tests with the exception of the Samtec interface have passed. This includes SRAM, RLDRAM, all 10G interfaces, CPLD and platform flash interface, power and clocks. Further, in standalone mode the PCIe interface cannot be tested, and the UART interface can only be tested in conjunction with a terminal device (see below)

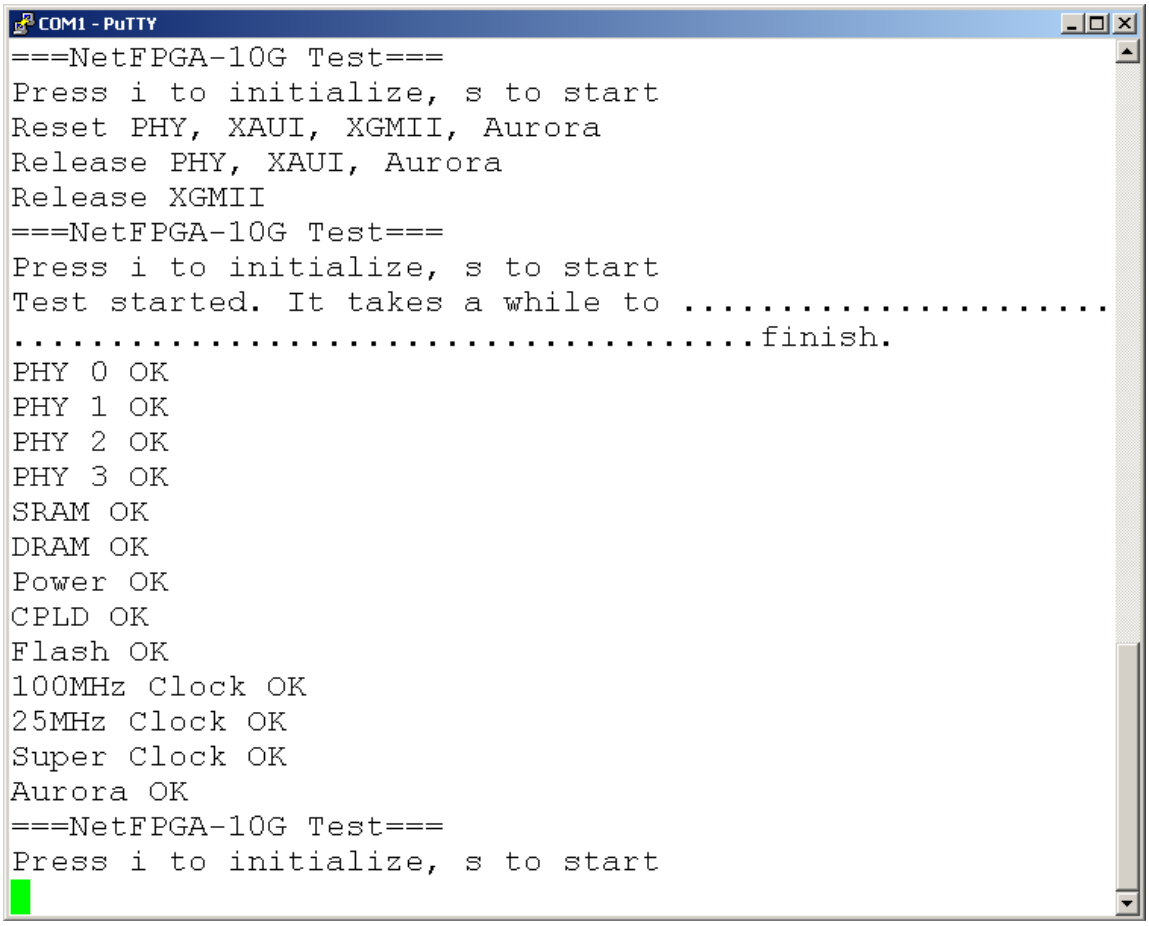
- FPGA LED1: This illuminates when the Samtec interface loopback test has passed (which can only be the case if the cable is fitted)

- CPLD LEDs 0 and 2 should be illuminated (PCI reset and flash device ok), CPLD LED1 illuminates once the FPGA is successfully programmed, and CPLD LED3 flashes when the clock to the CPLD is active and all power levels are ok.



After you've hooked up the host computer to the board over UART, startup a terminal over the serial connection (for instance, using minicom in linux), and

connect to the board at 9600bps, 8 databits, no parity, stop bits 1, without flow control. The UART interface can be used to control the test and review the status. It gives more detailed information on the test outcome than the LEDs and it also allows the user to rerun the test as many times as desired. The output looks something like this:



Press “i” to initialize the board. This resets all testbenches inside the FPGA and peripheral devices, and initializes the 10G PHY devices. When pressing “s” the tests rerun.

When the test passes successfully, the outputs should appear as above. (Note that if cables are not plugged-in for either the 10G interfaces or the Samtec interfaces, the corresponding interface test will fail). For more details on the various interface tests please refer to section 4.

b. Server mode

To test the board in a linux server, follow these procedures:

1. Add a “memmap=256M$0x5f700000” to the end of your current kernel’s boot options. This is for allocating a fixed region of kernel memory, used for the PCIe DMA test. The steps for doing that are roughly the following, although it will vary between linux distributions.

    a. As root, edit /boot/grub/grub.conf.

b. Locate the entry for your particular kernel (the “default=N” says that your default kernel is the Nth entry).

c. Find line starting with “kernel”.

d. Append “memmap=256M$0x5f700000” to the end of that line.

e. The result should look like the figure below.

```
title CentOS (2.6.18-194.17.1.el5)
        root (hd0,0)
        uppermem 524288
        kernel /vmlinuz-2.6.18-194.17.1.el5 ro root=/dev/VolGroup00/LogV
ol00 rhgb quiet vmalloc=256M memmap=256M$0x5f700000
        initrd /initrd-2.6.18-194.17.1.el5.img
```

2. Save grub.conf and reboot.

3. Verify the option was applied correctly.

   a. cat /proc/cmdline

   b. you should see something like:

```
ro root=/dev/VolGroup00/LogVol00 rhgb quiet vmalloc=256M memmap=256M$0x5
f700000
                                  _
```

4. If you haven’t got the board installed in the server already, shut down the server, install the board, and bring the server back up again. Make sure that the power switch on the board is set to accept power from the PCIe bus.

5. Program the FPGA with the prod_test.bit design for the FPGA, and the cpld.jed design for the CPLD.

6. Reboot.

7. At the terminal, type:

   a. lspci –vxx | grep Xilinx –A3

   b. If the “lspci” command is not found, then it may not be in your path. Try checking /sbin

   c. You should see something like below (probably with different addresses):

```
03:00.0 RAM memory: Xilinx Corporation Unknown device 4243 (rev 02)
        Subsystem: Xilinx Corporation Unknown device 0007
        Flags: bus master, fast devsel, latency 0, IRQ 255
        Memory at dc000000 (32-bit, non-prefetchable) [size=16M]
        Memory at ddff0000 (32-bit, non-prefetchable) [size=64K]
```

   d. If not, please check that the board is properly installed and powered by the ATX power supply.

8. At this stage, please doublecheck all LEDs as far as you can see them. First of all, all power LEDs should be lit up:

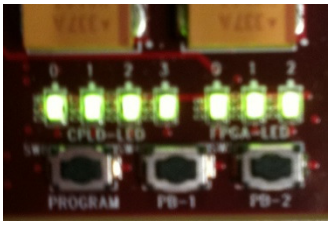
9. Now, if possible, check the FPGA and CPLD LEDs

    a. FPGA LED0: is a heartbeat signal derived from the system clock. If this LED is not flashing, then there is no need to continue any further as it is highly unlikely that the test will run.

    b. FPGA LED1: This illuminates when the Samtec interface loopback test has passed (which can only be the case if the cable is fitted).

    c. FPGA LED2: When illuminated then this indicates that all tests with the exception of the Samtec interface have passed. This includes SRAM, RLDRAM, all 10G interfaces, CPLD and platform flash interface, power and clocks. Further, in standalone mode the PCIe interface ca not be tested, and the UART interface can only be tested in conjunction with a terminal device (see below).

    d. CPLD LEDs 0 and 2 should be illuminated (PCI reset and flash device ok), CPLD LED1 illuminates once the FPGA is successfully programmed, and CPLD LED3 flashes when the clock to the CPLD is active and all power levels are ok.



10. Extract the production test, go to the root folder, make, and run the production test:

    a. tar –xvzf prod_test_sw.tar.-gz

    b. cd prod_test_sw/

    c. make

    d. cd scripts/

e. sudo ./production_test.py

11. The output will look something like this:

```
NetFPGA-10G Production Test
Version: 1.0
Time: 2010-10-27 02:13:18.852668

Running UART test...
UART test finished!
---------- UART Test Report ----------
UART Test Result: PASS

Running PCIe DMA test... (will take 10 seconds)...
PCIe DMA test finished!
---------- PCIe DMA Test Report ----------
DMA Test Result:              PASS
DMA Transfers:                69451 totaling 142.24 MB

Checking FPGA system status registers...
---------- FPGA System Report ----------
Address  Name                      Value
0x00000: HW Version                0x00000104    PASS: Detected Supported Board Revision
0x00004: CLOCK ok                  0x00000007    PASS
0x00008: QDRII ok                  0x00000015    PASS
0x0000c: PWR ok                    0x00000001    PASS
0x00010: CPLD/Flash ok             0x00000007    PASS
0x00014: RLDRAMII ok               0x0000035a    PASS
0x00018: 10G if 0 link             0x00000001    PASS
0x00024: 10G if 0 er count         0x00000000    PASS
0x00028: 10G if 1 link             0x00000001    PASS
0x00034: 10G if 1 er count         0x00000000    PASS
0x00038: 10G if 2 link             0x00000001    PASS
0x00044: 10G if 2 er count         0x00000000    PASS
0x00048: 10G if 3 link             0x00000001    PASS
0x00054: 10G if 3 er count         0x00000000    PASS
0x0005c: Samtec 0 link             0x00000001    PASS
0x00064: Samtec 1 link             0x00000001    PASS

Production test finished.
```

a. This result explains that the UART port is working, DMA is working over PCIe, there's a problem with the RLDRAMII subsystem, and link 2 and 3 are not connected. Don't worry about running the test without links connected, the UART port connected, the Samtec connector connected, etc… the test will still proceed anyway and simply report a failure on those parts.

12. If you would like the test to generate a report in the output/reports/ directory, you can run the production test with an argument which is the report's filename (note that you will not see output on stdout in this case):

a. sudo ./production_test.py board_55635.txt

The board's UART port is tested by sending a short message over it to the microblaze processor on the FPGA, which will respond with another message, which is then checked on the host side against an expected string. The PCIe DMA test sends data continuously over PCIe to the board where the data is looped back and sent back to the host. This goes on for about 10 seconds, while the host checks that the data received equals the data sent. Finally, several FPGA side monitor registers are read out and whose values are validated. The results of the validation process are printed in the rightmost column as either PASS or FAIL.

4. Production test design

The following section describes in more details how the production test verifies the various parts of the board. The production test consists of a number of components which are then described in more detail in the following subsections:

- QDRII memory interface test
- RLDRAMII memory interface test
- 10G SFP+/PHY interface test
- Samtec interface
- Clock & power test
- CPLD test
- Flash test
- PCIe test
- UART test

a. QDR memory test

This test exercises the SRAM interface with 100% utilization @ 250MHz. The test writes and reads every memory location in bursts of 4 with data values. The data values are comprised of 9bit counters. Result if fed out over UART, PCIe and LED

b. RLDRAM memory test

This test exercises the RLDRAM interface with 100% utilization @ 200MHz. Result is reported out on UART interface, PCIe and LED.

c. 10G SFP+/PHY test

This test sends and receives packets at close to 100% line rate in loopback mode. Interfaces need to be wired A-B and C-D with direct attach cables as was shown in section 1. The test generates packets at line rate for each XAUI transmit interface and implements a checker on each XAUI receive interface. The test design logs tx and rx counts and rx error counts, verifies PMA, PCS and XAUI link status. Only if all results are as expected, the test passes. Output is reported via UART, PCIe and LED.

d. Samtec interface test

To test the Samtec interfaces, we have implemented an Aurora testbench which generates packets at 6.25Gbps line rate per GTX, transmits them over the loopback cable, and receives and checks them.

e. Clock and power test

This test is simply checking the clock frequencies (100MHz, 25MHz, Super clock) to be within range and checking the power ok signals from the DC2DCs. Results are reported over UART, PCIe and LED.

f. CPLD test

This test shifts a '1' across the wide CPLD-FPGA interface and checks its results continuously. Results are reported over UART, PCIe and LED.

g. Flash test

The CPLD is continuously reading back device information from the platform flash devices. While these values are returned as expected, the test passes. Results are passed to the FPGA and from there reported over UART, PCIe and LED.

h. PCIe test

This test can only be conducted in server mode. The host CPU is issuing data transfers to and from the board over the PCIe and checking the returned values. The result of this test can only be seen on the output of the production test software executed on the server.

i. UART test

In standalone mode, the UART interface is a debug output and used for the production test report itself. In server mode, the host issues a message to the board via UART and checks the returned answer is as expected.

5. Shortcomings

The production test aims to test the board as thoroughly as possible, however there are certain parts of the design which can currently not be tested:

a. The operation of the 10G interfaces are verified with SFP+ direct attach cables.
b. Some of the clock inputs to the GTXs cannot be verified through this production test.
c. SRAM is verified up to 250MHz.
d. RLDRAM is verified up to 200MHz.
e. Samtec interface is verified up to 6.25Gbps.
f. Configuration from flash and programming to flash is currently not supported.