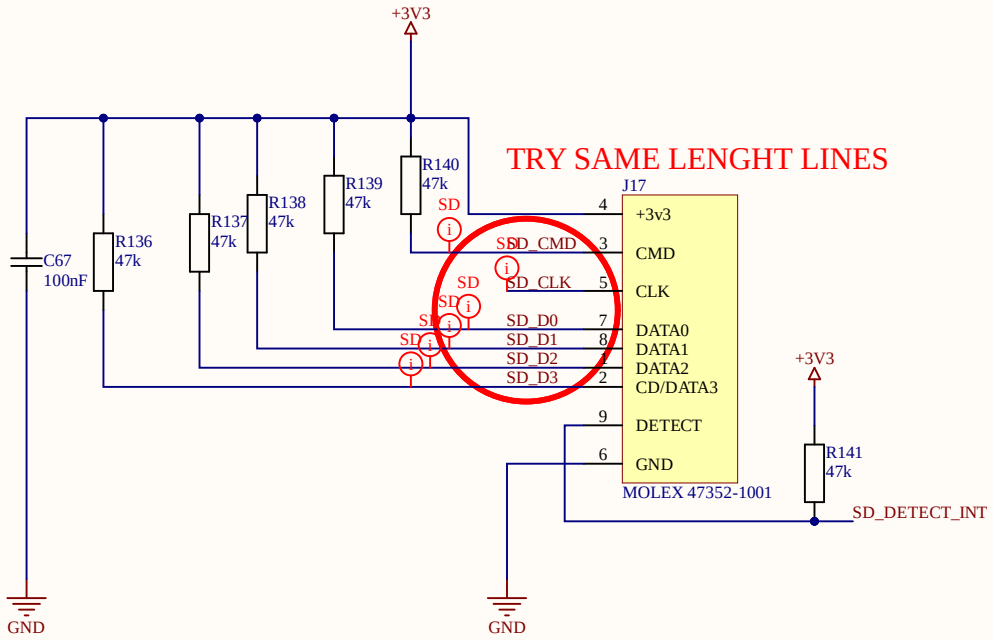
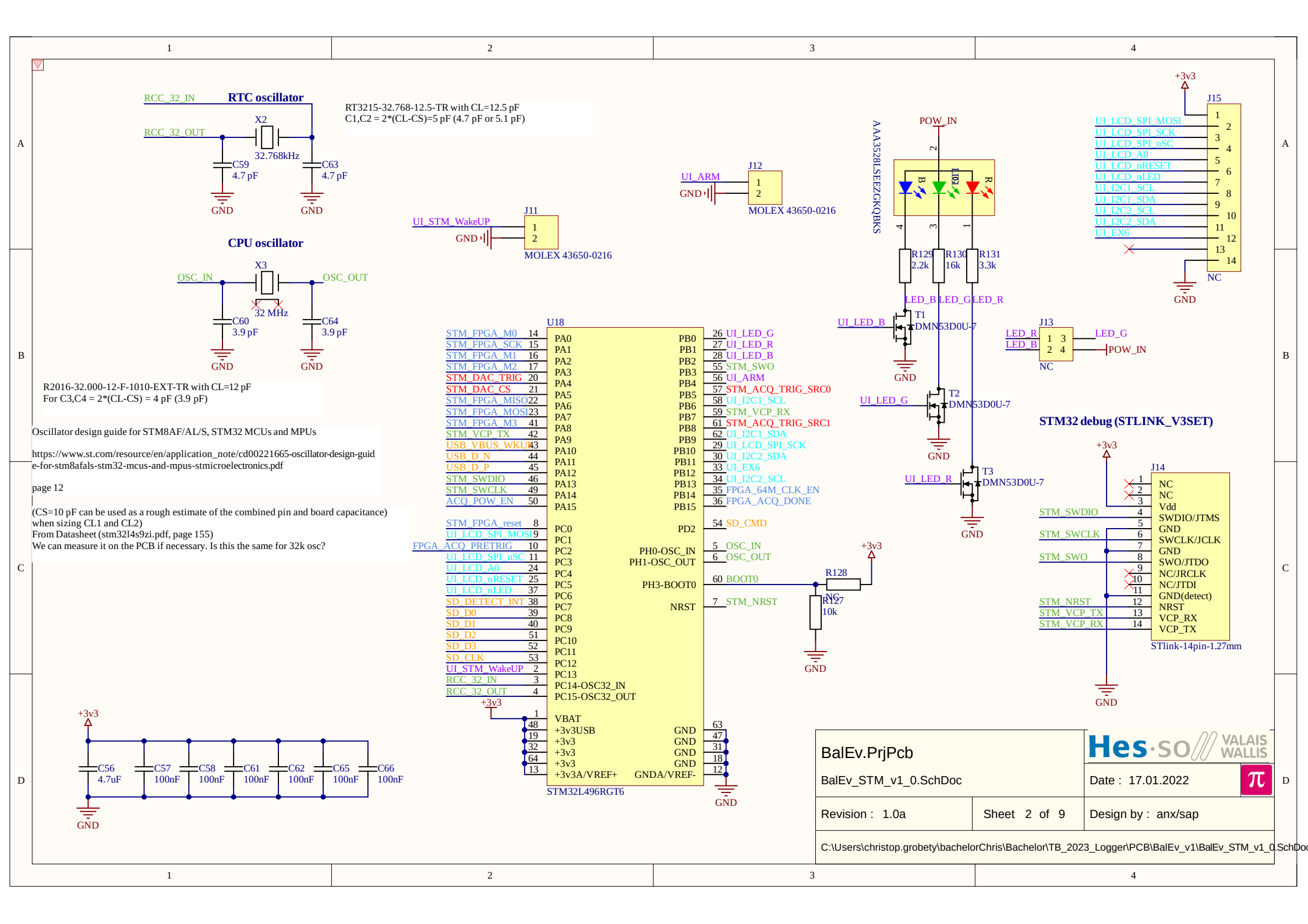
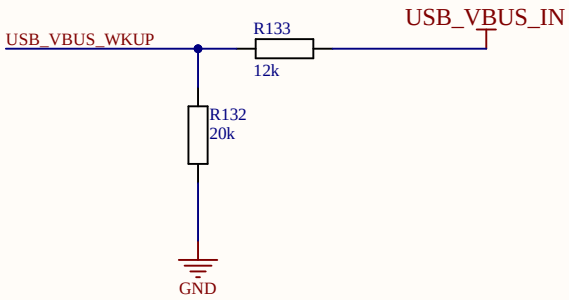
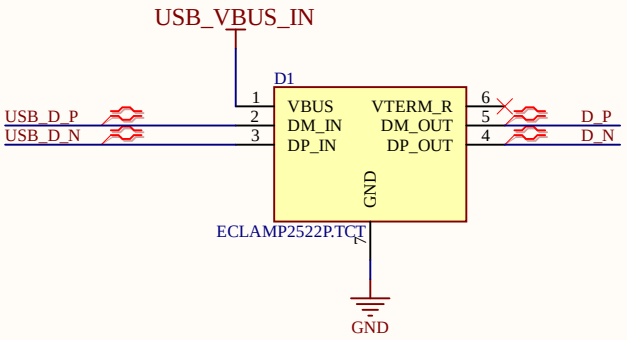
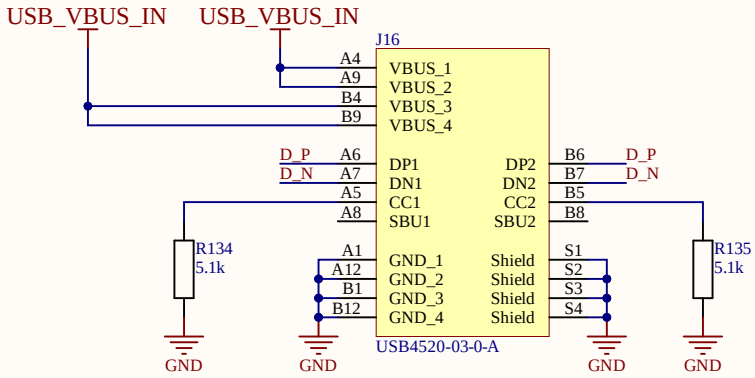


BalEv.PrjPcb		Hes·SO VALAIS WALLIS
BalEv_SD_card_v1_0.SchDoc		Date : 17.01.2022
Revision : 1.0a	Sheet 1 of 9	Design by : anx/sap
C:\Users\christop.grobety\bachelorChris\Bachelor\TB_2023_Logger\PCB\BalEv_v1\BalEv_SD_card_v1_0.Sch		


RTC oscillator
RCC_32_IN
RCC_32_OUT
X2
32.768kHz
C59
4.7 pF
C63
4.7 pF
GND
GND
RT3215-32.768-12.5-TR with CL=12.5 pF
C1,C2 = 2*(CL-CS)=5 pF (4.7 pF or 5.1 pF)
CPU oscillator
OSC_IN
OSC_OUT
X3
32 MHz
C60
3.9 pF
C64
3.9 pF
GND
GND
R2016-32.000-12-F-1010-EXT-TR with CL=12 pF
For C3,C4 = 2*(CL-CS) = 4 pF (3.9 pF)
Oscillator design guide for STM8AF/AL/S, STM32 MCUs and MPUs
https://www.st.com/resource/en/application_note/cd00221665-oscillator-design-guide-for-stm8afals-stm32-mcus-and-mpus-stmicroelectronics.pdf
page 12
(CS=10 pF can be used as a rough estimate of the combined pin and board capacitance)
when sizing CL1 and CL2)
From Datasheet (stm32l4s9zi.pdf, page 155)
We can measure it on the PCB if necessary. Is this the same for 32k osc?
UI_ARM
GND
J12
MOLEX 43650-0216
UI_STM_WakeUP
GND
J11
MOLEX 43650-0216
U18
STM32L496RGT6
STM_FPGA_M0
STM_FPGA_SCK
STM_FPGA_M1
STM_FPGA_M2
STM_DAC_TRIG
STM_DAC_CS
STM_FPGA_MISO
STM_FPGA_MOSI
STM_FPGA_M3
STM_VCP_TX
USB_VBUS_WKUP
USB_D_N
USB_D_P
STM_SWDIO
STM_SWCLK
ACQ_POW_EN
STM_FPGA_reset
UI_LCD_SPI_MOSI
FPGA_ACQ_PRETRIG
UI_LCD_SPI_nSC
UI_LCD_A0
UI_LCD_nRESET
UI_LCD_nLED
SD_DETECT_INT
SD_D0
SD_D1
SD_D2
SD_D3
SD_CLK
UI_STM_WakeUP
RCC_32_IN
RCC_32_OUT
UI_LED_G
UI_LED_R
UI_LED_B
STM_SWO
STM_ACQ_TRIG_SRC0
STM_VCP_RX
STM_ACQ_TRIG_SRC1
UI_I2C1_SCL
UI_LCD_SPI_SCK
UI_I2C2_SDA
UI_I2C2_SCL
UI_EX6
FPGA_64M_CLK_EN
FPGA_ACQ_DONE
SD_CMD
OSC_IN
OSC_OUT
BOOT0
STM_NRST
+3v3
R128
NC
R127
10k
GND
POW_IN
AAA3528LSEEZGKQBKS
R129
2.2k
R130
16k
R131
3.3k
LED_B
LED_G
LED_R
T1
DMN53D0U-7
T2
DMN53D0U-7
T3
DMN53D0U-7
GND
J13
LED_R
LED_B
LED_G
POW_IN
NC
J15
UI_LCD_SPI_MOSI
UI_LCD_SPI_SCK
UI_LCD_SPI_nSC
UI_LCD_A0
UI_LCD_nRESET
UI_LCD_nLED
UI_I2C1_SCL
UI_I2C1_SDA
UI_I2C2_SCL
UI_I2C2_SDA
UI_EX6
NC
STM32 debug (STLINK_V3SET)
J14
NC
NC
Vdd
SWDIO/JTMS
GND
SWCLK/JCLK
GND
SWO/JTDO
NC/JRCLK
NC/JTDI
GND(detect)
NRST
VCP_RX
VCP_TX
STLink-14pin-1.27mm
C56
4.7uF
C57
100nF
C58
100nF
C61
100nF
C62
100nF
C65
100nF
C66
100nF
BalEv.PrjPcb
BalEv_STM_v1_0.SchDoc
Hes·so VALAIS WALLIS
Date : 17.01.2022
Revision : 1.0a
Sheet 2 of 9
Design by : anx/sap
C:\Users\christop.grobety\bachelorChris\Bachelor\TB_2023_Logger\PCB\BalEv_v1\BalEv_STM_v1_0.SchDoc







BalEv.PrjPcb		Hes·SO VALAIS WALLIS
BalEv_USB_v1_0.SchDoc		Date : 17.01.2022
Revision : 1.0a	Sheet 3 of 9	Design by : anx/sap
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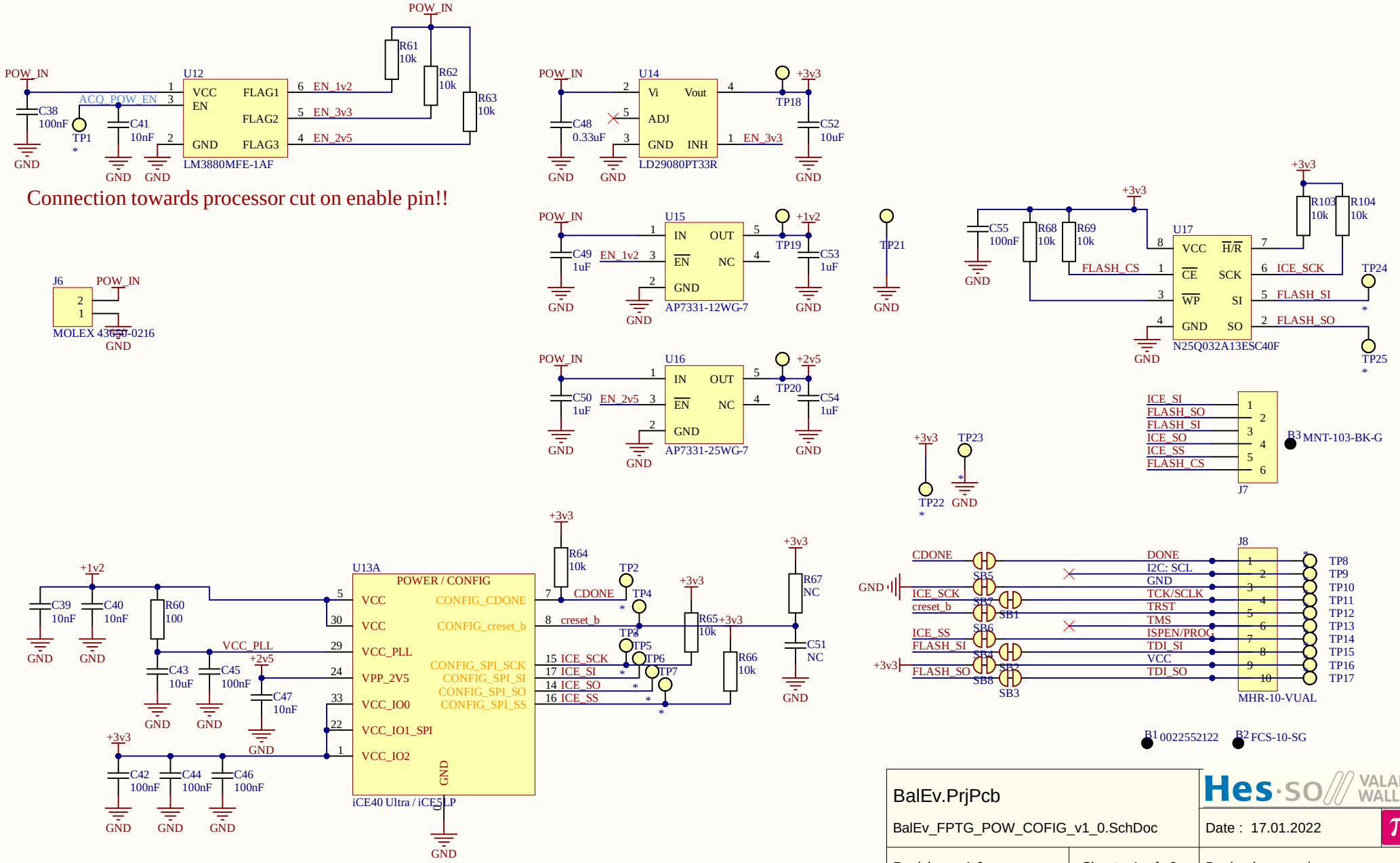

BalEv.PrjPcb		Hes·SO VALAIS WALLIS
BalEv_FPTG_POW_COFIG_v1_0.SchDoc		Date : 17.01.2022
Revision : 1.0a	Sheet 4 of 9	Design by : anx/sap
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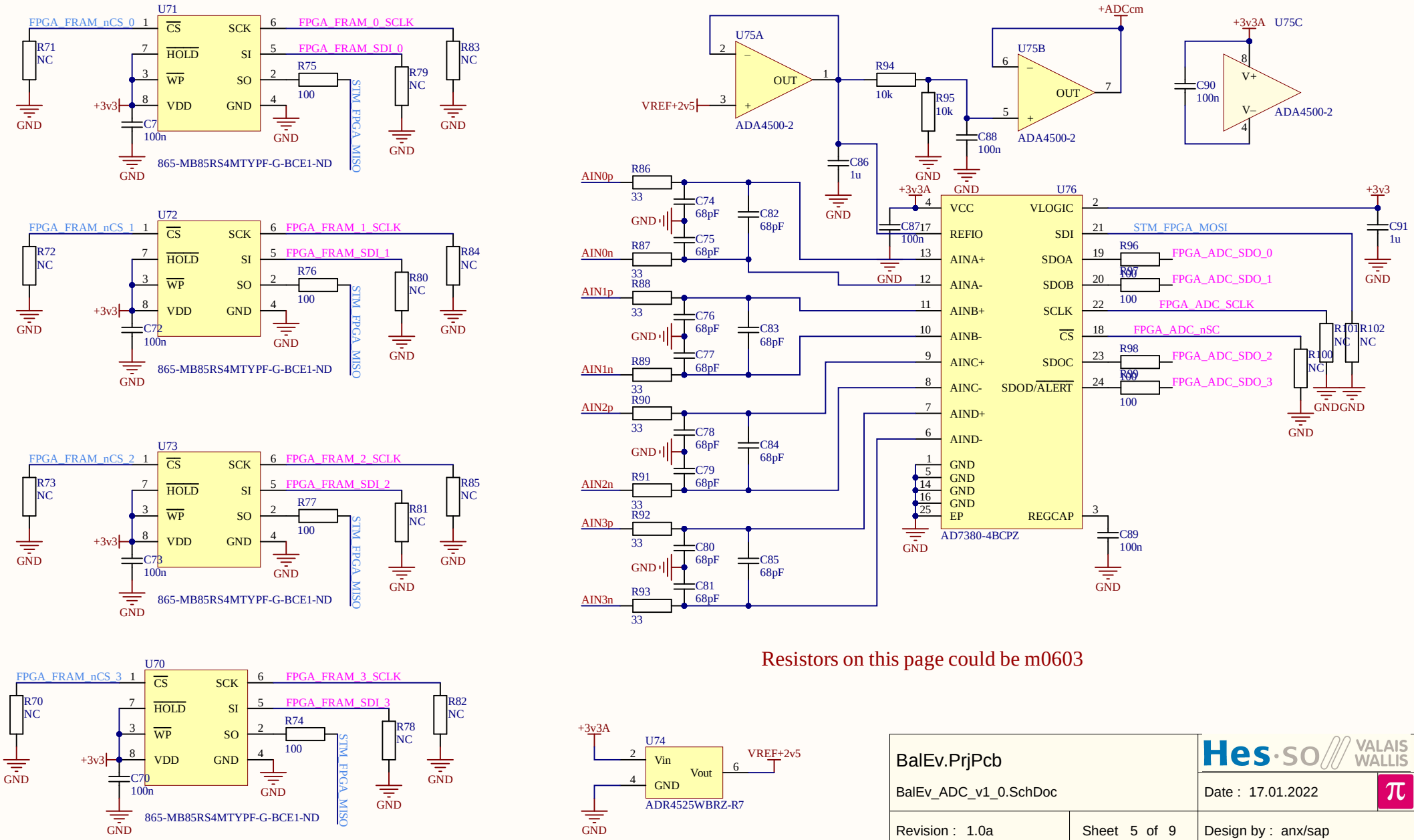

Resistors on this page could be m0603

BalEv.PrjPcb		Hes·so VALAIS WALLIS
BalEv_ADC_v1_0.SchDoc		Date : 17.01.2022
Revision : 1.0a	Sheet 5 of 9	Design by : anx/sap
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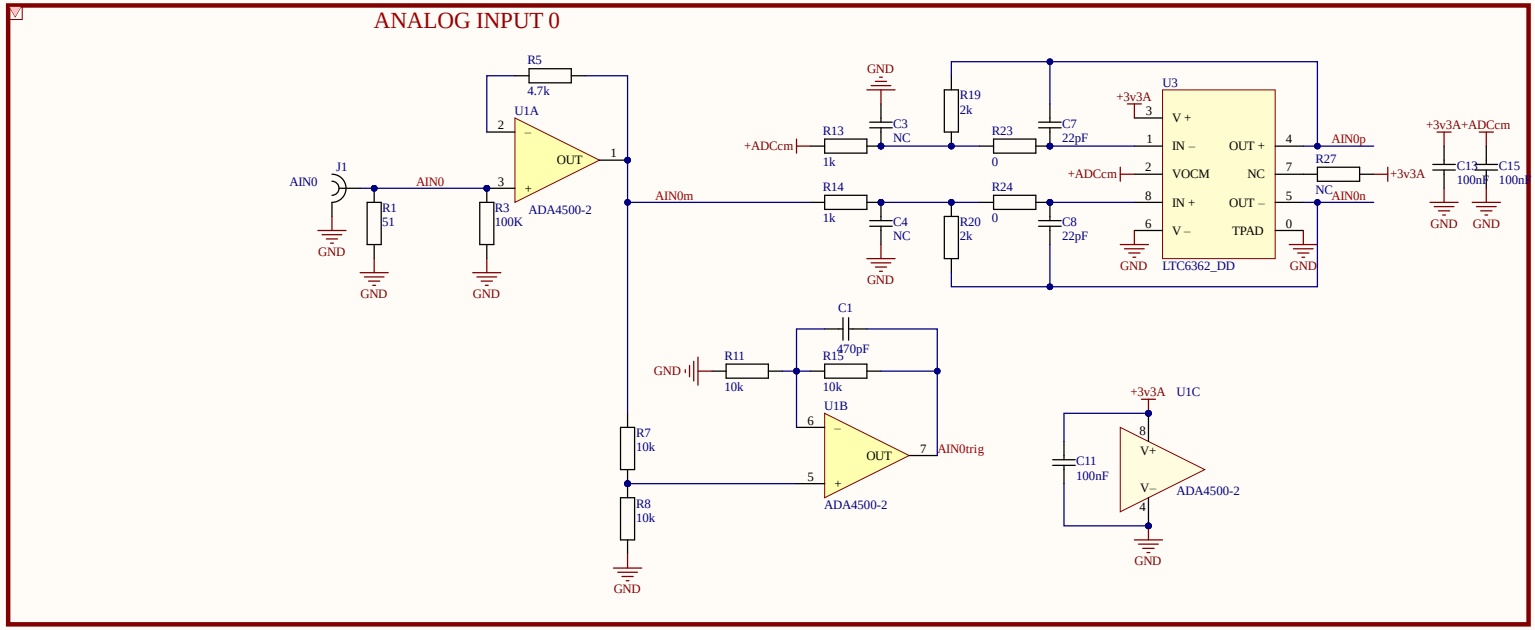

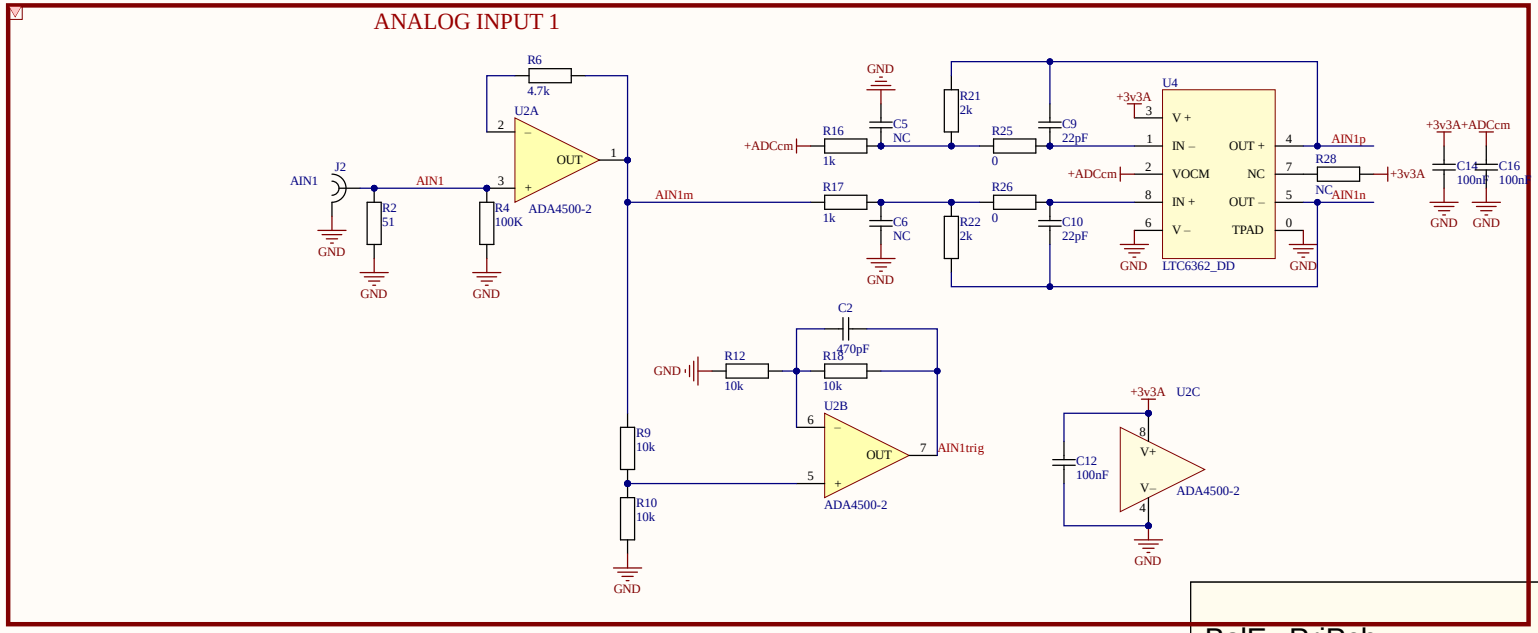

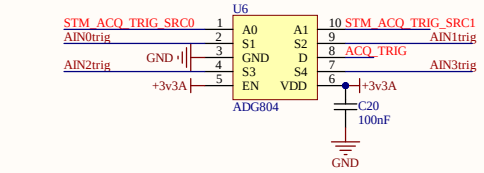

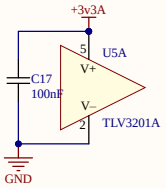

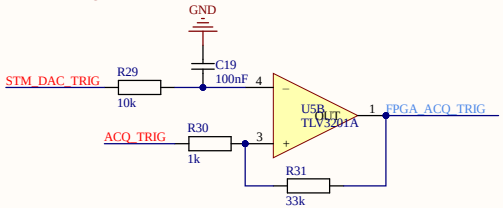

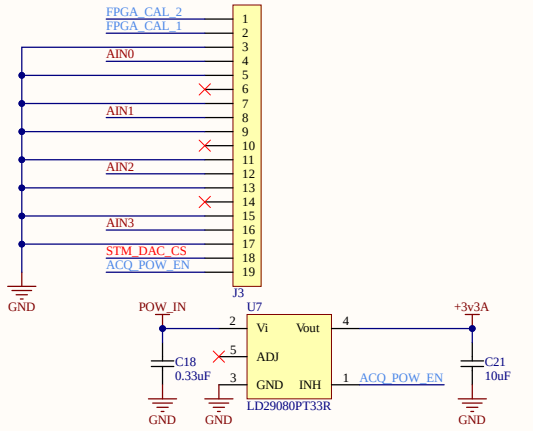

BalEv.PrjPcb		Hes·SO VALAIS WALLIS
BalEv_AINa_v1_0.SchDoc		Date : 17.01.2022
Revision : 1.0a	Sheet 6 of 9	Design by : anx/sap
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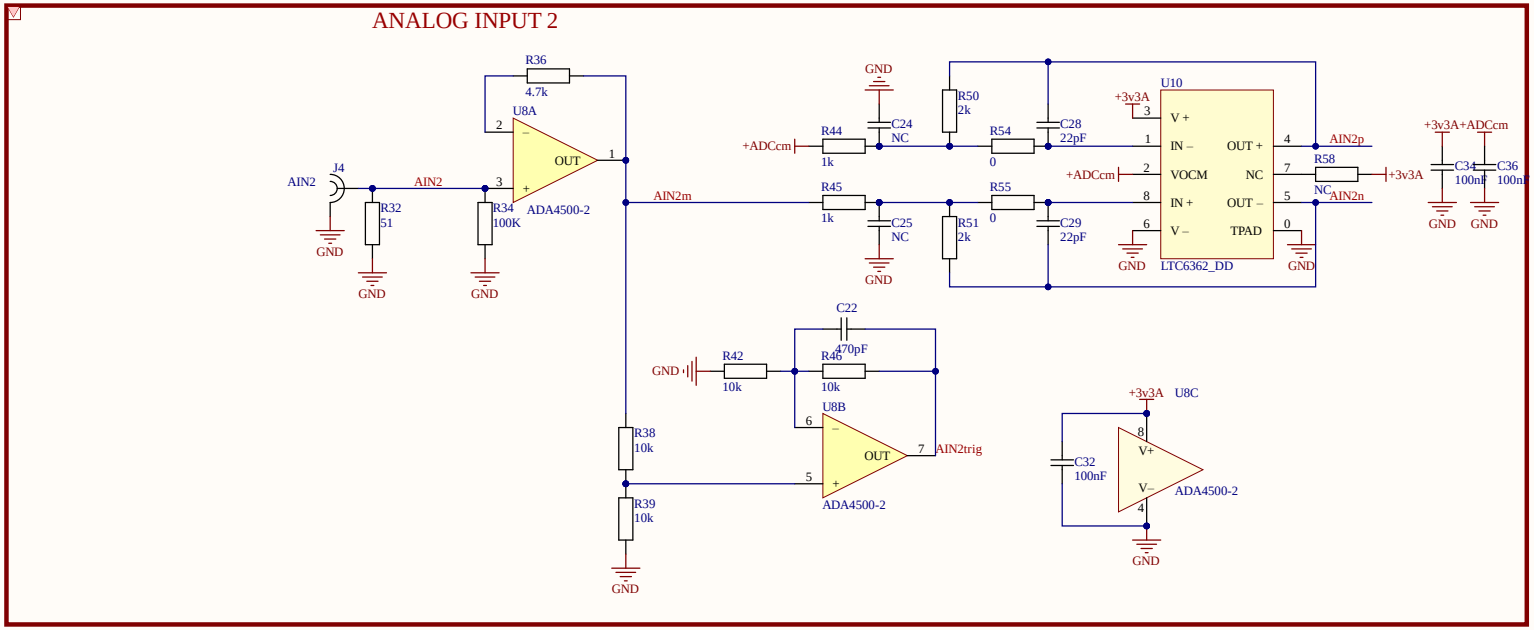
ANALOG INPUT 2



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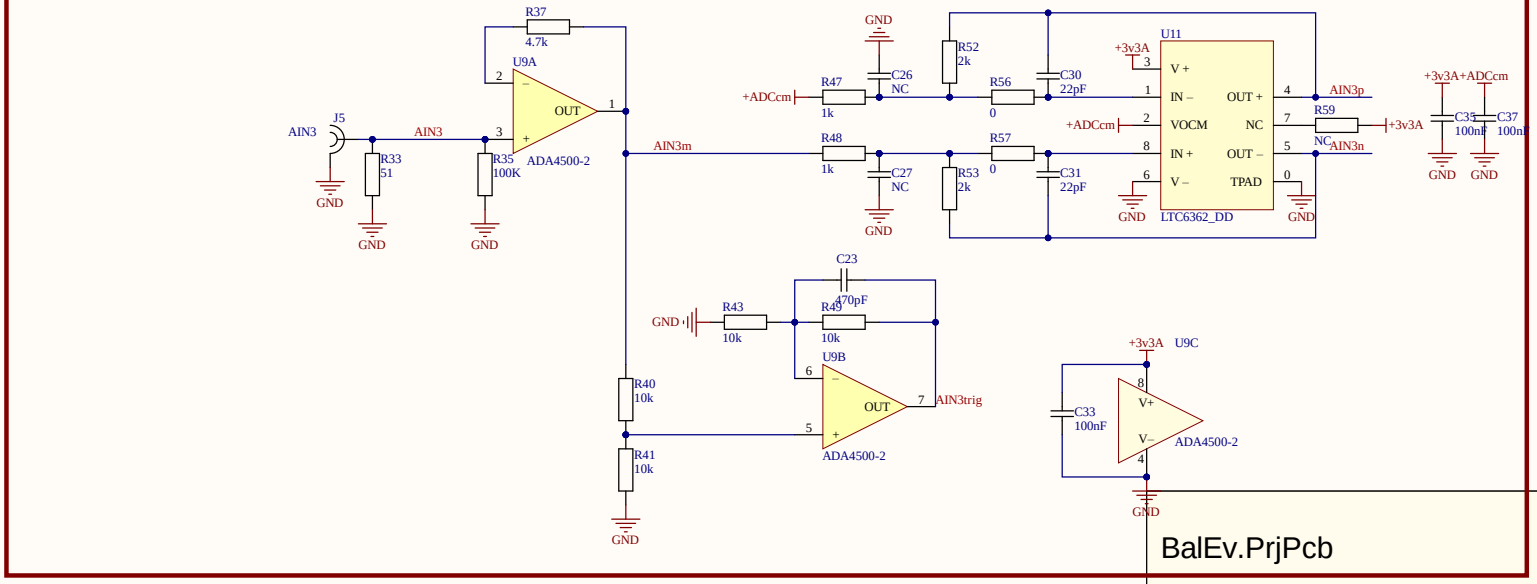

BalEv.PrjPcb		Hes·SO VALAIS WALLIS
BalEv_AINb_v1_0.SchDoc		Date : 17.01.2022
Revision : 1.0a	Sheet 7 of 9	Design by : anx/sap
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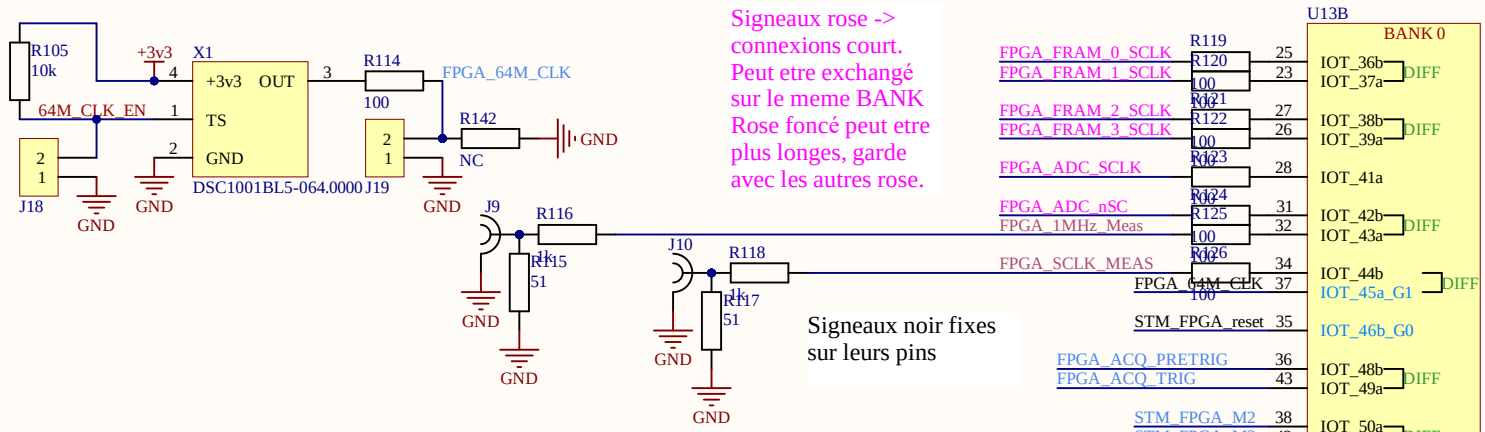
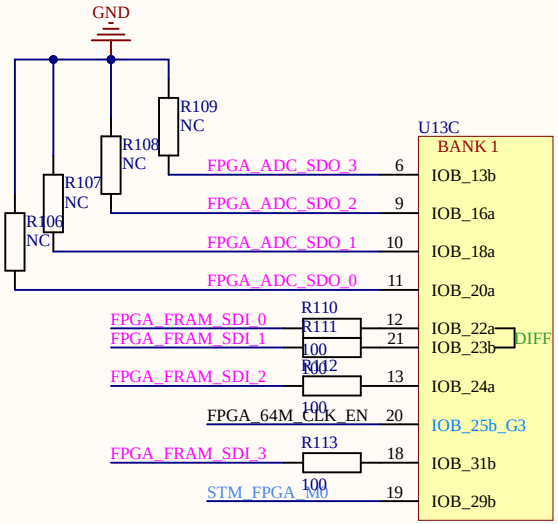
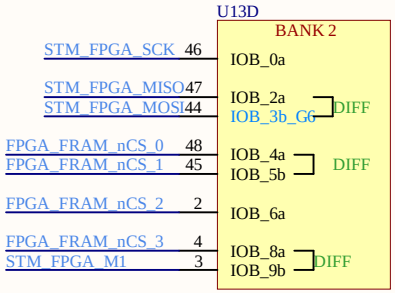


Resistors on this page could be m0603

Signeaux bleu peut etre exchangé





BalEv.PrjPcb		Hes·SO VALAIS WALLIS
BalEv_FPTG_IO_v1_0.SchDoc		Date : 17.01.2022
Revision : 1.0a	Sheet 8 of 9	Design by : anx/sap
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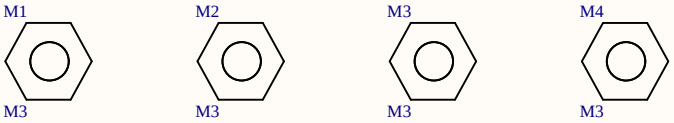

BalEv.PrjPcb		Hes·SO VALAIS WALLIS
BalEv_Mechanic_v1_0.SchDoc		Date : 17.01.2022
Revision : 1.0a	Sheet 9 of 9	Design by : anx/sap
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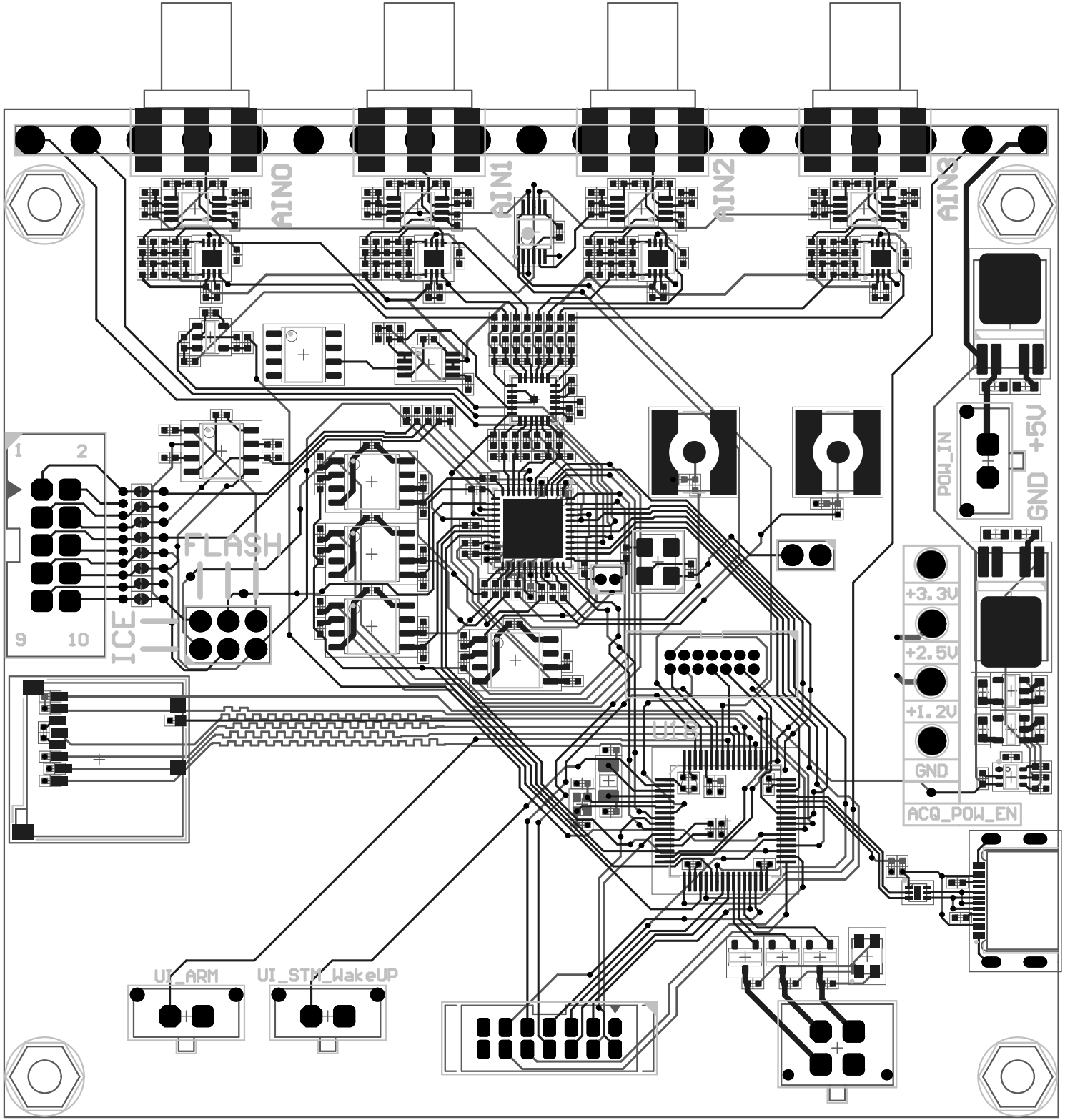
AIN0
AIN1
AIN2
AIN3
POW_IN
GND
+5V
FLASH
ICE
1
2
9
10
+3.3V
+2.5V
+1.2V
GND
ACQ_POW_EN
UI_ARM
UI_STM_WakeUP