Package List

```
LIBRARY ieee;
  USE ieee.std_logic_1164.all;
  USE ieee.numeric_std.all;

LIBRARY gates;
  USE gates.gates.all;
```

<company name>	Project:	hds
		<enter comments here>
Title:	<enter diagram title here>	
Path:	Bachelor/mainCircuit/struct	
Edited:	by christop.grobety on 11 août 2023	

Declarations

Ports:

```
acq_pretrig     : std_ulogic
acq_trig        : std_ulogic
adc_sdo         : std_ulogic_vector(3 downto 0)
clk             : std_ulogic
clk_en          : std_ulogic
fpga_m          : std_ulogic_vector(3 downto 0)
fpga_mosi       : std_ulogic
fpga_sck        : std_ulogic
rst             : std_uLogic
adc_nsc         : std_ulogic
adc_sclk        : std_ulogic
cal             : std_ulogic_vector(2 DOWNTO 1)
fpga_miso       : std_ulogic
fram_ncs        : std_ulogic_vector(3 DOWNTO 0)
fram_sclk       : std_ulogic_vector(3 DOWNTO 0)
fram_sdi        : std_ulogic_vector(3 DOWNTO 0)
meas_1mhz       : std_ulogic
out1            : std_ulogic
sclk_meas       : std_uLogic
```

Pre User:

Diagram Signals:

```
SIGNAL AW_CLOCK         : std_ulogic
SIGNAL MISO_AF          : std_ulogic
SIGNAL MISO_AW          : std_ulogic
SIGNAL Memory           : unsigned(18 DOWNTO 0)
SIGNAL T                : std_uLogic
SIGNAL adc_nscAF        : std_ulogic
SIGNAL adc_nscAW        : std_ulogic
SIGNAL adc_sclkAF       : std_ulogic
SIGNAL clock_1mhz       : std_ulogic
SIGNAL clock_32         : std_uLogic
SIGNAL count_go         : std_ulogic
SIGNAL enable           : std_ulogic
SIGNAL fram_ncsAF       : std_ulogic_vector(3 DOWNTO 0)
SIGNAL fram_ncsFW       : std_ulogic_vector(3 DOWNTO 0)
SIGNAL fram_sclkAF      : std_ulogic_vector(3 DOWNTO 0)
SIGNAL fram_sclkFW      : std_ulogic_vector(3 DOWNTO 0)
SIGNAL fram_sdiAF       : std_ulogic_vector(3 DOWNTO 0)
SIGNAL fram_sdiFW       : std_ulogic_vector(3 DOWNTO 0)
SIGNAL preTriggerValue  : unsigned(7 DOWNTO 0)
```