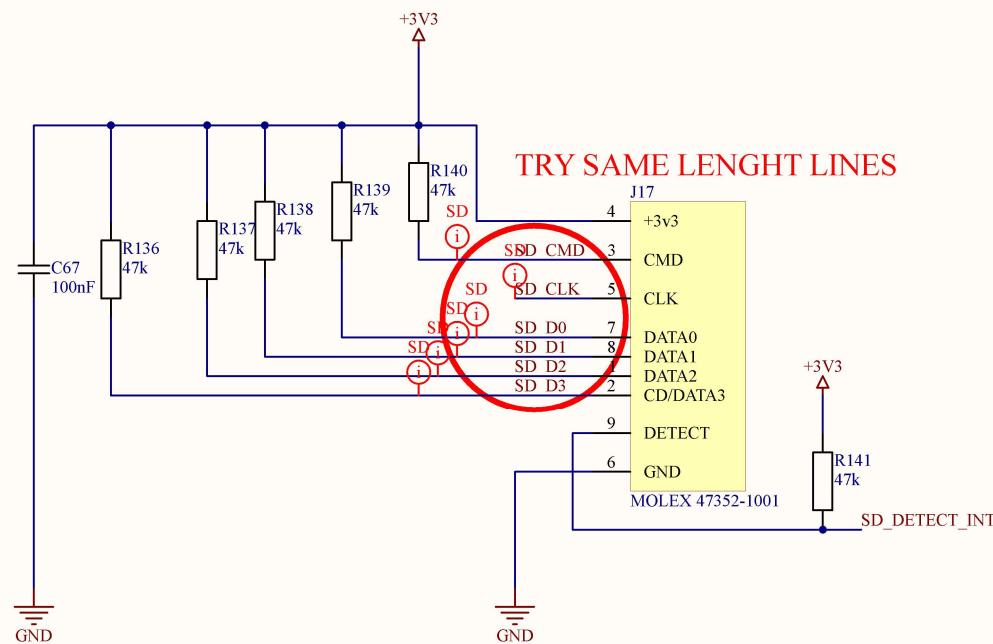


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BalEv.PrjPcb

BalEv_SD_card_v1_0.SchDoc

Hes-SO // VALAIS WALLIS

Date : 17.01.2022

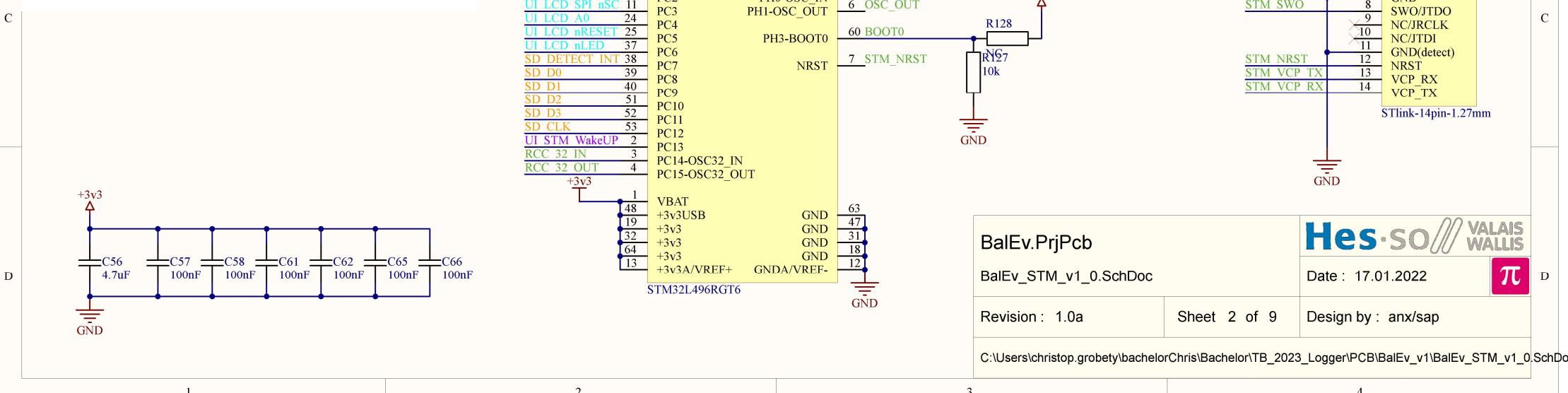
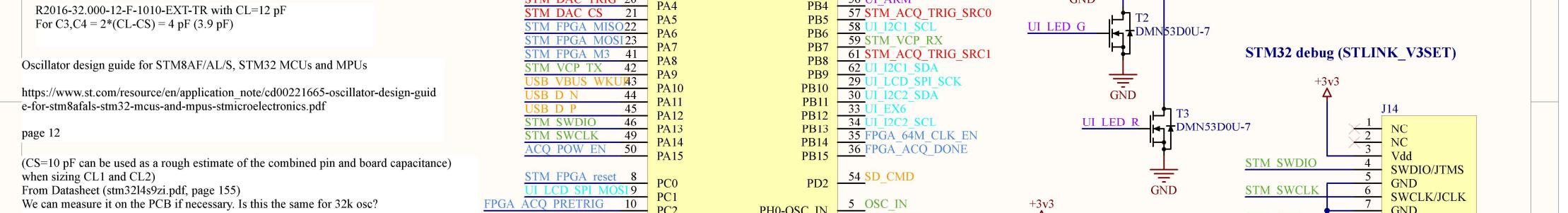
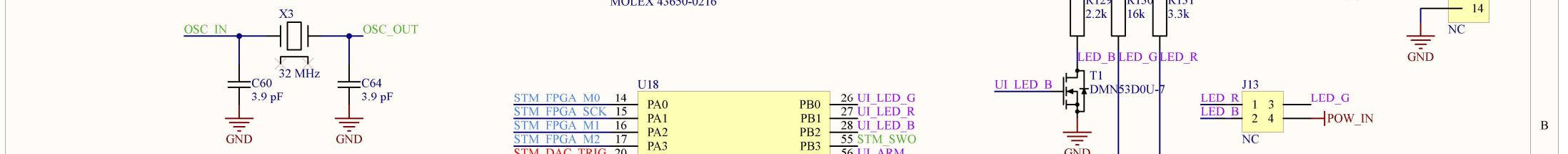
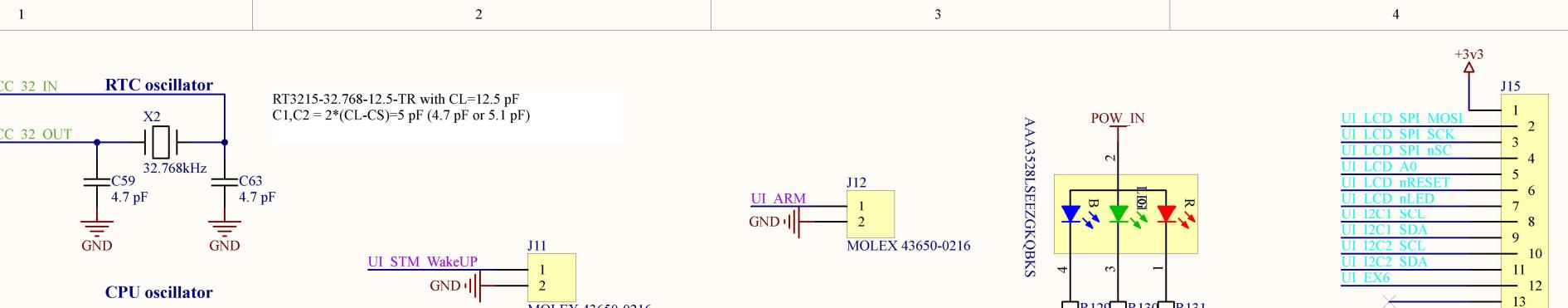


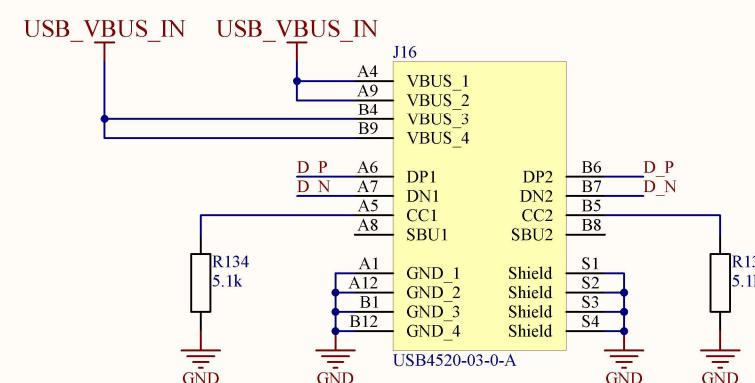
Revision : 1.0a

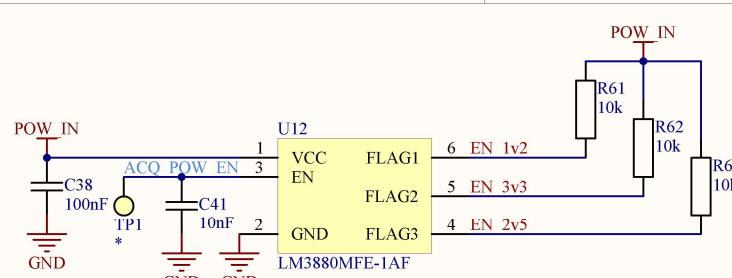
Sheet 1 of 9

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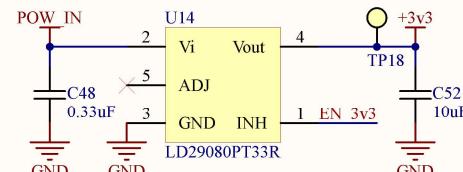
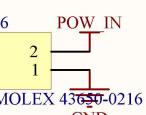
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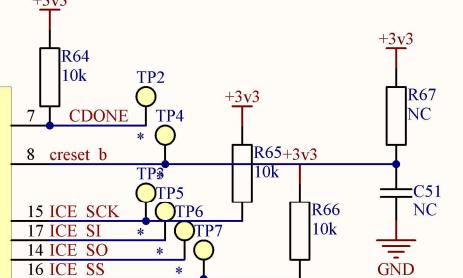
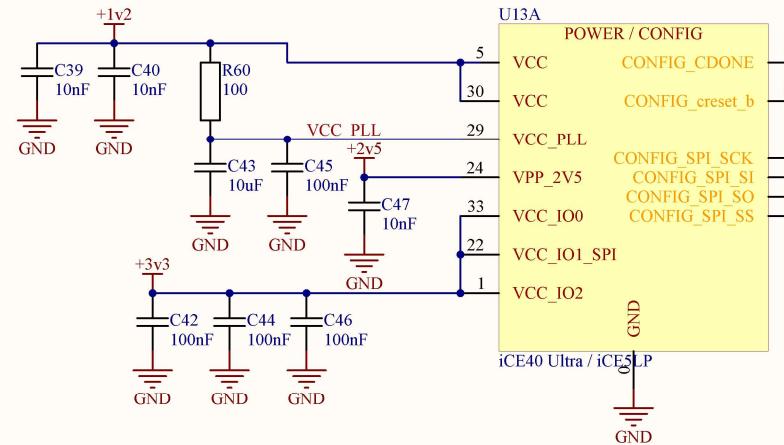
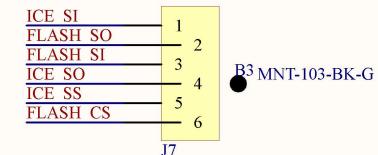
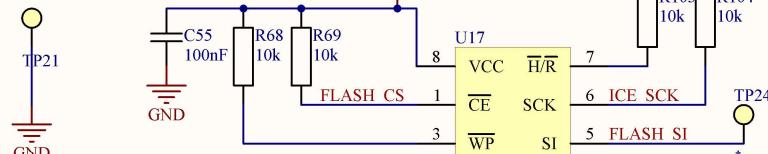
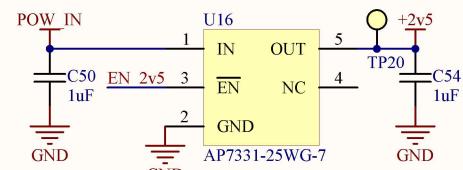
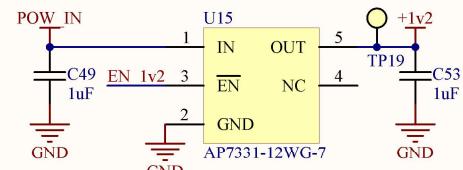




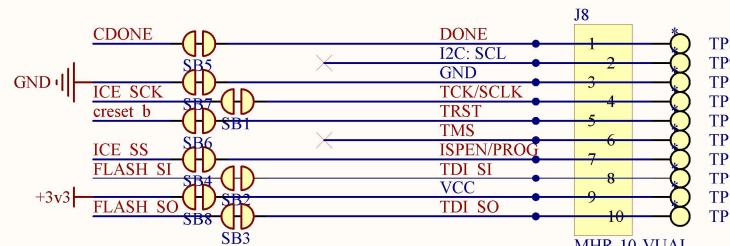
Connection towards processor cut on enable pin!!



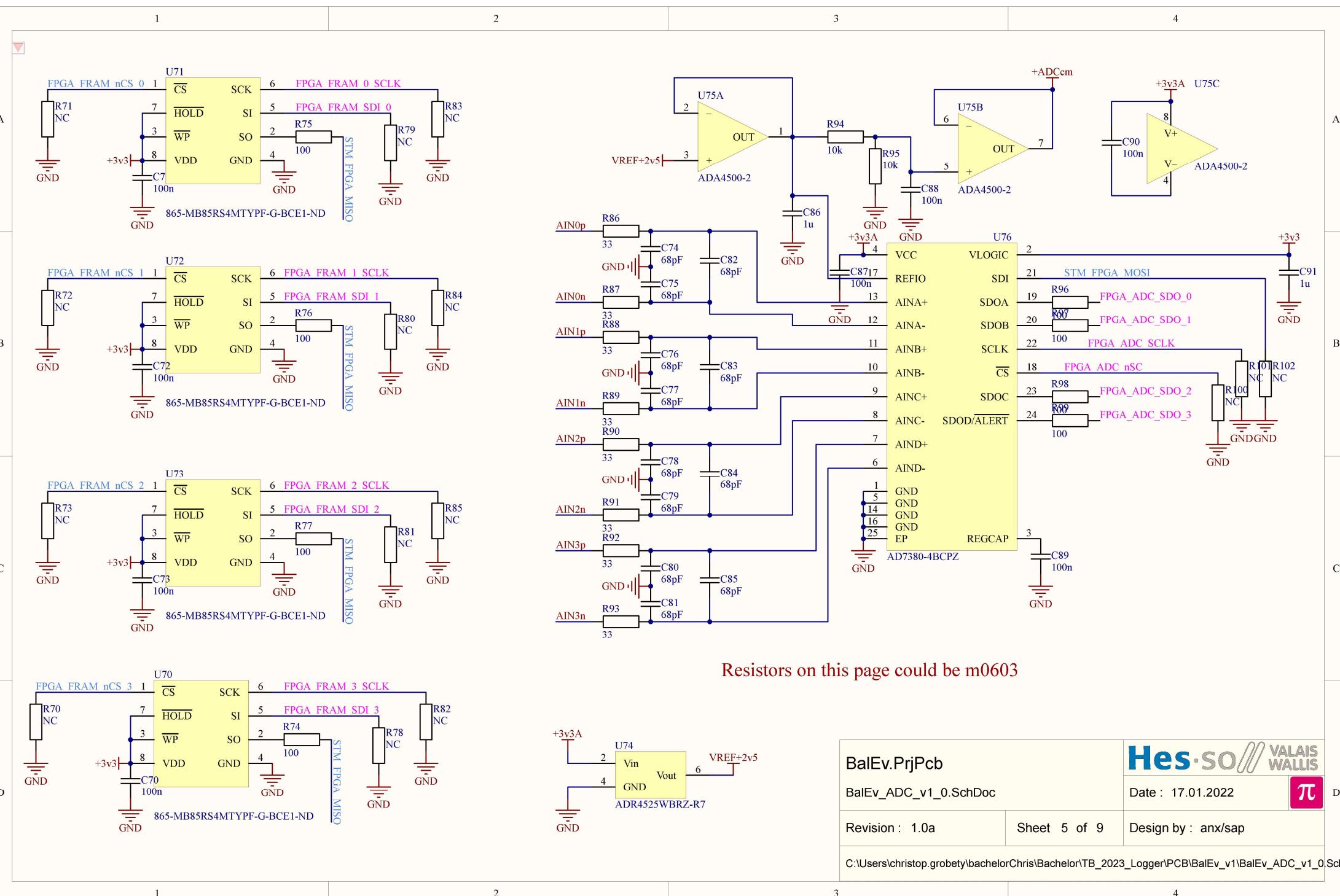
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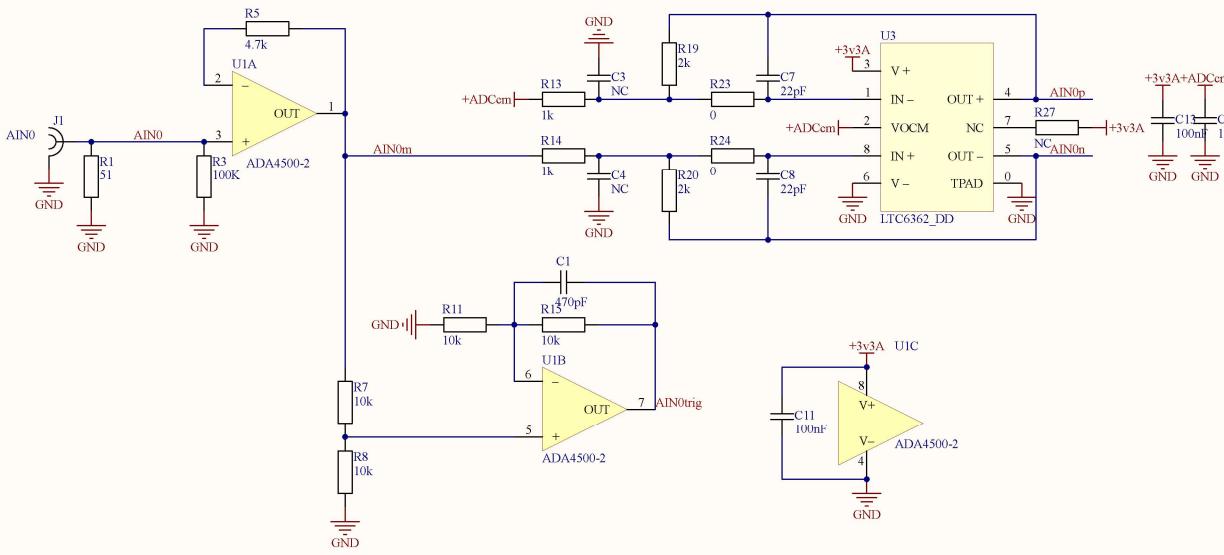


REMOVE R66

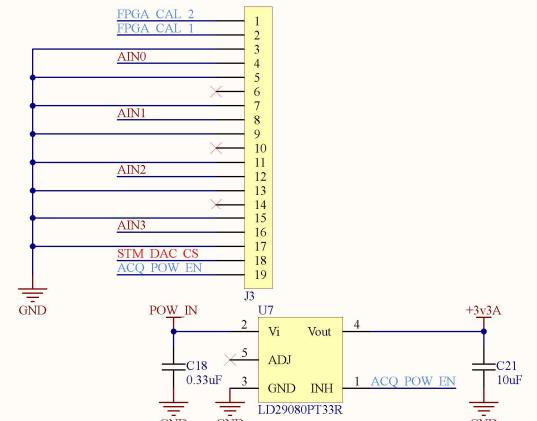
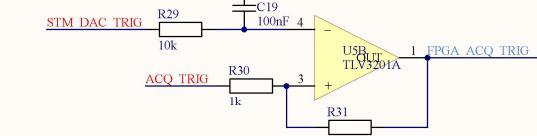
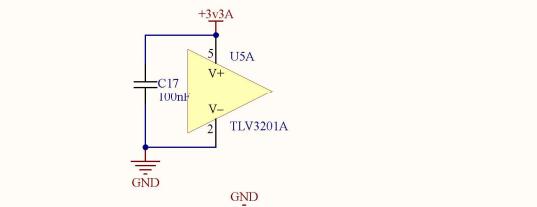
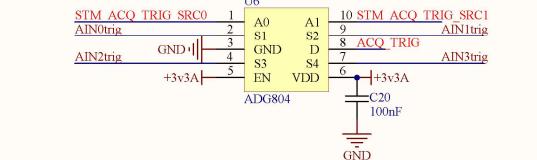
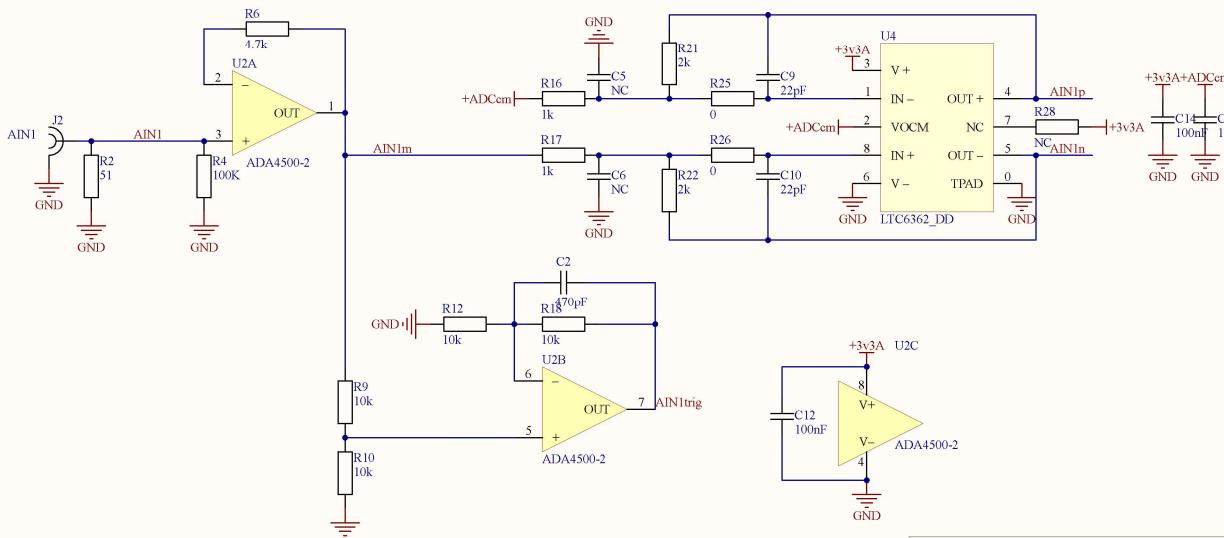


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ANALOG INPUT



BalEv.PriPcb

BalEv_AINa_v1_0.SchDoc

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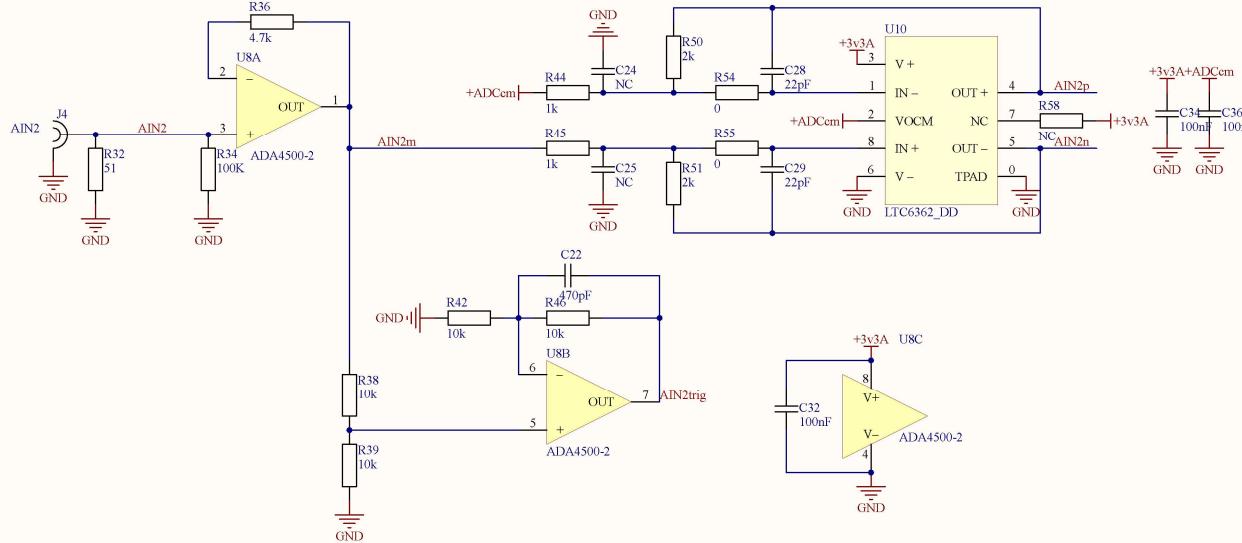
Date : 17.01.2022

Revision : 1.0a

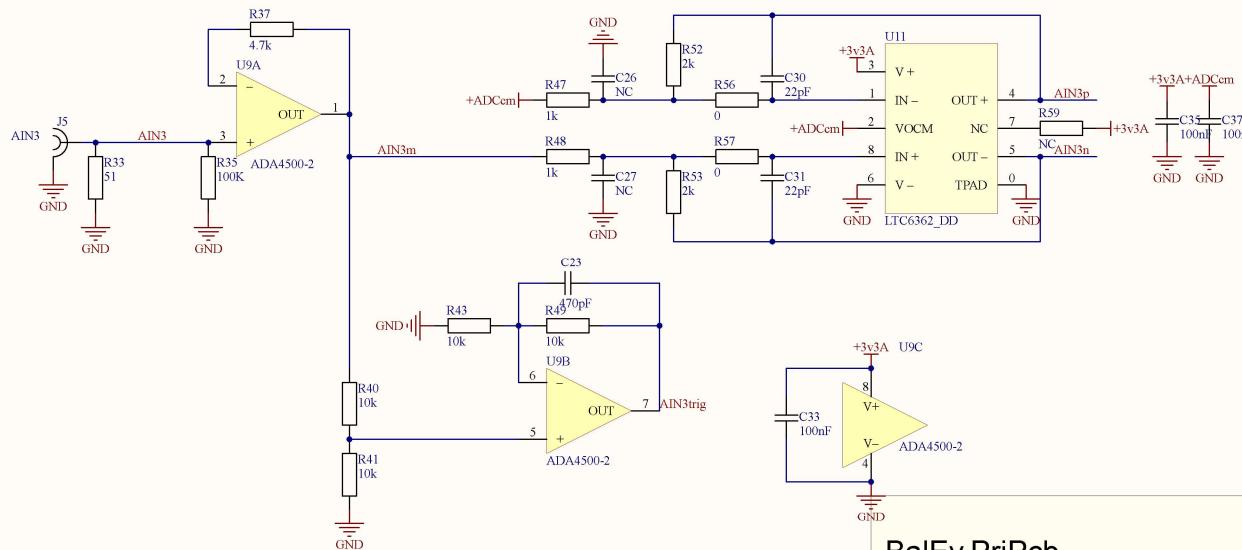
Sheet 6 of 9 Design by : anx/sap

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ANALOG INPUT 2



ANALOG INPUT 3



BalEv.PrjPcb

Hes-SO // VALAIS WALLIS

Date : 17.01.2022



BalEv_AInb_v1_0.SchDoc

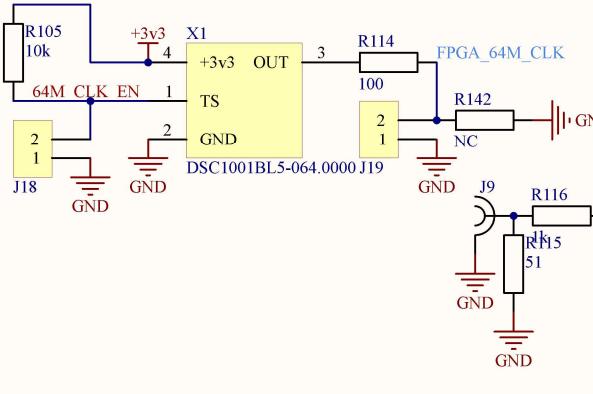
Revision : 1.0a

Sheet 7 of 9

Design by : anx/sap

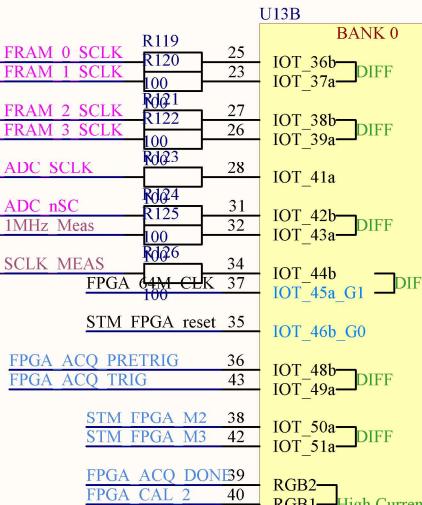
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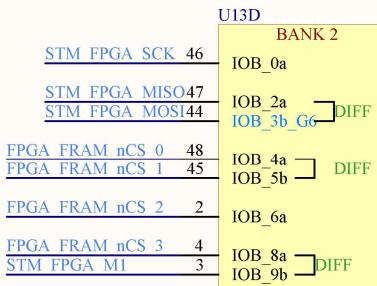
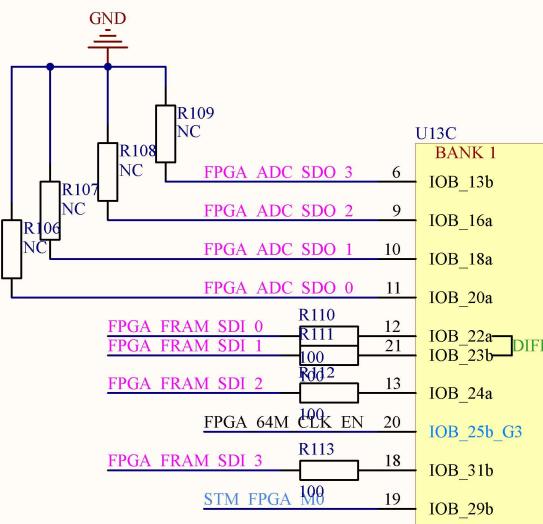
Signaux rose ->
connexions court.
Peut etre exchange
sur le meme BANK
Rose foncé peut etre
plus longues, garde
avec les autres rose.

Signaux noir fixes
sur leurs pins



Signaux bleu peut
etre exchange

Resistors on this page could be m0603



BalEv.PrjPcb

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WALLIS

Date : 17.01.2022



BalEv_FPTG_IO_v1_0.SchDoc

Revision : 1.0a Sheet 8 of 9 Design by : anx/sap

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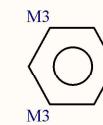
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BalEv.PrjPcb

BalEv_Mechanic_v1_0.SchDoc

Hes-SO // VALAIS WALLIS

Date : 17.01.2022

Revision : 1.0a

Sheet 9 of 9

Design by : anx/sap

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