Bachelor_test/mainCircuit_tb/struct

<company name>		Project:	hds
		<enter comments here>	
Title:	<enter diagram title here>		
Path:	Bachelor_test/mainCircuit_tb/struct		
Edited:	by christop.grobety on 13 juin 2023		

Package List

```
LIBRARY ieee;
  USE ieee.std_logic_1164.all;
  USE ieee.numeric_std.all;
LIBRARY gates;
USE gates.gates.all;
```

Declarations

Ports:

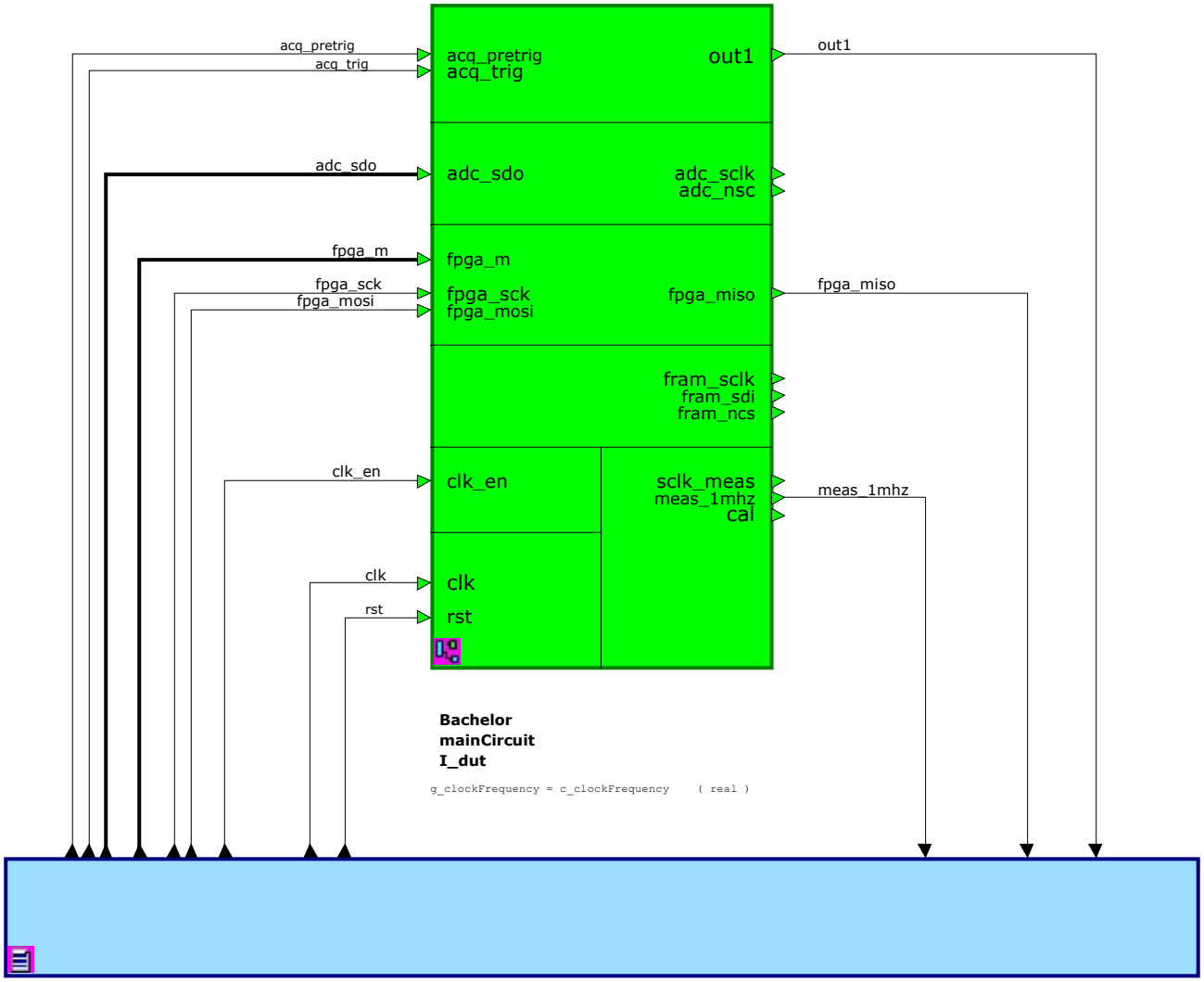
Pre User:

```
constant c_clockFrequency : real := 64.0E6;
```

Diagram Signals:

```
SIGNAL acq_pretrig : std_ulogic
SIGNAL acq_trig    : std_ulogic
SIGNAL adc_sdo     : std_ulogic_vector(3 downto 0)
SIGNAL clk         : std_uLogic
SIGNAL clk_en      : std_ulogic
SIGNAL fpga_m      : std_ulogic_vector(3 downto 0)
SIGNAL fpga_miso   : std_ulogic
SIGNAL fpga_mosi   : std_ulogic
SIGNAL fpga_sck    : std_ulogic
SIGNAL meas_1mhz   : std_ulogic
SIGNAL out1        : std_uLogic
SIGNAL rst         : std_ulogic
```

Post User:



Bachelor_test
mainCircuit_tester
I_tester

```
g_clockFrequency = c_clockFrequency    ( real )
```