

## Bachelor/mainCircuit/struct

## Package List

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.numeric_std.all;
```

```
LIBRARY gates;
USE gates.gates.all;
```

<company name>		Project: hds
Title: <enter diagram title here>	<enter comments here>	
Path: Bachelor/mainCircuit/struct		
Edited: by christop.grobety on 11 août 2023		

## Declarations

**Ports:**

```

acq_pretrig      : std_logic
acq_trig         : std_logic
adc_sdo         : std_logic_vector(3 downto 0)
clk              : std_logic
clk_en          : std_logic
fpga_m          : std_logic_vector(3 downto 0)
fpga_mosi       : std_logic
fpga_sck        : std_logic
fpga_sdo        : std_logic
adc_nsc         : std_logic
adc_sckl        : std_logic
cal              : std_logic_vector(2 downto 0)
fpga_miso       : std_logic
fpga_mcs        : std_logic_vector(3 downto 0)
fpga_mdi        : std_logic_vector(3 downto 0)
fpga_mdi        : std_logic_vector(3 downto 0)
fpga_mdi        : std_logic_vector(3 downto 0)
meas_lmhz       : std_logic
out1            : std_logic
sckl_meas       : std_logic

```

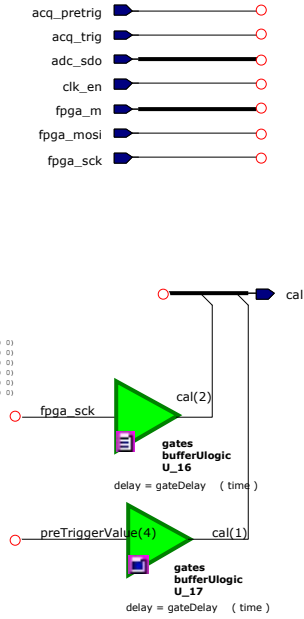
**Pre User:**

**Diagram Signals:**

```

SIGNAL AN_CLOCK      : std_logic
SIGNAL MISO_A        : std_logic
SIGNAL MISO_B        : std_logic
SIGNAL MISO_story     : std_logic
SIGNAL MISO_story     : unsigned(18 DOWNTO 0)
SIGNAL T              : std_logic
SIGNAL adc_nscAF      : std_logic
SIGNAL adc_nscAW      : std_logic
SIGNAL adc_selK1AF     : std_logic
SIGNAL adc_selK1AW     : std_logic
SIGNAL clock_inh2     : std_logic
SIGNAL clock_inh3     : std_logic
SIGNAL count_go       : std_logic
SIGNAL enable         : std_logic
SIGNAL fram_nscAF     : std_logic_vector(3 DOWNTO 0)
SIGNAL fram_nscAW     : std_logic_vector(3 DOWNTO 0)
SIGNAL fram_selK1AF   : std_logic_vector(3 DOWNTO 0)
SIGNAL fram_selK1AW   : std_logic_vector(3 DOWNTO 0)
SIGNAL fram_sdiAF     : std_logic_vector(3 DOWNTO 0)
SIGNAL fram_sdiAW     : std_logic_vector(3 DOWNTO 0)
SIGNAL preFriggerValue : unsigned(7 DOWNTO 0)

```



Example : 1 MHz toggler

