

# FPGA-EBS3 Electronic

Technical documentation

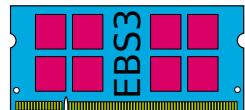
**Hes·so**  VALAIS  
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 School of Engineering

Author: [Amand Axel, Silvan Zahno](#)

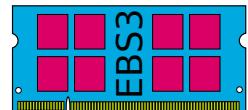
Date: March 20, 2023

Version: v1.0

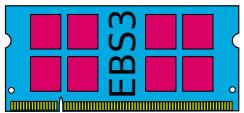


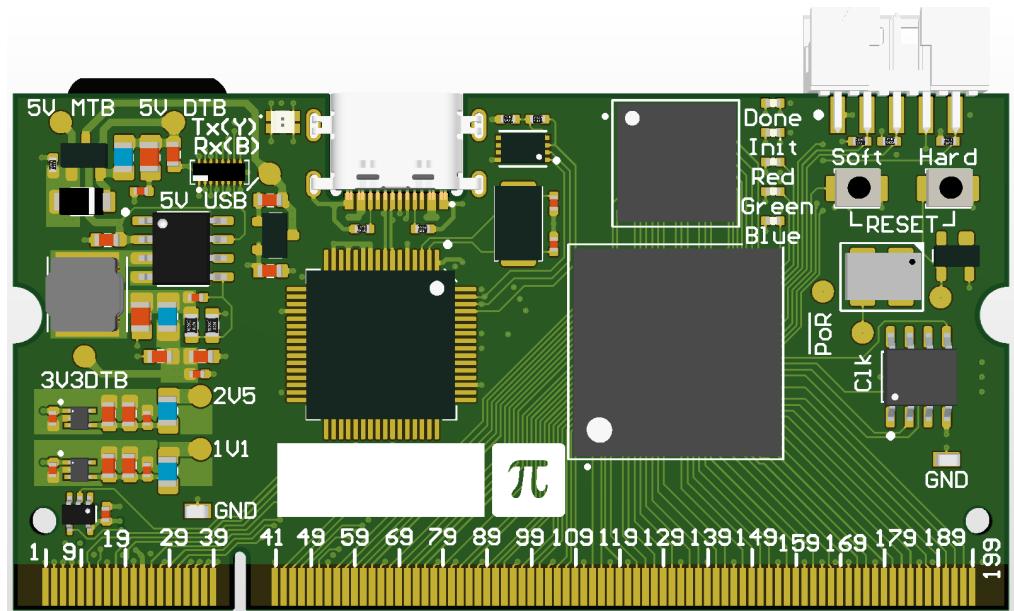
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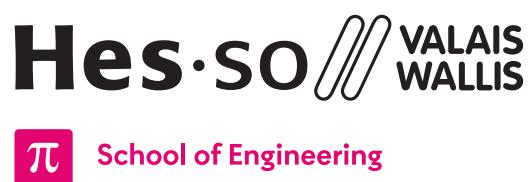


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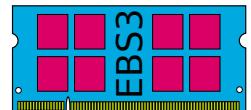




## Labs Daughterboard (LFE5U-25F)



Author: [Amand Axel](#), [Silvan Zahno](#)  
Date: March 20, 2023  
Version: v1.0



## 1 Overview

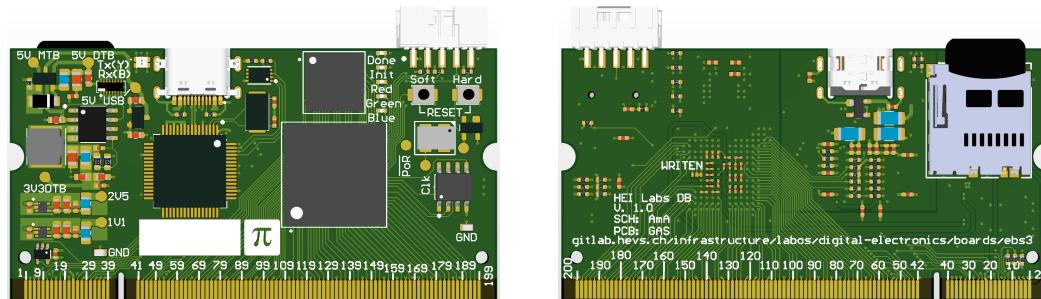


Figure 1: PCB board

The boards embeds the following functionalities:

- USB or MoBo +5V power input, creating internal voltages and a +3.3V / 3A user rail.
- USB connectivity, with one JTAG channel and one UART (virtual COM port) with TX/Rx LEDs.
- External JTAG programmer, automatic JTAG path extender.
- Power-on-reset chip, with an extra reset-button (either on the board or from a MoBo).
- 32 Mb flash for the user-program (allows for two partitions with all BRAMs filled), with a dedicated reset button.
- Three user LEDs + 1 power LED indicator.
- Micro-SD card slot with QSPI support and card detect.
- 256 Mb synchronous DRAM.

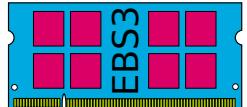
### Technical files

The schematic of the board is given under [I Schematic](#).

Rooting is available under [II Rooting](#) (*open the page with Inkscape for layers*).

The bill of material is given under [III BOM](#).

The pinout of the SODIMM-200 connector is available under [IV Pinout](#).



## 2 Specifications

### 2.1 Overview

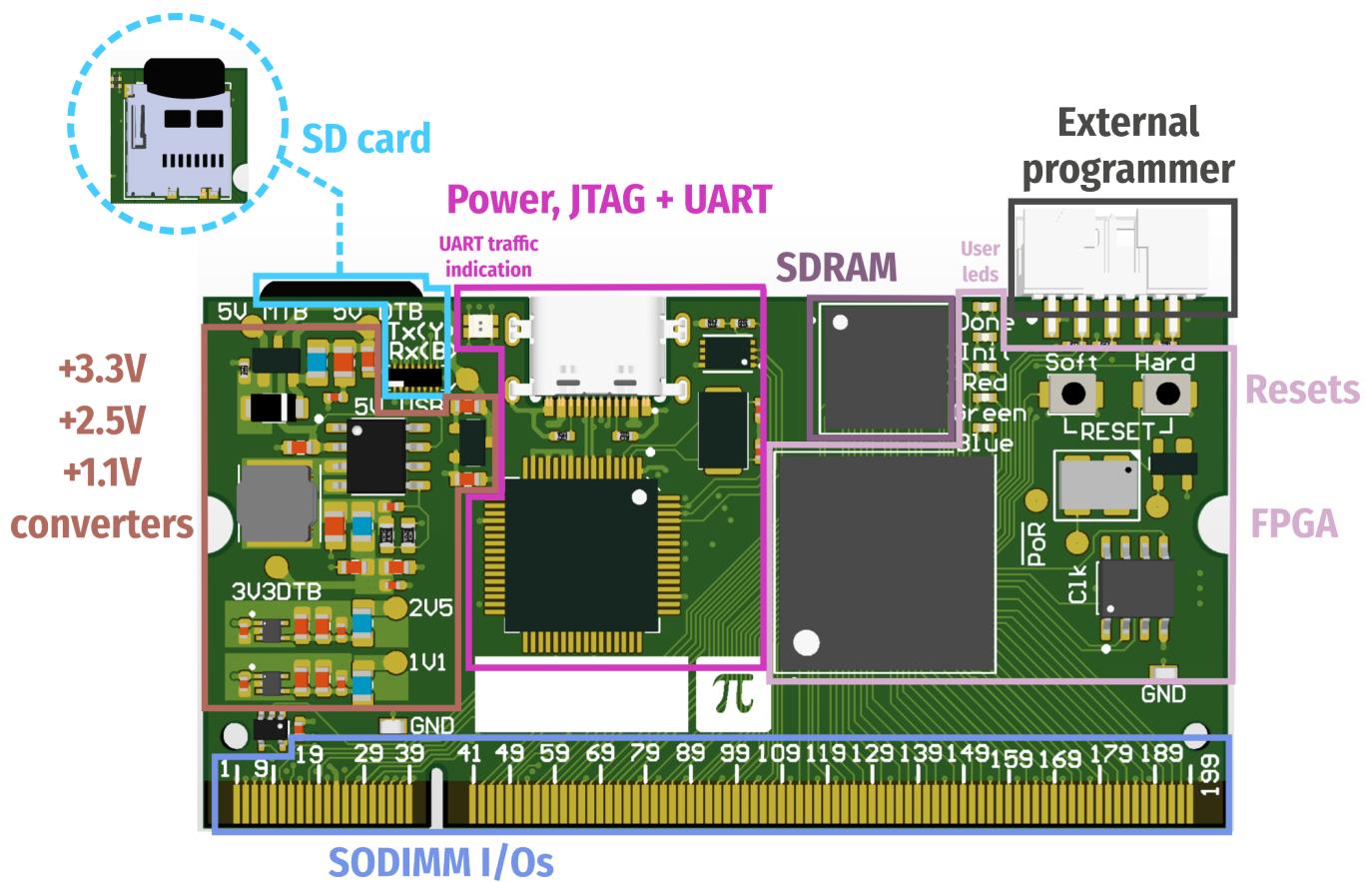
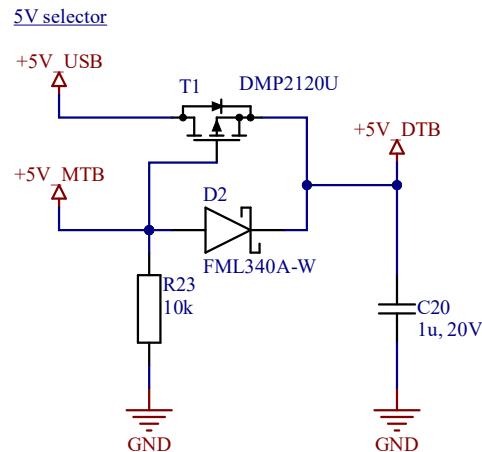


Figure 2: Card overview

### 2.2 Supply

The board can be powered either through USB ( $+5V$ , no PD) or from the motherboard (through dedicated SODIMM pins).

The MoBo rail is prioritized over the USB one:



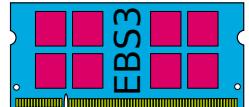
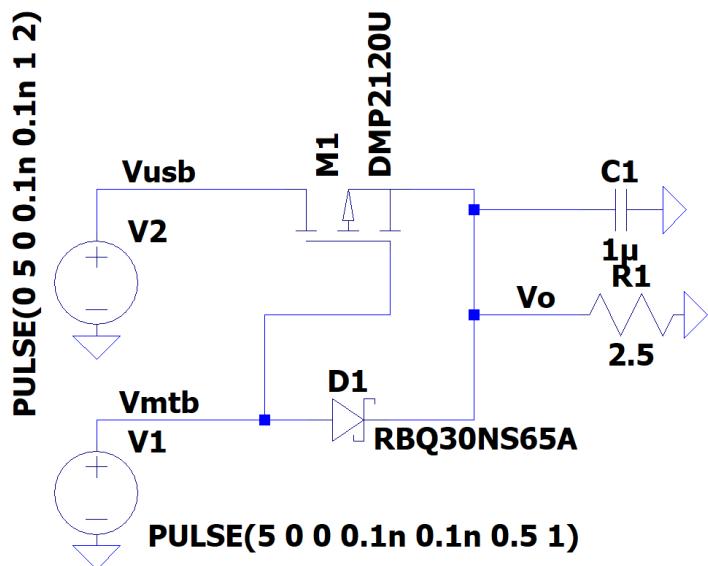


Figure 3: +5V selector - Circuit

Three cases:

- **+5V\_USB**, no **+5V\_MTB** : the transistors gate is low => it conducts fully, the diode blocks the path back to **+5V\_MTB**.
- no **+5V\_USB**, **+5V\_MTB** : the diode conducts with a slight loss, while the transistors diode blocks the path back to **+5V\_USB**.
- **+5V\_USB, +5V\_MTB** : the transistors gate is high => it blocks, and the internal diode blocks too (+5V on both sides). *Danger here would be for a too high voltage on the USB rail which would then take precedence over the MTB rail if  $U_{usb} > U_{mtb} - U_{d2} + U_{dt1}$* .



.tran 2s

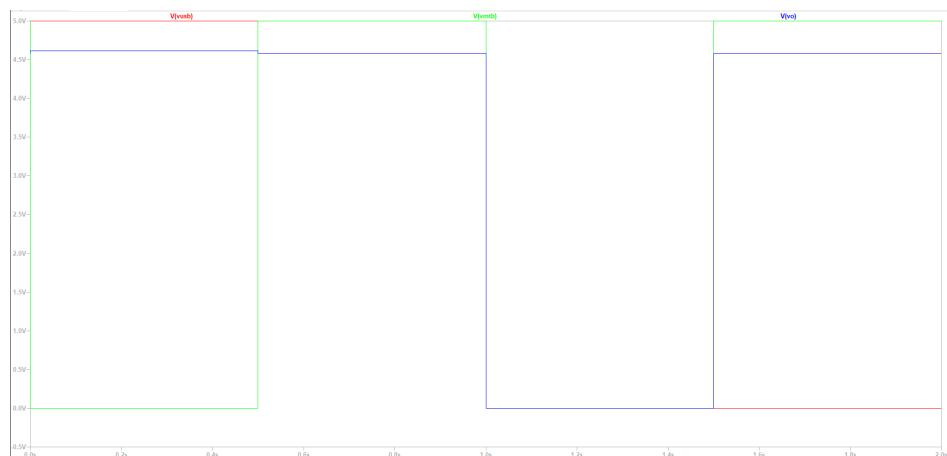


Figure 4: +5V selector - Simulation

Internally, a +1.1V, a +2.5V and a +3.3V rails are created with the PAM2320 buck converter first, then LDOs are used for internal voltages:

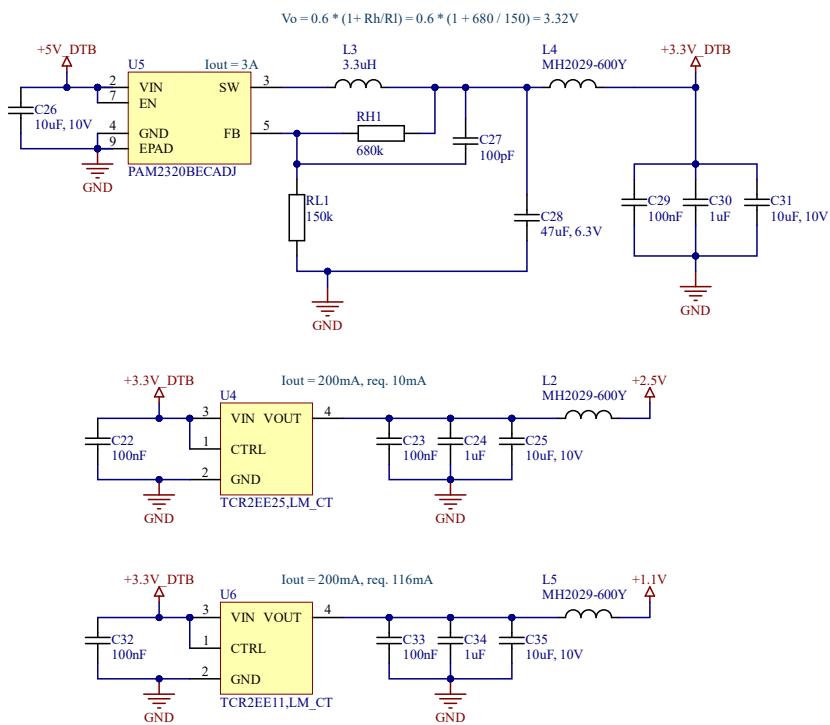
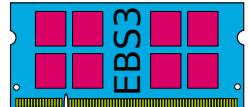


Figure 5: Voltage converters

The feedback pin of the buck converter sets the output voltage such as:

$$V_{out} = V_{ref} * \left(1 + \frac{R_h}{R_1}\right), \text{ with } V_{ref} = 0.6[V] \Rightarrow 0.6 * \left(1 + \frac{680k}{150k}\right) = 3.32[V]$$

Then, the TCR2EE25 (10 mA max. required out of the 200 possible) and the TCR2EE11 (116 mA max. required out of the 200 possible) create the two needed power rails for the [FPGA](#).

Only the +3.3V is available further through dedicated SODIMM pins.



The rail is limited to 3A. *No protection against overvoltage or overcurrent exists.*

### 2.3 USB

Thanks to a FTDI2232H chip, the USB connector (over the USB 2.0 norm) can also be used to:

- Flash the FPGA through JTAG (channel A)
- Communicate through UART (Virtual COM port on the PC side, channel B)

The chip is configured through FTDI's program named **FT\_Prog**, which saves it into the 93LC56B EEPROM:



<p><b>Device Tree</b></p> <ul style="list-style-type: none"> <li>Template: didlabs_ftprog.xml           <ul style="list-style-type: none"> <li>FT EEPROM               <ul style="list-style-type: none"> <li>Chip Details</li> <li>USB Device Descriptor</li> <li>USB Config Descriptor</li> <li>USB String Descriptors</li> </ul> </li> <li>Hardware Specific               <ul style="list-style-type: none"> <li>Port A                   <ul style="list-style-type: none"> <li>Hardware</li> <li>Driver</li> </ul> </li> <li>Port B                   <ul style="list-style-type: none"> <li>Hardware</li> <li>Driver</li> </ul> </li> <li>IO Pins</li> </ul> </li> </ul> </li> </ul>	<table border="1"> <thead> <tr> <th>Property</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>Manufacturer:</td> <td>HEI</td> </tr> <tr> <td>Product Description:</td> <td>LFE5U-25F</td> </tr> <tr> <td>Serial Number Enabled:</td> <td><input checked="" type="checkbox"/></td> </tr> <tr> <td>Auto Generate Serial No.:</td> <td><input type="checkbox"/></td> </tr> <tr> <td>Serial Number:</td> <td>018VFT3</td> </tr> <tr> <td>Serial Number Prefix:</td> <td>01</td> </tr> </tbody> </table>	Property	Value	Manufacturer:	HEI	Product Description:	LFE5U-25F	Serial Number Enabled:	<input checked="" type="checkbox"/>	Auto Generate Serial No.:	<input type="checkbox"/>	Serial Number:	018VFT3	Serial Number Prefix:	01	<p><b>Device Tree</b></p> <ul style="list-style-type: none"> <li>Template: ss1_ftprog.xml           <ul style="list-style-type: none"> <li>FT EEPROM               <ul style="list-style-type: none"> <li>Chip Details</li> <li>USB Device Descriptor</li> <li>USB Config Descriptor</li> <li>USB String Descriptors</li> </ul> </li> <li>Hardware Specific               <ul style="list-style-type: none"> <li>Port A                   <ul style="list-style-type: none"> <li>Hardware</li> <li>Driver</li> </ul> </li> <li>Port B                   <ul style="list-style-type: none"> <li>Hardware</li> <li>Driver</li> </ul> </li> <li>IO Pins</li> </ul> </li> </ul> </li> </ul>
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CPU FIFO	<input checked="" type="radio"/>															
OPTO Isolate	<input type="radio"/>															

Figure 6: FT\_Prog configuration

The UART (channel B) consists of Rx and Tx lines with CTS/RTS flow control (not mandatory). The bicolor LED LD1 indicates data transfer: blue means the board is receiving, while yellow is for data sent to host.



The chip needs to be configured first for the UART to work !

## 2.4 JTAG

The JTAG protocol is used to flash the [FPGA](#).

It is done either through the USB or with an external programmer on connector J2 with the following pinning (as seen from top):

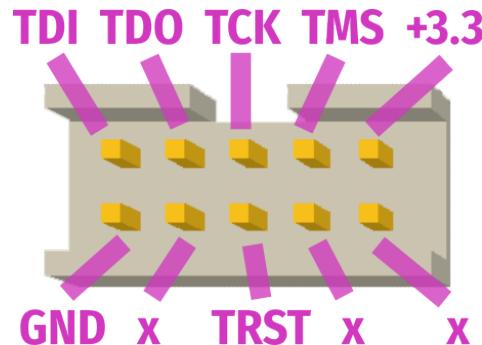
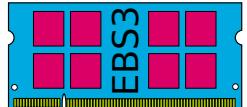


Figure 7: External programmer pinning

FPGA programming is explained under [Diamond \(Lattice\)](#).

The NC7SV126P5X buffer is used to extend the JTAG path through any other chip who may be present on the motherboard. By setting the signal **JTAG\_SHORT\_SEL** to '0', the output is no



more linked to TDI such that the motherboard is responsible to close the JTAG data path.

## 2.5 FPGA

The [FPGA](#) is a LFE5U-25F from Lattice.

It is clocked with a 100MHz oscillator. PLL blocks are internally available.

It is configured to read its program from a QSPI flash (the AT25SF321B) on wake-up (or when the soft-reset button is pressed). The flash is programmed by reaching the LFE5U through JTAG which then is in charge to forward the program to the flash.

The red [LED](#) LD3 indicates the [FPGA](#) is ready to be configured (i.e. power is good and program not loaded yet). The green [LED](#) LD2 indicates the startup sequence is running (i.e. loading program from given source).



By default, once the program is loaded, both [LEDs](#) shut off. The behavior can be modified by specific settings of the program (see [Diamond \(Lattice\)](#)).

**Reset** The APX811-31U is used as power-on-reset, holding the reset signal low while either the power is bad or the user presses the button labeled **Hard Reset**. Also, one can reset the FPGA by setting the dedicated **nRESET\_IN** signal low from the motherboard.

**Reload program** The button labeled **Soft Reset** is used to force the [FPGA](#) to reload its configuration from the flash memory.

## 2.6 DRAM

The IS42S16160J is a 256 Mb static DRAM chip which allows to store and read temporary informations from the [FPGA](#) quickly.

It works either in a 32M \* 8 bits or 16M \* 16 bits configuration with a parallel access to both address and data.

## 2.7 Micro-SD card

The MEM2051 is a micro-SD card slot of the push-push type (i.e. push the card in → it clicks and retains it, push again → the card is freed) to offer user flash memory.

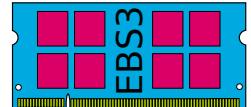
It contains a dedicated detection pin for when the card is inserted ('0' when the card is inserted) which can be read with the **nSD\_DETECT** signal name.

QSPI lines are rooted to the card, allowing for fast transfers.

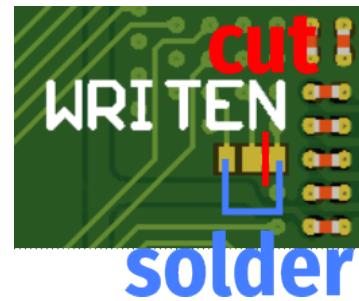
## 2.8 WRITEN

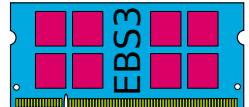
A jumper on the back of the board labeled **WRITEN** allows to modify the behavior of the [FPGA](#) towards its flash memory on start. If soldered to GND, it issues a 0xFF write on MOSI (forcing a reset of QSPI devices). Pulling it to VCC avoid sending this byte.

It is soldered to GND by default.



To modify the jumper, due to an incorrect wiring, do NOT cut the current trace and solder the middle tab with the left one. It must be soldered as:





### 3 SW Configuration

The board is used with [Diamond \(Lattice\)](#).

#### 3.1 Board configuration

The default configuration (constraints file) for the board is available under [V Constraints file](#).

- Pins voltages are set with:

```
IOBUF ALLPORTS IO_TYPE=LVC MOS33 ; , setting all ports to +3.3V  
Two pins in the same bank cannot have different voltages.
```

- The system is configured with:

```
SYS CONFIG MCCLK_FREQ=62 MASTER_SPI_PORT=ENABLE DONE_OD=ON  
CONFIG_MODE=SPI_QUAD INBUF=OFF CONFIG_IOVOLTAGE=3.3 ;
```

*The various options are given in the constraints file. Here :*

- The flash access clock to load the program is set to its maximum, i.e. 62 MHz*
- Mode is MASTER\_SPI\_PORT, with CONFIG\_MODE specifying the flash can be read in quad-SPI mode*
- The DONE pin is open-drain*
- Unused input buffers are deactivated*
- Pins from the sysCONFIG bank are set to 3.3V*

- The clock is specified by its frequency (for timing analysis) with:

```
FREQUENCY PORT "CLK" 100.000000 MHz ;
```

The pin is then specified with:

```
LOCATE COMP "CLK" SITE "K16" ;
```

- The reset signal pin is set with:

```
LOCATE COMP "nRST" SITE "E13" ;
```

As is, this pin is considered as a standard I/O. To help Diamond detecting it as the GSR (Global Set-Reset) net for flip-flops, add the line:

```
GSR_NET net "resetSynch_n" ;
```

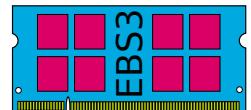


In the VHDL file, the reset signal must be named `resetSynch_n`. Otherwise, modify the previous line accordingly.

- I/Os directions are not specified. The pin is first linked to the net with:

```
LOCATE COMP "SD_DETECT" SITE "G12" ; special functionalities can be set:  
IOBUF PORT "SD_DETECT" PULLMODE=UP ;
```

- for inputs, a pull resistor can be set with `PULLMODE=UP|DOWN`
- for outputs, the slewrate can be set with `SLEWRATE=SLOW|FAST`, the driving capability with `DRIVE=4|8|12|16`
- Other settings exist. In Diamond, open the "Spreadsheet View" for an interactive edit of the I/O pins.*



### 3.2 Test project

The tester is planned for 100 MHz clocks.

A HDL Designer test project is available with the following:

- Most LEDs and I/Os will light at three various frequencies.
- The UART and flow controls are redirected to the motherboard.
- The DRAM and SD-card are disabled (not tested yet).
- The blue LED lights up when a SD-card is detected.

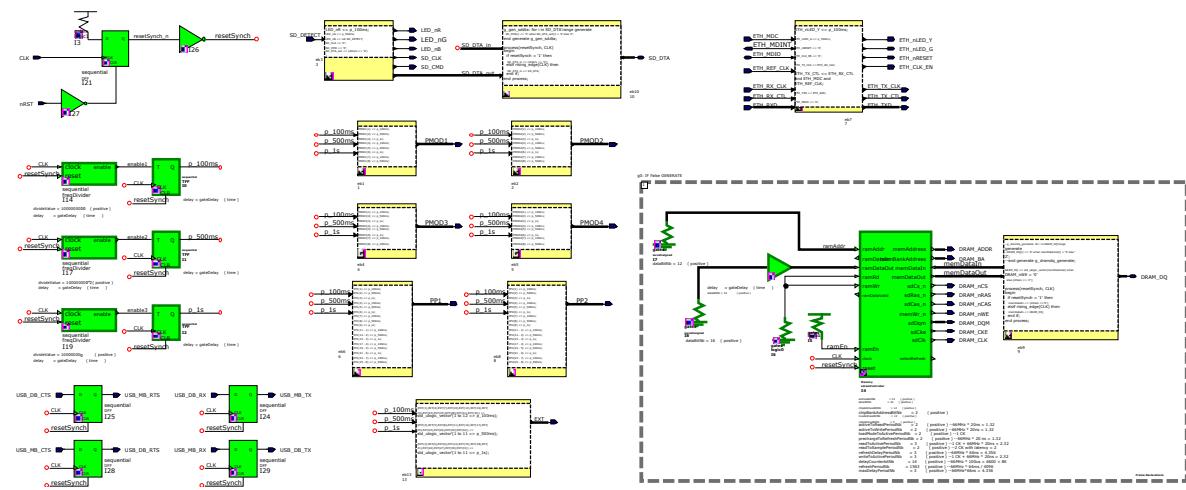
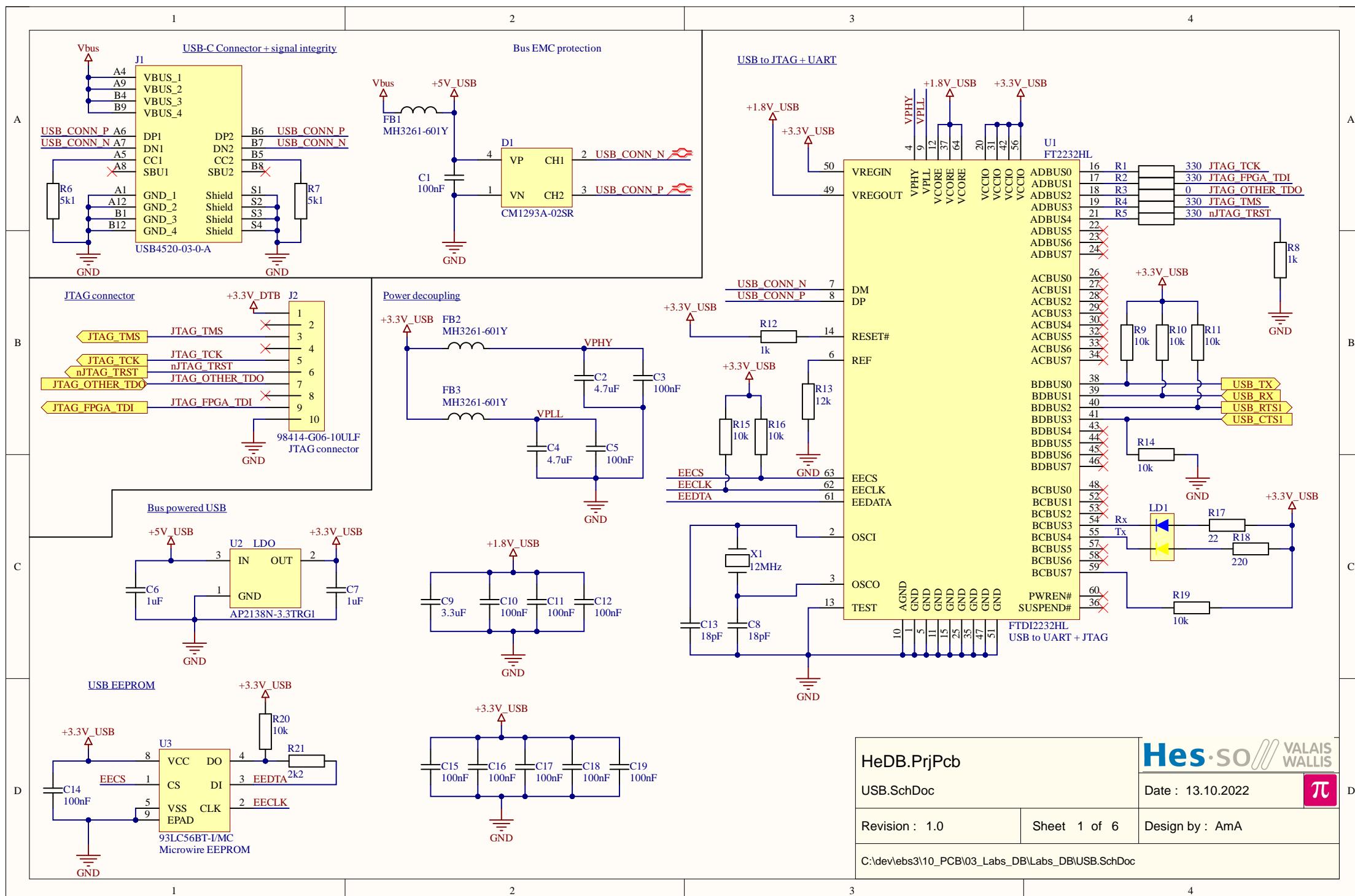


Figure 8: HDL Designer test program

# I Schematic

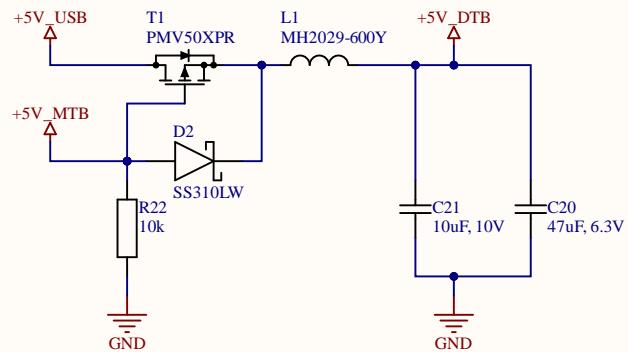
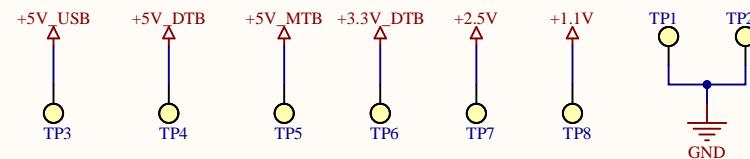
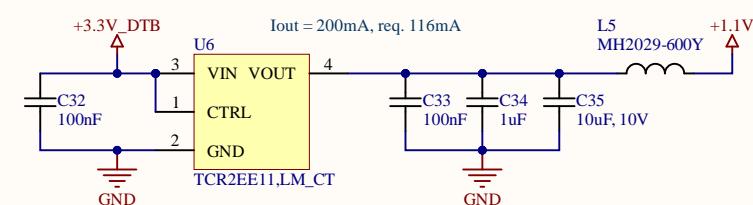
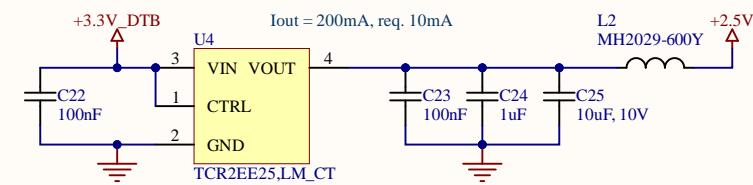
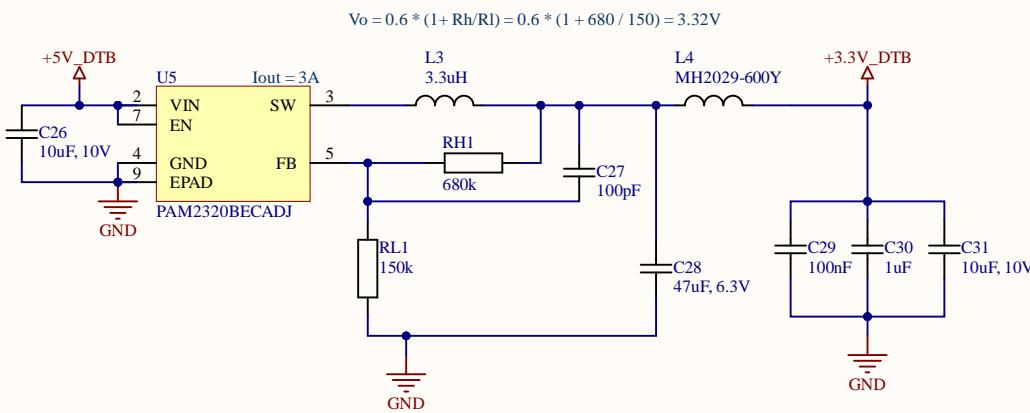


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5V selectorTest pointsBuck converters

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Power.SchDoc

Date : 13.10.2022



Revision : 1.0

Sheet 2 of 6

Design by : AmA

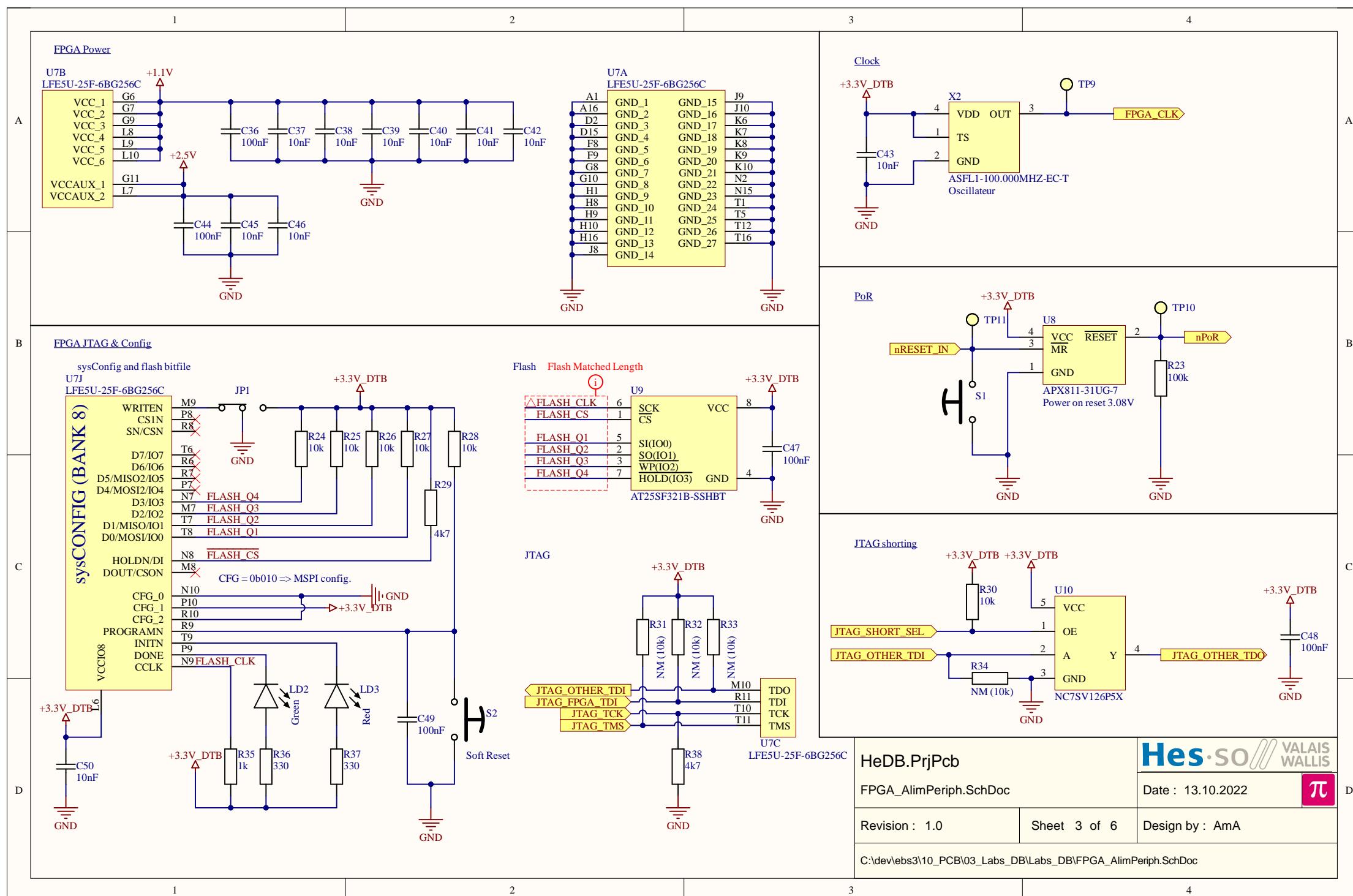
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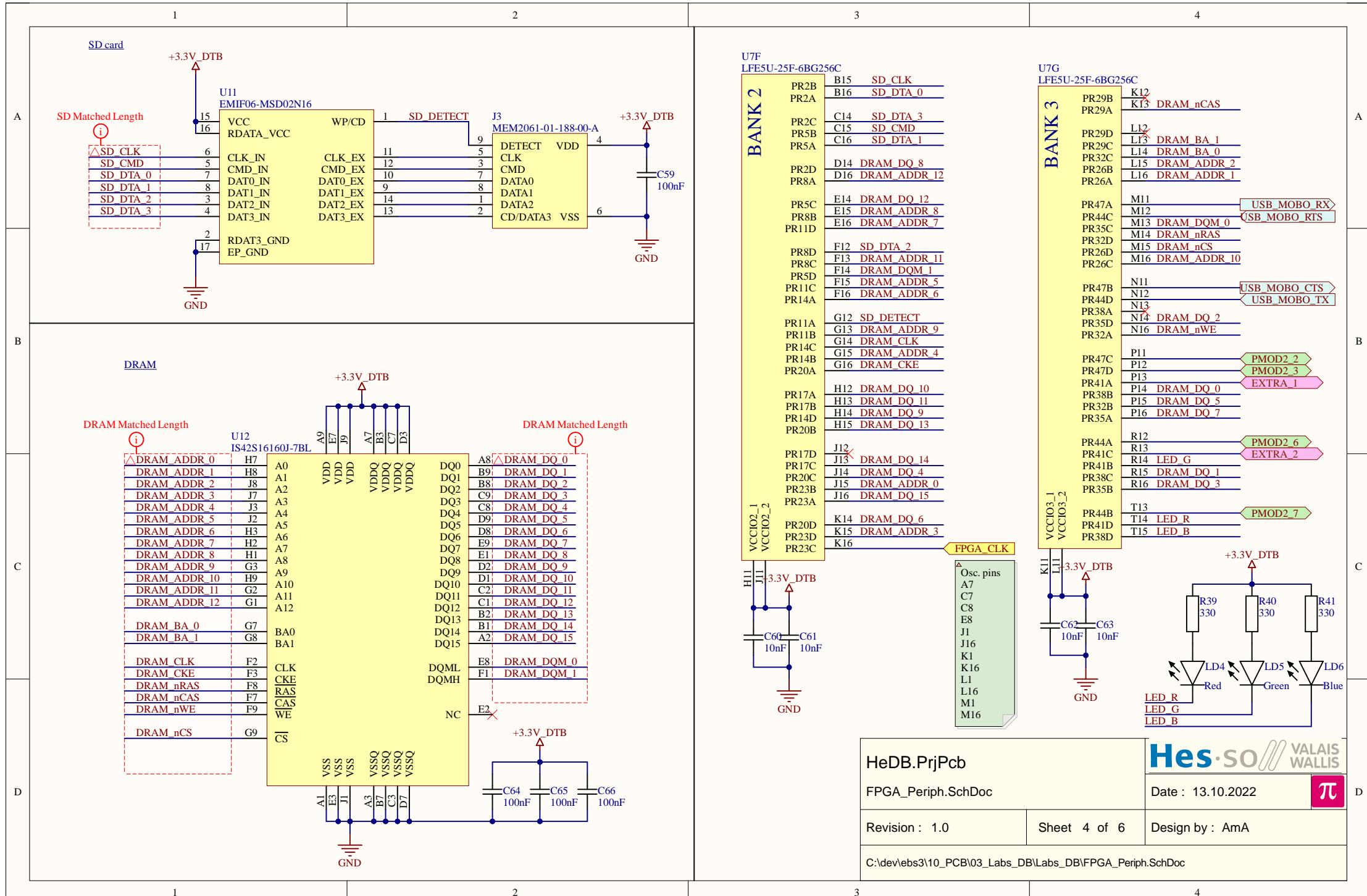
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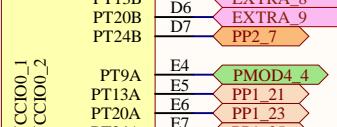
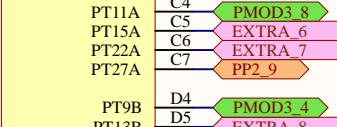
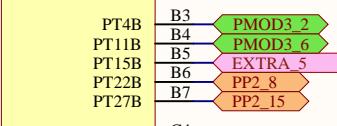
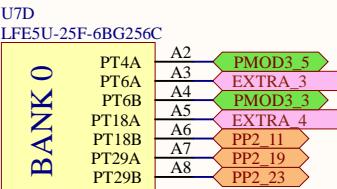
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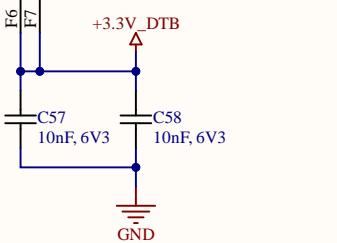




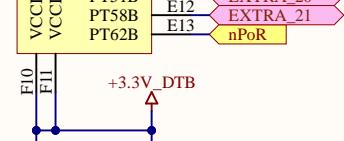
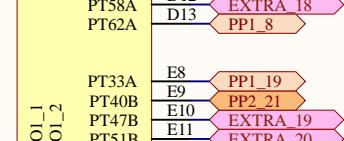
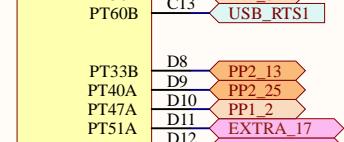
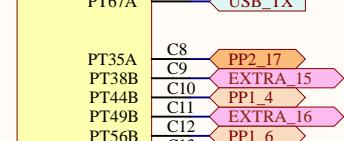
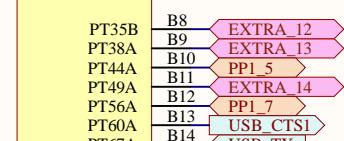
## FPGA IOs

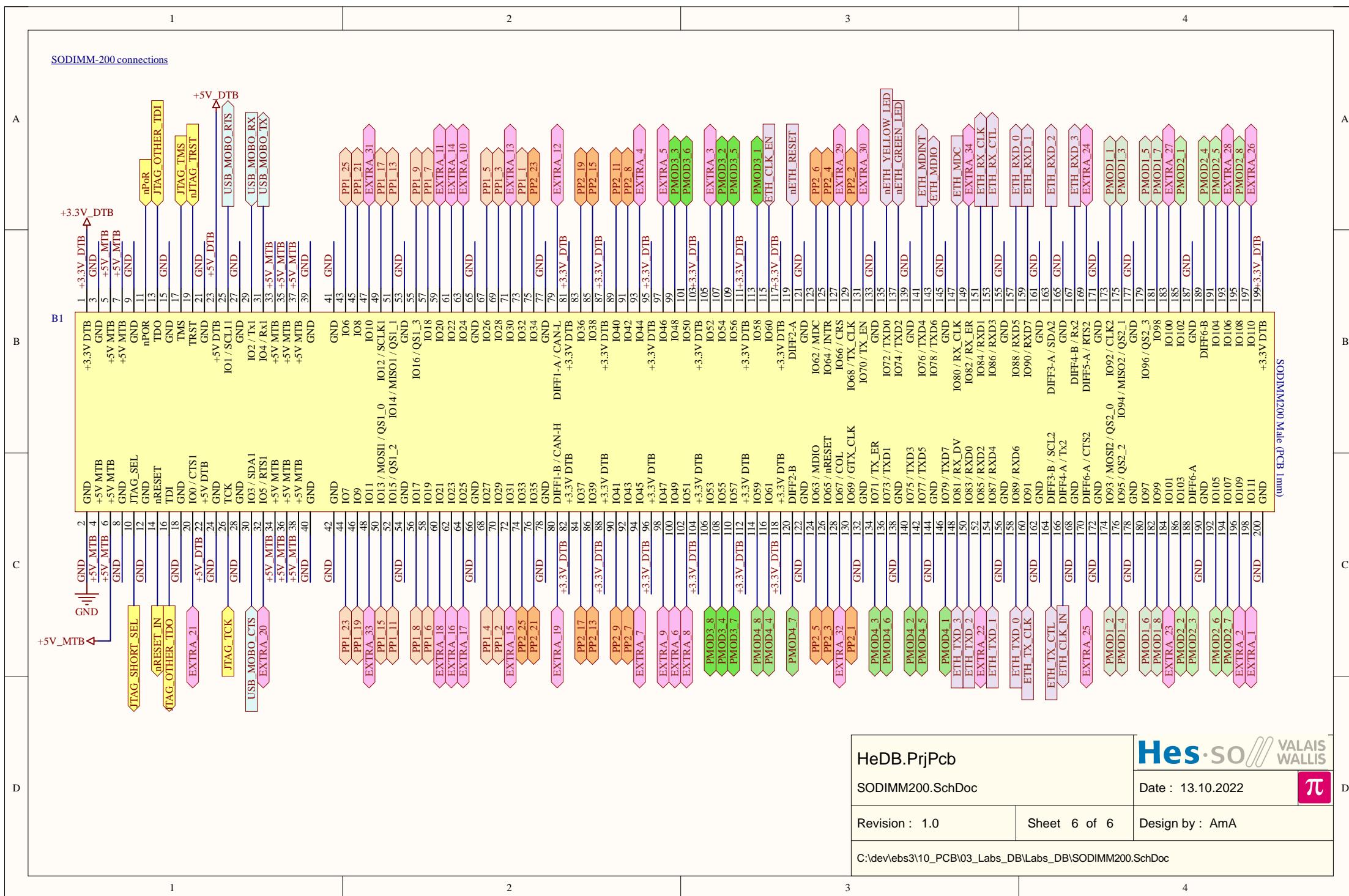


VCCIO0\_1 VCCIO0\_2



**U7E LFE5U-25F-6BG256C**





HeDB.PrjPcb

SODIMM200.SchDoc

**Hes-SO** VALAIS WALLIS

Date : 13.10.2022



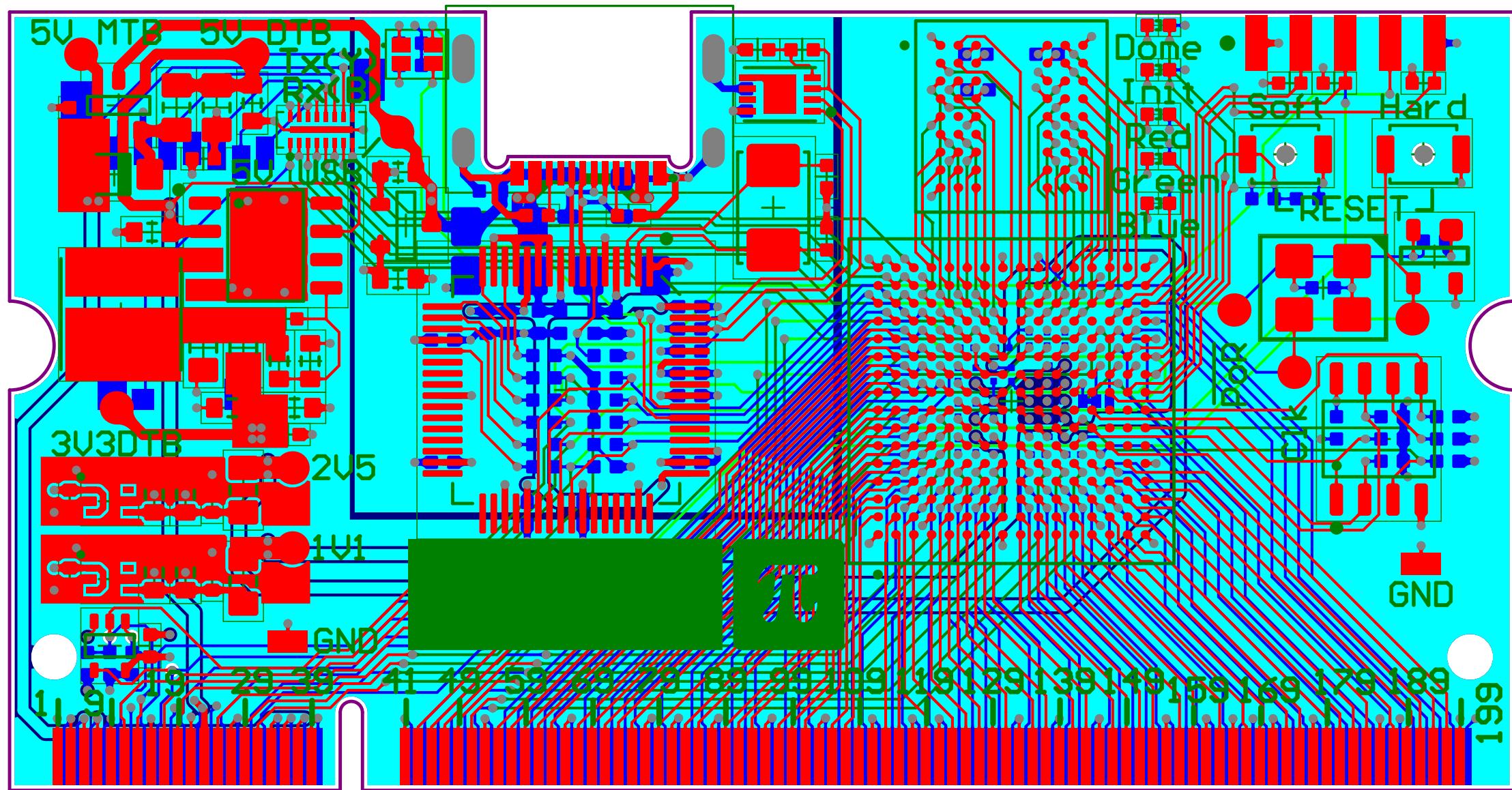
Revision : 1.0

Sheet 6 of 6

Design by : AmA

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## **II Rooting**



**III BOM**

Name	Description	Designator	Quantity	Footprint
PCB Board (1mm thick)	DDR1 & DDR2 Board 0.6mm pitch 200 Positions	B1	1	1DDR2 SODIMM Socket 0.6mm pitch 200 Positions 2.5V
100nF	Capacitor	C1, C3, C5, C10, C11, C12, C14, C15, C16, C17, C18, C19, C22, C23, C29, C32, C33, C47, C48, C49, C59, C64, C65, C66	24	CAPACITOR 1005 REFLOW
4.7uF	Capacitor	C2, C4	2	CAPACITOR 1005 REFLOW
1uF	Capacitor	C6, C7, C24, C30, C34	5	CAPACITOR 1608 REFLOW
18pF	Capacitor	C8, C13	2	CAPACITOR 1005 REFLOW
3.3uF	Capacitor	C9	1	CAPACITOR 1005 REFLOW
47uF, 6.3V	Capacitor	C20, C28	2	CAPACITOR 2012 REFLOW
10uF, 10V	Capacitor	C21, C25, C26, C31, C35	5	CAPACITOR 1608 REFLOW
100pF	Capacitor	C27	1	CAPACITOR 1005 REFLOW
100nF	Capacitor	C36, C44	2	CAPACITOR 0603 REFLOW
10nF	Capacitor	C37, C38, C39, C40, C41, C42, C45, C46, C50, C60, C61, C62, C63	13	CAPACITOR 0603 REFLOW
10nF	Capacitor	C43	1	CAPACITOR 1005 REFLOW
10nF, 6V3	Capacitor	C51, C52, C53, C54, C55, C56, C57, C58	8	CAPACITOR 0603 REFLOW
CM1293A-02SR	ESD Protection Array 2 Channels	D1	1	SOT143 P1.9 C1.4X3.0 H1.1
SS310LW	Diode Schottky generic 2 Leads	D2	1	DIODE SOD123-FL REFLOW
MH3261-601Y	Inductor	FB1, FB2, FB3	3	INDUCTOR 3216 REFLOW
USB4520-03-0-A	Connector	J1	1	USB-C-SMD GCT USB4520030A
98414-G06-10ULF	FlatCable 2x5	J2	1	FlatCable 2x5 2MM Edge Mount FCI 98414-G06-10ULF
MEM2061-01-188-00-A	SD Card Micro	J3	1	SD MICRO GCT MEM2051-00-195-00-A
MH2029-600Y	Inductor	L1, L2, L4, L5	4	INDUCTOR 2012 REFLOW
LOH5BPN3R3NTOL	Inductor	L3	1	Murata LO5BPN
LTST-C195TBKSKT-5A	Standard-LEDs - SMD SMD LED Bi-Color Blue 45/Yellow 70mcd	LD1	1	LED LiteOn LTST-C195 series
B2841NG-05D000514U1930	LED generic	LD2, LD5	2	LED 1005 REFLOW
B2841URO-20C00114U1930	LED generic	LD3, LD4	2	LED 1005 REFLOW
B2841NB-20C001414U1930	LED generic	LD6	1	LED 1005 REFLOW
330	Resistor	R1, R2, R4, R5, R36, R37, R39, R40, R41	9	RESISTOR 1005 REFLOW
0	Resistor	R3	1	RESISTOR 1005 REFLOW
5k1	Resistor	R6, R7	2	RESISTOR 1005 REFLOW
1k	Resistor	R8, R12, R35	3	RESISTOR 1005 REFLOW
10k	Resistor	R9, R10, R11, R14, R15, R16, R19, R20, R22, R24, R25, R26, R27, R28, R30	15	RESISTOR 1005 REFLOW
12k	Resistor	R13	1	RESISTOR 1005 REFLOW
22	Resistor	R17	1	RESISTOR 1005 REFLOW
220	Resistor	R18	1	RESISTOR 1005 REFLOW
2k2	Resistor	R21	1	RESISTOR 1005 REFLOW
100k	Resistor	R23	1	RESISTOR 1005 REFLOW
4k7	Resistor	R29, R38	2	RESISTOR 1005 REFLOW
NM (10k)	Resistor	R31, R32, R33, R34	4	RESISTOR 1005 REFLOW
680k	Resistor	RH1	1	RESISTOR 1608 REFLOW
150k	Resistor	RL1	1	RESISTOR 1608 REFLOW
B3U-1000PM-B	Push Button, 2 pins	S1, S2	2	Push Button C2.5X3.0 OMRON B3U-1000P(M)-B
PMV50XPR	Generic MOS-P	T1	1	SOT23 P0.95 C1.6x3.0 H1.3
S2761-46R	Test Point	TP1, TP2	2	Test Point HARWIN S2761-46R
FT2232HL	Dual High Speed USB to Multipurpose UART/FIFO IC	U1	1	LQFP64 P0.5 C10.0x10.0 H1.6
AP2138N-3.3TRG1	Generic Positive Voltage Regulator	U2	1	SOT23 P0.95 C1.6x3.0 H1.3
93LC56BT-I/MC	2K bit low voltage serial EEPROMs, Without ORG Pin	U3	1	DFN8 P0.5 T1.45X1.75 C2.0X3.0 H0.9
TCR2EE25_LM_CT	200 mA CMOS Low Dropout Regulator with Fast Load Transient Response	U4	1	SOT553 P0.5 C1.6x1.2 H0.55
PAM2320BECAJD	3A step-down DC-DC converter	U5	1	S08 P1.27 T2.4x2.4 C4.0X5.0 H1.4
TCR2EE11_LM_CT	200 mA CMOS Low Dropout Regulator with Fast Load Transient Response	U6	1	SOT553 P0.5 C1.6x1.2 H0.55
LFE5U-25F-6BG256C	ECP5 Field Programmable Gate Array	U7	1	BGA256 P0.8 C14.0X14.0 H1.7
APX811-31UG-7	4-Pin Microprocessor Supervisor With Manual Reset	U8	1	SOT143 P1.9 C1.4X3.0 H1.1
AT25SF321B-SHGBT	32-Mbit SPI Serial Flash Memory	U9	1	S08 P1.27 C4.0X5.0 H1.75
NC7SV126P5X	single 3-State buffer	U10	1	SC70-5 P0.65 C1.4x2.2 H1.0
EMIF06-MSD02N16	6-line IPAD EMI filter and ESD protection in micro QFN package	U11	1	DIODE EMIF06MSD02N16
IS42S16160J-7BL	256Mb Synchronous DRAM	U12	1	BGA54 P0.8 C8.0x8.0 H1.2
445123C12M00000	Crystal C5.0x3.2 CTS 445	X1	1	CRYSTAL C5.0x3.2 CTS 445
ASFL1-100.000MHz-EC-T	Oscillator C5.0x3.2 Abraneon ASFL1	X2	1	Oscillator C5.0x3.2 Abraneon ASFL1

# **IV Pinout**

Connector name on the schematic : B1

Product Name LFE5U-25F	Standard	Pin Numbers	Standard	Product Name LFE5U-25F
Pin Type	Pin Type	Top	Bottom	Pin Type
+3.3V	+3.3V	1	2	GND
GND	GND	3	4	+5V MTB
+5V MTB	+5V MTB	5	6	+5V MTB
+5V MTB	+5V MTB	7	8	GND
GND	GND	9	10	JTAG_SEL
POR/	POR/	11	12	GND
TDO	TDO	13	14	RESET/
GND	GND	15	16	TDI
TMS	TMS	17	18	GND
TRST	TRST	19	20	IO0 / CTS1
GND	GND	21	22	+5V DTB
+5V DTB	+5V DTB	23	24	GND
RTS1	IO1 / SCL1	25	26	TCK
GND	GND	27	28	GND
RX1	IO2 / Tx1	29	30	IO3 / SDA1
TX1	IO4 / RX1	31	32	CTS1
+5V MTB	+5V MTB	33	34	+5V MTB
+5V MTB	+5V MTB	35	36	+5V MTB
+5V MTB	+5V MTB	37	38	+5V MTB
GND	GND	39	40	GND
GND	GND	41	42	GND
PP1_25	IO6	43	44	IO7
PP1_21	IO8	45	46	PP1_23
EXTRA_31	IO10	47	48	IO9
PP1_17	IO12 / SCLK1	49	50	IO10
PP1_13	IO14 / MISO1 / QS1_1	51	52	IO11
GND	GND	53	54	GND
PP1_9	IO16 / QS1_3	55	56	IO17
PP1_7	IO18	57	58	IO19
EXTRA_11	IO20	59	60	IO21
EXTRA_14	IO22	61	62	IO23
EXTRA_10	IO24	63	64	IO25
GND	GND	65	66	GND
PP1_5	IO26	67	68	IO27
PP1_3	IO28	69	70	IO29
EXTRA_13	IO30	71	72	IO31
PP1_1	IO32	73	74	IO33
PP2_23	IO34	75	76	IO35
GND	GND	77	78	GND
EXTRA_12	DIFF1-A / CANL	79	80	DIFF1-B / CANH
+3.3V	+3.3V	81	82	+3.3V
PP2_19	IO36	83	84	IO37
PP2_15	IO38	85	86	IO39
+3.3V	+3.3V	87	88	+3.3V
PP2_11	IO40	89	90	IO41
PP2_8	IO42	91	92	IO43
PP2_EXTRA_4	IO44	93	94	IO45
+3.3V	+3.3V	95	96	+3.3V
EXTRA_5	IO46	97	98	IO47
PMOD3_3	IO48	99	100	IO49
PMOD3_6	IO50	101	102	IO51
+3.3V	+3.3V	103	104	+3.3V
EXTRA_3	IO52	105	106	IO53
PMOD3_2	IO54	107	108	IO55
PMOD3_5	IO56	109	110	IO57
+3.3V	+3.3V	111	112	+3.3V
PMOD3_1	IO58	113	114	IO59
ETH_CLK_EN	IO60	115	116	IO61
+3.3V	+3.3V	117	118	+3.3V
nETH_RESET	DIFF2-A	119	120	DIFF2-B
GND	GND	121	122	GND
PP2_6	IO62 / MDC	123	124	IO63 / MDIO
PP2_4	IO64 / INTR	125	126	IO65 / nRESET
EXTRA_29	IO66 / CRS	127	128	IO67 / COL
PP2_2	IO68 / TX_CLK	129	130	IO69 / GTX_CLK
EXTRA_30	IO70 / TX_EN	131	132	GND
GND	GND	133	134	IO71 / TX_ER
nETH_YELLOW_LED	IO72 / TXD0	135	136	IO73 / TxD1
nETH_GREEN_LED	IO74 / TXD2	137	138	GND
GND	GND	139	140	IO75 / TXD3
ETH_MDINT	IO76 / TXD4	141	142	IO77 / TXD5
ETH_MDIO	IO78 / TXD6	143	144	GND
GND	GND	145	146	IO79 / TXD7
ETH_MDC	IO80 / RX_CLK	147	148	IO81 / RX_DV
EXTRA_34	IO82 / RX_ER	149	150	IO83 / RXD0
ETH_RX_CLK	IO84 / RXD1	151	152	IO85 / RXD2
ETH_RX_CTL	IO86 / RXD3	153	154	IO87 / RXD4
GND	GND	155	156	GND
ETH_RXD0	IO88 / RXD5	157	158	IO89 / RXD6
ETH_RXD1	IO90 / RXD7	159	160	IO91
GND	GND	161	162	GND
ETH_RXD2	DIFF3-A / SDA2	163	164	DIFF3-B / SCL2
GND	GND	165	166	DIFF4-A / TX2
ETH_RXD3	DIFF4-B / Rx2	167	168	GND
EXTRA_24	DIFF5-A / RTS2	169	170	DIFF5-B / CTS2
GND	GND	171	172	GND
PMOD1_1	IO92 / SCLK2	173	174	IO93 / MOSI2 / QS2_0
PMOD1_3	IO94 / MISO2 / QS2_1	175	176	IO95 / QS2_2
GND	GND	177	178	GND
PMOD1_5	IO96 / QS2_3	179	180	IO97
PMOD1_7	IO98	181	182	IO99
EXTRA_27	IO100	183	184	IO101
PMOD2_1	IO102	185	186	IO103
GND	GND	187	188	DIFF6-A
PMOD2_4	DIFF6-B	189	190	GND
PMOD2_5	IO104	191	192	IO105
EXTRA_28	IO106	193	194	IO107
PMOD2_8	IO108	195	196	IO109
EXTRA_26	IO110	197	198	IO111
+3.3V	+3.3V	199	200	GND

FREE PINS (no NC) : 0  
FREE PINS (NC comprised) : 0

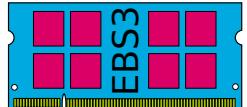
Signals names as seen from the daughterboard if not specified otherwise (e.g. Tx is the output of FPGA's UART block)

GND	Common ground
+3.3V	Daughterboard 3.3V output (max 1.5 [A])
+5V DTB	Daughterboard 5V output (LOW CURRENT CONSUMPTION IF RUNNING ON USB !)
+5V MTB	Motherboard 5V output
Txx	JTAG signals /JTAG_SEL : 1 = no extra chip, 0 = extra JTAG line used)
RESET/	Daughterboard reset input (active low)
POR/	Daughterboard PowerOnReset signal output (active low)
DIFFx-A/B	Differential pair I/O preferred pins (can be used as standard I/O)
IOx	Input / output pin
TX / Rx	3.3V USART signals, any I/O for complementary (CTR, DTS ...)
SCL / SDA	3.3V I2C signals
SCLK / MOSI / MISO	3.3V SPI signals, any I/O as slave select
QS	SPI dual/quad interface
CANL / CANH	3.3V CAN signals (REQUIRES A TRANSCEIVER ON THE MOTHERBOARD !)
TXD, RXD ...	Gigabit ethernet signals ((G)MII, MDC/MDIO, interrupt)

Jedec 4.20.11-1 link :

- Power pins, except pin 200 (added as GND), 199 and 1 as standard +3.3V
- 69, 83, 120 and 163 (test pins) as standard I/Os
- 30, 32, 164 and 166 (clock outputs) as standard I/Os
- Fixed JTAG signals, + RESET/ and POR/

## **V Constraints file**



```

### For reference, see TN1262 / FPGA-TN-02032
# .lpf file format is not really documented by Lattice, normally generated through Diamond

#####
#### sysCONFIG
#####

# The BLOCK commands disable tracing of paths within clock domains (impacting overall
#   ↳ timing score)
# It can also be used on paths if the TRACE should not consider the clock domain crossing
#   like : BLOCK PATH FROM CLKNET "CLK_A" TO CLKNET "CLK_B" ;
BLOCK RESETPATHS ;
BLOCK ASYNCPATHS ;
BLOCK JTAGPATHS ;

# Not comprehensive
# dflt : CONFIG_IOVOLTAGE      1.2, 1.5, 1.8, 2.5(dflt), 3.3          voltage is 3.3V
# dflt : COMPRESS_CONFIG        OFF (dflt), ON                            no bitstream compression
# mod  : MCCLK_FREQ             2.4, 4.8, 9.7, 19.4, 38.8, 62           NOR program read @ 62MHz
# mod  : MASTER_SPI_PORT        DISABLE (dflt), ENABLE                  master SPI port stays SPI and
#   ↳ not GPIOs, other mods disabled by dflt
# dflt : BACKGROUND_RECONFIG   -                                         no soft ERC when hot-loading
#   ↳ bitstream (due to cosmic rays)
# dflt : DONE_PULL              ON (dflt), OFF                         IPU on DONE pin
# dflt : DONE_EX                OFF (dflt), ON                         not delaying end of the
#   ↳ configuration (used for daisy chaining FPGAs)
# mod  : DONE_OD                OFF (dflt), ON                         DONE pin as open-drain
#   ↳ instead of push-pull
# dflt : CONFIG_SECURE          OFF (dflt), ON                         allows external access to
#   ↳ current program
# mod  : CONFIG_MODE            JTAG (dflt), SSPI, SPI_SERIAL, SPI_DUAL, SPI_QUAD,
#   ↳ SLAVE_PARALLEL, SLAVE_SERIAL                                which bus and mode is used to
#   ↳ load configuration (for the Lattice IDE)
# dflt : TRANSFR                OFF (dflt), ON                         if using TransFR tool from
#   ↳ Lattice
# dflt : WAKE_UP                4 (set DONE=1 before starting user code, dflt for
#   ↳ DONE_EX=ON)
#   ↳ 21 (set DONE=1 once FPGA is already running user code, dflt
#   ↳ for DONE_EX=OFF)
# mod  : INBUF                  ON, OFF                           disable unused input buffers
#   ↳ (not sure it impacts the ECP5 family)
SYSCONFIG MCCLK_FREQ=62 MASTER_SPI_PORT=ENABLE DONE_OD=ON CONFIG_MODE=SPI_QUAD INBUF=OFF
#   ↳ CONFIG_IOVOLTAGE=3.3 ;
IOBUF ALLPORTS IO_TYPE=LVCMOS33 ;
#SYSCONFIG MCCLK_FREQ=62 MASTER_SPI_PORT=ENABLE DONE_OD=ON CONFIG_MODE=SPI_QUAD INBUF=OFF
#   ↳ CONFIG_IOVOLTAGE=3.3 ;
#IOBUF ALLPORTS IO_TYPE=LVCMOS33 ;

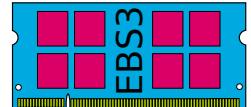
#####
#### Labs DB
#####

### Clock and reset ###
#INPUT_SETUP ALLPORTS 50.000000 ns HOLD 10.000000 ns CLKPORT "CLK" ;
#INPUT_SETUP PORT "nRST" 50.000000 ns CLKPORT "CLK" ;

FREQUENCY PORT "CLK" 100.000000 MHz ;
LOCATE COMP "CLK" SITE "K16" ;
IOBUF PORT "CLK" PULLMODE=None ;

LOCATE COMP "nRST" SITE "E13" ;
GSR_NET net "resetSynch_n" ;

```



```

### LEDs ###
LOCATE COMP "LED_nR" SITE "T14" ;
LOCATE COMP "LED_nG" SITE "R14" ;
LOCATE COMP "LED_nB" SITE "T15" ;

### USB (FTDI2232HL located on the daughterboard) ###
LOCATE COMP "USB_DB_TX" SITE "A14" ;
IOBUF PORT "USB_DB_TX" SLEWRATE=FAST ;
LOCATE COMP "USB_DB_RX" SITE "B14" ;
IOBUF PORT "USB_DB_RX" PULLMODE=UP ;
LOCATE COMP "USB_DB_RTS" SITE "B13" ;
IOBUF PORT "USB_DB_RTS" SLEWRATE=FAST ;
LOCATE COMP "USB_DB_CTS" SITE "C13" ;
IOBUF PORT "USB_DB_CTS" PULLMODE=UP ;

### SD Flash (External SD card) ###
LOCATE COMP "SD_DETECT" SITE "G12" ;
IOBUF PORT "SD_DETECT" PULLMODE=UP ;

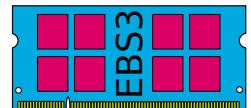
LOCATE COMP "SD_CMD" SITE "C15" ;
IOBUF PORT "SD_CMD" SLEWRATE=FAST ;
LOCATE COMP "SD_CLK" SITE "B15" ;
IOBUF PORT "SD_CLK" SLEWRATE=FAST ;

LOCATE COMP "SD_DTA[0]" SITE "B16" ;
#IOBUF PORT "SD_DTA[0]" SLEWRATE=FAST ;
LOCATE COMP "SD_DTA[1]" SITE "C16" ;
#IOBUF PORT "SD_DTA[1]" SLEWRATE=FAST ;
LOCATE COMP "SD_DTA[2]" SITE "F12" ;
#IOBUF PORT "SD_DTA[2]" SLEWRATE=FAST ;
LOCATE COMP "SD_DTA[3]" SITE "C14" ;
#IOBUF PORT "SD_DTA[3]" SLEWRATE=FAST ;

### DRAM ###
LOCATE COMP "DRAM_ADDR[0]" SITE "J15" ;
IOBUF PORT "DRAM_ADDR[0]" SLEWRATE=FAST ;
LOCATE COMP "DRAM_ADDR[1]" SITE "L16" ;
IOBUF PORT "DRAM_ADDR[1]" SLEWRATE=FAST ;
LOCATE COMP "DRAM_ADDR[2]" SITE "L15" ;
IOBUF PORT "DRAM_ADDR[2]" SLEWRATE=FAST ;
LOCATE COMP "DRAM_ADDR[3]" SITE "K15" ;
IOBUF PORT "DRAM_ADDR[3]" SLEWRATE=FAST ;
LOCATE COMP "DRAM_ADDR[4]" SITE "G15" ;
IOBUF PORT "DRAM_ADDR[4]" SLEWRATE=FAST ;
LOCATE COMP "DRAM_ADDR[5]" SITE "F15" ;
IOBUF PORT "DRAM_ADDR[5]" SLEWRATE=FAST ;
LOCATE COMP "DRAM_ADDR[6]" SITE "F16" ;
IOBUF PORT "DRAM_ADDR[6]" SLEWRATE=FAST ;
LOCATE COMP "DRAM_ADDR[7]" SITE "E16" ;
IOBUF PORT "DRAM_ADDR[7]" SLEWRATE=FAST ;
LOCATE COMP "DRAM_ADDR[8]" SITE "E15" ;
IOBUF PORT "DRAM_ADDR[8]" SLEWRATE=FAST ;
LOCATE COMP "DRAM_ADDR[9]" SITE "G13" ;
IOBUF PORT "DRAM_ADDR[9]" SLEWRATE=FAST ;
LOCATE COMP "DRAM_ADDR[10]" SITE "M16" ;
IOBUF PORT "DRAM_ADDR[10]" SLEWRATE=FAST ;
LOCATE COMP "DRAM_ADDR[11]" SITE "F13" ;
IOBUF PORT "DRAM_ADDR[11]" SLEWRATE=FAST ;
LOCATE COMP "DRAM_ADDR[12]" SITE "D16" ;
IOBUF PORT "DRAM_ADDR[12]" SLEWRATE=FAST ;

LOCATE COMP "DRAM_BA[0]" SITE "L14" ;
IOBUF PORT "DRAM_BA[0]" SLEWRATE=FAST ;
LOCATE COMP "DRAM_BA[1]" SITE "L13" ;

```



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IOBUF PORT "DRAM_BA[1]" SLEWRATE=FAST ;

LOCATE COMP "DRAM_CLK" SITE "G14" ;
IOBUF PORT "DRAM_CLK" SLEWRATE=FAST ;
LOCATE COMP "DRAM_CKE" SITE "G16" ;
IOBUF PORT "DRAM_CKE" SLEWRATE=FAST ;
LOCATE COMP "DRAM_nRAS" SITE "M14" ;
IOBUF PORT "DRAM_nRAS" SLEWRATE=FAST ;
LOCATE COMP "DRAM_nCAS" SITE "K13" ;
IOBUF PORT "DRAM_nCAS" SLEWRATE=FAST ;
LOCATE COMP "DRAM_nWE" SITE "N16" ;
IOBUF PORT "DRAM_nWE" SLEWRATE=FAST ;
LOCATE COMP "DRAM_nCS" SITE "M15" ;

LOCATE COMP "DRAM_DQ[0]" SITE "P14" ;
LOCATE COMP "DRAM_DQ[1]" SITE "R15" ;
LOCATE COMP "DRAM_DQ[2]" SITE "N14" ;
LOCATE COMP "DRAM_DQ[3]" SITE "R16" ;
LOCATE COMP "DRAM_DQ[4]" SITE "J14" ;
LOCATE COMP "DRAM_DQ[5]" SITE "P15" ;
LOCATE COMP "DRAM_DQ[6]" SITE "K14" ;
LOCATE COMP "DRAM_DQ[7]" SITE "P16" ;
LOCATE COMP "DRAM_DQ[8]" SITE "D14" ;
LOCATE COMP "DRAM_DQ[9]" SITE "H14" ;
LOCATE COMP "DRAM_DQ[10]" SITE "H12" ;
LOCATE COMP "DRAM_DQ[11]" SITE "H13" ;
LOCATE COMP "DRAM_DQ[12]" SITE "E14" ;
LOCATE COMP "DRAM_DQ[13]" SITE "H15" ;
LOCATE COMP "DRAM_DQ[14]" SITE "J13" ;
LOCATE COMP "DRAM_DQ[15]" SITE "J16" ;

LOCATE COMP "DRAM_DQM[0]" SITE "M13" ;
IOBUF PORT "DRAM_DQM[0]" SLEWRATE=FAST ;
LOCATE COMP "DRAM_DQM[1]" SITE "F14" ;
IOBUF PORT "DRAM_DQM[1]" SLEWRATE=FAST ;

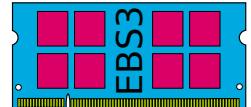
#####
#### SODIMM-200
#####

### USB (chip located on the motherboard) ###
LOCATE COMP "USB_MB_TX" SITE "M11" ;
IOBUF PORT "USB_MB_TX" SLEWRATE=FAST ;
LOCATE COMP "USB_MB_RX" SITE "N12" ;
IOBUF PORT "USB_MB_RX" PULLMODE=UP ;
LOCATE COMP "USB_MB RTS" SITE "N11" ;
IOBUF PORT "USB_MB RTS" SLEWRATE=FAST ;
LOCATE COMP "USB_MB CTS" SITE "M12" ;
IOBUF PORT "USB_MB CTS" PULLMODE=UP ;

### PMOD1 ###
LOCATE COMP "PMOD1[1]" SITE "P1" ;
LOCATE COMP "PMOD1[2]" SITE "N4" ;
LOCATE COMP "PMOD1[3]" SITE "P2" ;
LOCATE COMP "PMOD1[4]" SITE "P5" ;
LOCATE COMP "PMOD1[5]" SITE "R1" ;
LOCATE COMP "PMOD1[6]" SITE "N5" ;
LOCATE COMP "PMOD1[7]" SITE "R2" ;
LOCATE COMP "PMOD1[8]" SITE "N6" ;

### PMOD2 ###
LOCATE COMP "PMOD2[1]" SITE "R3" ;
LOCATE COMP "PMOD2[2]" SITE "P11" ;
LOCATE COMP "PMOD2[3]" SITE "P12" ;
LOCATE COMP "PMOD2[4]" SITE "T3" ;

```



```

LOCATE COMP "PMOD2[5]" SITE "R4" ;
LOCATE COMP "PMOD2[6]" SITE "R12" ;
LOCATE COMP "PMOD2[7]" SITE "T13" ;
LOCATE COMP "PMOD2[8]" SITE "R5" ;

### PMOD3 ####
LOCATE COMP "PMOD3[1]" SITE "B2" ;
LOCATE COMP "PMOD3[2]" SITE "B3" ;
LOCATE COMP "PMOD3[3]" SITE "A4" ;
LOCATE COMP "PMOD3[4]" SITE "D4" ;
LOCATE COMP "PMOD3[5]" SITE "A2" ;
LOCATE COMP "PMOD3[6]" SITE "B4" ;
LOCATE COMP "PMOD3[7]" SITE "C3" ;
LOCATE COMP "PMOD3[8]" SITE "C4" ;

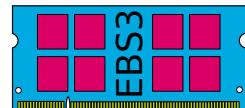
### PMOD4 ####
LOCATE COMP "PMOD4[1]" SITE "J4" ;
LOCATE COMP "PMOD4[2]" SITE "J5" ;
LOCATE COMP "PMOD4[3]" SITE "H4" ;
LOCATE COMP "PMOD4[4]" SITE "E4" ;
LOCATE COMP "PMOD4[5]" SITE "J3" ;
LOCATE COMP "PMOD4[6]" SITE "H3" ;
LOCATE COMP "PMOD4[7]" SITE "E3" ;
LOCATE COMP "PMOD4[8]" SITE "D3" ;

### PP1 ####
LOCATE COMP "PP1[1]" SITE "A9" ;
LOCATE COMP "PP1[2]" SITE "D10" ;
LOCATE COMP "PP1[3]" SITE "A10" ;
LOCATE COMP "PP1[4]" SITE "C10" ;
LOCATE COMP "PP1[5]" SITE "B10" ;
LOCATE COMP "PP1[6]" SITE "C12" ;
LOCATE COMP "PP1[7]" SITE "B12" ;
LOCATE COMP "PP1[8]" SITE "D13" ;
LOCATE COMP "PP1[9]" SITE "A13" ;
LOCATE COMP "PP1[10]" SITE "M5" ; # PP1 11
LOCATE COMP "PP1[11]" SITE "L5" ; # PP1 13
LOCATE COMP "PP1[12]" SITE "K5" ; # PP1 15
LOCATE COMP "PP1[13]" SITE "H5" ; # PP1 17
LOCATE COMP "PP1[14]" SITE "E8" ; # PP1 19
LOCATE COMP "PP1[15]" SITE "E5" ; # PP1 21
LOCATE COMP "PP1[16]" SITE "E6" ; # PP1 23
LOCATE COMP "PP1[17]" SITE "E7" ; # PP1 25

### PP2 ####
LOCATE COMP "PP2[1]" SITE "G3" ;
LOCATE COMP "PP2[2]" SITE "E1" ;
LOCATE COMP "PP2[3]" SITE "F3" ;
LOCATE COMP "PP2[4]" SITE "D1" ;
LOCATE COMP "PP2[5]" SITE "F4" ;
LOCATE COMP "PP2[6]" SITE "C1" ;
LOCATE COMP "PP2[7]" SITE "D7" ;
LOCATE COMP "PP2[8]" SITE "B6" ;
LOCATE COMP "PP2[9]" SITE "C7" ;
LOCATE COMP "PP2[10]" SITE "A6" ; # PP2 11
LOCATE COMP "PP2[11]" SITE "D8" ; # PP2 13
LOCATE COMP "PP2[12]" SITE "B7" ; # PP2 15
LOCATE COMP "PP2[13]" SITE "C8" ; # PP2 17
LOCATE COMP "PP2[14]" SITE "A7" ; # PP2 19
LOCATE COMP "PP2[15]" SITE "E9" ; # PP2 21
LOCATE COMP "PP2[16]" SITE "A8" ; # PP2 23
LOCATE COMP "PP2[17]" SITE "D9" ; # PP2 25

### Ethernet ####

```



```

LOCATE COMP "ETH_CLK_EN" SITE "B1" ;
LOCATE COMP "ETH_nRESET" SITE "C2" ;

LOCATE COMP "ETH_nLED_Y" SITE "F1" ;
LOCATE COMP "ETH_nLED_G" SITE "G2" ;

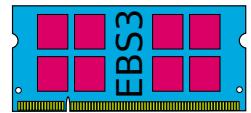
LOCATE COMP "ETH_MDC" SITE "J1" ;
LOCATE COMP "ETH_MDIO" SITE "H2" ;
IOBUF PORT "ETH_MDIO" OPENDRAIN=ON SLEWRATE=FAST ;
LOCATE COMP "ETH_MDINT" SITE "G1" ;
IOBUF PORT "ETH_MDINT" SLEWRATE=FAST ;

LOCATE COMP "ETH_REF_CLK" SITE "P3" ;
LOCATE COMP "ETH_TX_CLK" SITE "M4" ;
IOBUF PORT "ETH_TX_CLK" SLEWRATE=FAST ;
LOCATE COMP "ETH_TX_CTL" SITE "N3" ;
IOBUF PORT "ETH_TX_CTL" SLEWRATE=FAST ;
LOCATE COMP "ETH_TXD[0]" SITE "M3" ;
IOBUF PORT "ETH_TXD[0]" SLEWRATE=FAST ;
LOCATE COMP "ETH_TXD[1]" SITE "L4" ;
IOBUF PORT "ETH_TXD[1]" SLEWRATE=FAST ;
LOCATE COMP "ETH_TXD[2]" SITE "K4" ;
IOBUF PORT "ETH_TXD[2]" SLEWRATE=FAST ;
LOCATE COMP "ETH_TXD[3]" SITE "K3" ;
IOBUF PORT "ETH_TXD[3]" SLEWRATE=FAST ;

LOCATE COMP "ETH_RX_CLK" SITE "K1" ;
LOCATE COMP "ETH_RX_CTL" SITE "K2" ;
LOCATE COMP "ETH_RXD[0]" SITE "L1" ;
LOCATE COMP "ETH_RXD[1]" SITE "L2" ;
LOCATE COMP "ETH_RXD[2]" SITE "M1" ;
LOCATE COMP "ETH_RXD[3]" SITE "M2" ;

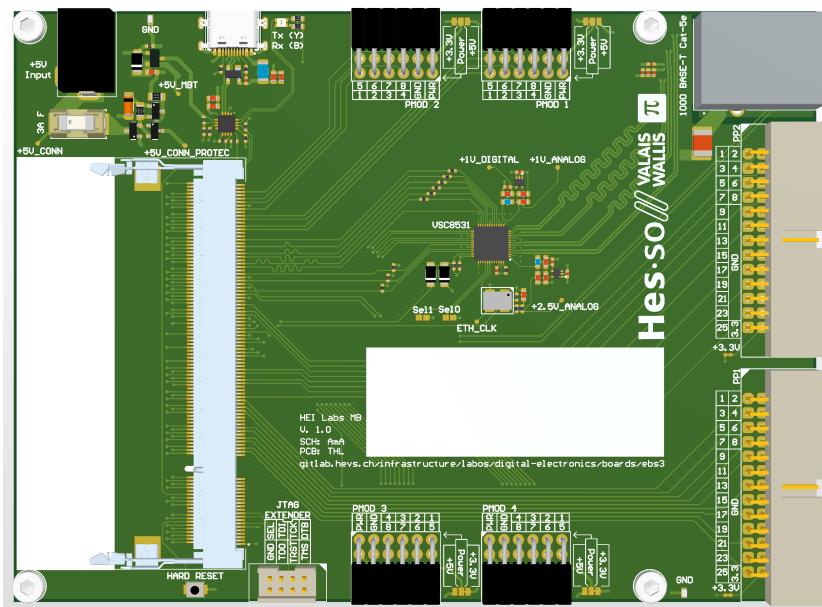
### Extras ###
LOCATE COMP "EXT[1]" SITE "P13" ;
LOCATE COMP "EXT[2]" SITE "R13" ;
LOCATE COMP "EXT[3]" SITE "A3" ;
LOCATE COMP "EXT[4]" SITE "A5" ;
LOCATE COMP "EXT[5]" SITE "B5" ;
LOCATE COMP "EXT[6]" SITE "C5" ;
LOCATE COMP "EXT[7]" SITE "C6" ;
LOCATE COMP "EXT[8]" SITE "D5" ;
LOCATE COMP "EXT[9]" SITE "D6" ;
LOCATE COMP "EXT[10]" SITE "A11" ;
LOCATE COMP "EXT[11]" SITE "A12" ;
LOCATE COMP "EXT[12]" SITE "B8" ;
LOCATE COMP "EXT[13]" SITE "B9" ;
LOCATE COMP "EXT[14]" SITE "B11" ;
LOCATE COMP "EXT[15]" SITE "C9" ;
LOCATE COMP "EXT[16]" SITE "C11" ;
LOCATE COMP "EXT[17]" SITE "D11" ;
LOCATE COMP "EXT[18]" SITE "D12" ;
LOCATE COMP "EXT[19]" SITE "E10" ;
LOCATE COMP "EXT[20]" SITE "E11" ;
LOCATE COMP "EXT[21]" SITE "E12" ;
LOCATE COMP "EXT[22]" SITE "L3" ;
LOCATE COMP "EXT[23]" SITE "M6" ;
LOCATE COMP "EXT[24]" SITE "N1" ;
LOCATE COMP "EXT[25]" SITE "P4" ;
LOCATE COMP "EXT[26]" SITE "P6" ;
LOCATE COMP "EXT[27]" SITE "T2" ;
LOCATE COMP "EXT[28]" SITE "T4" ;
LOCATE COMP "EXT[29]" SITE "E2" ;
LOCATE COMP "EXT[30]" SITE "F2" ;
LOCATE COMP "EXT[31]" SITE "F5" ;
LOCATE COMP "EXT[32]" SITE "G4" ;

```



```
LOCATE COMP "EXT[33]" SITE "G5" ;  
LOCATE COMP "EXT[34]" SITE "J2" ;
```





# Labs Motherboard (Pmod, Gigabit Eth., Parallel Port)

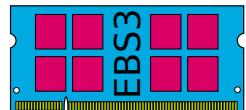
**Hes-SO**// **VALAIS**  
**WALLIS**

 School of Engineering

Author: [Amand Axel, Silvan Zahno](#)

Date: March 20, 2023

Version: v1.0



## 1 Overview

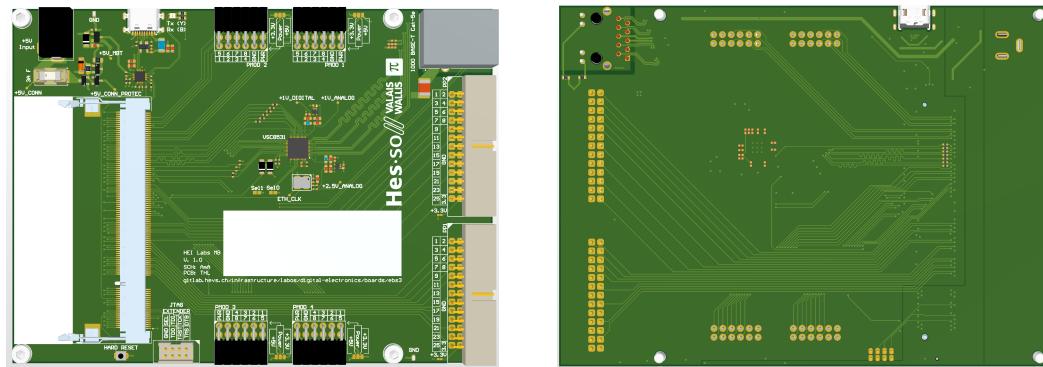


Figure 1: PCB board

The boards embeds the following functionalities:

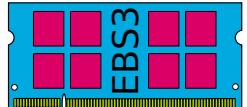
- Barrel-plug power input with reverse voltage and overvoltage protection
- Four standard dual PMOD connectors (in 2 pairs configuration)
- Two parallel ports
- Gigabit ethernet controller
- USB-C (norm 2.0) - UART converter
- JTAG path extender connector
- Extra reset button for the [FPGA](#)

### Technical files

The schematic of the board is given under [I Schematic](#).

Rooting is available under [II Rooting](#) (*open the page with Inkscape for layers*).

The bill of material is given under [III BOM](#).



## 2 Specifications

### 2.1 Overview

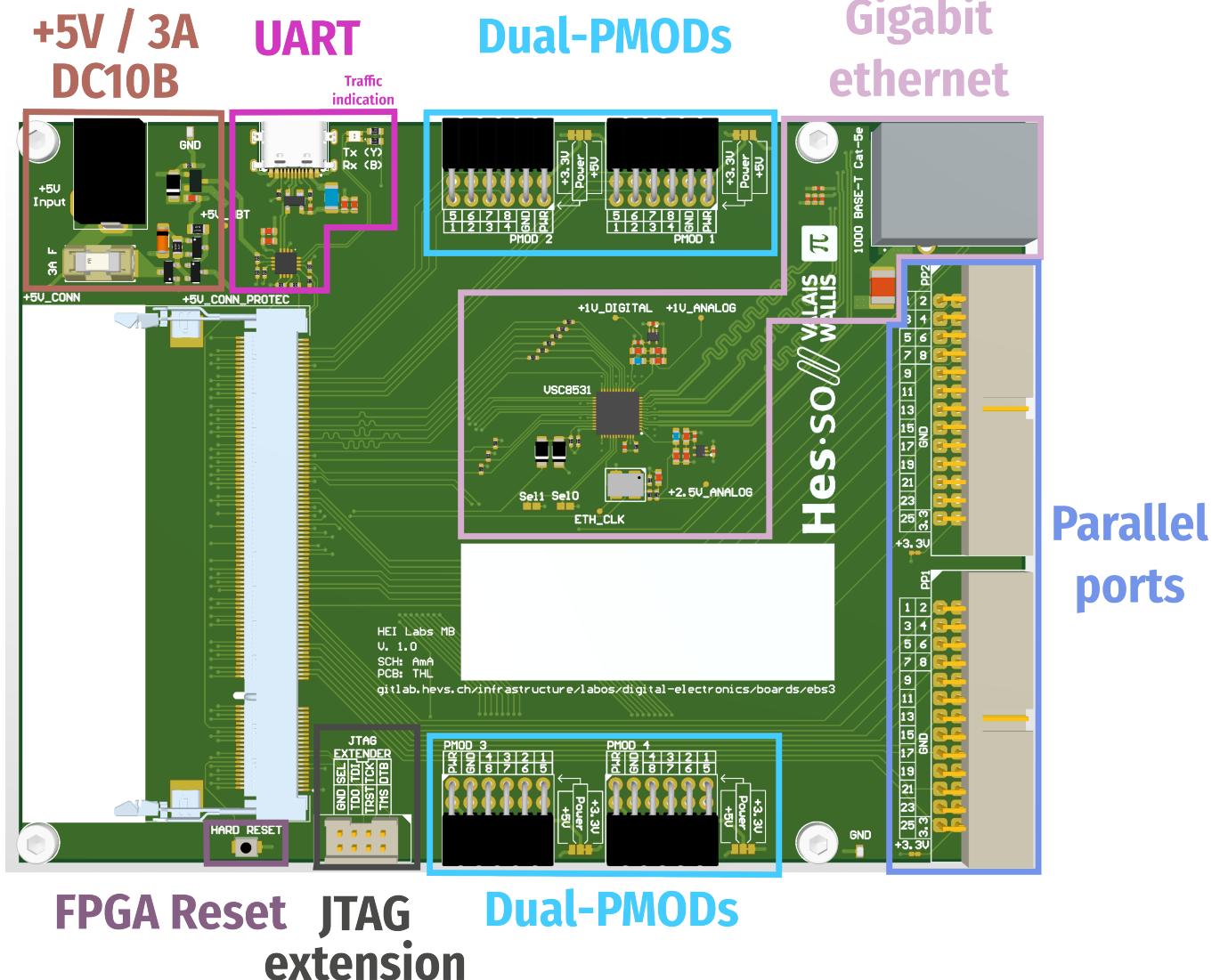


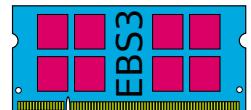
Figure 2: Card overview

### 2.2 Supply

The board is powered from either (in order of precedence):

1. The barrel plug (external +5VDC power supply)
2. The embedded USB connector
3. The USB-C on the daughterboard card

All sources will completely power the board, EXCEPT if the PMOD voltage jumpers are set to +5V instead of +3.3V (in which case they will not be fed with +5V when powered through the daughterboard).



**Source selection** The +5V input is chosen from either the barrel plug or the USB with the following circuit:

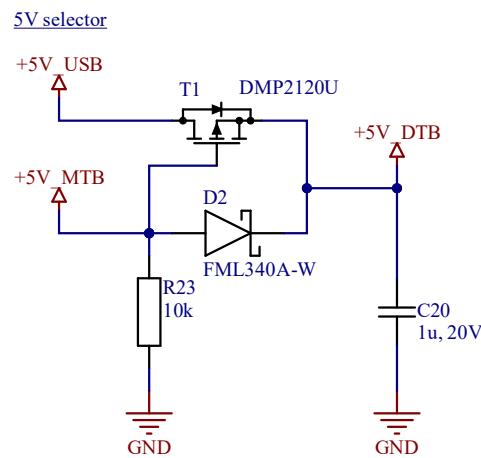


Figure 3: +5V selector - Circuit

Three cases:

- **+5V\_USB, no +5V\_MTB** : the transistors gate is low => it conducts fully, the diode blocks the path back to +5V\_MTB.
- no +5V\_USB, **+5V\_MTB** : the diode conducts with a slight loss, while the transistors diode blocks the path back to +5V\_USB.
- **+5V\_USB, +5V\_MTB** : the transistors gate is high => it blocks, and the internal diode blocks too (+5V on both sides). *Danger here would be for a too high voltage on the USB rail which would then take precedence over the MTB rail if  $U_{usb} > U_{mtb} - U_{d2} + U_{dt1}$ .*

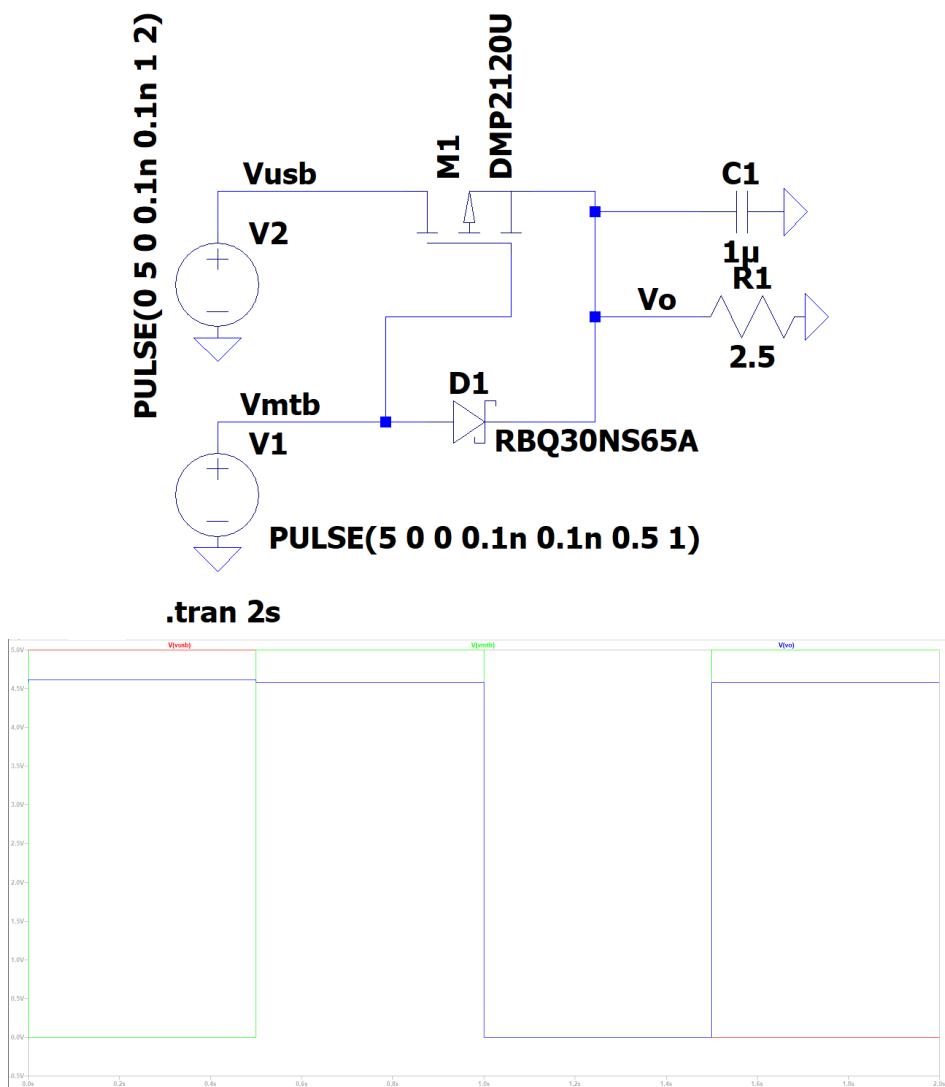
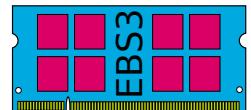


Figure 4: +5V selector - Simulation

The same system is present on the daughterboard to choose between its USB-C or the power coming from the motherboard (which takes precedence).

**Overvoltage protection** The overvoltage protection is solely present on the barrel plug connector, not on the USB source:

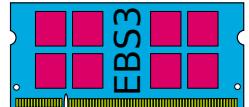
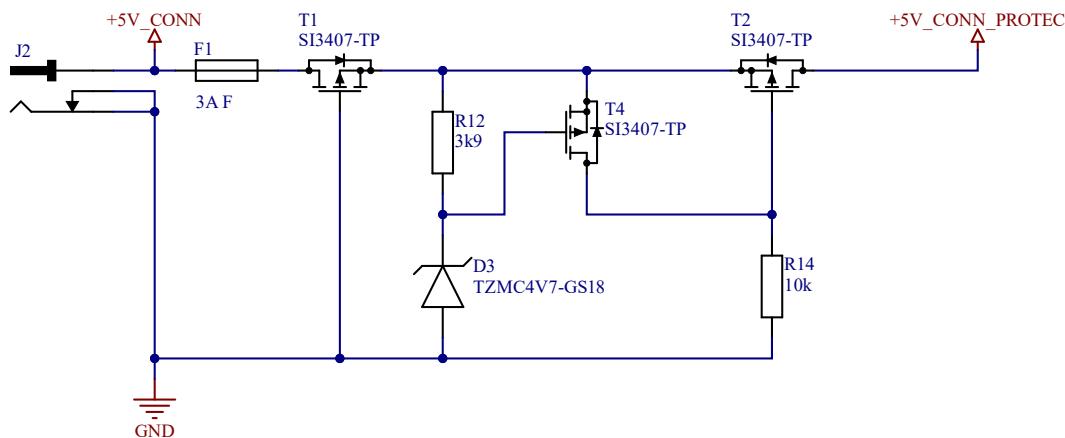
5V external supply

Figure 5: +5V protection - Circuit

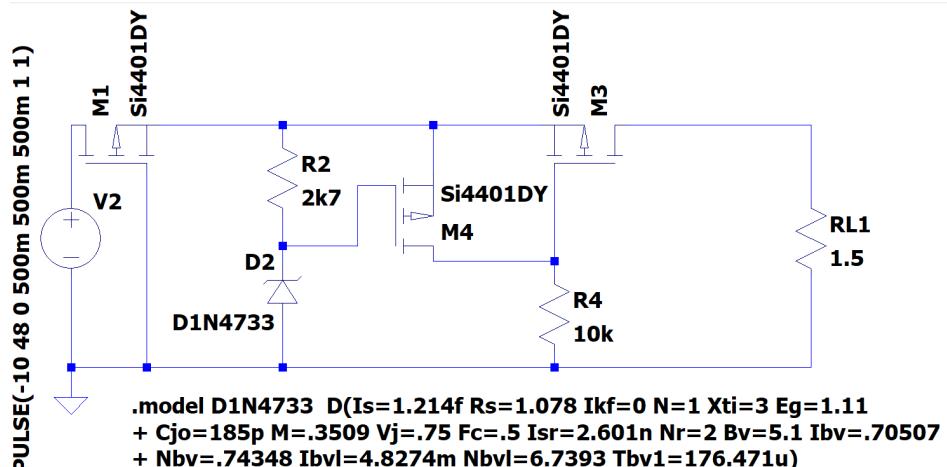
The reverse protection is provided by T1 which, when its power is reversed, will block. A 3A - slow blow fuse is present as extra protection over current surges.

The overvoltage protection works as follows:

- With  $V_{in}$  from 0 to 4.7 V, the voltage on the zener diode D3 rises with the input. T4 blocks while T2 conducts (its gate being set to ground through R14).
- Afterward,  $V_g$  of T4 is clamped to this value and such T4 slowly begins to conduct (T2's gate voltage rises).
- Some voltage higher, T2 blocks, protecting the output.

Since this circuit is open-loop (but cheap), variations will happen on the board (either the combo R12 - D3 changes T4's gate voltage, T4's gain is slightly different, or T2's  $V_{gs}$  differs). As a reference with given components, the mean threshold voltage is around 5.15 V and drops to 0 V in a tenth of millivolts.

With the rise in temperature, the threshold value decreases:



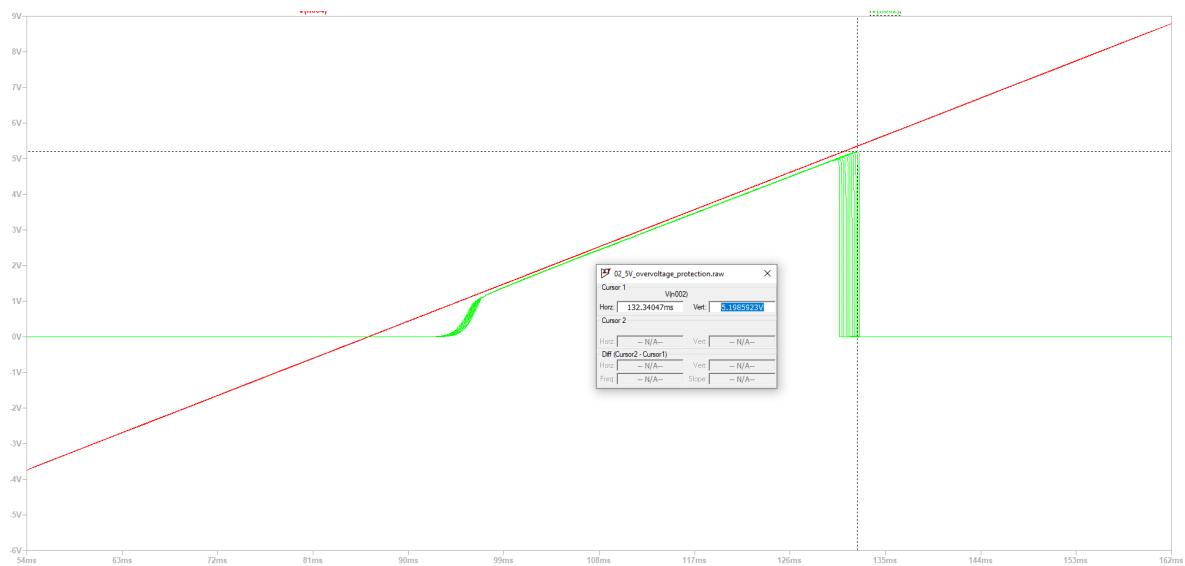
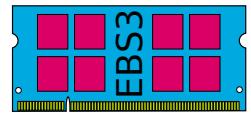


Figure 6: +5V protection - Simulation

### 2.3 I/Os connectors

**PMOD** The four PMOD connectors (J3 to J6) present on the board are standard dual PMODs (8 I/Os). The female socket, front faced, contains the following pins:

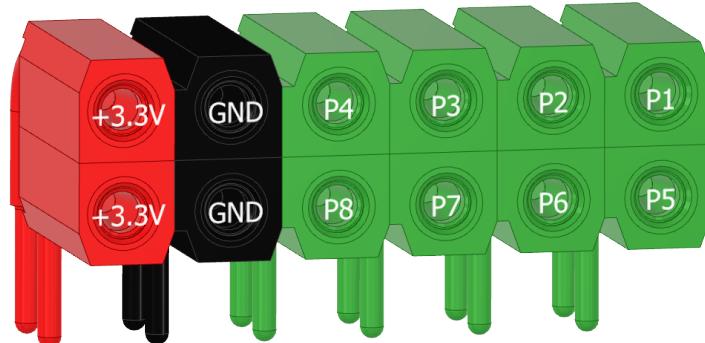


Figure 7: PMODs pinning

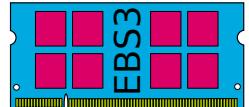


As a general rule, extension boards content ([LEDs](#), buttons ...) should face upward.

The delivered voltage can be changed by switching jumpers 1 to 4 (JPx) to either +3.3 V or +5 V.



+5 V can only be used to power boards which DO NOT feed this voltage back to the [FPGA](#) or it may destroy it.



**Parallel port** The two parallel port (PPx) offer 17 I/Os each with a fixed voltage of +3.3 V. The pinning as seen from the front of the connector:

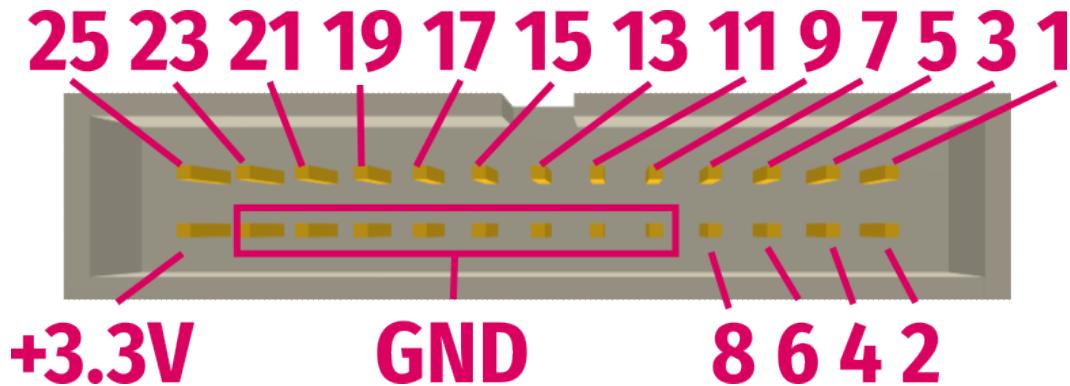


Figure 8: Parallel ports pinning

## 2.4 Reset

The button labeled **Hard Reset** allows to reset the FPGA by setting the **nRESET\_IN** signal low.

## 2.5 USB - UART

The USB-C connector (norm 2.0), the CP2102N from Cypress, offer an extra way to transmit data through a virtual COM port. The RTS/CTS flow control pins are also wired.

The yellow **LED** blinks when data is transmitted to the host, while the blue one indicates received data.

## 2.6 Gigabit ethernet

A gigabit ethernet port is available on the board, requiring at least a cat. 5e cable (1000 base-t). The MAC controller is a VSC8531 from Microchip clocked at 125 MHz (which can be enabled from the **FPGA**).

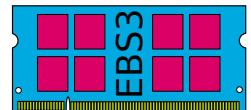
Only half of the Tx and Rx lines are exposed to the **FPGA**, requiring to read/send on both rising and falling edge of the clock.

The chip is controlled through a serial management interface (MDC, MDIO and MDINT).

Two user **LEDs** on the ethernet connector can be controlled from the **FPGA**.

Two jumpers **SEL1-0** are used when the oscillator frequency is modified. In default configuration, it expects a 125 MHz clock from an oscillator (one pin). They can be soldered following this table (0 meaning the pad is soldered, driving the chip's pin to GND):

SEL0	SEL1	Frequency MHz	Note
0	0	25	crystal on XTAL 1-2 (not possible on this board)
0	1	25	oscillator on XTAL 1
1	0	50	oscillator on XTAL 1
1	1	125	oscillator on XTAL 1



## 2.7 JTAG extender

Connector J11 allow for extending the JTAG path with extra chips. It is not standardized and will certainly require a specific cable:

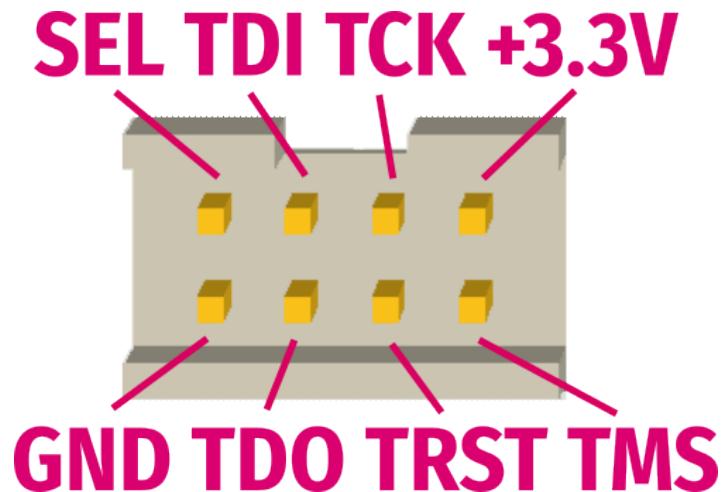
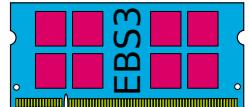


Figure 9: JTAG extender pining

**SEL** is a signal which must be set to GND which cuts the JTAG path of the daughterboard to allow data coming through this connector.



### 3 SW Configuration

The board is used with Diamond Diamond (Lattice).

#### 3.1 Board configuration

The default configuration (constraints file) for the board is available under [IV Constraints file](#).

- Pins voltages are set with:

```
IOBUF ALLPORTS IO_TYPE=LVCMS33 ; (set all ports to 3.3V)
Two pins in the same bank cannot have different voltages.
```

- The system is configured with:

```
SYS CONFIG MCCLK_FREQ=62 MASTER_SPI_PORT=ENABLE DONE_OD=ON
CONFIG_MODE=SPI_QUAD INBUF=OFF CONFIG_IOVOLTAGE=3.3 ;
```

*The various options are given in the constraints file. Here :*

- The flash access clock to load the program is set to its maximum, i.e. 62 MHz*
- Mode is MASTER\_SPI\_PORT, with CONFIG\_MODE specifying the flash can be read in quad-SPI mode*
- The DONE pin is open-drain*
- Unused input buffers are deactivated*
- Pins from the sysCONFIG bank are set to 3.3V*

- The clock is specified by its frequency (for timing analysis) with:

```
FREQUENCY PORT "CLK" 100.000000 MHz ;
```

The pin is then specified with:

```
LOCATE COMP "CLK" SITE "K16" ;
```

- The reset signal pin is set with:

```
LOCATE COMP "nRST" SITE "E13" ;
```

To specify the reset net for possibly undefined latches resets (Global Set-Reset net):

```
GSR_NET net "resetSynch_n" ;
```

*In the VHDL file, the reset signal must be name resetSynch\_n.*

- I/Os directions are not specified. The pin is first linked to the net with:

```
LOCATE COMP "SD_DETECT" SITE "G12" ; special functionalities can be set:
```

```
IOBUF PORT "SD_DETECT" PULLMODE=UP ;
```

- for inputs, a pull resistor can be set with PULLMODE=UP | DOWN
- for outputs, the slewrate can be set with SLEWRATE=SLOW | FAST, the driving capability with DRIVE=4|8|12|16

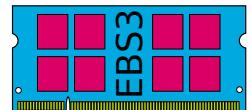
- Other settings exist. In Diamond, open the "Spreadsheet View" for an interactive edit of the I/O pins.*

#### 3.2 Test project

*The tester is planned for 100 MHz clocks.*

A HDL Designer test project is available with the following:

- Most LEDs and I/Os will light at three various frequencies.



- The UART and flow controls are redirected to the motherboard.
- The DRAM and SD-card are disabled (not tested yet).
- The blue LED lights up when a card is detected.

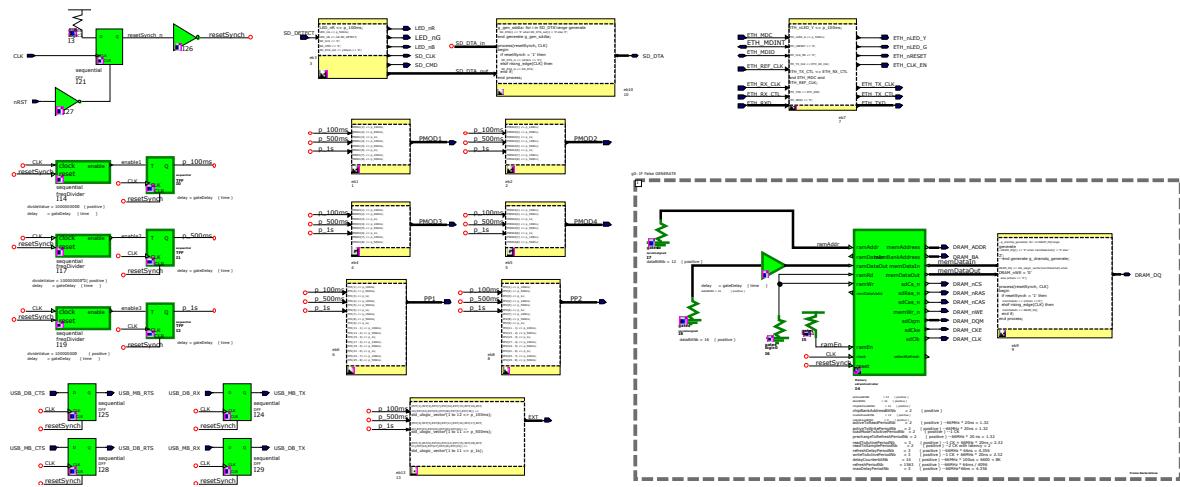
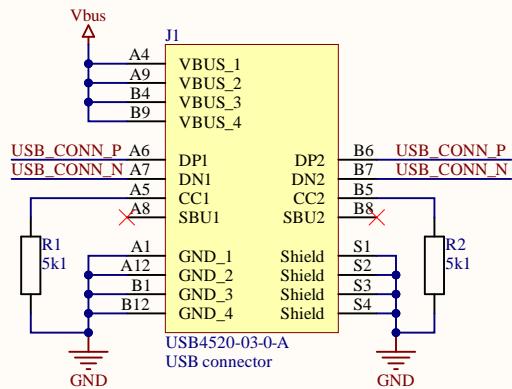
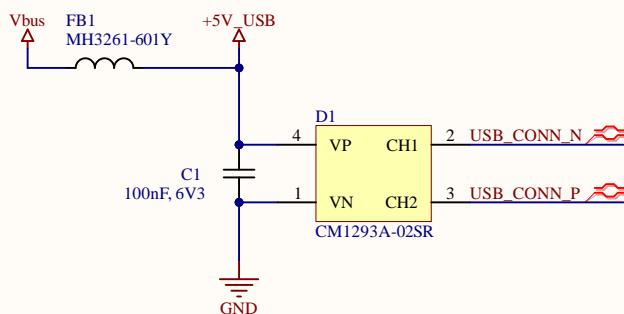
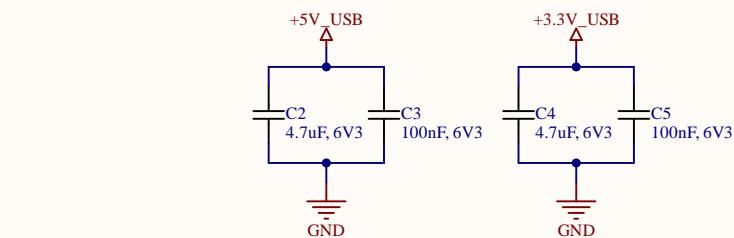
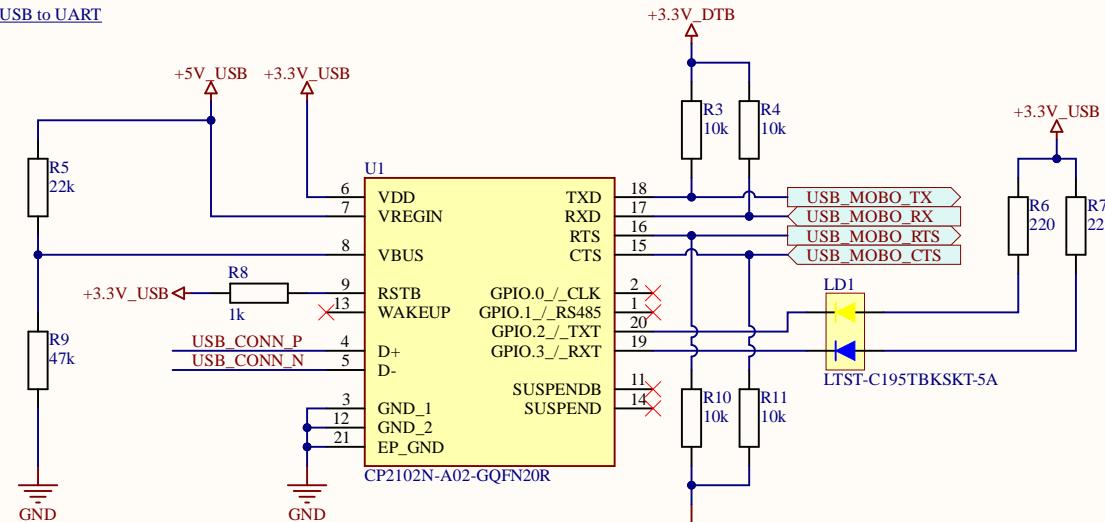


Figure 10: HDL Designer test program

# I Schematic

USB-C Connector + signal integrity

## Bus EMC protection

USB to UART

Lab\_Mobo.PrjPcb

USB.SchDoc

**Hes-SO** VALAIS WALLIS

Date : 15.11.2022



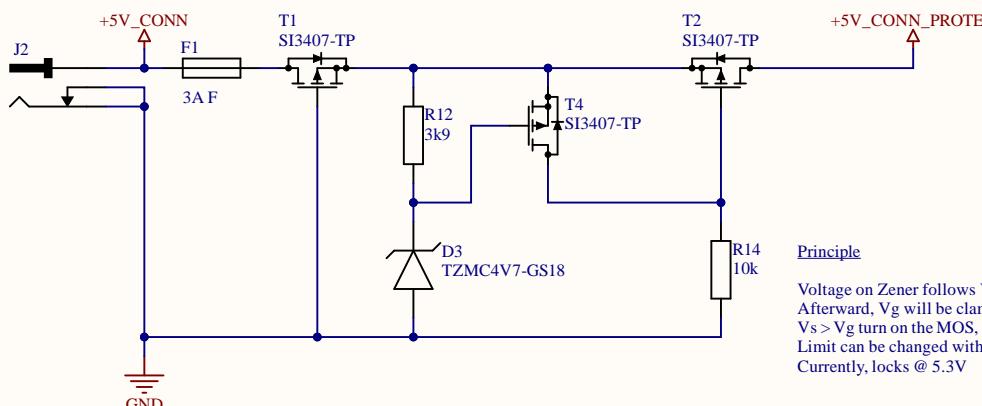
Revision : 1.0

Sheet 1 of 6

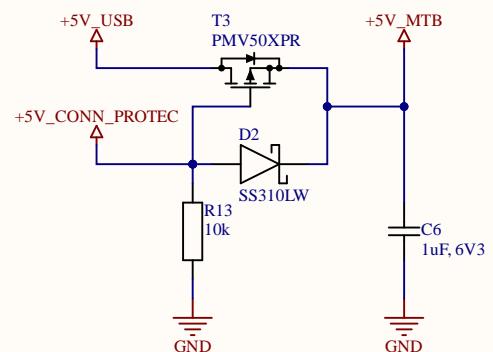
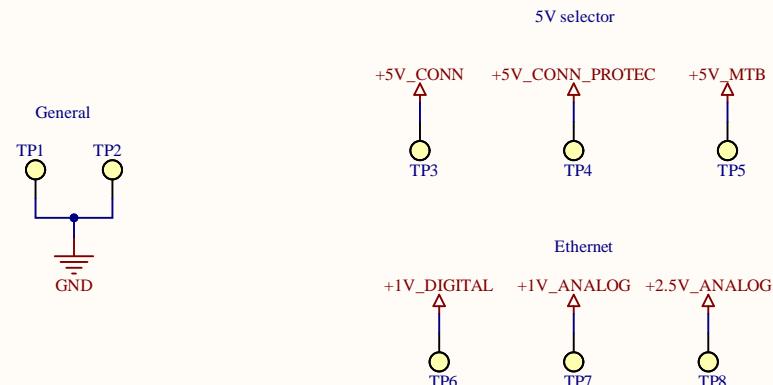
Design by : AmA

C:\dev\eb3\10\_PCB\04\_Labs\_Mobo\Lab\_Mobo\USB.SchDoc

1 2 3 4

5V external supplyPrinciple

Voltage on Zener follows Vin in the range 0 ... 4.7 V  
 Afterward, Vg will be clamped while Vs raises (as Vs = Vin)  
 $V_s > V_g$  turn on the MOS, making the second gate high and blocking voltage.  
 Limit can be changed with R12 (and ev. D3 value)  
 Currently, locks @ 5.3V

5V selectorTestpoints

Lab\_Mobo.PrjPcb

**Hes-SO** VALAIS WALLIS

Power.SchDoc

Date : 15.11.2022



Revision : 1.0

Sheet 2 of 6

Design by : AmA

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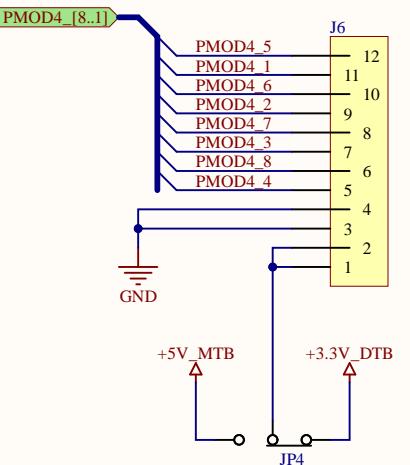
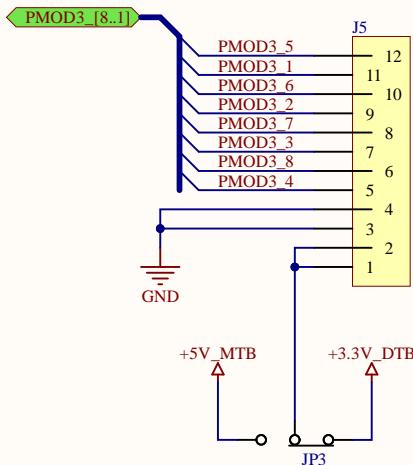
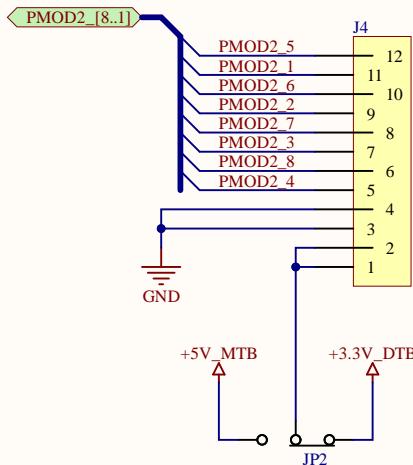
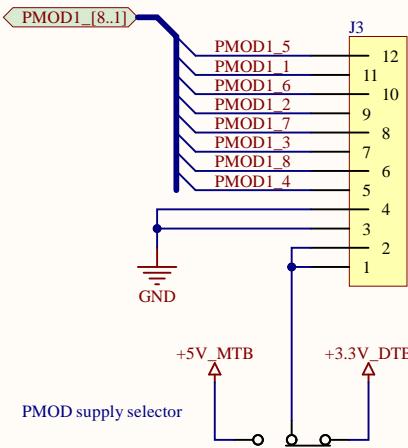
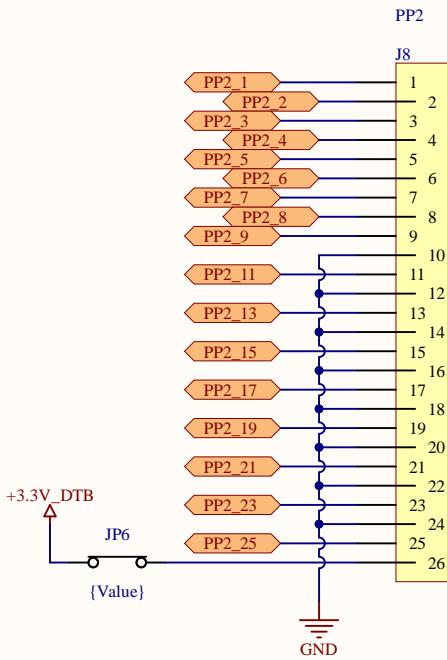
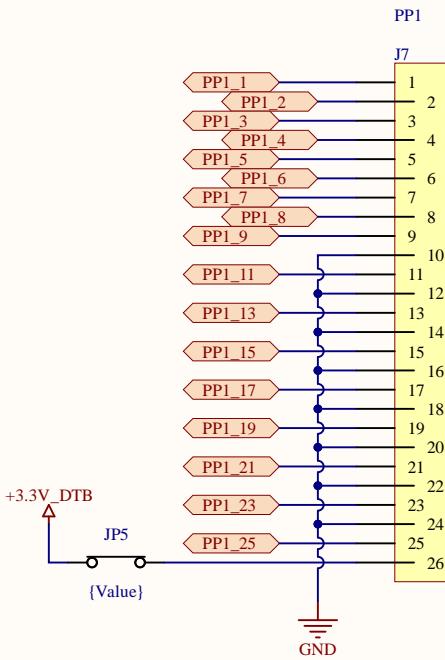
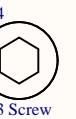
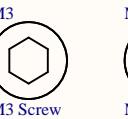
1 2 3 4

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PMOD connectorsParallel portsOther

Lab\_Mobo.PrjPcb

**Hes-SO** // VALAIS WALLIS

Date : 15.11.2022



IOs.SchDoc

Revision : 1.0

Sheet 3 of 6

Design by : AmA

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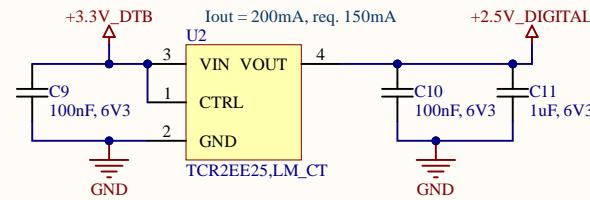
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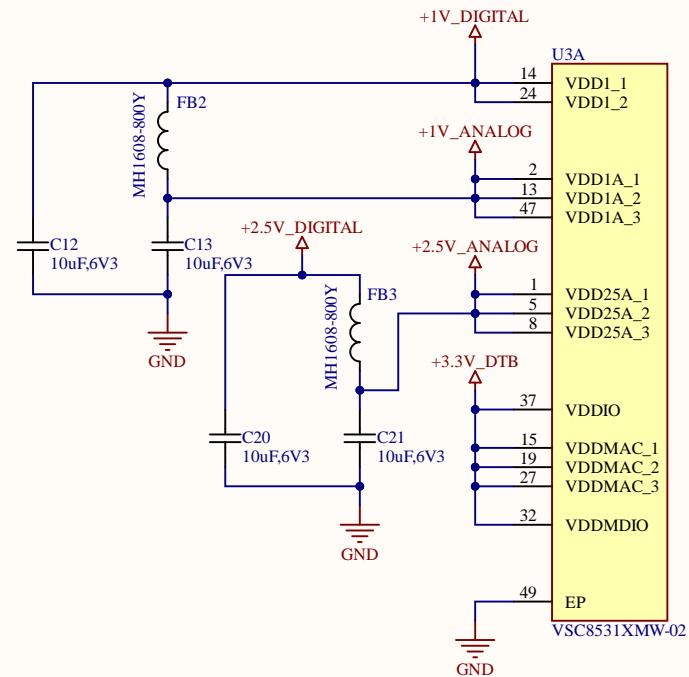
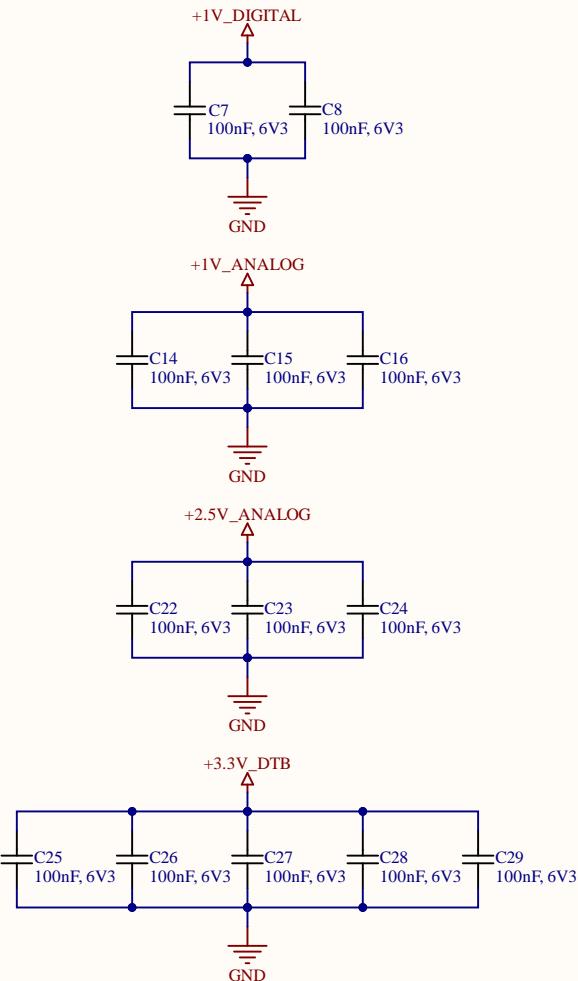
Regulators

A

B

C

D

Ethernet powerDecoupling
**Hes-SO** // VALAIS WALLIS

Date : 15.11.2022



Lab\_Mobo.PrjPcb

Ethernet\_Power.SchDoc

Revision : 1.0

Sheet 4 of 6

Design by : AmA

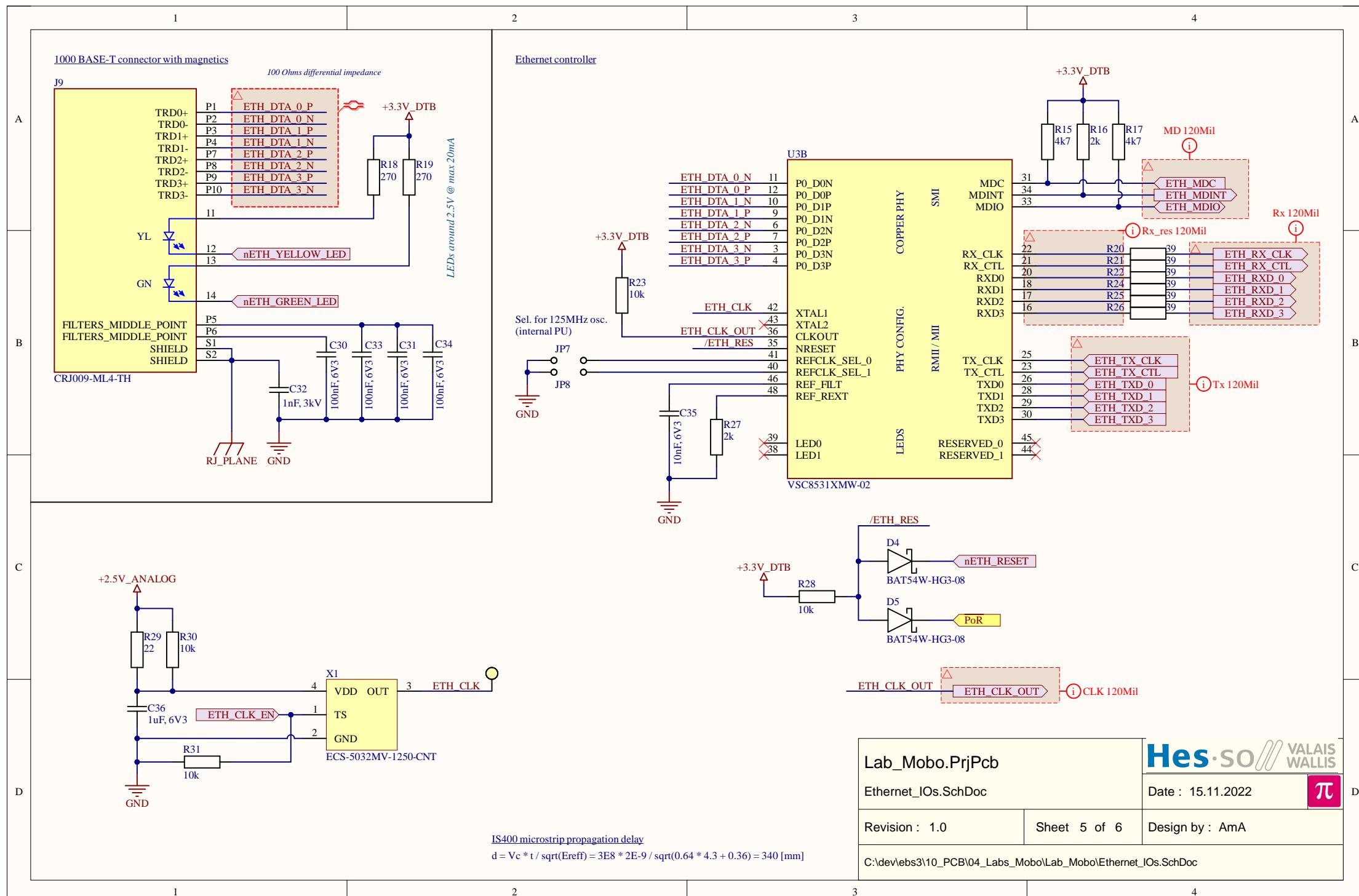
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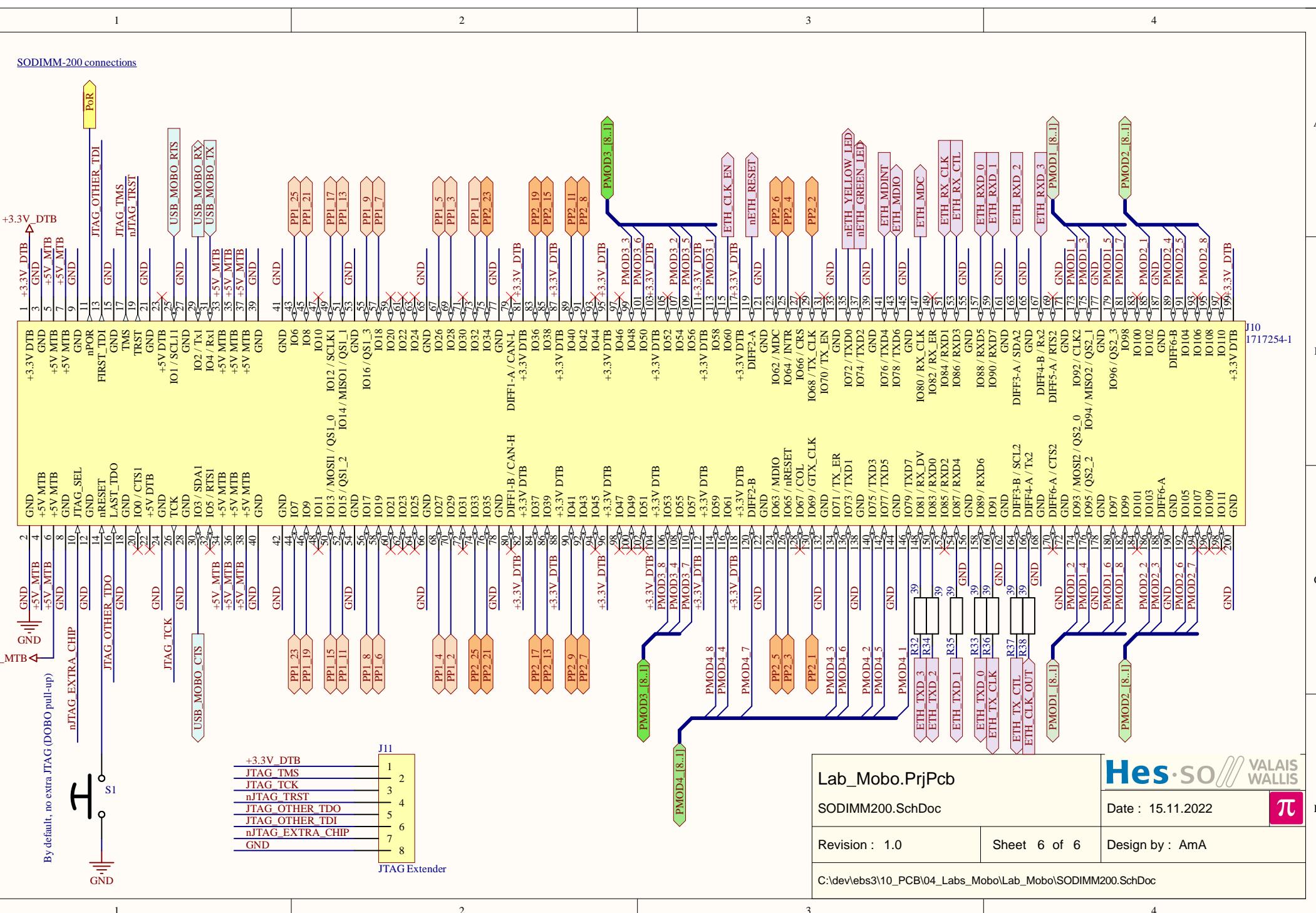
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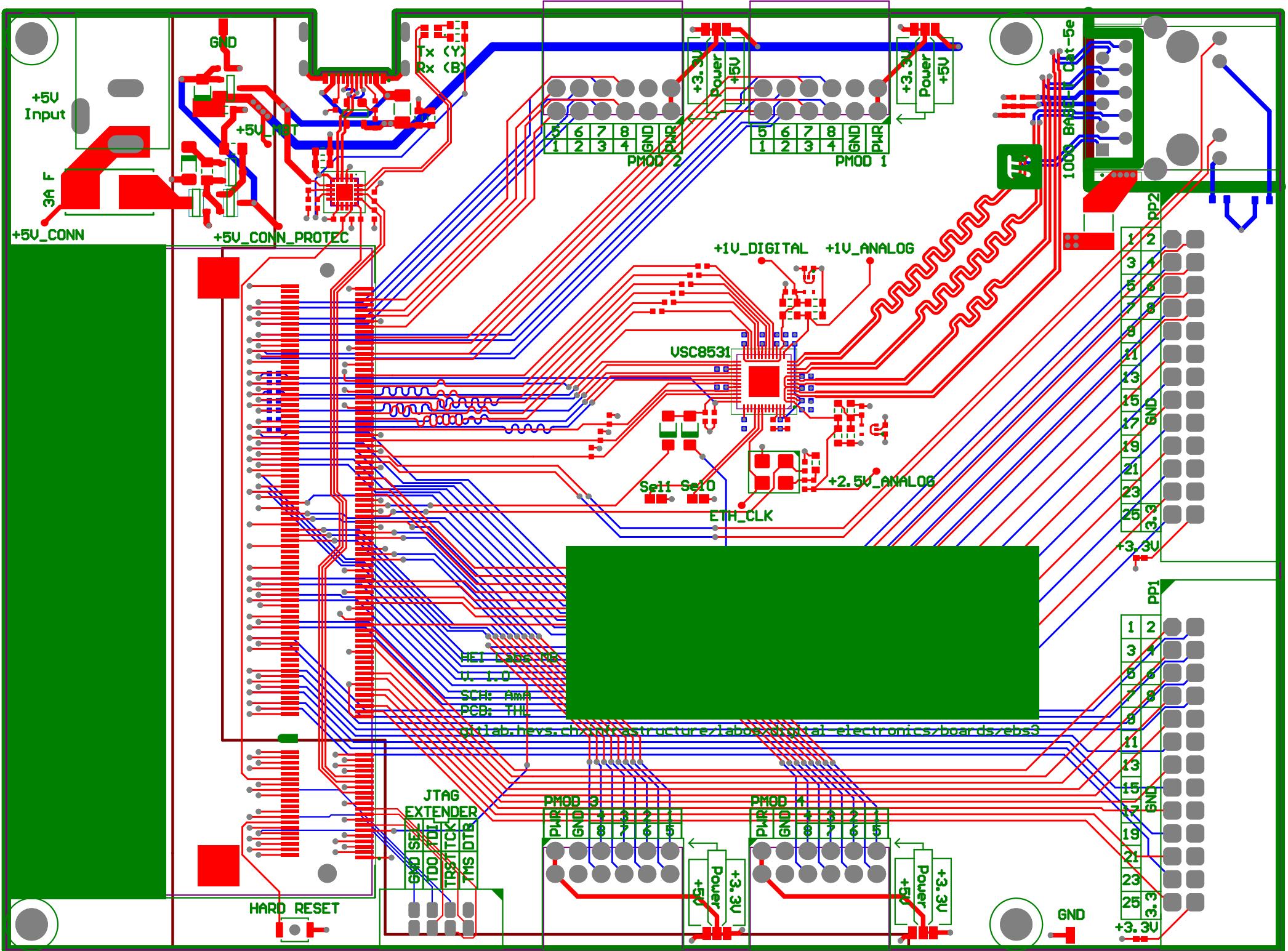
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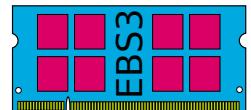
## **II Rooting**



**III BOM**

Name	Description	Designator	Quantity	Footprint
100nF, 6V3	Capacitor	C1, C7, C8, C9, C10, C14, C15, C16, C17, C18, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C33, C34	22	CAPACITOR 1005 REFLOW
4.7uF, 6V3	Capacitor	C2, C4	2	CAPACITOR 1608 REFLOW
100nF, 6V3	Capacitor	C3, C5	2	CAPACITOR 1608 REFLOW
1uF, 6V3	Capacitor	C6, C11, C19, C36	4	CAPACITOR 1608 REFLOW
10uF, 6V3	Capacitor	C12, C13, C20, C21	4	CAPACITOR 1608 REFLOW
1nF, 3kV	Capacitor	C32	1	CAPACITOR 4532 REFLOW
10nF, 6V3	Capacitor	C35	1	CAPACITOR 1005 REFLOW
CM1293A-02SR	ESD Protection Array 2 Channels	D1	1	SOT143 P1.9 C1.4X3.0 H1.1
SS310LW	Diode Schottky generic 2 Leads	D2	1	DIODE SOD123-FL REFLOW
TZMC4V7-GS18	Diode zener generic	D3	1	DIODE MINI MELF DO213AA
BAT54W-HG3-08	Diode Schottky generic 2 Leads	D4, D5	2	DIODE SOD123-FL REFLOW
0154003.DR	LittleFuse series 0154 C10X5.0 H3.8	F1	1	LittleFuse series 0154 C10X5.0 H3.8
MH3261-601Y	Inductor	FB1	1	INDUCTOR 3216 REFLOW
MH1608-800Y	Inductor	FB2, FB3	2	INDUCTOR 1608 REFLOW
USB4520-03-0-A	Connector	J1	1	USB-C-SMD GCT USB452003A
DC10B	DC Power Connector Cliff DC10B	J2	1	DC10B CLIFF
PPTC062LJBN-RC	Right angle 2x6 female socket	J3, J4, J5, J6	4	Socket2X6 P2.54 RIGHT ANGLE
302-R261	FlatCable2x13	J7, J8	2	FlatCable2x13 2.54MM RIGHT ANGLE TH
CRJ009-ML4-TH	RJ45, 8P10C, 10/100/1000 BASE-T socket with LEDs	J9	1	RJ45 CRJ009-ML4-TH
1717254-1	DDR1 & DDR2 SODIMM Socket, Standard pinout for Hevs in house use	J10	1	SO-DIMM TE 1473149-1
98414-G06-08ULF	FlatCable2x4	J11	1	FlatCable2x4 2MM Straight TH FCI 98414-G06-08ULF
Copper	JUMPER 2 POS	JP7, JP8	2	JUMPER2 SMD 1608
LTST-C195TBKSKT-5A	Standard-LEDs - SMD SMD LED Bi-Color Blue 45/Yellow 70mcd	LD1	1	LED LiteOn LTST-C195 series
M3 Screw	Screw Hex Socket Unconnected BN610	M1, M2, M3, M4	4	Screw Hex Socket M3X5 Unconnected
5k1	Resistor	R1, R2	2	RESISTOR 1005 REFLOW
10k	Resistor	R3, R4, R10, R11, R13, R23, R28, R30, R31	9	RESISTOR 1005 REFLOW
22k	Resistor	R5	1	RESISTOR 1005 REFLOW
220	Resistor	R6	1	RESISTOR 1608 REFLOW
22	Resistor	R7	1	RESISTOR 1608 REFLOW
1k	Resistor	R8	1	RESISTOR 1005 REFLOW
47k	Resistor	R9	1	RESISTOR 1005 REFLOW
3k9	Resistor	R12	1	RESISTOR 2012 REFLOW
10k	Resistor	R14	1	RESISTOR 2012 REFLOW
4k7	Resistor	R15, R17	2	RESISTOR 1005 REFLOW
2k	Resistor	R16, R27	2	RESISTOR 1005 REFLOW
270	Resistor	R18, R19	2	RESISTOR 1608 REFLOW
39	Resistor	R20, R21, R22, R24, R25, R26, R32, R33, R34, R35, R36, R37, R38	13	RESISTOR 1005 REFLOW
22	Resistor	R29	1	RESISTOR 1005 REFLOW
B3U-1000PM-B	Push Button, 2 pins	S1	1	Push Button C.2.5X3.0 OMRON B3U-1000P(M)-B
SI3407-TP	Generic MOS-P	T1, T2, T4	3	SOT23 P0.95 C1.6x3.0 H1.3
PMV50XPR	Generic MOS-P	T3	1	SOT23 P0.95 C1.6x3.0 H1.3
S2761-46R	Test Point	TP1, TP2	2	Test Point HARWIN S2761-46R
CP2102N-A02-GQFN20R	Integrated Circuit	U1	1	CP2102NA02GQFN20
TCR2EE25,LM_CT	200 mA CMOS Low Dropout Regulator with Fast Load Transient Response	U2	1	SOT553 P0.5 C1.6x1.2 H0.55
VSC8531XMW-02	Integrated Circuit	U3	1	QFN40P600X600X90-49N-D
TCR2EE10,LM_CT	200 mA CMOS Low Dropout Regulator with Fast Load Transient Response	U4	1	SOT553 P0.5 C1.6x1.2 H0.55
ECS-5032MV-1250-CNT	Oscillator C5.0x3.2 Abracon ASFL1	X1	1	Oscillator C5.0x3.2 Abracon ASFL1

## **IV Constraints file**



```

### For reference, see TN1262 / FPGA-TN-02032
# .lpf file format is not really documented by Lattice, normally generated through Diamond

#####
#### sysCONFIG
#####

# The BLOCK commands disable tracing of paths within clock domains (impacting overall
#   ↳ timing score)
# It can also be used on paths if the TRACE should not consider the clock domain crossing
#   like : BLOCK PATH FROM CLKNET "CLK_A" TO CLKNET "CLK_B" ;
BLOCK RESETPATHS ;
BLOCK ASYNCPATHS ;
BLOCK JTAGPATHS ;

# Not comprehensive
# dflt : CONFIG_IOVOLTAGE      1.2, 1.5, 1.8, 2.5(dflt), 3.3          voltage is 3.3V
# dflt : COMPRESS_CONFIG        OFF (dflt), ON                           no bitstream compression
# mod  : MCCLK_FREQ             2.4, 4.8, 9.7, 19.4, 38.8, 62           NOR program read @ 62MHz
# mod  : MASTER_SPI_PORT        DISABLE (dflt), ENABLE                  master SPI port stays SPI and
#   ↳ not GPIOs, other mods disabled by dflt
# dflt : BACKGROUND_RECONFIG   -                                         no soft ERC when hot-loading
#   ↳ bitstream (due to cosmic rays)
# dflt : DONE_PULL              ON (dflt), OFF                         IPU on DONE pin
# dflt : DONE_EX                OFF (dflt), ON                         not delaying end of the
#   ↳ configuration (used for daisy chaining FPGAs)
# mod  : DONE_OD                OFF (dflt), ON                         DONE pin as open-drain
#   ↳ instead of push-pull
# dflt : CONFIG_SECURE          OFF (dflt), ON                         allows external access to
#   ↳ current program
# mod  : CONFIG_MODE            JTAG (dflt), SSPI, SPI_SERIAL, SPI_DUAL, SPI_QUAD,
#   ↳ SLAVE_PARALLEL, SLAVE_SERIAL                                     which bus and mode is used to
#   ↳ load configuration (for the Lattice IDE)
# dflt : TRANSFR                OFF (dflt), ON                         if using TransFR tool from
#   ↳ Lattice
# dflt : WAKE_UP                4 (set DONE=1 before starting user code, dflt for
#   ↳ DONE_EX=ON)
#   ↳ 21 (set DONE=1 once FPGA is already running user code, dflt
#   ↳ for DONE_EX=OFF)
# mod  : INBUF                  ON, OFF                                disable unused input buffers
#   ↳ (not sure it impacts the ECP5 family)
SYSCONFIG MCCLK_FREQ=62 MASTER_SPI_PORT=ENABLE DONE_OD=ON CONFIG_MODE=SPI_QUAD INBUF=OFF
#   ↳ CONFIG_IOVOLTAGE=3.3 ;
IOBUF ALLPORTS IO_TYPE=LVCMOS33 ;
#SYSCONFIG MCCLK_FREQ=62 MASTER_SPI_PORT=ENABLE DONE_OD=ON CONFIG_MODE=SPI_QUAD INBUF=OFF
#   ↳ CONFIG_IOVOLTAGE=3.3 ;
#IOBUF ALLPORTS IO_TYPE=LVCMOS33 ;

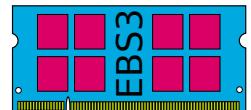
#####
#### Labs DB
#####

### Clock and reset ###
#INPUT_SETUP ALLPORTS 50.000000 ns HOLD 10.000000 ns CLKPORT "CLK" ;
#INPUT_SETUP PORT "nRST" 50.000000 ns CLKPORT "CLK" ;

FREQUENCY PORT "CLK" 100.000000 MHz ;
LOCATE COMP "CLK" SITE "K16" ;
IOBUF PORT "CLK" PULLMODE=None ;

LOCATE COMP "nRST" SITE "E13" ;
GSR_NET net "resetSynch_n" ;

```



```

### LEDs ###
LOCATE COMP "LED_nR" SITE "T14" ;
LOCATE COMP "LED_nG" SITE "R14" ;
LOCATE COMP "LED_nB" SITE "T15" ;

### USB (FTDI2232HL located on the daughterboard) ###
LOCATE COMP "USB_DB_TX" SITE "A14" ;
IOBUF PORT "USB_DB_TX" SLEWRATE=FAST ;
LOCATE COMP "USB_DB_RX" SITE "B14" ;
IOBUF PORT "USB_DB_RX" PULLMODE=UP ;
LOCATE COMP "USB_DB_RTS" SITE "B13" ;
IOBUF PORT "USB_DB_RTS" SLEWRATE=FAST ;
LOCATE COMP "USB_DB_CTS" SITE "C13" ;
IOBUF PORT "USB_DB_CTS" PULLMODE=UP ;

### SD Flash (External SD card) ###
LOCATE COMP "SD_DETECT" SITE "G12" ;
IOBUF PORT "SD_DETECT" PULLMODE=UP ;

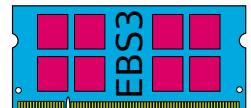
LOCATE COMP "SD_CMD" SITE "C15" ;
IOBUF PORT "SD_CMD" SLEWRATE=FAST ;
LOCATE COMP "SD_CLK" SITE "B15" ;
IOBUF PORT "SD_CLK" SLEWRATE=FAST ;

LOCATE COMP "SD_DTA[0]" SITE "B16" ;
#IOBUF PORT "SD_DTA[0]" SLEWRATE=FAST ;
LOCATE COMP "SD_DTA[1]" SITE "C16" ;
#IOBUF PORT "SD_DTA[1]" SLEWRATE=FAST ;
LOCATE COMP "SD_DTA[2]" SITE "F12" ;
#IOBUF PORT "SD_DTA[2]" SLEWRATE=FAST ;
LOCATE COMP "SD_DTA[3]" SITE "C14" ;
#IOBUF PORT "SD_DTA[3]" SLEWRATE=FAST ;

### DRAM ###
LOCATE COMP "DRAM_ADDR[0]" SITE "J15" ;
IOBUF PORT "DRAM_ADDR[0]" SLEWRATE=FAST ;
LOCATE COMP "DRAM_ADDR[1]" SITE "L16" ;
IOBUF PORT "DRAM_ADDR[1]" SLEWRATE=FAST ;
LOCATE COMP "DRAM_ADDR[2]" SITE "L15" ;
IOBUF PORT "DRAM_ADDR[2]" SLEWRATE=FAST ;
LOCATE COMP "DRAM_ADDR[3]" SITE "K15" ;
IOBUF PORT "DRAM_ADDR[3]" SLEWRATE=FAST ;
LOCATE COMP "DRAM_ADDR[4]" SITE "G15" ;
IOBUF PORT "DRAM_ADDR[4]" SLEWRATE=FAST ;
LOCATE COMP "DRAM_ADDR[5]" SITE "F15" ;
IOBUF PORT "DRAM_ADDR[5]" SLEWRATE=FAST ;
LOCATE COMP "DRAM_ADDR[6]" SITE "F16" ;
IOBUF PORT "DRAM_ADDR[6]" SLEWRATE=FAST ;
LOCATE COMP "DRAM_ADDR[7]" SITE "E16" ;
IOBUF PORT "DRAM_ADDR[7]" SLEWRATE=FAST ;
LOCATE COMP "DRAM_ADDR[8]" SITE "E15" ;
IOBUF PORT "DRAM_ADDR[8]" SLEWRATE=FAST ;
LOCATE COMP "DRAM_ADDR[9]" SITE "G13" ;
IOBUF PORT "DRAM_ADDR[9]" SLEWRATE=FAST ;
LOCATE COMP "DRAM_ADDR[10]" SITE "M16" ;
IOBUF PORT "DRAM_ADDR[10]" SLEWRATE=FAST ;
LOCATE COMP "DRAM_ADDR[11]" SITE "F13" ;
IOBUF PORT "DRAM_ADDR[11]" SLEWRATE=FAST ;
LOCATE COMP "DRAM_ADDR[12]" SITE "D16" ;
IOBUF PORT "DRAM_ADDR[12]" SLEWRATE=FAST ;

LOCATE COMP "DRAM_BA[0]" SITE "L14" ;
IOBUF PORT "DRAM_BA[0]" SLEWRATE=FAST ;
LOCATE COMP "DRAM_BA[1]" SITE "L13" ;

```



```

IOBUF PORT "DRAM_BA[1]" SLEWRATE=FAST ;
LOCATE COMP "DRAM_CLK" SITE "G14" ;
IOBUF PORT "DRAM_CLK" SLEWRATE=FAST ;
LOCATE COMP "DRAM_CKE" SITE "G16" ;
IOBUF PORT "DRAM_CKE" SLEWRATE=FAST ;
LOCATE COMP "DRAM_nRAS" SITE "M14" ;
IOBUF PORT "DRAM_nRAS" SLEWRATE=FAST ;
LOCATE COMP "DRAM_nCAS" SITE "K13" ;
IOBUF PORT "DRAM_nCAS" SLEWRATE=FAST ;
LOCATE COMP "DRAM_nWE" SITE "N16" ;
IOBUF PORT "DRAM_nWE" SLEWRATE=FAST ;
LOCATE COMP "DRAM_nCS" SITE "M15" ;

LOCATE COMP "DRAM_DQ[0]" SITE "P14" ;
LOCATE COMP "DRAM_DQ[1]" SITE "R15" ;
LOCATE COMP "DRAM_DQ[2]" SITE "N14" ;
LOCATE COMP "DRAM_DQ[3]" SITE "R16" ;
LOCATE COMP "DRAM_DQ[4]" SITE "J14" ;
LOCATE COMP "DRAM_DQ[5]" SITE "P15" ;
LOCATE COMP "DRAM_DQ[6]" SITE "K14" ;
LOCATE COMP "DRAM_DQ[7]" SITE "P16" ;
LOCATE COMP "DRAM_DQ[8]" SITE "D14" ;
LOCATE COMP "DRAM_DQ[9]" SITE "H14" ;
LOCATE COMP "DRAM_DQ[10]" SITE "H12" ;
LOCATE COMP "DRAM_DQ[11]" SITE "H13" ;
LOCATE COMP "DRAM_DQ[12]" SITE "E14" ;
LOCATE COMP "DRAM_DQ[13]" SITE "H15" ;
LOCATE COMP "DRAM_DQ[14]" SITE "J13" ;
LOCATE COMP "DRAM_DQ[15]" SITE "J16" ;

LOCATE COMP "DRAM_DQM[0]" SITE "M13" ;
IOBUF PORT "DRAM_DQM[0]" SLEWRATE=FAST ;
LOCATE COMP "DRAM_DQM[1]" SITE "F14" ;
IOBUF PORT "DRAM_DQM[1]" SLEWRATE=FAST ;

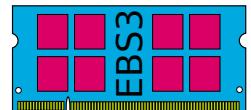
#####
#### SODIMM-200
#####

### USB (chip located on the motherboard) ###
LOCATE COMP "USB_MB_TX" SITE "M11" ;
IOBUF PORT "USB_MB_TX" SLEWRATE=FAST ;
LOCATE COMP "USB_MB_RX" SITE "N12" ;
IOBUF PORT "USB_MB_RX" PULLMODE=UP ;
LOCATE COMP "USB_MB RTS" SITE "N11" ;
IOBUF PORT "USB_MB RTS" SLEWRATE=FAST ;
LOCATE COMP "USB_MB CTS" SITE "M12" ;
IOBUF PORT "USB_MB CTS" PULLMODE=UP ;

### PMOD1 ###
LOCATE COMP "PMOD1[1]" SITE "P1" ;
LOCATE COMP "PMOD1[2]" SITE "N4" ;
LOCATE COMP "PMOD1[3]" SITE "P2" ;
LOCATE COMP "PMOD1[4]" SITE "P5" ;
LOCATE COMP "PMOD1[5]" SITE "R1" ;
LOCATE COMP "PMOD1[6]" SITE "N5" ;
LOCATE COMP "PMOD1[7]" SITE "R2" ;
LOCATE COMP "PMOD1[8]" SITE "N6" ;

### PMOD2 ###
LOCATE COMP "PMOD2[1]" SITE "R3" ;
LOCATE COMP "PMOD2[2]" SITE "P11" ;
LOCATE COMP "PMOD2[3]" SITE "P12" ;
LOCATE COMP "PMOD2[4]" SITE "T3" ;

```



```

LOCATE COMP "PMOD2[5]" SITE "R4" ;
LOCATE COMP "PMOD2[6]" SITE "R12" ;
LOCATE COMP "PMOD2[7]" SITE "T13" ;
LOCATE COMP "PMOD2[8]" SITE "R5" ;

### PMOD3 ####
LOCATE COMP "PMOD3[1]" SITE "B2" ;
LOCATE COMP "PMOD3[2]" SITE "B3" ;
LOCATE COMP "PMOD3[3]" SITE "A4" ;
LOCATE COMP "PMOD3[4]" SITE "D4" ;
LOCATE COMP "PMOD3[5]" SITE "A2" ;
LOCATE COMP "PMOD3[6]" SITE "B4" ;
LOCATE COMP "PMOD3[7]" SITE "C3" ;
LOCATE COMP "PMOD3[8]" SITE "C4" ;

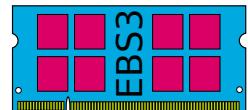
### PMOD4 ####
LOCATE COMP "PMOD4[1]" SITE "J4" ;
LOCATE COMP "PMOD4[2]" SITE "J5" ;
LOCATE COMP "PMOD4[3]" SITE "H4" ;
LOCATE COMP "PMOD4[4]" SITE "E4" ;
LOCATE COMP "PMOD4[5]" SITE "J3" ;
LOCATE COMP "PMOD4[6]" SITE "H3" ;
LOCATE COMP "PMOD4[7]" SITE "E3" ;
LOCATE COMP "PMOD4[8]" SITE "D3" ;

### PP1 ####
LOCATE COMP "PP1[1]" SITE "A9" ;
LOCATE COMP "PP1[2]" SITE "D10" ;
LOCATE COMP "PP1[3]" SITE "A10" ;
LOCATE COMP "PP1[4]" SITE "C10" ;
LOCATE COMP "PP1[5]" SITE "B10" ;
LOCATE COMP "PP1[6]" SITE "C12" ;
LOCATE COMP "PP1[7]" SITE "B12" ;
LOCATE COMP "PP1[8]" SITE "D13" ;
LOCATE COMP "PP1[9]" SITE "A13" ;
LOCATE COMP "PP1[10]" SITE "M5" ; # PP1 11
LOCATE COMP "PP1[11]" SITE "L5" ; # PP1 13
LOCATE COMP "PP1[12]" SITE "K5" ; # PP1 15
LOCATE COMP "PP1[13]" SITE "H5" ; # PP1 17
LOCATE COMP "PP1[14]" SITE "E8" ; # PP1 19
LOCATE COMP "PP1[15]" SITE "E5" ; # PP1 21
LOCATE COMP "PP1[16]" SITE "E6" ; # PP1 23
LOCATE COMP "PP1[17]" SITE "E7" ; # PP1 25

### PP2 ####
LOCATE COMP "PP2[1]" SITE "G3" ;
LOCATE COMP "PP2[2]" SITE "E1" ;
LOCATE COMP "PP2[3]" SITE "F3" ;
LOCATE COMP "PP2[4]" SITE "D1" ;
LOCATE COMP "PP2[5]" SITE "F4" ;
LOCATE COMP "PP2[6]" SITE "C1" ;
LOCATE COMP "PP2[7]" SITE "D7" ;
LOCATE COMP "PP2[8]" SITE "B6" ;
LOCATE COMP "PP2[9]" SITE "C7" ;
LOCATE COMP "PP2[10]" SITE "A6" ; # PP2 11
LOCATE COMP "PP2[11]" SITE "D8" ; # PP2 13
LOCATE COMP "PP2[12]" SITE "B7" ; # PP2 15
LOCATE COMP "PP2[13]" SITE "C8" ; # PP2 17
LOCATE COMP "PP2[14]" SITE "A7" ; # PP2 19
LOCATE COMP "PP2[15]" SITE "E9" ; # PP2 21
LOCATE COMP "PP2[16]" SITE "A8" ; # PP2 23
LOCATE COMP "PP2[17]" SITE "D9" ; # PP2 25

### Ethernet ####

```



```

LOCATE COMP "ETH_CLK_EN" SITE "B1" ;
LOCATE COMP "ETH_nRESET" SITE "C2" ;

LOCATE COMP "ETH_nLED_Y" SITE "F1" ;
LOCATE COMP "ETH_nLED_G" SITE "G2" ;

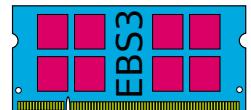
LOCATE COMP "ETH_MDC" SITE "J1" ;
LOCATE COMP "ETH_MDIO" SITE "H2" ;
IOBUF PORT "ETH_MDIO" OPENDRAIN=ON SLEWRATE=FAST ;
LOCATE COMP "ETH_MDINT" SITE "G1" ;
IOBUF PORT "ETH_MDINT" SLEWRATE=FAST ;

LOCATE COMP "ETH_REF_CLK" SITE "P3" ;
LOCATE COMP "ETH_TX_CLK" SITE "M4" ;
IOBUF PORT "ETH_TX_CLK" SLEWRATE=FAST ;
LOCATE COMP "ETH_TX_CTL" SITE "N3" ;
IOBUF PORT "ETH_TX_CTL" SLEWRATE=FAST ;
LOCATE COMP "ETH_TXD[0]" SITE "M3" ;
IOBUF PORT "ETH_TXD[0]" SLEWRATE=FAST ;
LOCATE COMP "ETH_TXD[1]" SITE "L4" ;
IOBUF PORT "ETH_TXD[1]" SLEWRATE=FAST ;
LOCATE COMP "ETH_TXD[2]" SITE "K4" ;
IOBUF PORT "ETH_TXD[2]" SLEWRATE=FAST ;
LOCATE COMP "ETH_TXD[3]" SITE "K3" ;
IOBUF PORT "ETH_TXD[3]" SLEWRATE=FAST ;

LOCATE COMP "ETH_RX_CLK" SITE "K1" ;
LOCATE COMP "ETH_RX_CTL" SITE "K2" ;
LOCATE COMP "ETH_RXD[0]" SITE "L1" ;
LOCATE COMP "ETH_RXD[1]" SITE "L2" ;
LOCATE COMP "ETH_RXD[2]" SITE "M1" ;
LOCATE COMP "ETH_RXD[3]" SITE "M2" ;

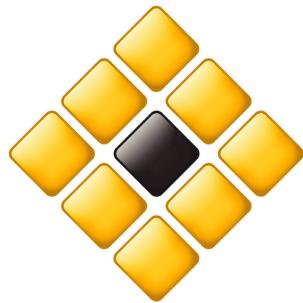
### Extras ###
LOCATE COMP "EXT[1]" SITE "P13" ;
LOCATE COMP "EXT[2]" SITE "R13" ;
LOCATE COMP "EXT[3]" SITE "A3" ;
LOCATE COMP "EXT[4]" SITE "A5" ;
LOCATE COMP "EXT[5]" SITE "B5" ;
LOCATE COMP "EXT[6]" SITE "C5" ;
LOCATE COMP "EXT[7]" SITE "C6" ;
LOCATE COMP "EXT[8]" SITE "D5" ;
LOCATE COMP "EXT[9]" SITE "D6" ;
LOCATE COMP "EXT[10]" SITE "A11" ;
LOCATE COMP "EXT[11]" SITE "A12" ;
LOCATE COMP "EXT[12]" SITE "B8" ;
LOCATE COMP "EXT[13]" SITE "B9" ;
LOCATE COMP "EXT[14]" SITE "B11" ;
LOCATE COMP "EXT[15]" SITE "C9" ;
LOCATE COMP "EXT[16]" SITE "C11" ;
LOCATE COMP "EXT[17]" SITE "D11" ;
LOCATE COMP "EXT[18]" SITE "D12" ;
LOCATE COMP "EXT[19]" SITE "E10" ;
LOCATE COMP "EXT[20]" SITE "E11" ;
LOCATE COMP "EXT[21]" SITE "E12" ;
LOCATE COMP "EXT[22]" SITE "L3" ;
LOCATE COMP "EXT[23]" SITE "M6" ;
LOCATE COMP "EXT[24]" SITE "N1" ;
LOCATE COMP "EXT[25]" SITE "P4" ;
LOCATE COMP "EXT[26]" SITE "P6" ;
LOCATE COMP "EXT[27]" SITE "T2" ;
LOCATE COMP "EXT[28]" SITE "T4" ;
LOCATE COMP "EXT[29]" SITE "E2" ;
LOCATE COMP "EXT[30]" SITE "F2" ;
LOCATE COMP "EXT[31]" SITE "F5" ;
LOCATE COMP "EXT[32]" SITE "G4" ;

```



```
LOCATE COMP "EXT[33]" SITE "G5" ;  
LOCATE COMP "EXT[34]" SITE "J2" ;
```





**LATTICE  
DIAMOND**  
DESIGN SOFTWARE

## Diamond (Lattice)

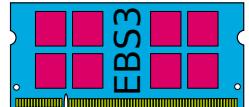
**Hes·so** // VALAIS  
WALLIS

 School of Engineering

Author: [Amand Axel, Silvan Zahno](#)

Date: March 20, 2023

Version: v1.0



## 1 Overview



Lattice Diamond is a design software from Lattice for [FPGAs](#) from the following families:

- CrossLink
- ECP5U
- MachXO3D, MachXO3L, MachXO2, MachXO
- Platform Manager 2
- LatticeXP2
- ECP5UM (subscription license)
- ECP3 (subscription license)

### 1.1 Licensing

Lattice Diamond offers a free license for most of their [FPGA](#) families by requesting a [node-locked license](#) (based on the network interface card (NIC) ID).

Otherwise, a floating license is granted through a node server by connecting to HEI's VPN or locally by using the **secure-hevs** Wi-Fi or an ethernet cable.

The server includes 50 seats.

In order to correctly obtain said license, the server must be added as an environment variable:

- Windows     • Right-click on **Computer** → **Properties** → **Advanced** → **Environment Variables**  
               • Select or add the system variable **LM\_LICENSE\_FILE**  
               • Append it **7788@latticelm.hevs.ch**

- Unix     • Open a shell and type the following:

```
• export LM_LICENSE_FILE=$LM_LICENSE_FILE:7788@latticelm.hevs.ch
```

### 1.2 Version

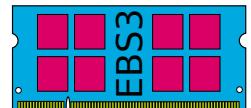
To get a compatible license, Diamond's version must be the v3.12 SP1 (3.12.1.454) which can be downloaded from [Lattice's website](#). Both the base version and the service pack must be installed.

Also select Symplify Pro while installing.

### 1.3 Running Diamond

#### Synthesis

Diamond can be launched as a standalone or from one of its **\*.Idf** project file to complete the synthesis process [2 Synthesis](#).



By using a correctly configured HDL Designer project one can launch Diamond directly from it.

The dedicated HDL tasks are found under the

**Prefs/hds\_user/vXXX/tasks/diamond\_project\_navigator.tsk** folder. Libraries available in the **Libs** folder, pulled from the [DiD-libs](#) repository. Scripts are located in the **Scripts** folder, pulled from the [DiD-scripts](#) repository.

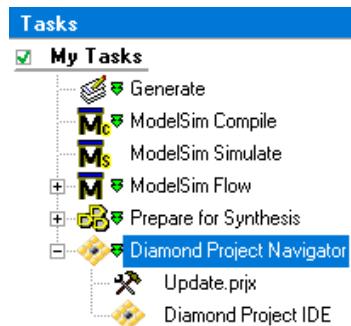


Figure 1: HDL Designer - Diamond shortcut

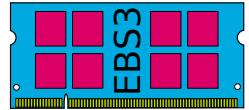


Figure 2: HDL Designer - Update .ldf (left) and Diamond IDE (right) configurations

## Flash

The [FPGA](#)'s flash is done through the DiamondProgrammer software included with Diamond through the generated \*.bit bitfile thanks to the embedded FTDI chip on the daughterboard.

It can be launched as a standalone or directly from within Diamond [3 Flashing](#).



## 2 Synthesis

*Diamond may be very slow to start depending on which hardware is used (not depending on the overall machine power). In such case, removing USB devices before booting it may help.*

### 2.1 Create project

- Launch Diamond
- Click on **File** → **New** → **Project...**
- Give a name and location
- Add the vhdl file to synthesize (when created through HDL Designer, select the **Board/-concat/projectName.vhd** (not the concatenated one)) - do not check the **Copy source** box to keep a link and not a copy of the file
- select the correct chip. Example for the Labs board:
  - **Family** : ECP5U
  - **Device** : LFE5U-25F
  - **Grade** : 6
  - **Package**: CABGA256
  - Gives the par number LFE5U-25F-6BG256C
- Select Synplify Pro assynthesis tool
- Finish

To add the constraints, go to the **File List** tab, right click on **LPF Constraint File** → **Add** → **Existing File**, select the \*.lpf file - do not check the **Copy source** box to keep a link and not a copy of the file.

Right click on the newly added file → **Set as Active Preference File**. The default file can be removed.

### 2.2 Prepare project

The timing constraints are set in the \*.lpf file. To check those, click on the **Spreadsheet View** button (or **Tools** → **Spreadsheet View**).



If modifying settings or pins here, the default file format will not be retained and may be hard for a human to read afterward. Lattice constraints file are not documented and such not user-friendly.

Once open, go to the **Timing Preferences** tab and check the correct clock frequency is detected:



Preference Name	Preference Value	Preference Unit
BLOCK		
FREQUENCY		
PORT "CLK"		
Frequency	100.000000	MHz
Hold Margin	0.000000	ns
PAR_ADJ	0.000000	
Clock Jitter(p-p)	0.000000	ns
PERIOD		
INPUT_SETUP		
CLOCK_TO_OUT		
MULTICYCLE		
MAXDELAY		
CLKSKEWDIFF		
<a href="#">Port Assignments</a> <a href="#">Pin Assignments</a> <a href="#">Clock Resource</a> <a href="#">Route Priority</a>		

Figure 3: Timings check

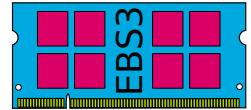
To check pinning, first the file needs to be synthesized and translated by going under the **Process** tab and double clicking **Translate Design**. Then, the **Port Assignments** tab of the **Spreadsheet View** will show found and linked pins:

Name	Group By	Pin	BANK	BANK_VCC	VREF	IO_TYPE	PULLMODE	DRIVE	SLEWRATE	CLAMP	OPENDRAIN	DIFFRESISTOR	DIFFDRIVE	HYSERES
1	All Ports	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
1.1	Input	in1[0]	N/A	N/A	N/A	LVCMS33	DOWN	NA	NA	ON	OFF	OFF	NA	ON
1.1.1		in1[1]	N/A	N/A	N/A	LVCMS33	DOWN	NA	NA	ON	OFF	OFF	NA	ON
1.1.2		in1[2]	N/A	N/A	N/A	LVCMS33	DOWN	NA	NA	ON	OFF	OFF	NA	ON
1.1.3		in1[3]	N/A	N/A	N/A	LVCMS33	DOWN	NA	NA	ON	OFF	OFF	NA	ON
1.1.4		in1[4]	N/A	N/A	N/A	LVCMS33	DOWN	NA	NA	ON	OFF	OFF	NA	ON
1.1.5		in1[5]	N/A	N/A	N/A	LVCMS33	DOWN	NA	NA	ON	OFF	OFF	NA	ON
1.1.6		in1[6]	N/A	N/A	N/A	LVCMS33	DOWN	NA	NA	ON	OFF	OFF	NA	ON
1.1.7		in1[7]	N/A	N/A	N/A	LVCMS33	DOWN	NA	NA	ON	OFF	OFF	NA	ON
1.1.8														
1.2	Output	out1[0]	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
1.2.1		out1[1]	N/A	N/A	N/A	LVCMS33	NONE	8	SLOW	ON	OFF	OFF	NA	NA
1.2.2		out1[2]	N/A	N/A	N/A	LVCMS33	NONE	8	SLOW	ON	OFF	OFF	NA	NA
1.2.3		out1[3]	N/A	N/A	N/A	LVCMS33	NONE	8	SLOW	ON	OFF	OFF	NA	NA
1.2.4		out1[4]	N/A	N/A	N/A	LVCMS33	NONE	8	SLOW	ON	OFF	OFF	NA	NA
1.2.5		out1[5]	N/A	N/A	N/A	LVCMS33	NONE	8	SLOW	ON	OFF	OFF	NA	NA
1.2.6		out1[6]	N/A	N/A	N/A	LVCMS33	NONE	8	SLOW	ON	OFF	OFF	NA	NA
1.2.7		out1[7]	N/A	N/A	N/A	LVCMS33	NONE	8	SLOW	ON	OFF	OFF	NA	NA
1.2.8														

Figure 4: Pins check

A lot of features may be changed from there.

The **Global Preferences** tab shows configurations related to the banks, software load ...but also shows the GSR - Global Set Reset net, which must be the same as the reset signal name in the VHDL file:



Preference Name	Preference Value
Junction Temperature (Tj)(C)	85
Voltage (V)	1.045
SYSTEM_JITTER(ns)	Default
Block Path	
Block Asynchnpaths	ON
Block Resetpaths	ON
Block RD During WR Paths	OFF
Block InterClock Domain Paths	OFF
Block Jitter	OFF
sysConfig	
SLAVE_SPI_PORT	DISABLE
MASTER_SPI_PORT	ENABLE
SLAVE_PARALLEL_PORT	DISABLE
BACKGROUND_RECONFIG	OFF
DONE_EX	OFF
DONE_OD	ON
DONE_PULL	ON
MCCLK_FREQ	62
TRANSFR	OFF
CONFIG_IOVOLTAGE	3.3
CONFIG_SECURE	OFF
WAKE_UP	21
COMPRESS_CONFIG	OFF
CONFIG_MODE	SPI_QUAD
INBUF	OFF
User Code	
UserCode Format	Binary
UserCode	00000000000000000000000000000000
Unique ID	
UniqueId	0000
Derating	
> VCCIO	NOMINAL
Global Set/Reset Net	
resetSynch_n	
Bank VCCIO	
Bank0 (V)	Auto
Bank1 (V)	Auto
Bank2 (V)	Auto
Bank3 (V)	Auto
Bank6 (V)	Auto
Bank7 (V)	Auto
Bank8 (V)	Auto

Figure 5: Global preferences

From the picture, the **FPGA** is set to load its configuration from an external flash chip by accessing it with a QSPI protocol at 62 MHz.

Banks are set to +3.3V.

The target GSR is named **resetSynch\_n**.

### 2.3 Strategy

The strategy changes how the circuit is handled through the various process. Double-click the active strategy (default is **Strategy1**) and change the required settings:

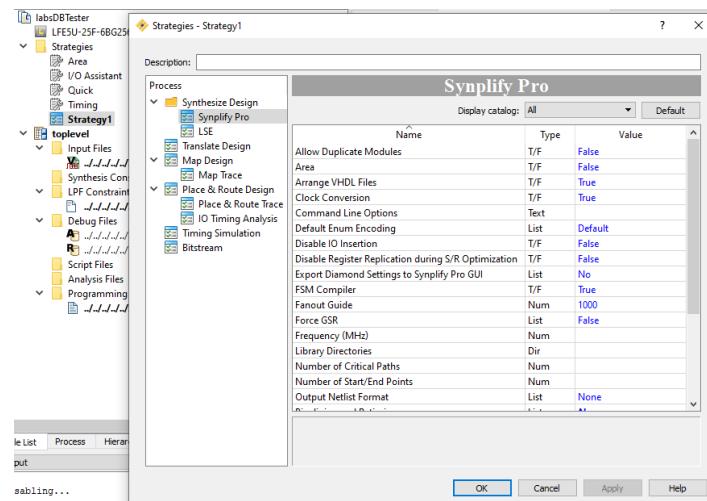
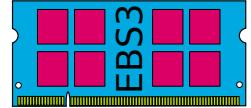


Figure 6: Strategy setup

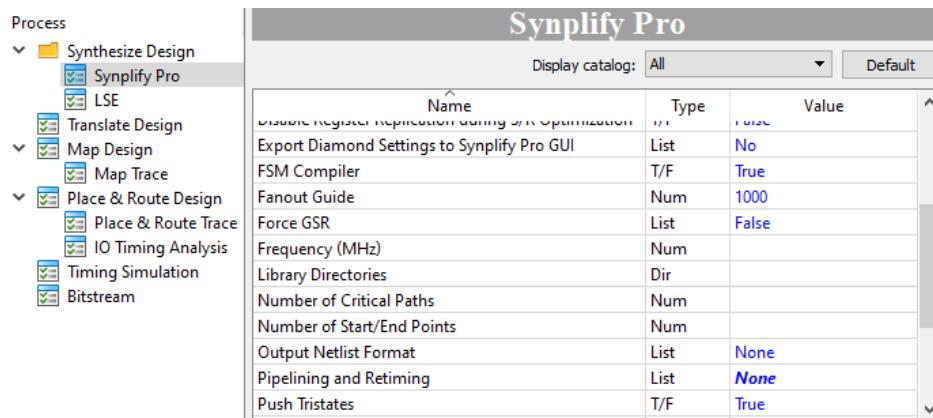
By default, it focuses more on speed than area.

**Pre-defined strategies** A few pre-define strategies are available (right-click on the desired one and **Set As Active Strategy** to use it):

- Area: optimize the area by minimizing the logic gates used. May fail with dense and large designs.
- I/O Assistant: helps to select a legal device pinout and setup I/O buffers.
- Quick: very few optimizations to get a quick overview of the routing results. Helps to identify and debug combinatorial loops, unwanted clocks ...
- Timing: focuses on timing constraints by using high effort level in placement and routing. Slowest strategy.

**Multi-cycle architectures** With default settings, Synplify may add extra registers to cut the longest paths and achieve a better timing closure (referred to as pipelining). The default strategy must be altered for architectures based on multi-cycle processes where synchronism is key.

Under **Synthesize Design → Synplify Pro → Pipelining and Retiming**, set the value to **None**:



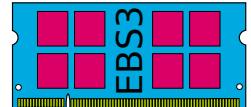


Figure 7: Synplify pipelining

## 2.4 Synthesize

When the project is ready, the VHDL file must be synthesized, compiled and rooted on the chip.

Click on **Place Route Design** under the **Process** tab.

*Pins which appear in the constraints file but not in the design will appear as warning and be discarded. It allows to keep all of them for further implementation.*

The **Output** window on the bottom of Libero can be used to check for errors and warning (both should always be checked). Some parts of the circuit may be pruned, clocks inferred unintentionally, unused signals found ...

In addition, reports can be browsed in the **Report - Design Summary** tab, notably:

- **Process - Map**

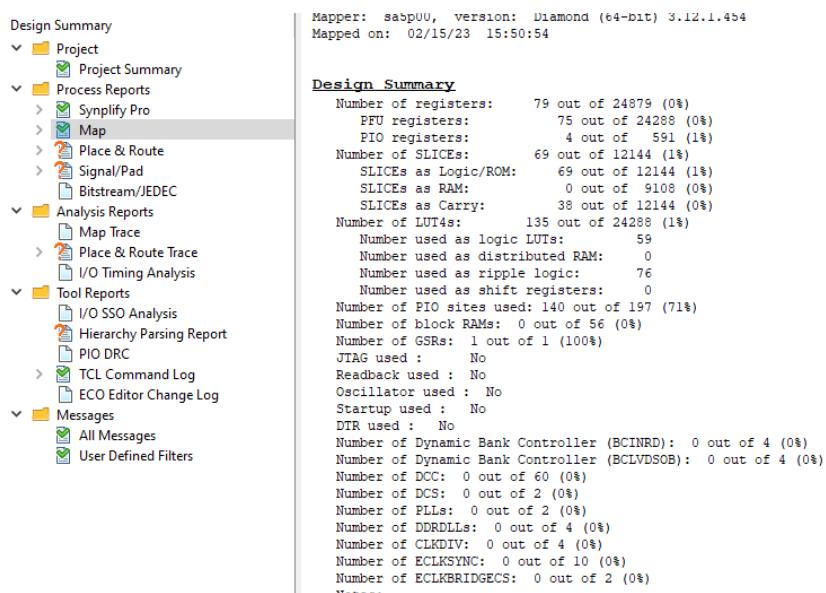


Figure 8: Map report

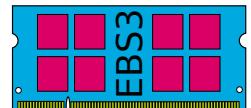
which contains informations on:

- **Design Summary:** used registers, LUTs, BRAMs ...
- **Removed logic:** removed blocks and signals
- **Process - Signal/Pad** shows the pins types and properties summary as well as banks voltages under **PAD Specification File**
- **Analysis Reports - Place Route Trace**
  - **Preference Summary:** targeted clock speed and detected timing errors
  - **Clock Domains Analysis:** detected clocks and domains

## 2.5 Bitfile

If the compilation succeeds, double click on **Bitstream File** to generate a **\*.bit** bitfile.

From there, refer to [3 Flashing](#). Diamond Programmer can be launched directly with a click on



the button **Programmer** or from **Tools → Programmer**.

## 2.6 Hardware debugging

Reveal Inserter is used to create extra debug logic which can be implemented inside the **FPGA** directly and sniffed through the Reveal Analyzer tool. Open it from the Diamond toolbar or in **Tools → Reveal Inserter**.

Under the **Trace Signal Setup** tab, add all required signals to sniff, set the buffer depth and the implementation type (either in BRAM (prefered for placement and timing purposes) or as distributed RAM):

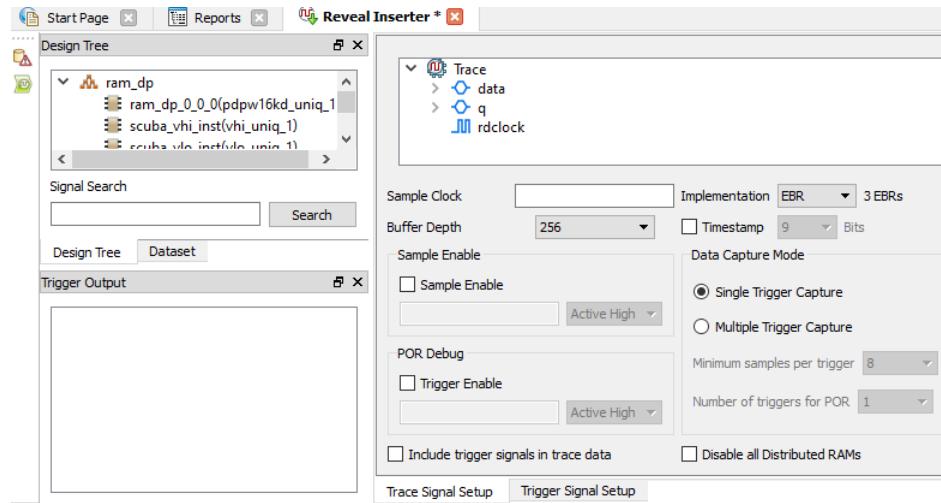


Figure 9: Reveal Inserter - Trace Signal Setup

Under **Sample Clock**, set the clock used to sample the signals internally (better with a higher clock than the one used in the sniffed logic to see transitions).

Under the **Trigger Signal Setup** tab, define the required trigger units (the signal(s) which are used to trigger a potential data transmission) and the trigger expressions (i.e. a composition of triggers, e.g. **myTrigger1** and **myTrigger2**) to detect when the data should be sent to the PC:

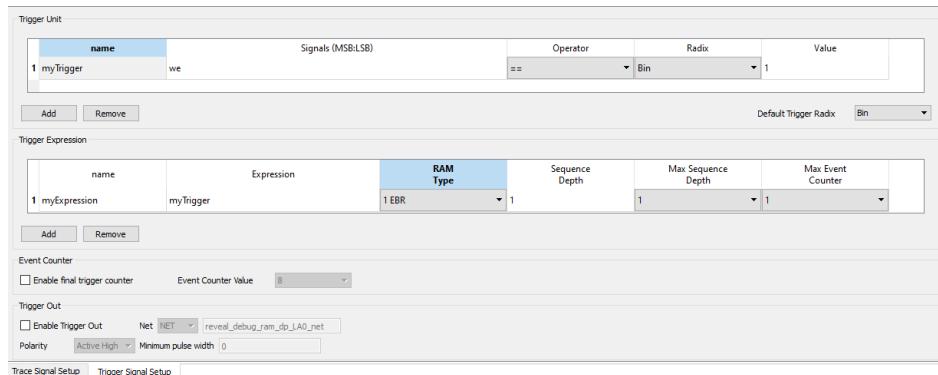


Figure 10: Reveal Inserter - Trigger Signal Setup

Save the project and click on **Insert Debug** to add it to the project. The main file is automatically modified to integrate the new debug logic. When the board is flashed, launch Reveal Analyzer from the toolbar or **Tools → Reveal Analyzer**.

Click on the play button to wait for a trigger (you can also trigger it manually by clicking the



button next to it):

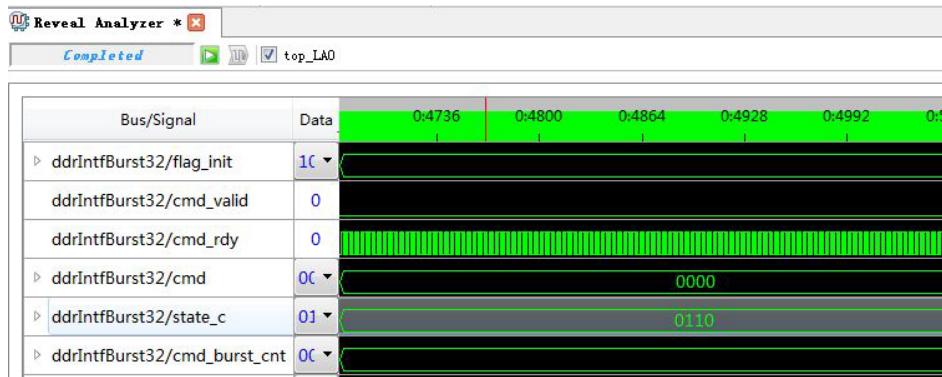


Figure 11: Reveal Analyzer

## 2.7 IP integration

Clarity Designer is the dedicated tool to create IPs from Lattice. Open it as a standalone, from the Diamond toolbar or in **Tools** → **Clarity Designer** and create a new project.

The list of supported IPs is then shown. Choose the desired one, give it a name and customize it as needed:

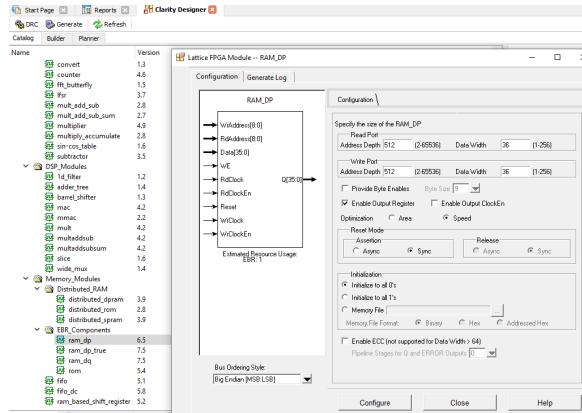


Figure 12: Clarity Designer - RAM dual-port IP

Then click **Configure**. The generated \*.vhd file is available under the projects location.

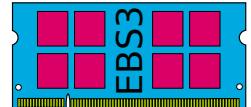
By adding the clarity design to the project (under **Input Files**), the main design may make use of black boxes to adapt itself directly on configurations change without the need to reimport the generated code inside e.g. HDL Designer and synthesizing the whole design again.

The dedicated Diamond libraries must be built to get simulations running with IP cores. For this:

- Launch Diamond
- In the Tcl console, run

```
cmpl_libs -sim_path C:/path/modelsim/win64
           -target_path c:/path/libs_out
           -device ecp5u
           -lang vhdl
```

- Restart Modelsim



### 3 Flashing

#### 3.1 Diamond Programmer

##### Overview

Diamond Programmer is the official tool supported for the [FPGAs](#) listed on [1 Overview](#) and comes with Lattice Diamond (v3.12.1.454 here).

It can also be downloaded as standalone from [Lattice's website](#).

##### Usage

Launch Diamond Programmer directly or from within the Diamond project with a click on the **Programmer** button or from **Tools → Programmer**.

Select **Create a new blank project** (or open a **.xcf** file). On the right, set the cable to **HW-USBN-2B (FTDI)** and use a custom clock divider of **4**.

Click on **Detect cable** while the board is plugged in. Detected FTDI chips are shown. Select the interface A of desired board:

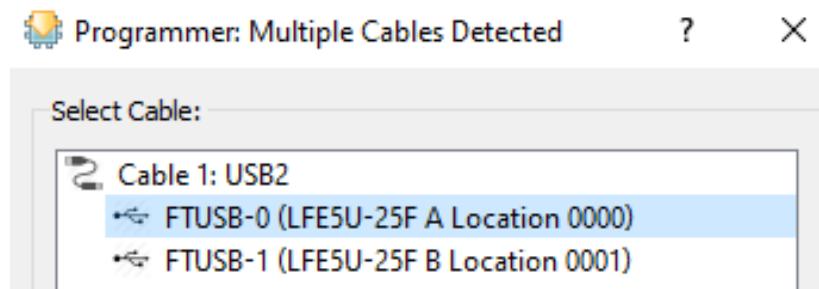


Figure 13: Board detection

It is possible to program the [FPGA](#) through JTAG (will lose the program on power loss) or program the SPI flash in background (program retained).

##### JTAG

Double click on **Operation** and set it as **JTAG 1532 mode** such as:

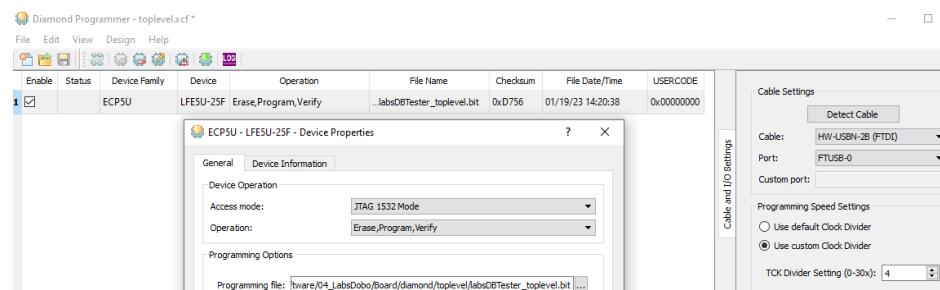
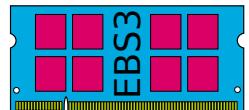


Figure 14: JTAG programming

Then click on the **Program** button. **Status** column is set to **PASS** when the operation is successfully completed.

##### SPI

To support the Renesas AT25SF321B SPI chip installed on the daughterboard, modify the programmer files as:



- Download files from [Gitlab](#)
- Follow the path given in folder **diamond** to replace the file **ispVM\_008.xdf** in the Diamond installation **diamondInstallPath/lscd/diamond/3.12/data/vmdata/database/flash** (if using the standalone programmer, the path is under **programmerStandalonePath/data/vmdata/database/flash**)
- If already launched, restart Diamond (Programmer)

See appendix [I Diamond ispVM\\_008.xdf file modification](#) for the beginning of the **ispVM\_008.xdf file**. Only the `<Device name="AT25SF321B">` part is required to be added to the base file.

Double click on **Operation** and set it as **SPI Flash Background Programming** such as:

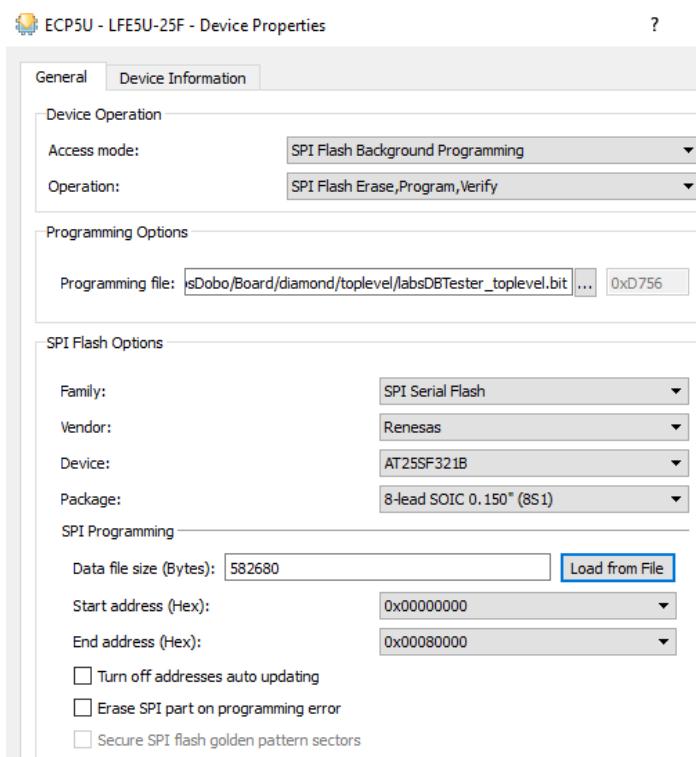


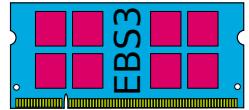
Figure 15: SPI programming

For the **Data file size**, click on **Load from file** to automatically set it.

Then click on the **Program** button. **Status** column is set to **PASS** when the operation is successfully completed.

The new program is loaded only when the soft (software) reset button is pressed.

# I Diamond ispVM\_008.xdf file modification



```

<?xml version='1.0' encoding='utf-8' ?>
<!DOCTYPE ispXDF SYSTEM "IspXDF.dtd" >
<ispXDF version="15.0">
    <Comment>FLASH technology Devices List</Comment>
    <Family name="SPI Serial Flash">

        <!-- Custom chips -->
        <Device name="AT25SF321B">
            <Comm> JTAG </Comm>
            <Vendor> Renesas </Vendor>
            <CodeName> AT25SF321B </CodeName>
            <FullName> AT25SF321B </FullName>
            <AlgoTemplate>ATMEL_AT26_Algo.svp</AlgoTemplate>
            <JtagID>0x87</JtagID>
            <IspID>0x1F</IspID>
            <IDMask>0x000000FF</IDMask>
            <TotalFuses> 32 </TotalFuses> <!-- Mib size -->
            <Address_range> ;0x000000;0x010000;0x020000;0x030000;
                0x040000;0x050000;0x060000;0x070000;0x080000;0x090000;
                0x0A0000;0x0B0000;0x0C0000;0x0D0000;0x0E0000;0x0F0000;
                0x100000;0x110000;0x120000;0x130000;0x140000;0x150000;
                0x160000;0x170000;0x180000;0x190000;0x1A0000;0x1B0000;
                0x1C0000;0x1D0000;0x1E0000;0x1F0000;0x200000;0x210000;
                0x220000;0x230000;0x240000;0x250000;0x260000;0x270000;
                0x280000;0x290000;0x2A0000;0x2B0000;0x2C0000;0x2D0000;
                0x2E0000;0x2F0000;0x300000;0x310000;0x320000;0x330000;
                0x340000;0x350000;0x360000;0x370000;0x380000;0x390000;
                0x3A0000;0x3B0000;0x3C0000;0x3D0000;0x3E0000;0x3F0000;
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                <PON> AT25SF321B-SSHB </PON>
            </Package>
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                <Type> 8-lead SOIC 0.208" (8S2) </Type>
                <PON> AT25SF321B-SHB </PON>
            </Package>
            <Package>
                <Type> 8-pad UDFN (8MA1) </Type>
                <PON> AT25SF321B-MHB </PON>
            </Package>
        </Device>

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            <Vendor> Adesto </Vendor>
            <CodeName> AT25SF128</CodeName>
        ...
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    </Family>
</ispXDF>

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