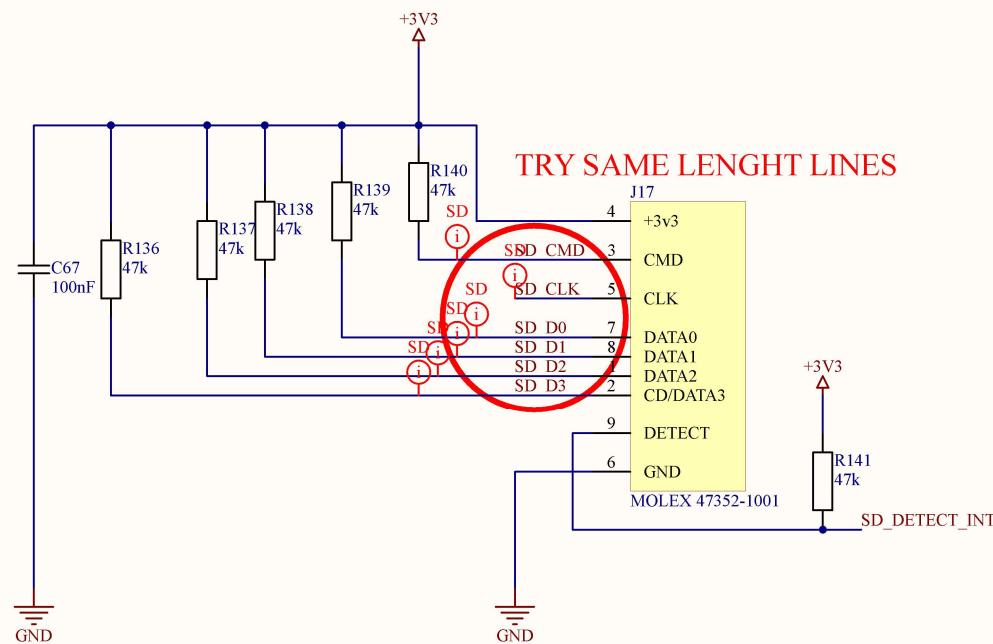


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BalEv.PrjPcb

Hes-SO // VALAIS WALLIS

Date : 17.01.2022



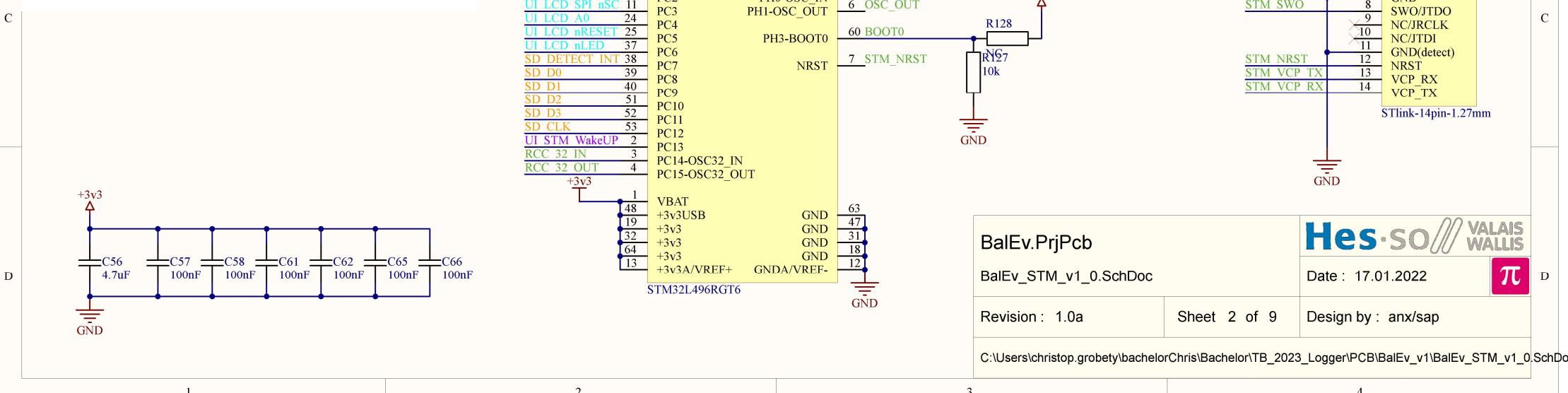
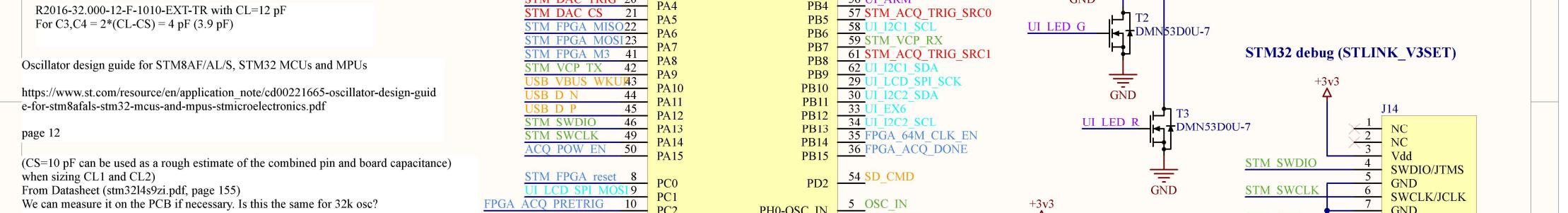
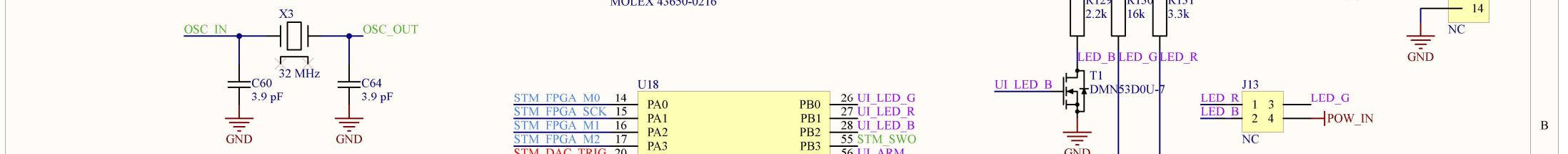
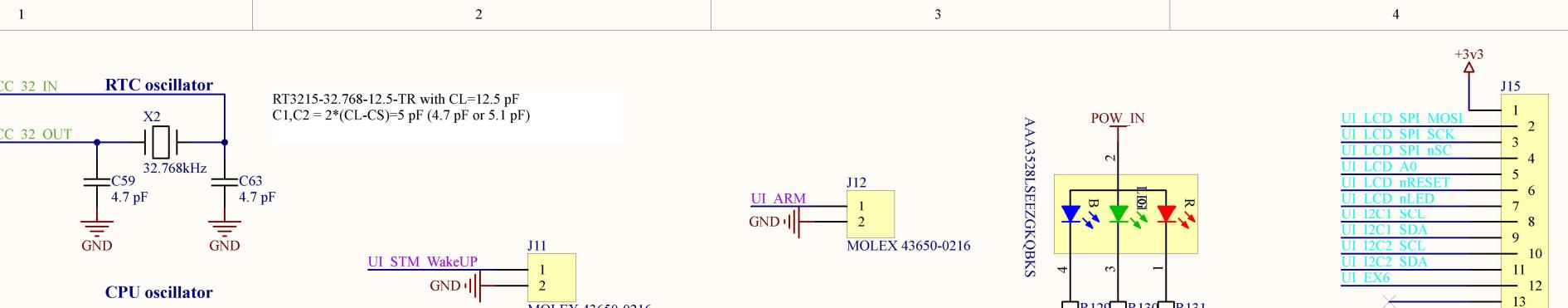
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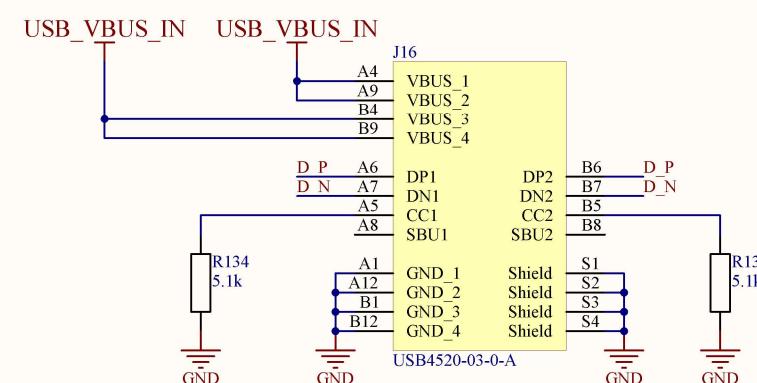
Revision : 1.0a

Sheet 1 of 9

Design by : anx/sap

C:\Users\christop.grobety\bachelorChris\Bachelor\TB_2023_Logger\PCB\BalEv_v1\BalEv_SD_card_v1_0.SchDoc





BalEv.PrjPcb

BalEv_USB_v1_0.SchDoc

Hes-SO // VALAIS WALLIS

Date : 17.01.2022

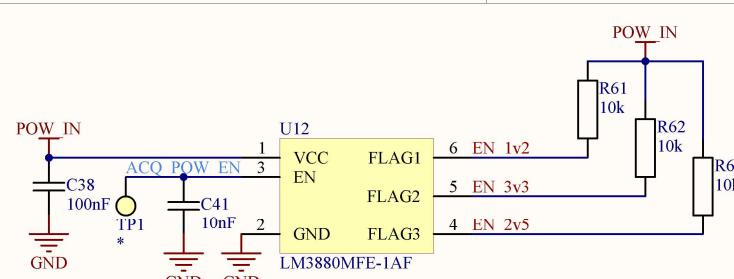


Revision : 1.0a

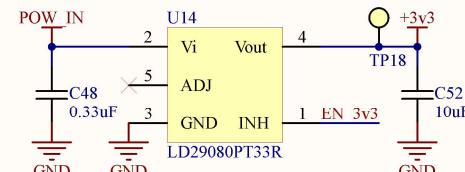
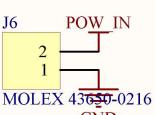
Sheet 3 of 9

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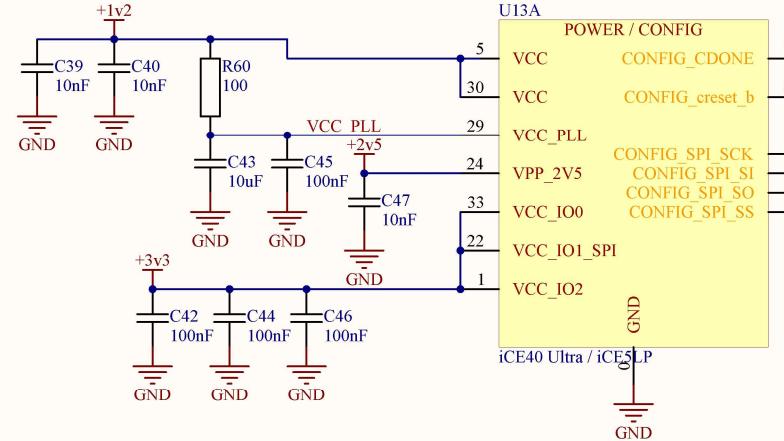
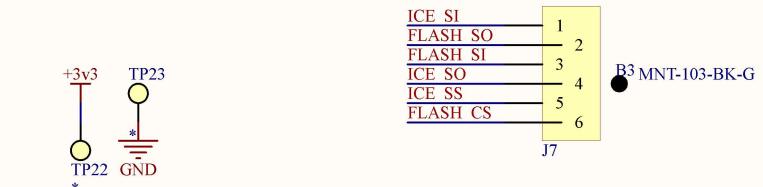
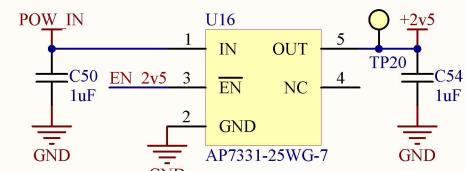
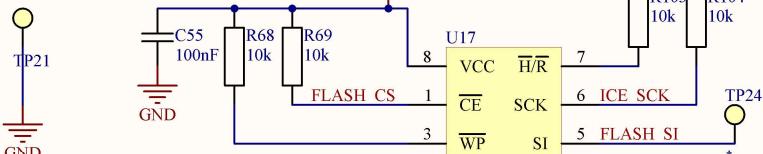
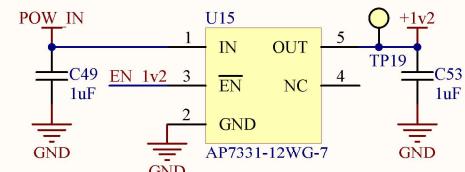
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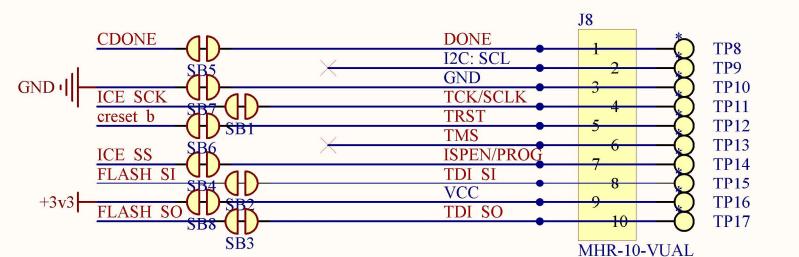
Connection towards processor cut on enable pin!!



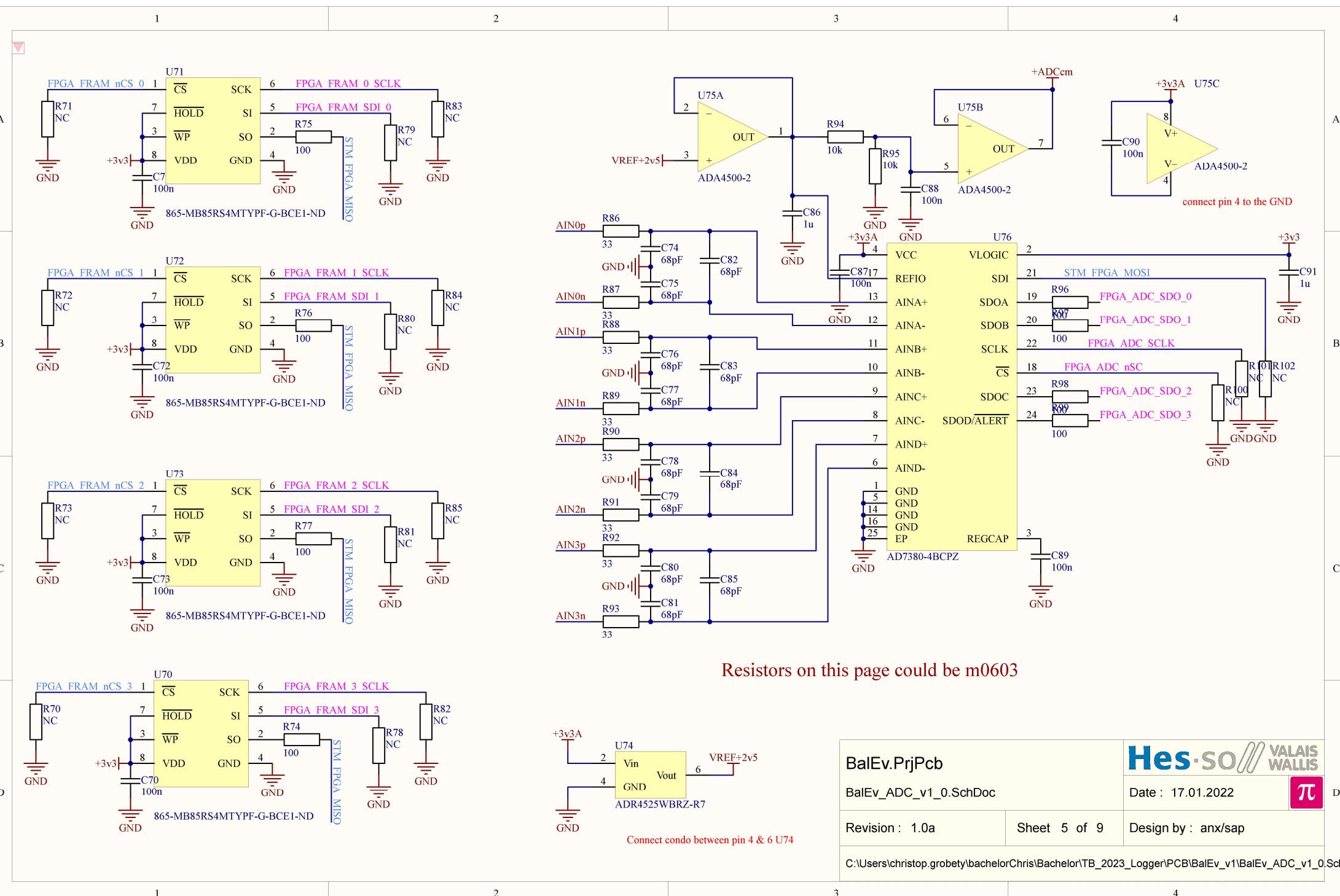
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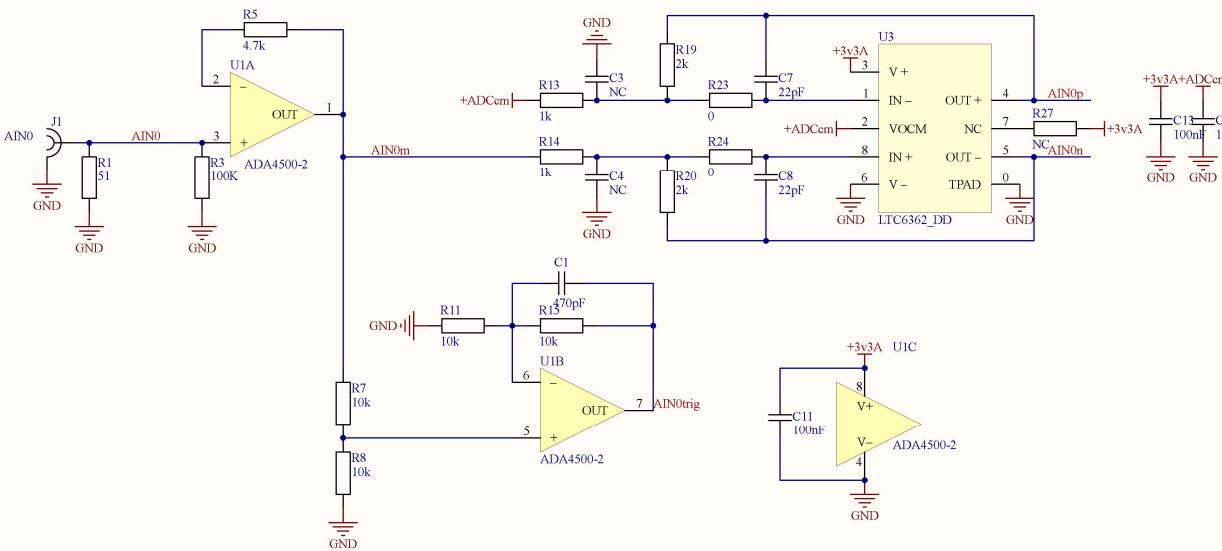
REMOVE R66



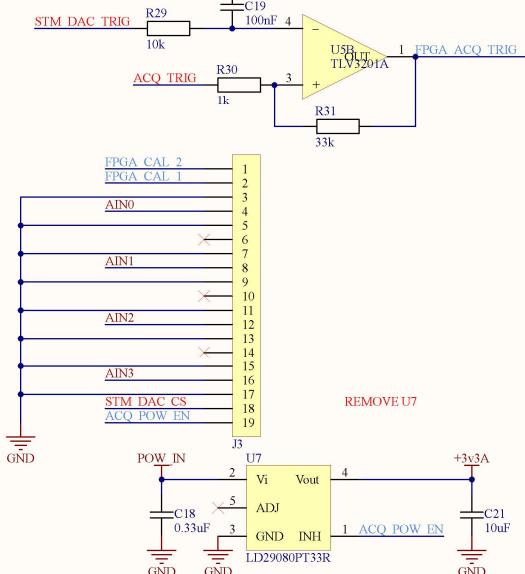
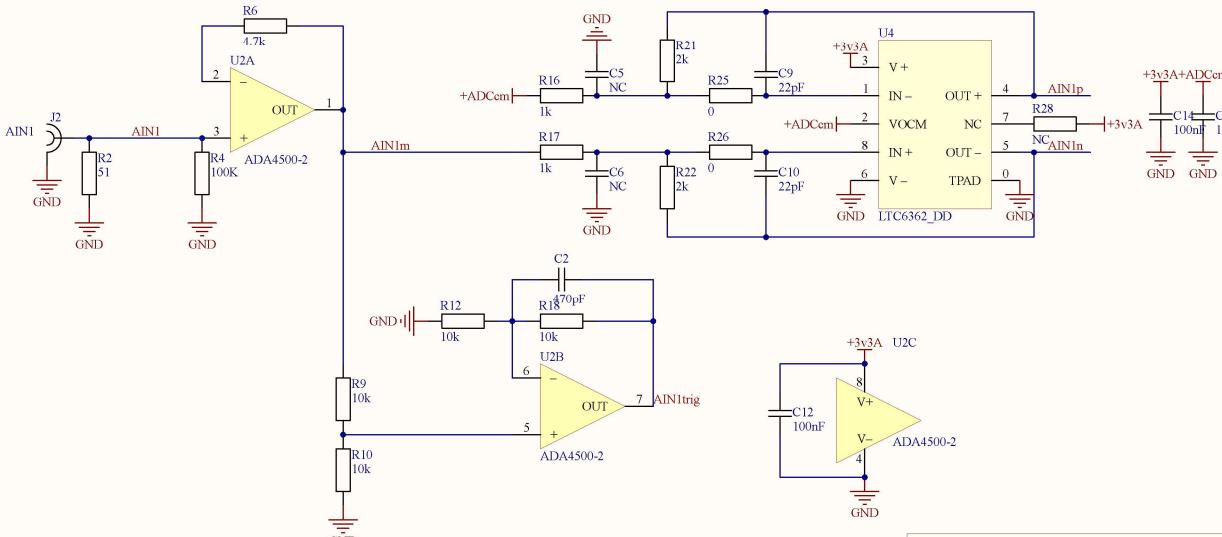
B1 0022552122 B2 FCS-10-SG



ANALOG INPUT 0



ANALOG INPUT 1



BalEv.PrjPcb

BalEv_AINa_v1_0.SchDoc

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Date : 17.01.2022

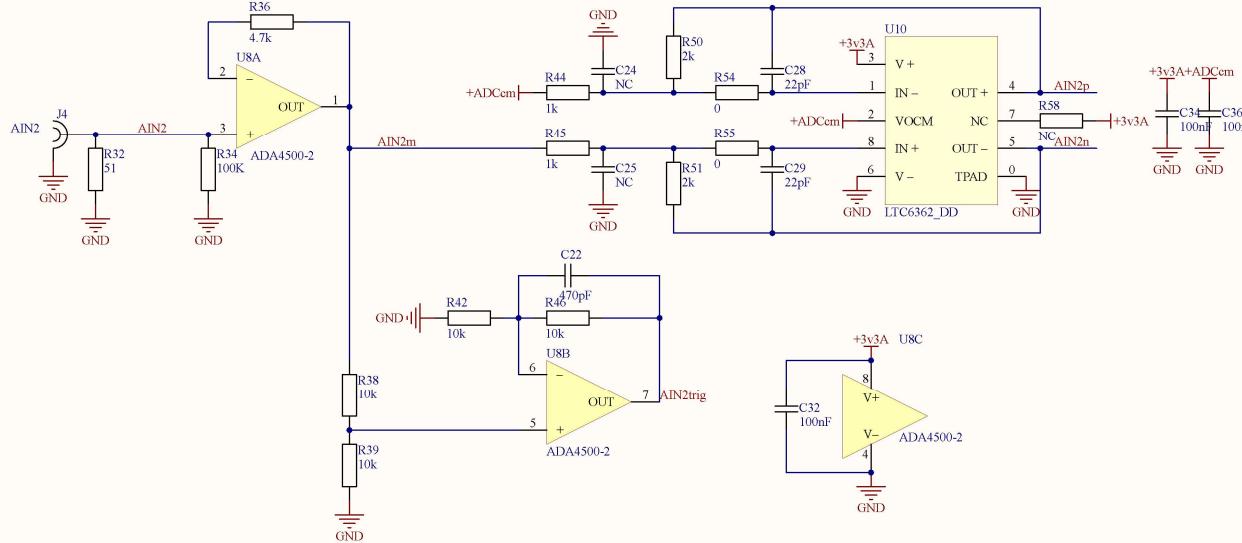


Revision : 1.0a

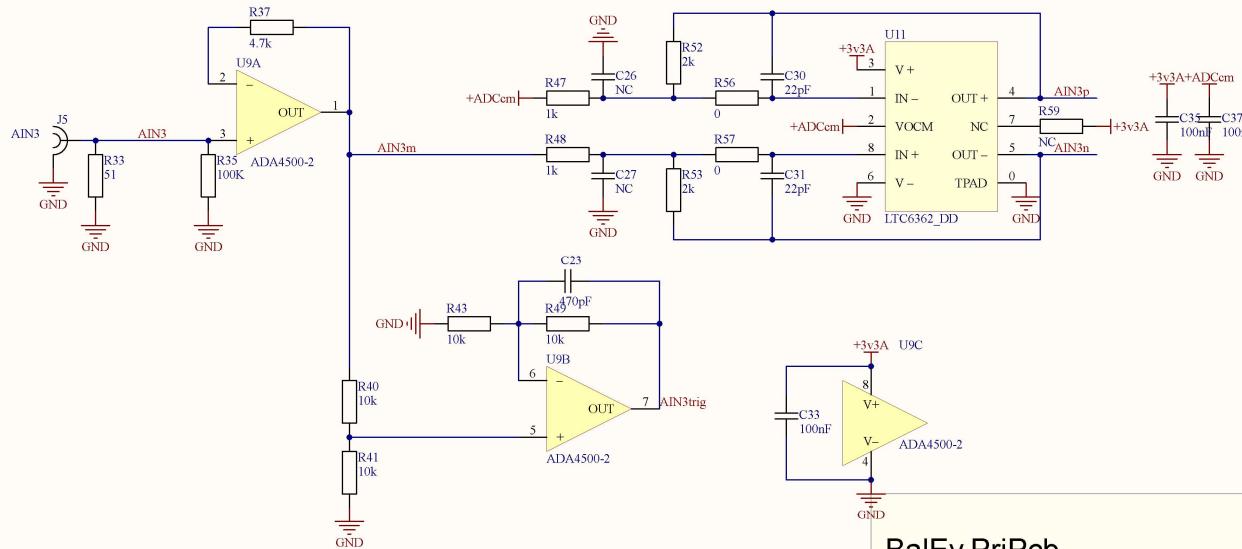
Sheet 6 of 9

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ANALOG INPUT 2



ANALOG INPUT 3



BalEv.PrjPcb

Hes-SO // VALAIS WALLIS

Date : 17.01.2022

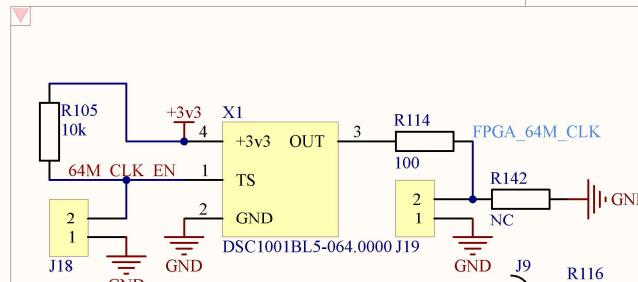


BalEv_AINb_v1_0.SchDoc

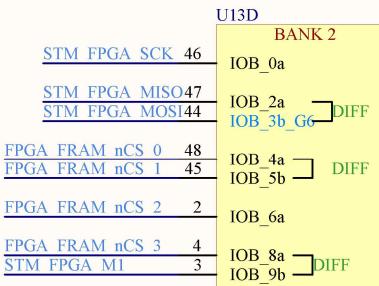
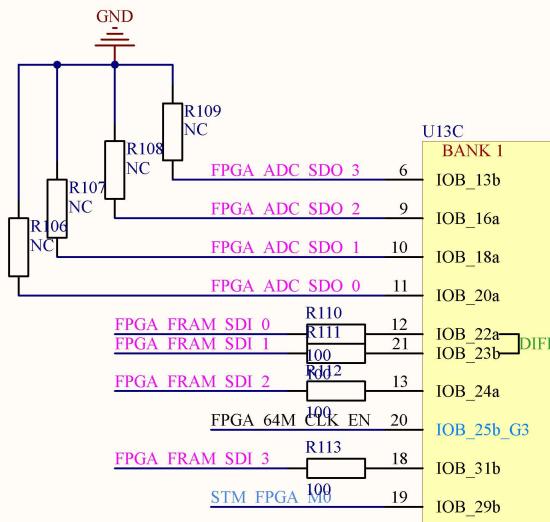
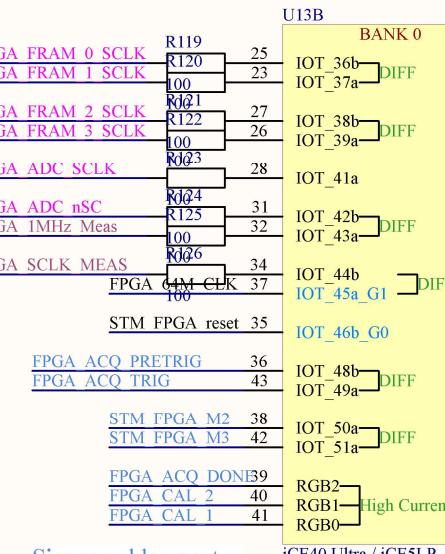
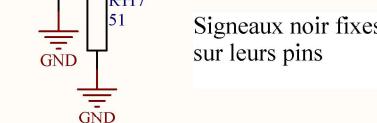
Revision : 1.0a

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Signaux rose ->
connexions court.
Peut être échangé
sur le même BANK.
Rose foncé peut être
plus longues, garde
avec les autres rose.



iCE40 Ultra / iCE5LP

BalEv.PrjPcb

BalEv_FPTG_IO_v1_0.SchDoc

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Date : 17.01.2022



Revision : 1.0a

Sheet 8 of 9

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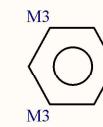
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BalEv.PrjPcb

BalEv_Mechanic_v1_0.SchDoc

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Date : 17.01.2022

Revision : 1.0a

Sheet 9 of 9

Design by : anx/sap

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