## Power-up / idle ??

## Setup / readout

1. **Processor** read/write **ADC** registers
   * *ADC\_nCS* control by proc, *FRAM\_x\_nCS* high, *FPGA\_nCS* high
   * Proc\_SPI ↔ ADC\_SPI (SCLK, SDO\_0, SDI, ADC\_nCS)
2. **Processor** read/reset **FPGA** *FRAM\_ADDR\_CNT* and write **FPGA** *ACQ\_LEN* (default 90% )
   * *ADC\_nCS* high, *FRAM\_x\_nCS* high, *FPGA\_nCS* low
   * Proc\_SPI ↔ FPGA\_SPI (SCLK, SDO, SDI)
3. **Processor** read from one of four **FRAM**
   * *ADC\_nCS* high, *FRAM\_x\_nCS* one low others high, *FPGA\_nCS* high
   * Proc\_SPI ↔ FRAM\_SPI (SCLK, SDO, SDI)
4. **Processor** write to all four **FRAM** simultaneously (setup for acquisition)
   * *ADC\_nCS* high, *FRAM\_x\_nCS* all low, *FPGA\_nCS* high
   * Proc\_SPI ↔ FRAM\_SPI (SCLK, SDO, SDI)
   * *FRAM\_x\_nCS* stays low on transition to ACQ mode

## ACQ wait for trigger on external signal *ACQ\_trig*

* Should happen after Setup point 4**.** *FRAM\_x\_nCS* must be continuously asserted low
* FPGA generates acquisition clock *ACQ\_CLK*
  + Send to *ADC\_nCS*
* FPGA generates acquisition SPI data clock *ACQ\_SCLK*
  + Send to *ADC\_SCLK* and *FRAM\_x\_SCLK*
* FPGA connects *ADC\_SDOx* with *FRAM\_x\_SDI*
* FPGA increment *FRAM\_ADDR\_CNT* each *ACQ\_CLK* rising edge
* Can only be interrupted by *ACQ\_trig* (and global reset)

## ACQ trigger received on external signal *ACQ\_trig*

* FPGA continues as above for *ACQ\_LEN* additional *ACQ\_CLK* rising edges
  + Then performs offset calibration
    - stops: *ACQ\_CLK, ACQ\_SCLK*
    - Change the analogue muxes to GND connection
    - Delay some time
    - starts: *ACQ\_CLK, ACQ\_SCLK,* records ~1000 samples
  + Then performs gain calibration
    - stops: *ACQ\_CLK, ACQ\_SCLK*
    - Change the analogue muxes to Reference DC voltage connection
    - Delay some time
    - starts: *ACQ\_CLK, ACQ\_SCLK,* records ~1000 samples
  + Then stops: *ACQ\_CLK, ACQ\_SCLK,* all four *FRAM\_x\_nCS* goes high
  + Signal *ACQ\_DONE* to processor
  + Cannot be interrupted (except global reset)

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| FPGA external connections to other devices. → is input to FPGA, ← is output from FPGA | | | | | | | |
| Proc. Connections | | ADC Connections | | FRAM\_x Connections X 4 | | OTHER | |
| → | PROC\_SCLK | ← | ADC\_SCLK | ← | FRAM\_x\_SCLK | → | 64 MHz in |
| ← | PROC\_SDI | → | ADC\_SDO\_0 | → | FRAM\_x\_SDI | → | ACQ\_trig |
| → | PROC\_SDO | → | ADC\_SDO\_1 | ← | FRAM\_x\_SDO? | → | Reset? |
| → | PROC\_nCS | → | ADC\_SDO\_2 | → | FRAM\_x\_nCS |  |  |
| → | ACQ\_pretrig | → | ADC\_SDO\_3 |  |  |  |  |
| ← | ACQ\_DONE | ← | ADC\_SDI? |  |  |  |  |
|  |  | ← | ADC\_nCS |  |  |  |  |
|  | 6 + mode control! |  | 7 pins |  | 16 pins |  | 2 pins |

* Could connect FRAM\_x\_SDO directly with PROC\_SDI outside FPGA and tristate FPGA SPI bus.
* Could connect ADC\_SDI directly with PROC\_SDO outside FPGA and tristate FPGA SPI bus
* Can we reset from CRESET\_B to redo configuration download from SRAM? Or power cycle reset?