

# TXB0304 4-Bit Bidirectional Level-Shifter/Voltage Translator with Automatic Direction Sensing

## 1 Features

- Fully Symmetric Supply Voltages, 0.9 V to 3.6 V on A Port and 0.9 V to 3.6 V
- $V_{CC}$  Isolation Feature – If Either  $V_{CC}$  Input is at GND, all Outputs are in High-Impedance State
- OE Input Circuit Referenced to  $V_{CCA}$
- Low Power Consumption, 5  $\mu$ A Max ( $I_{CCA}$  or  $I_{CCB}$ )
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 8000-V Human-Body Model (A114-B)
  - 1000-V Charged-Device Model (C101)

## 2 Applications

- Personal Electronics
- Industrial
- Enterprise
- Telecom

## 3 Description

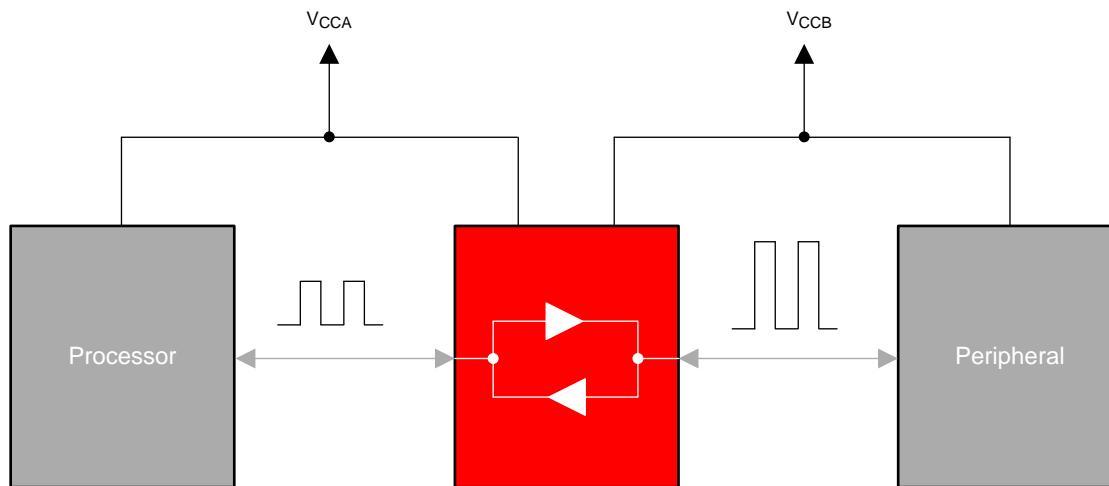
This 4-bit non-inverting translator uses two separate configurable power-supply rails. The A port is designed to track  $V_{CCA}$ .  $V_{CCA}$  accepts any supply voltage from 0.9 V to 3.6 V. The B port is designed to track  $V_{CCB}$ .  $V_{CCB}$  accepts any supply voltage from 0.9 V to 3.6 V. This allows for low Voltage bidirectional translation between 1 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V voltage nodes. For the TXB0304, when the output-enable (OE) input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pull-down resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver. The OE device control pin input circuit is supplied by  $V_{CCA}$ . This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The only difference between TXB0304 and TXBN0304 is the OE signal being active high and active low respectively.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TXB0304	RUT UQFN (12)	2.00 mm x 1.70 mm
	RSV UQFN (16)	2.60 mm x 1.80 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

### Typical Application Block Diagram for TXB0304



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (May 2016) to Revision G	Page
• Changed text in <i>Power Supply Recomendations</i> section.	13

Changes from Revision E (August 2014) to Revision F	Page
• Made changes to <i>Description</i> section.....	1
• Made changes to <i>Absolute Maximum Ratings</i> , <i>Recommended Operating Conditions<sup>(1)(2)</sup></i> , <i>Switching Characteristics</i> and <i>Electrical Characteristics</i> tables.....	1

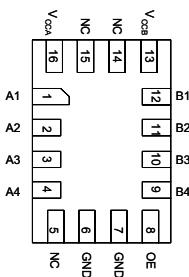
Changes from Revision D (October 2012) to Revision E	Page
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section.	1
• Changed VCCA and VCCB in the ABS MAX table to V <sub>C<sub>CA</sub></sub> and V <sub>C<sub>CB</sub></sub> in 3 places .....	4
• Changed in ELEC CHARAC table the 0.9 x V <sub>C<sub>CA</sub></sub> and 0.9 x V <sub>C<sub>CB</sub></sub> from MAX column into the MIN column .....	5
• Changed in ELEC CHARAC table 0.2 (2 places) in the MIN column to the MAX .....	5

Changes from Revision C (May 2012) to Revision D	Page
• Added <i>Application Information</i> section .....	12

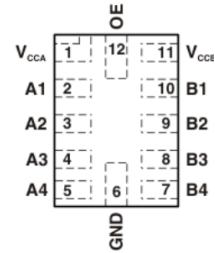
Changes from Revision B (September 2011) to Revision C	Page
• Added package pin out diagram notes.....	3

## 5 Pin Configuration and Functions

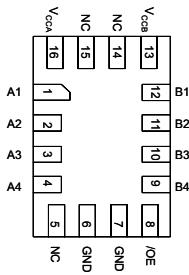
**RSV Package**  
**16-Pin UQFN**  
**TXB0304 Top View**



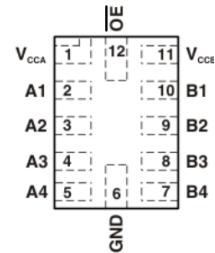
**RUT Package**  
**12-Pin UQFN**  
**TXB0304 Top View**



**RSV Package**  
**16-Pin UQFN**  
**TXBN0304 Top View**



**RUT Package**  
**12-Pin UQFN**  
**TXBN0304 Top View**



- A. See [Layout Guidelines](#) for notes about package pin out diagrams.

### Pin Functions

NAME	PIN				TYPE	DESCRIPTION		
	TXB0304		TXBN0304					
	RSV	RUT	RSV	RUT				
A1	1	2	1	2	I/O	Input/output 1		
A2	2	3	2	3	I/O	Input/output 2		
A3	3	4	3	4	I/O	Input/output 3		
A4	4	5	4	5	I/O	Input/output 4		
B1	12	10	12	10	I/O	Input/output 4		
B2	11	9	11	9	I/O	Input/output 3		
B3	10	8	10	8	I/O	Input/output 2		
B4	9	7	9	7	I/O	Input/output 1		
GND	6, 7	6	6,7	6	GND	Ground		
NC	5, 14, 15	—	5, 14, 15	—	—	No connection; not internally connected		
OE	8	12	—	—	I	3-state output-mode enable. Pull OE (TXB0304) low to place all outputs in 3-state mode. Referenced to VCCA.		
$\overline{OE}$	—	—	8	12	I	3-state output-mode enable. Pull $\overline{OE}$ (TXBN0304) high to place all outputs in 3-state mode. Referenced to VCCA.		
VCCA	16	1	16	1	—	A-port supply voltage $0.9 \text{ V} \leq V_{CCA} \leq 3.6 \text{ V}$		
VCCB	13	11	13	11	—	B-port supply voltage $0.9 \text{ V} \leq V_{CCB} \leq 3.6 \text{ V}$		

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CCA</sub>	Supply voltage	A port	-0.5	4.6	V
V <sub>CCB</sub>		B port	-0.5	4.6	
V <sub>I</sub>	Input voltage	A port	-0.5	4.6	V
		B port	-0.5	4.6	
V <sub>O</sub>	Voltage applied to any output in the high-impedance or power-off state	A port	-0.5	4.6	V
		B port	-0.5	4.6	
V <sub>O</sub>	Voltage applied to any output in the high or low state <sup>(2)</sup>	A port	-0.5	V <sub>CCA</sub> + 0.5	V
		B port	-0.5	V <sub>CCB</sub> + 0.5	
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50	mA
I <sub>O</sub>	Continuous output current			±50	mA
	Continuous current through V <sub>CCA</sub> , V <sub>CCB</sub> , or GND			±100	mA
T <sub>stg</sub>	Storage temperature		-65	150	°C
T <sub>J</sub>	Junction temperature		-40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The value of V<sub>CCA</sub> and V<sub>CCB</sub> are provided in the recommended operating conditions table.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±8000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions<sup>(1)(2)</sup>

		V <sub>CCA</sub>	V <sub>CCB</sub>	MIN	MAX	UNIT
V <sub>CCA</sub>	Supply voltage			0.9	3.6	V
V <sub>IH</sub>	High-level input voltage	Data inputs	0.9 V to 3.6 V	0.9 V to 3.6 V	V <sub>CCI</sub> × 0.65	V
		OE/̄OE	0.9 V to 3.6 V	0.9 V to 3.6 V	V <sub>CCA</sub> × 0.65	
V <sub>IL</sub>	Low-level input voltage	Data inputs	0.9 V to 3.6 V	0.9 V to 3.6 V	0	V
		OE/̄OE	0.9 V to 1.2 V	0.9 V to 3.6 V	0	
			1.2 V to 3.6 V	0.9 V to 3.6 V	0	
V <sub>O</sub>	Voltage range applied to any output in the high-impedance or power-off state	A-port	0.9 V to 3.6 V	0.9 V to 3.6 V	0	V
		B-port	0.9 V to 3.6 V	0.9 V to 3.6 V	0	
Δt/Δv	Input transition rise or fall rate	A-port inputs	0.9 V to 3.6 V	0.9 V to 3.6 V	40	ns/V
		B-port inputs	0.9 V to 3.6 V	0.9 V to 3.6 V	40	
T <sub>A</sub>	Operating free-air temperature			-40	85	°C

(1) The A and B sides of an unused data I/O pair must be held in the same state, such as, both at V<sub>CCI</sub> or both at GND.

(2) V<sub>CCI</sub> is the supply voltage associated with the input port.

## 6.4 Thermal Information

	THERMAL METRIC <sup>(1)</sup>	TXB0304		UNIT
		RUT (UQFN)	RSV (UQFN)	
		12 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.4	131.7	°C/W
$R_{\theta JC(\text{top})}$	Junction-to-case (top) thermal resistance	45.7	55.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.9	55.3	°C/W
$\psi_{JT}$	Junction-to-top characterization parameter	0.6	1.4	°C/W
$\psi_{JB}$	Junction-to-board characterization parameter	46.9	55.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V <sub>CCA</sub>	V <sub>CCB</sub>	MIN	TYP	MAX	UNIT
V <sub>OHA</sub>	High-level output voltage	I <sub>OH</sub> = -20 μA	T <sub>A</sub> = 25°C	0.9 V to 3.6 V		0.9 x V <sub>CCA</sub>		V
V <sub>OLA</sub>	Low-level output voltage	I <sub>OL</sub> = 20 μA	-40°C to 85°C	0.9 V to 3.6 V			0.2	V
V <sub>OHB</sub>	High-level output voltage	I <sub>OH</sub> = -20 μA	T <sub>A</sub> = 25°C		0.9 V to 3.6 V	0.9 x V <sub>CCB</sub>		V
V <sub>OLB</sub>	Low-level output voltage	I <sub>OL</sub> = 20 μA	-40°C to 85°C		0.9 V to 3.6 V		0.2	V
I <sub>I</sub>	OE	V <sub>I</sub> = V <sub>CCI</sub> or GND	T <sub>A</sub> = 25°C -40°C to 85°C	0.9 V to 3.6 V	0.9 V to 3.6 V	±1 ±2		μA
I <sub>off</sub>	A port	V <sub>I</sub> or V <sub>O</sub> = 0 to 3.6 V	T <sub>A</sub> = 25°C -40°C to 85°C	0 V	0 V to 3.6 V	±1 ±2		μA
	B port	V <sub>I</sub> or V <sub>O</sub> = 0 to 3.6 V	T <sub>A</sub> = 25°C -40°C to 85°C	0.9 V to 3.6 V	0 V	±1 ±2		
I <sub>OZ</sub>	A or B port	OE = GND	T <sub>A</sub> = 25°C -40°C to 85°C	0.9 V to 3.6 V	0.9 V to 3.6 V	±1 ±2		μA
I <sub>CCA</sub>		V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0	-40°C to 85°C	0.9 V to 3.6 V	0.9 V to 3.6 V		5	μA
I <sub>CCB</sub>		V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0	-40°C to 85°C	0.9 V to 3.6 V	0.9 V to 3.6 V		5	μA
I <sub>CCA</sub> + I <sub>CCB</sub>		V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0	-40°C to 85°C	0.9 V to 3.6 V	0.9 V to 3.6 V		10	μA
I <sub>CCZA</sub>	High-Z state supply current	V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0, OE = GND	-40°C to 85°C	0.9 V to 3.6 V	0.9 V to 3.6 V		5	μA
I <sub>CCZB</sub>	High-Z state supply current	V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0, OE = GND	-40°C to 85°C	0.9 V to 3.6 V	0.9 V to 3.6 V		5	μA
C <sub>i</sub>	OE	T <sub>A</sub> = 25°C		0.9 V to 3.6 V	0.9 V to 3.6 V		3	pF
C <sub>io</sub>	A port	T <sub>A</sub> = 25°C, OE = GND		0.9 V to 3.6 V	0.9 V to 3.6 V	6.7		pF
	B port					6.7		

## 6.6 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	LOAD	V <sub>CCA</sub>	V <sub>CCB</sub>	MIN	MAX	UNIT
Data rate	C <sub>L</sub> = 15 pF	0.9 to 3.6 V	0.9 to 3.6 V		50	Mbps
	C <sub>L</sub> = 15 pF	1.2 to 3.6 V	1.2 to 3.6 V		100	Mbps
	C <sub>L</sub> = 15 pF	1.8 to 3.6 V	1.8 to 3.6 V		140	Mbps
	C <sub>L</sub> = 30 pF	0.9 to 3.6 V	0.9 to 3.6 V		40	Mbps
	C <sub>L</sub> = 30 pF	1.2 to 3.6 V	1.2 to 3.6 V		90	Mbps
	C <sub>L</sub> = 30 pF	1.8 to 3.6 V	1.8 to 3.6 V		130	Mbps
	C <sub>L</sub> = 50 pF	1.2 to 3.6 V	1.2 to 3.6 V		80	Mbps
	C <sub>L</sub> = 50 pF	1.8 to 3.6 V	1.8 to 3.6 V		120	Mbps
	C <sub>L</sub> = 100 pF	1.2 to 3.6 V	1.2 to 3.6 V		70	Mbps
	C <sub>L</sub> = 100 pF	1.8 to 3.6 V	1.8 to 3.6 V		100	Mbps

## 6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted). (For parameter descriptions, see [Figure 2](#) and [Figure 3](#).)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD	V <sub>CCA</sub>	V <sub>CCB</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
t <sub>pd</sub>	A	B	C <sub>L</sub> = 15	0.9-3.6	0.9-3.6		18.9	30	ns
	A	B	C <sub>L</sub> = 15	1.2-3.6	1.2-3.6		7.5	11.5	
	A	B	C <sub>L</sub> = 15	1.8-3.6	1.8-3.6		3.7	4.8	
	A	B	C <sub>L</sub> = 30	0.9-3.6	0.9-3.6		19.5	34	
	A	B	C <sub>L</sub> = 30	1.2-3.6	1.2-3.6		7.8	11.9	
	A	B	C <sub>L</sub> = 30	1.8-3.6	1.8-3.6		3.8	5.2	
	A	B	C <sub>L</sub> = 50	1.2-3.6	1.2-3.6		8	12.3	
	A	B	C <sub>L</sub> = 50	1.8-3.6	1.8-3.6		4	5.4	
	A	B	C <sub>L</sub> = 100	1.2-3.6	1.2-3.6		8.6	13.5	
	A	B	C <sub>L</sub> = 100	1.8-3.6	1.8-3.6		4.5	6	
t <sub>en</sub>	B	A	C <sub>L</sub> = 15	0.9-3.6	0.9-3.6		18.9	30	ns
	B	A	C <sub>L</sub> = 15	1.2-3.6	1.2-3.6		7.5	11.5	
	B	A	C <sub>L</sub> = 15	1.8-3.6	1.8-3.6		3.7	5	
	B	A	C <sub>L</sub> = 30	0.9-3.6	0.9-3.6		19.5	34	
	B	A	C <sub>L</sub> = 30	1.2-3.6	1.2-3.6		7.8	11.9	
	B	A	C <sub>L</sub> = 30	1.8-3.6	1.8-3.6		3.8	5.2	
	B	A	C <sub>L</sub> = 50	1.2-3.6	1.2-3.6		8	12.3	
	B	A	C <sub>L</sub> = 50	1.8-3.6	1.8-3.6		4	5.4	
	B	A	C <sub>L</sub> = 100	1.2-3.6	1.2-3.6		8.6	13.5	
	B	A	C <sub>L</sub> = 100	1.8-3.6	1.8-3.6		4.5	6	
t <sub>dis</sub>	OE	A	C <sub>L</sub> = 15	0.9-3.6	0.9-3.6		262		ns
				1.2-3.6	1.2-3.6		64		
				1.8-3.6	1.8-3.6		37		
		B	C <sub>L</sub> = 15	0.9-3.6	0.9-3.6		332		
				1.2-3.6	1.2-3.6		76		
				1.8-3.6	1.8-3.6		41		
t <sub>rB</sub> , t <sub>fB</sub>	B-port rise and fall times	A	C <sub>L</sub> = 15	0.9-3.6	0.9-3.6		172		ns
				0.9-3.6	0.9-3.6		169		
t <sub>sA</sub> , t <sub>fA</sub>	A-port rise and fall times		C <sub>L</sub> = 15	0.9-3.6	0.9-3.6		2.95		ns
t <sub>SK(O)</sub>	Channel-to-channel skew		C <sub>L</sub> = 15	0.9-3.6	0.9-3.6		3.1		ns
							0.15		ns

(1) T<sub>A</sub> = 25°C

## 6.8 Operating Characteristics

$C_{pd}$  - power dissipation capacitance measured at  $T_A = 25^\circ\text{C}$ .

PARAMETER		TEST CONDITIONS	TYP <sup>(1)</sup>	UNIT
$C_{pdA}$	A-port input, B-port output	$C_L = 0$ , $f = 10 \text{ MHz}$ , $t_r = t_f = 1 \text{ ns}$ , $\text{OE} = V_{CCA}$ (outputs enabled)	34	pF
	B-port input, A-port output		34	pF
$C_{pdB}$	A-port input, B-port output	$C_L = 0$ , $f = 10 \text{ MHz}$ , $t_r = t_f = 1 \text{ ns}$ , $\text{OE} = \text{GND}$ (outputs disabled)	34	pF
	B-port input, A-port output		34	pF
$C_{pdA}$	A-port input, B-port output	$C_L = 0$ , $f = 10 \text{ MHz}$ , $t_r = t_f = 1 \text{ ns}$ , $\text{OE} = \text{GND}$ (outputs disabled)	0.01	pF
	B-port input, A-port output		0.01	pF
$C_{pdB}$	A-port input, B-port output	$C_L = 0$ , $f = 10 \text{ MHz}$ , $t_r = t_f = 1 \text{ ns}$ , $\text{OE} = \text{GND}$ (outputs disabled)	0.01	pF
	B-port input, A-port output		0.01	pF

(1)  $V_{CCA}$ ,  $V_{CCB}$  0.9 V to 3.6 V

## 6.9 Typical Characteristics

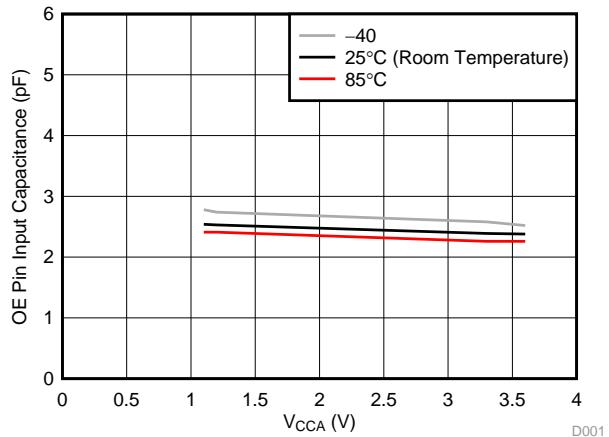
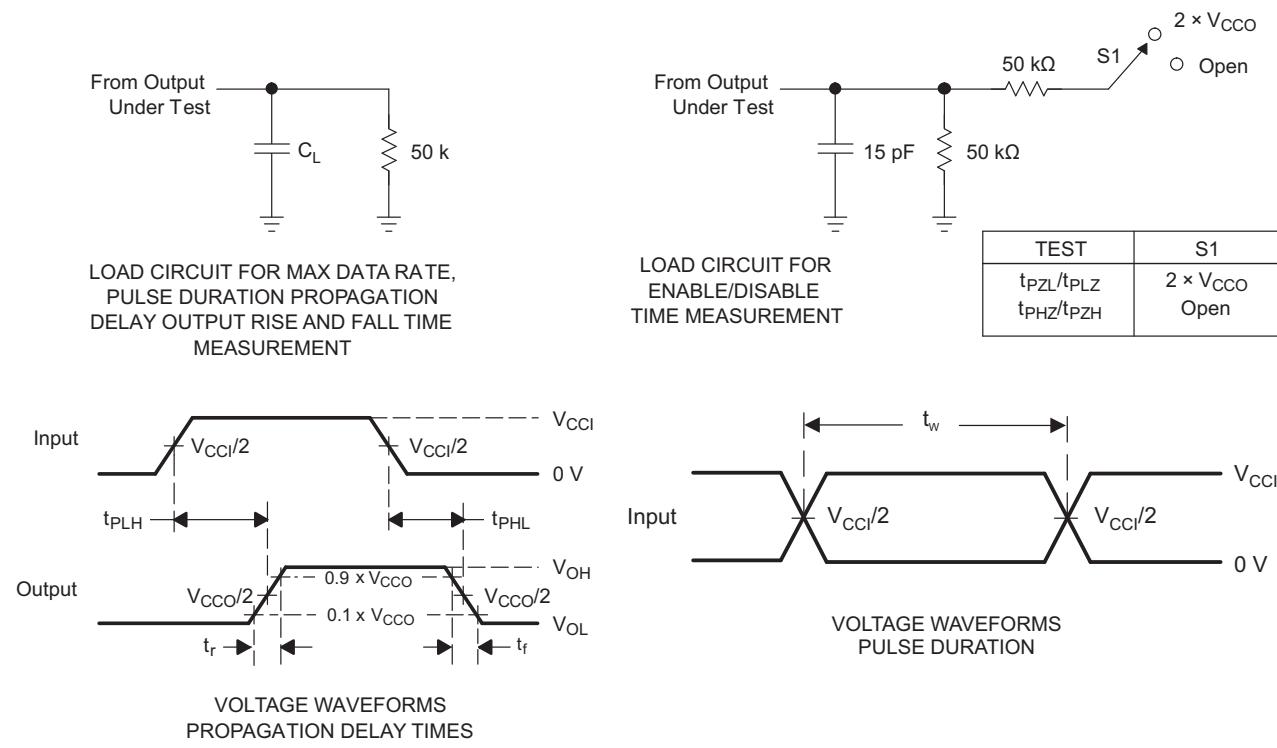


Figure 1. Input Capacitors for OE Pin ( $C_OE$ ) vs Power Supply ( $V_{CCA}$ )

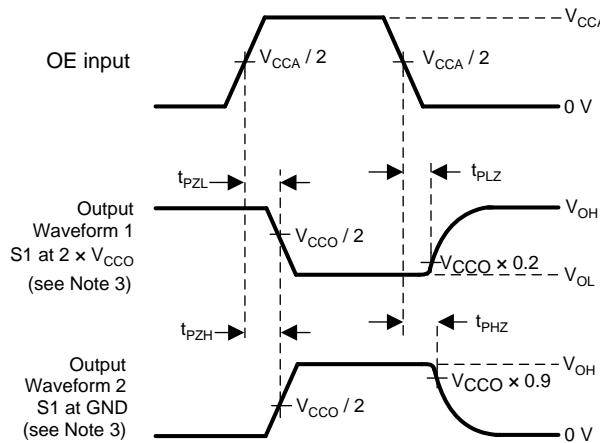
## 7 Parameter Measurement Information



- A.  $C_L$  includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: PRR 10 MHz,  $Z_O = 50 \Omega$ ,  $dv/dt \geq 1$  V/ns.
- C. The outputs are measured one at a time, with one transition per measurement.
- D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- E.  $V_{CCI}$  is the  $V_{CC}$  associated with the input port.
- F.  $V_{CCO}$  is the  $V_{CC}$  associated with output port.
- G. All parameters and waveforms are not applicable to all devices.

**Figure 2. Load Circuits and Voltage Waveforms**

### Parameter Measurement Information (continued)



- (1)  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- (2)  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- (3) Waveform 1 is for an output with internal such that the output is high, except when OE is high. Waveform 2 is for an output with conditions such that the output is low, except when OE is high.

**Figure 3. Enable and Disable Times**

## 8 Detailed Description

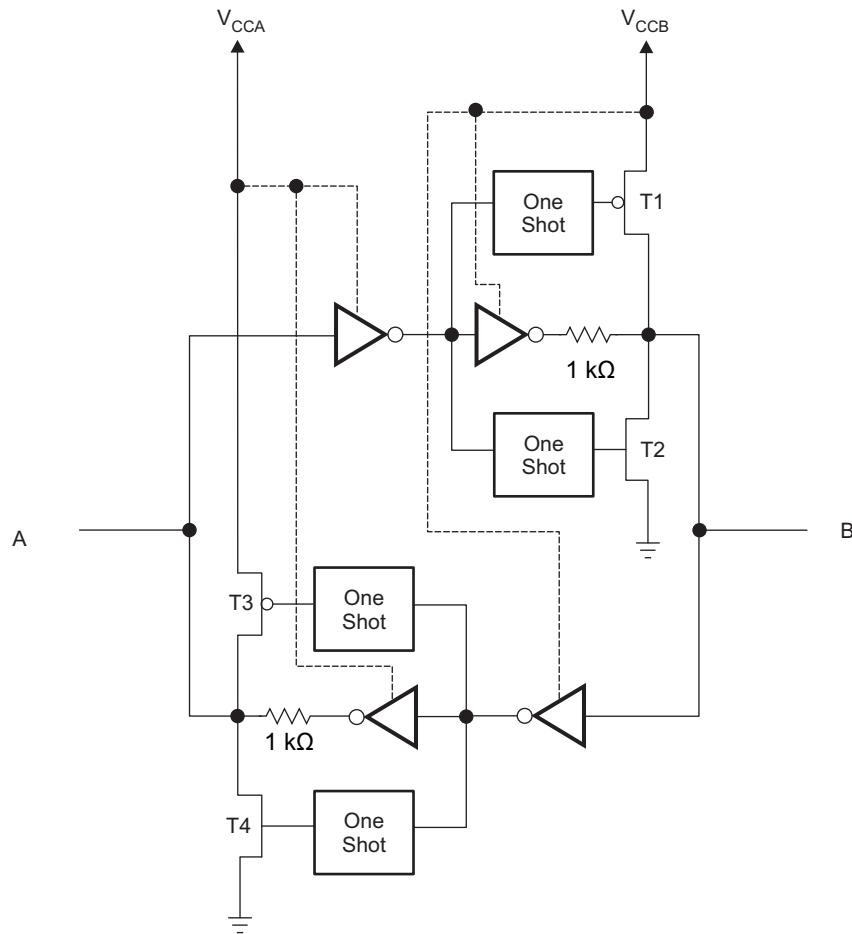
### 8.1 Overview

The TXB0304 and TXBN0304 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another.

#### 8.1.1 Architecture

The TXB0304 and TXBN0304 architecture (see [Figure 4](#)) does not require a direction-control signal to control the direction of data flow from A to B or from B to A. In a dc state, the output drivers of the TXB0304 can maintain a high or low, but are designed to be weak, so that they can be overdriven by an external driver when data on the bus starts flowing the opposite direction. The output one shots detect rising or falling edges on the A or B ports. During a rising edge, the one shot turns on the PMOS transistors (T1, T3) for a short duration, which speeds up the low-to-high transition. Similarly, during a falling edge, the one shot turns on the NMOS transistors (T2, T4) for a short duration, which speeds up the high-to-low transition. The typical output impedance during output transition is  $30\ \Omega$  at  $V_{CCO} = 0.9\text{ V}$  to  $1\text{ V}$ ,  $10\ \Omega$  at  $V_{CCO} = 1.1\text{ V}$  to  $1.7\text{ V}$ , and  $5\ \Omega$  at  $V_{CCO} = 1.8\text{ V}$  to  $3.3\text{ V}$ .

### 8.2 Functional Block Diagram



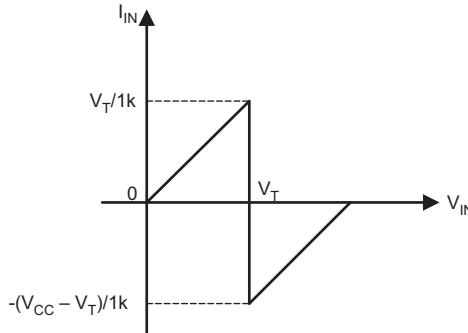
Copyright © 2016, Texas Instruments Incorporated

**Figure 4. Architecture of TXB0304 I/O Cell**

## 8.3 Feature Description

### 8.3.1 Input Driver Requirements

Typical  $I_{IN}$  vs  $V_{IN}$  characteristics of the TXB0304/TXBN0304 are shown in [Figure 5](#). For proper operation, the device driving the data I/Os of the TXB0304 must have drive strength of at least  $\pm 3$  mA.



- (1)  $V_{CC}$  is power supply of TXB0304.
- (2)  $V_T$  is the input threshold voltage of TXB0304 (typically it is  $V_{CC}/2$ ).

**Figure 5. Typical  $I_{IN}$  vs  $V_{IN}$  Curve**

## 8.4 Device Functional Modes

### 8.4.1 Enable and Disable

The TXB0304 has an OE input that is used to disable the device by setting OE = low ( $\overline{OE}$  = high for TXBN0304), which places all I/Os in the high-impedance (Hi-Z) state. The disable time ( $t_{dis}$ ) indicates the delay between when OE goes low and when the outputs actually get disabled (Hi-Z). The enable time ( $t_{en}$ ) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is high.

### 8.4.2 Pullup or Pulldown Resistor on I/O Lines

The TXB0304/TXBN0304 is designed to drive capacitive loads of up to 100 pF. The output drivers of the TXB0304 have low dc drive strength. If pull-up or pull-down resistors are connected externally to the data I/Os, their values must be kept higher than 20 k $\Omega$  to ensure that they do not contend with the output drivers of the TXB0304. but if the receiver is integrated with the smaller pull down or pull up resistor, below formula can be used for estimation to evaluate the  $V_{OH}$  and  $V_{OL}$  .

$$V_{ol} = V_{CCout} \times \frac{1.5k\Omega}{1.5k\Omega + R_{pu}} \quad (1)$$

$$V_{oh} = V_{CCout} \times \frac{R_{pd}}{1.5k\Omega + R_{pd}}$$

where

- $V_{CCOUT}$  is the output port supply voltage on either  $V_{CCA}$  or  $V_{CCB}$
- $R_{PD}$  is the value of the external pull down resistor
- $R_{PU}$  is the value of the external pull up resistor
- 1.5 k $\Omega$  is the counting the variation of the serial resistor 1k $\Omega$  in the I/O line. (2)

Because of this restriction on external resistors, the TXB0304 should not be used in applications such as I<sup>2</sup>C or 1-Wire where an open-drain driver is connected on the bidirectional data I/O. For these applications, use a device from the TI [TXS010X](#) series of level translators.

## 9 Application and Implementation

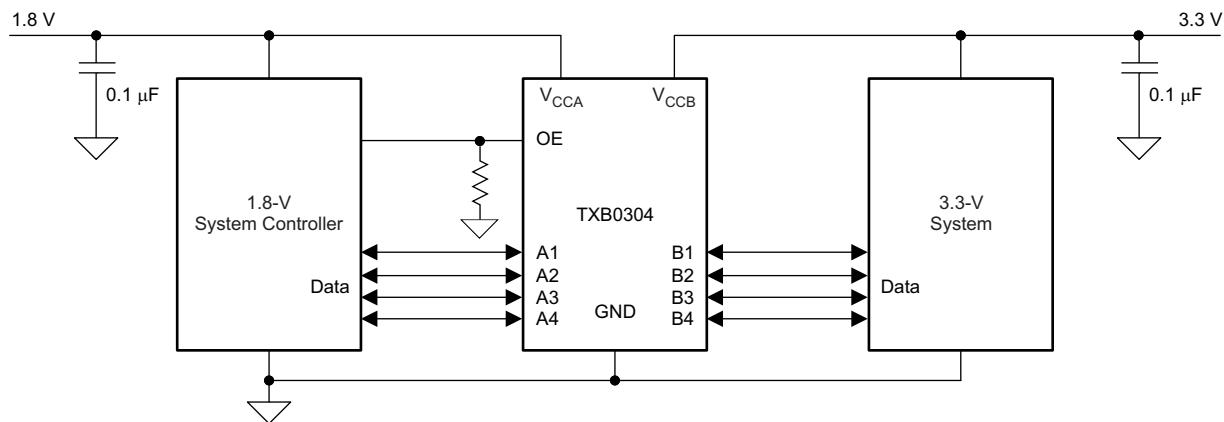
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TXB0304 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. It can only translate push-pull CMOS logic outputs. If for open-drain signal translation, please refer to TI [TXS010X](#) products. Any external pull-down or pull-up resistors are recommended larger than 20 kΩ.

### 9.2 Typical Application



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**Figure 6. Typical Application Schematic**

#### 9.2.1 Design Requirements

For this design example, use the parameters listed in [Table 1](#).

**Table 1. Design Parameters**

DESIGN PARAMETERS	EXAMPLE VALUE
Input voltage range	0.9 V to 3.6 V
Output voltage range	0.9 V to 3.6 V

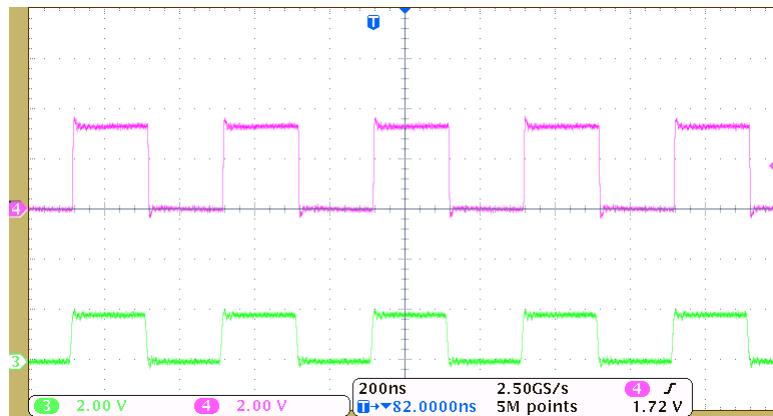
#### 9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the TXB0304 device to determine the input voltage range. For a valid logic high the value must exceed the  $V_{IH}$  of the input port. For a valid logic low the value must be less than the  $V_{IL}$  of the input port.
- Output voltage range
  - Use the supply voltage of the device that the TXB0304 device is driving to determine the output voltage range.
  - Don't recommend to have the external pull-up or pull-down resistors. If mandatory, it is recommended the value should be larger than 20 kΩ.

- An external pull-down or pull-up resistor decreases the output  $V_{OH}$  and  $V_{OL}$ . Use the below equations in section 8.5.2 to draft estimate the  $V_{OH}$  and  $V_{OL}$  as a result of an external pull-down and pull-up resistor.

### 9.2.3 Application Curve



**Figure 7. Level-Translation of a 2.5-MHz Signal**

## 10 Power Supply Recommendations

During operation, TXB0304 can work at both  $VCCA \leq VCCB$  and  $VCCA \geq VCCB$ . During power-up sequencing, any power supply can be ramped up first. Both the supplies are recommended to be powered down together. The TXB0304 has circuitry that disables all input/output ports when either VCC is switched off ( $VCCA/B = 0$  V).

## 11 Layout

### 11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended.

- Bypass capacitors should be used on power supplies. And should be placed as close as possible to the  $V_{CCA}$ ,  $V_{CCB}$  pin and GND pin
- Short trace-lengths should be used to avoid excessive loading.
- For long transmission lines, place a series resistor equivalent to the impedance of the transmission lines to avoid signal integrity issues
- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one-shot duration, approximately 10 ns, ensuring that any reflection encounters low impedance at the source driver.
- Pullup resistors are not required on both sides for Logic I/O.
- If pullup or pulldown resistors are needed, the resistor value must be over 20 k $\Omega$ .
- 20 k $\Omega$  is a safe recommended value, if the customer can accept higher  $V_{OL}$  or lower  $V_{OH}$ , smaller pull up or pull down resistor is allowed, the draft estimation is  $V_{OL} = V_{CCout} \times 1.5k/(1.5k + R_{pu})$  and  $V_{OH} = V_{CCout} \times R_{pd}/(1.5k + R_{pd})$ .
- If pullup resistors are needed, please refer to the TXS0104 or contact TI.
- For detailed information, refer to application note [SCEA043](#).

## 11.2 Layout Example

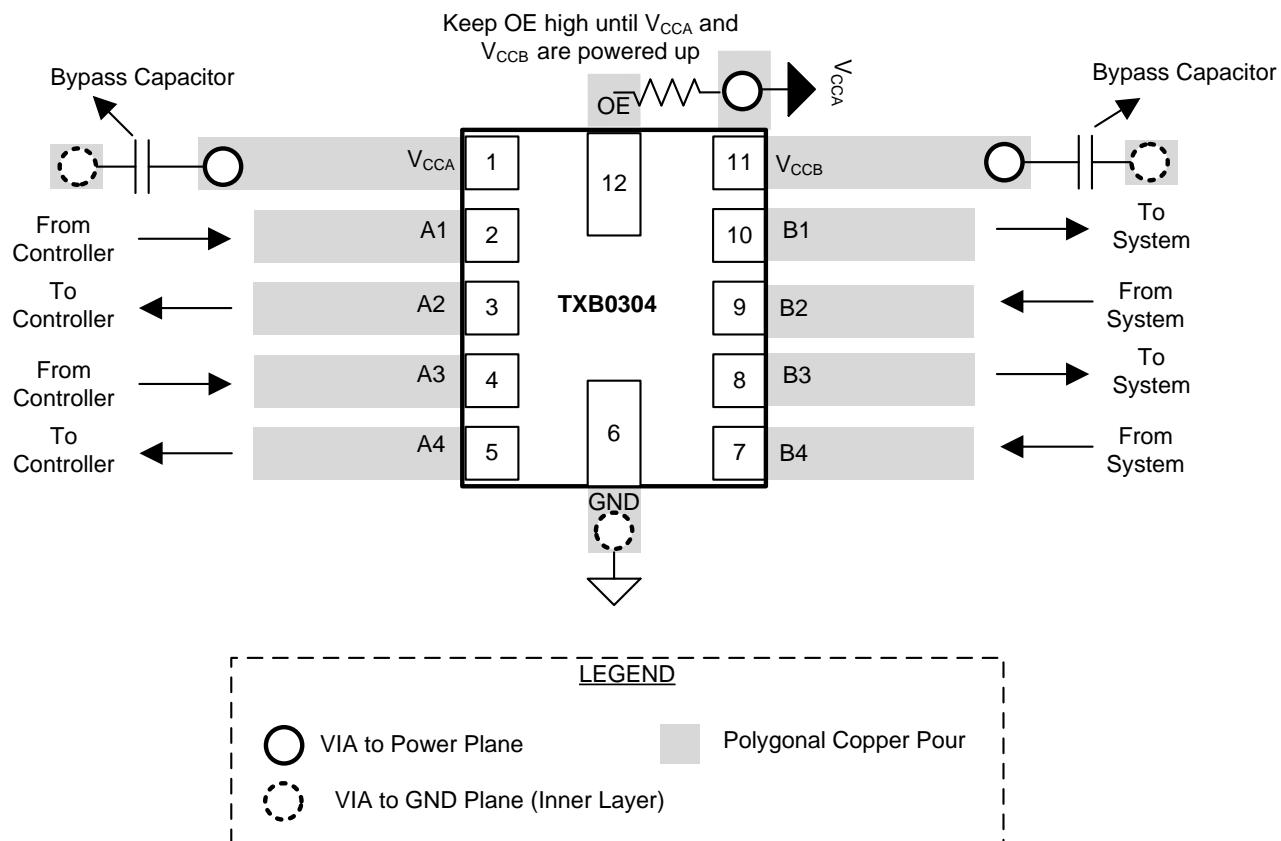


Figure 8. TXB0304 PCB Layout

## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 Development Support

For TI TXS010X products, go to [www.ti.com/product/txs0101](http://www.ti.com/product/txs0101).

For the TXB0304 IBIS Model, see [SCEM544](#).

### 12.2 Documentation Support

#### 12.2.1 Related Documentation

For related documentation see the following:

- Application Report, *A Guide to Voltage Translation With TXB-Type Translators*, [SCEA043](#)
- User's Guide, *TXB0304 Evaluation Module*, [SCEU003](#)

### 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.4 Trademarks

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### 12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TXB0304RSVR</a>	Active	Production	UQFN (RSV)   16	3000   LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ZTJ
<a href="#">TXB0304RSVR.B</a>	Active	Production	UQFN (RSV)   16	3000   LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ZTJ
<a href="#">TXB0304RUTR</a>	Active	Production	UQFN (RUT)   12	3000   LARGE T&R	Yes	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(737, 73R, 73V)
<a href="#">TXB0304RUTR.B</a>	Active	Production	UQFN (RUT)   12	3000   LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(737, 73R, 73V)
<a href="#">TXBN0304RSVR</a>	Active	Production	UQFN (RSV)   16	3000   LARGE T&R	Yes	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ZTK
<a href="#">TXBN0304RSVR.B</a>	Active	Production	UQFN (RSV)   16	3000   LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ZTK
<a href="#">TXBN0304RUTR</a>	Active	Production	UQFN (RUT)   12	3000   LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	74R
<a href="#">TXBN0304RUTR.B</a>	Active	Production	UQFN (RUT)   12	3000   LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	74R

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

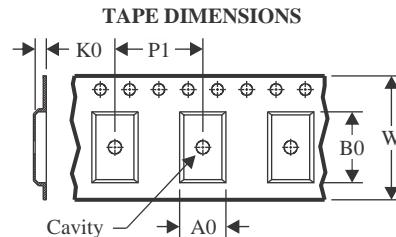
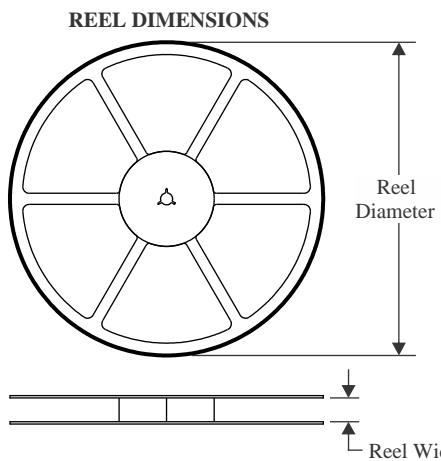
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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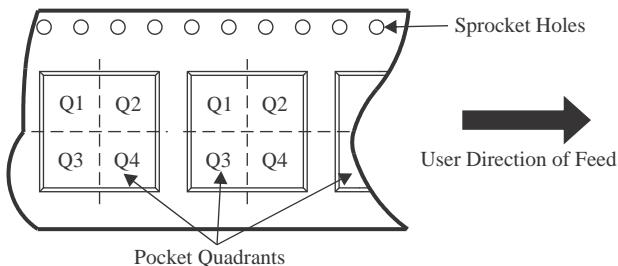
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



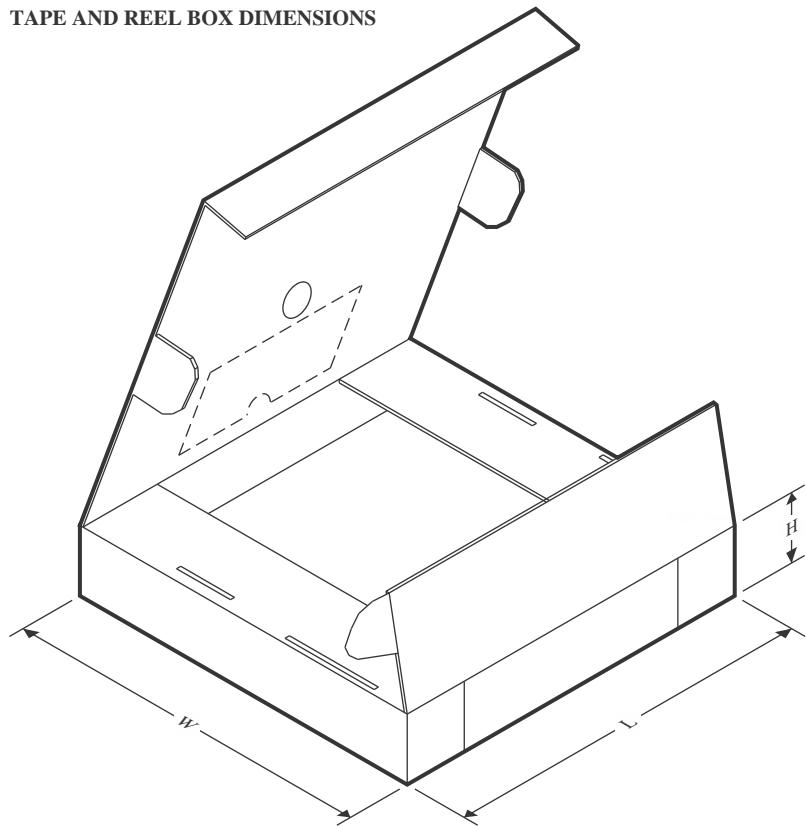
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXB0304RSVR	UQFN	RSV	16	3000	177.8	12.4	2.0	2.8	0.7	4.0	12.0	Q1
TXB0304RUTR	UQFN	RUT	12	3000	180.0	8.4	1.95	2.3	0.75	4.0	8.0	Q1
TXB0304RUTR	UQFN	RUT	12	3000	180.0	9.5	1.9	2.3	0.75	4.0	8.0	Q1
TXBN0304RSVR	UQFN	RSV	16	3000	177.8	12.4	2.0	2.8	0.7	4.0	12.0	Q1
TXBN0304RSVR	UQFN	RSV	16	3000	330.0	12.4	2.1	2.9	0.75	4.0	12.0	Q1
TXBN0304RUTR	UQFN	RUT	12	3000	180.0	8.4	1.95	2.3	0.75	4.0	8.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXB0304RSVR	UQFN	RSV	16	3000	202.0	201.0	28.0
TXB0304RUTR	UQFN	RUT	12	3000	202.0	201.0	28.0
TXB0304RUTR	UQFN	RUT	12	3000	184.0	184.0	19.0
TXBN0304RSVR	UQFN	RSV	16	3000	202.0	201.0	28.0
TXBN0304RSVR	UQFN	RSV	16	3000	184.0	184.0	19.0
TXBN0304RUTR	UQFN	RUT	12	3000	202.0	201.0	28.0

## GENERIC PACKAGE VIEW

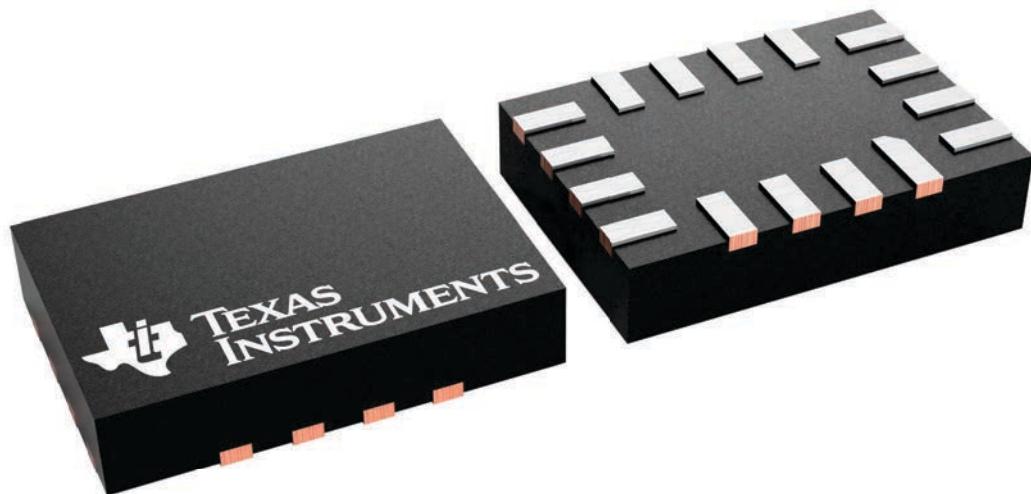
**RSV 16**

**UQFN - 0.55 mm max height**

**1.8 x 2.6, 0.4 mm pitch**

**ULTRA THIN QUAD FLATPACK - NO LEAD**

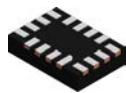
This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4231225/A

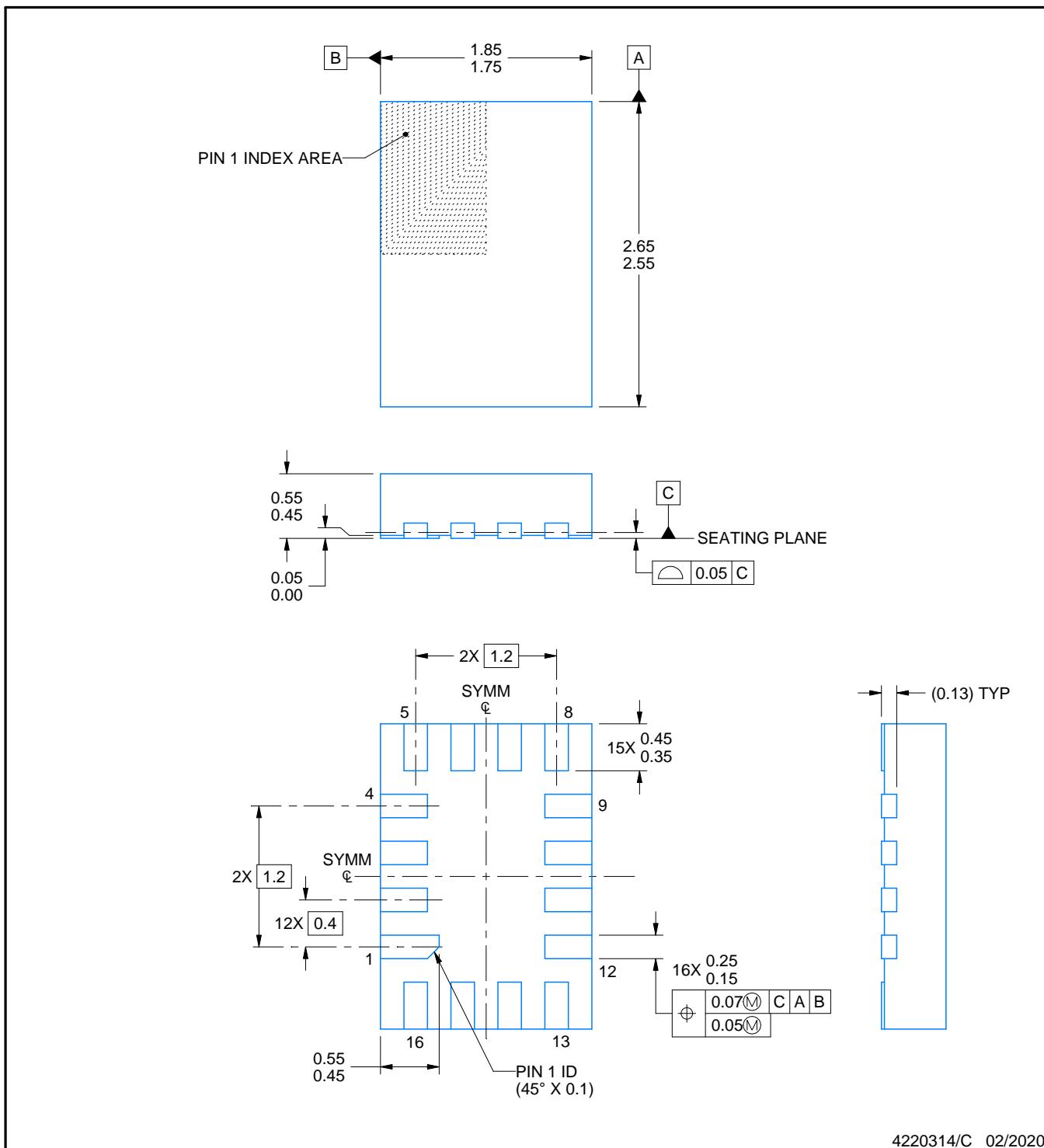
# PACKAGE OUTLINE

**RSV0016A**



**UQFN - 0.55 mm max height**

ULTRA THIN QUAD FLATPACK - NO LEAD



4220314/C 02/2020

**NOTES:**

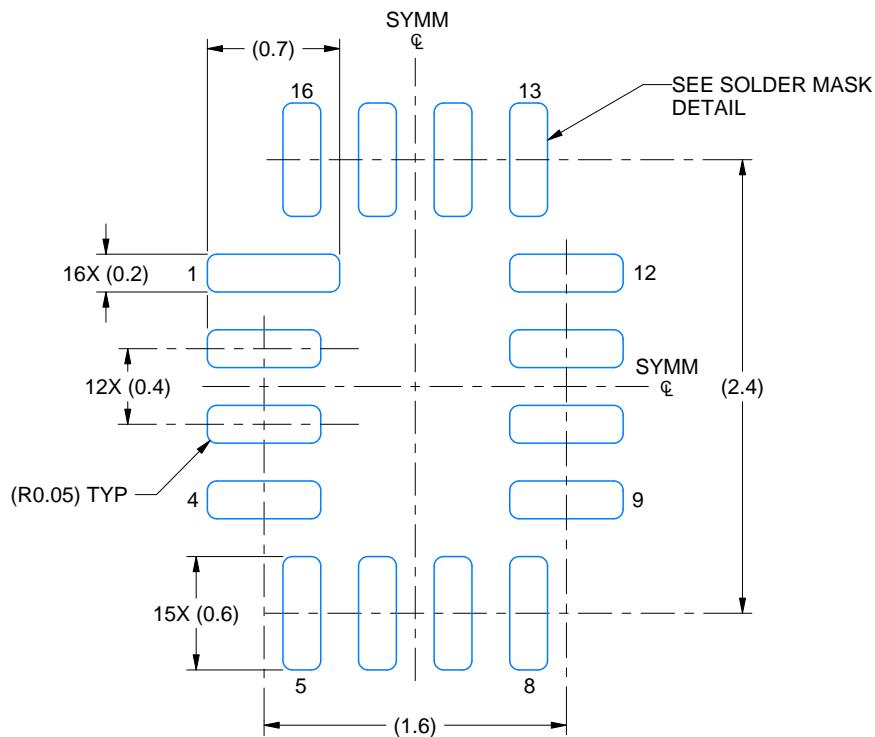
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

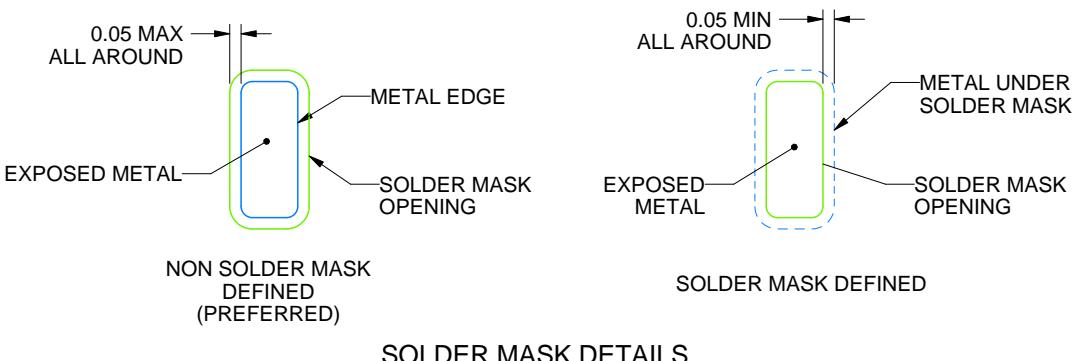
RSV0016A

UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 25X



SOLDER MASK DETAILS

4220314/C 02/2020

NOTES: (continued)

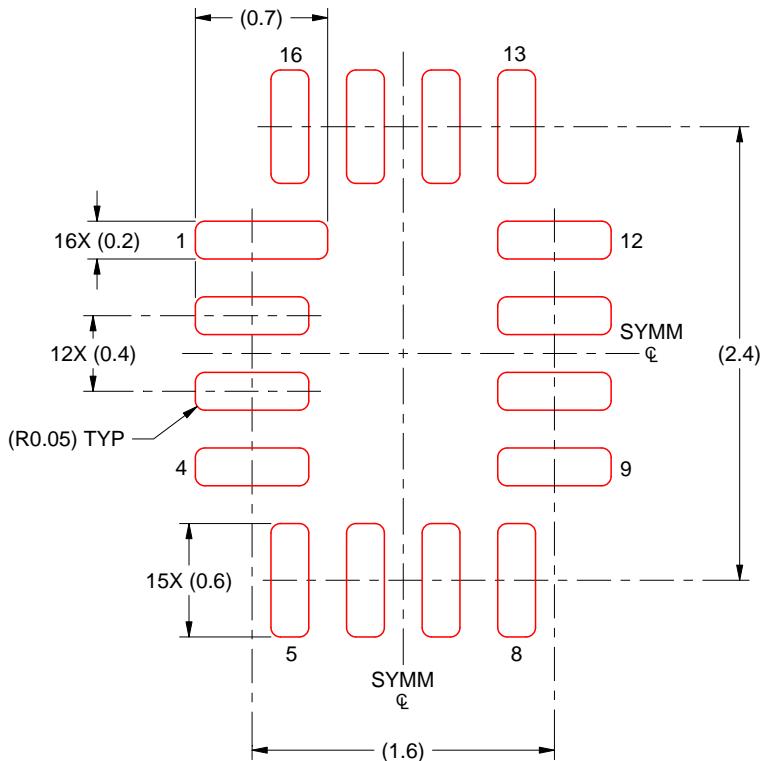
3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

RSV0016A

UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 25X

4220314/C 02/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

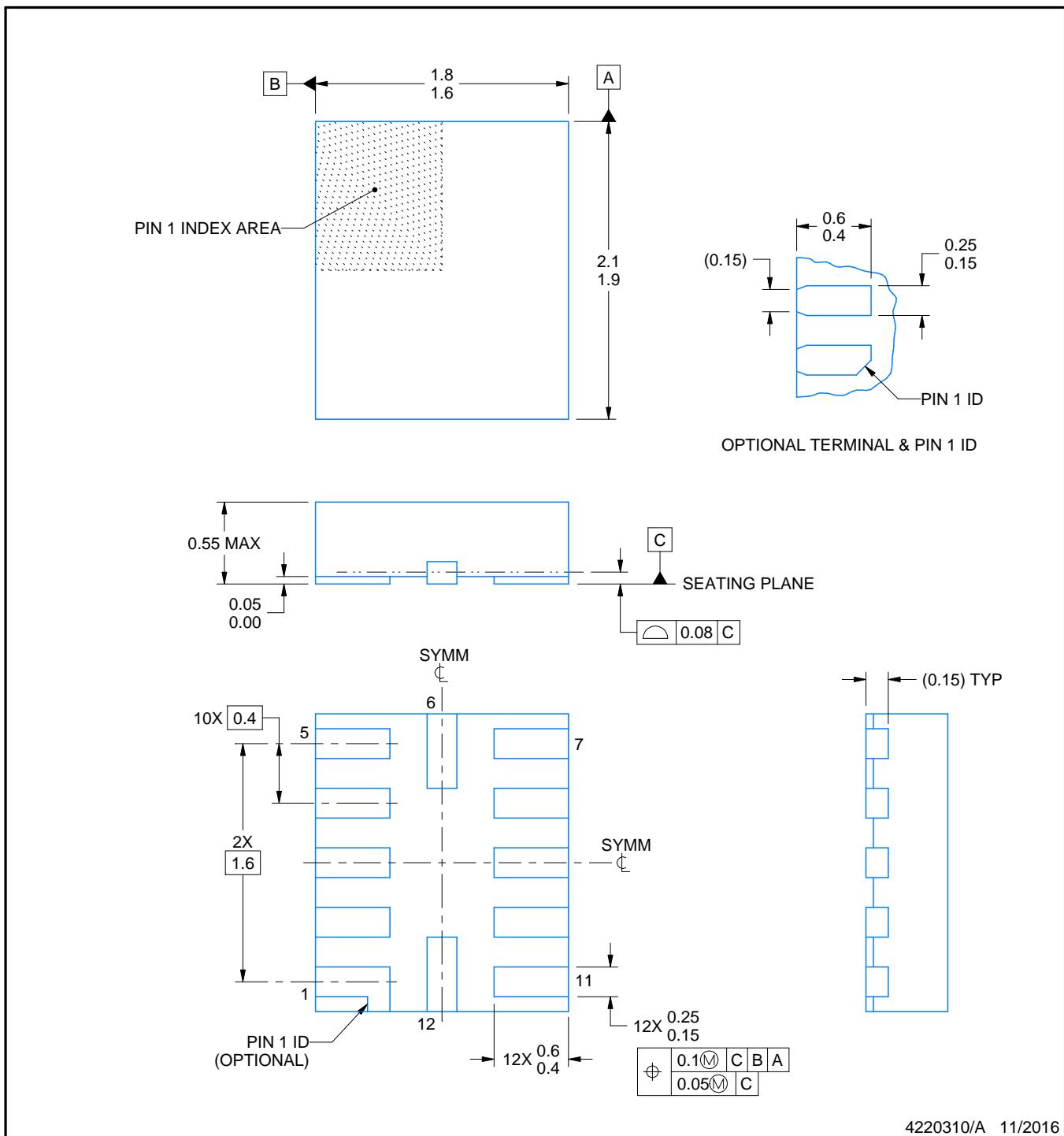
# PACKAGE OUTLINE

RUT0012A



**UQFN - 0.55 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



4220310/A 11/2016

## NOTES:

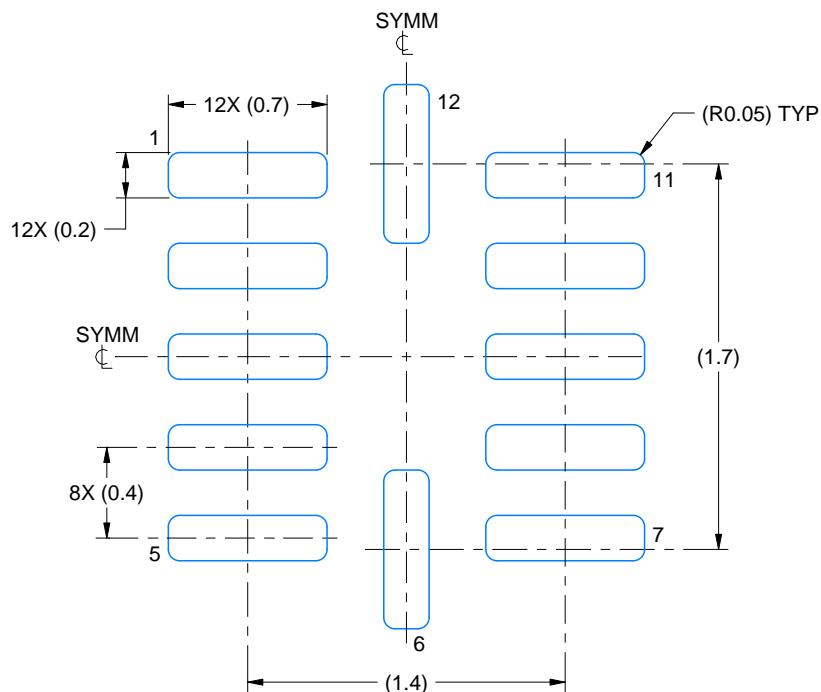
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2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

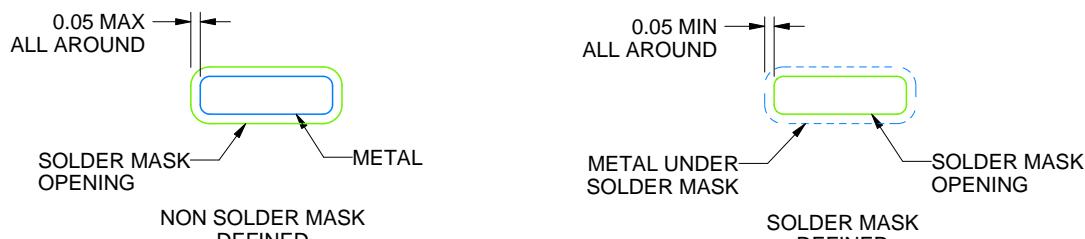
RUT0012A

UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:30X



SOLDER MASK DETAILS

4220310/A 11/2016

NOTES: (continued)

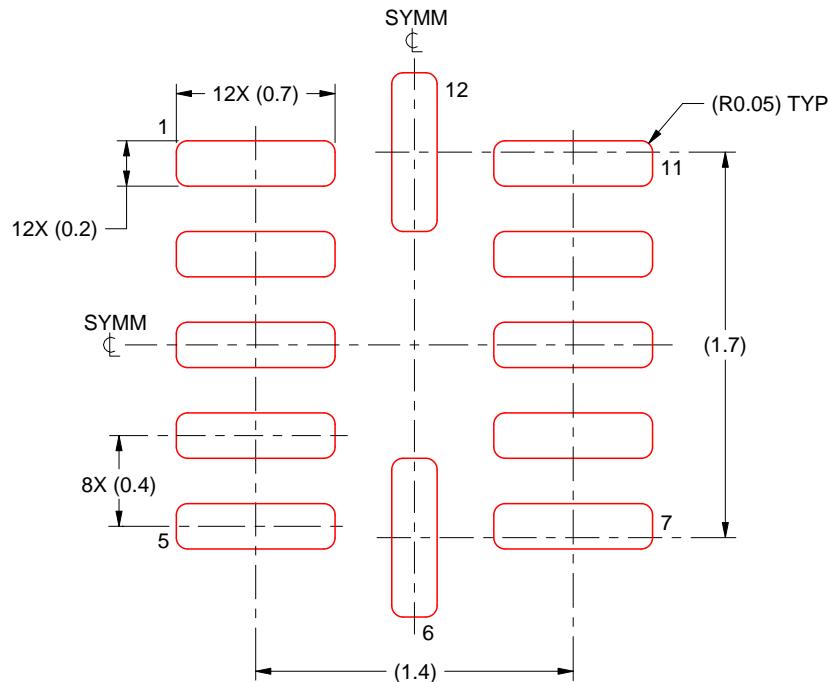
3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

RUT0012A

UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE: 30X

4220310/A 11/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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