Harshith Kantamneni

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Madison, Wisconsin – 53726, USA

M.S. ECE student specializing in ML-accelerated systems, embedded architecture, and CUDA optimization
Actively seeking full-time roles in: ML + Hardware, Embedded Systems, Computer Architecture, Accelerators

Education

University of Wisconsin-Madison — *Madison, USA*
M.S. in Electrical and Computer Engineering — Sep 2024 – Dec 2025

- Relevant Coursework: Advanced Computer Architecture 2, High Performance Computing, Machine Learning, Computer Architecture, Digital System Design

Vellore Institute of Technology — *Amaravati, India*
B.Tech in Electronics and Communication Engineering — Nov 2020 – May 2024

Projects

ML-Guided CUDA Kernel Configuration — Jan 2025 – May 2025
Python, PyTorch, CUDA — GitHub

- Built a PyTorch model to predict optimal CUDA launch configurations based on matrix size.
- Integrated predictions into kernel launcher achieving 30% speedup over static tuning.
- Benchmarked kernel performance using timing-based scripts across varied matrix sizes.
- Compared runtime vs. configurations to validate prediction accuracy and stability.

TDG Partition Size Prediction — Jan 2025 – May 2025
Python, XGBoost — GitHub

- Engineered TDG and matrix workload features to train XGBoost for predicting optimal partition sizes.
- Reduced configuration tuning time by 25% with sub-5% error vs. exhaustive search.
- Validated model generalization across 5+ workloads and runtime conditions.

5-Stage Pipelined RISC Processor — Aug 2024 – Dec 2024
Verilog, ModelSim

- Designed a pipelined WISC-F24 ISA processor with hazard detection and full forwarding logic.
- Achieved 100% instruction coverage using cycle-accurate ModelSim testbench.
- Simulated 10+ instruction sequences including control-flow and memory-access edge cases.

Knight's Tour FSM Design — Aug 2024 – Dec 2024
SystemVerilog, Quartus Prime, ModelSim

- Designed a pipelined FSM in Verilog to solve the Knight's Tour problem, achieving synthesis timing closure at 333 MHz on FPGA.
- Integrated UART and SPI interfaces to support Bluetooth-based Knight movement via mobile app control.
- Synthesized the RTL design in Quartus and reviewed resource usage to identify and reduce unnecessary logic.
- Verified functional and timing correctness through post-synthesis gate-level simulations using Synopsys Design Compiler.

Embedded CO/CO_2 Monitoring System — Aug 2024 – Dec 2024
FreeRTOS, C, PSoC 6, Altium Designer

- Developed an embedded home monitoring system using PSoC 6 for real-time sensor data acquisition and processing.
- Wrote custom I2C drivers for SCD-41 (CO_2) and MQ-7 (CO) sensors to enable reliable environmental data capture.
- Designed and assembled a 2-layer PCB to integrate PSoC, power, and sensors with minimal EMI and robust signal traces.
- Implemented Ethernet-based data transmission and logging for real-time monitoring of CO/CO_2 levels over network.

Experience

Society for Space Education, Research and Development — *Bengaluru, India*
Research Intern — Nov 2021 – Jan 2022

- Programmed ESP32 firmware for environmental telemetry and GPS data acquisition on balloon payload.
- Optimized startup sequence, reducing boot latency by 30%.

Skills

- **Languages:** C, C++, Python, Verilog, SystemVerilog
- **Tools:** ModelSim, Quartus, Altium Designer, MATLAB, Simulink, Git, Synopsis Design Compiler
- **Domains:** ML for Hardware, Embedded Systems, Computer Architecture, RTL Design, PCB Design, CUDA, OpenMP
- **Protocols:** I2C, SPI, UART, CAN, CAN FD, LIN, UDS, WiFi, Bluetooth

Achievements & Leadership

- **Team Lead – Communication Subsystem**, Students for Space Exploration and Development (2022–2023)
- **3rd Prize**, KRITAGYA National Hackathon 3.0 (2022–2023)