Harshith Kantamneni

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M.S. ECE student specializing in Computer Architecture, RTL Design, and High-Performance SoC Systems
Seeking full-time roles in: RTL Design, Processor Architecture, ASIC/FPGA Verification, and Performance Modeling

Skills

- **Languages:** Verilog, SystemVerilog, C, C++, Python
- **Tools:** ModelSim, Quartus, gem5, McPAT, MATLAB, Simulink, Git, Nsight
- **Domains:** Computer Architecture, RTL Design, SoC Performance Modeling, FPGA Prototyping, Fault-Tolerant Computing
- **Protocols:** I2C, SPI, UART, CAN, WiFi, Bluetooth

Education

University of Wisconsin-Madison — *Madison, USA*
M.S. in Electrical and Computer Engineering — Sep 2024 – Dec 2025

- Relevant Coursework: Computer Architecture, Advanced Computer Architecture II, High-Performance Computing, Digital System Design, Fault-Tolerant Computing, Machine Learning

Vellore Institute of Technology — *Amaravati, India*
B.Tech in Electronics and Communication Engineering — Nov 2020 – May 2024

Certifications

- **NVIDIA Deep Learning Institute (DLI) – Getting Started with Accelerated Computing using CUDA C++**, 2025

Hardware Design Projects

Architectural Performance Modeling using gem5 — Sep 2025 – Present
gem5, Python, McPAT

- Profiled and compared **TimingSimple**, **Minor**, and **O3 CPU** architectures in gem5 to evaluate performance, CPI, and energy efficiency.
- Executed and analyzed vector arithmetic workloads including **IAXPY, SAXPY, and DAXPY** to quantify instruction mix and cache/memory behavior.
- Automated simulation, metric extraction, and power estimation using Python, enabling scalable SoC-level performance exploration.
- Correlated architectural trends with RTL-level design trade-offs for SoC methodology development and validation.

5-Stage Pipelined RISC CPU Design — Aug 2024 – Dec 2024
Verilog, ModelSim

- Implemented a pipelined **WISC-F24 ISA** CPU with hazard detection, forwarding, and branch handling logic.
- Verified functionality using a cycle-accurate testbench achieving **100% instruction coverage**.
- Applied RTL design methodologies, modular verification, and waveform debugging in ModelSim.

FSM-Based Knight's Tour Solver — Aug 2024 – Dec 2024
SystemVerilog, Quartus, ModelSim

- Designed a pipelined FSM-based accelerator achieving **333 MHz timing closure** on FPGA for solving the Knight's Tour problem.
- Integrated UART/SPI interfaces enabling external communication and Bluetooth-based movement control.
- Performed **post-synthesis gate-level verification** to ensure timing and functional correctness.