# Harshith Kantamneni

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*M.S. ECE student specializing in Computer Architecture, RTL Design, and Fault-Tolerant Systems*
*Seeking full-time roles in: RTL Design, Processor Architecture, ASIC/FPGA Verification*

## Skills

- **Languages:** Verilog, SystemVerilog, C, C++, Python
- **Tools:** ModelSim, Quartus, gem5, MATLAB, Simulink, Git, Nsight
- **Domains:** Computer Architecture, RTL Design, FPGA Prototyping, Fault-Tolerant Computing
- **Protocols:** I2C, SPI, UART, CAN, WiFi, Bluetooth

## Education

**University of Wisconsin-Madison** — *Madison, USA*
*M.S. in Electrical and Computer Engineering* — Sep 2024 – Dec 2025

- Relevant Coursework: Advanced Computer Architecture II, Digital System Design, Fault-Tolerant Computing, High Performance Computing, Introduction to Artificial Neural Networks

**Vellore Institute of Technology** — *Amaravati, India*
*B.Tech in Electronics and Communication Engineering* — Nov 2020 – May 2024

## Certifications

- **NVIDIA Deep Learning Institute (DLI) – Getting Started with Accelerated Computing using CUDA C++**, 2025

## Projects

**5-Stage Pipelined RISC CPU Design** — Aug 2024 – Dec 2024
*Verilog, ModelSim*

- Implemented a pipelined WISC-F24 ISA CPU with hazard detection, forwarding, and branch handling logic.
- Verified functionality using cycle-accurate testbench achieving **100% instruction coverage**.
- Applied RTL design methodologies, modular verification, and waveform debugging in ModelSim.

**High-Performance FSM Accelerator (Knight's Tour)** — Aug 2024 – Dec 2024
*SystemVerilog, Quartus, ModelSim*

- Designed a pipelined FSM accelerator to solve Knight's Tour problem with **333 MHz timing closure** on FPGA.
- Integrated UART/SPI interfaces enabling external communication and Bluetooth-based movement control.
- Conducted **post-synthesis gate-level verification** ensuring timing/functional correctness.

**Smart $CO/CO_2$ Monitoring System** — Aug 2024 – Dec 2024
*FreeRTOS, C, PSoC 6, Altium Designer*

- Developed embedded monitoring system with real-time $CO/CO_2$ data acquisition and network logging.
- Implemented custom I2C drivers for SCD-41 ($CO_2$) and MQ-7 (CO) sensors ensuring accurate sampling.
- Designed and fabricated a 2-layer PCB with **EMI mitigation** and robust signal integrity.

## Experience

**Society for Space Education, Research and Development** — *Bengaluru, India*
*Research Intern* — Nov 2021 – Jan 2022

- Developed ESP32 firmware for telemetry and GPS, reducing boot latency by **30%**.
- Integrated sensor interfacing and startup optimization improving reliability in real-time systems.