

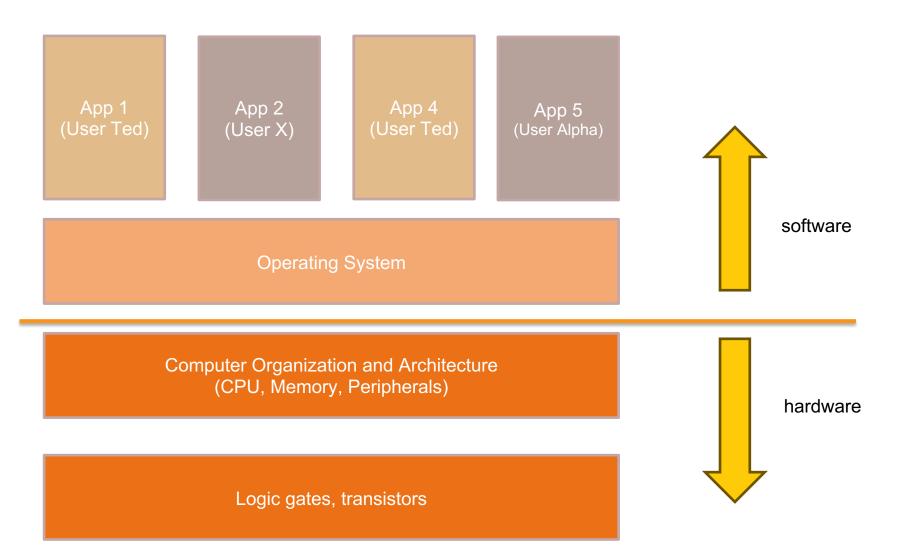
Computer Organization and Architecture (CS2600 and CS2610)

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The Compute Stack





The Compute Stack



App 1 User Ted) App 2 (User X)

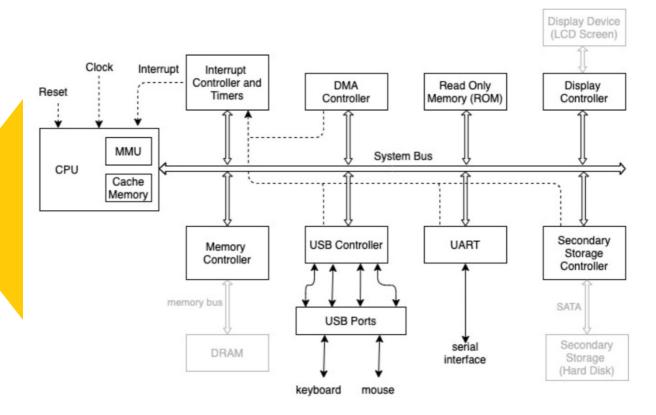
App 4 (User Ted)

App 5 (User Alpha)

Operating System

Computer Organization and Architecture (CPU, Memory, Peripherals)

Logic gates, transistors



The Wish List



Fast

Energy Efficient

Program support

Security and Protection

Multi-user systems

App 1 (User Ted) App 2 (User X) App 4 (User Ted)

App 5 (User Alpha)

Operating System

Computer Organization and Architecture (CPU, Memory, Peripherals)

Logic gates, transistors

Where does COA fit in the Compute Stack



App 1 User Ted) App 2 (User X)

App 4 (User Ted) App 5 (User Alpha)

Operating System

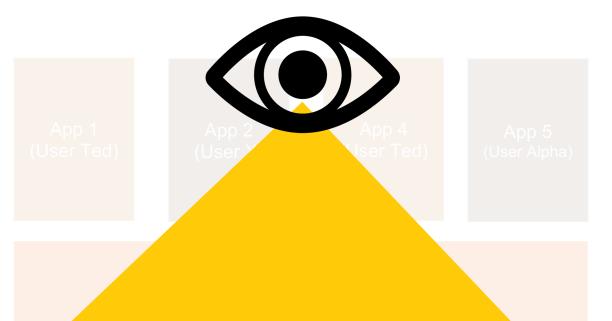
Computer Organization and Architecture (CPU, Memory, Peripherals)

The layer which converts the logic gates into modules that can be usable by software to achieve the wishlist

Logic gates, transistors

Computer Architecture





Aspects of the hardware visible from software.

An abstraction of the hardware

Computer Organization and Architecture (CPU, Memory, Peripherals)

Instruction Set Architecture (ISA) + Operating System Interface

Computer Organization





Aspects of the hardware not visible from software.

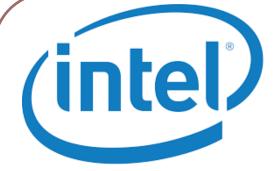
Internal working of the CPU that realizes the ISA.

Hardware (CPU, Memory, Peripherals)

Two processors can have the same ISA but different implementations of the architecture, with varying cost and performance.

Microprocessors





General Purpose













Application Specific

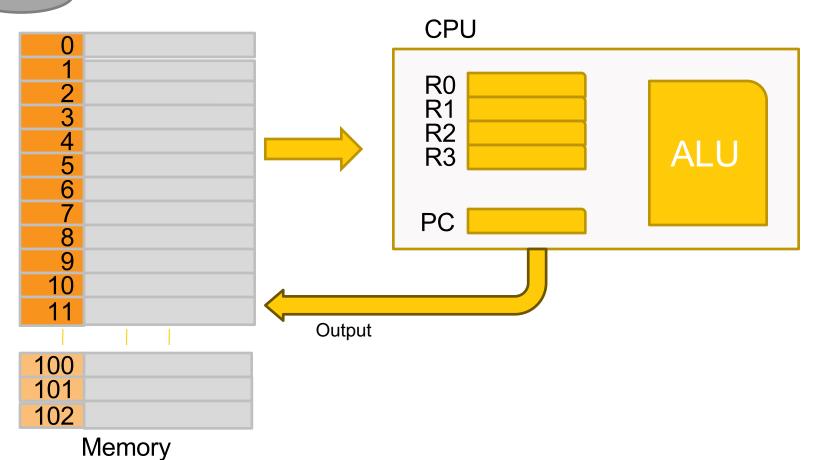
Many different processors, but underlying concept used is the same: Stored Program Concept

Stored Program Concept



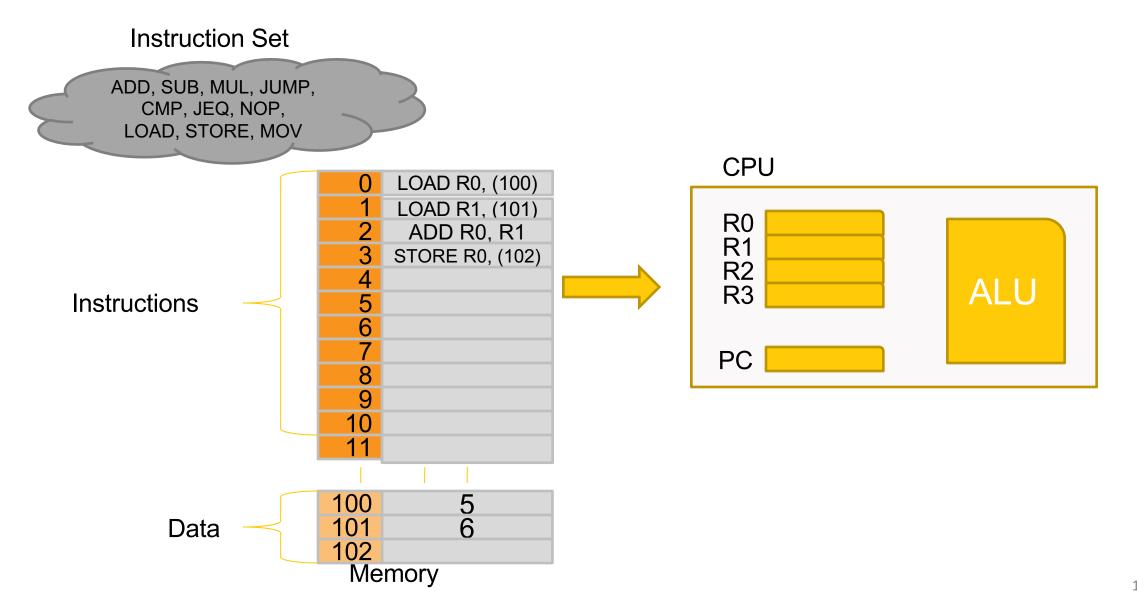
Instruction Set

ADD, SUB, MUL, JUMP, CMP, JEQ, NOP, LOAD, STORE, MOV



Stored Program Concept





This Course (theory and Lab)



- How does the processor support programming languages?
- How does the processor support operating systems?
- How to design a processor to improve speed and performance?
- How to design a processor to support multiple users with limited resources?
- Lab: Assembly coding, processor design / analysis



Logistics and Grading



Grading CS2600:

Quiz 1: 25 marks;

Quiz 2: 25 marks;

End Semester Exam: 40 marks

Tutorials: 10 marks

Grading CS2610

Based on ~8 assignments

LOGISTICS

The slides and assignments will be shared through Microsoft Teams (work or school).

Please create an account with your small ID and join this team.

Classes will be held from 17th Jan, 2024 in Slot C at CS15 (CSE, IITM). Labs will be in P slot

■ Monday: 10:00 - 10:50 AM

■ Tuesday: 9:00 - 9:50 AM

■ Wednesday: 8:00 - 8:50 AM

Friday: 1:00 - 1:50PM (Tutorials)

■ Labs: Monday 2:00 - 4:00 PM

Website

https://sites.google.com/cse.iitm.ac.in/cs2600-2024/home



Reference Books



