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Investigating the Impact of Single Event Burnout on Radiation Hardened Trench Shielded Power UMOSFET

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***Abstract*— Power metal-oxide-semiconductor field-effect transistors (MOSFETs) are the most important device for the space power systems which are expected to meet the requirements of radiation hardness and electrical performance at the same time. Thus, it is essential to investigate the hardening techniques to improve device radiation tolerance. This research proposes a radiation-hardened Trench Shielded Power U-shape MOSFET (TS-UMOSFET). The structure comprises of added n-region surrounding the P^+ shielding region under the trench bottom and inclusive of a buffer layer between drift layer and substrate. With SILVACO ATLAS software, the TS-UMOSFET is investigated to prove that the addition of n-region spreads out the electrons to the downward direction and the device to be more resistant for radiation environment. In addition, this study also presents two-dimensional numerical simulation results, which investigates the impact of single-event burnout (SEB) on electrical characteristics, triggering criteria and SEB threshold voltage. The simulation results show that the SEB performance improved for hardened TS-UMOSFET structure compared to a standard structure, even at high linear energy transfer (LET) value.**

***Index Terms*— Single-Event Burnout (SEB), Power MOSFET, Radiation Hardening, Electric field, Linear Energy Transfer (LET)**

I. Introduction

POWER MOSFETs are essential components of power supply, which are widely used in space and atmospheric applications. However, its reliability is limited by the space radiation environment, which is composed of heavy energetic particles such as galactic cosmic rays, heavy ions, and solar flares [1], [2]. Total Ionizing Dose (TID) and Single-Event Effects (SEE) are the main destructive effects that capable of causing significant damage to the device. SEEs are further classified into Single-Event Burnout (SEB) and Single-Event Gate Rupture (SEGR); SEB is a major catastrophic failure mode on power MOSFET device; it's mainly dependent on the inherent parasitic BJT in the MOSFET structure [3], [4]. A heavy-ion deposits charge along its ions track passing through the power MOSFET when biased in its OFF state. The deposited charge leads to turning ON the parasitic BJT and creates carrier multiplication. In trench gate power MOSFET devices, the electric field at the corner of the trench bottom increases that results in the high level of currents which causes the device to burnout by melting down the substrate [5]. Therefore, suppression of the electric field density and the activity of parasitic BJT turn out to be the primary design concerns in structure enhancement.

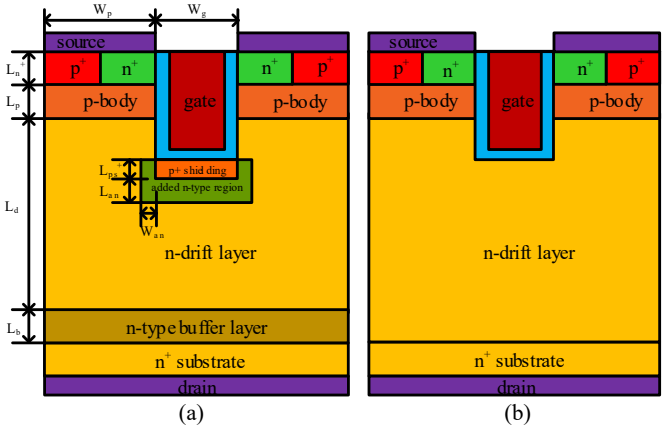

Fig. 1: Schematic Diagram of (a) hardened Power TS-UMOSFET (b) standard Power UMOSFET

Many technical methods to improve the SEE survivability of power Vertical Double Diffused Metal Oxide Semiconductor Field Effect Transistor (VDMOSFET) have been extensively investigated was given in [6]–[10]. It's been proved that the addition of a buffer layer is an efficient way to improve the SEB performance of the device. However, the high resistivity thickness of constant buffer layer dominates the on-state resistance and degrades the performance of the device. Thus, to overcome this issue, Jia et al. presented the N-type linear buffer layer which was offered with doping linear concentration distribution [11]. Then, the triggering criteria and sensitive volume for SEB performance of power VDMOSFETs have been defined in [12], [13]. Low Carrier Lifetime Control Region (LCLCR) has been introduced in VDMOSFET for the SEB hardening and removing poly gate region, increase the oxide thickness by the local oxidation of silicon (LOCOS)

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for SEGR hardening also given in [14]. Another hardening technique proposed by Lu et al, the elimination of P-well region below the N+ source influences the SEB performance [15]. Recently, both SEB and SEGR hardening for VDMOS by addition of Double Stagger Partial Silicon-On-Insulator (DSPSOI) layers to the device [16] has been considered. This device increases the SOA but drops the overall specific ON-resistance. On the other hand, the authors Mo et al. and Wan et al. motivated on different high-k dielectric material for an inner dielectric layer (ILD) and passivation layer design for TID and SEB hardening [17].

Besides, the potential hardening solution [18]–[20] of buffer layer technology is extended to UMOSFET in alternative structural configurations such as Schottky diode, power trench Accumulation-Mode Field Effect Transistor (ACCUFET) and Double Channel Split-Gate Enhanced (DSGE)-UMOS. Further, several hardening solutions have been suggested, such as the UMOSFET with modified p+ plug geometry, carrier lifetime and emitter doping effects, Schottky source, enhanced split gate trench structure and replacement of gate oxide with high-k gate dielectrics [21]–[23]. By using these structures, SEE effects can be reduced to some extent and the device performance have been increased successfully. However, the electric field increases near the corner of the trench gate due to the presence of a sensitive region in the previous structures, the impact factor in SEB performance remains dominant [24]–[26].

In this work, the SEB hardened power TS-UMOSFET with an added n-type region to cover the P^+ shielded region at the bottom of the trench was proposed. In addition, the SEB triggering mechanism and performance of SEB on hardened power TS-UMOSFET is investigated. Furthermore, the impact of insertion of n-buffer layer was explored for understanding the hardening mechanism. Two-dimensional SEB simulation results for the TS-UMOSFET and UMOSFET are performed using Silvaco ATLAS simulator to compare the parameter characteristics. Additionally, the SEB performance is investigated by analyzing the inner physical behavior, a critical value of LET and safe operating voltage of the device during heavy-ion radiation.

II. Device descriptions and simulation setup

A. Device structure

The power UMOSFET structure offered a reduced internal resistance by removal of a JFET region within the VD-MOSFET structure, it also increased the operating frequency. Fig. 1 illustrates the schematic diagram of the standard power UMOSFET and hardened TS-UMOSFET with breakdown voltage of $70V$ [22]. The device's unit cell width is $3.0\mu m$ and the channel length is considered as $0.4\mu m$. The epitaxial layer thickness is $2.5\mu m$ with a concentration of $5.6 \times 10^{14} cm^{-3}$ grown on the silicon substrate with a doping concentration of $1.0 \times 10^{19} cm^{-3}$. Then, to form a p-base region a boron implanted into the drift region with a depth of $0.6\mu m$ and the doping concentration of $1.7 \times 10^{17} cm^{-3}$. A highly doped p^+ region diffused within the p-well with a junction depth of $0.2\mu m$ and a surface concentration of $2.0 \times 10^{19} cm^{-3}$. A highly doped phosphorous well diffused to form a n^+ source region with a depth of $0.2\mu m$ and a doping concentration of $1.0 \times 10^{19} cm^{-3}$.

TABLE I: DEVICE PARAMETERS FOR SIMULATION

Device Parameter	Value for standard UMOS	Value for hardened UMOS
Trench width (W_g)	$0.5\mu m$	$0.5\mu m$
Mesa width (W_p)	$1\mu m$	$1\mu m$
Trench depth	$1\mu m$	$1\mu m$
Gate oxide thickness	$0.05nm$	$0.05nm$
P^+ shielded thickness	-	$0.1\mu m$
n region thickness (L_{an})	-	$0.1\mu m$
n region width (W_{an})	-	$0.25\mu m$
P^+ source depth	$0.2\mu m$	$0.2\mu m$
N^+ source depth	$0.2\mu m$	$0.2\mu m$
P-base region depth	$0.6\mu m$	$0.5\mu m$
Drift region thickness	$2.5\mu m$	$2.4\mu m$
Buffer Layer thickness	-	$1.0\mu m$
P^+ source doping	$2.0 \times 10^{19} cm^{-3}$	$2.0 \times 10^{19} cm^{-3}$
N^+ source doping	$1.0 \times 10^{19} cm^{-3}$	$1.0 \times 10^{19} cm^{-3}$
n region doping	-	$6.0 \times 10^{16} cm^{-3}$
P^+ shielded doping	-	$1.0 \times 10^{18} cm^{-3}$
P-base region doping	$1.7 \times 10^{17} cm^{-3}$	$1.7 \times 10^{17} cm^{-3}$
Buffer Layer doping	-	$5.6 \times 10^{16} cm^{-3}$
Drain region doping	$5.6 \times 10^{14} cm^{-3}$	$5.6 \times 10^{14} cm^{-3}$
Substrate doping	$1.0 \times 10^{19} cm^{-3}$	$1.0 \times 10^{19} cm^{-3}$

In contrast to standard UMOSFET, the SEB hardened TS-UMOSFET additionally includes a P^+ shielding region under the bottom of trench gate and added n-region surrounding the shielding layer, inserted buffer layer in the drift region. In this structure, during the heavy ion strike the gate oxide layer will be protected by P^+ shielding region. However, this increases the ON-resistance. To overcome this, the n-type doped region is incorporated to reduce the electric field near the trench corner by spreading out the electrons in a downward direction. The thickness of P+ shielding and n-region are set to 0.1 and $0.2\mu m$, respectively. Besides, the doping concentration of the layers are $1.0 \times 10^{19} cm^{-3}$ and $6.0 \times 10^{16} cm^{-3}$. In addition, the n-buffer layer is included to enhance the SEB performance [26]. The thickness of the drift region is reduced from 2.5 to $2.4\mu m$ in order to insert the buffer layer. In order to reduce the electric field without changing the breakdown voltage, the thickness and doping concentrations of buffer layers have been optimized. The thickness of buffer layer varied from 0.6 to $1.0\mu m$ and doping concentration is set to $5.6 \times 10^{16} cm^{-3}$ respectively. The device parameters used for design simulation are summarized in Table I.

The simulations are conducted using Silvaco ATLAS device simulator's two-dimensional numerical simulations. The essential physical models covered in simulations are classified into mobility, recombination, carrier statistics and impact ionization model. The mobility models inclusive of FLDMOD for electric field dependencies and Caughey-Thomas ANALYTIC model is for calculating concentration and temperature. Recombination models employed with ShockleyReadHall (SRH), concentration-dependent carrier lifetimes (CONSRH) is recommended for silicon material and Auger recombination for high current densities. Carrier statistics model contains Fermi Dirac and Band-gap narrowing model (BGN), since heavily doped regions existence in the structure. In addition, impact

ionization model is utilized to calculate the ionization rates and Selberherr model is used for the blocking characteristics simulation [27].

While performing radiation experiments, the LET describes the total energy lost per path length by a charged particle, which can be given in units of $MeV/mg/cm^2$. In the simulations, the LET is usually described as the deposited charge per unit length of the track and expressed in $pC/\mu m$. The conversion formula from $MeV/mg/cm^2$ to $pC/\mu m$ is given in the equation 1.

$$\frac{Q}{W_{ehp}} \times LET(MeV/mg/cm^2) \times \rho = LET(pC/\mu m) \quad (1)$$

where, W_{ehp} is the average energy required to produce a electron-hole pair in silicon (Si) is $3.6eV$, the ρ is the density of the silicon material is $2.33g/cm^3$ and Q denotes the charge of an electron $(1.6 \times 10^{-19}C)$. Hence, for the silicon material the simplified results is $1pC/\mu m = 97MeV/(mg/cm^2)$. The temperature of 300 K was chosen for simulation of the SEB analysis and basic electrical characterisation [18]–[21], [23].

To investigate the SEB performance, a simplified heavy-ion model is additionally included using the $SINGLEEVENTUPSET$ statement. To simulate an ionizing impact within a structure, a function that generates the electron-hole pairs at the vertical direction in a specific area has to be defined and can be computed in equation 2.

$$G(r,l,t) = G_{LET}(l) * S(r,l) * T(t) \quad (2)$$

where, $S(r,l)$ and $T(t)$ are functions describing the spatial and temporal variations of the generation rate. $G_{LET}(l)$ is the LET generation density relating to the LET $(pC/\mu m)$ of the ions [28]. For this research simulation, the track radius of the spatial Gaussian function ω is set to $0.05\mu m$, the initial time T_0 of the charge generation is fixed to $4 \times 10^{-12}s$ and the temporal gaussian function width T_C is set to $2 \times 10^{-12}s$. The ion track information is specified by an entrypoint and exitpoint locations (x_0, y_0, z_0) and (x_1, y_1, z_1) respectively. For the 2-dimensional simulation, z_0 and z_1 assumed to be negligible. The incident position of ion x_0 and x_1 are varied for different locations such as 0, 0.7, 1.25 to identify the sensitive position. Heavy ion track is assumed to penetrate in perpendicular direction, for that y_0, y_1 coordinates are set to 0 and 4.3 respectively. The desirable LET values used in the simulation is 0.6 $pC/\mu m$, which correspond to $60.0MeV/mg/cm^2$ for heavy ion beam Iodine(I) $(Z = 53)$, depending on the conversion factor of 0.0097.

B. Device parameter characteristics

The basic electrical characteristics of power UMOSFET before the heavy ion radiation was characterized as shown in Fig. 2 to identify the gate threshold voltage, breakdown voltage, drain current, leakage current and capacitances. The transfer characteristics of UMOSFET and TS-UMOSFET devices are compared as shown in Fig. 2a. From the graph, the threshold voltage was identified as 2.6 V and it can also be seen that drive current slightly higher for hardened TS-UMOSFET because of the specific resistance R_s is lower in the buffer layer. The breakdown characteristics for both structures have been shown in Fig. 2b, it can been seen that breakdown voltage of the hardened structure is reduced for minimum percentage but with better threshold voltage. The IV characteristics for positive drain currents at $V_{GS} = 4$, 5, 6 and $7V$ are shown in Fig. 2c. It clearly shows that the transconductance is similar but the resistance is slightly higher for the conventional structure. In order to increase the SEB threshold voltage of hardened structure, a lot of geometrical modifications need to be carried out, this will degrade the current handling capability of the device. Nevertheless, the SEB hardened mechanism of trench shielding is not affected by current handling capability.

TABLE II: SENSITIVE POSITION DETERMINATION

Position	V_{ds}				
	30	40	50	65	68
(a)	✗	✓	✓	✓	✓
(b)	✗	✗	✓	✓	✓
(c)	✗	✗	✗	✓	✓

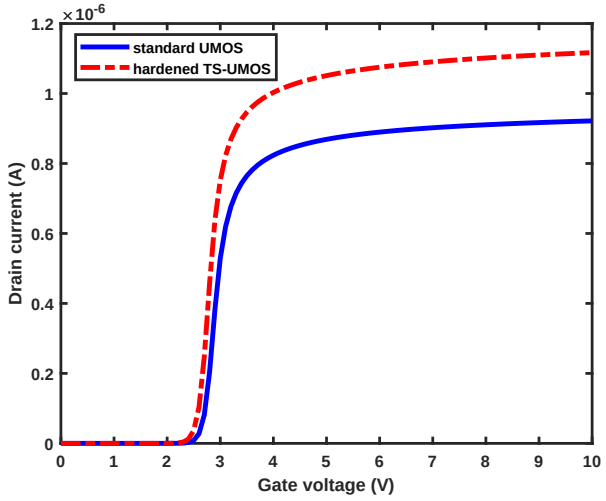
* ✓SEB effect is present, ✗SEB effect is absent

The negative drain current characteristics have been characterized at bias voltage $V_{GS} = -4V$ as shown in Fig. 2d. The value of the negative drain current for the hardened device increases to about $12\mu A$ compared to standard device's $8\mu A$. The dynamic characteristics of standard and hardened power MOSFETs are shown in Fig. 2e. It is found that the input (Ciss), reference (Crss) and output (Coss) capacitances are showing similar trends for the hardened structure as compared to the standard one. The fundamental electrical characteristics of the two structures are found to be almost the same.

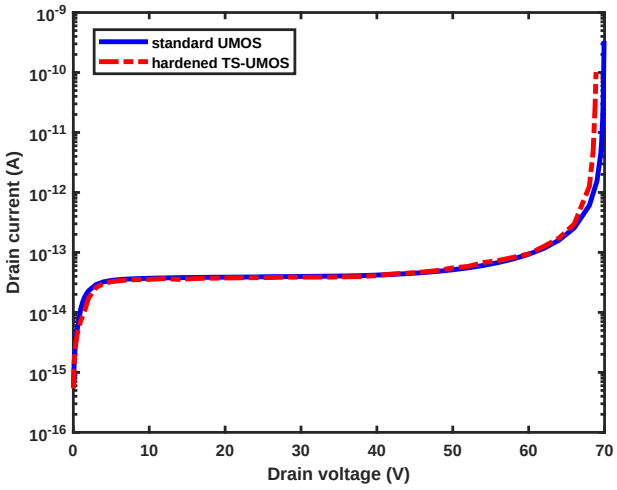
III. SEB Simulation Results and Discussion

The SEB performance has been extensively investigated using the heavy-ion strike model for the variable drain to source voltage while the gate voltage is kept constant at 0V (device biased at OFF-state). The position of the ion strike is defined by the entry and exit points of x and y directions respectively. When the power MOSFET is biased at off-state condition, the energetic ion strikes on the structure will cause SEB by triggering the parasitic bipolar transistor. To investigate the SEB triggering mechanism, it is essential to find the most vulnerable heavy ion strike position where the device is affected more compared to other strike positions. The most sensitive position of SEB for both the conventional and proposed UMOSFET and TS-UMOSFET are investigated respectively through simulation as shown in Fig. 3. In the simulation, the heavy ion having the LET= $0.6pC/\mu m$ at a different incident, the transient drain performance is investigated for several drain bias voltages. Table I summarizes the results, where the presence and absence of SEB are denoted by ✓and ✗.

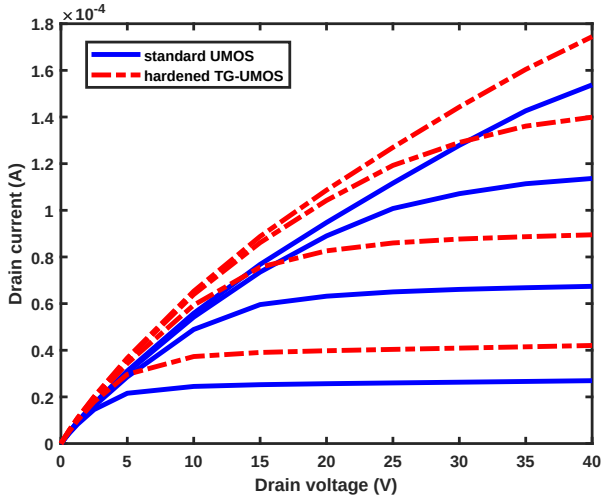
The most sensitive positions for both UMOSFET and TS-UMOSFET are at position (a), due to the high field region



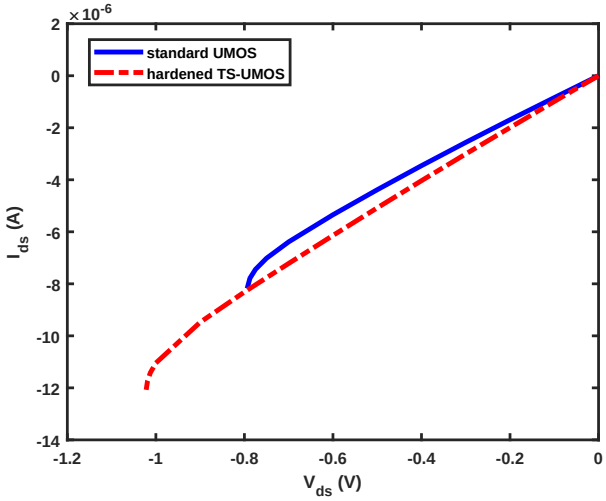
(a) Transfer characteristics



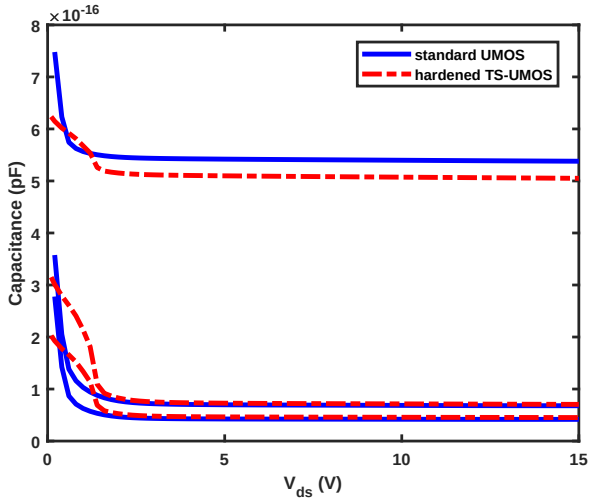
(b) Breakdown chararcteristics



(c) I-V characteristics for positive drain current



(d) I-V characteristics for negative drain current



(e) The input (Ciss), reference (Crss) and output (Coss) capacitances

Fig. 2: The basic electrical characteristics of standard power UMOSFET and hardened power TS-UMOSFET

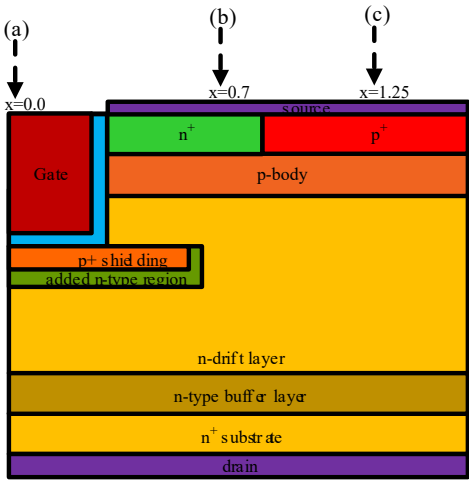


Fig. 3: Simulation of half-cell device structure for heavy ion strikes at different position

TABLE III: SEB SIMULATION RESULTS WITH DIFFERENT LET VALUES

LET (pC/μm)	V_{ds} 30	40	45	50	55	60	65	68
0.1	✗	✗	✗	✗	✗	✗	✗	✓
0.3	✗	✗	✗	✗	✗	✗	✗	✓
0.4	✗	✗	✗	✗	✗	✗	✗	✓
0.6	✗	✓	✓	✓	✓	✓	✓	✓
0.9	✗	✓	✓	✓	✓	✓	✓	✓

* ✓SEB effect is present, ✗SEB effect is absent

existing near the gate field plate between the gate and the drain. The high field accelerates more carriers, which triggers SEB. Then, the impact of different LETs was simulated under various drain bias voltages. The SEB threshold voltage is 40 V. With the increase in LET after $0.6pC/\mu m$, the occurrence of SEB is not sensitive. In this research, further analyses of the SEB influence on the device is chosen as the LET value is $0.6pC/\mu m$ and ions track position (a) which is $x_0 = 0\mu m$.

To better understanding of the SEB triggering mechanism inside the physical structure, the evolution of the holes concentration inside the structure after an ion's strike at time 150ps and 1 ns was extracted for a drain voltage of 40V at a LET= $0.6pC/\mu m$ as shown in Fig. 4. The hole concentration distribution after an ions strike with respect to time will decide the occurrence of the SEB. It confirms that the hole concentration at t=150ps for the conventional structure reaches the substrate and causes a SEB. On the contrary, the hole

TABLE IV: INVESTIGATION OF SEB THRESHOLD VOLTAGES OF POWER UMOSFETS AT ($LET = 0.6pC/\mu m$)

Type		V_{ds} supply (V) 40	50	55	60	65	68
Conventional UMOSFET		✓	✓	✓	✓	✓	✓
Hardened TS-UMOSFET with different buffer layer thickness	0.6	✗	✗	✓	✓	✓	✓
	0.7	✗	✗	✗	✗	✓	✓
	1.0	✗	✗	✗	✗	✗	✓

* ✓SEB effect is present, ✗SEB effect is absent

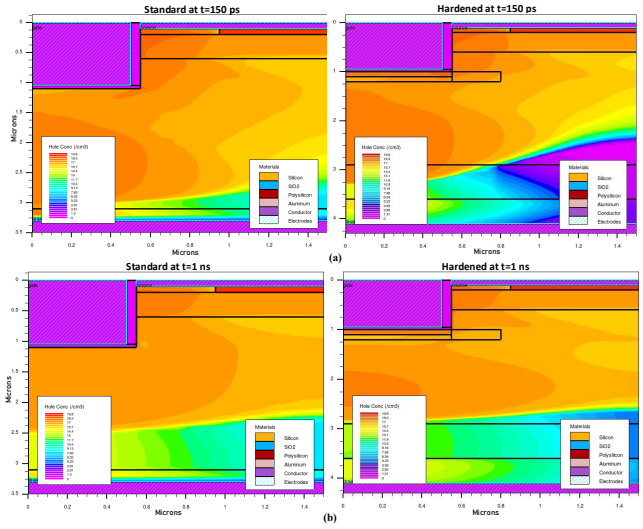


Fig. 4: Hole concentrations of standard (left) and hardened (right) power UMOSFET at (a) t=150 ps (b) t=1 ns after an ion's strike at $LET = 0.6pC/\mu m$

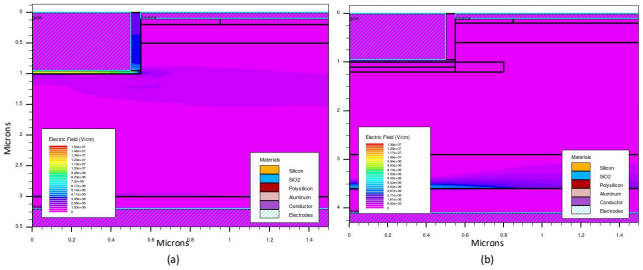
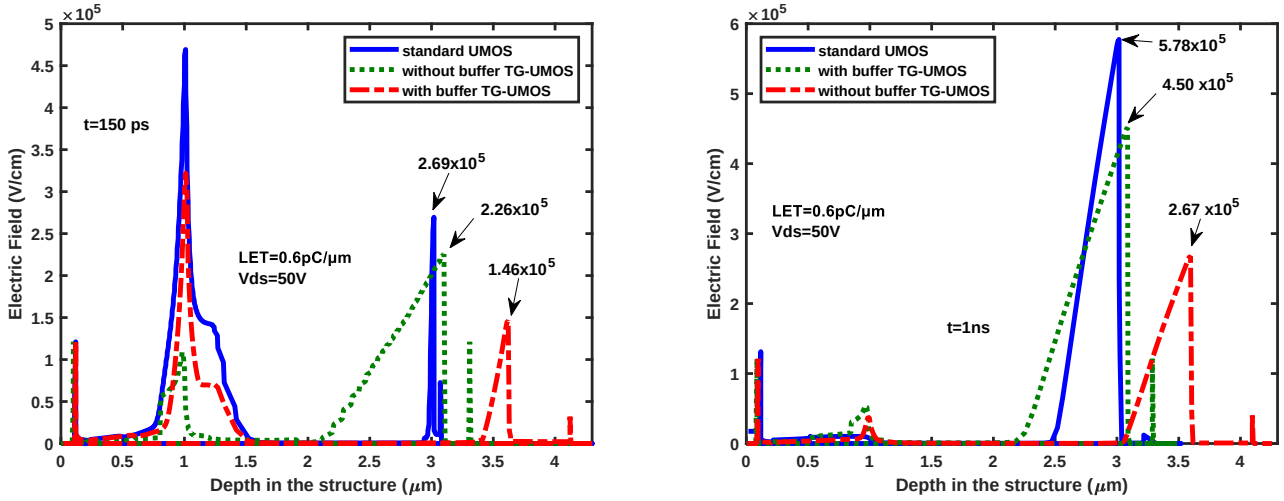


Fig. 5: Electric field density inside the structure of (a) standard and (b) hardened power UMOSFET at t=150 ps after an ion's strike at $LET = 0.6pC/\mu m$

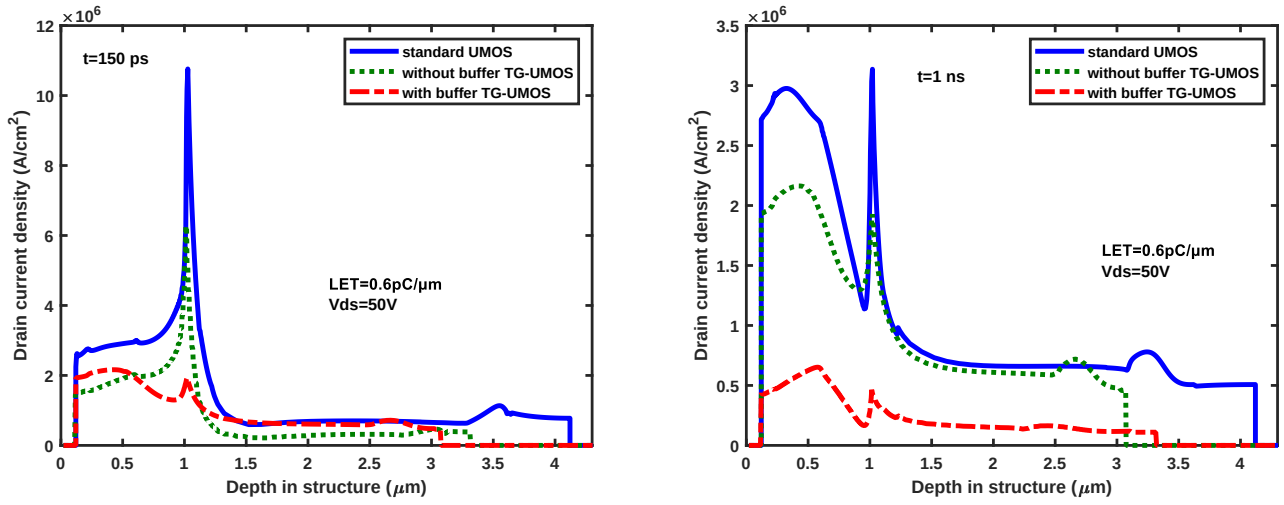
concentration decreases to a very low level at the substrate because of the buffer layer. The simulation results also clearly show that the holes concentration of hardened TS-UMOSFET (right) (a, b) decreases with the holes collection effect of buffer layer and distribution of electrons by the n-type region at the bottom of the trench when compared with the standard UMOSFET.

Another physical influence of the heavy ions strike is electric field distribution inside the structure, which is compared for conventional and proposed structure in Fig. 5. It can be observed that higher electric field was present in the trench corner of conventional structure. In the hardened structure, the shielding prevents the electric field and leak out at the buffer layer. Fig. 6a compares the electric field distributions of a TS-UMOSFET with and without the buffer layer under $V_{DS} = 50V$ after ion's strike at $t = 150ps$. The peak electric field of the standard UMOSFET reaches the value of $2.69\times10^5 V/cm$, when for TS-UMOSFET is $2.26\times10^5 V/cm$. However, the electric field in the drift layer of the hardened TS-UMOSFET is lowered at $1.46 \times 10^5 V/cm$, because the elevated distribution of electric fields spreads over the buffer



(a) t=150 ps (b) t=1 ns

Fig. 6: Electric Field distributions of standard and hardened UMOSFET after an ions strike



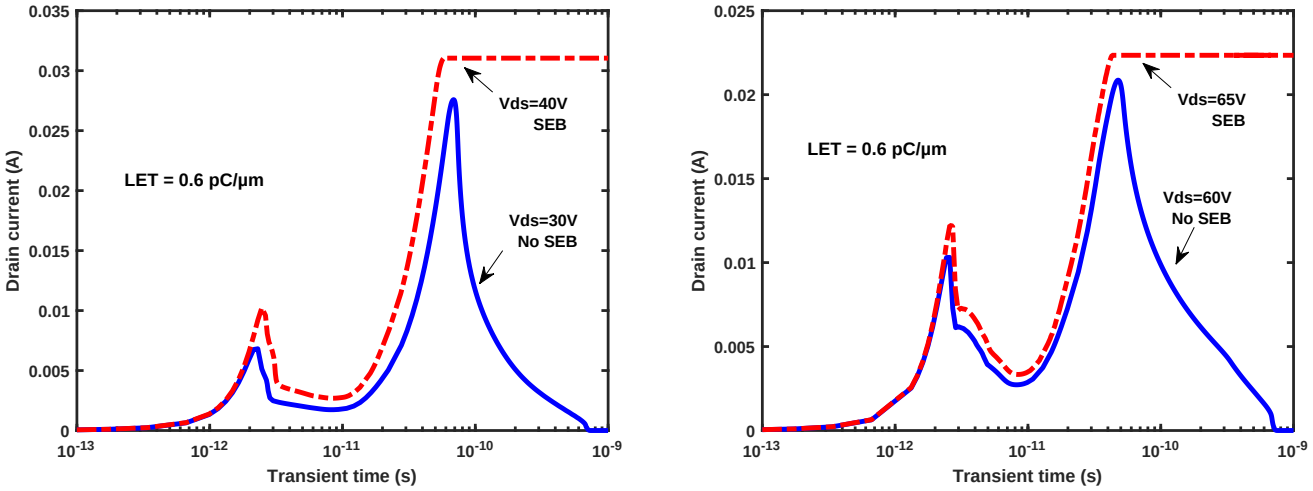
(a) t=150 ps (b) t=1 ns

Fig. 7: Total current density contours inside the structure after an ions strike

layer enabling this unit to support greater voltages than the device without a buffer layer. Electric field distributions of standard UMOS and hardened TS-UMOS at $t = 1ns$ after an ions strike was given in Fig. 6b It is observed that the high electric field reaches a peak value of $5.78 \times 10^5 V/cm$ compared to $4.50 \times 10^5 V/cm$ for TS-UMOS without buffer layer and $2.67 \times 10^5 V/cm$ with buffer layer. The peak electric field is directly proportional to the impact ionization coefficient, which is related to SEB sensitivity. Reducing the peak electric field will improve the SEB performance. Hence, the hardened structure ionization coefficients are relatively low. Lower electric field makes the device less sensitive to SEB.

The total current density distribution of the standard structure and the hardened structure for the case of ion's strike after $t = 150ps$ and $t = 1ns$ has been shown in Fig. 7a and Fig. 7b. As observed from the results, total current density for the TS-UMOS with buffer layer at the corner of the trench reduces for a great extent as compared to the conventional structure. It is seen that the added n-doped region which wraps the p+ shielding and the addition of buffer layer prevents SEB.

One of the main indexes to characterize the devices SEB performance is drain SEB threshold voltage. Table IV gives the summarized SEB threshold voltage simulation results of devices for different biased voltages. It includes, conventional power UMOSFET and hardened TS-UMOSFET with three different buffer layer thickness of 0.6, 0.7 and 1.0. It can be seen that if the thickness of the buffer layer increased, SEB threshold value also increased. It is a necessity to choose an optimal buffer value to prevent a higher on resistance. Hence, for the hardened structure, the thickness is chosen as 0.7 to obtain an optimum SEB threshold value and ON-resistance. Fig. 8a and 8b represent the drain currents for both



(a) Standard power UMOSFET (b) Hardened power TS-UMOSFET

Fig. 8: Analysis of drain current versus time under different drain voltages after an ion strike $(LET = 0.6pC/\mu m)$

UMOSFET and TSMOSFET at different biased conditions after the ion strike with the LET of $0.6pC/\mu m$. For the conventional MOSFET, SEB occurs when the drain voltage is 40 V, but no SEB happens at 30 V. For the proposed structure, SEB threshold voltage is 65 V, but no SEB happens at 60 V. Even at the critical LET value, the proposed structure shows a greater SEB threshold voltage. Therefore, the SEB behaviour associated with high-electric fieldwork at the trench corner in the proposed structure can be decreased to a certain degree.

IV. Conclusion

The impact of single-event burnout effects on trench shielded power UMOSFET device is investigated with a two-dimensional simulator, SILVACO ATLAS. The added n-type region that covers the p+ shielded region at the bottom of the trench corner reduces the electric field and the addition of a buffer layer can improve the SEB threshold value effectively. The holes concentration, total current density distribution and electric field inside the device have been given and analyzed to understand the difference of the inner physical mechanisms. The hardened TS-UMOSFET is burnout at 65 V, whereas the burnout voltage of the standard power UMOSFET is 40 V at LET value of $0.6pC/\mu m$. Therefore, the proposed structure achieves about 62.5% improvement in the device's susceptibility to SEB.

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