Reviewer: 1

Investigation of the Impact of Single Event Burnout on Radiation Hardened Trench Shielded …

1. English language usage needs significant improvement. The authors need to carefully proofread their work. Perhaps they could get a native English-speaker to edit the paper.

2. I do not believe that the title is appropriate. This is a paper on device simulation. You have proposed a device structural modification that may improve device survivability to heavy ion exposure. You in no way "Investigate the Impact of ….." You only simulate the possible result that might occur with your imaginary structure.

3. Pg. 1, left col. Line 46 --- Refs. 1 and 2 are not appropriate for describing the space radiation environment. Also, ref. 2 is one of your own papers, not even on the topic of the space environment. Consider replacing refs. 1 and 2 with ……...

E.G. Stassinopoulos and J.P. Raymond, "The space radiation environment for electronics," Proceedings of the IEEE, Volume: 76 , Issue: 11 , Nov 1988 .

Sébastien Bourdarie and Michael Xapsos, "The Near-Earth Space Radiation Environment," IEEE Ttans. Nucl. Sci., VOL. 55, NO. 4, AUGUST 2008

4. Pg. 1, left col., line 52 --- Some researchers believe that there are mechanisms in addition to bipolar BJT turn-on. The BJT turn-on has been described in detail by a number of authors – papers primarily in the IEEE Transactions on Nuclear Science. Some of these should be referenced.

5. Pg. 1, left col., line 52 --- Refs. 3 and 4 are not appropriate references for ("……; it's mainly dependent on the inherent parasitic BJT in the MOSFET ……"

6. Pg. 1, right col., lin 39 --- I do not believe that this is an appropriate interpretation of Ref. 5. Burnout occurs when there is a short between source and drain. The substrate does not melt. Occasinally, thermal damage at the surface can be detected. See many photographs that are in the literature.

7. Pg. 1, right col., line 46 --- Refs. 6 – 10 are an odd collection of Refs. To establish "extensively investigated." I would suggest that you re-think the impact of the papers that you reference here.

8. Pg. 1, right col., line 46 --- There are many important papers on this topic. The authors should avoid self-citation just for the purpose of self-citation. Ref. 10 is not a highly cited nor well - known contribution to this field.

9. Pg. 1, right col., line 47 --- Credit for the buffer layer belongs to S. Liu and her collaborators (including Titus). In their papers, they actually fabricated and tested devices to illustrate the benefits. Her work should be credited when the buffer layer approach is discussed.

10. Pg. 1, right col., line 53 --- The author names are listed incorrectly for Ref.11. The first author is Jia, not Yunpeng. Please correct.

11. Pg. 1, Figure 1 --- The proposed structure in Fig. 1 is interesting. The use of a buffer layer is not new. The p+ shielding (misspelled in the figure) is interesting and achievable. The "added n region surrounding the shielding layer" may be very difficult to achieve in practice. It is not hard to dream up interesting device structures; often they cannot be fabricated. The authors need to explain how the TS-UMOSFET might be fabricated with the "added n region surrounding the shielding layer."

12. Pg. 2, left col., line 9 --- you refer to papers by Mo and Wan but only give a Ref. to Mo, Ref. 17, what is the Wan Ref.?

13. Pg. 2, Why was a 3-D simulator not used? It would yield better fidelity.

14. Pg. 2 and 3, Many researchers use the Silvaco codes. Perhaps you have over explained what is available there – you only need to say which physics models were turned on. Also, most readers will find equation 1 superfluous.

15. Pg. 3, left col., line 21 --- Basic electrical characterization? You have not done any basic electrical characterization since you have never fabricated this device. You have only simulated the device's electrical characteristics.

16. Pg. 3, left col., line 23 --- Is there anything unique about your description of the track structure? A number of papers have been published on this topic.

17. Pg. 3, left col., line 51 --- So you have just adopted the parameters for the imaginary UMOSFET that Wang simulated in Ref. 22 --- see Wang's table I. Have you looked at the parameters for an actual working power UMOS device?

18. Pg. 3, let col., line 48 --- An LET of 60 is high for a real space mission. Heavy ion flux drops off quickly after the iron-knee.

19. Pg. 3, left col., line 55 --- You have not characterized any electrical characteristics of a power UMOSFET device. No actual device has been fabricated and measured.You have only simulated the characteristics. The authors should clearly point out that the results presented in figure 2 represent simulated values.

20. Pg. 3, right col. Line 46 --- The authors should specify their criteria for declaring that SEB has occurred. It might be good to show a plot of the drain current versus time after the ion strike for several different choices of LET and reverse voltage. See figure 7 in Ref. 22 and in other so-called hardening papers by Wang.

21. Pg. 4 --- Figure 2 does not convey very much information. Most of this figure can be eliminated. What are the threshold UMOSFET voltages from (a)? What are the gate voltages for each of the traces given in 2(c)?

22. Pg.5 --- Figures 3,4,and 5 do not convey very much information.
23. Pg 6, Figures 6 and 7 --- Just what is the TG-UMOS device referenced in these figures? I am not sure that these figures as labeled are correct. I believe that this is just another needless error.
24. Pg. 6 --- The authors are correct in exploring the effect that a modified structure has on the electric field distributions. This is key to understanding why a buffer layer leads to improvement. Other authors have done this and more extensively so. The authors should read and reference those papers.
25. Overall. This is a poorly written manuscript with many needless errors. The authors do not demonstrate a strong grasp of the device physics and single-event burnout process. This paper adds little to the scientific and engineering literature.

Reviewer: 2

Comments to the Author
Overall the paper seems to be nicely written, with a good review of the previous literature for radiation-hardened power MOSFETs. This manuscript reports a simulated device structure called TS-UMOSFET: the P+ shielding region can protect the gate oxide layer during the heavy ion and the n-buffer layer can enhance the SEB performance. A couple of comments from my side:
1. The authors should explain that "How the p+ shielding region works for protecting the gate oxide layer during the heavy ion". In my opinion, the electric field in gate oxide layer may be reduced, and the results should be given.
2. Page 2, second column, lines 40-45, "the thickness and doping concentrations of buffer layers have been optimized." In this paper, they presented three different buffer layers, and the optimized concentration for every buffer layer may be different for SEB hardening. The authors need to verify that.
3. The authors had better compared the simulation result of total accumulated charge at a given LET value with the theoretical value to verify the correctness of the models and simulator.
4. In table III, the authors only perform the simulation result for standard UMOS. The other two structures (without buffer TG-UMOS and with buffer TG-UMOS) are also needed to given.
5. In table IV, the unit of LET should be given.
6. In Fig. 4, the finally hole concentrations of the two structures had better be given to judge whether a SEB occurs or not. The unit/values for the hole concentration seems be expressed by log type, and this should be explained in this paper. Besides, the numbers and words are very hard to read, and are needed to be re-edited (also in Fig. 5).
7. In Fig. 6 (b): the labels for green and red lines are false.
8. Page 6, second column, lines 53-55, "It can be seen that if the thickness of the buffer layer increased, SEB threshold value also increased." Whether the SEB threshold value can achieve the BV value (70V) with the help of buffer layer is also need to be discussed.
9. Page 6, second column, lines 57-59, "the thickness is chosen as 0.7 to obtain an optimum SEB threshold value and ON-resistance." The authors had given the 0.7 as the optimum buffer thickness, so they also need to give a more detailed discuss about the SEB threshold value and ON-resistance based on different buffer thickness.