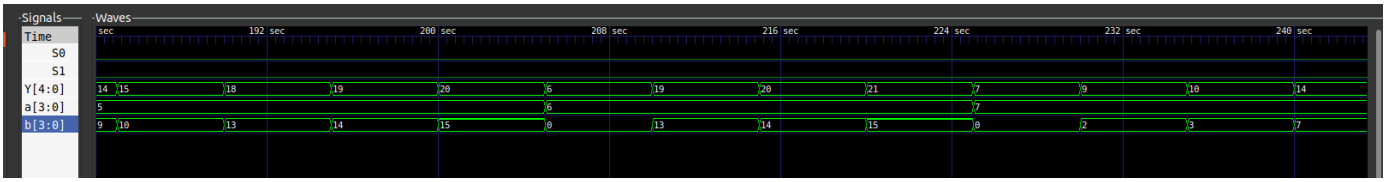
VLSI PROJECT Report

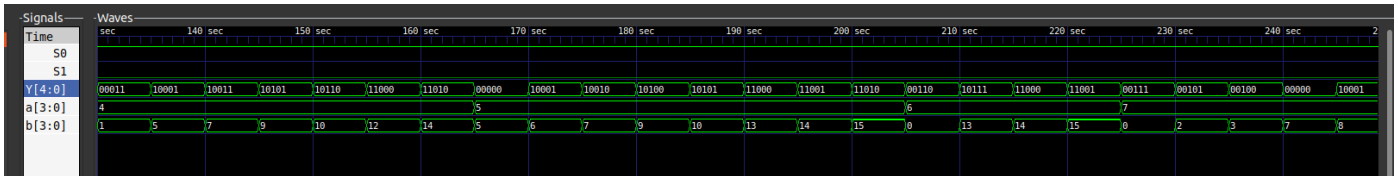
E Druvitha, 2022102029

VERILOG

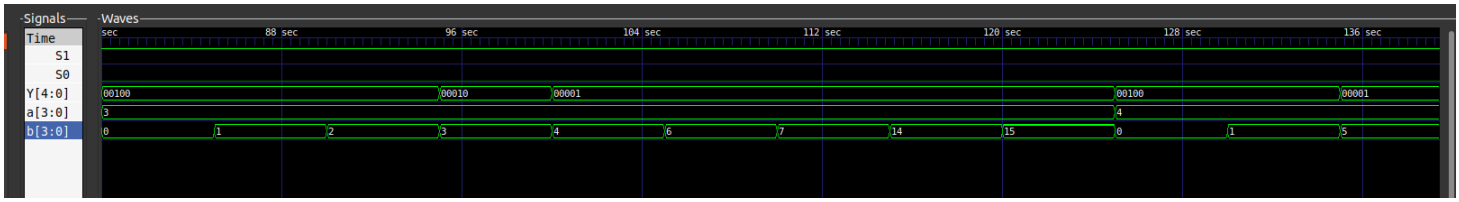
S=00



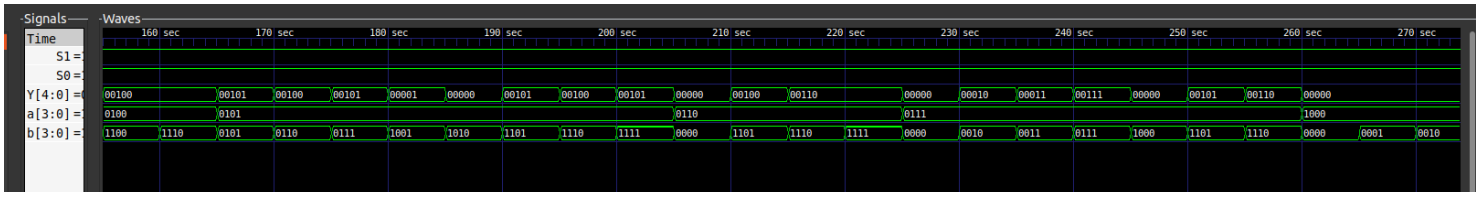
S=01



S=10



S = 11



For comparator in the output y[2] represents a>b, y[1] represents a=b and y[0] represents b>a I.e if it is true the bit is 1 otherwise 0.

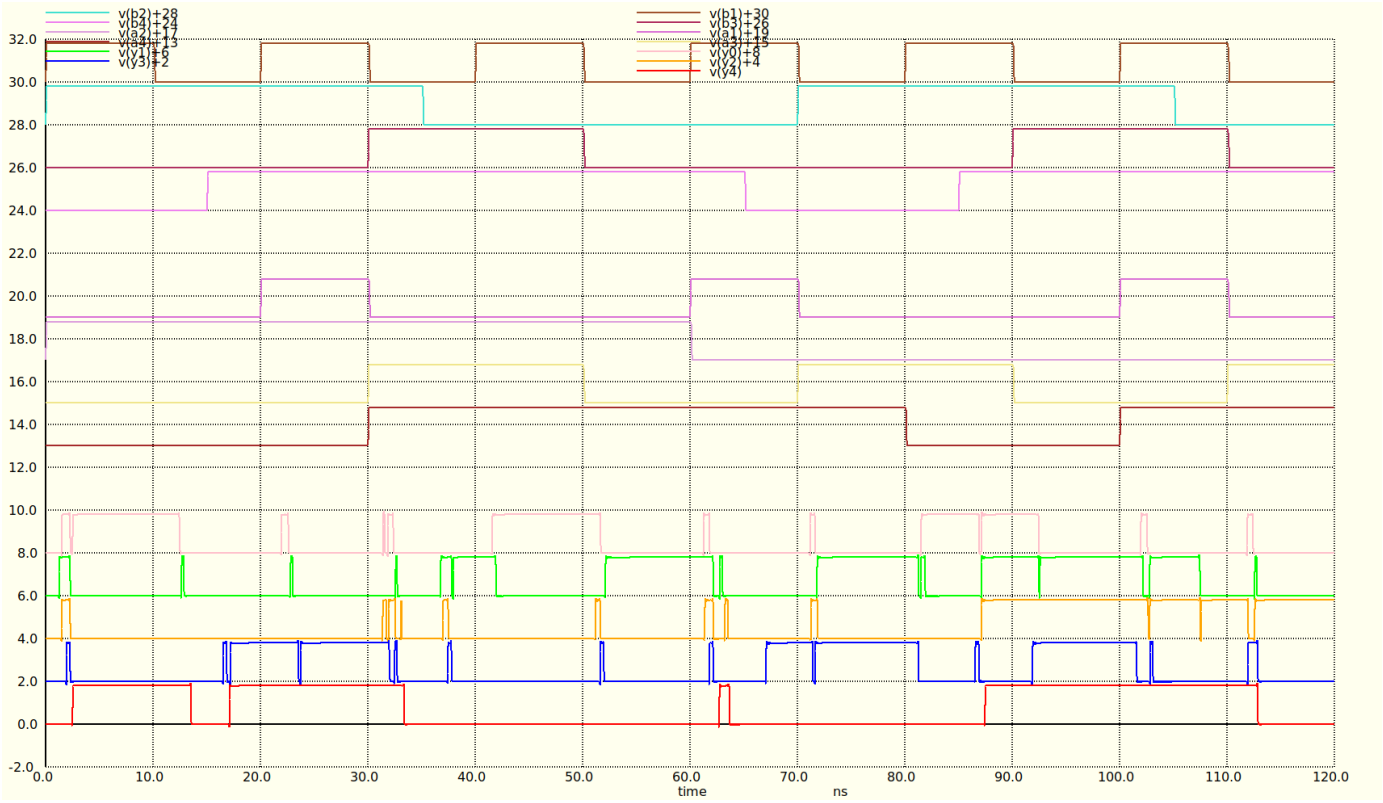
In SUBRACTOR S = 01 the output is 5 bit sign representation.

For different type of inputs the outputs are plotted and attached above for different select lines.

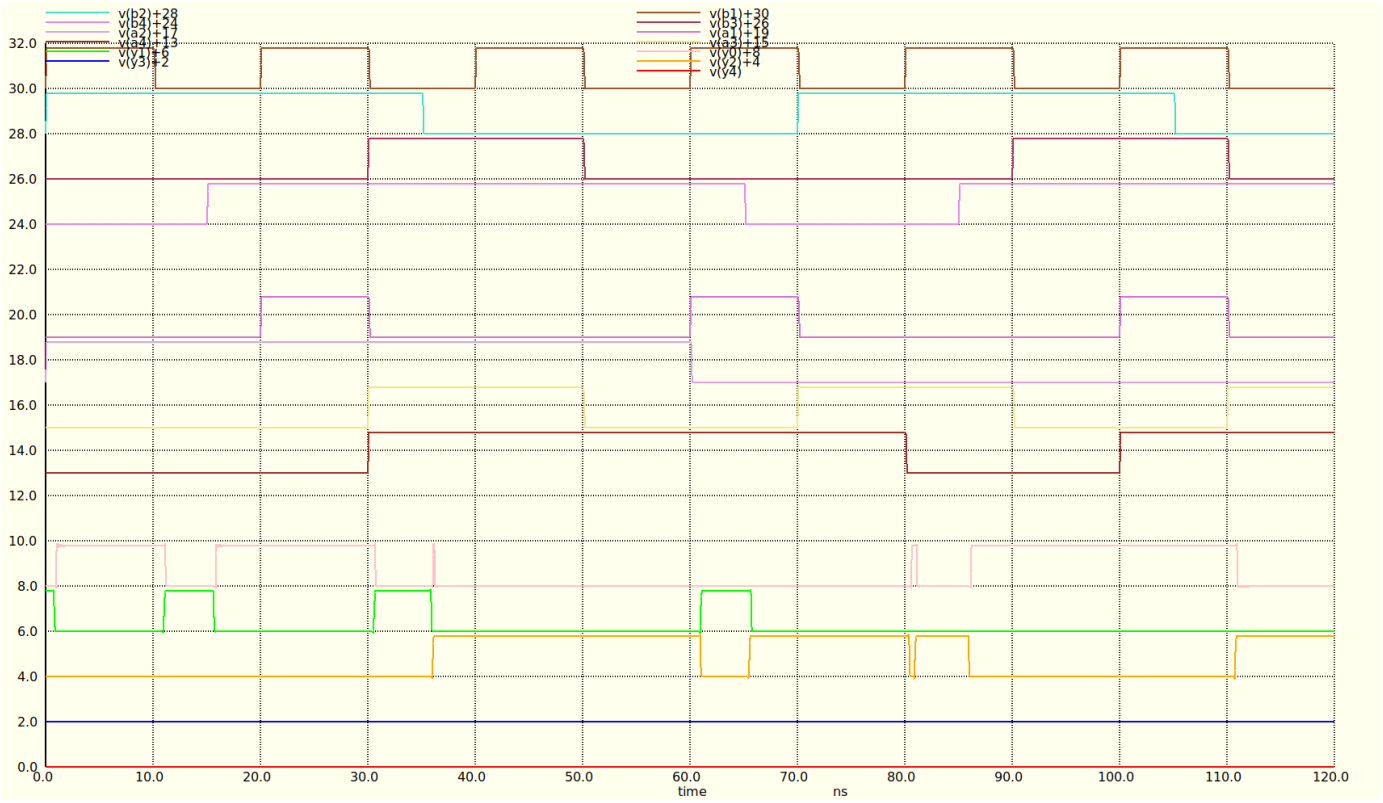
NGSPICE

S=00

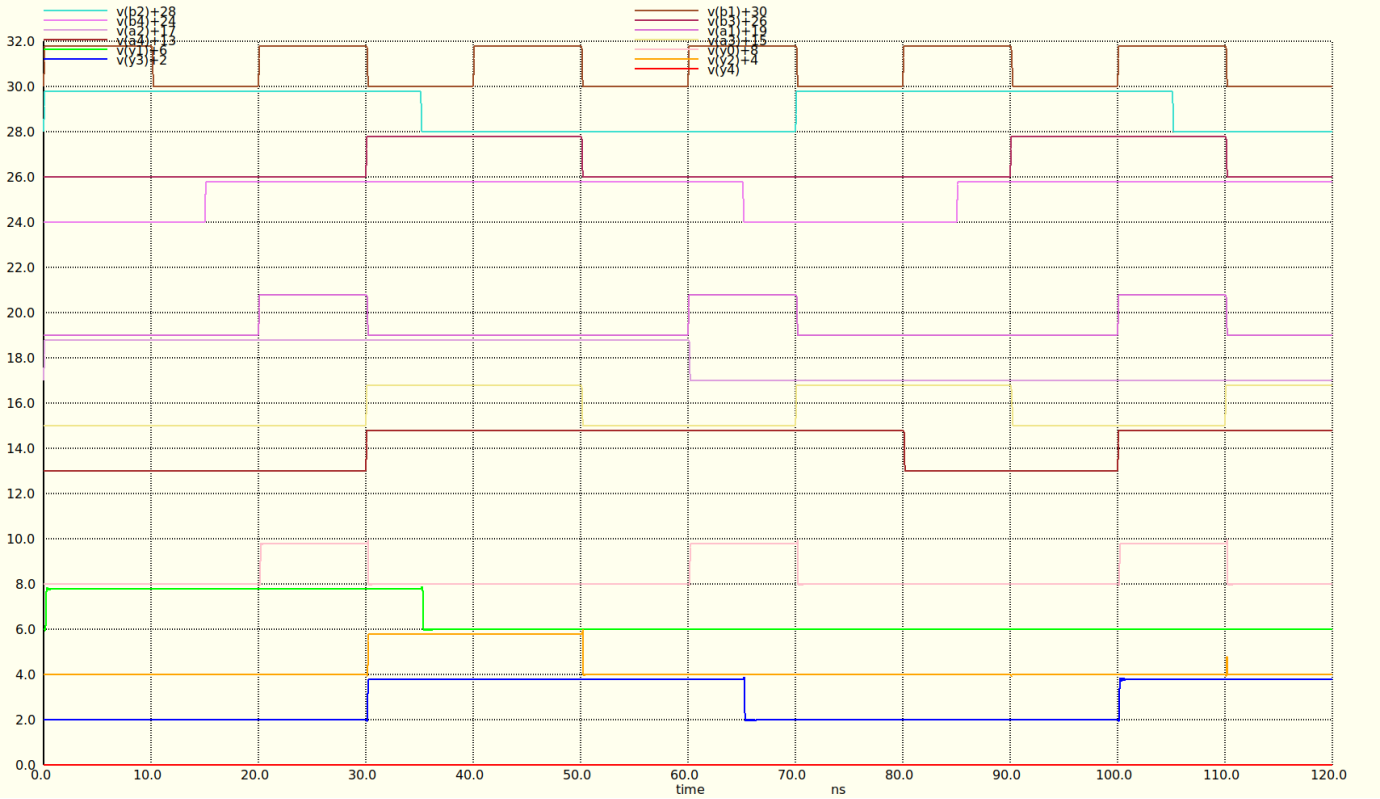
S=01


v(b2)+28
v(b4)+24
v(a2)+17
v(a4)+13
v(y1)+6
v(y3)+2
v(b1)+30
v(b3)+26
v(a1)+16
v(a3)+15
v(y0)+8
v(y2)+4
v(y4)
32.0
30.0
28.0
26.0
24.0
22.0
20.0
18.0
16.0
14.0
12.0
10.0
8.0
6.0
4.0
2.0
0.0
-2.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
110.0
120.0
time
ns

S = 10


v(b2)+28
v(b4)+24
v(a2)+17
v(a4)+13
v(y1)+6
v(y3)+2
v(b1)+30
v(b3)+26
v(a1)+19
v(a3)+15
v(y0)+8
v(y2)+4
v(y4)
32.0
30.0
28.0
26.0
24.0
22.0
20.0
18.0
16.0
14.0
12.0
10.0
8.0
6.0
4.0
2.0
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
110.0
120.0
time
ns

S = 11


v(b2)+28
v(b4)+24
v(a2)+17
v(a4)+13
v(y1)+6
v(y3)+2
v(b1)+30
v(b3)+26
v(a1)+19
v(a3)+15
v(y0)+8
v(y2)+4
v(y4)
32.0
30.0
28.0
26.0
24.0
22.0
20.0
18.0
16.0
14.0
12.0
10.0
8.0
6.0
4.0
2.0
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
110.0
120.0
time
ns

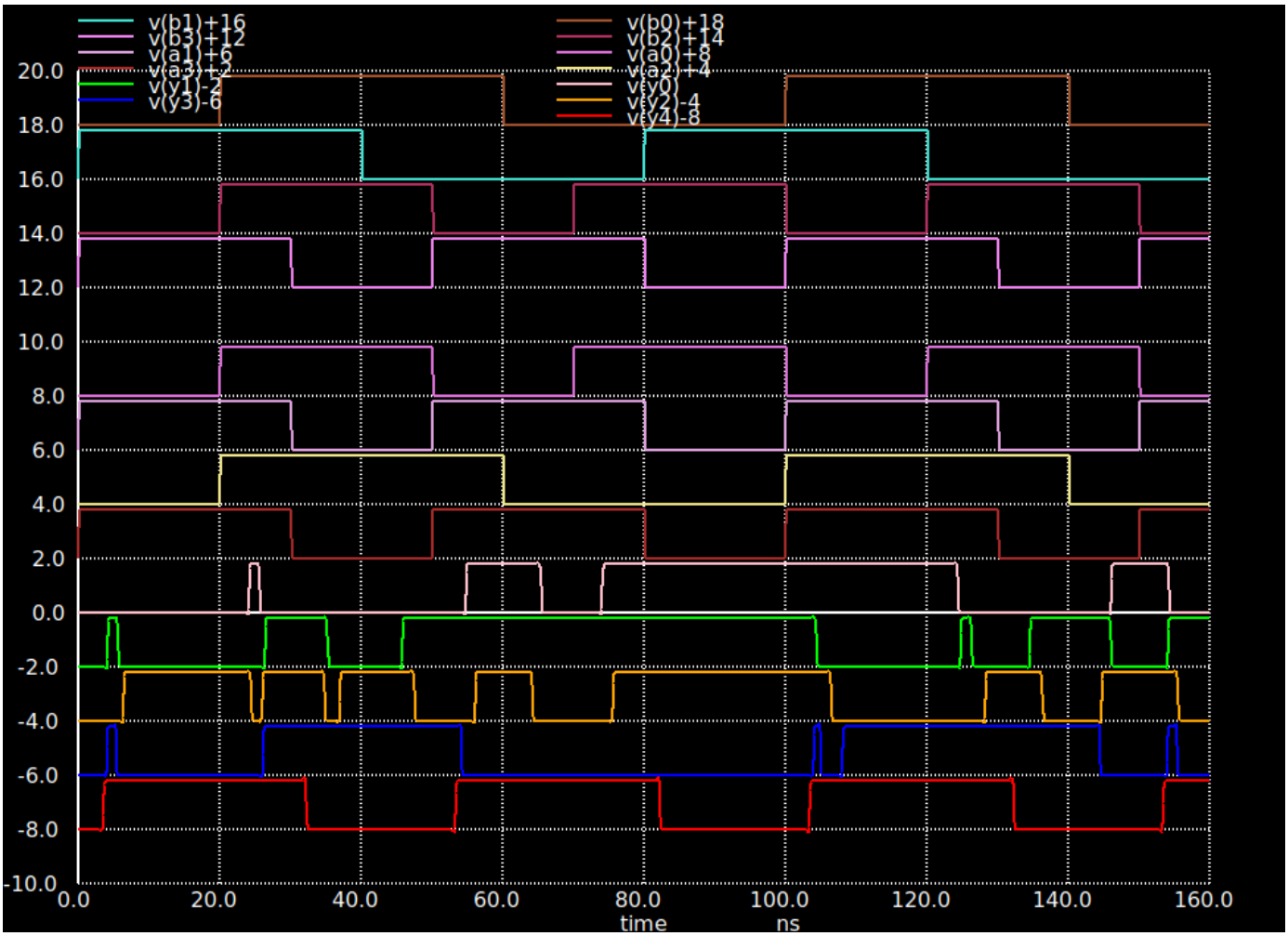
MAGIC

Plots of outputs when extracted from layouts using ext2spice command line for different input lines

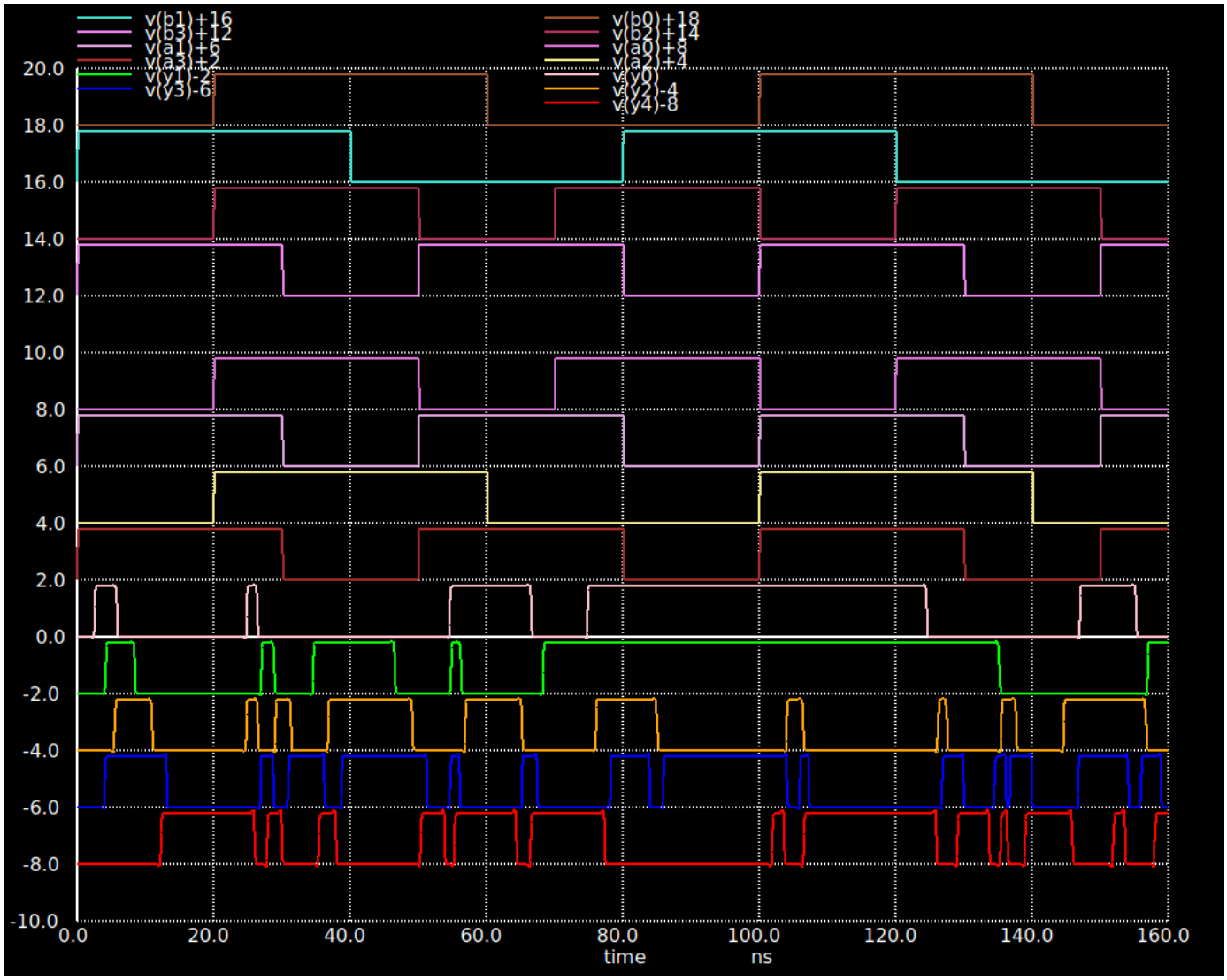
Above 4 represents b[4:0] , next four represents a[4:0] and the bottom 5 represents output y[5:0]

Where the bottom line in each represents msb.

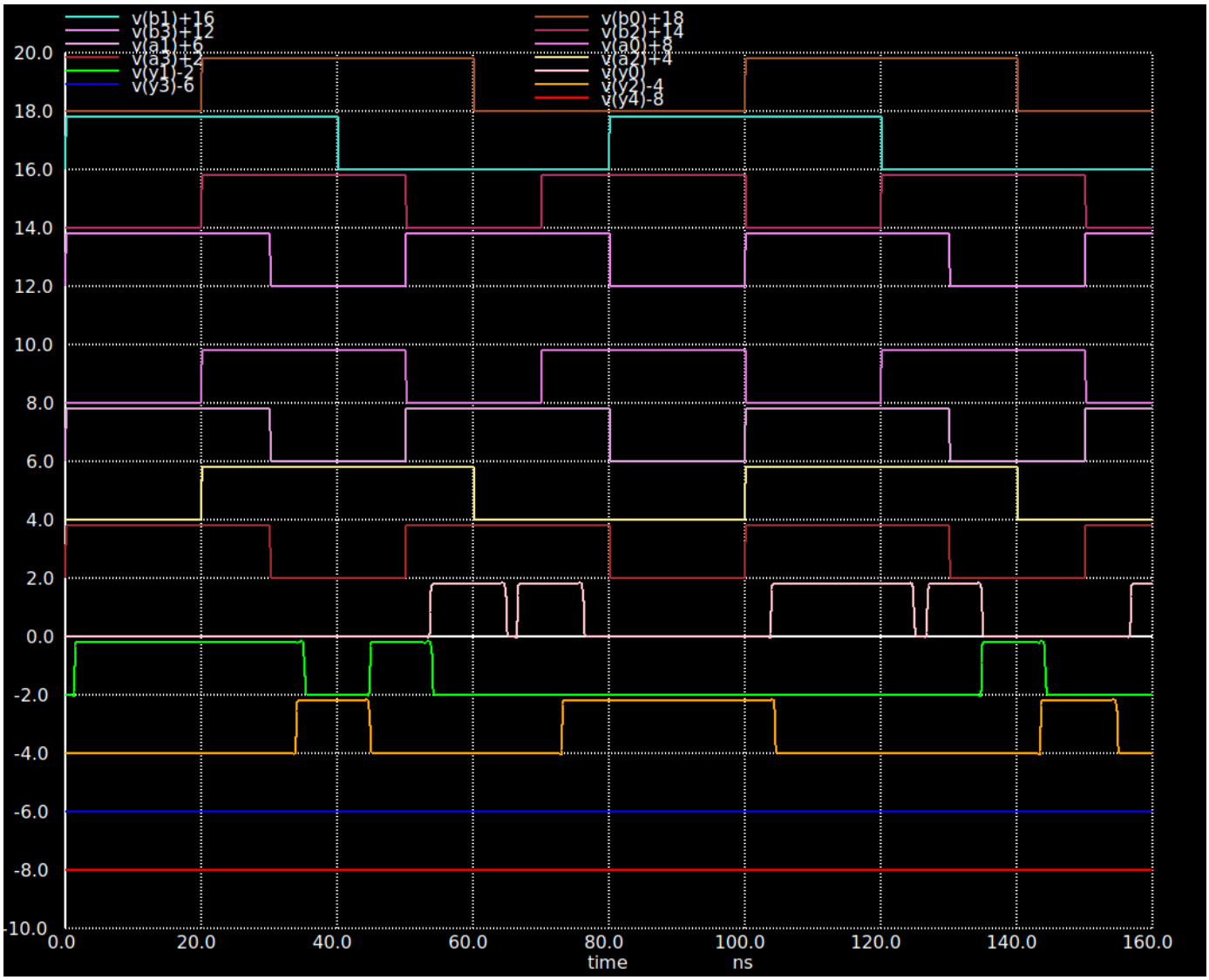
(i) S=00



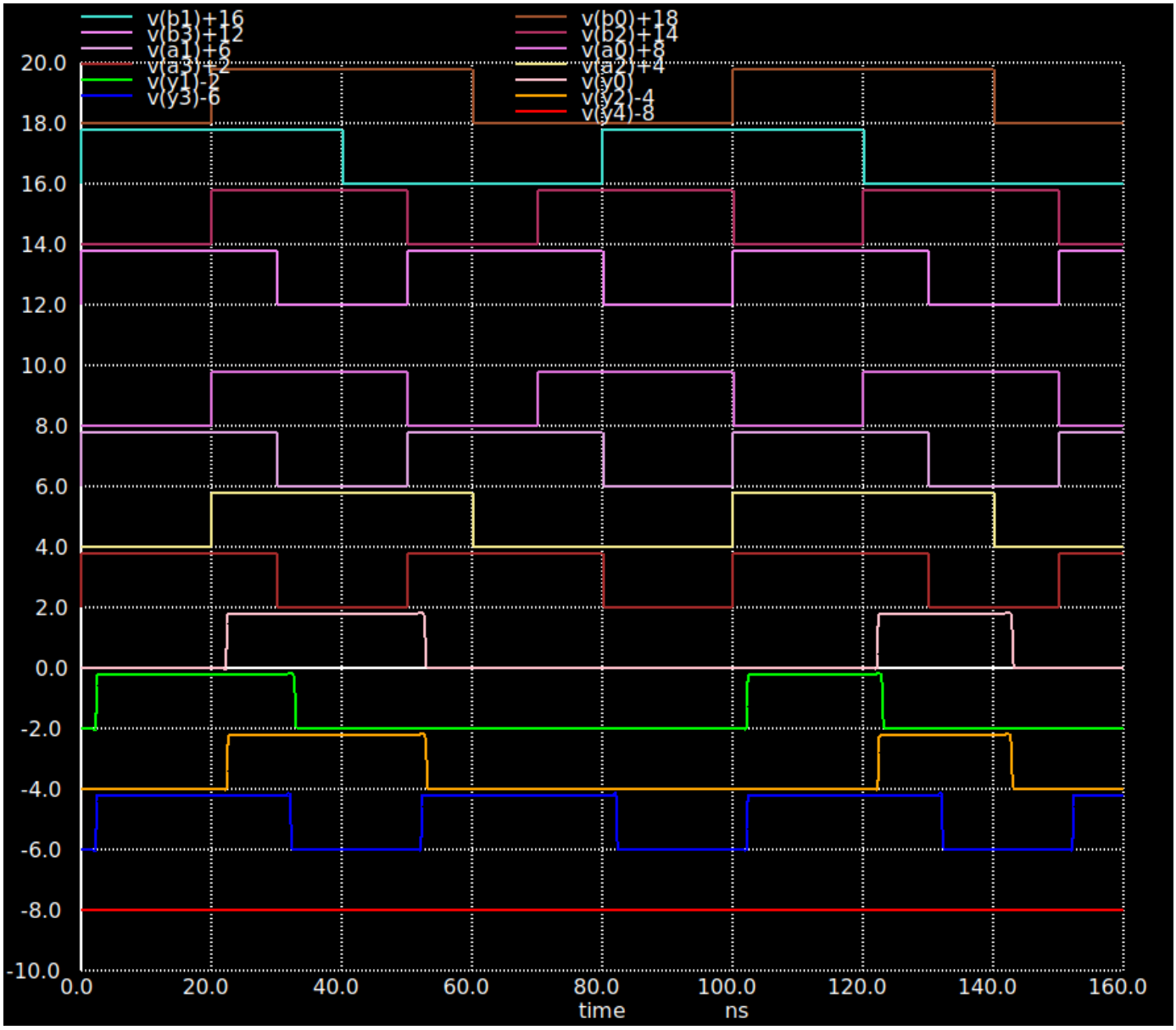
(ii) S = 01


v(b1)+16
v(b3)+12
v(a1)+6
v(a3)+2
v(y1)-2
v(y3)-6
v(b0)+18
v(b2)+14
v(a0)+8
v(a2)+4
v(y0)
v(y2)-4
v(y4)-8
20.0
18.0
16.0
14.0
12.0
10.0
8.0
6.0
4.0
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
time
ns

(iii) S = 10

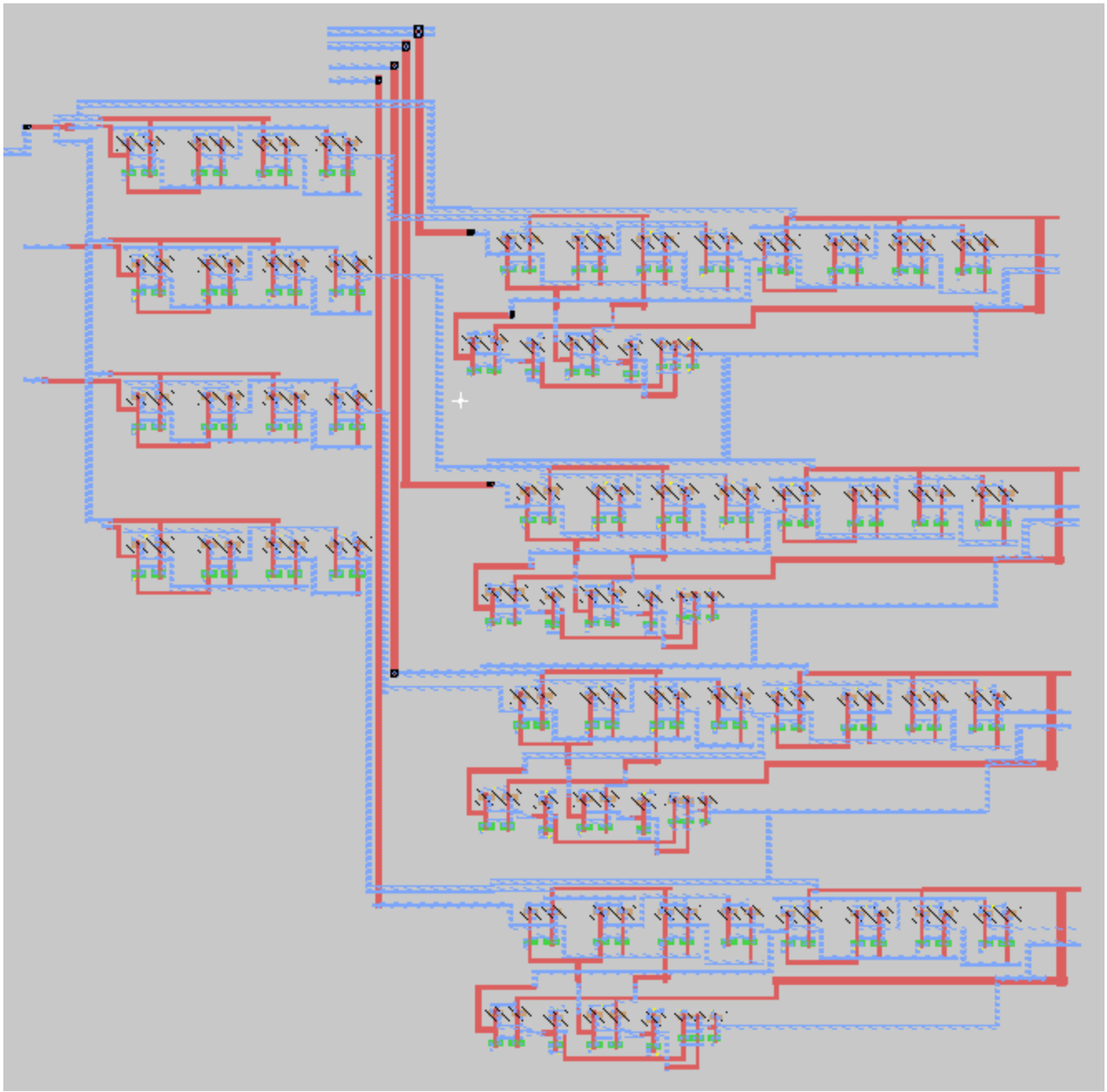

v(b1)+16
v(b3)+12
v(a1)+6
v(a3)-2
v(y1)-2
v(y3)-6
v(b0)+18
v(b2)+14
v(a0)+8
v(a2)+4
v(y0)
v(y2)-4
v(y4)-8
20.0
18.0
16.0
14.0
12.0
10.0
8.0
6.0
4.0
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
time
ns

(iv) S = 11

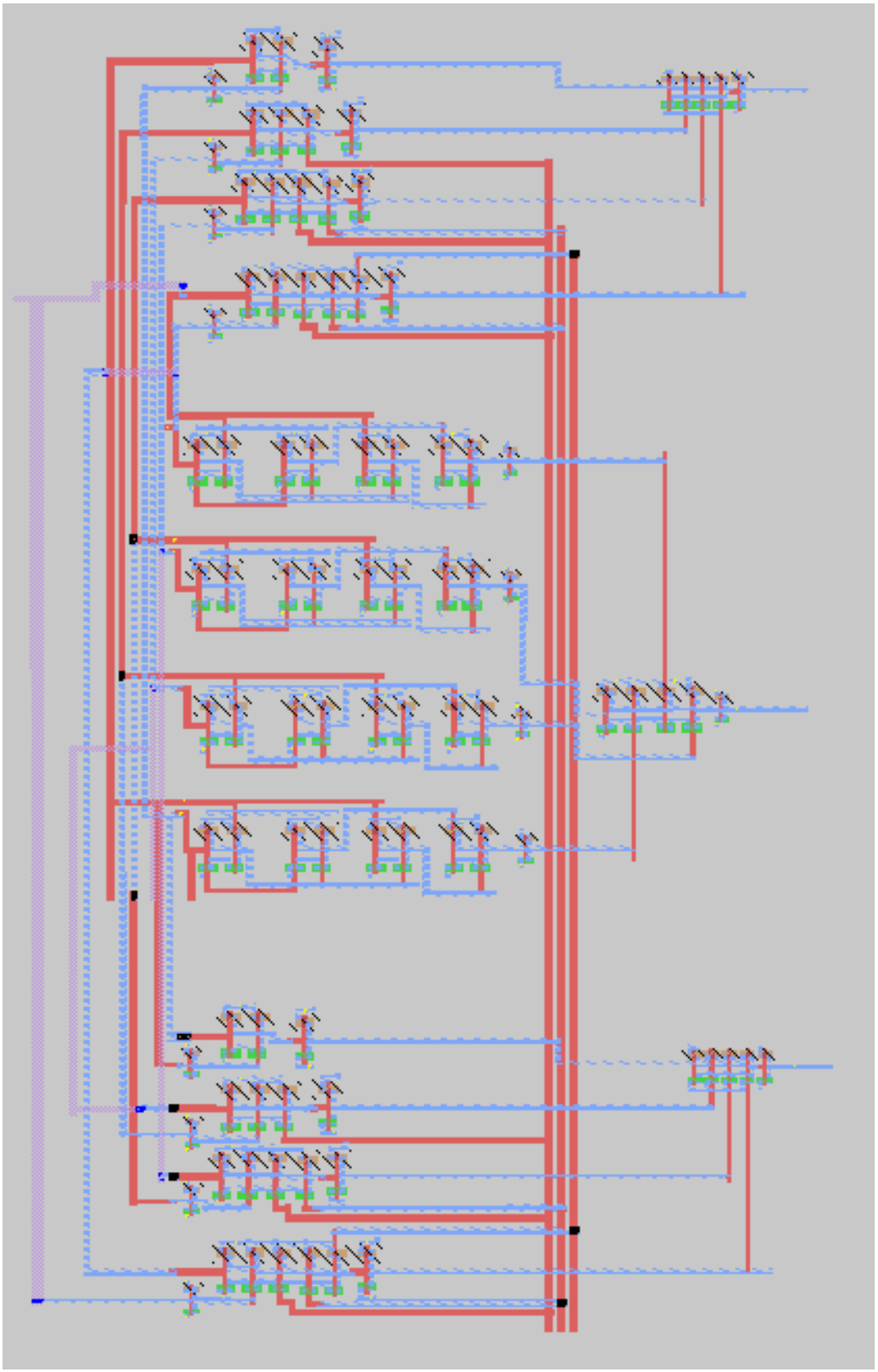

v(b1)+16
v(b3)+12
v(a1)+6
v(a3)+2
v(y1)-2
v(y3)-6
v(b0)+18
v(b2)+14
v(a0)+8
v(a2)+4
v(y0)
v(y2)-4
v(y4)-8
20.0
18.0
16.0
14.0
12.0
10.0
8.0
6.0
4.0
2.0
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
time
ns

Screenshots of magic layouts

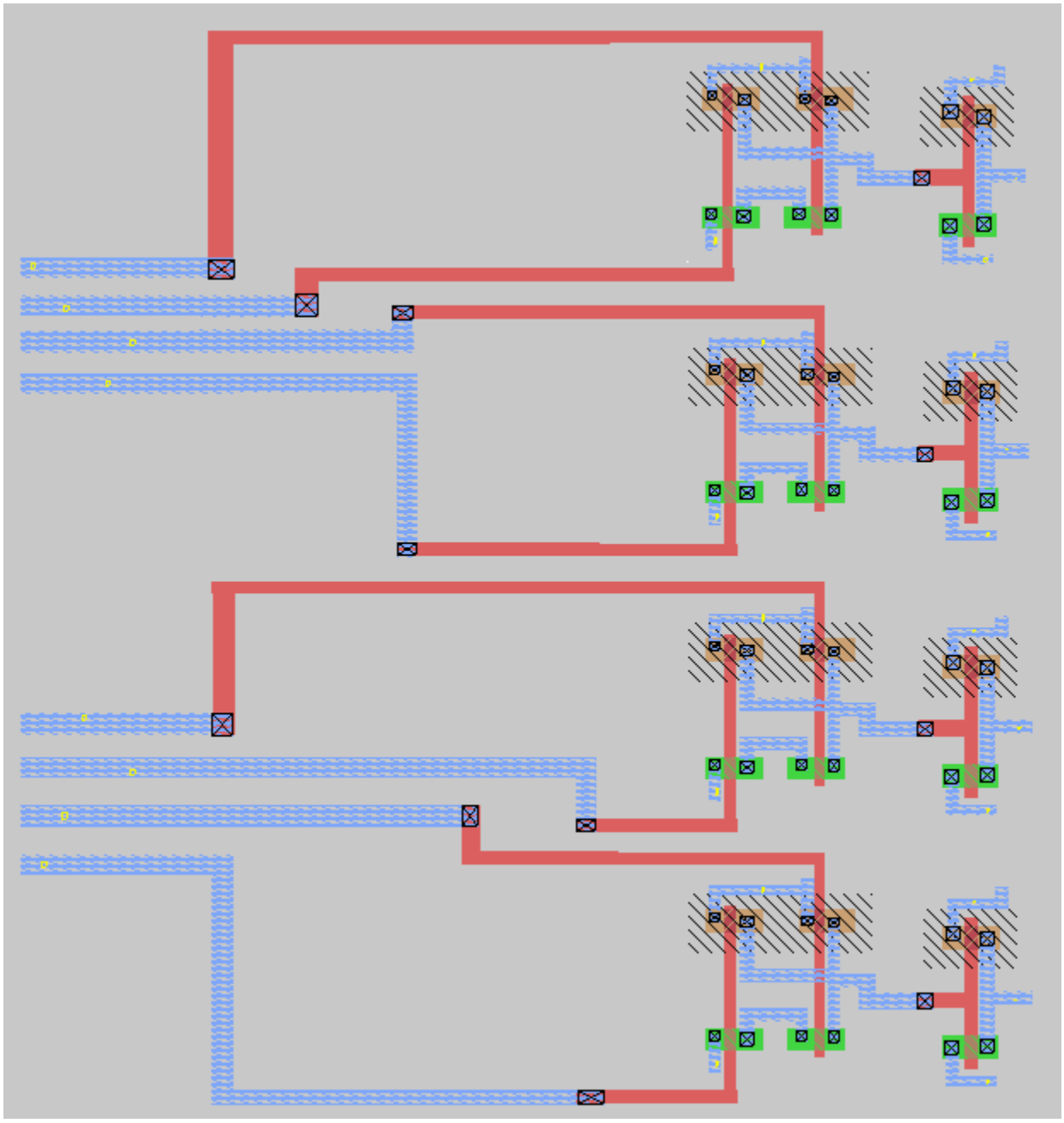
(i) Addsub part



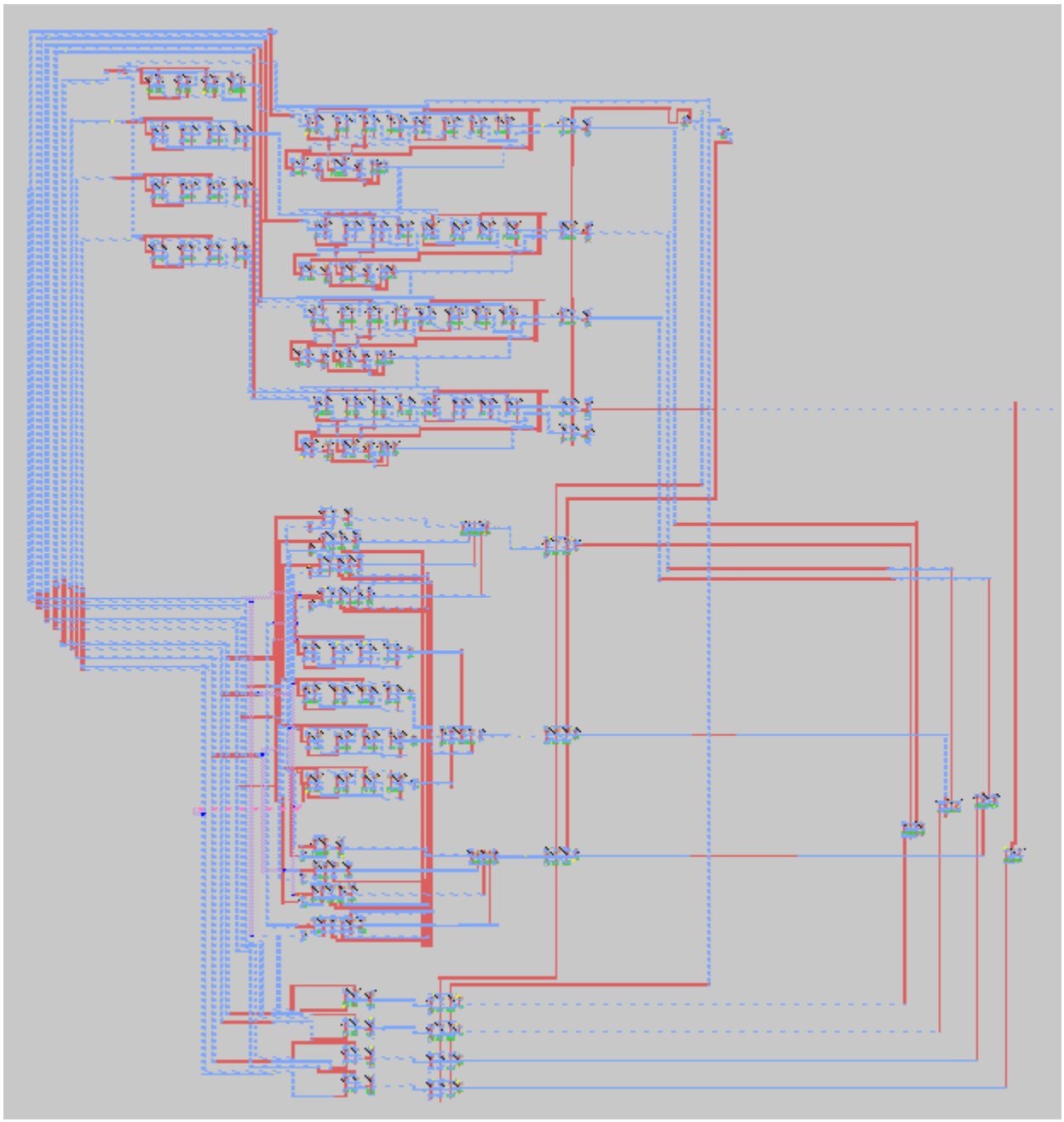
(ii) Comparator part



(iii) ANDing part



The total ALU part including mux



Using enable we implemented mux such that based on select lines output is displayed in spice when extracted from layout.

Delay analysis

In a circuit the path between an input and an output with the maximum delay is known as Critical path.

ADDER :

- For adder we have different cases to calculate delays
- We have 2 src files for delay analysis of input vs output for S = 00
- Src file 1 - adddel1 where we have inputs

  A 1111 0000 1111 0000

  B 0000 0000 0000 0000

  Y 1111 0000 1111 0000

- Src file 2 - adddel2 where we have inputs

  A 0000 0000 0000 0000

  B 1111 0000 1111 0000

  Y 1111 0000 1111 0000

- In src file1 we will get A vs Y delay i.e each a0,a1,a2,a3 vs each y0,y1,y2,y3 So total 16 delays and in src file2 we will get B vs Y delay Even 16 delays here So total of 32 delays in adder
- Now all these 32 delays are generated using python script and printed those delays in i1delay.txt
- Among the obtained delays the max delays are
  For y0 max delay is 5.43802e-09
  For y1 max delay is 5.39522e-09
  For y2 max delay is 5.49035e-09
  For y3 max delay is 5.20504e-09

Subtractor:

- For the delay analysis of subtractor we do the same analysis as adder part but for different input cases and we have different src files named subdel1 and subdel2
- Here all the 32 delays are generated using python script and printed them in i2delay.txt.
- Among the obtained delays the max delays are

  For y0 max delay is 4.98614e-09

  For y1 max delay is 3.76208e-08

  For y2 max delay is 3.89412e-08

  For y3 max delay is 3.99361e-08

Comparator:

- For this part we have 4 src files where src file1 - has inputs

A	1111	0000	1111	0000
B	0000	1111	0000	1111
Y0	1	0	1	0
Y1	0	0	0	0
Y3	0	1	0	1

  From this we get delay of A vs Y0 and A vs Y3 total of 4 + 4 = 8 delays

- In src file2 we have inputs

A	0000	1111	0000	1111
B	1111	0000	1111	0000
Y0	0	1	0	1

Y1 0 0 0 0

Y3 1 0 1 0

From this we get delay of B vs Y0 and B vs Y3 total of 4 + 4 = 8 delays

- In src file3 we have inputs

  A 1111 0000 1111 0000

  B 1111 1111 1111 1111

  Y0 0 0 0 0

  Y1 1 0 1 0

  Y3 0 1 0 1

  From this we get delay of A vs Y1 total of 4 delays

- In src file4 we have inputs

  A 1111 1111 1111 1111

  B 1111 0000 1111 0000

  Y0 0 1 0 1

  Y1 1 0 1 0

  Y3 0 0 0 0

  From this we get delay of B vs Y1 total of 4 delays

- So total 8 + 8 + 4 + 4 = 24 delays total fro comparator
- Using a python script we generated the delays and printed them in i3delay.txt.
  - Among the obtained delays the max delays are
    For y0 max delay is 5.40446e-08

For y1 max delay is 2.68862e-09

For y2 max delay is 5.38176e-08

ANDing:

- For delay analyzing of this part we only have one src file which test all the delays a vs y and b vs y So total of 32 delays
- Inputs in src files is

A 1111 0000 1111 0000

B 1111 0000 1111 0000

Y 1111 0000 1111 0000

- Among the obtained delays the max delays are

For y0 max delay is 2.33564e-09

For y1 max delay is 2.36815e-09

For y2 max delay is 2.40550e-09

For y3 max delay is 2.12758e-09

Among all the maximum delay is 5.40446e-08