COMSM1302 Overview of Computer Architecture

Lecture 3
Transistor logic and CMOS





In this lecture

Foundations

Data representation, logic, Boolean algebra.

Building blocks

• Transistors, transistor based logic, simple devices, storage.

Modules

 Memory, simple controllers, FSMs, processors and execution.

Programming

 Machine code, assembly, high-level languages, compilers.

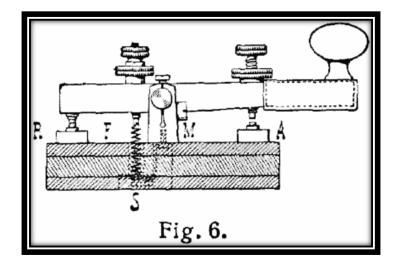
Wrap-up

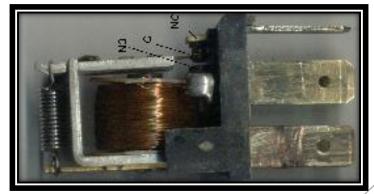
Operating systems, energy aware computing.



The switch - mechanical

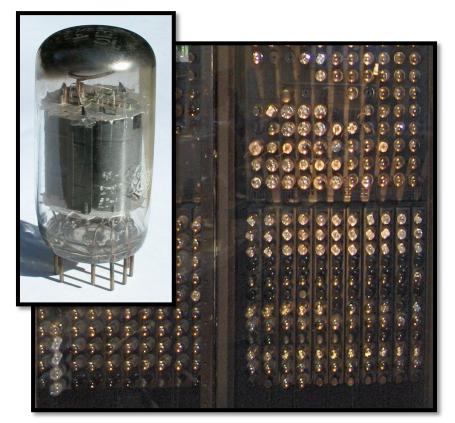
- Mechanical switches are very useful
 - Turn things on/off
 - With several switches,
 we can encode more useful things.
- What's wrong with them?







The switch - valve



Bank of valves from the ENIAC computer (1946). Photo source: TexDex, Wikimedia Commons.

- Valves or vacuum tubes.
- Current controlled by thermionic emission.
 - They have a heating element.
- Quicker than mechanical switches.
- Fairly reliable
 - If they're kept on!
 - ENIAC (1946) used 17,468
 vacuum tubes and consumed
 150 kW of power.



The switch - silicon

- Silicon, the element "Si"
 - The second most abundant element on Earth.
- A semiconductor
 - Can be constructed (using a process called doping) to pass electrons through a channel, when a voltage is applied to a gate.



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W Ore

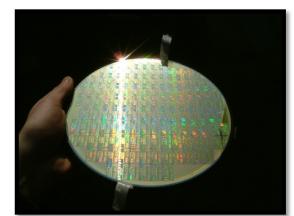


W Boule



Source: Stahlkocher, Wikimedia Commons

Wafer



Source: James Irwin, CC 2.0



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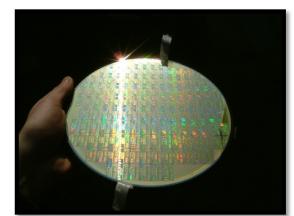


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Source: Stahlkocher, Wikimedia Commons

Wafer



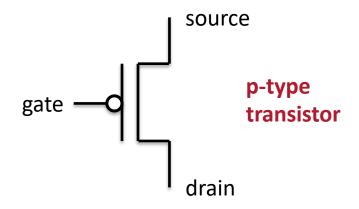
Source: James Irwin, CC 2.0



Making a switch out of silicon

- The transistor
 - Was invented in 1947 at AT&T's Bell Labs.
- Multiple uses
 - Amplification
 - Switching
- Multiple methods of construction
- We are interested in Integrated Circuits (ICs), so we want:

Complementary Metal-Oxide-Semiconductor (CMOS) technology.

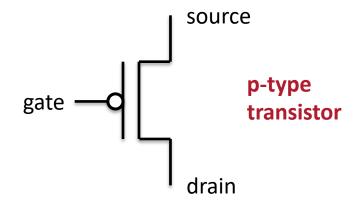


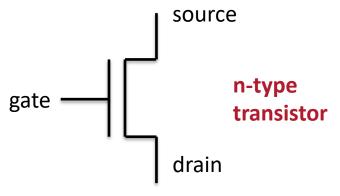


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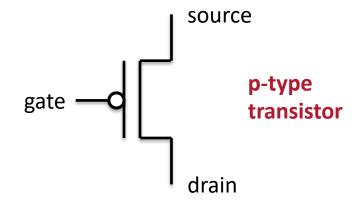


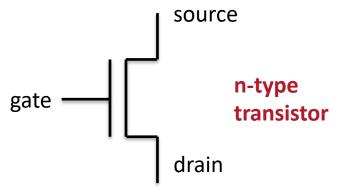


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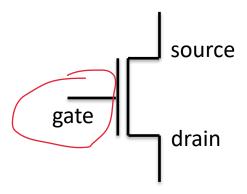
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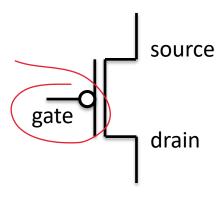






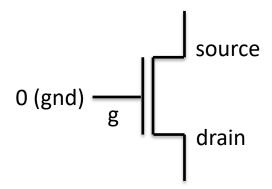
n-type transistor

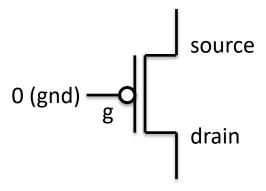






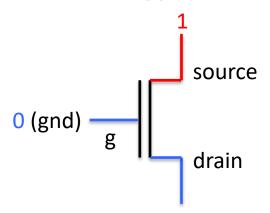
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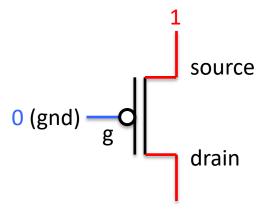




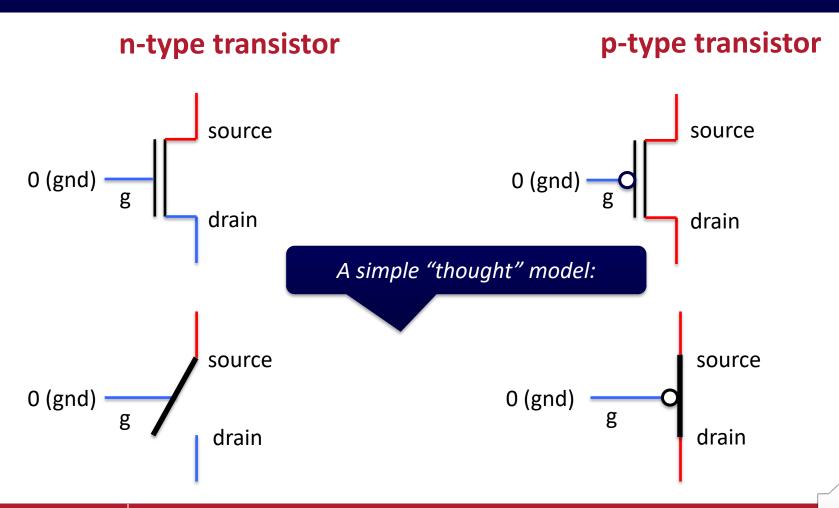


n-type transistor

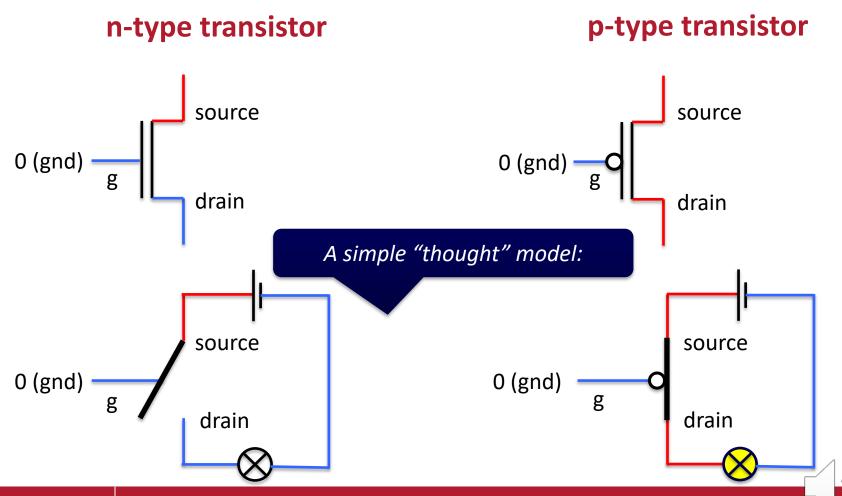






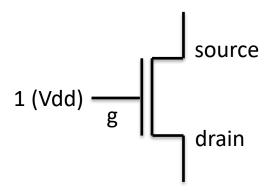


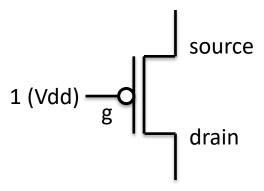






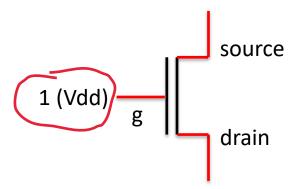
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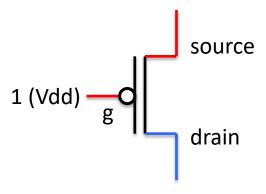




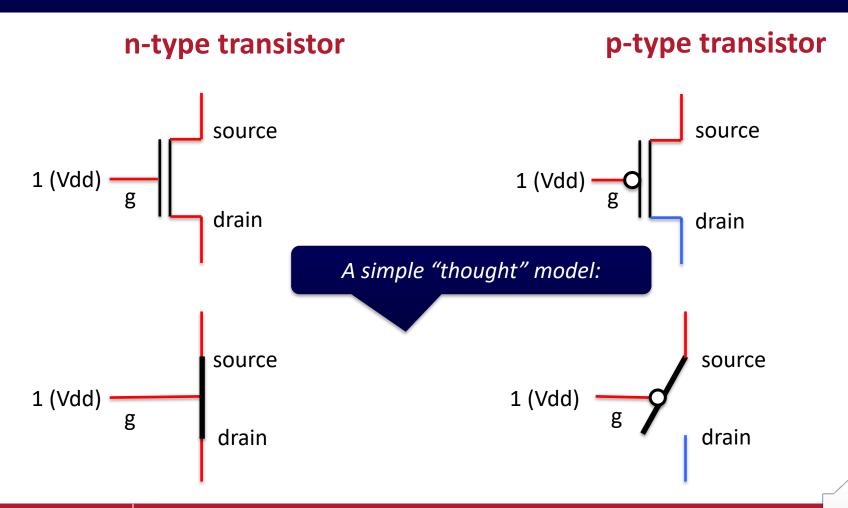


n-type transistor

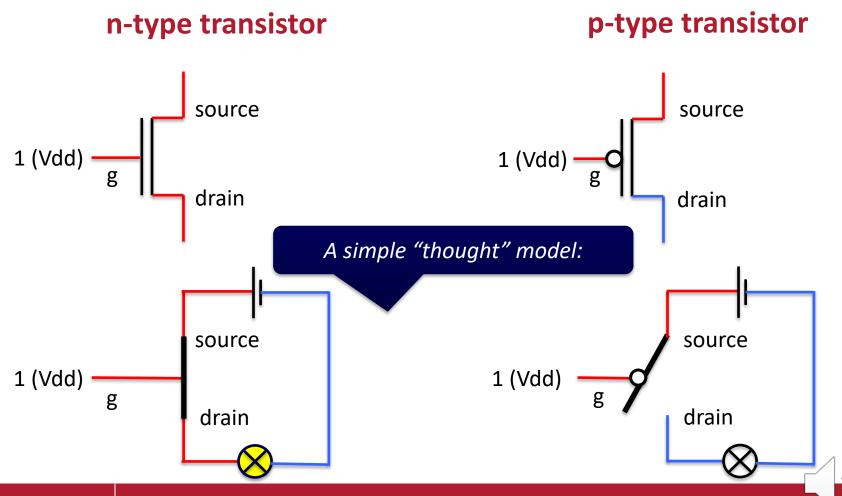












The most basic CMOS circuit

Composition of two complementary

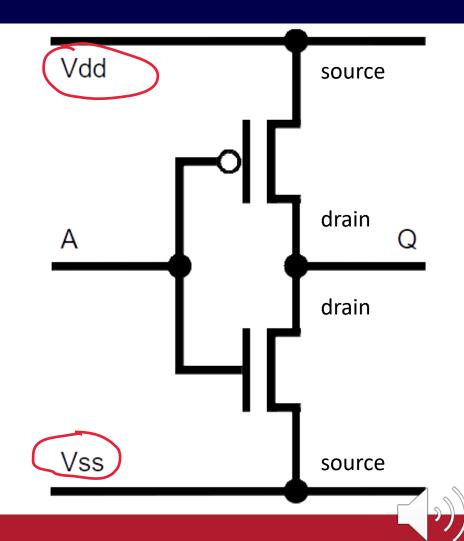
transistors

 The power supplies for CMOS are called

$$V_{dd}$$
 and V_{ss}

- Vdd = drain supply
- Vss = source supply
 - "0 V" or "ground" voltage

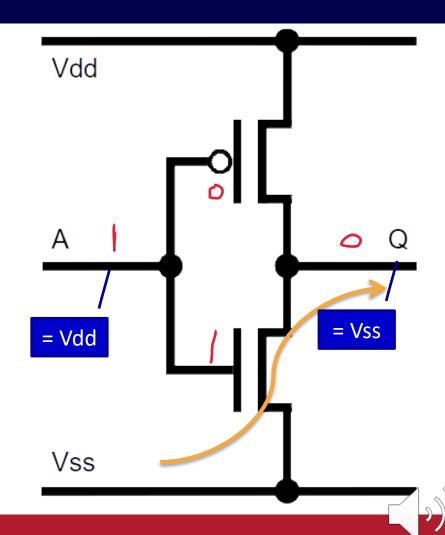
How does this work?





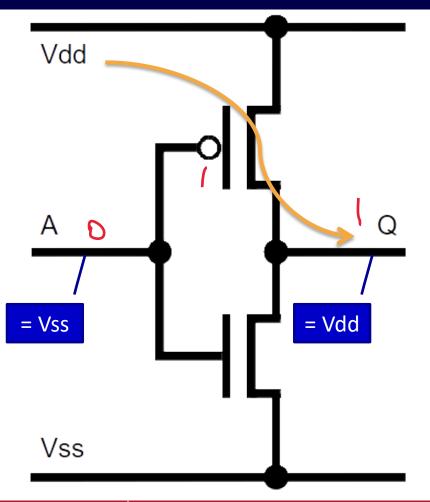
Modes of operation

- A = Vdd.
- The top "switch" is off/open.
 - PMOS transistor.
- The bottom "switch" is on/closed.
 - NMOS transistor
- Q is "connected" to Vss.





Modes of operation

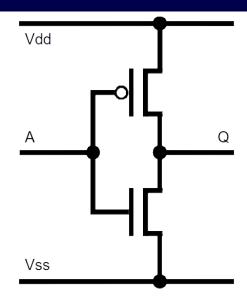


- A = Vss.
- The top "switch" is on/closed.
- The bottom "switch" is off/open.
- Q is "connected" to Vdd.



What did we just make?

- The circuit has four connections.
- Two are power-supply related.
 - Providing Vdd and Vss.
- One is an input, A.
- One is an output, Q.



Symbolic

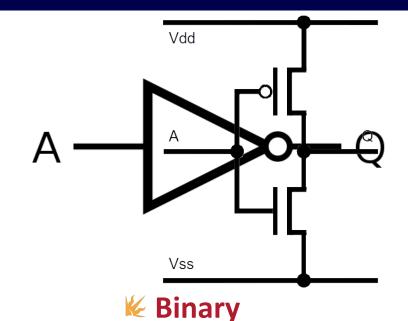
W Voltage

Α	Q	Α	Q
Vss	Vdd	0 V	3.3 V
Vdd	Vss	3.3 V	0 V



What did we just make?

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Symbolic

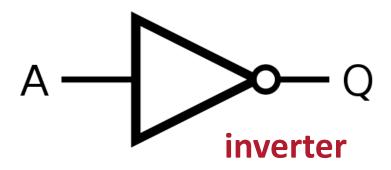
W Voltage

Α	Q	Α	Q	Α	Q
Vss	Vdd	0 V	3.3 V	0	1
Vdd	Vss	3.3 V	0 V	1	0



What did we just make?

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 - Providing Vdd and Vss.
- One is an input, A.
- One is an output, Q.



K Symbolic

W Voltage

K	Bi	n	ar	'

A	Q	Α	Q	Α	Q
Vss	Vdd	0 V	3.3 V	0	1
Vdd	Vss	3.3 V	0 V	1	0



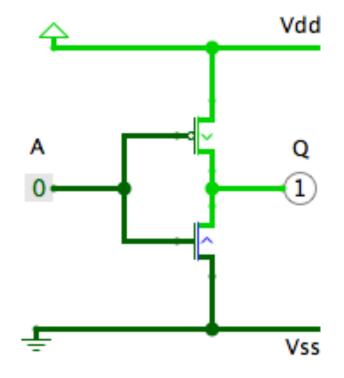
The CMOS inverter

<u>Logisim</u> design of a CMOS inverter for our next lab.

You can download Logisim from:

http://sourceforge.net/projec
ts/circuit/

 Install Logisim on your own computer and practice outside of lab hours.



NOT



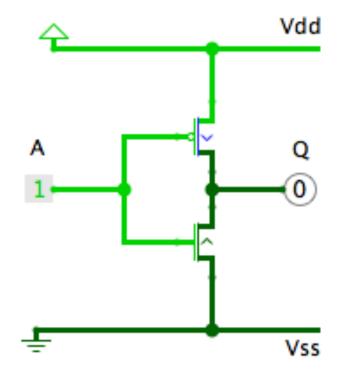
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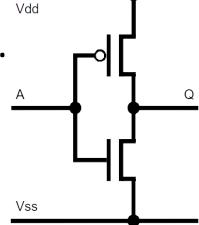


NOT



PMOS + NMOS = CMOS

- PMOS is good for making connections to Vdd.
- NMOS is good for making connections to Vss.
 - You can't make a reliable switch (or inverter) with just one type.
 - We either get 1/? or ?/0; we want 1/0.
- So we use a pair, one PMOS, one NMOS.
- They are complementary.



CMOS

Complementary Metal Oxide Semiconductor

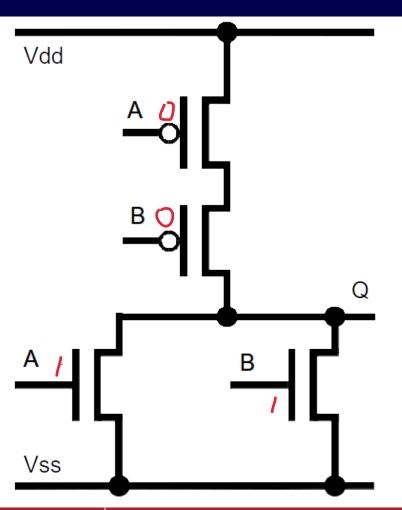


Boolean logic in CMOS

- We have a CMOS inverter.
 - Implements "not"
 - In a logic circuit, we call this a NOT gate.
- To build a more complex circuit, we need more than just a not gate.

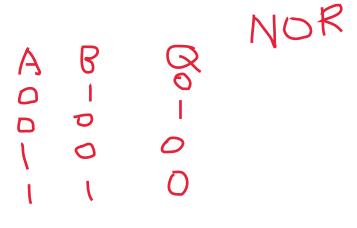
So ... what (else) can we make?



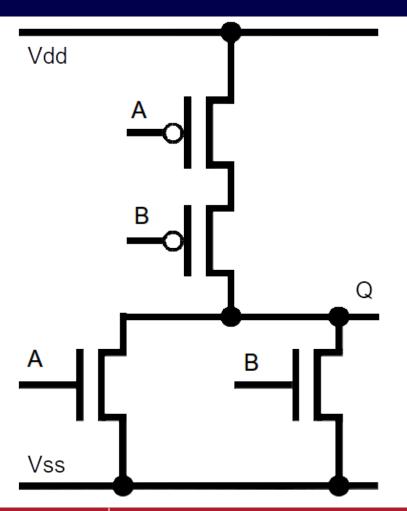


What is this?

How does it work?



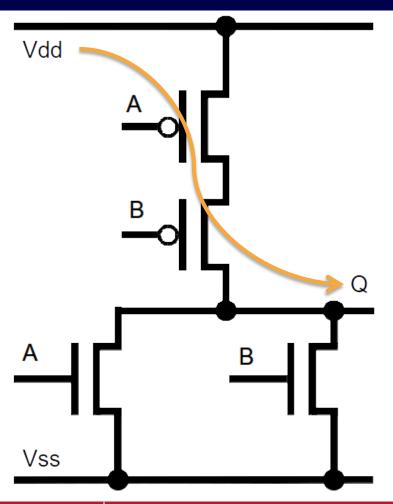




What is this?
How does it work?

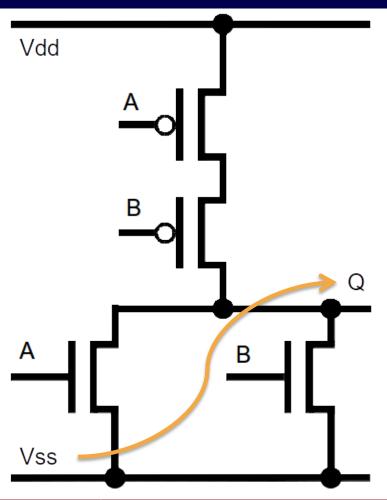
Please pause to see whether you can work this out. Carry on only when you've tried.





What is this?
How does it work?

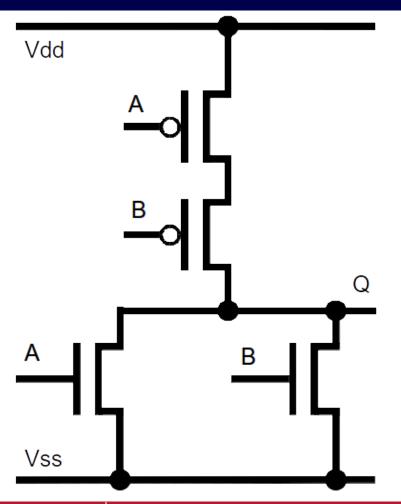




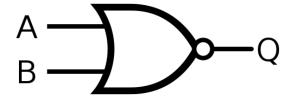
What is this?
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₩ NOR (NOT-OR)

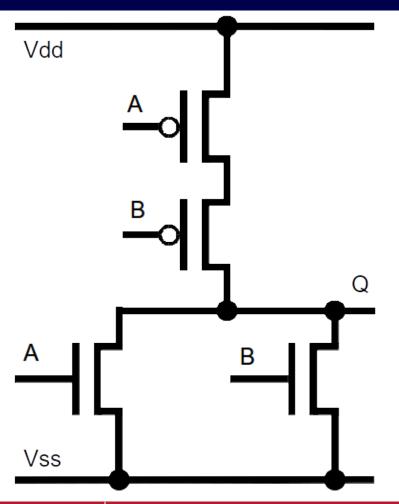


This is a NOR gate.

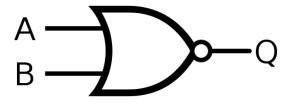




₩ NOR (NOT-OR)



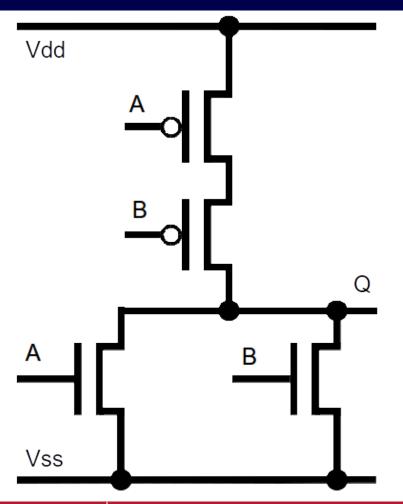
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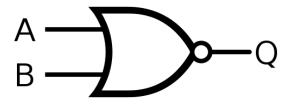
Α	В	Q
0	0	
0	1	
1	0	
1	1	



₩ NOR (NOT-OR)

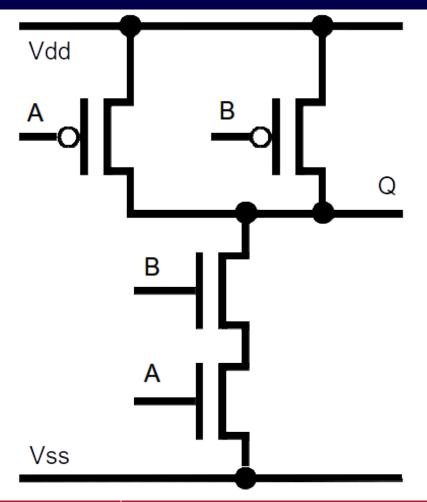


This is a NOR gate.



Α	В	Q
0	0	1
0	1	0
1	0	0
1	1	0

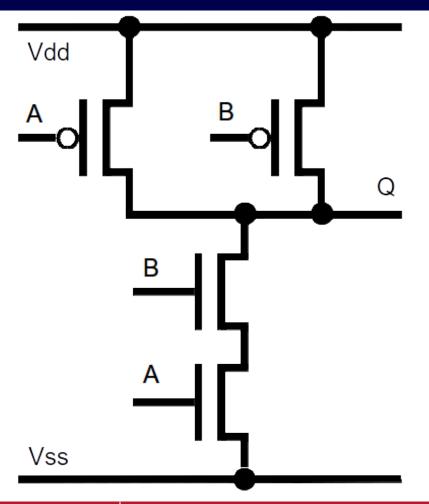




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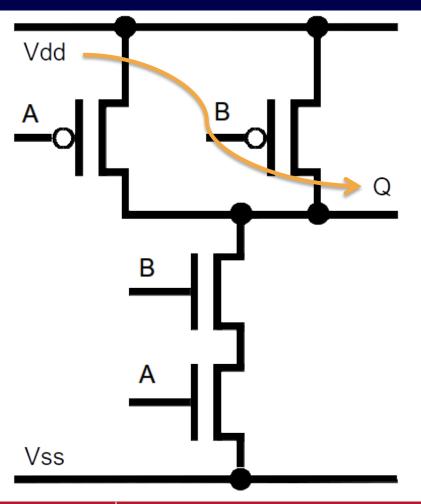
How does it work?





Can you work out under which conditions Q is connected to Vss?

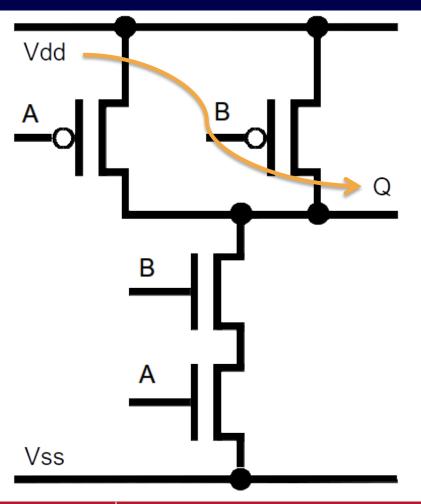






Α	В	Q
0	0	
0	1	
1	0	
1	1	

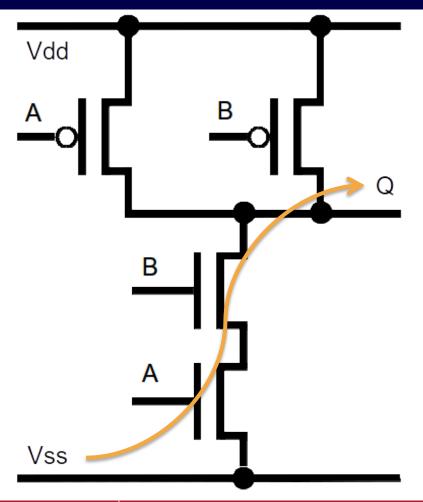






Α	В	Q
0	0	1
0	1	1
1	0	1
1	1	

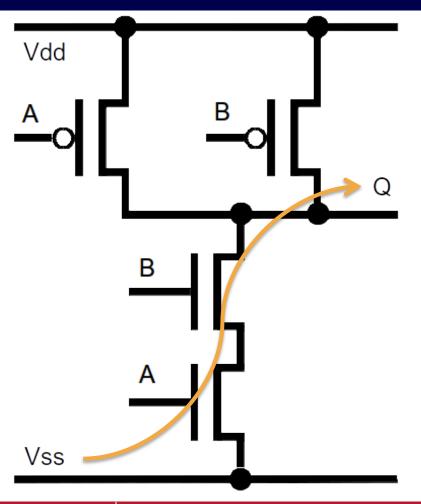






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1	1	

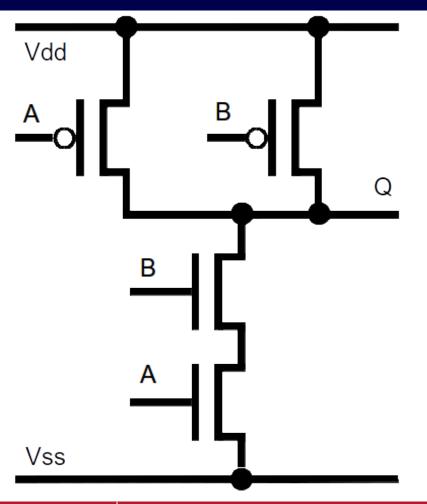






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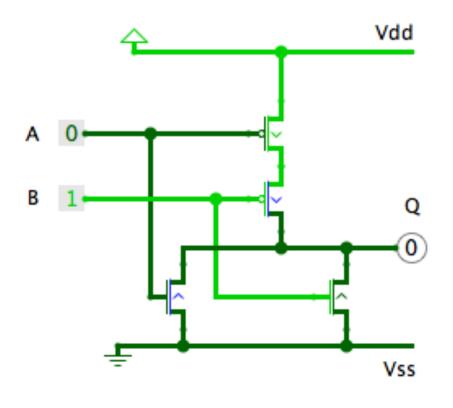


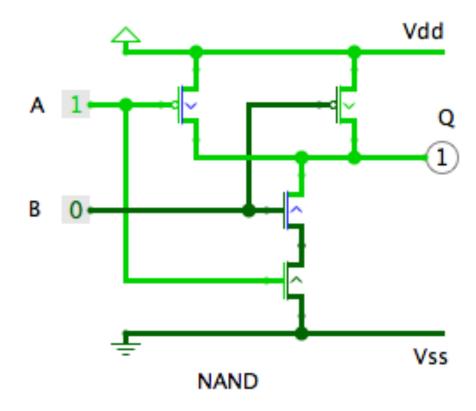


Α	В	Q
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0	1	1
1	0	1
1	1	0



NOR and NAND in Logisim



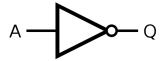


NOR



NAND is an excellent building block for other Boolean logic.

For example: NOT



W Diagram



W Boolean algebra

$$Q = \neg(A \wedge A)$$

 Idempotence axiom

Α	Q
0	1
1	0

Axioms in Boolean algebra

 Some rules help us avoid evaluating parts, because we can know the answer regardless of the values of the variables.

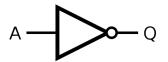
Rule	Axioms	From Lecture 2
Identity	$x \wedge 1 \equiv x$	Boolean Algebra
Null	$x \wedge 0 \equiv 0$	
Idempotence	$X \wedge X \equiv X$	
Inverse	$x \wedge \neg x \equiv 0$	

• **Duality**: Swap 0s and 1s, conjunction and disjunction. Equivalence property is preserved.

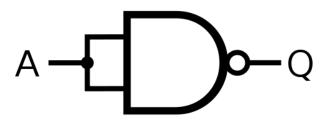


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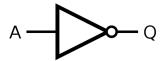
$$x \wedge x \equiv x$$

 $\neg(\underline{A} \wedge \underline{A}) \equiv \neg(\underline{A}) \equiv \neg\underline{A}$

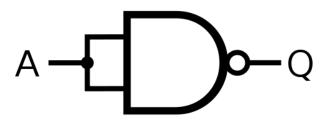
Α	Q
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W Diagram



K Boolean algebra

$$Q = \neg(A \wedge A) = \neg A$$

 Idempotence axiom

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 $\neg(\underline{A} \wedge \underline{A}) \equiv \neg(\underline{A}) \equiv \neg\underline{A}$

Α	Q
0	1
1	0



NAND is an excellent building block for other Boolean logic.

For example: AND

$$A \longrightarrow Q$$

K Algebra

W Diagram

$Q = \neg(t0)$

$$t0 = \neg (A \wedge B)$$

Α	В	t0	Q
0	0		
0	1		
1	0		
1	1		

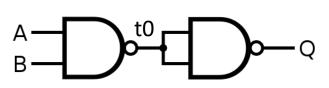




For example: AND

$$A \longrightarrow Q$$

W Diagram



$$t0 = \neg (A \wedge B)$$

K Algebra

$$Q = \neg(\neg(A \land B))$$
$$= A \land B$$

 Double negation axiom

$$\neg(\neg X) \equiv \neg \neg X \equiv X$$

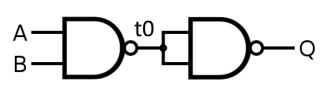
Α	В	t0	Q
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0	1		
1	0		
1	1		



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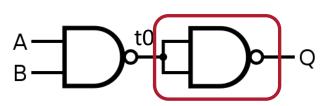


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For example: AND

$$A \longrightarrow Q$$

W Diagram



NOT gate

K Algebra

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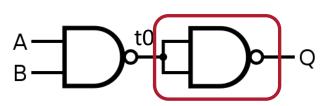


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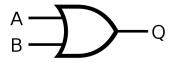
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0	1	1	0
1	0	1	0
1	1	0	1



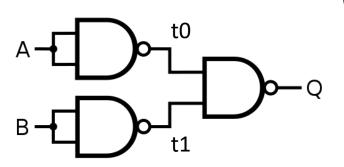
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For example: OR



W Diagram







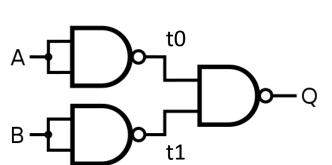
A	В	t0	t1	Q
0	0			
0	1			
1	0			
1	1			

NAND is an excellent **building block** for other Boolean logic.

For example: OR

$$A \longrightarrow Q$$

Diagram



K Algebra

$$Q = \neg(t0 \land t1)$$

$$t0 = \neg(A \land A)$$

$$t1 = \neg(B \land B)$$

Α	В	t0	t1	Q
0	0			
0	1			
1	0			
1	1			

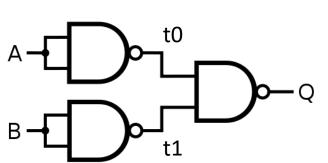


NAND is an excellent building block for other Boolean logic.

For example: OR



W Diagram



K Algebra

$$Q = \neg(\neg(A \land A) \land \neg(B \land B))$$

$$= \neg(\neg(A \land \neg B))$$

$$= \neg(\neg(A \lor B))$$

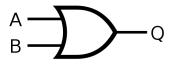
$$= A \lor B$$

A	В	t0	t1	Q
0	0			
0	1			
1	0			
1	1			

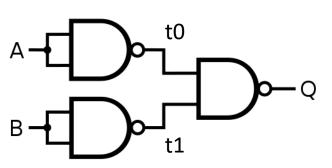


NAND is an excellent **building block** for other Boolean logic.

For example: **OR**



W Diagram



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$$= A \lor B$$

Idempotence, de Morgan and double negation

A	В	t0	t1	Q
0	0			
0	1			
1	0			
1	1			

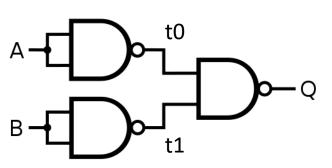


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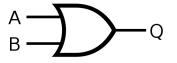
 Idempotence, de Morgan and double negation

A	В	t0	t1	Q
0	0	1	1	
0	1	1	0	
1	0	0	1	
1	1	0	0	

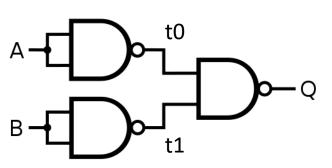


NAND is an excellent building block for other Boolean logic.

For example: OR



W Diagram



K Algebra

$$Q = \neg(\neg(A \land A) \land \neg(B \land B))$$

$$= \neg(\neg(A \land \neg B))$$

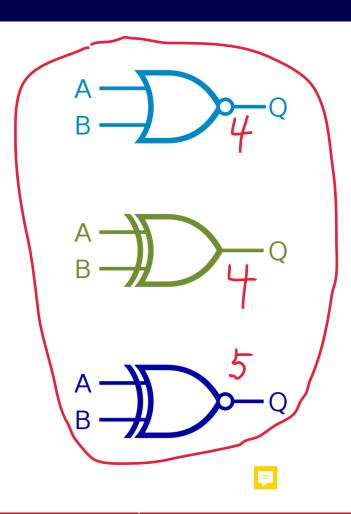
$$= \neg(\neg(A \lor B))$$

$$= A \lor B$$

 Idempotence, de Morgan and double negation

Α	В	t0	t1	Q
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	1

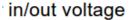


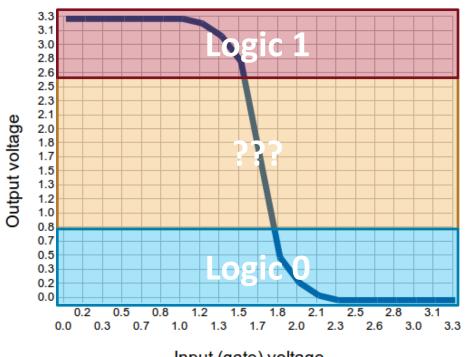


- NAND is an excellent **building** block for other Boolean logic.
- NAND is functionally complete.
 - All gates can be expressed with NAND gates arranged in various ways.
- NOT, AND, OR as previously shown.
- As well as NOR, XOR, XNOR.
 - NOR is also functionally complete.
 - NOR structure is slower than NAND.



Voltages and logic levels





Input (gate) voltage

- Simplified view so far.
- Ideal would be a rightangled response.
- Steepness and position of curve depend on transistor properties.
- There is also a delay between a change in input producing a change in output.
- This delay accounts for the physical signal propagation time in silicon.



COMSM1302 NAND Lab 1-3



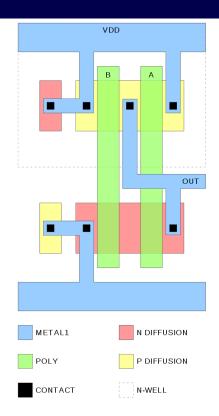
- NAND boards have either been sent to you or are ready for you to collect.
- The NAND boards are for you to work on your lab sheets during scheduled lab hours or on your own.
- Please be careful with the NAND boards. They have sharp edges and are sensitive electronic devices.

Summary

- Switches
 - Mechanical
 - Thermionic
 - Silicon
- Transistors
- CMOS
 - Inverter
 - NAND (functionally complete)
 - Making other gates from NAND
- More about how chips are made:

https://www.youtube.com/watch?v=qm67wbB5GmI https://www.youtube.com/watch?v=4FLBtQC0F0c https://www.youtube.com/watch?v=i8kxymmjdoM and this is also quite cool:

https://www.youtube.com/watch?v=Y33cf-lcq-g



The physical layout of a NAND circuit. [Source: By Jamesm76 at English Wikipedia -

Transferred from en.wikipedia to Commons., Public Domain, https://commons.wikimedia.org/w/index.php?curid=2944/



In this lecture

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Data representation, logic, Boolean algebra.

Building blocks

• Transistors, transistor based logic, simple devices, storage.

Modules

 Memory, simple controllers, FSMs, processors and execution.

Programming

 Machine code, assembly, high-level languages, compilers.

Wrap-up

Operating systems, energy aware computing.



K In the next lecture

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