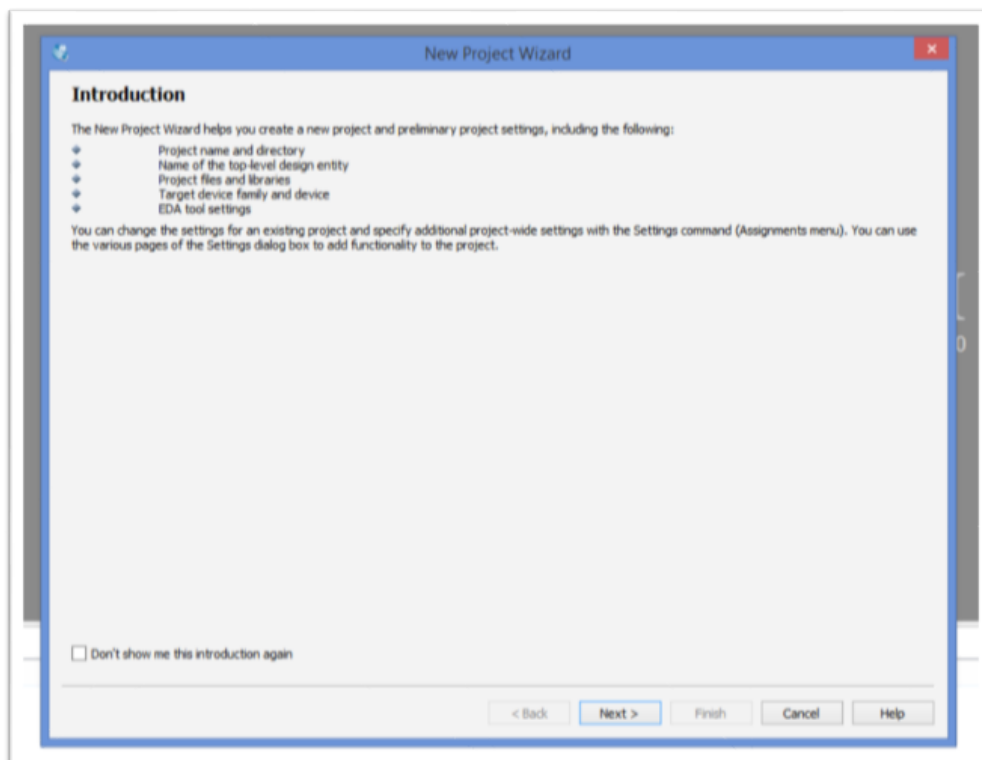


# Introduction to Quartus II Software

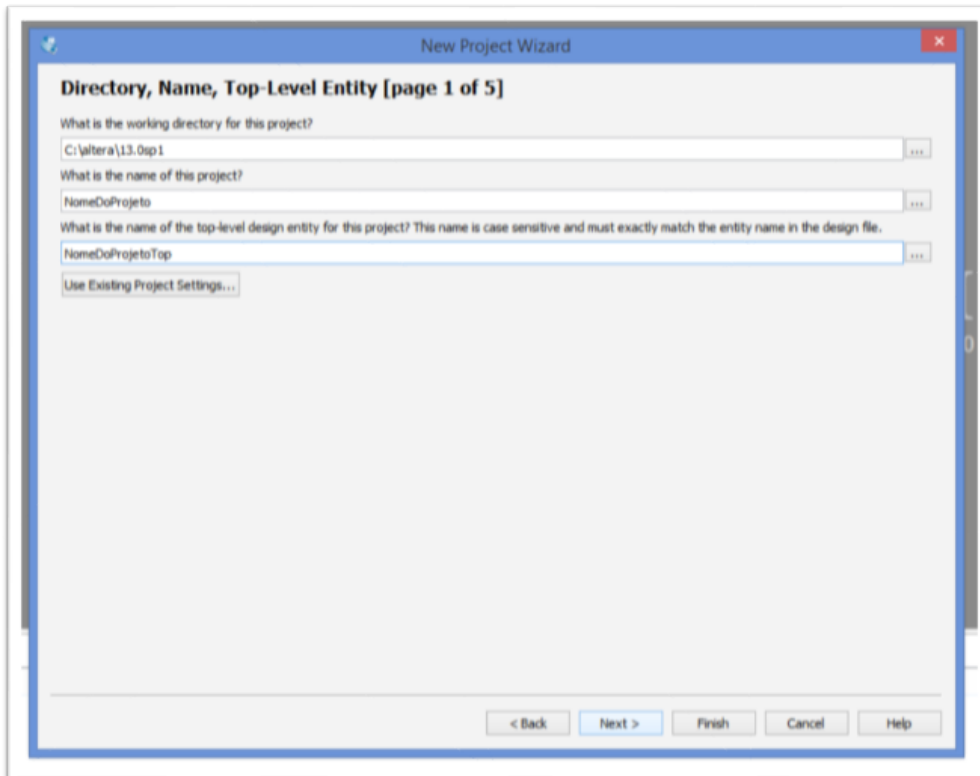
The present text present a quick starting steps to simulate a digital circuit

## Building a Circuit

Start Quartus II and select Create a new project.



Choose a Directory, name and Top-level entity for your project



The screenshot shows the first page of the 'New Project Wizard' dialog box. The title bar reads 'New Project Wizard'. The main heading is 'Directory, Name, Top-Level Entity [page 1 of 5]'. There are three text input fields with '...' buttons to their right. The first field is labeled 'What is the working directory for this project?' and contains 'C:\altera\13.0sp1'. The second field is labeled 'What is the name of this project?' and contains 'NoneDoProjeto'. The third field is labeled 'What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.' and contains 'NoneDoProjetoTop'. Below these fields is a button labeled 'Use Existing Project Settings...'. At the bottom right are five buttons: '< Back', 'Next >', 'Finish', 'Cancel', and 'Help'.

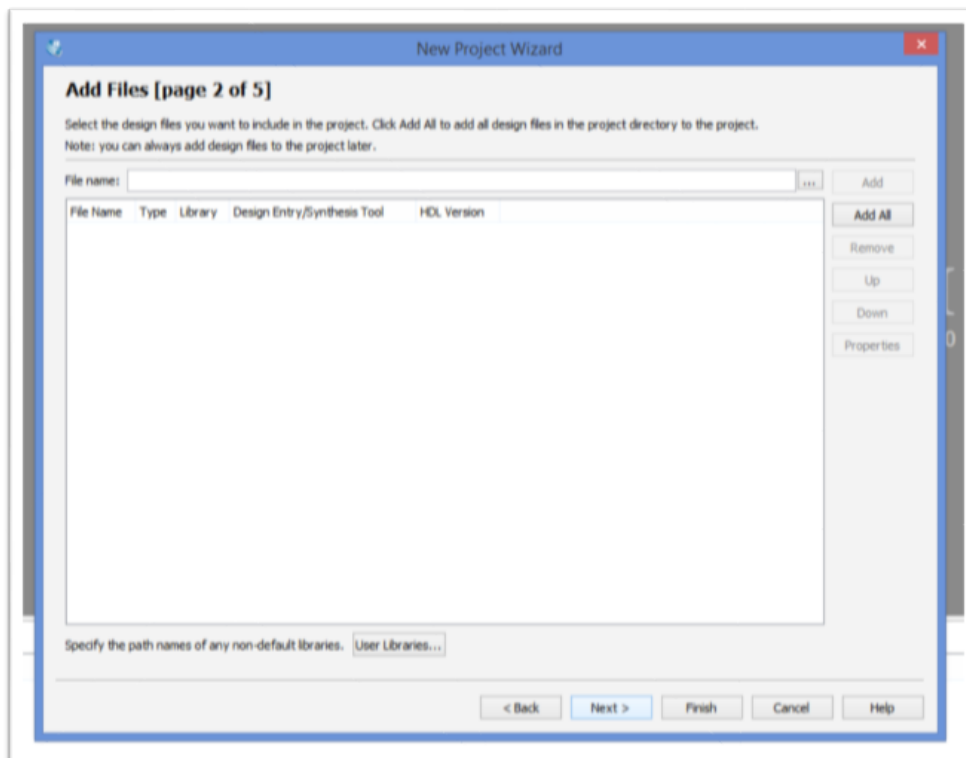
What is the working directory for this project?  
C:\altera\13.0sp1

What is the name of this project?  
NoneDoProjeto

What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.  
NoneDoProjetoTop

Use Existing Project Settings...

< Back Next > Finish Cancel Help



The screenshot shows the second page of the 'New Project Wizard' dialog box. The title bar reads 'New Project Wizard'. The main heading is 'Add Files [page 2 of 5]'. Below the heading is a paragraph: 'Select the design files you want to include in the project. Click Add All to add all design files in the project directory to the project. Note: you can always add design files to the project later.' There is a 'File name:' text input field with a '...' button to its right. Below this is a table with columns: 'File Name', 'Type', 'Library', 'Design Entry/Synthesis Tool', and 'HDL Version'. To the right of the table are buttons: 'Add', 'Add All', 'Remove', 'Up', 'Down', and 'Properties'. At the bottom left is a text input field labeled 'Specify the path names of any non-default libraries.' with a 'User Libraries...' button to its right. At the bottom right are five buttons: '< Back', 'Next >', 'Finish', 'Cancel', and 'Help'.

Select the design files you want to include in the project. Click Add All to add all design files in the project directory to the project. Note: you can always add design files to the project later.

File name:

File Name	Type	Library	Design Entry/Synthesis Tool	HDL Version
-----------	------	---------	-----------------------------	-------------

Add Add All Remove Up Down Properties

Specify the path names of any non-default libraries. User Libraries...

< Back Next > Finish Cancel Help

Choose the device family (Quartus II) and the specific device (EP2CBQ208c8)

New Project Wizard

### Family & Device Settings [page 3 of 5]

Select the family and device you want to target for compilation.  
You can install additional device support with the Install Devices command on the Tools menu.

Device family  
Family: **Cyclone II**  
Devices: **All**

Target device  
☐ Auto device selected by the Fitter  
☒ Specific device selected in 'Available devices' list  
☐ Other: n/a

Show in 'Available devices' list  
Package: **Any**  
Pin count: **Any**  
Speed grade: **Any**  
Name filter:   
☒ Show advanced devices ☐ HardCopy compatible only

Available devices:

Name	Core Voltage	LEs	User I/Os	Memory Bits	Embedded multiplier 9-bit elements	PLL	G
EP2CBF256I8	1.2V	8256	182	165888	36	2	8
EP2CBQ208C7	1.2V	8256	138	165888	36	2	8
<b>EP2CBQ208C8</b>	<b>1.2V</b>	<b>8256</b>	<b>138</b>	<b>165888</b>	<b>36</b>	<b>2</b>	<b>8</b>
EP2CBQ208I8	1.2V	8256	138	165888	36	2	8
EP2CBT144C6	1.2V	8256	85	165888	36	2	8
EP2CBT144C7	1.2V	8256	85	165888	36	2	8
EP2CBT144C8	1.2V	8256	85	165888	36	2	8

Companion device  
HardCopy:   
☐ Limit DSP & RAM to HardCopy device resources

< Back Next > Finish Cancel Help

New Project Wizard

### EDA Tool Settings [page 4 of 5]

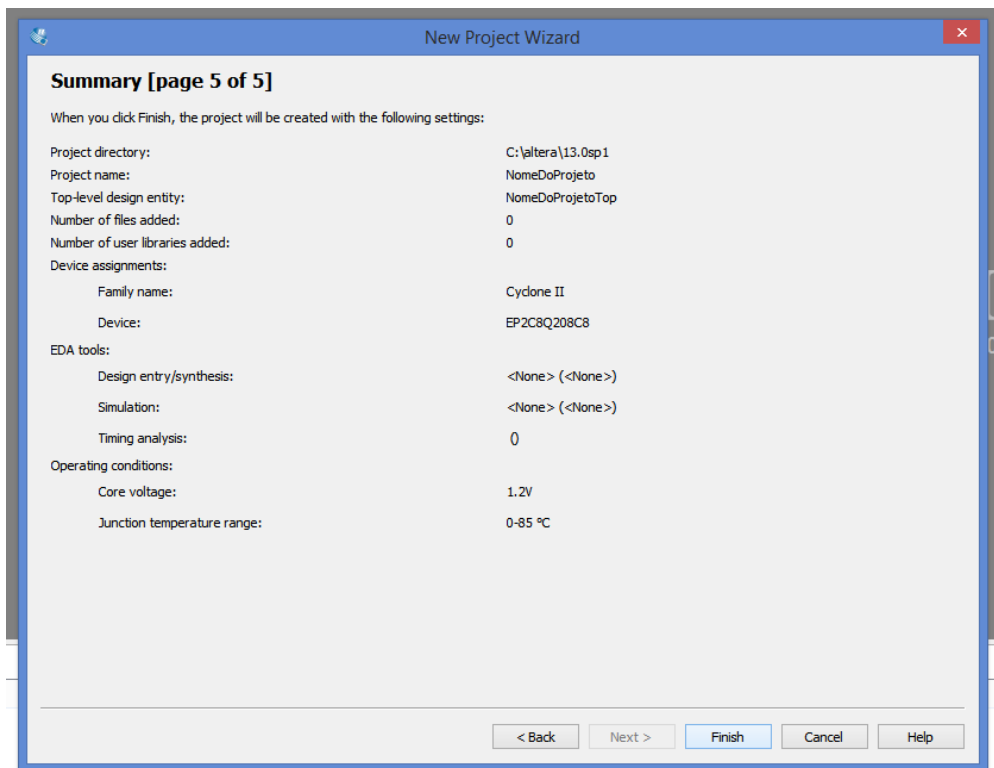
Specify the other EDA tools used with the Quartus II software to develop your project.

EDA tools:

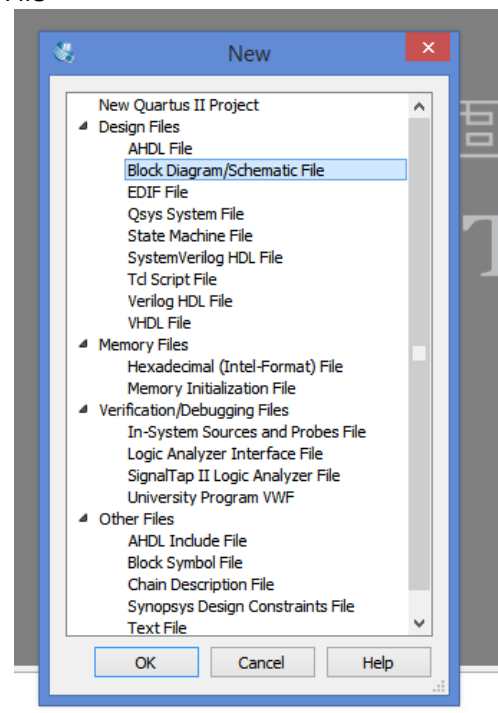
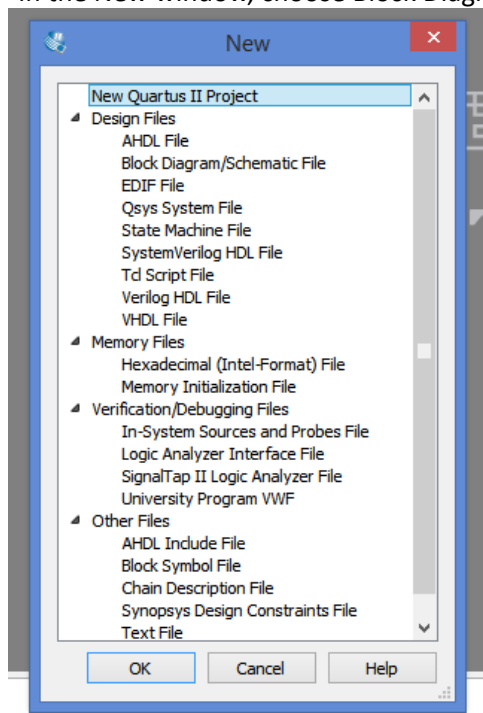
Tool Type	Tool Name	Format(s)	Run Tool Automatically
Design Entry/Synthesis	<None>	<None>	<input type="checkbox"/> Run this tool automatically to synthesize the current design
Simulation	<None>	<None>	<input type="checkbox"/> Run gate-level simulation automatically after compilation
Formal Verification	<None>	<None>	
Board-Level	Timing	<None>	
	Symbol	<None>	
	Signal Integrity	<None>	
	Boundary Scan	<None>	

< Back Next > Finish Cancel Help

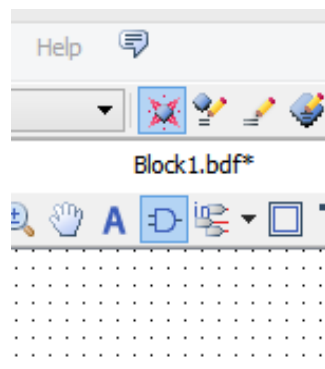
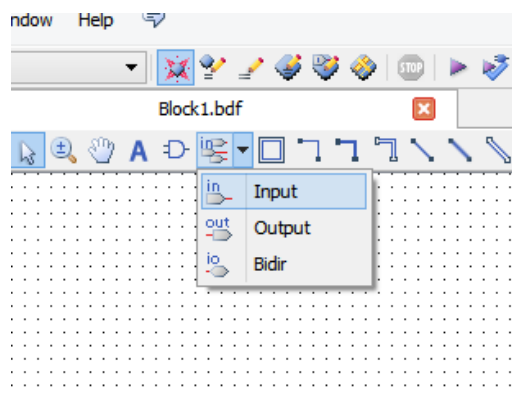
Check the Summary of your project before creating



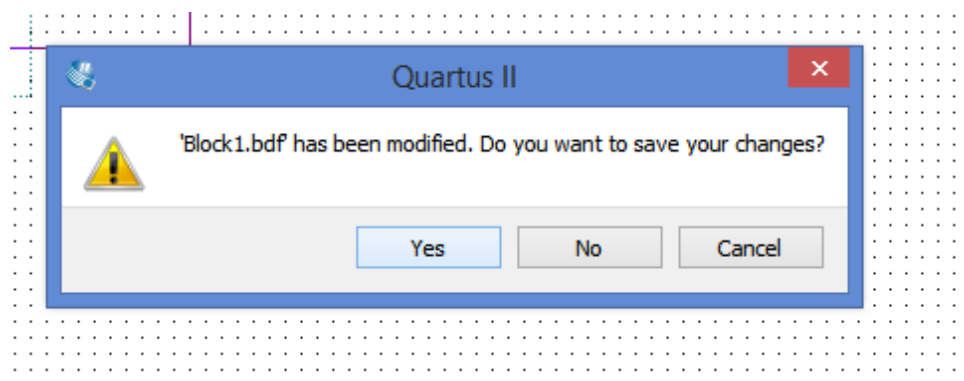
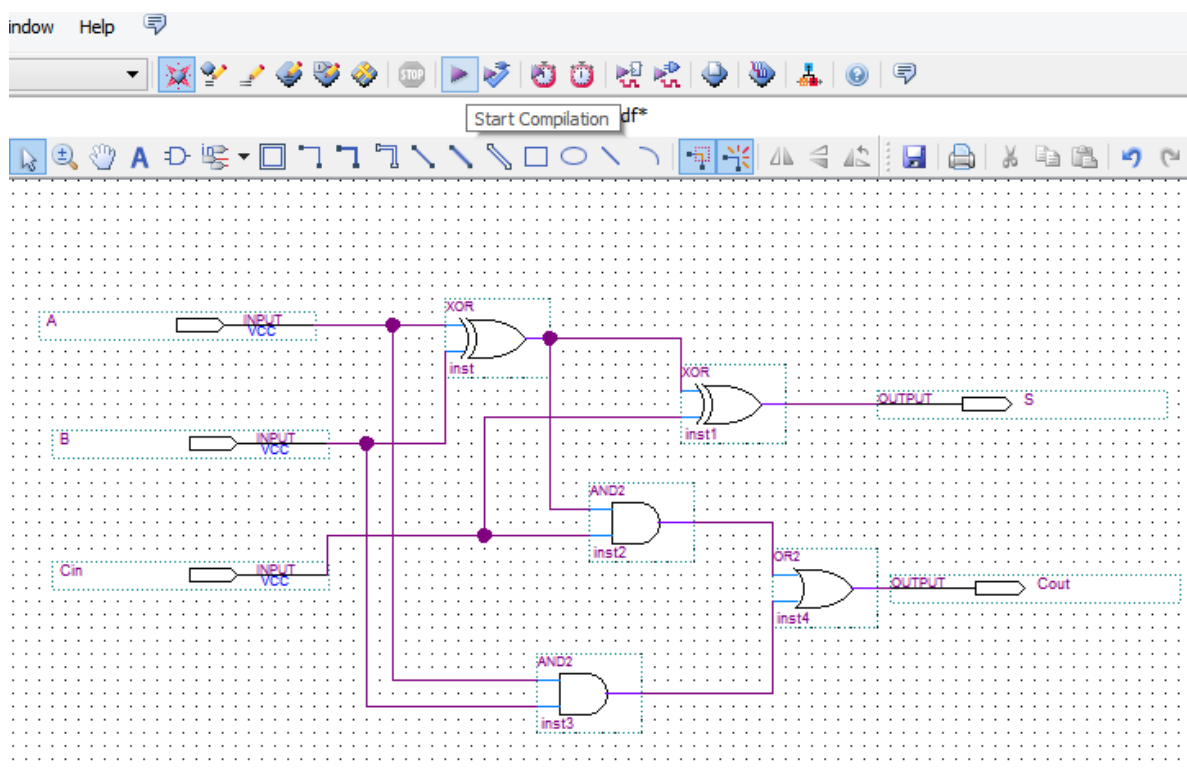
In the New window, choose Block Diagram/Schematic File

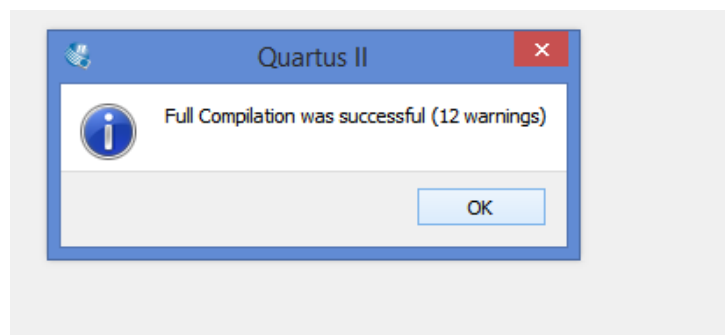
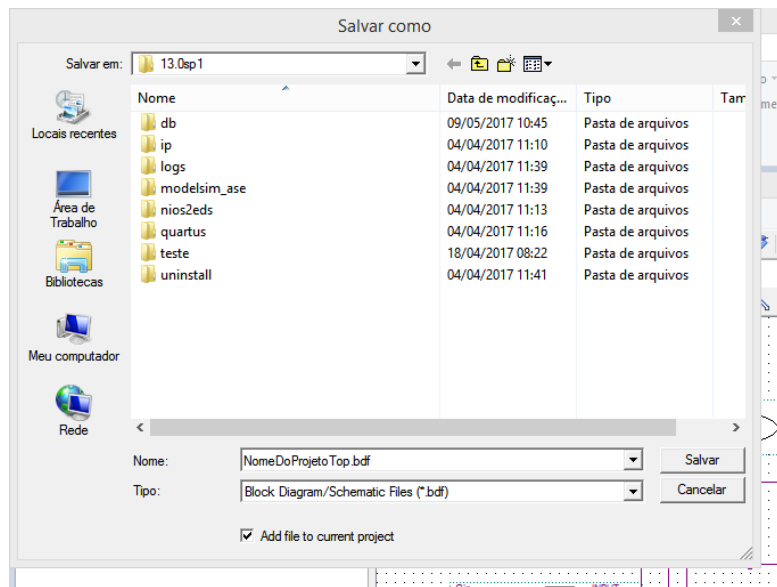


Start with the circuit building



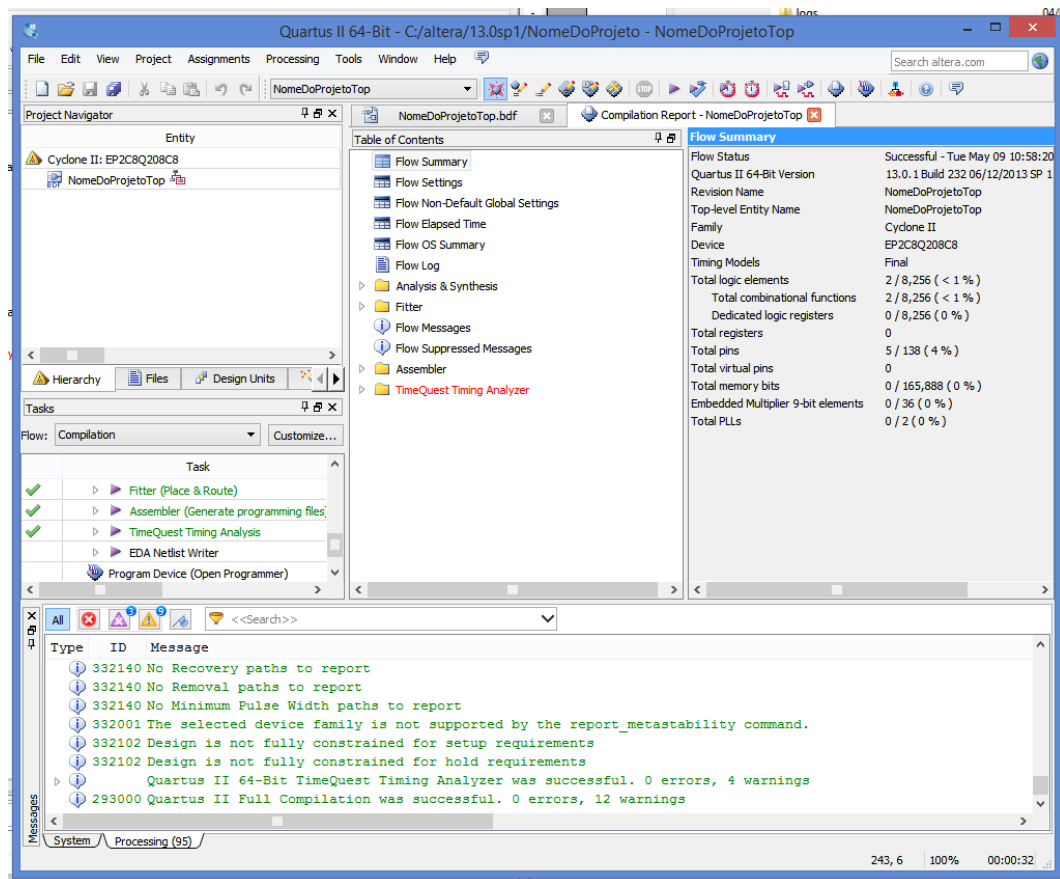
For example a circuit of a Full adder, save changes and start compilation.



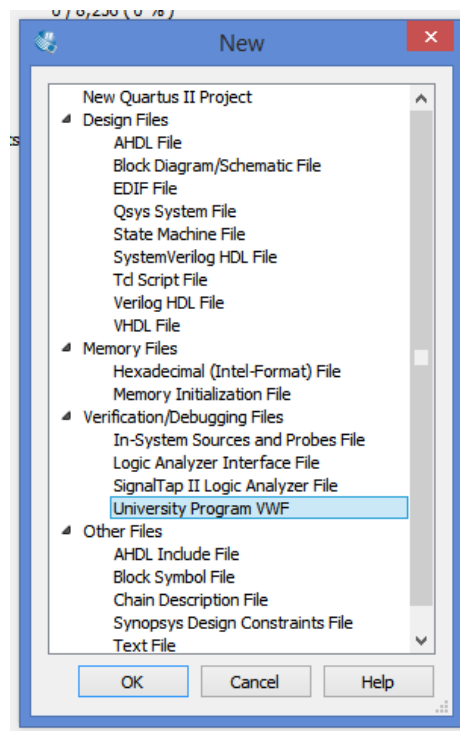


Simulating the Circuit

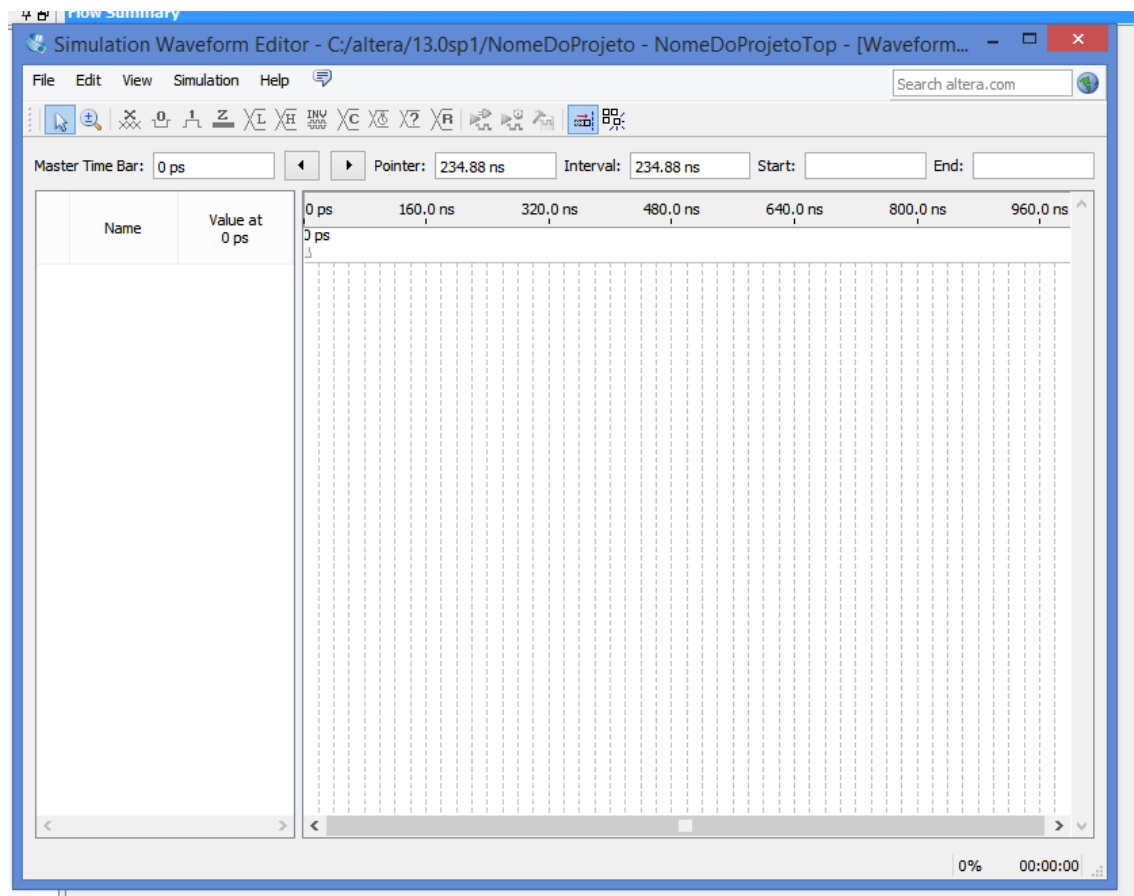
In the environment:



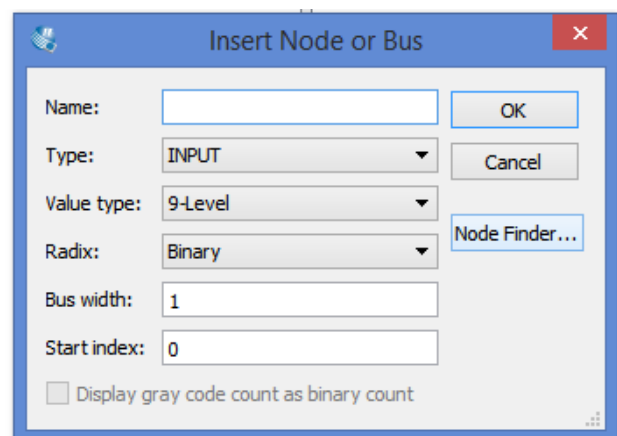
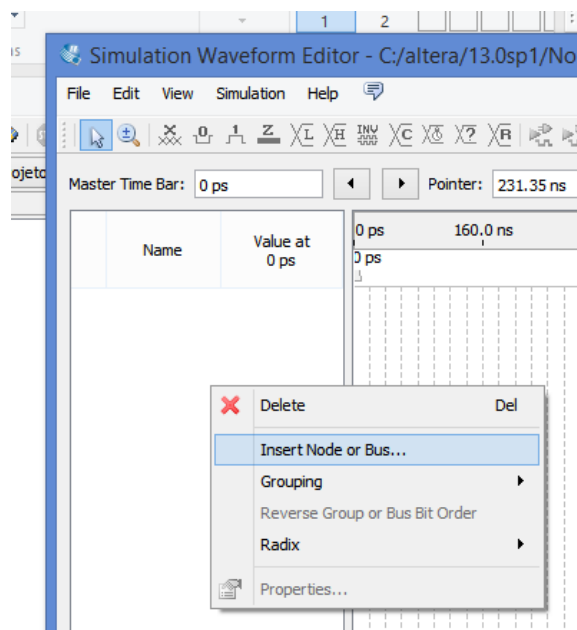
Go to the New window and select University program VWF



In the Simulation waveform editor,

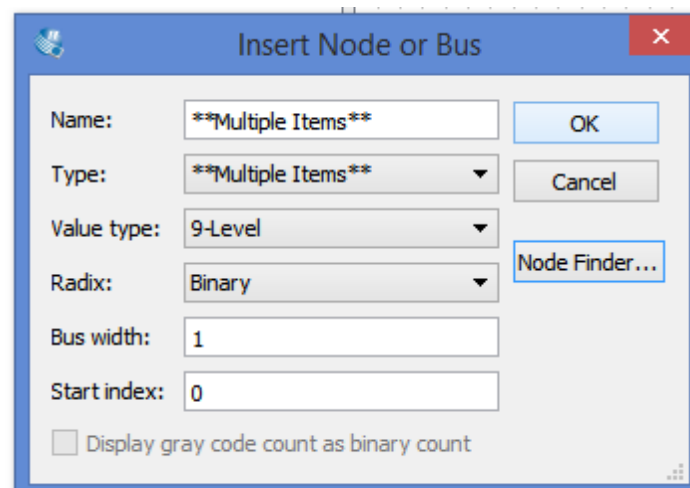
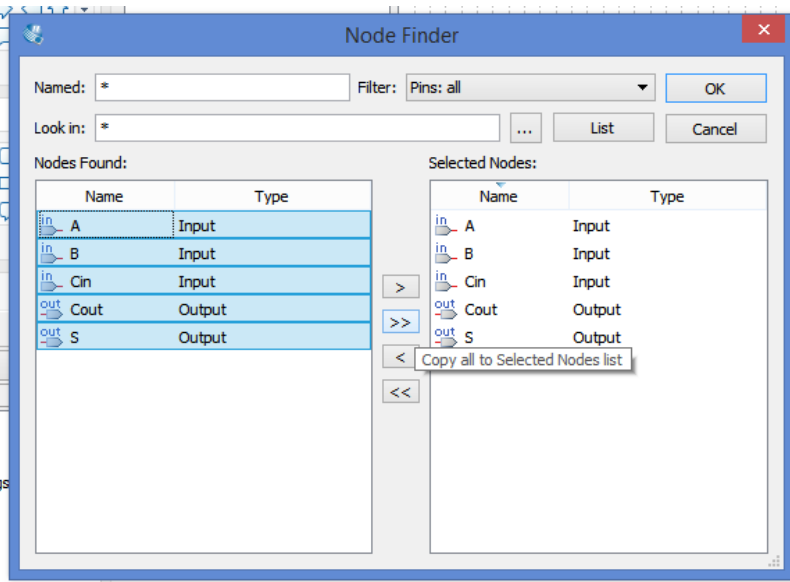
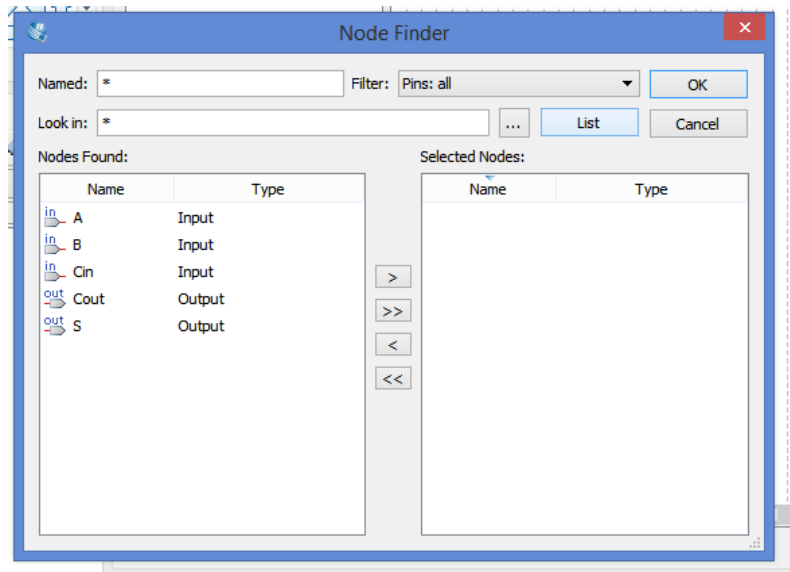


Select the inputs and outputs by right clicking and choosing Node finder command

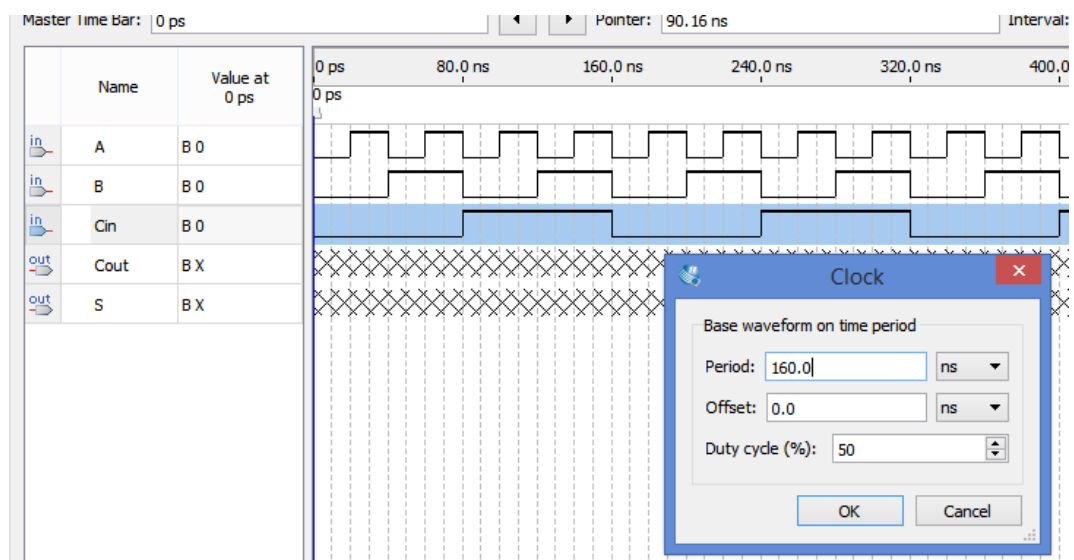
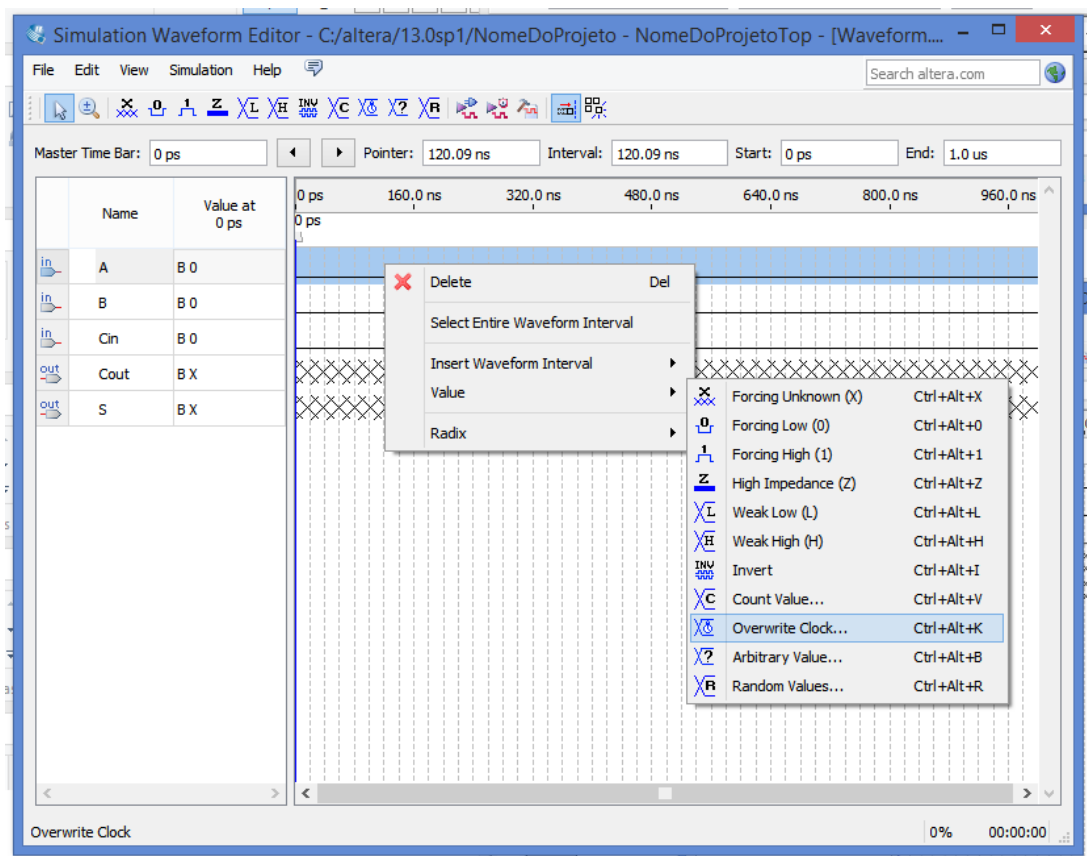




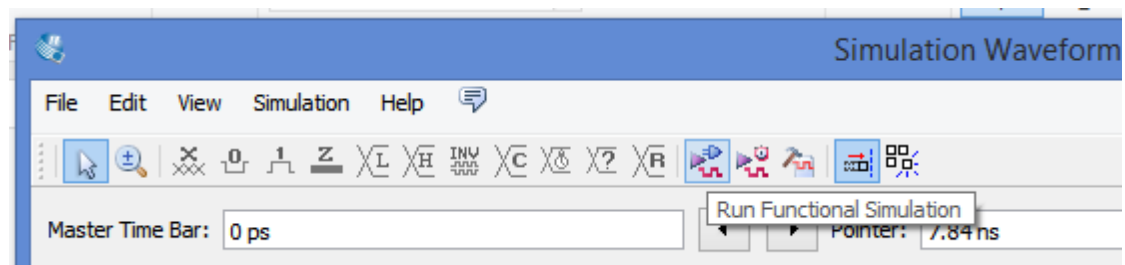
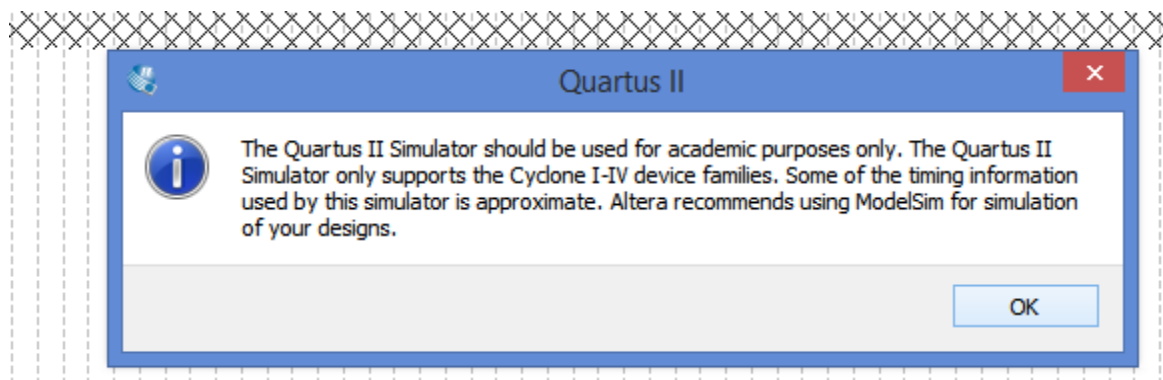
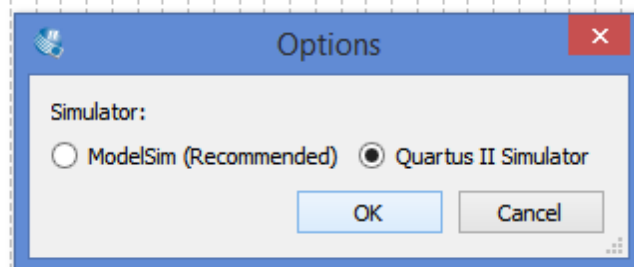
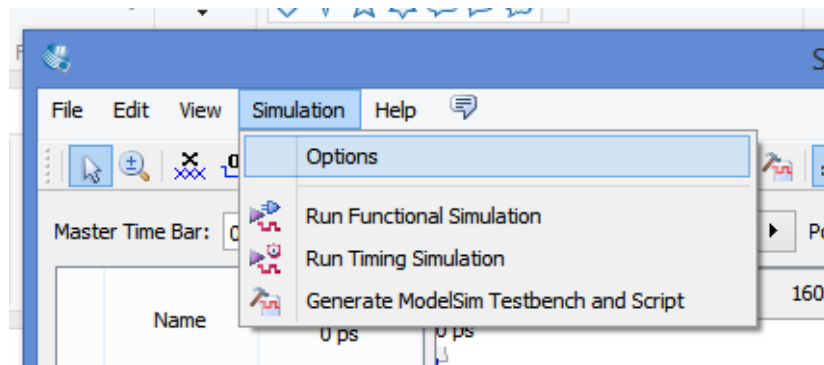
In the node finder, select all inputs and outputs



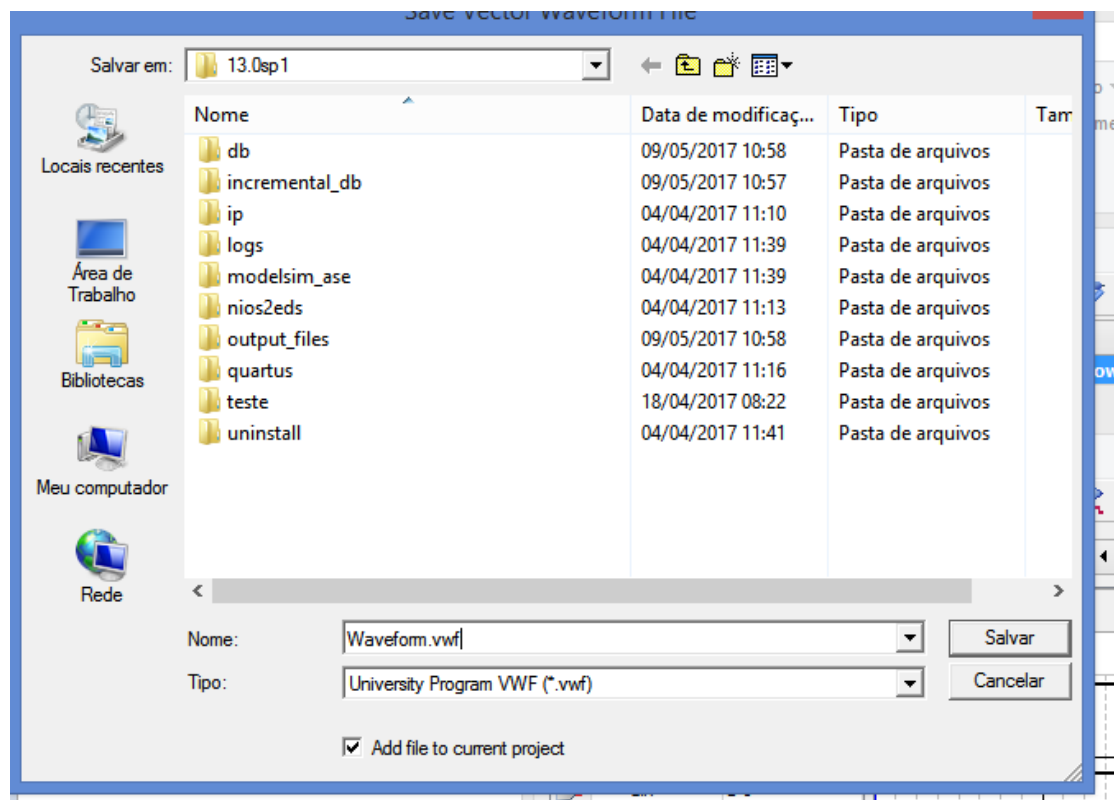
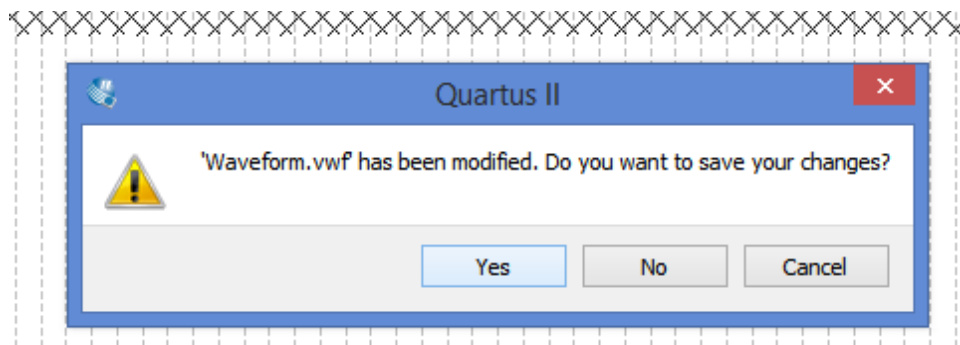
In the Waveform window, set the waveform of the inputs (overwrite clock)



Next, Run simulation; select Quartus II simulator

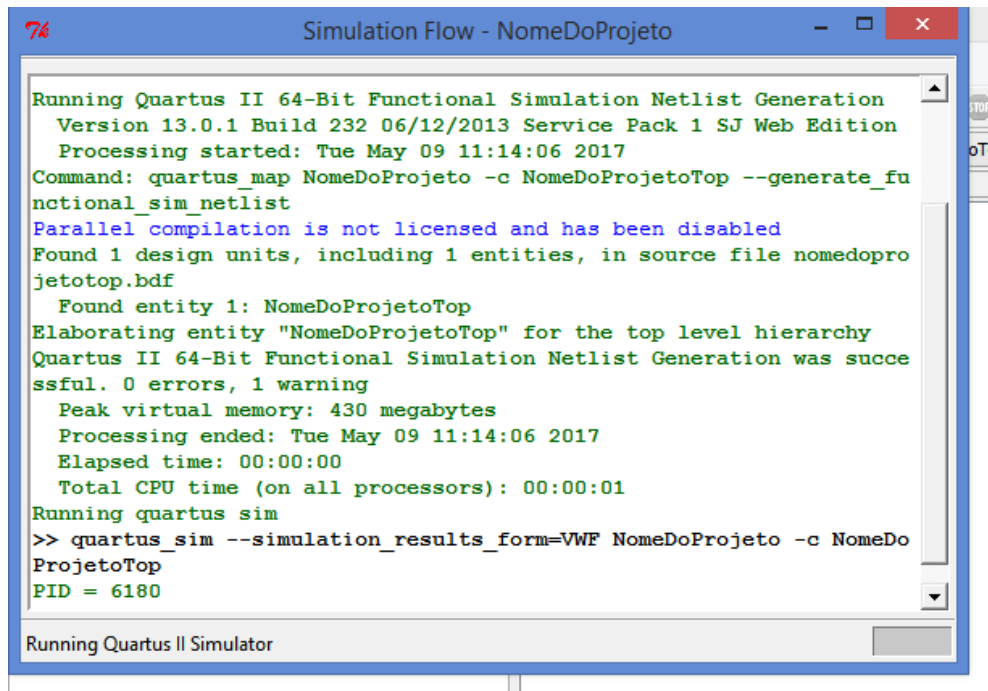


And save changes



## Results

### Simulation flow window



```
Running Quartus II 64-Bit Functional Simulation Netlist Generation
Version 13.0.1 Build 232 06/12/2013 Service Pack 1 SJ Web Edition
Processing started: Tue May 09 11:14:06 2017
Command: quartus_map NomeDoProjeto -c NomeDoProjetoTop --generate_fu
nctional_sim_netlist
Parallel compilation is not licensed and has been disabled
Found 1 design units, including 1 entities, in source file namedopro
jetotop.bdf
Found entity 1: NomeDoProjetoTop
Elaborating entity "NomeDoProjetoTop" for the top level hierarchy
Quartus II 64-Bit Functional Simulation Netlist Generation was succe
ssful. 0 errors, 1 warning
Peak virtual memory: 430 megabytes
Processing ended: Tue May 09 11:14:06 2017
Elapsed time: 00:00:00
Total CPU time (on all processors): 00:00:01
Running quartus sim
>> quartus_sim --simulation_results_form=VWF NomeDoProjeto -c NomeDo
ProjetoTop
PID = 6180

Running Quartus II Simulator
```

### Waveform of outputs

