Eletrônica digital

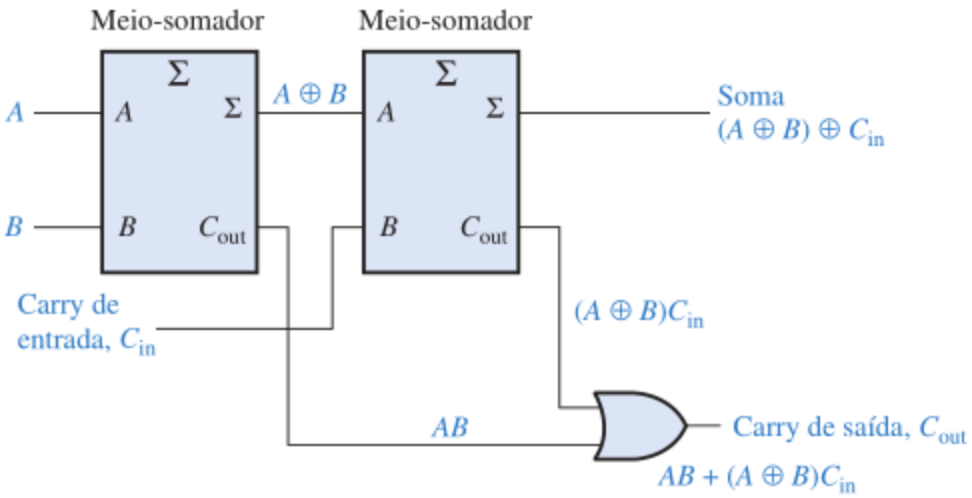
Funções de lógica digital

Introdução

- Circuitos lógicos combinacionais podem ser projetados usando álgebra booleana
- Somadores, comparadores, decodificadores, codificadores, conversores de código, multiplexadores, demultiplexadores e geradores/verificadores de paridade
- Existem CI de função fixa que realizam as mesmas operações

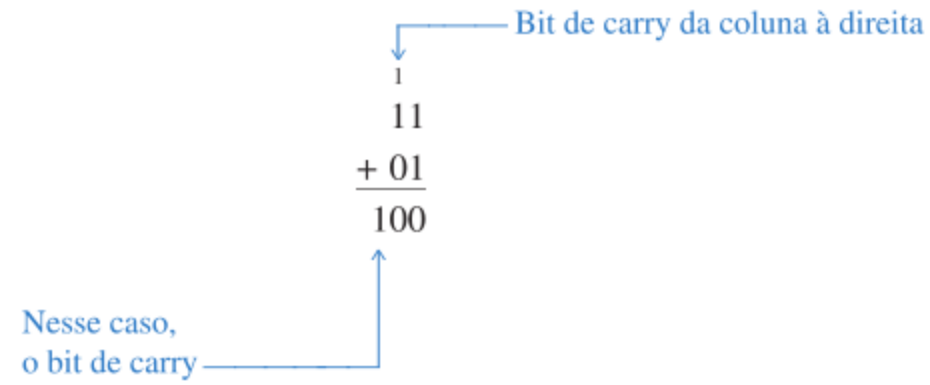
Somador

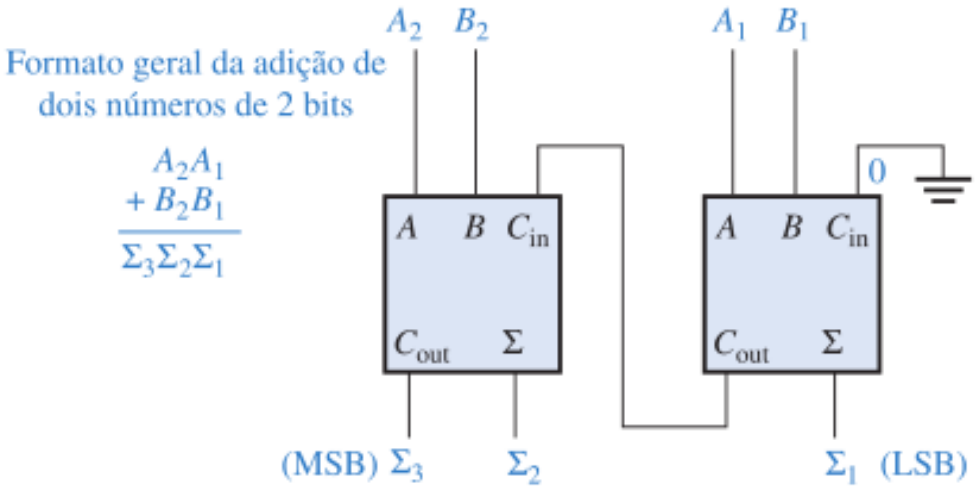
- Meio somador (half adder)
- Somador completo (full adder)



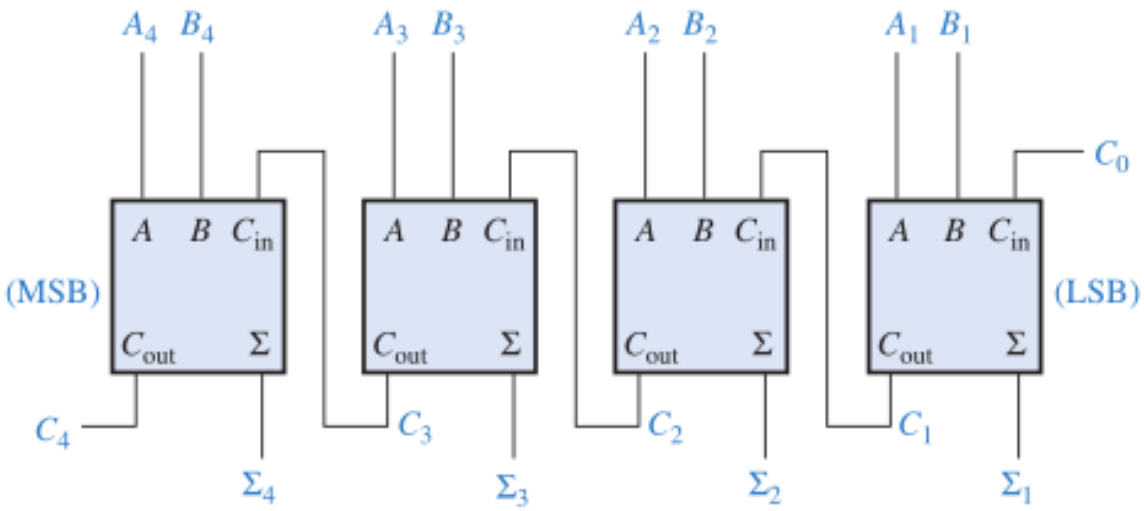
(a) Associação de dois meio-somadores para construir um somador-completo.

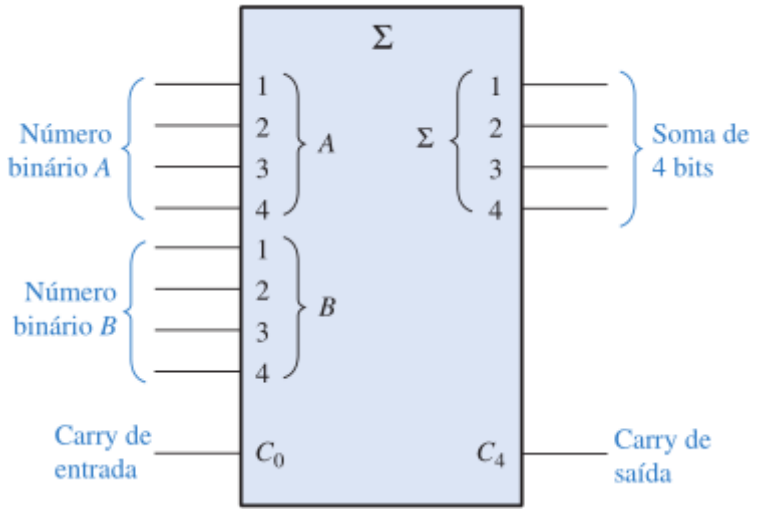
Somador paralelo



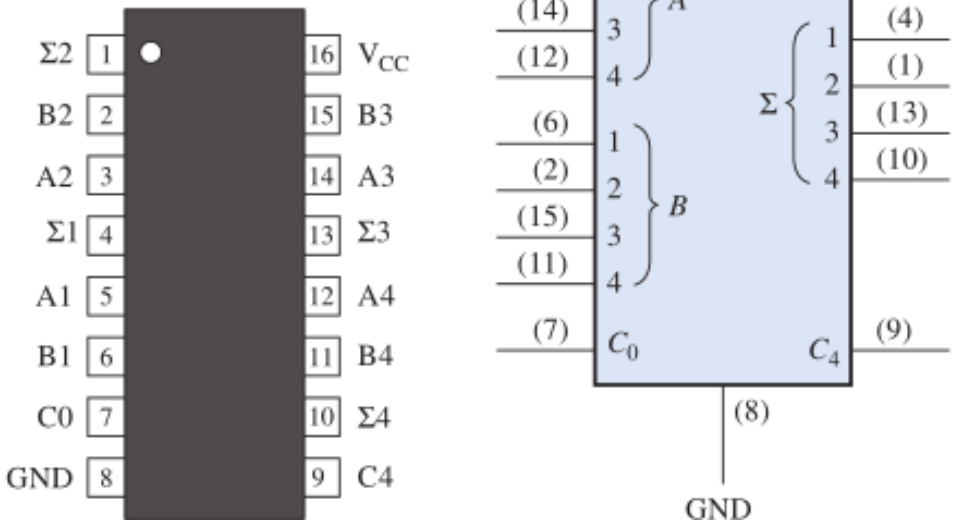


Somador paralelo de 4 bits

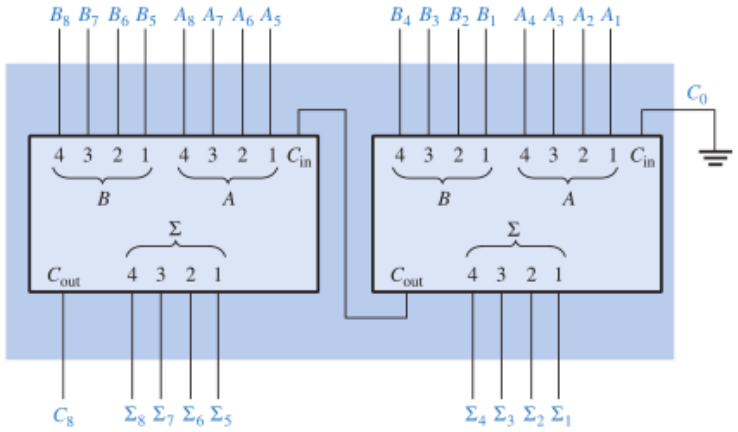




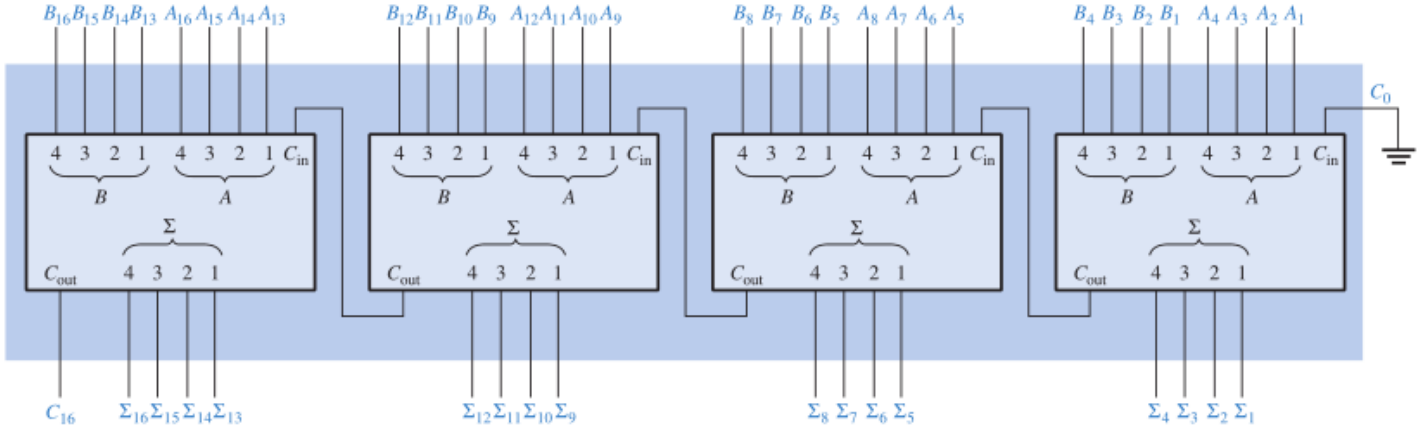
Somador paralelo de 4 bits (74LS283)



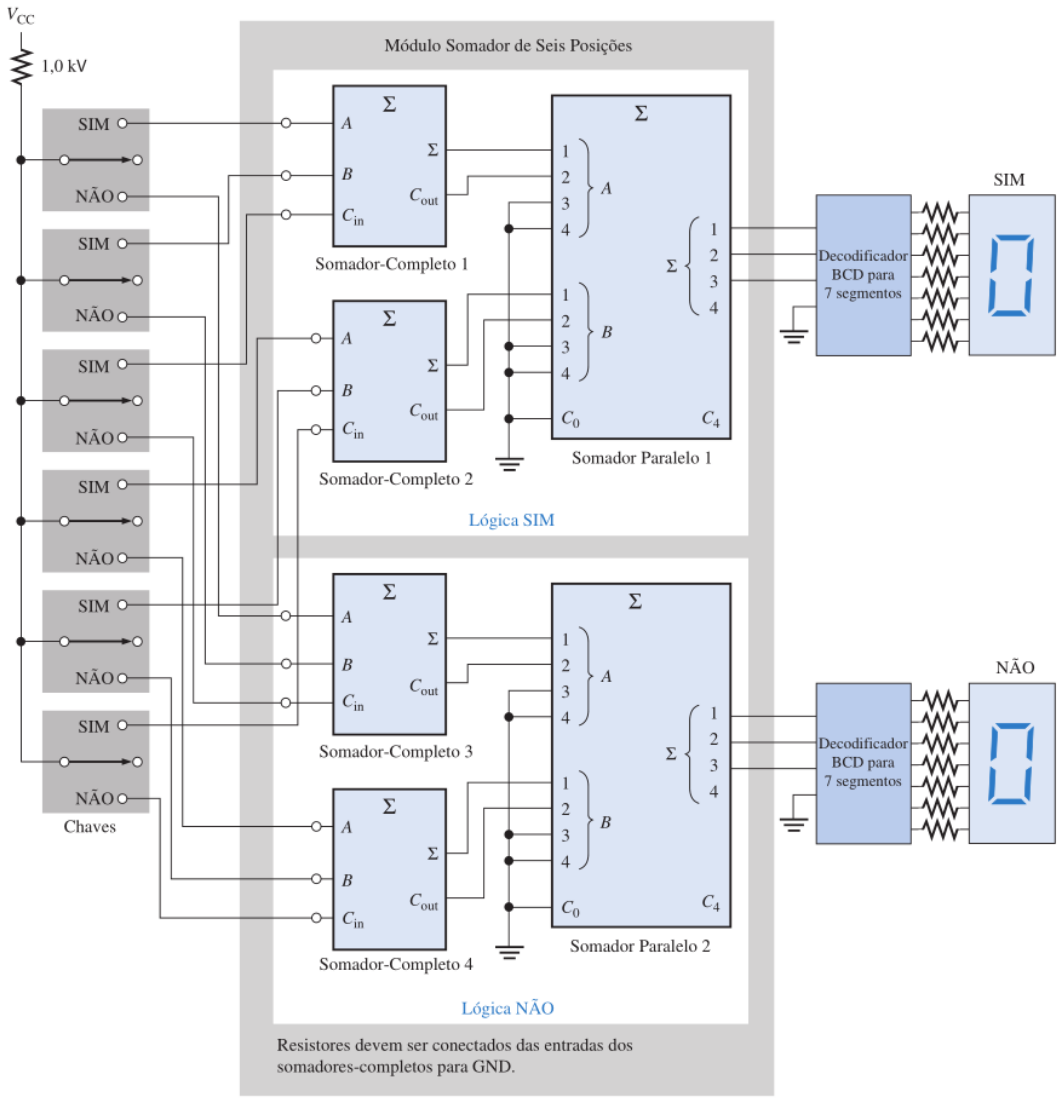
Expansão de um somador



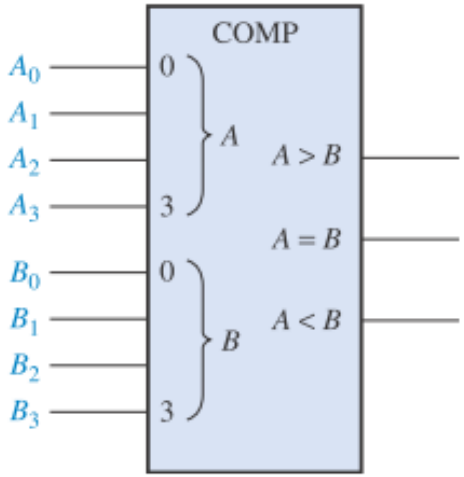
(a) Associação em cascata de dois somadores de 4 bits para construir um somador de 8 bits.

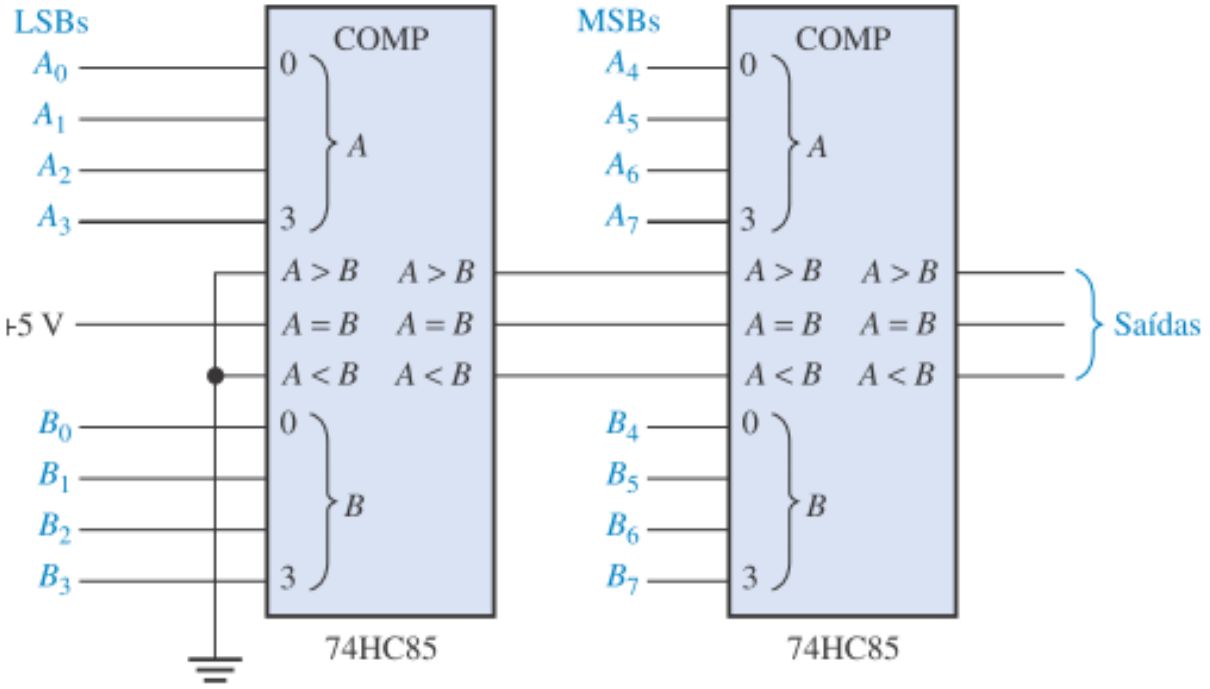


Expansão de um somador

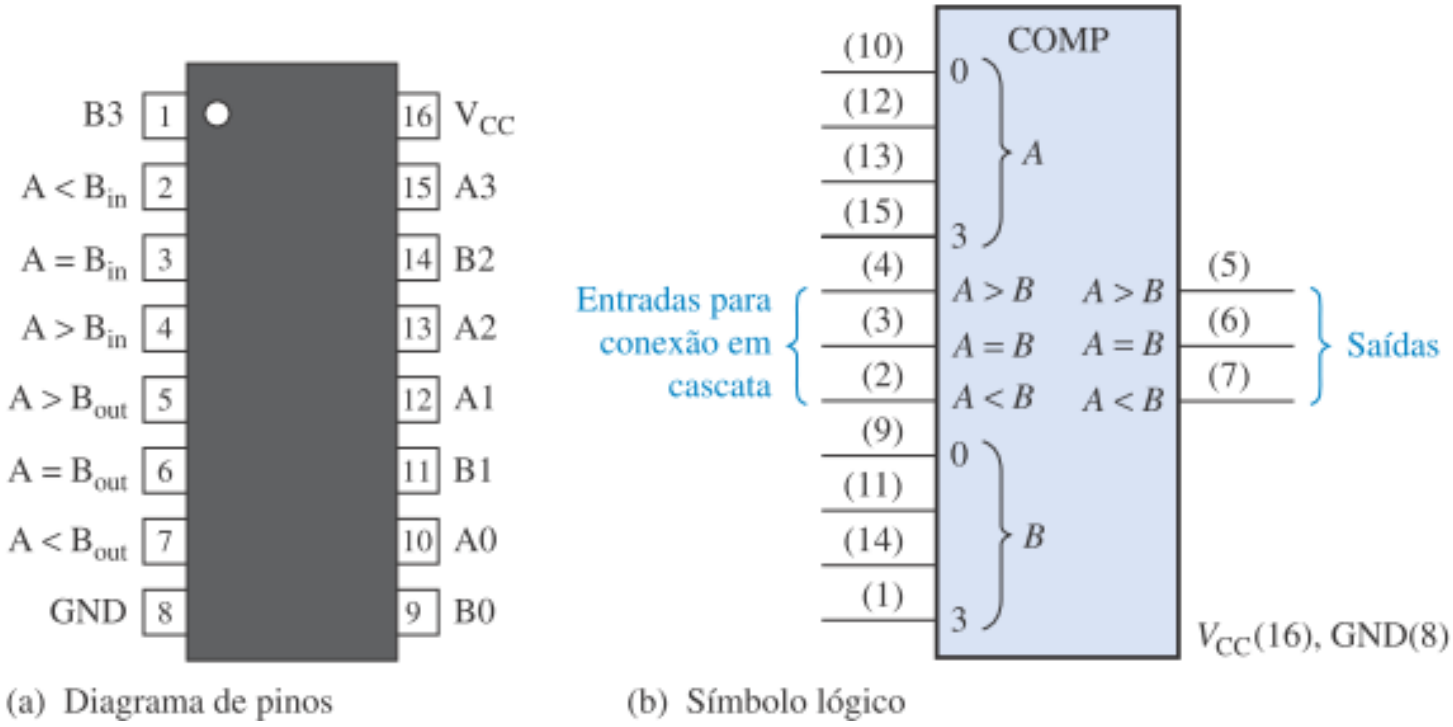


Comparador

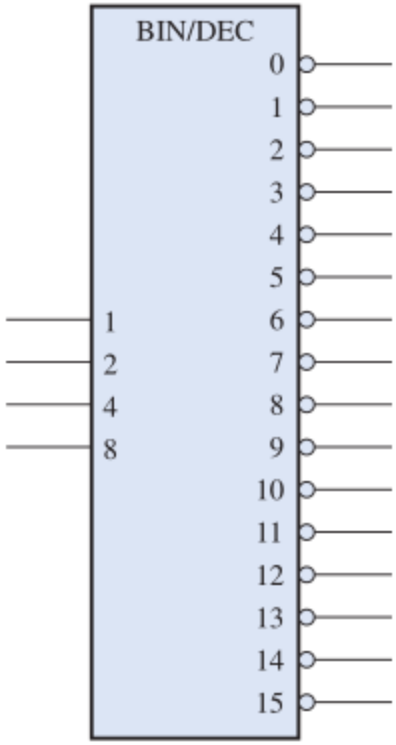

COMP
A_0
A_1
A_2
A_3
0
A
3
$A > B$
$A = B$
$A < B$
B_0
B_1
B_2
B_3
0
B
3


LSBs
COMP
A_0
A_1
A_2
A_3
0
A
3
$A > B$ $A > B$
+5 V
$A = B$ $A = B$
$A < B$ $A < B$
B_0
B_1
B_2
B_3
0
B
3
74HC85
MSBs
COMP
A_4
A_5
A_6
A_7
0
A
3
$A > B$ $A > B$
$A = B$ $A = B$
$A < B$ $A < B$
B_4
B_5
B_6
B_7
0
B
3
74HC85
Saídas

Comparador 74HC85

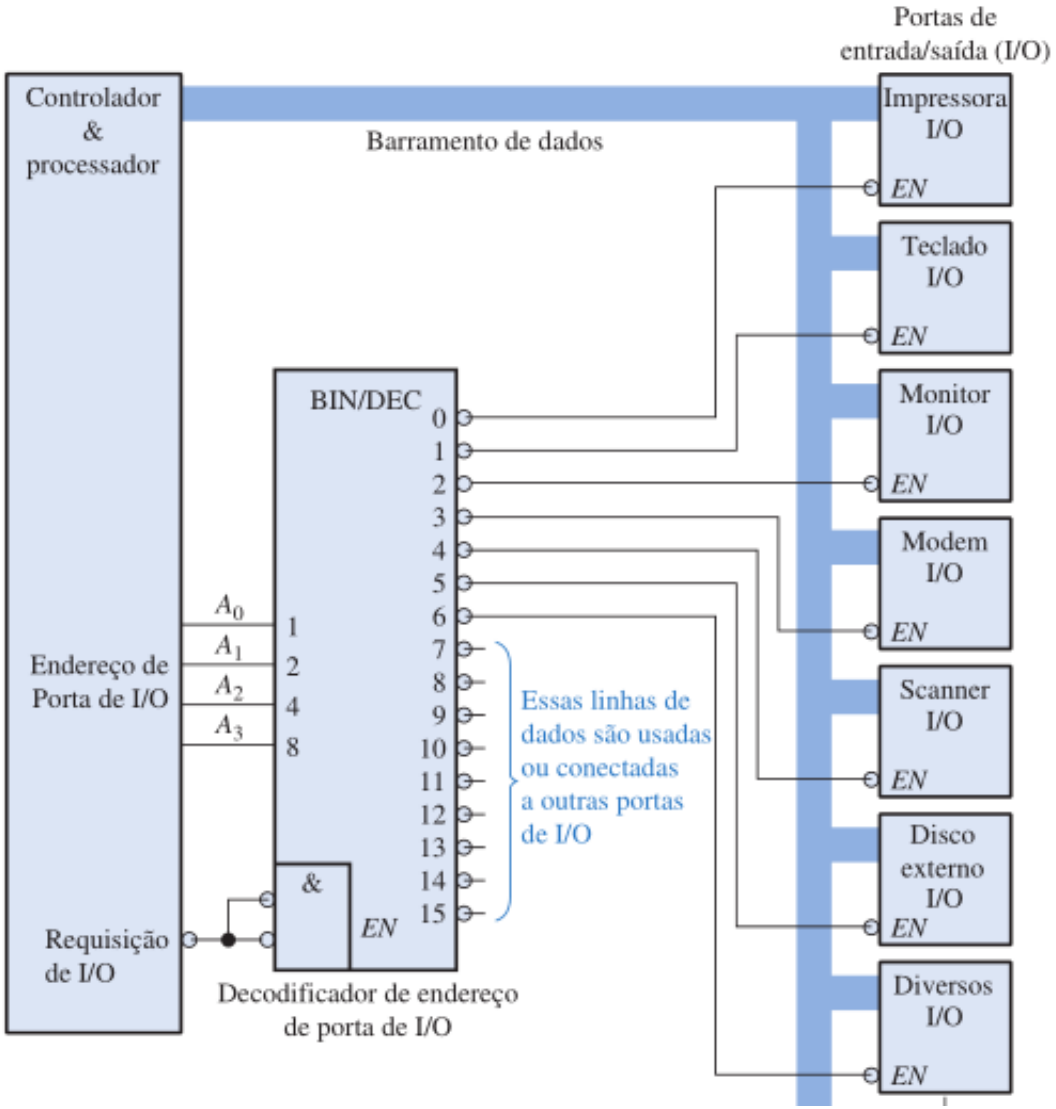


Decodificador

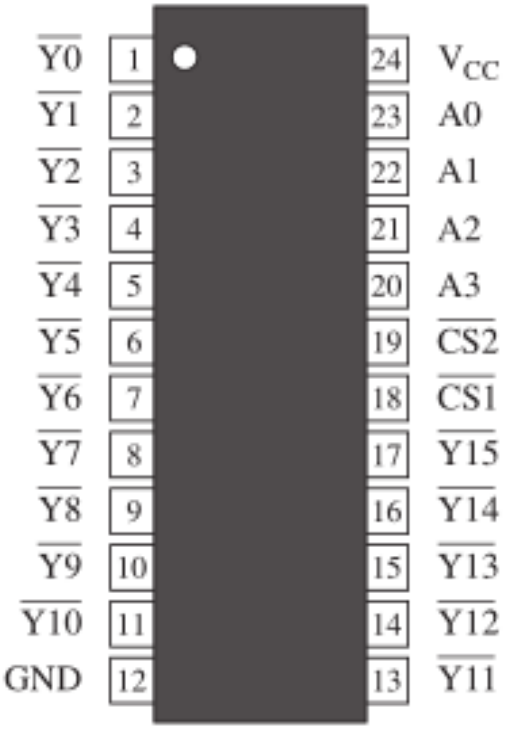


DÍGITO DECIMAL	ENTRADAS BINÁRIAS A_3	A_2	A_1	A_0	FUNÇÃO DE DECODIFICAÇÃO	SAÍDAS 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	$\overline{A}_3\overline{A}_2\overline{A}_1\overline{A}_0$	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	0	0	1	$\overline{A}_3\overline{A}_2\overline{A}_1A_0$	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	0	0	1	0	$\overline{A}_3\overline{A}_2A_1\overline{A}_0$	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
3	0	0	1	1	$\overline{A}_3\overline{A}_2A_1A_0$	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
4	0	1	0	0	$\overline{A}_3A_2\overline{A}_1\overline{A}_0$	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
5	0	1	0	1	$\overline{A}_3A_2\overline{A}_1A_0$	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
6	0	1	1	0	$\overline{A}_3A_2A_1\overline{A}_0$	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
7	0	1	1	1	$\overline{A}_3A_2A_1A_0$	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
8	1	0	0	0	$A_3\overline{A}_2\overline{A}_1\overline{A}_0$	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
9	1	0	0	1	$A_3\overline{A}_2\overline{A}_1A_0$	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
10	1	0	1	0	$A_3\overline{A}_2A_1\overline{A}_0$	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
11	1	0	1	1	$A_3\overline{A}_2A_1A_0$	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
12	1	1	0	0	$A_3A_2\overline{A}_1\overline{A}_0$	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
13	1	1	0	1	$A_3A_2\overline{A}_1A_0$	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
14	1	1	1	0	$A_3A_2A_1\overline{A}_0$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
15	1	1	1	1	$A_3A_2A_1A_0$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

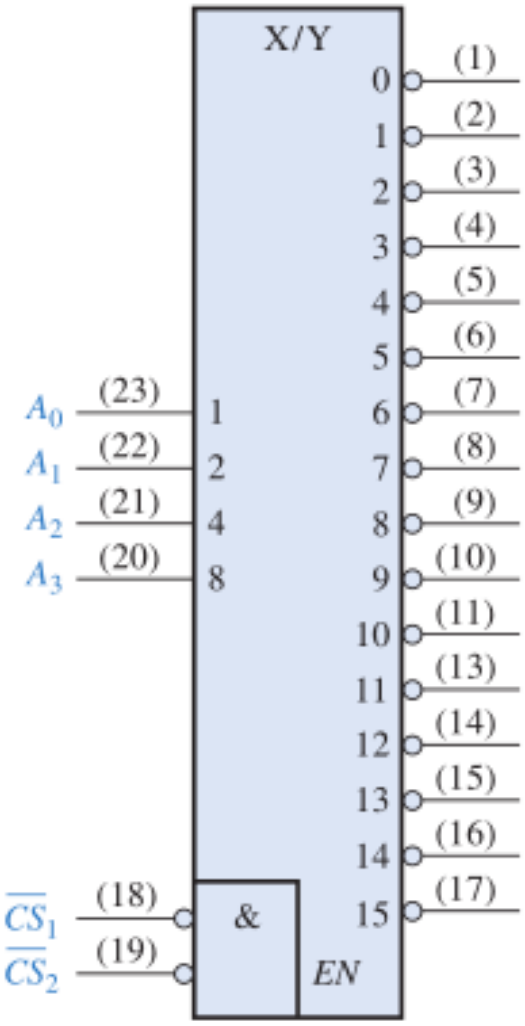
Decodificador



Decodificador 74HC154

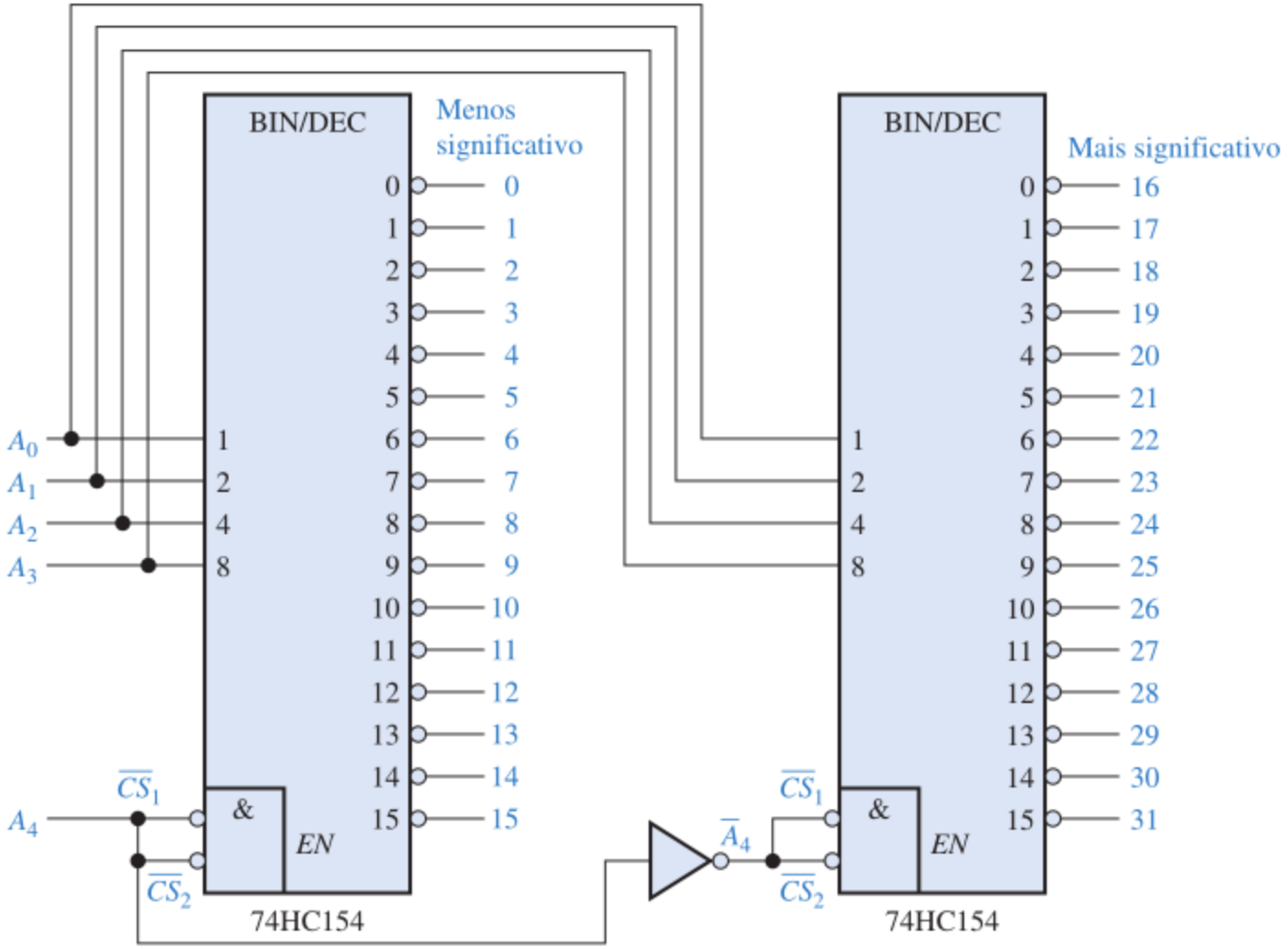


(a) Diagrama de pinos

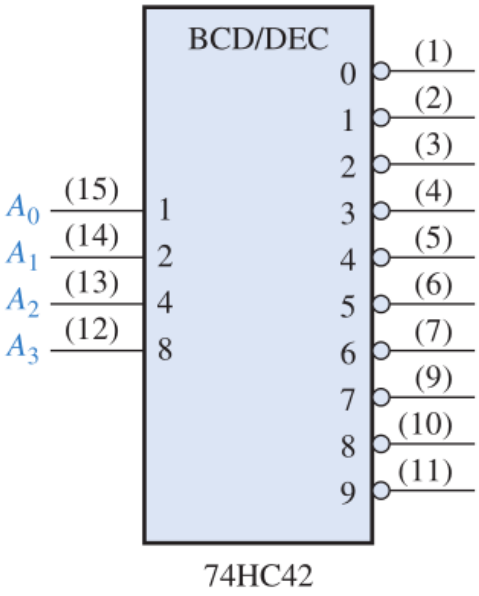


(b) Símbolo lógico

Decodificador 74HC154

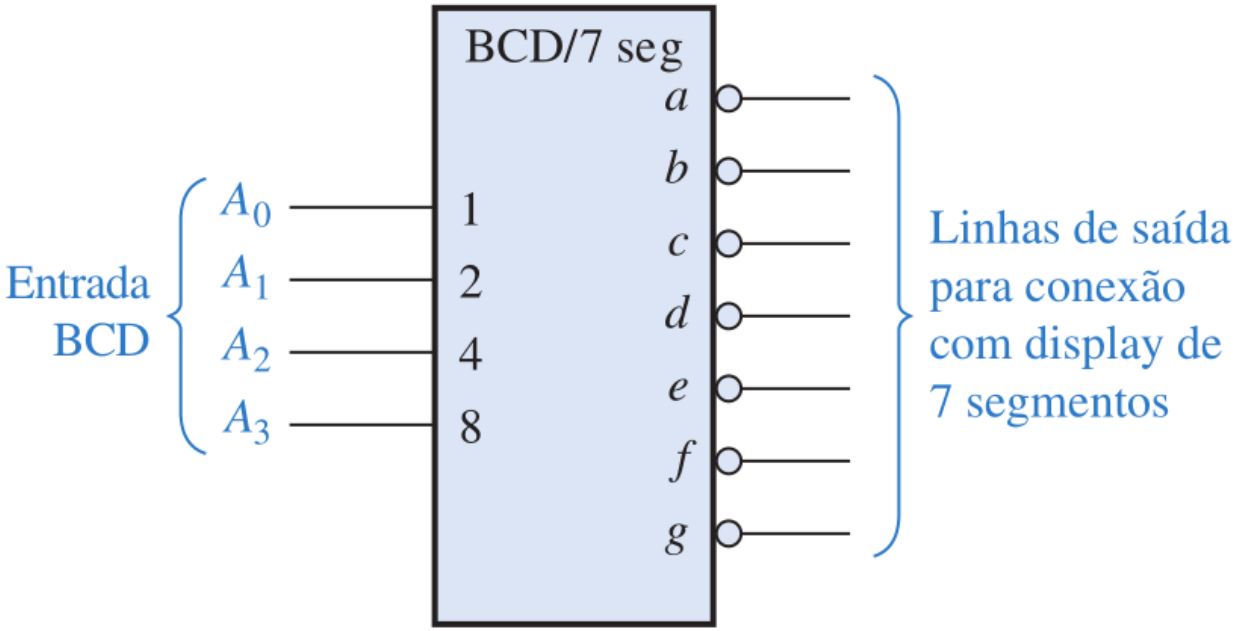


Decodificador BCD para Decimal

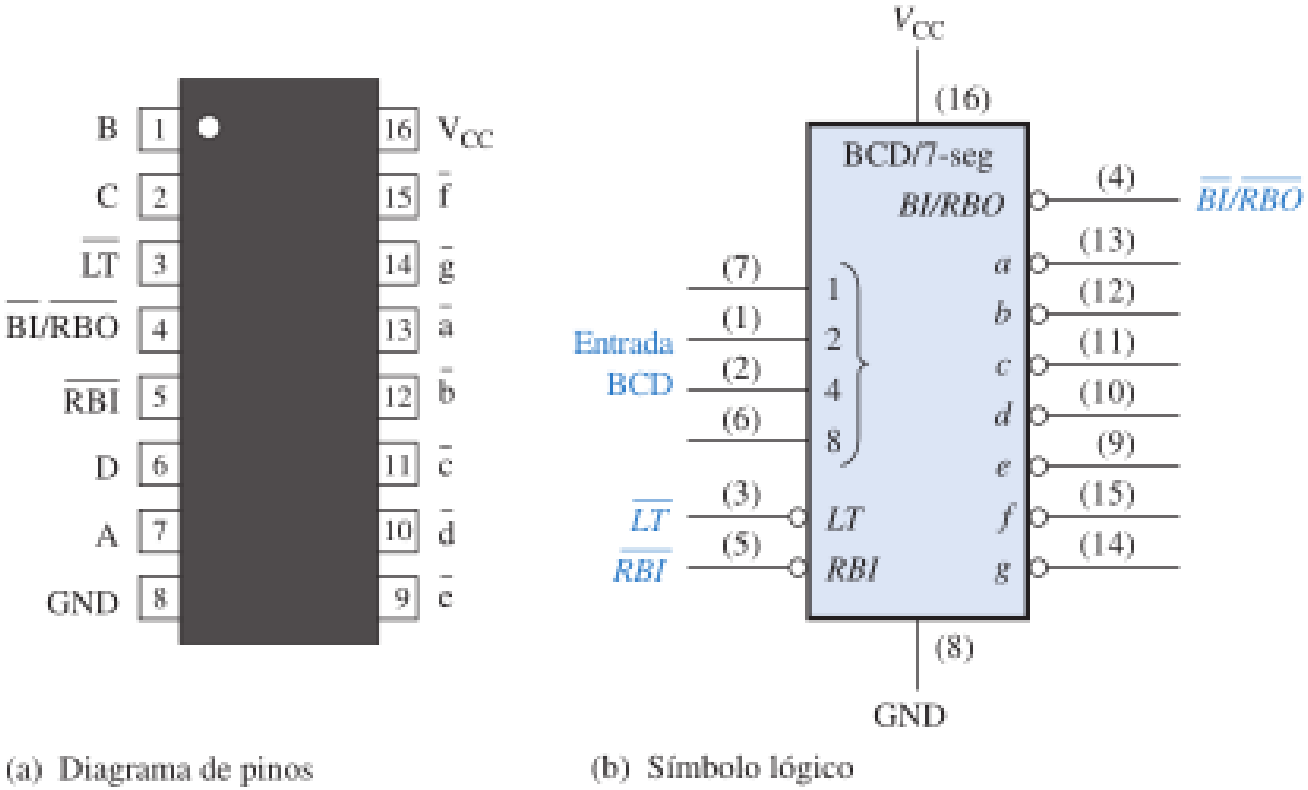


DÍGITO DECIMAL	CÓDIGO BCD A_3	A_2	A_1	A_0	FUNÇÃO DE DECODIFICAÇÃO
0	0	0	0	0	$\overline{A}_3\overline{A}_2\overline{A}_1\overline{A}_0$
1	0	0	0	1	$\overline{A}_3\overline{A}_2\overline{A}_1A_0$
2	0	0	1	0	$\overline{A}_3\overline{A}_2A_1\overline{A}_0$
3	0	0	1	1	$\overline{A}_3\overline{A}_2A_1A_0$
4	0	1	0	0	$\overline{A}_3A_2\overline{A}_1\overline{A}_0$
5	0	1	0	1	$\overline{A}_3A_2\overline{A}_1A_0$
6	0	1	1	0	$\overline{A}_3A_2A_1\overline{A}_0$
7	0	1	1	1	$\overline{A}_3A_2A_1A_0$
8	1	0	0	0	$A_3\overline{A}_2\overline{A}_1\overline{A}_0$
9	1	0	0	1	$A_3\overline{A}_2\overline{A}_1A_0$

Decodificador BCD para 7-segmentos



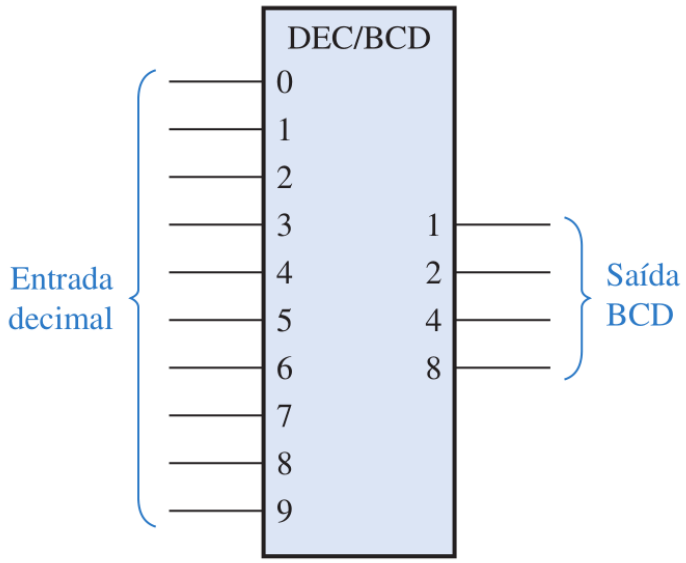
Decodificador 74HC47



(a) Diagrama de pinos

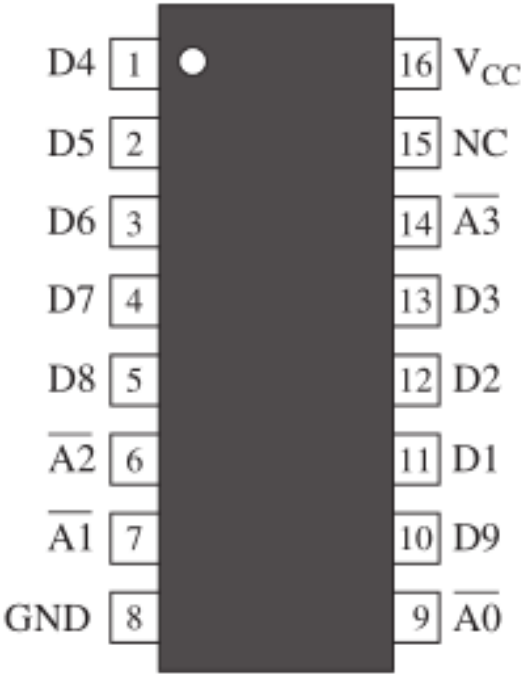
(b) Símbolo lógico

Codificador

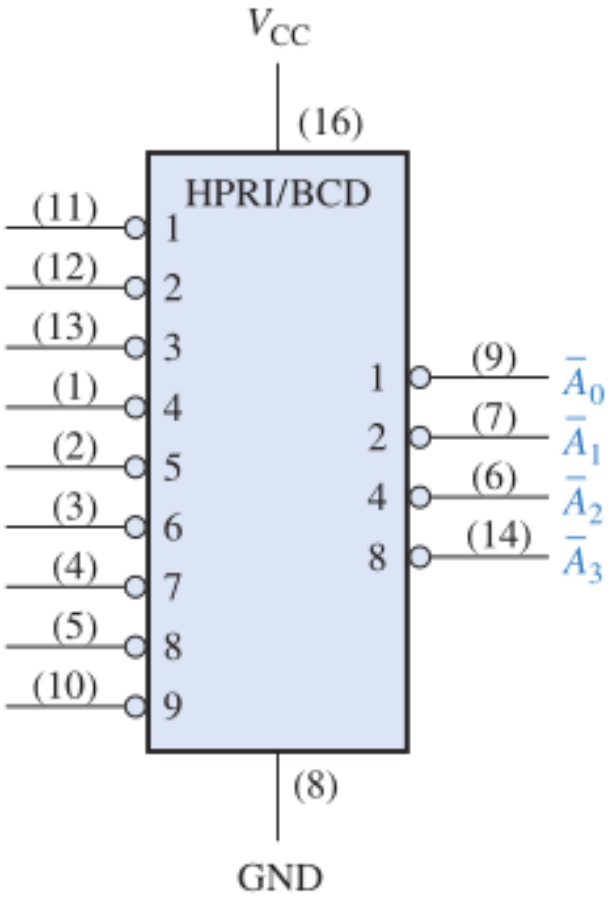


DÍGITO DECIMAL	CÓDIGO BCD A_3	A_2	A_1	A_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Codificador DEC-to-BCD 74HC147

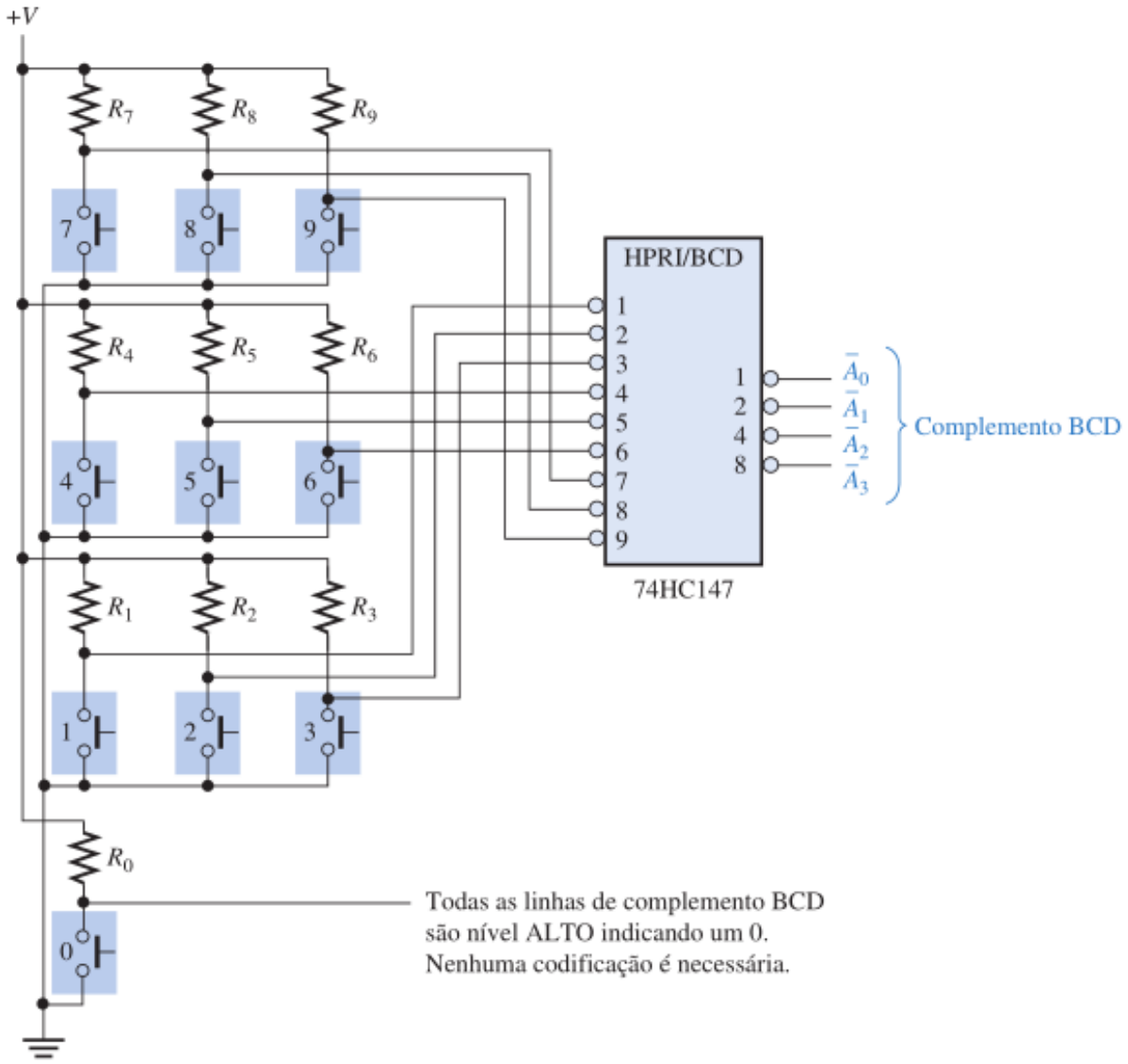


(a) Diagrama de pinos



(b) Símbolo lógico

Codificador DEC-to-BCD 74HC147



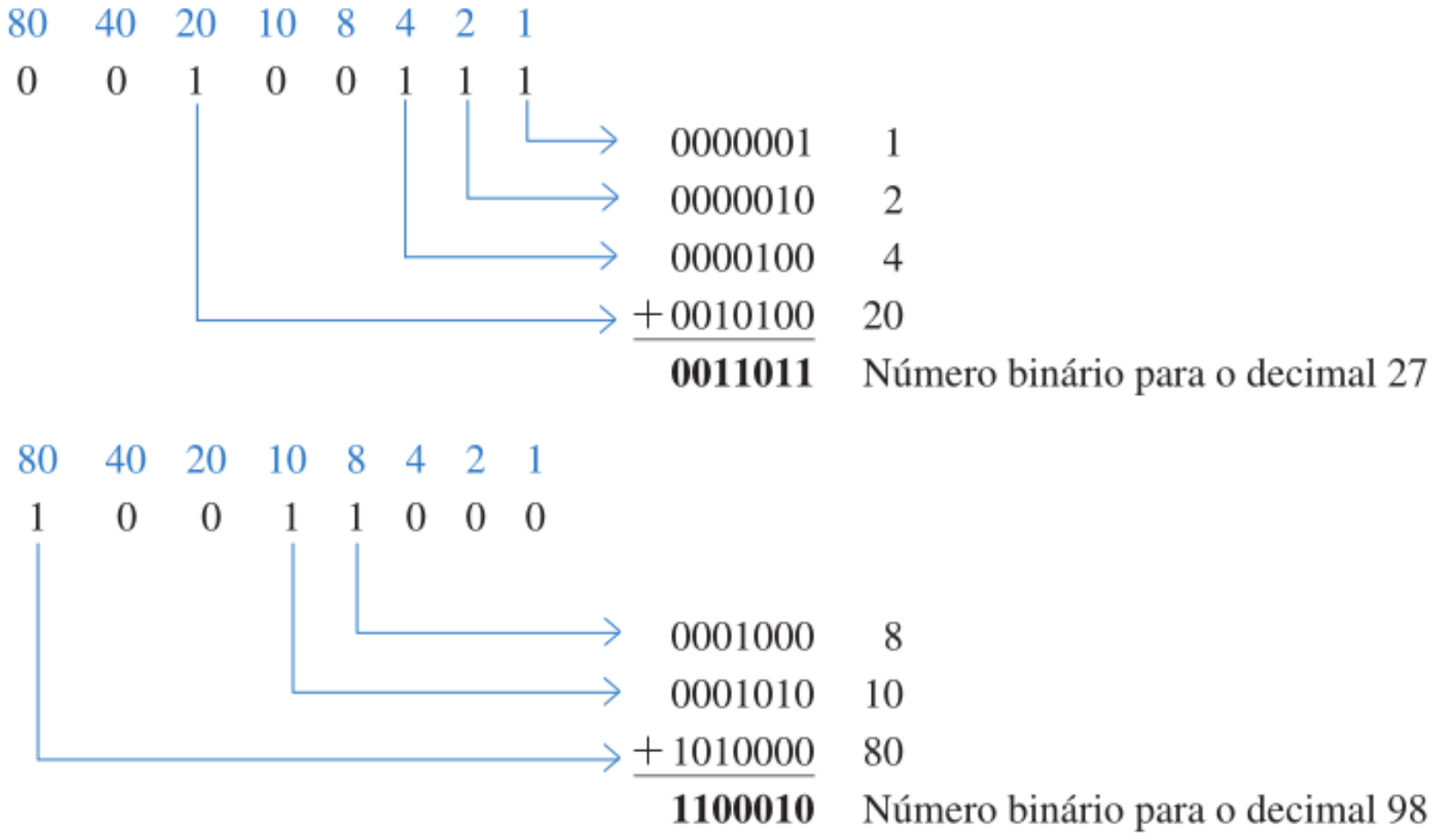
Conversor de código

$\underbrace{1000}_{8}$ $\underbrace{0111}_{7}$

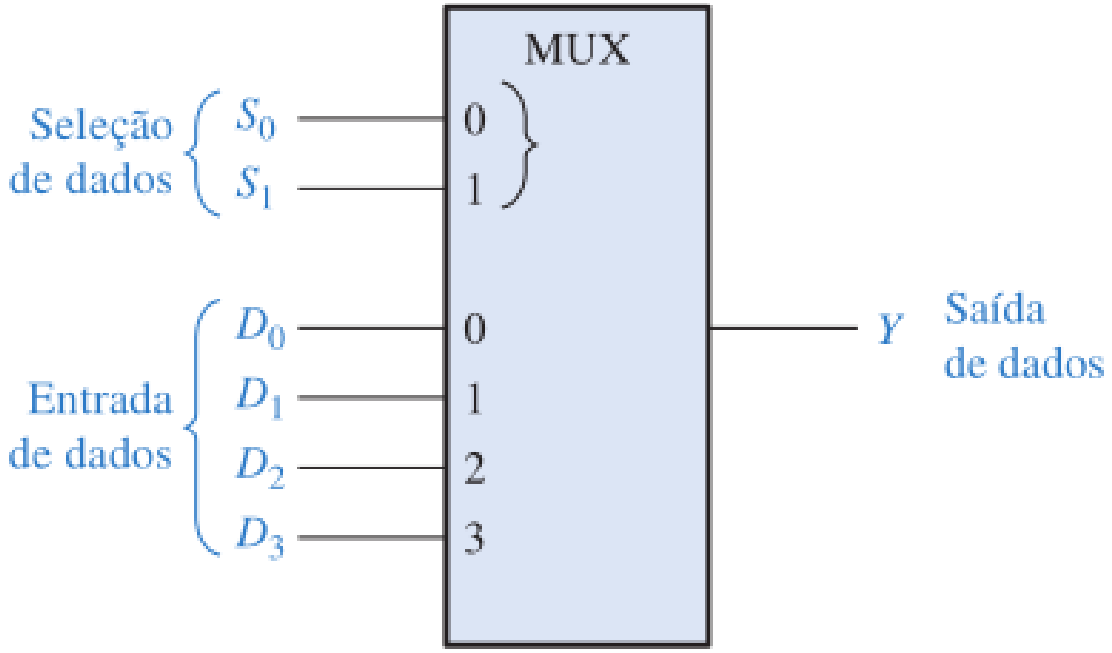
	Dezenas				Unidades			
Peso:	80	40	20	10	8	4	2	1
Indicação de bit:	B_3	B_2	B_1	B_0	A_3	A_2	A_1	A_0

BIT BCD	PESO EM BCD	(MSB) REPRESENTAÇÃO BINÁRIA 64	32	16	8	4	2	(LSB) 1
A_0	1	0	0	0	0	0	0	1
A_1	2	0	0	0	0	0	1	0
A_2	4	0	0	0	0	1	0	0
A_3	8	0	0	0	1	0	0	0
B_0	10	0	0	0	1	0	1	0
B_1	20	0	0	1	0	1	0	0
B_2	40	0	1	0	1	0	0	0
B_3	80	1	0	1	0	0	0	0

Conversor de código

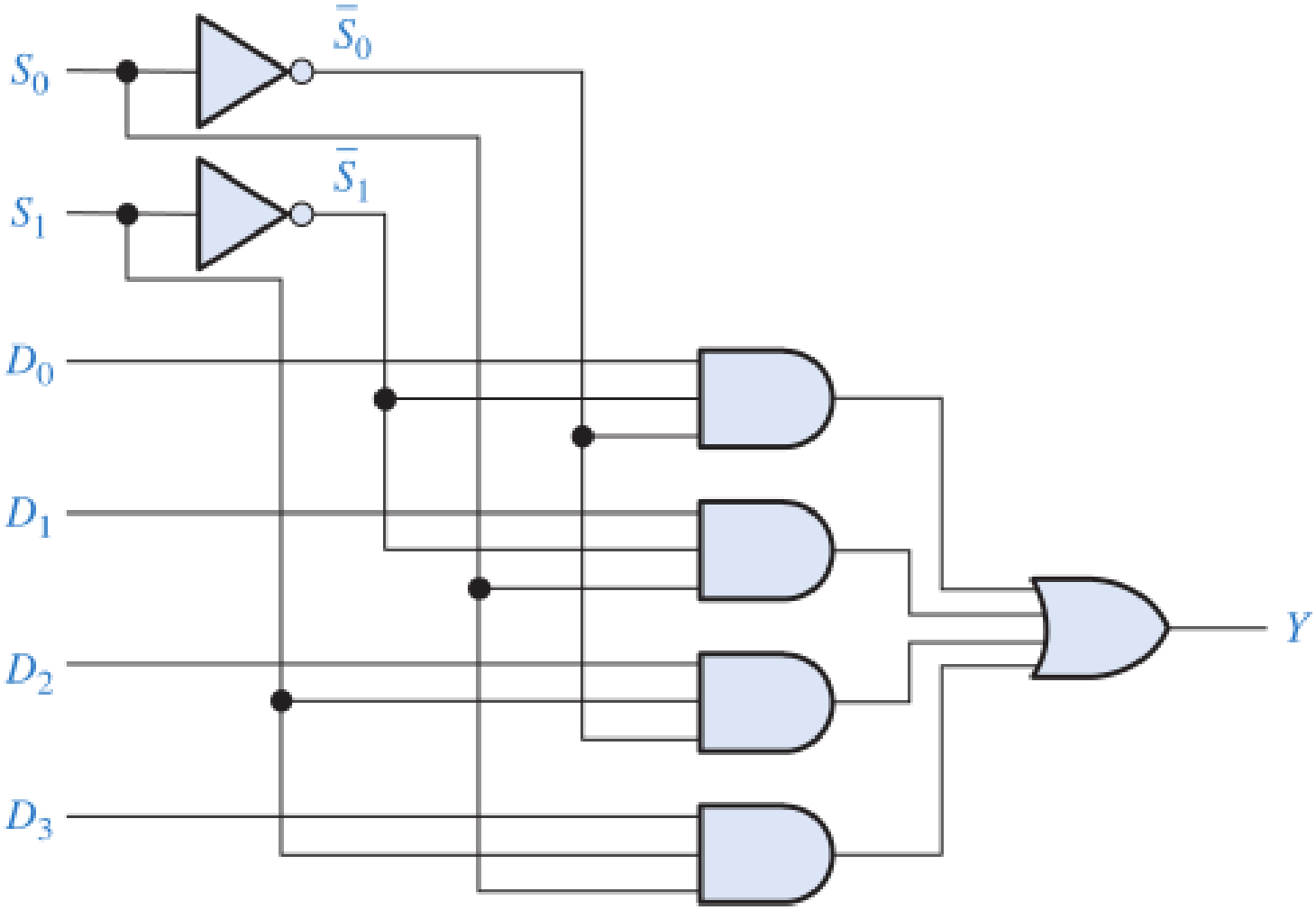


Multiplexador (seletor de dados)

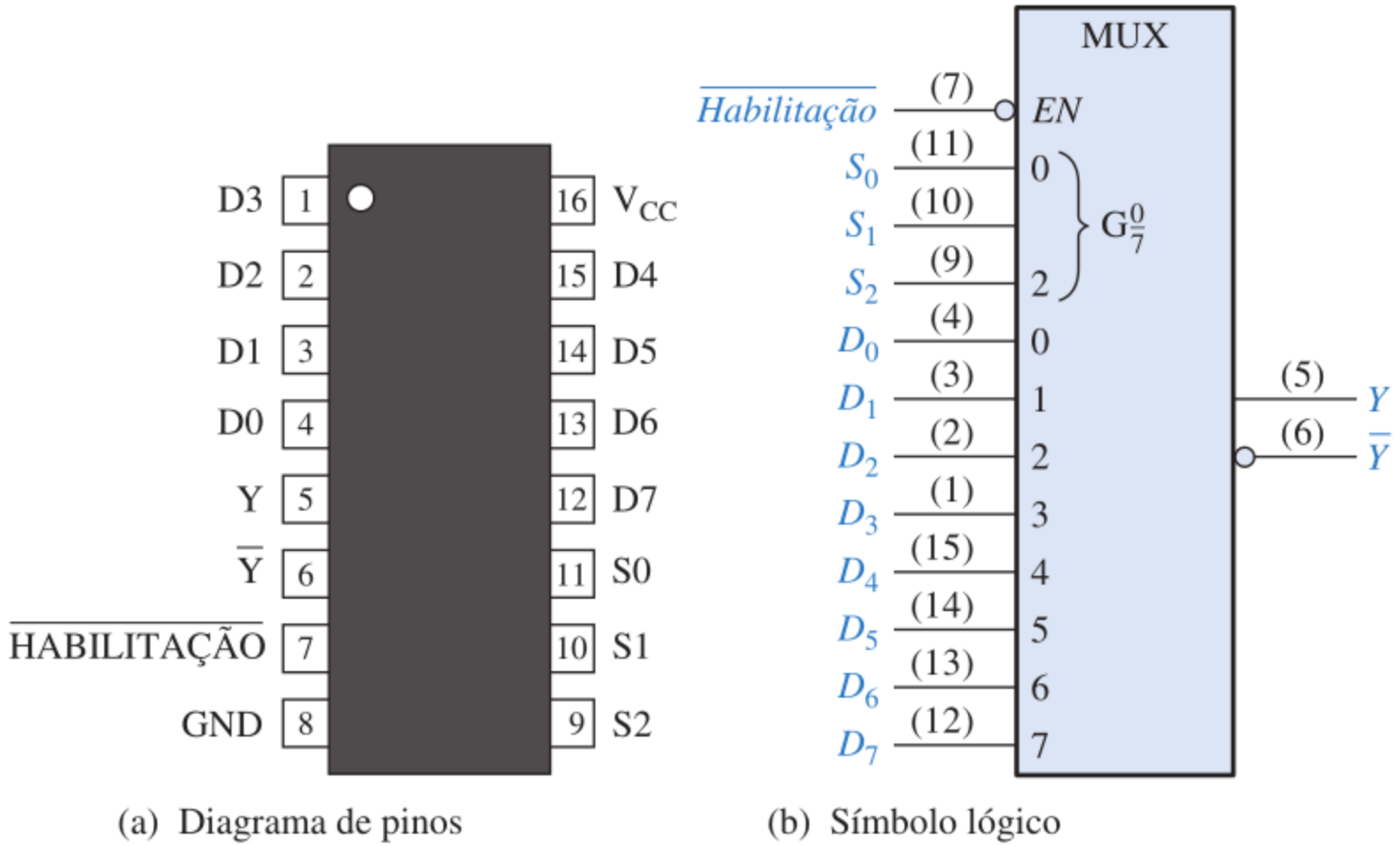


ENTRADAS DE SELEÇÃO DE DADOS S_1	S_0	ENTRADA SELECIONADA
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

Multiplexador (seletor de dados)



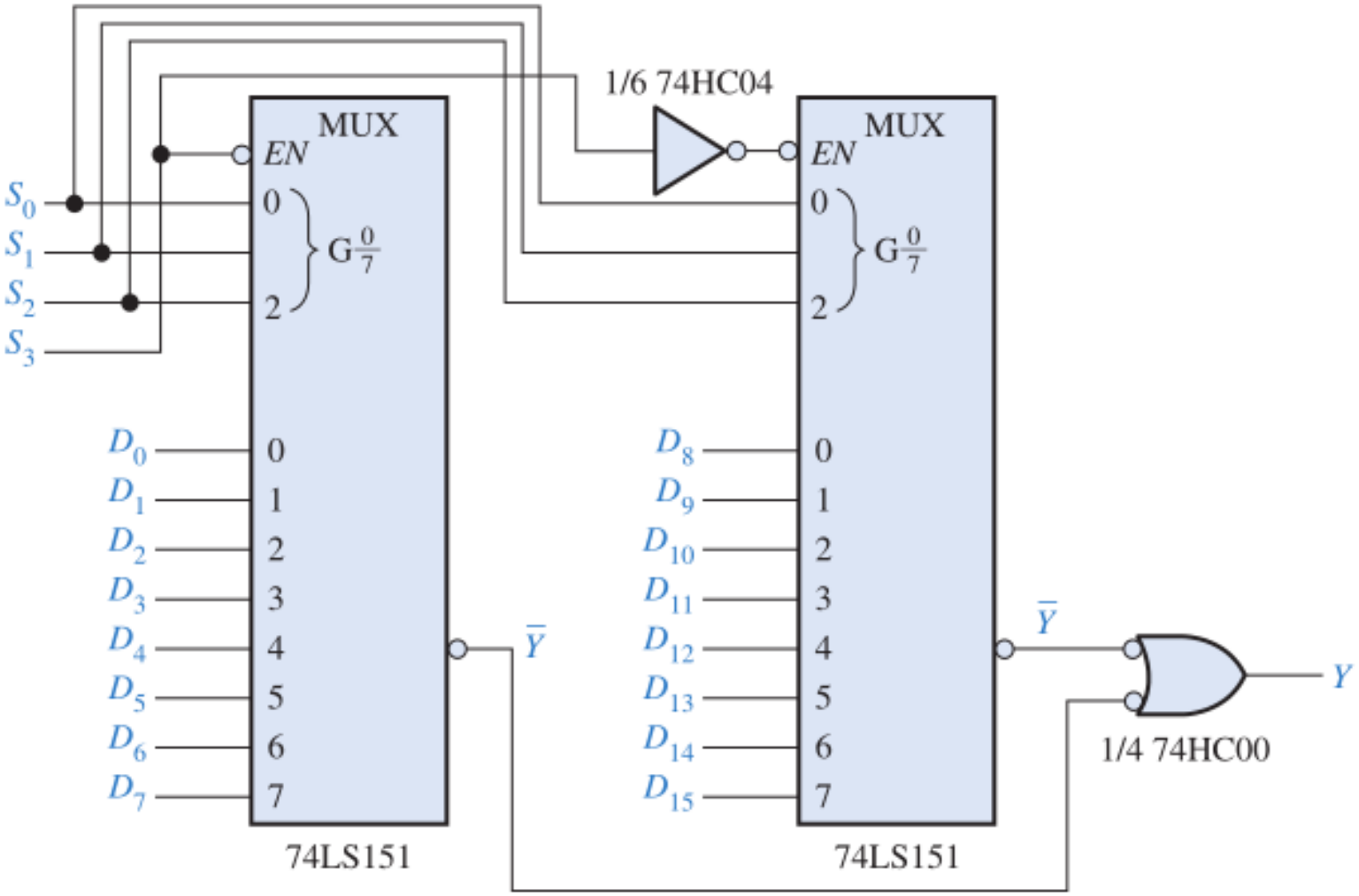
Multiplexador 74LS151



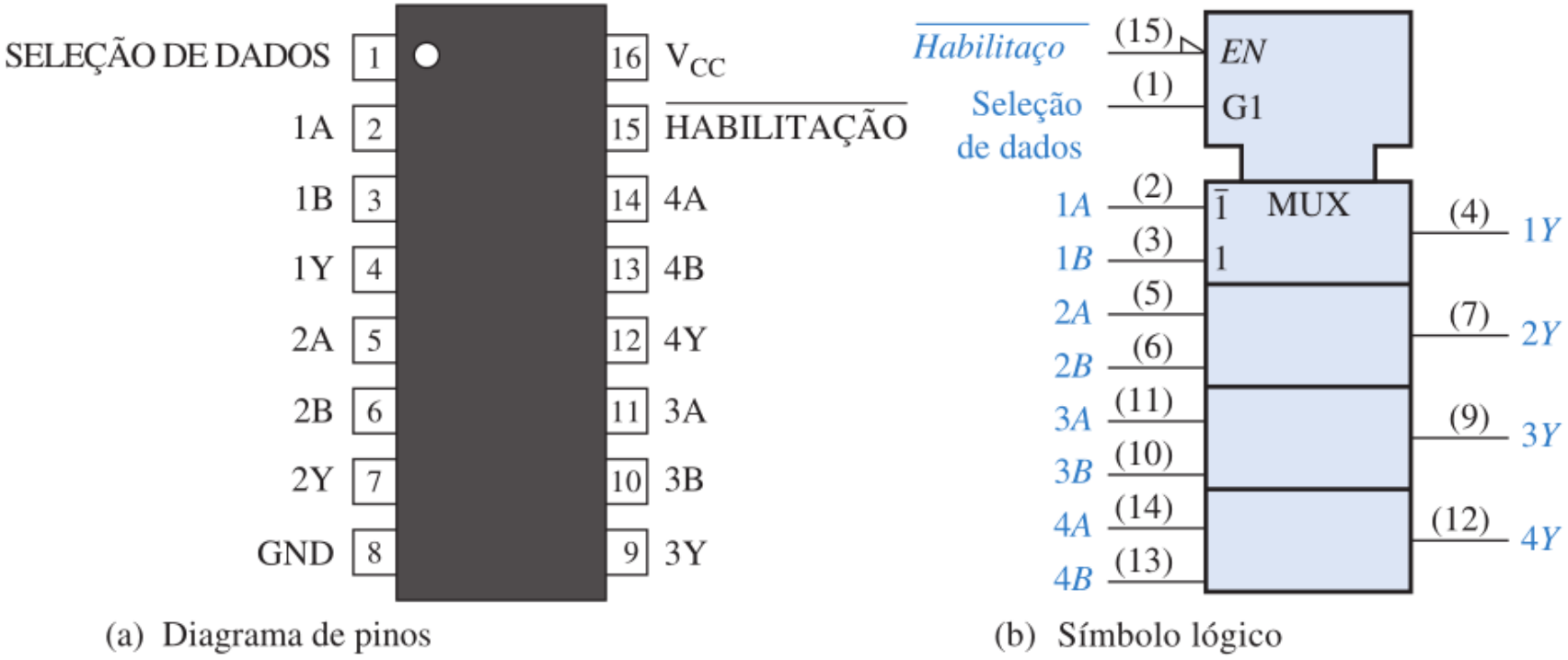
(a) Diagrama de pinos

(b) Símbolo lógico

Multiplexador 74LS151

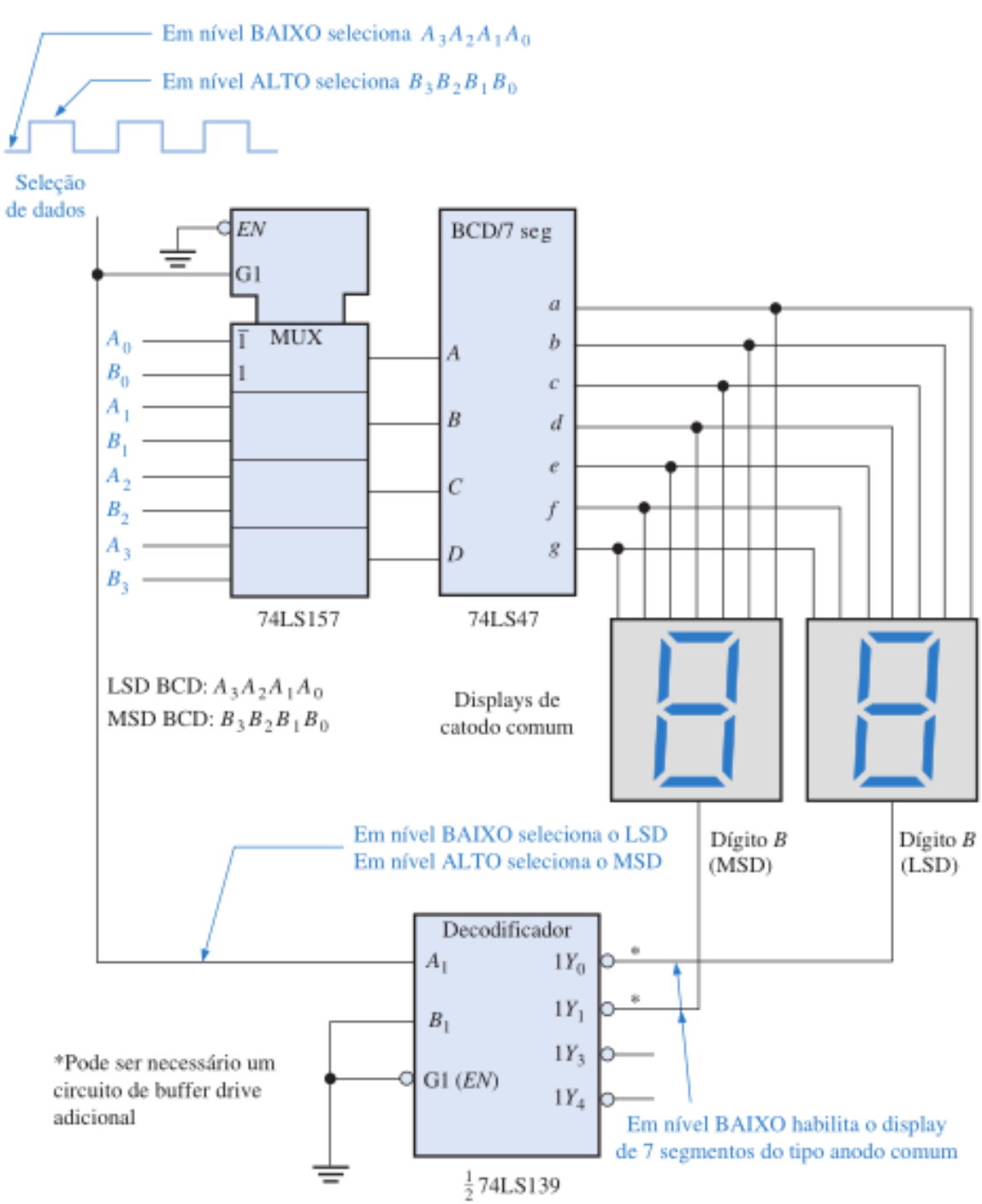


Multiplexador 74LS157

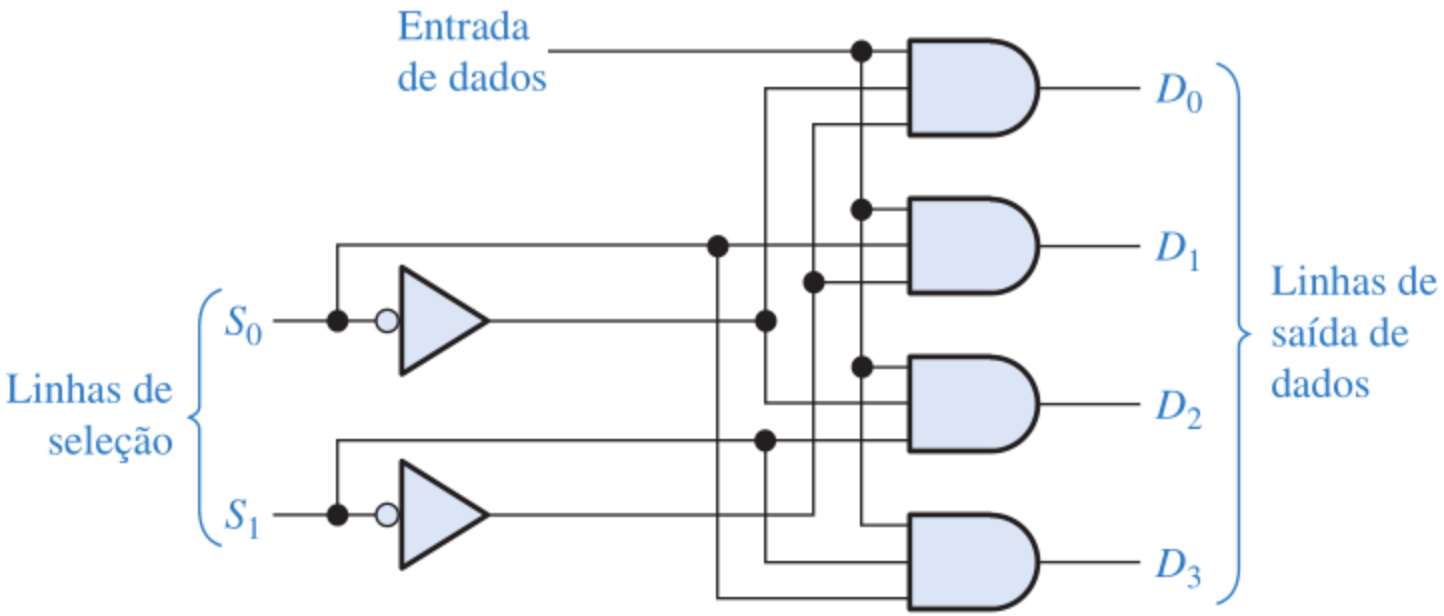


(a) Diagrama de pinos

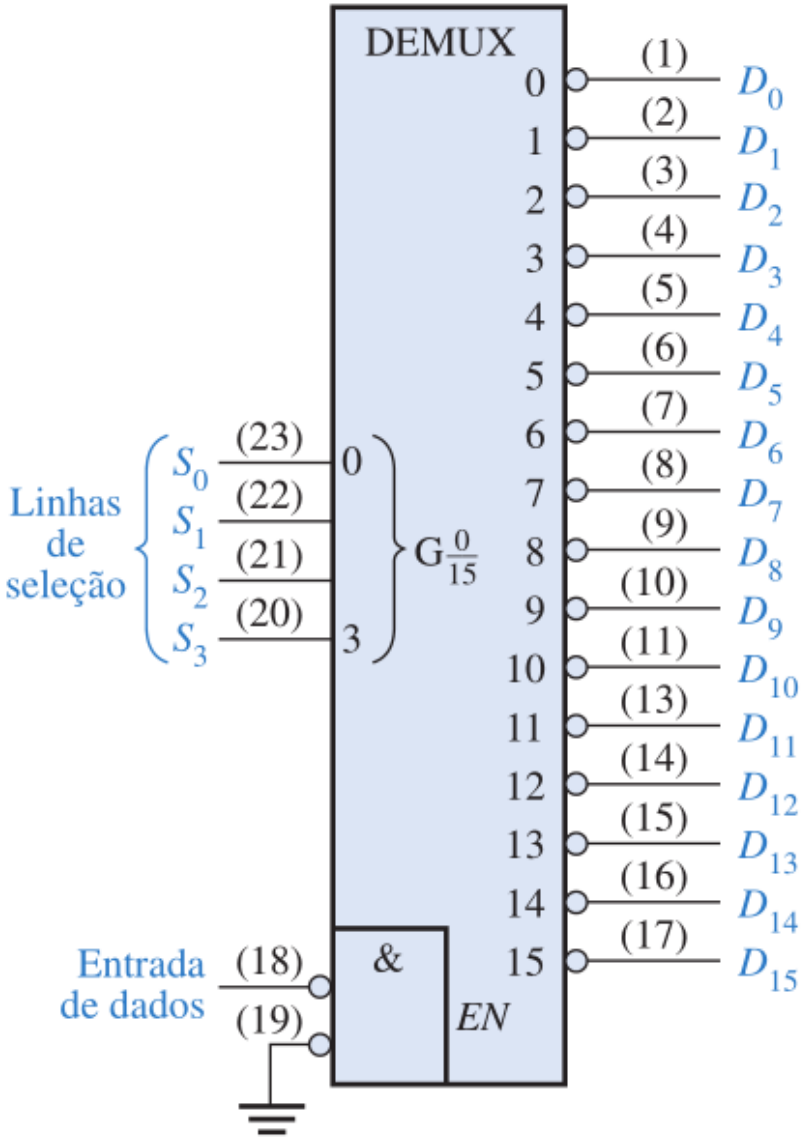
(b) Símbolo lógico


Em nível BAIXO seleciona $A_3A_2A_1A_0$
Em nível ALTO seleciona $B_3B_2B_1B_0$
Seleção de dados
EN
G1
$\overline{1}$ MUX
1
A_0
B_0
A_1
B_1
A_2
B_2
A_3
B_3
74LS157
BCD/7 seg
A
B
C
D
a
b
c
d
e
f
g
74LS47
LSD BCD: $A_3A_2A_1A_0$
MSD BCD: $B_3B_2B_1B_0$
Displays de catodo comum
Em nível BAIXO seleciona o LSD
Em nível ALTO seleciona o MSD
Dígito B (MSD)
Dígito B (LSD)
Decodificador
A_1
B_1
G1 (EN)
$1Y_0$
$1Y_1$
$1Y_3$
$1Y_4$
*Pode ser necessário um circuito de buffer drive adicional
Em nível BAIXO habilita o display de 7 segmentos do tipo anodo comum
$\frac{1}{2}$ 74LS139

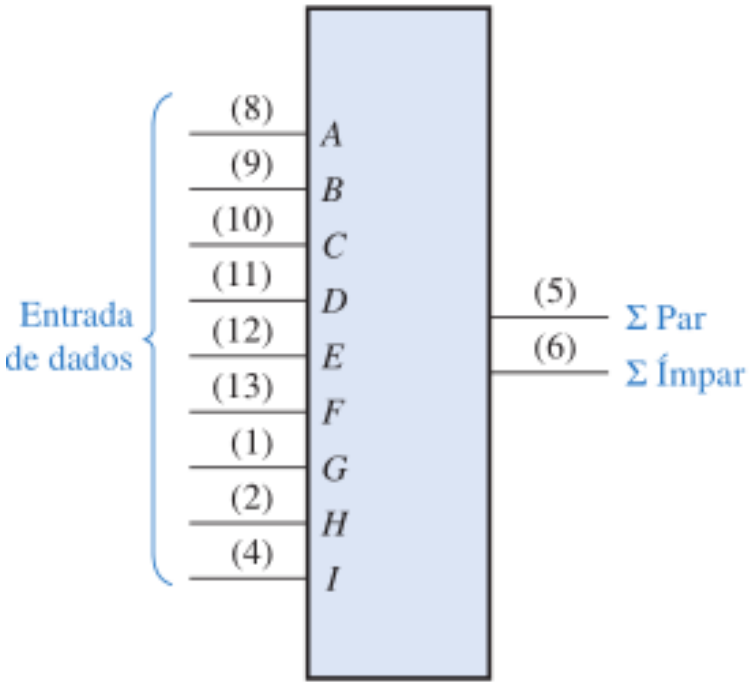
De-multiplexador



De-multiplexador 74HC154



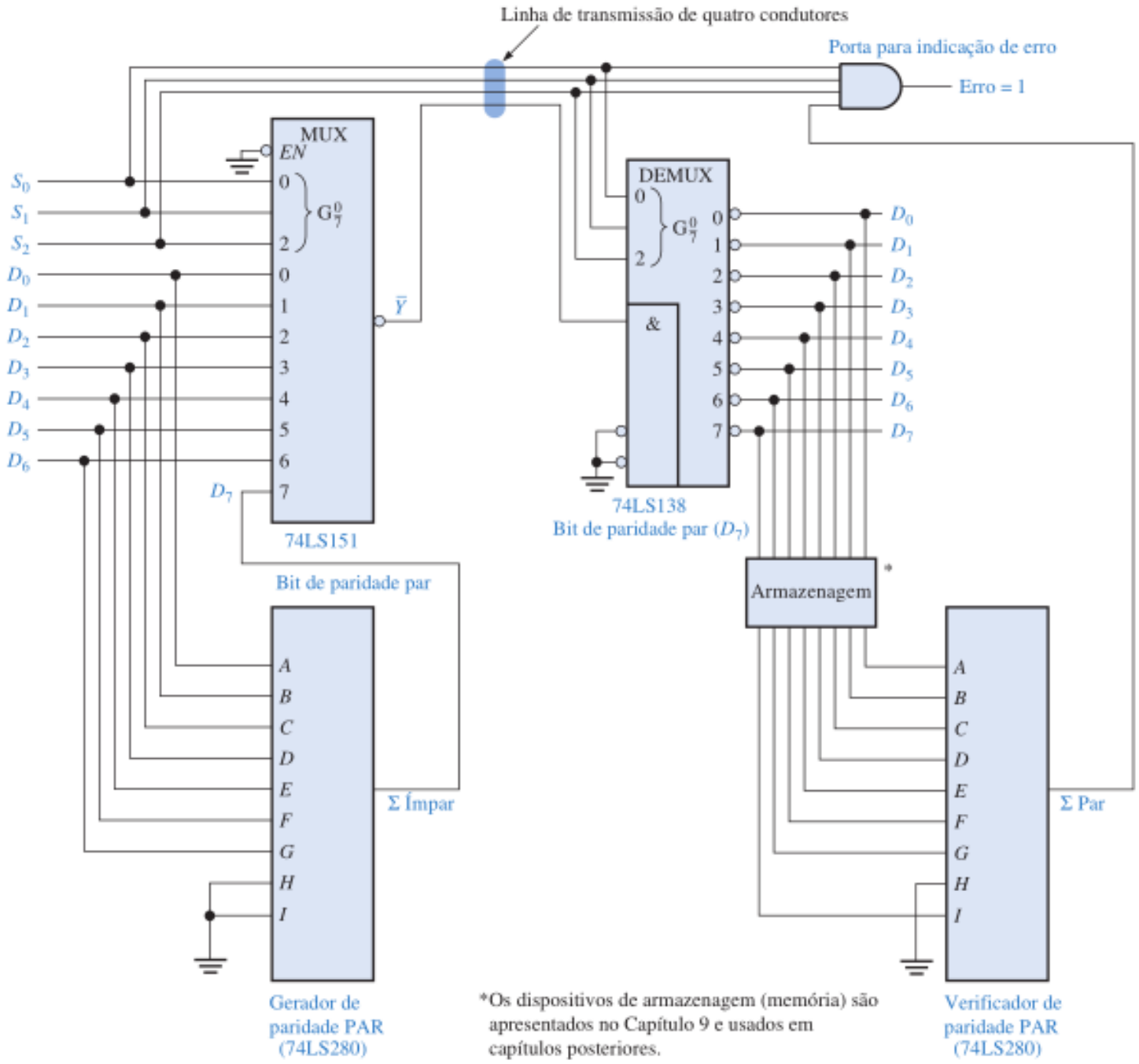
Gerador de paridade 74LS280



(a) Símbolo lógico tradicional

Número de entradas de A a I que são nível ALTO	Saídas	
	Σ Par	Σ Ímpar
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

(b) Tabela de funções


Linha de transmissão de quatro condutores
Porta para indicação de erro
Erro = 1
MUX
EN
S_0
S_1
S_2
D_0
D_1
D_2
D_3
D_4
D_5
D_6
D_7
$\overline{Y}$
74LS151
Bit de paridade par
DEMUX
&
74LS138
Bit de paridade par (D_7)
Armazenagem
*
A
B
C
D
E
F
G
H
I
Σ Ímpar
Σ Par
Gerador de paridade PAR (74LS280)
Verificador de paridade PAR (74LS280)
*Os dispositivos de armazenagem (memória) são apresentados no Capítulo 9 e usados em capítulos posteriores.

Desafio

- Projete e implemente em Logisim, o circuito completo de uma balança de serviço de autoatendimento
- Assuma como entrada a saída de um ADC com o valor do peso mensurado por um sensor
- Inclua botões e displays de 7 segmentos
- Siga os exemplos dos videoclipes disponibilizados
- Se for o caso, pode usar as funções de multiplicação e divisão disponíveis em Logisim