Errata Sheet
MM32F3270
Rev 1.1

Contents

1 About this document

This errata sheet describes all known functional issues of MM32F3270 series products, and aims to provide users with errata information and corresponding solutions for the product.

Table 1 Applicable series and part numbers

Series	Part numbers
MM32F3270	For latest part numbers, please refer to MM32F3270 series product data sheet

2 Overview

Table 2 Errata sheet summary

Module	Description	Revision	Detail
TIM	TIM count abnormally using single edge trigger mode in encoder capture mode	A	3.1.1
DMA	Incorrect data reading may occur when multiple DMA channels are accessed at the same time	A	3.2.1
LSE	LSE ready bit doesn't work properly	A	3.3.1
ADC	ADC window comparison function doesn't work properly in multi-channel conversion mode	A	3.4.1
ADC	ADC trigger doesn't work properly when selecting trigger source CC4 || CC5	A	3.4.2
Power	Wake up function doesn't work properly in standby mode	A	3.5.1
BKP	BKP TIF/TEF read abnormal after power on	A	3.6.1
CAN	CAN responds to bus requests in listen-only mode	A	3.7.1

In above table, the letter in the column 'Revision' indicates the chip revision where this phenomenon will occur. The chip revision information can be found in the chip marking. For details, please refer to the "Marking" section in MM32F3270 series product data sheet.

3 Issues and solutions

3.1 TIM

3.1.1 TIM count abnormally using single edge trigger mode in encoder capture mode

Issue:

When TIM works in encoder mode, user can configure the SMS bit of TIMx_SMCR register to select among TI1 edge count, TI2 edge count or TI1 edge and TI2 edge count. Regardless of the counting mode, the counting pulse and direction signal will be generated according to the transition sequence of the two input signals, the counter counts up or down, and set the DIR bit of the TIMx_CR1 register accordingly.

When SMS = 011, the counter counts on both TI1 and TI2 edge, the DIR bit can be set or cleared according to the transition sequence of the two input signals, and the counter will also count up or down accordingly.

When SMS = 001 or 010, the counter counts on the edge of TI1 or TI2, the DIR bit can be set or cleared according to the transition sequence of the two input signals, but the counter will only count up and not count down.

Solution:

It is recommended to set SMS = 011 and use both TI1 and TI2 edge counting mode.

3.2 DMA

3.2.1 Incorrect data reading may occur when multiple DMA channels are accessed at the same time

Issue:

When multiple peripherals send access requests to multiple DMA channels at the same time, and the data width of one or more of the requests is configured to 8-bit or 16-bit, then transferred data of the high priority channel may be incorrect.

Solution:

Any of the following methods can be used to avoid this issue:

1. Configure all DMA channels to 32-bit data width.

2. The software guarantees that only one peripheral sends DMA request at the same time.

3. If the chip has multiple DMA modules, this issue won’t happen when multiple DMA modules are used at the same time.

3.3 LSE

3.3.1 LSE ready bit doesn’t work properly

Issue:

The LSE ready bit LSERDY may be set when the external crystal oscillator has not reached a stable state.

Solution:

Normally, the external crystal oscillator will reach a stable state 3 seconds after LSE is enabled (experience value obtained from simulation and characterization). In the application, it’s recommended to use counter to count for 3 seconds after enabling the LSE, then it can be considered that the external crystal oscillator has reached a stable state.

3.4 ADC

3.4.1 ADC window comparison function doesn’t work properly in multi-channel conversion mode

Issue:

In window comparison mode of the ADC, user can set the CMPCH bit to select the monitoring channel. When the channel value of the monitoring channel selected by the CMPCH bit is within the pre-set window comparison range (CMPHDATA, CPLDATA), the ADWIF bit of the status register ADSTA is set to 1.

When the ADC only has one channel for conversion, the ADWIF will be set or clear according to the comparison result of the monitoring channel value and the pre-set window comparison range. But when the ADC has multiple channels for conversion, it’s found that the ADWIF bit won’t be set or clear according to the comparison result of the monitoring channel and the pre-set window comparison range, but will be set or clear accordingly to the comparison result of the previous channel value of the monitoring channel and the pre-set window comparison range.

Solution:

When only one ADC channels is enabled, configure the CMPCH bit to select actual monitoring channel; When multiple ADC channels are enabled, configure the CMPCH bit to select the previous channel of the actual monitoring channel.

For example: if ADC channel 1, 3, 4, 5 are enabled, channel 4 is enabled as window comparison function, the reference pseudo code is as follows:

```
//Initialize ADC
ADCInit();
```

```
//Enable channel 1, 3, 4, 5 conversion function
ADCChannelConfig(Channel_1|Channel_3|Channel_4|Channel_5);
//Set the ADC window comparison upper and lower threshold
ADCAnalogWatchdogThresholdsConfig(Thresholds_High, Thresholds_Low);
//Enable channel 3 for window comparison function (actual channel to monitor is channel 4)
ADCAnalogWatchdogChannelConfig(Channel_3);
//Enable ADC function comparison function
ADCAnalogWatchdogCmd(ENABLE);
```

3.4.2 ADC trigger doesn’t work properly when selecting trigger source CC4 || CC5

Issue:

When the ADC external trigger source selects “TIM1_CC4 || TIM1_CC5” (TRGSEL = 00101) or “TIM8_CC4 || TIM8_CC5” (TRGSEL = 01010), it may happen that the ADC cannot capture all the trigger signals of CC4 and CC5; For the triggered ADC sampling, the software cannot determine whether the trigger is caused by CC4 or CC5.

Solution:

Select any one of the trigger sources (CC4 or CC5) and use DMA to simulate two trigger signals. Take TIM1 for example, select CC4 as trigger source (TRGSEL = 10000), assume the original compare value for CC4 and CC5 are 400 and 800 respectively, set the TIM1_CCR4 to 400 first, once the counter counts to 400, then trigger the DMA to update the TIM_CCR4 to 800; Once the counter counts to 800, then trigger the DMA to update the TIM1_CCR4 to 400 again. Using this method to update the TIM1_CCR4 value repeatedly.

3.5 Power

3.5.1 Wake up function doesn’t work properly in standby mode

Issue:

Under 3.3V supply voltage, when the chip enters the standby mode, if it’s configured to wake up on the rising edge, the chip may not be able to wake up.

Solution:

Under 3.3V supply voltage, when the chip enters the standby mode, use falling edge to wake up the chip; Under 5V supply voltage, both rising and falling edge can wake up the chip.

3.6 BKP

3.6.1 BKP TIF/TEF read abnormal after power on

Issue:

After the VBAT domain is powered on for the first time, the tamper flag TIF/TEF is in an undetermined state.

Solution:

After the VBAT domain is powered on, write the CTI/CTE bit to clear TIF/TEF flag first.

3.7 CAN

3.7.1 CAN responds to bus requests in listen-only mode

Issue:

When configured as listen-only mode, the CAN module will still respond to the bus request and send out an ACK or NAK response.

Solution:

It is recommended to use other mode.

4 Revision history

Table 3 Revision hisotory

Date	Revision	Description
2021/10/09	1.1	Add BKP, ADC, DMA and CAN related description
2021/07/12	1.0	New errata sheet