Date:

EXPERIMENT NO. 4

AIM: Implement arithmetic and logic unit circuits in Logisim.

OBJECTIVES:

i. Implement 1-bit, 2-bit, 4-bit and 8-bit arithmetic unit circuits

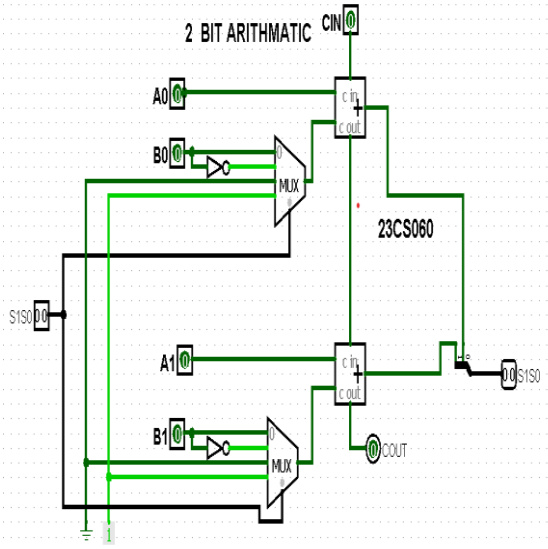
ii. Implement 1-bit, 2-bit, 4-bit and 8-bit logical unit circuits for four logical functions

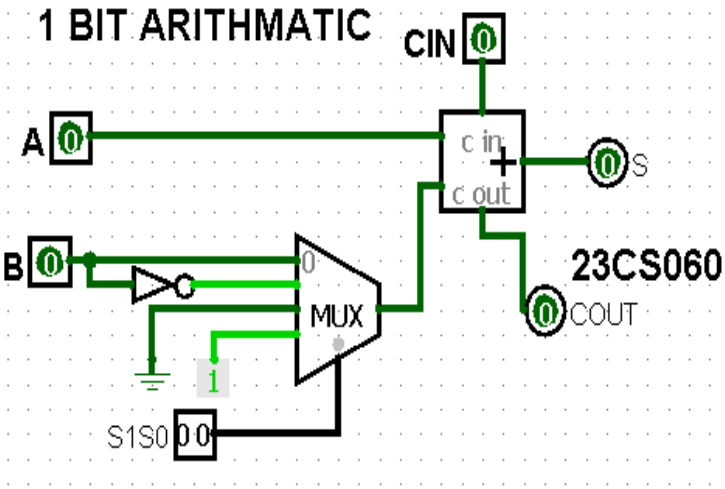
iii. Implement 1-bit and 2-bit logical unit circuits for sixteen logical functions

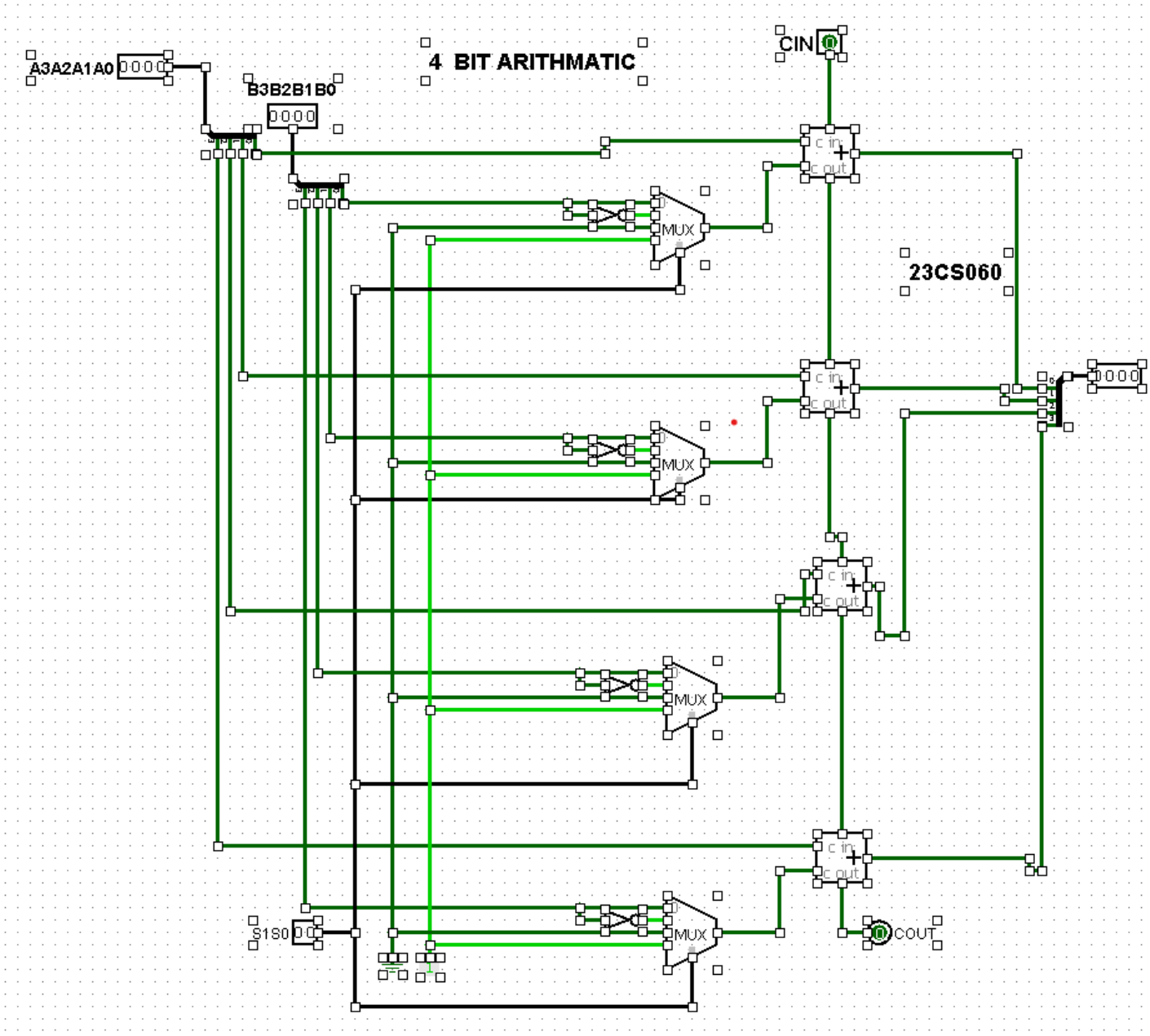
iv. Implement 2-bit, 4-bit and 8-bit bidirectional shifter

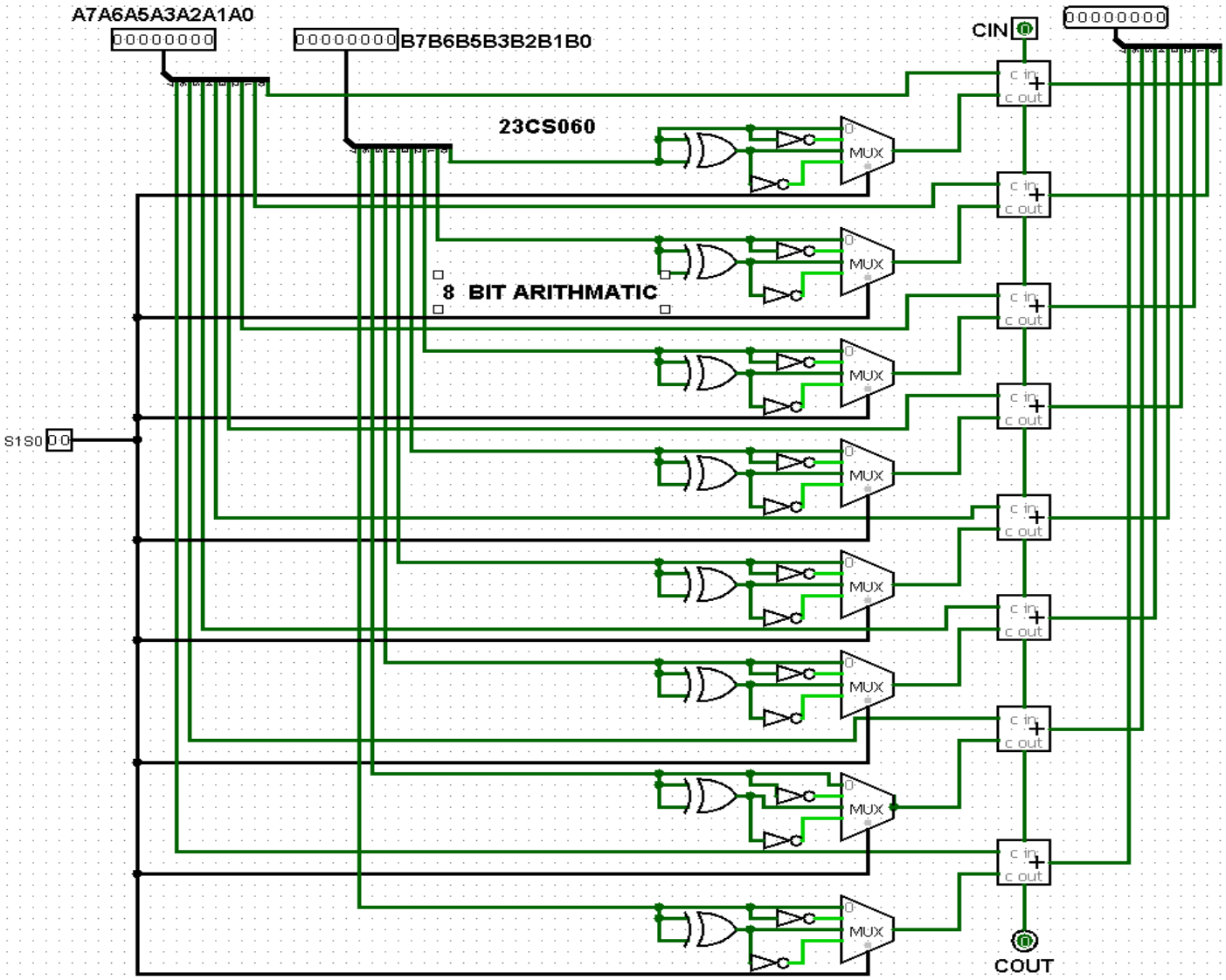
v. Implement 1-bit, 2-bit, 4-bit and 8-bit ALU

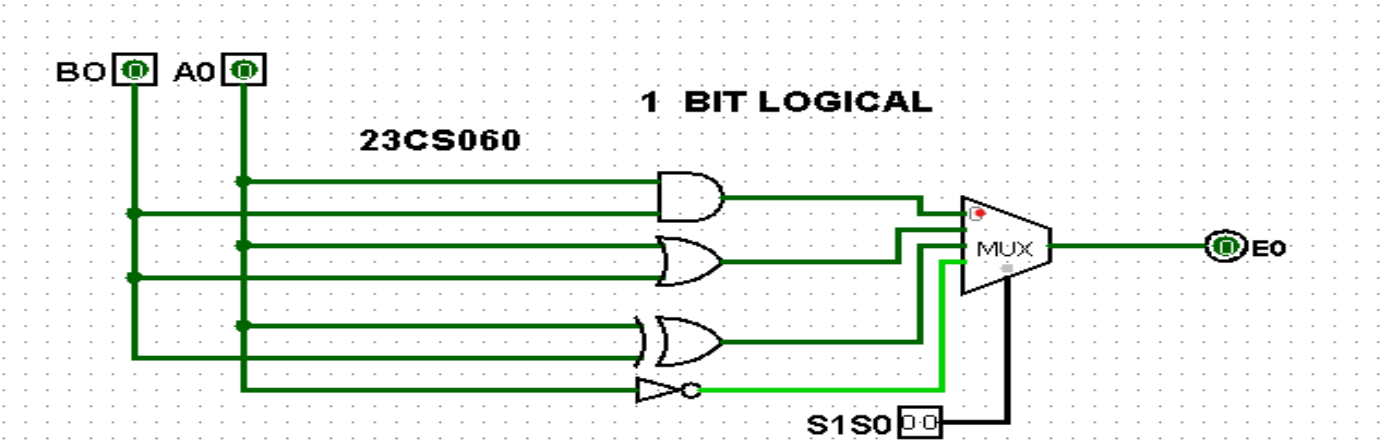
CIRCUITS:

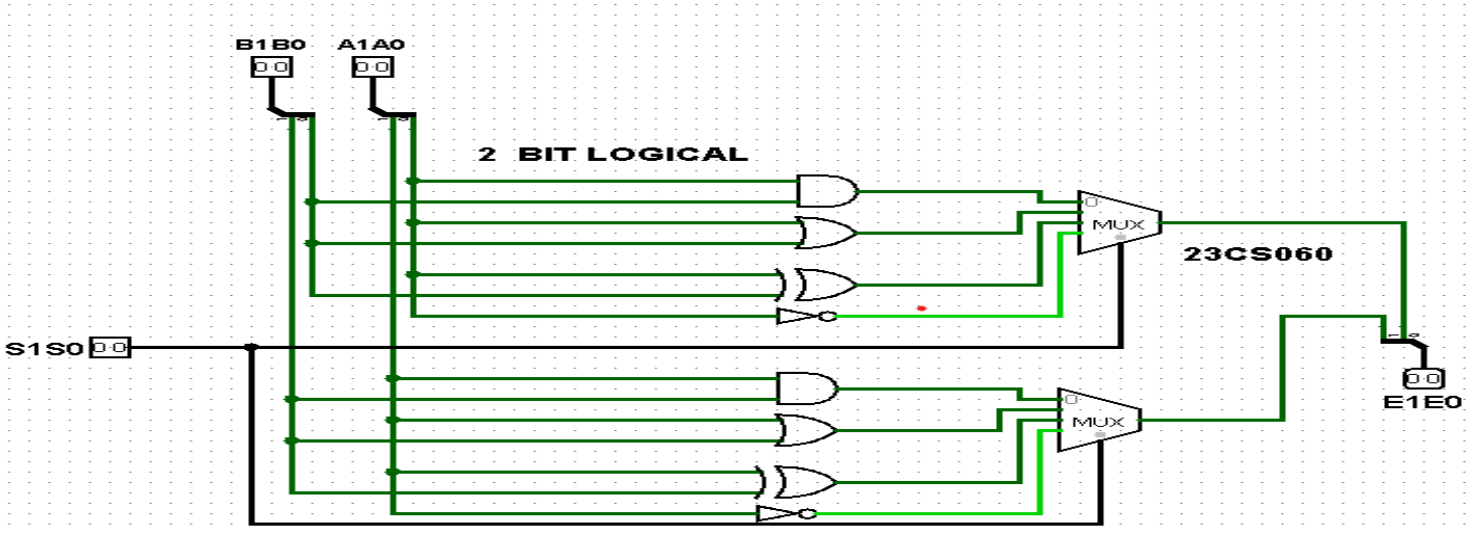


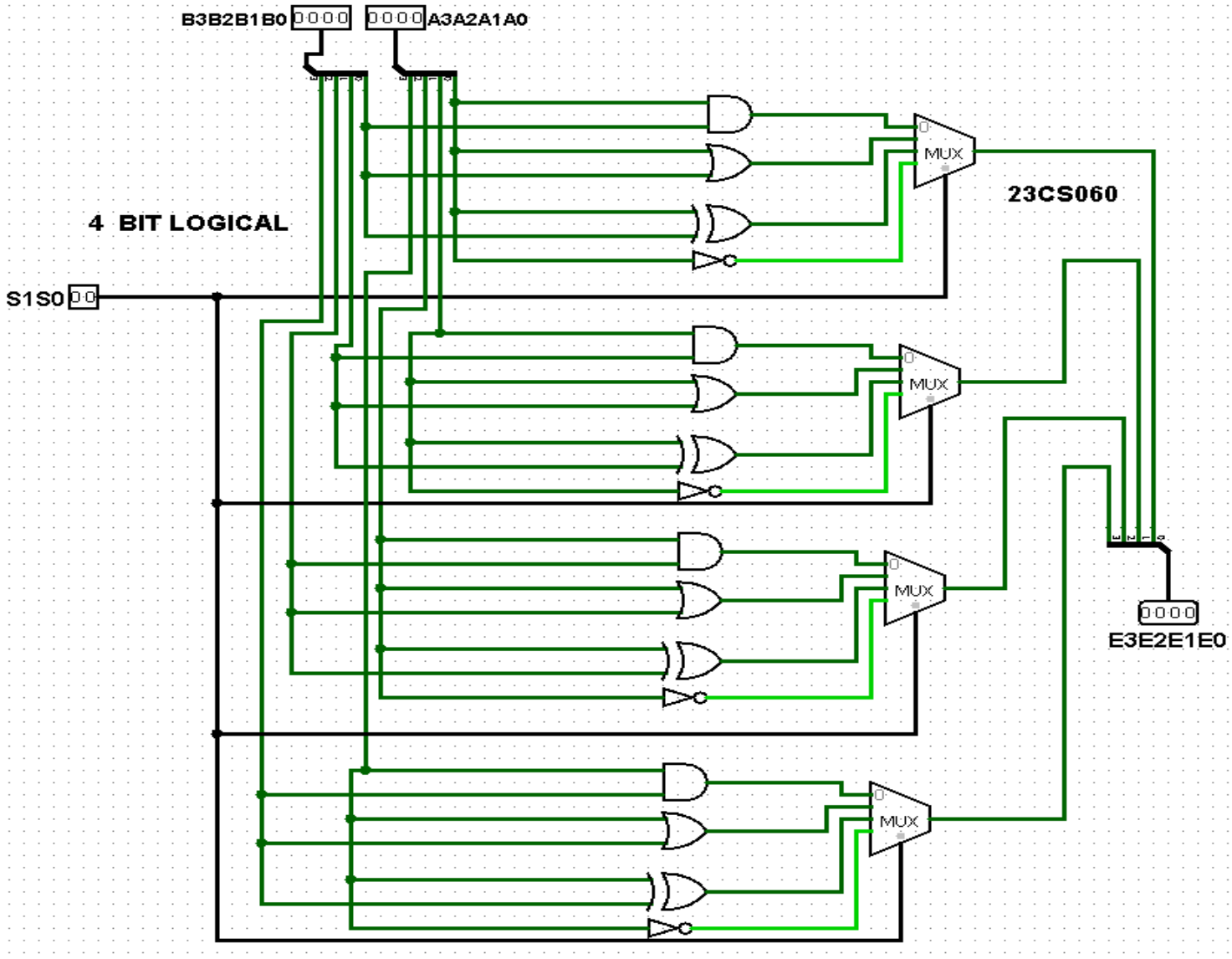


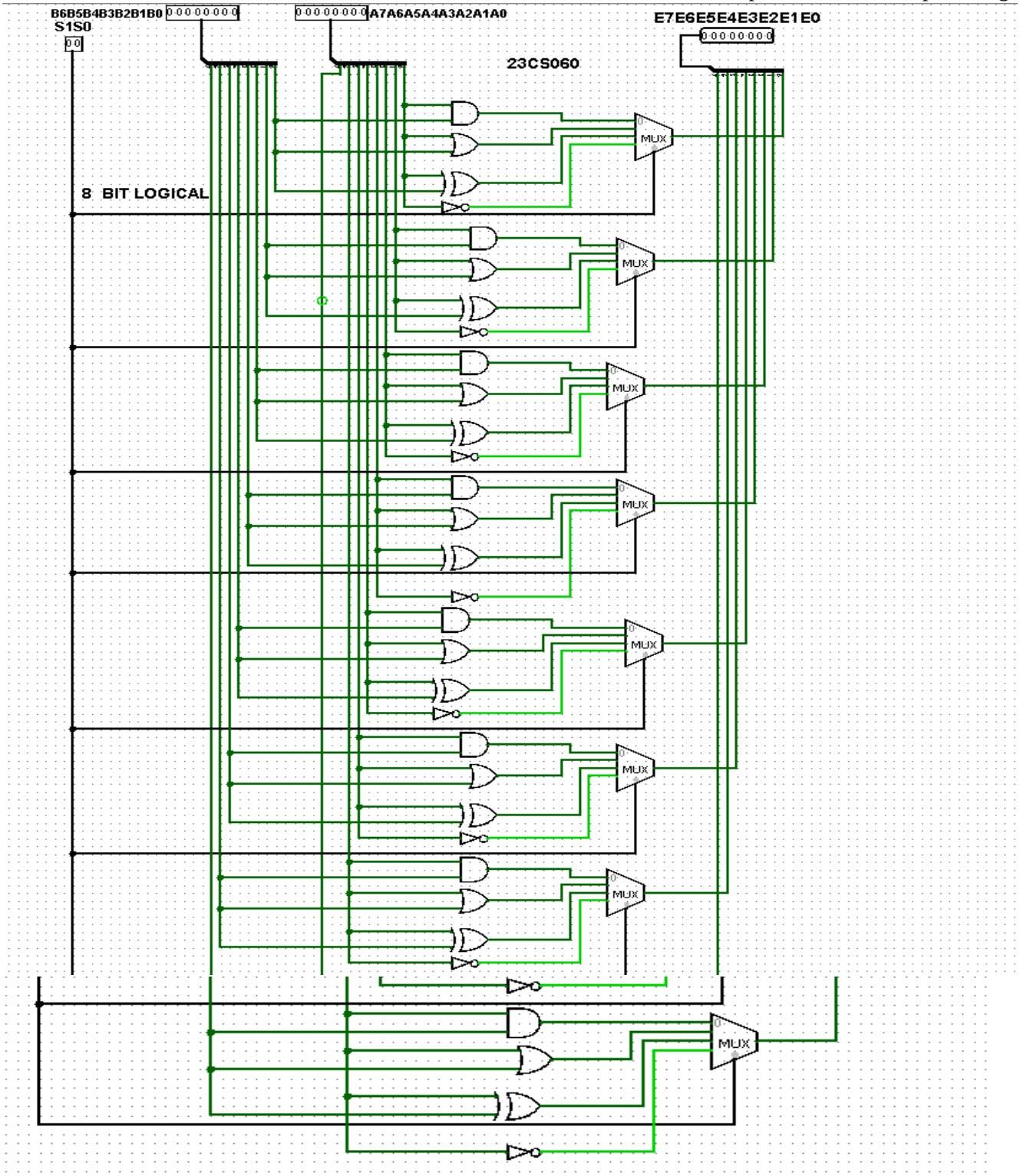

4 BIT ARITHMATIC
A3A2A1A0
0000
B3B2B1B0
0000
CIN
c in
c out
MUX
23CS060
0000
S1S0
COUT

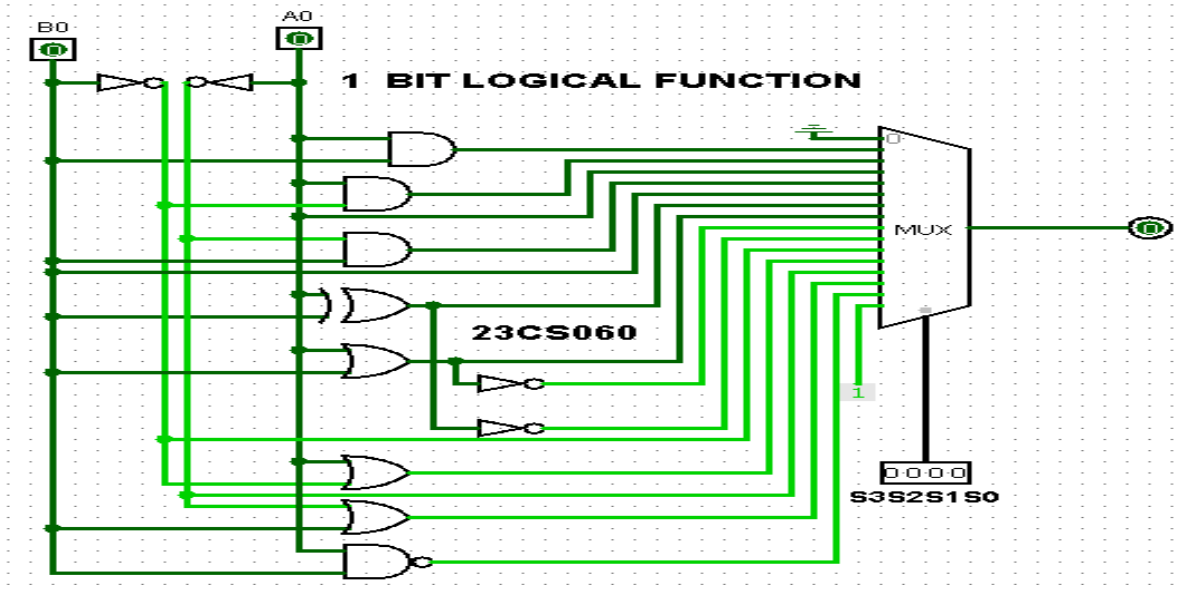

A7A6A5A3A2A1A0
B7B6B5B3B2B1B0
CIN
23CS060
8 BIT ARITHMATIC
MUX
c in
c out
S1S0
COUT

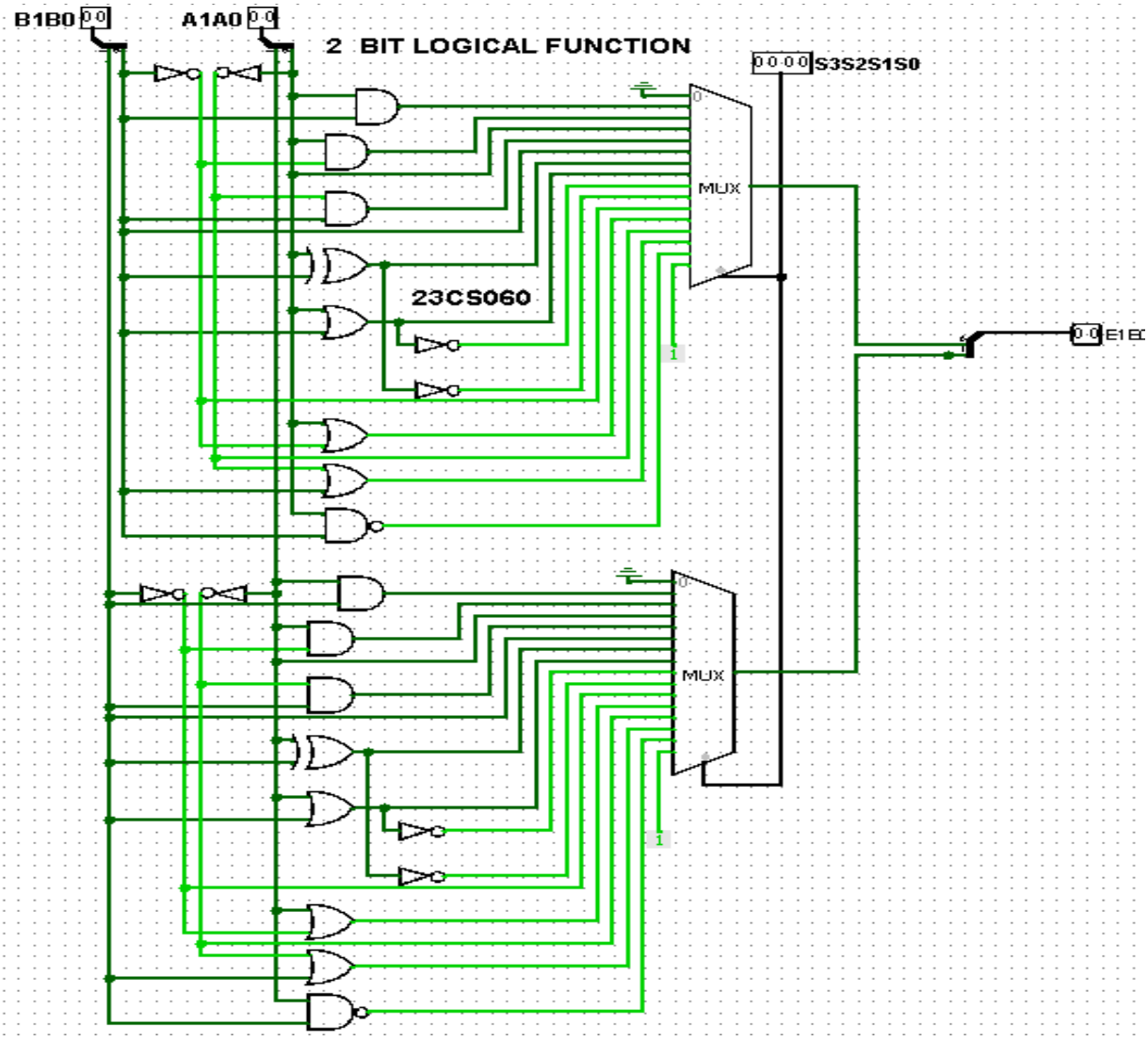

BO
A0
1 BIT LOGICAL
23CS060
MUX
E0
S1S0

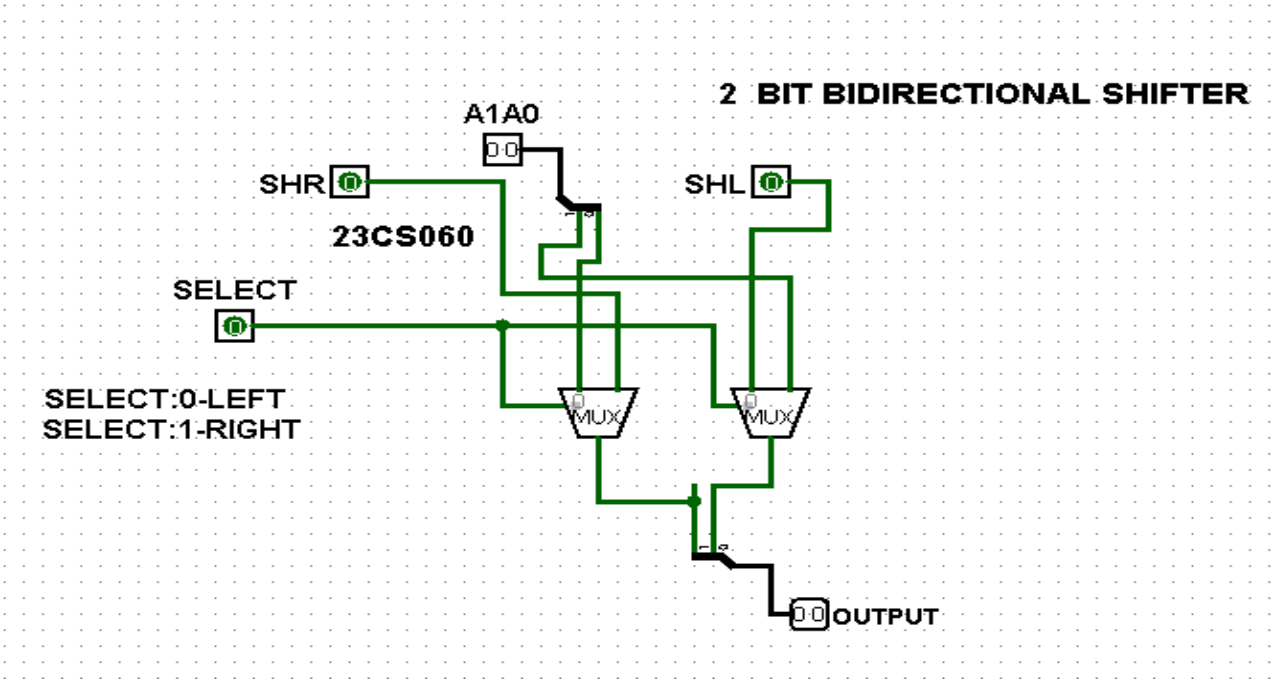

B1B0
A1A0
2 BIT LOGICAL
MUX
23CS060
S1S0
MUX
E1E0

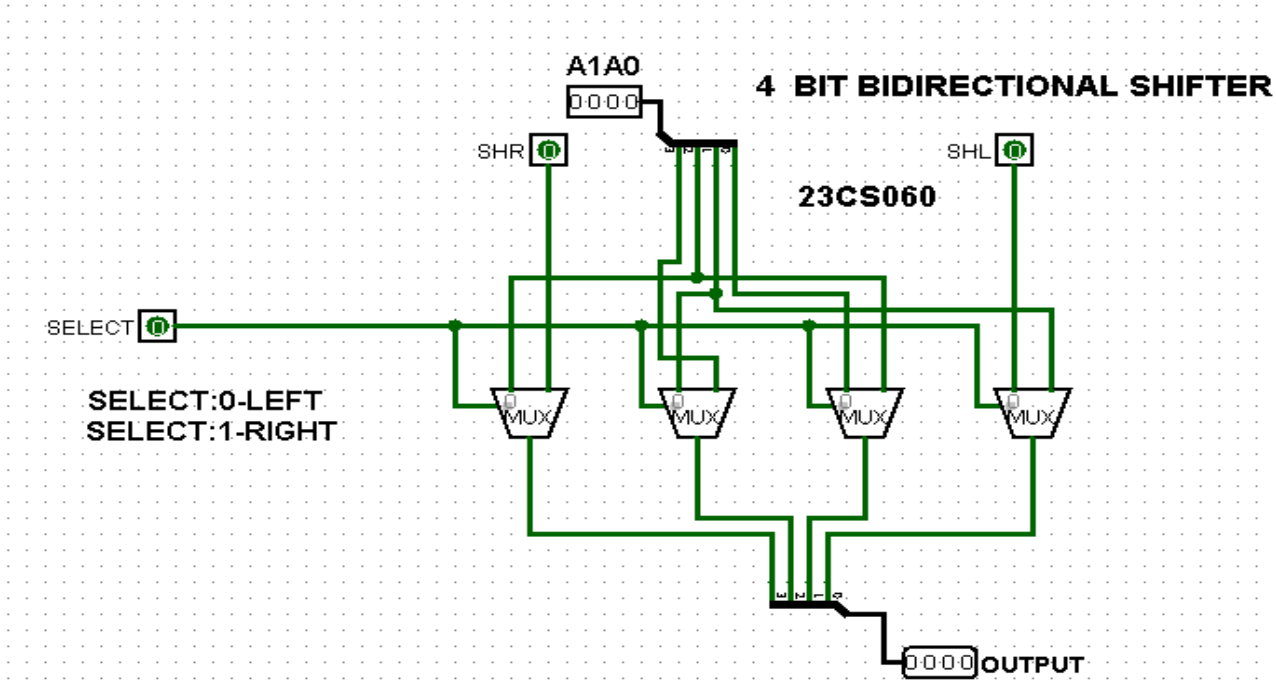

B3B2B1B0
A3A2A1A0
4 BIT LOGICAL
MUX
23CS060
S1S0
MUX
MUX
MUX
E3E2E1E0

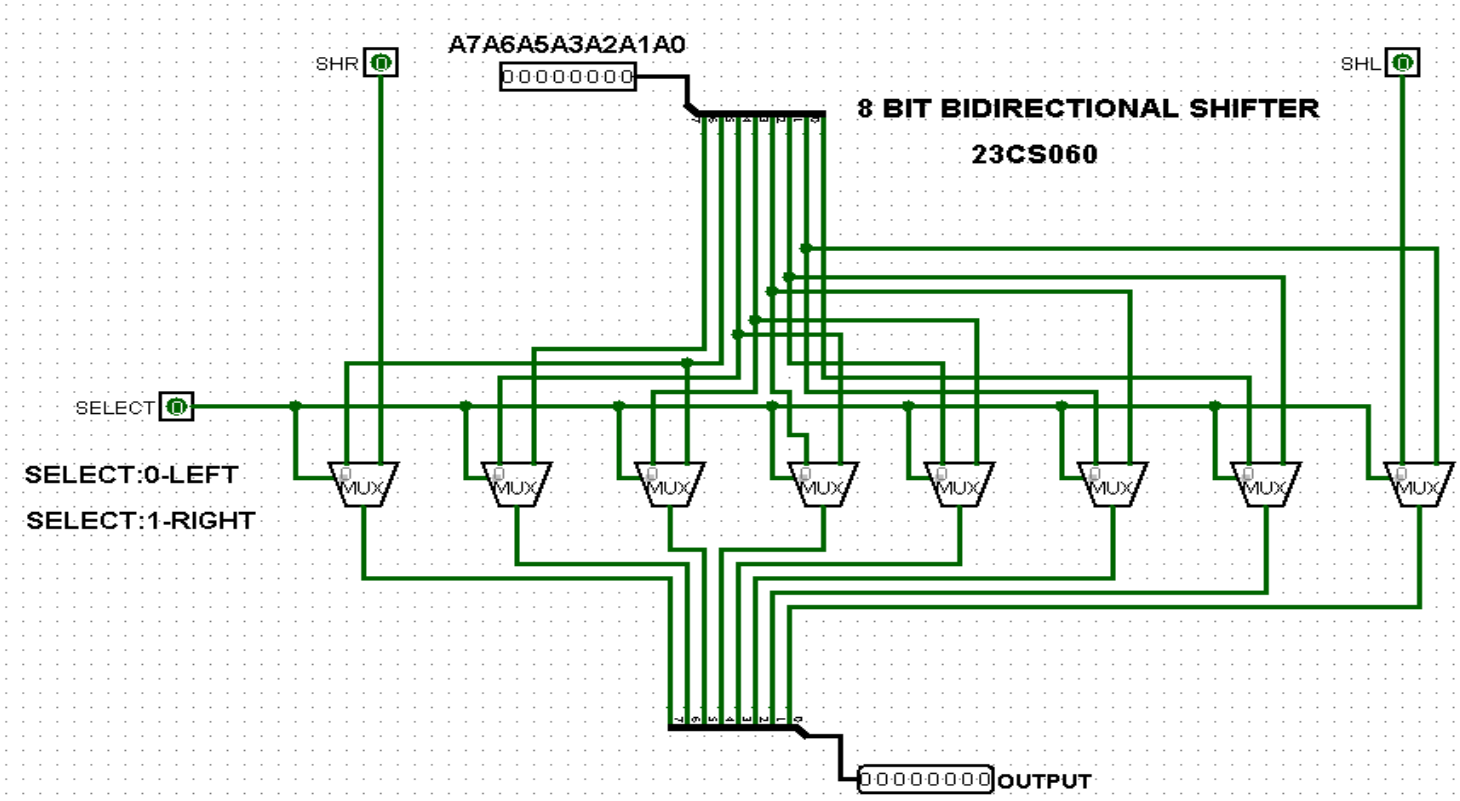

B6B5B4B3B2B1B0
S1S0
A7A6A5A4A3A2A1A0
E7E6E5E4E3E2E1E0
23CS060
8 BIT LOGICAL
MUX

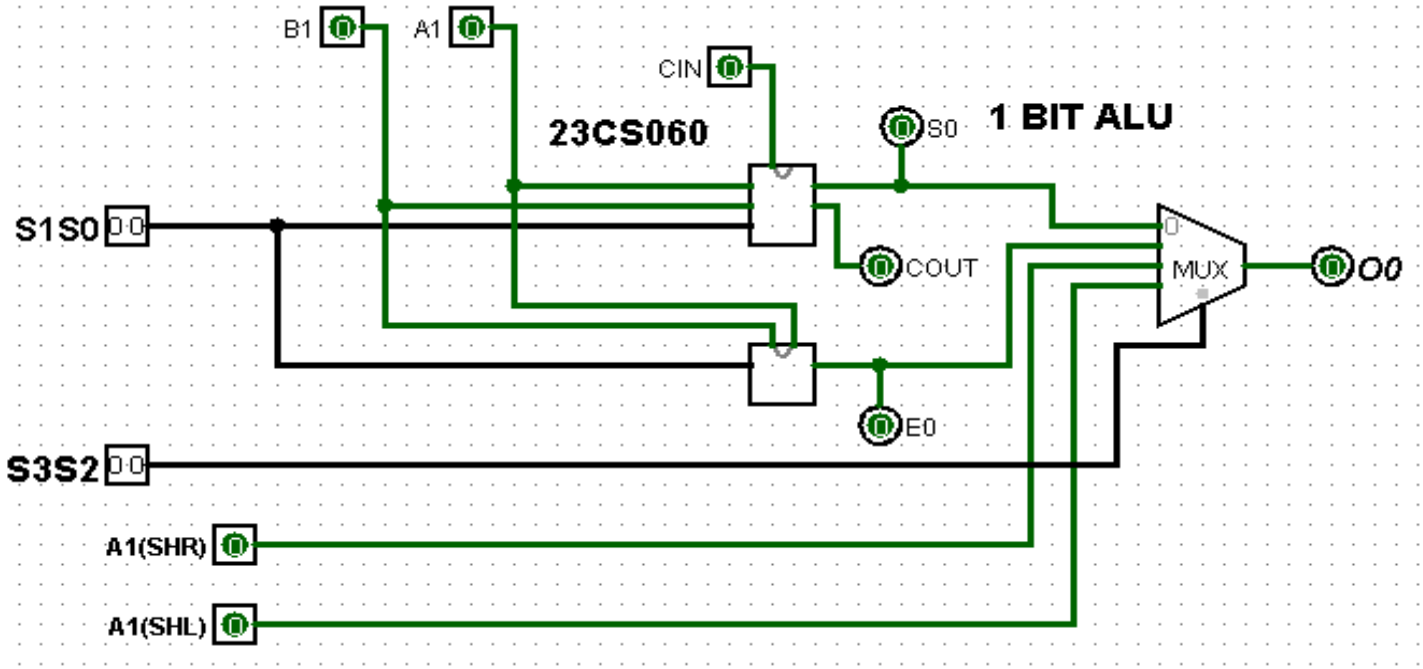

B0
A0
1 BIT LOGICAL FUNCTION
MUX
23CS060
0000
S3S2S1S0

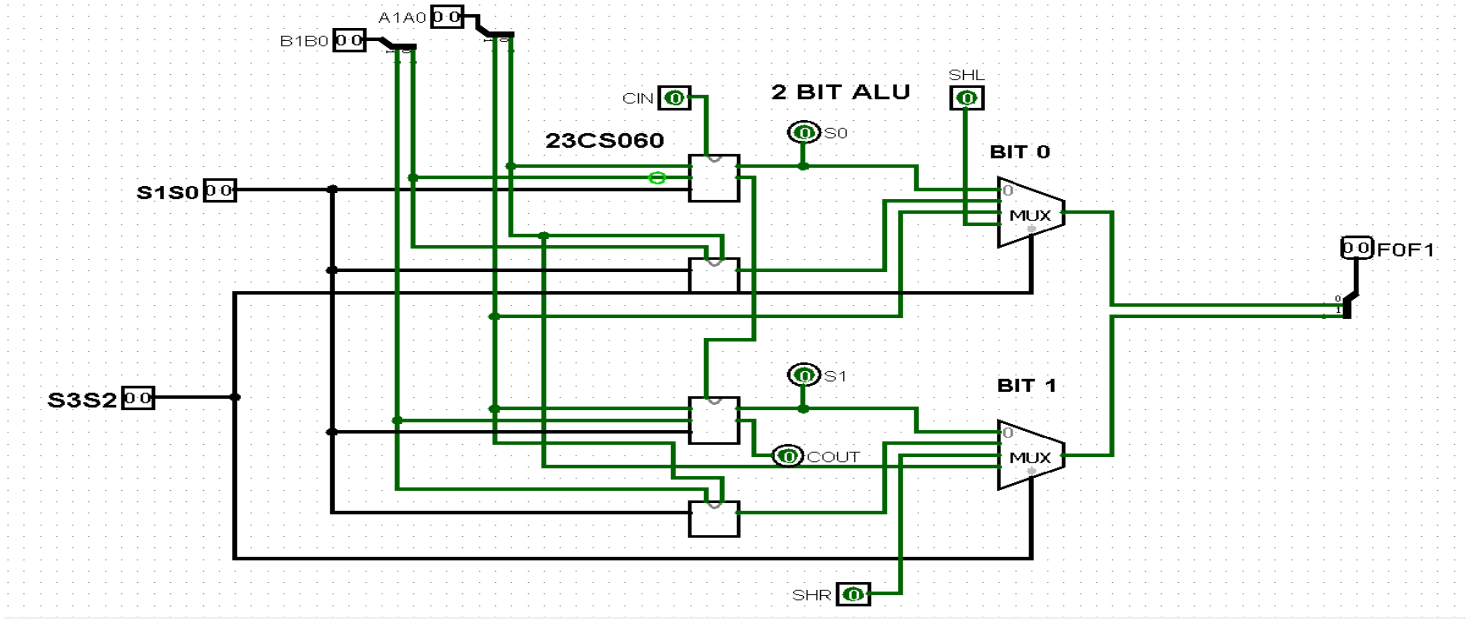

B1B0
A1A0
2 BIT LOGICAL FUNCTION
0000 S3S2S1S0
MUX
23CS060
MUX

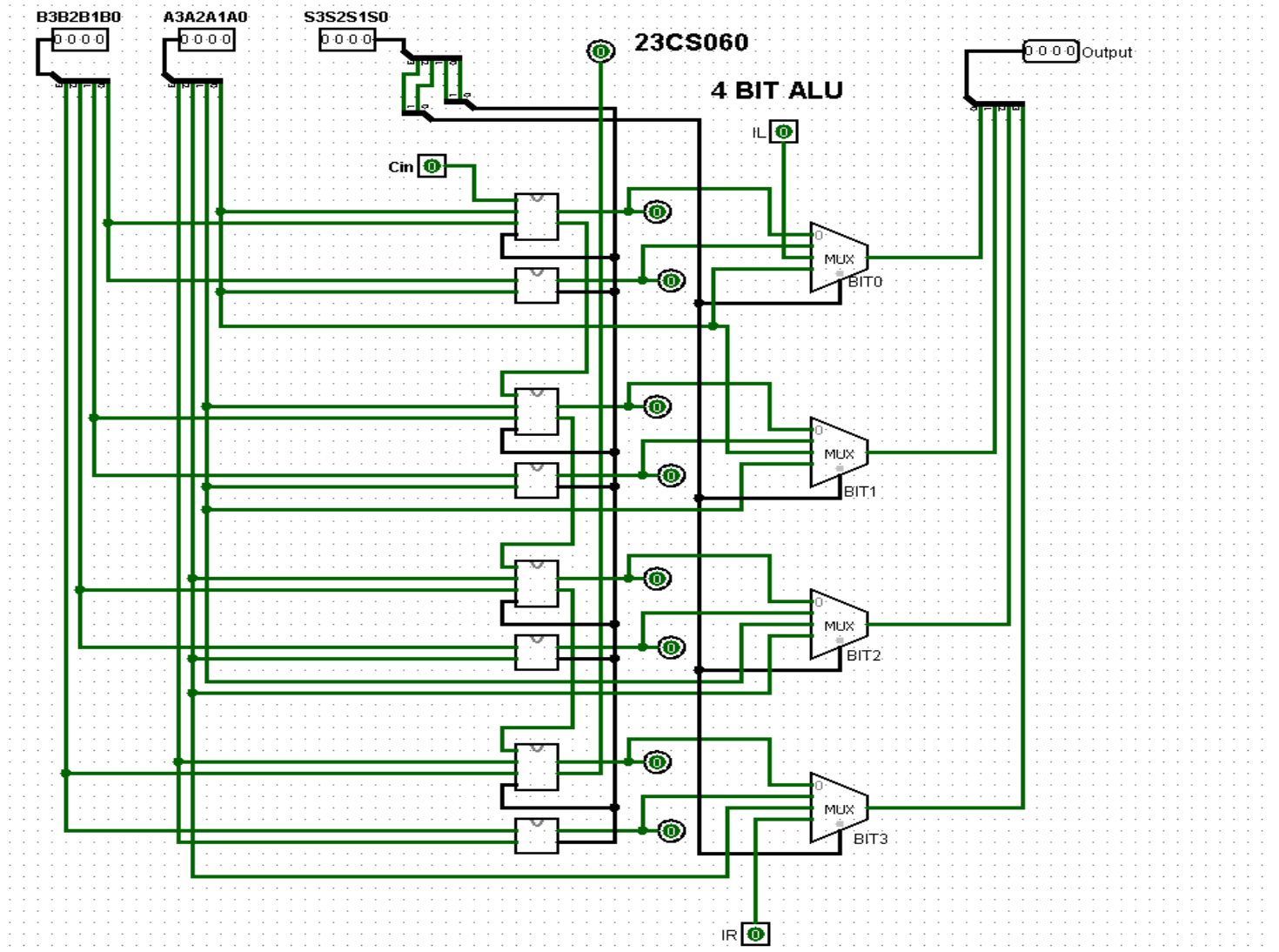

2 BIT BIDIRECTIONAL SHIFTER
A1A0
00
SHR
SHL
23CS060
SELECT
SELECT:0-LEFT
SELECT:1-RIGHT
MUX
MUX
00
OUTPUT

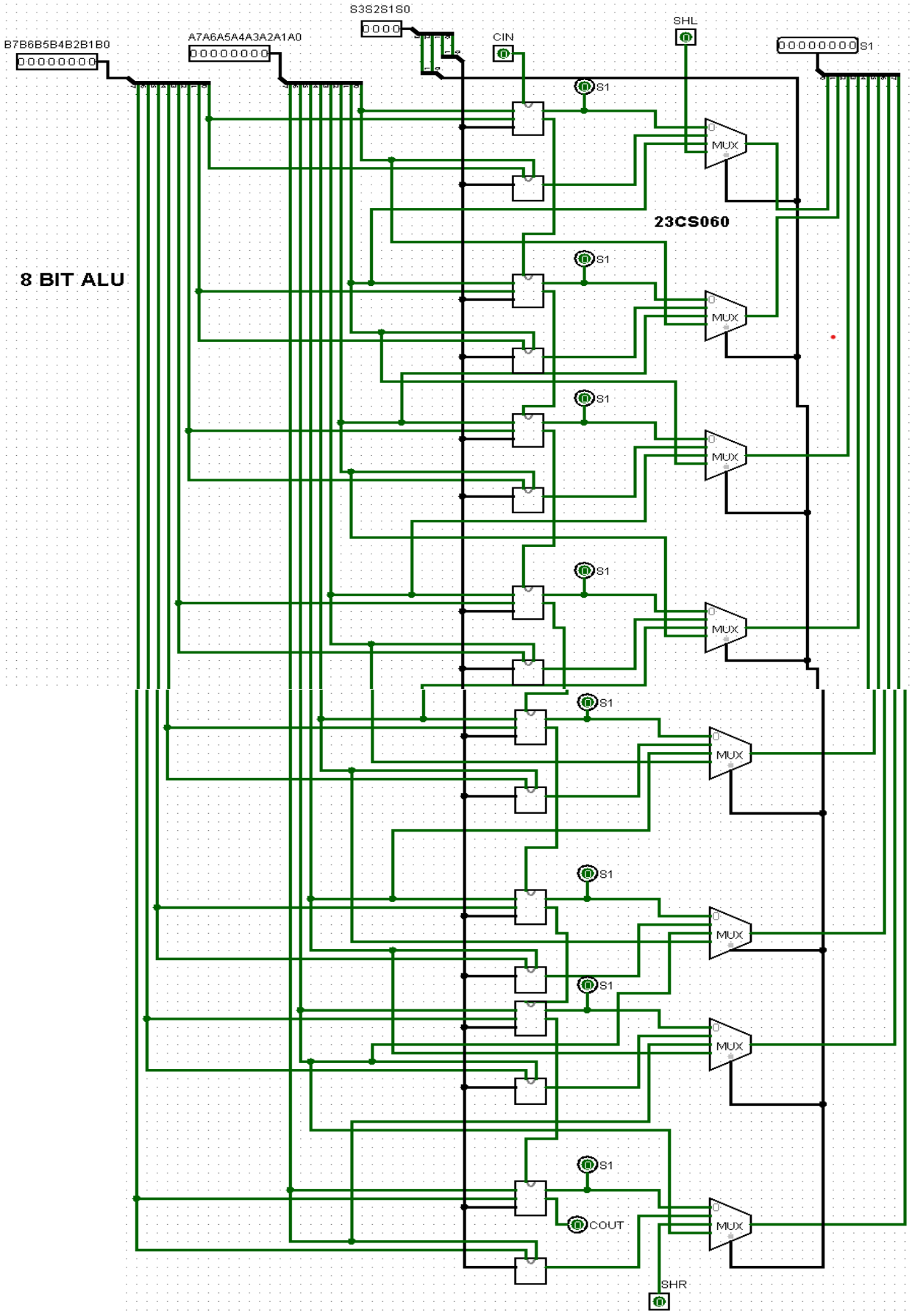

A1A0
0000
4 BIT BIDIRECTIONAL SHIFTER
SHR
SHL
23CS060
SELECT
SELECT:0-LEFT
SELECT:1-RIGHT
MUX
MUX
MUX
MUX
0000
OUTPUT


A7A6A5A3A2A1A0
SHR
SHL
8 BIT BIDIRECTIONAL SHIFTER
23CS060
SELECT
SELECT:0-LEFT
SELECT:1-RIGHT
MUX
OUTPUT

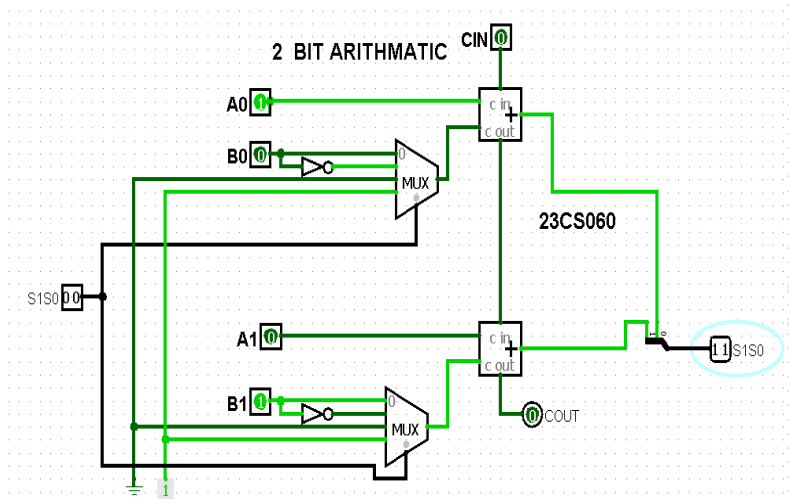

B1
A1
CIN
23CS060
S0
1 BIT ALU
S1S0
COUT
MUX
O0
E0
S3S2
A1(SHR)
A1(SHL)

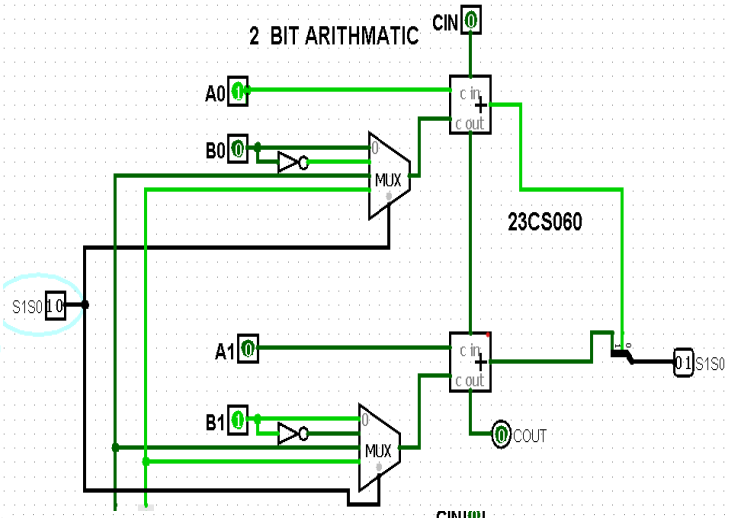

A1A0
B1B0
CIN
2 BIT ALU
SHL
23CS060
S0
BIT 0
S1S0
MUX
FOF1
S1
BIT 1
S3S2
COUT
MUX
SHR

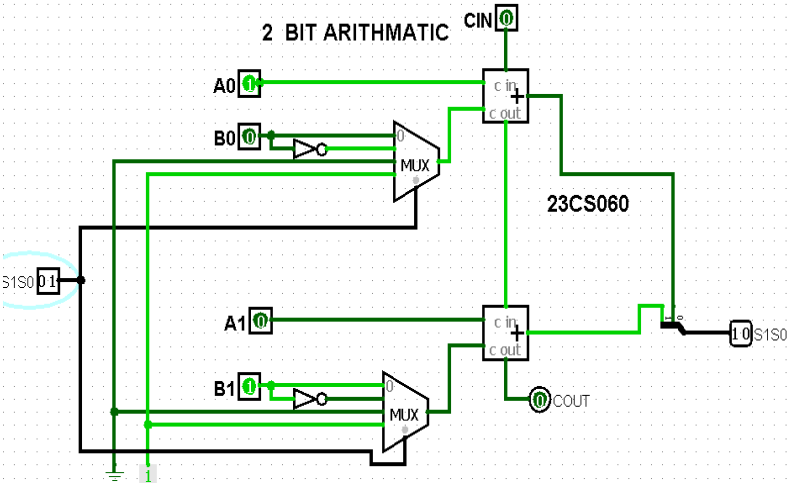

B3B2B1B0
A3A2A1A0
S3S2S1S0
23CS060
4 BIT ALU
Output
IL
Cin
MUX
BIT0
MUX
BIT1
MUX
BIT2
MUX
BIT3
IR

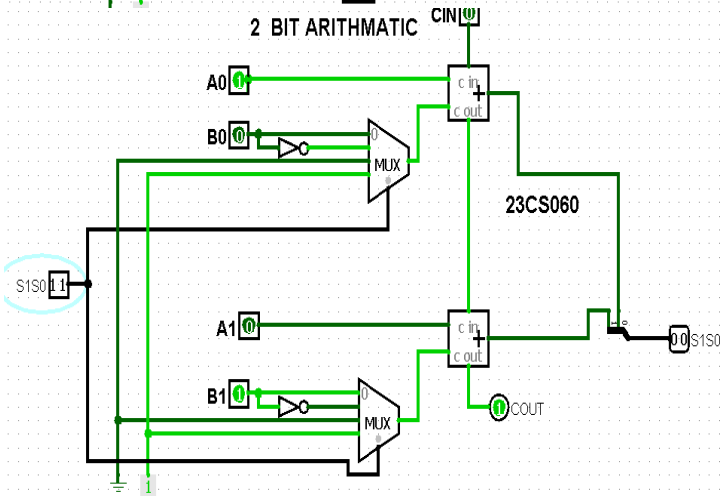

8 BIT ALU
23CS060
B7B6B5B4B2B1B0
A7A6A5A4A3A2A1A0
S3S2S1S0
CIN
SHL
S1
MUX
COUT
SHR

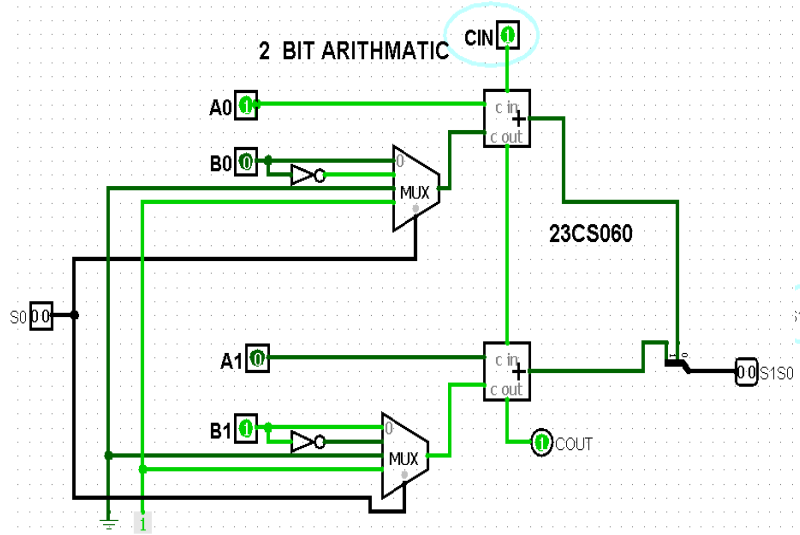
OUTPUT:

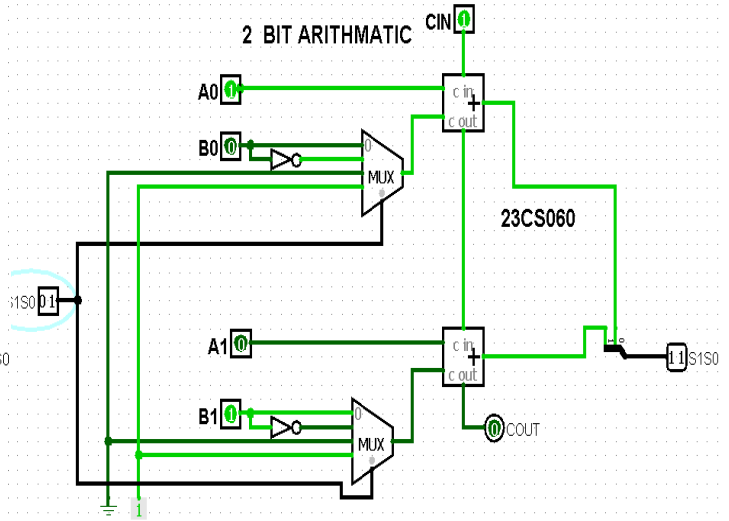

2 BIT ARITHMATIC
CIN
A0
B0
MUX
23CS060
S1S0 0 0
A1
B1
COUT
1 1 S1S0

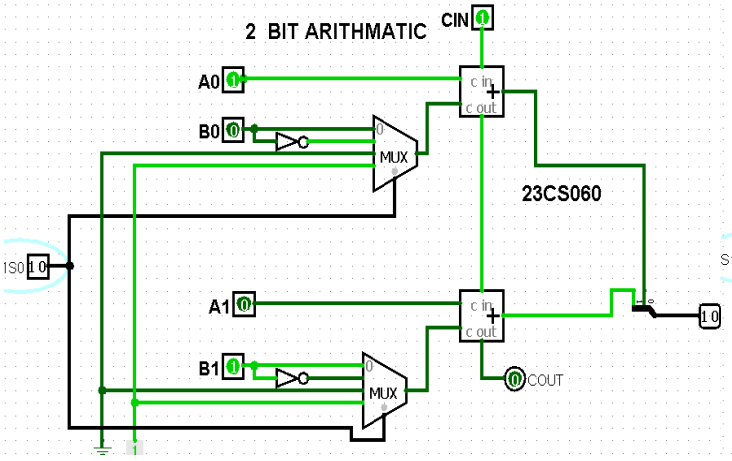

2 BIT ARITHMATIC
CIN
A0
B0
MUX
23CS060
S1S0 1 0
A1
B1
COUT
0 1 S1S0

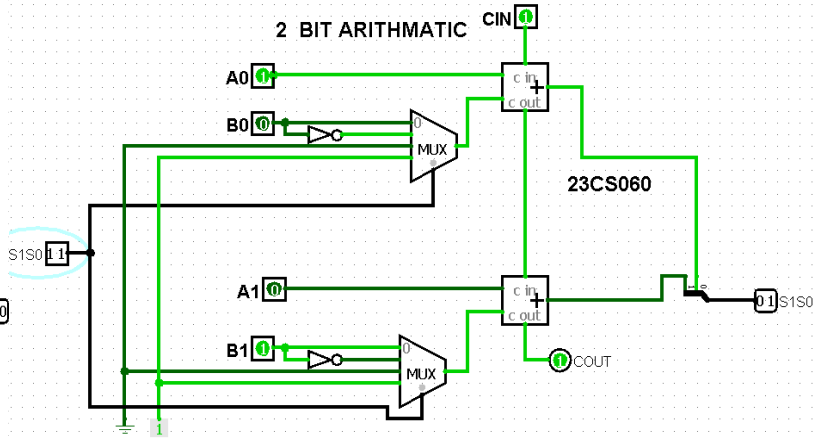

2 BIT ARITHMATIC
CIN
A0
B0
MUX
23CS060
S1S0 0 1
A1
B1
COUT
1 0 S1S0

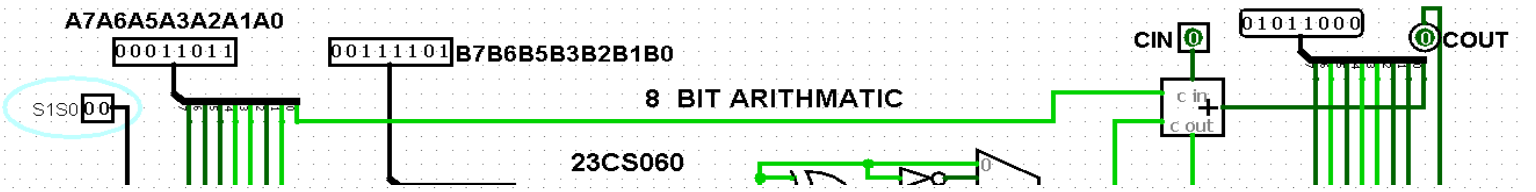

2 BIT ARITHMATIC
CIN
A0
B0
MUX
23CS060
S1S0 1 1
A1
B1
COUT
0 0 S1S0

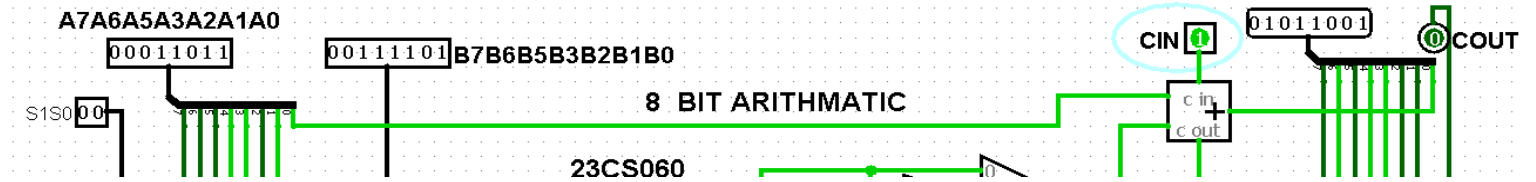

2 BIT ARITHMATIC
CIN
A0
B0
MUX
23CS060
S0 0 0
A1
B1
COUT
0 0 S1S0


2 BIT ARITHMATIC
CIN
A0
B0
MUX
23CS060
S1S0 0 1
A1
B1
COUT
1 1 S1S0

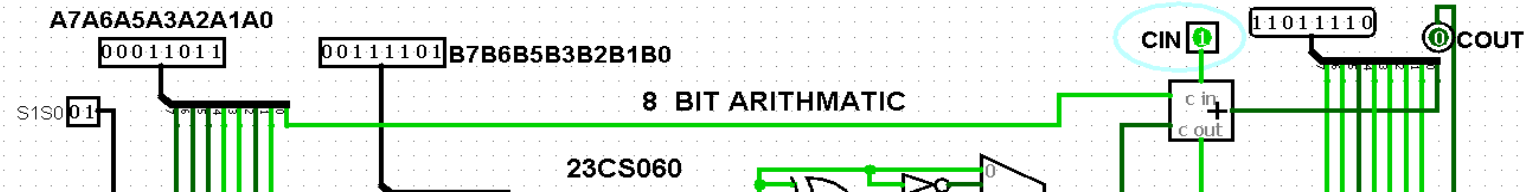

2 BIT ARITHMATIC
CIN
A0
B0
MUX
23CS060
A1
B1
COUT


2 BIT ARITHMATIC
CIN
A0
B0
MUX
23CS060
A1
B1
COUT


A7A6A5A3A2A1A0
00011011
00111101B7B6B5B3B2B1B0
S1S0 00
8 BIT ARITHMATIC
23CS060
CIN
01011000
COUT

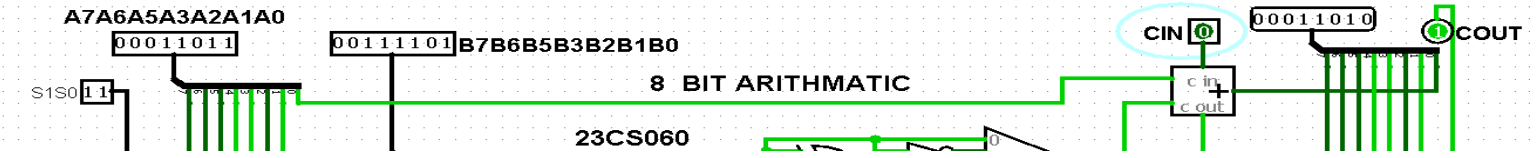

A7A6A5A3A2A1A0
00011011
00111101B7B6B5B3B2B1B0
S1S0 00
8 BIT ARITHMATIC
23CS060
CIN
01011001
COUT


A7A6A5A3A2A1A0
00011011
00111101B7B6B5B3B2B1B0
S1S0 01
8 BIT ARITHMATIC
CIN
11011101
COUT

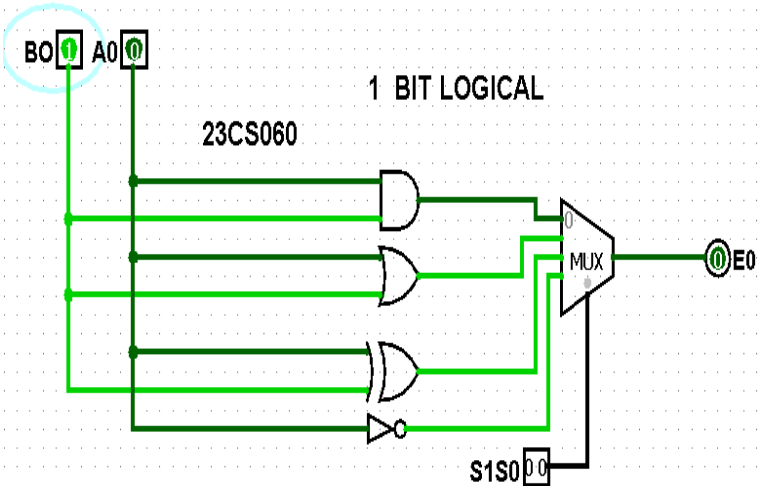

A7A6A5A3A2A1A0
00011011
00111101B7B6B5B3B2B1B0
S1S0 01
8 BIT ARITHMATIC
23CS060
CIN
11011110
COUT

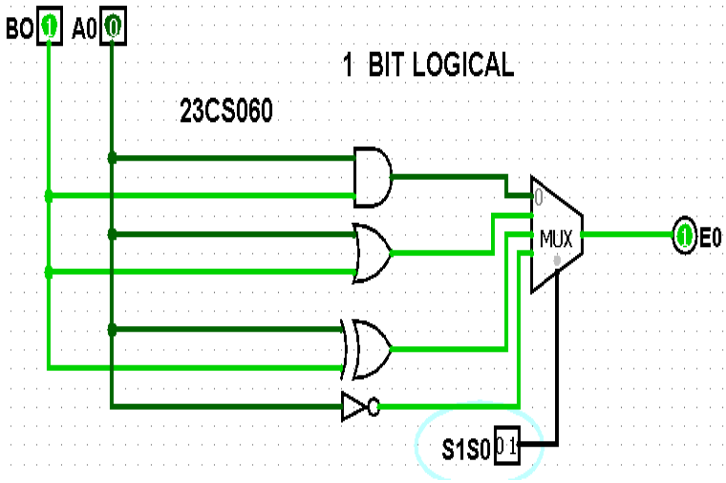

A7A6A5A3A2A1A0
00011011
00111101B7B6B5B3B2B1B0
S1S0 10
8 BIT ARITHMATIC
23CS060
CIN
00011011
COUT

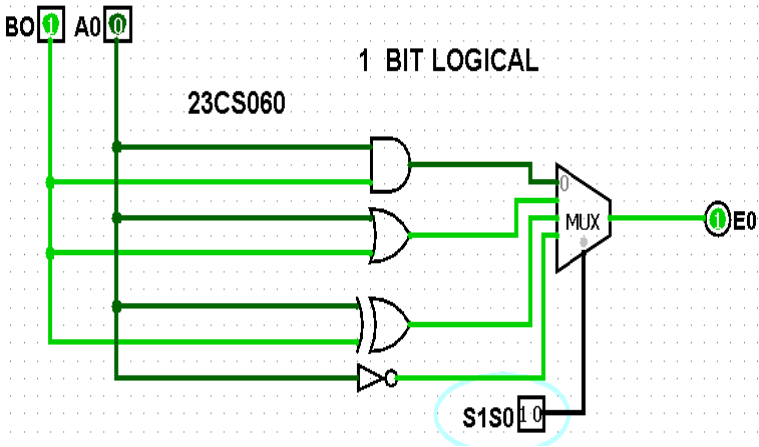

A7A6A5A3A2A1A0
00011011
00111101B7B6B5B3B2B1B0
S1S0 10
8 BIT ARITHMATIC
CIN
00011100
COUT

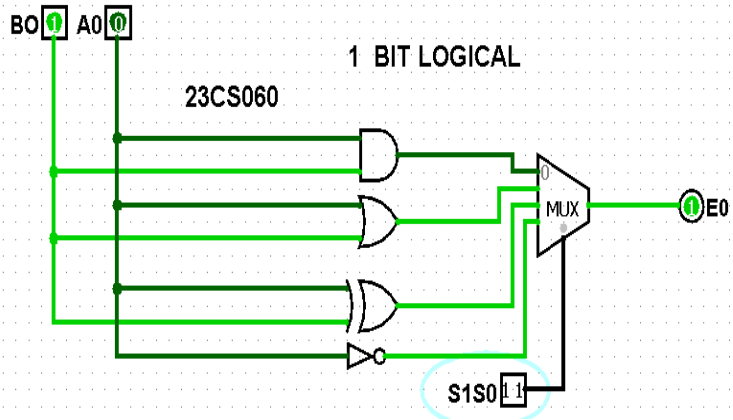

A7A6A5A3A2A1A0
00011011
00111101B7B6B5B3B2B1B0
S1S0 11
8 BIT ARITHMATIC
23CS060
CIN
00011010
COUT

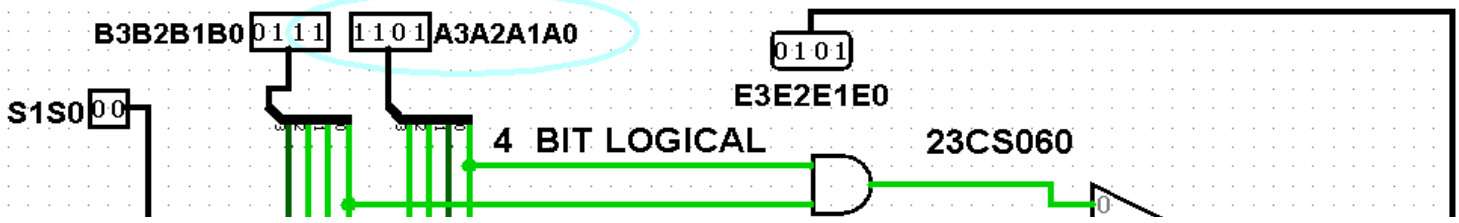

A7A6A5A3A2A1A0
00011011
00111101B7B6B5B3B2B1B0
S1S0 11
8 BIT ARITHMATIC
23CS060
CIN
00011011
COUT
c in
c out

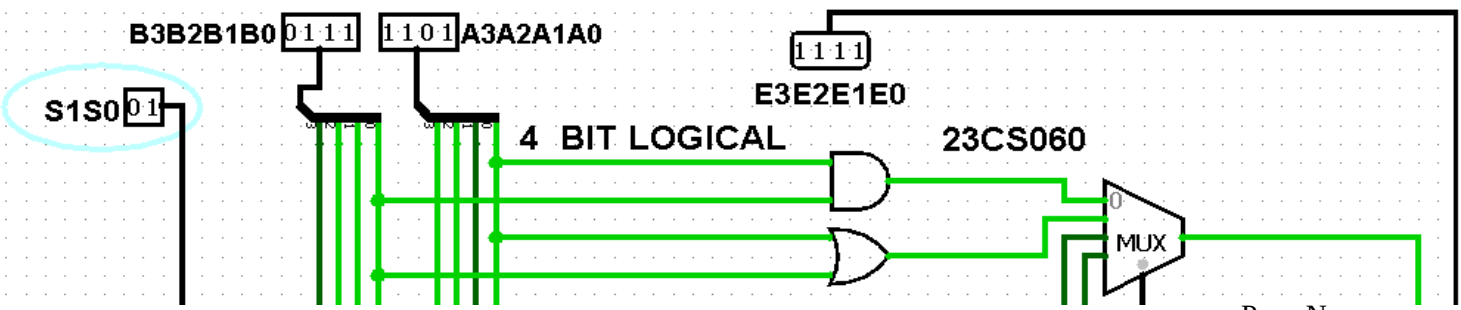

BO A0
1 BIT LOGICAL
23CS060
MUX
E0
S1S0 00

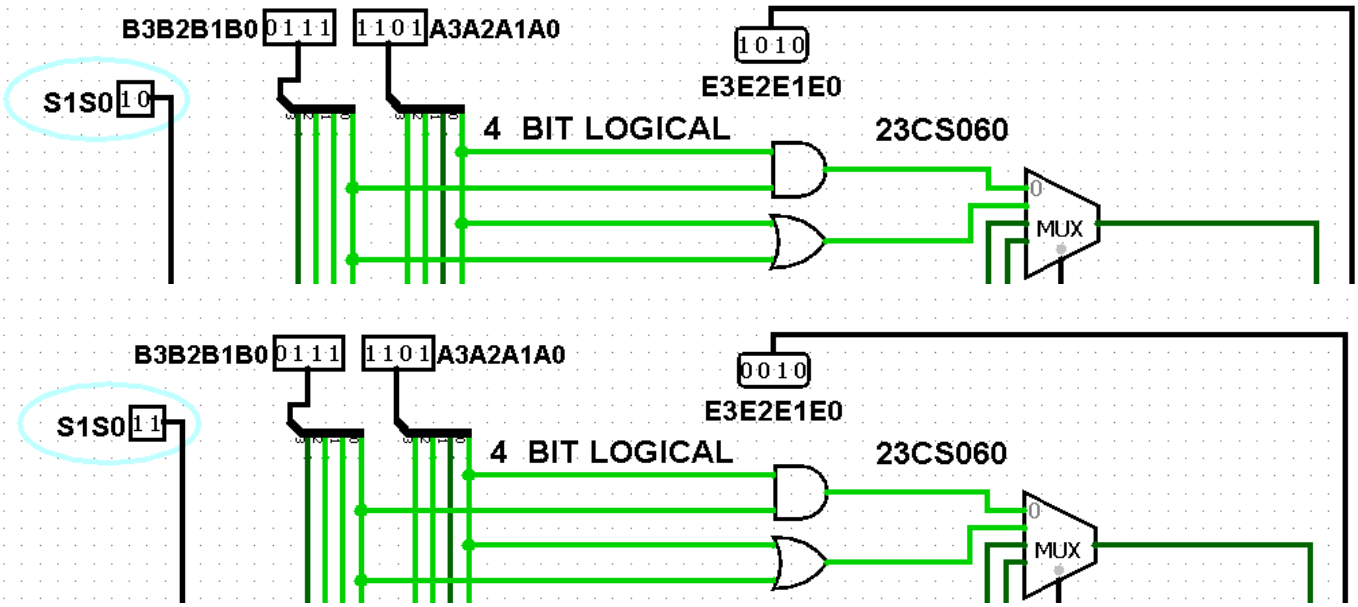

BO A0
1 BIT LOGICAL
23CS060
MUX
E0
S1S0 01

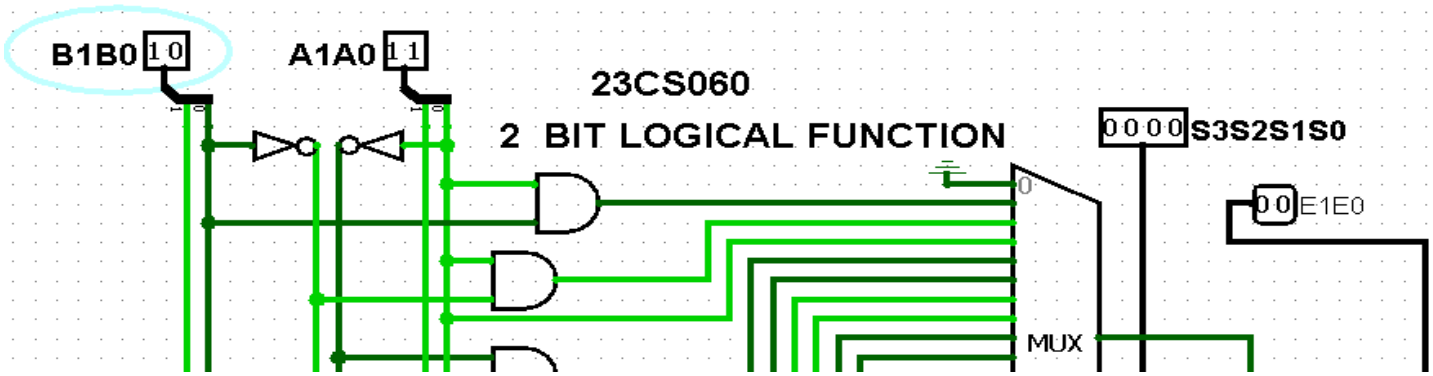

BO A0
1 BIT LOGICAL
23CS060
MUX
E0
S1S0 10

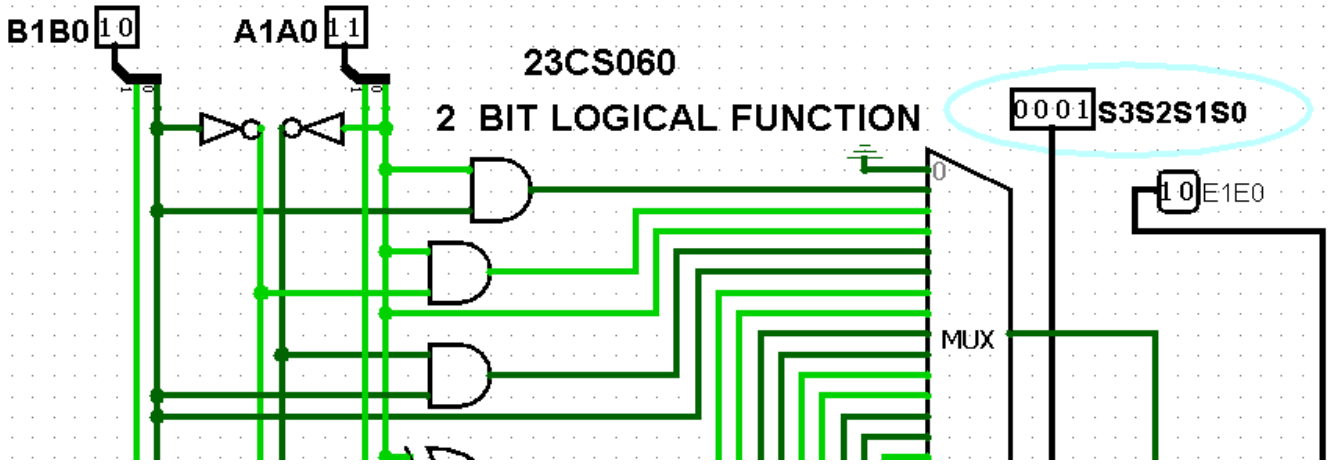

BO A0
1 BIT LOGICAL
23CS060
MUX
E0
S1S0 11

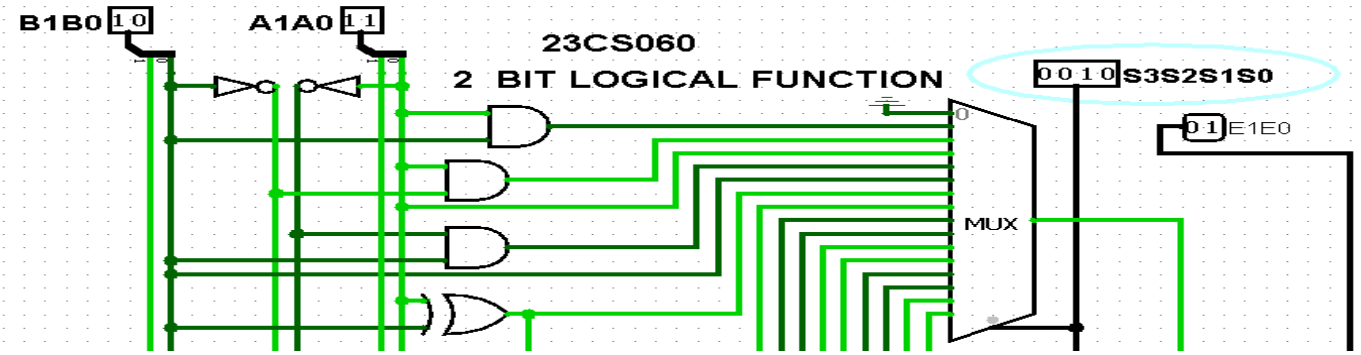

B3B2B1B0 0111
1101 A3A2A1A0
0101
E3E2E1E0
S1S0 00
4 BIT LOGICAL
23CS060

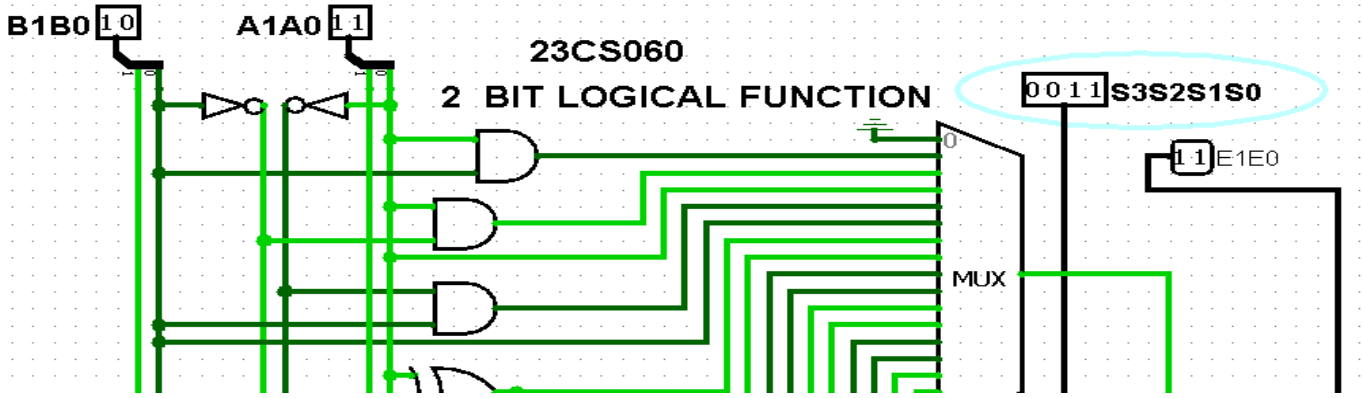

B3B2B1B0 0111
1101 A3A2A1A0
1111
E3E2E1E0
S1S0 01
4 BIT LOGICAL
23CS060
MUX

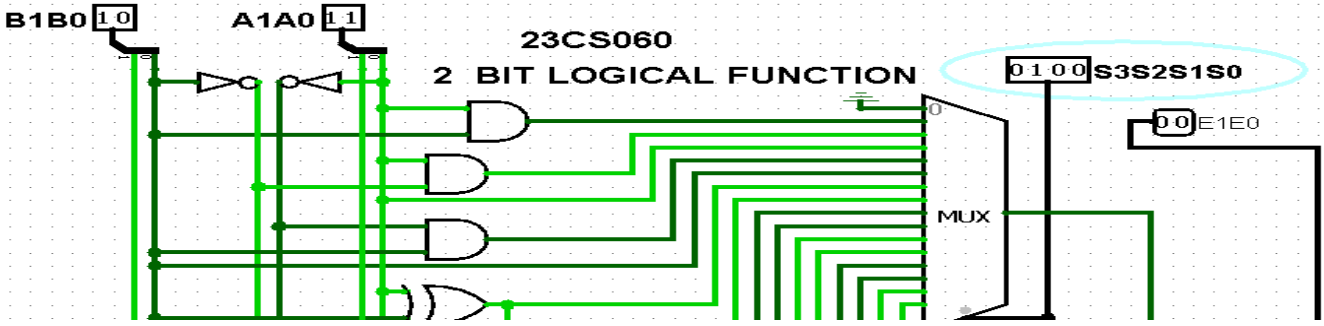

B3B2B1B0 0 1 1 1
1 1 0 1 A3A2A1A0
1 0 1 0
E3E2E1E0
S1S0 1 0
4 BIT LOGICAL
23CS060
0
MUX
B3B2B1B0 0 1 1 1
1 1 0 1 A3A2A1A0
0 0 1 0
E3E2E1E0
S1S0 1 1
4 BIT LOGICAL
23CS060
0
MUX

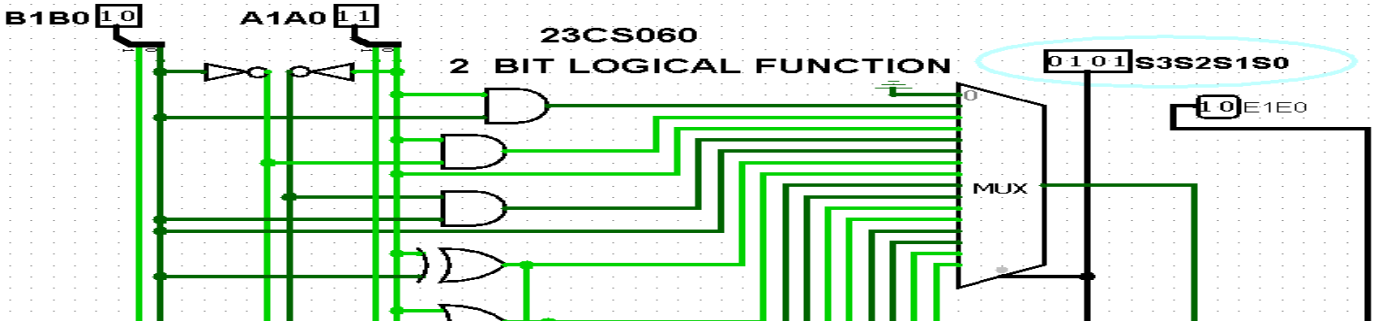

B1B0 1 0
A1A0 1 1
23CS060
2 BIT LOGICAL FUNCTION
0 0 0 0 S3S2S1S0
0 0 E1E0
0
MUX

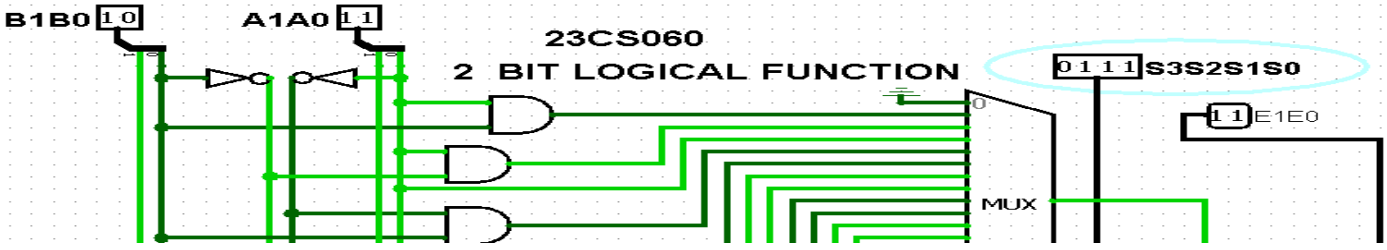

B1B0 1 0
A1A0 1 1
23CS060
2 BIT LOGICAL FUNCTION
0 0 0 1 S3S2S1S0
1 0 E1E0
0
MUX

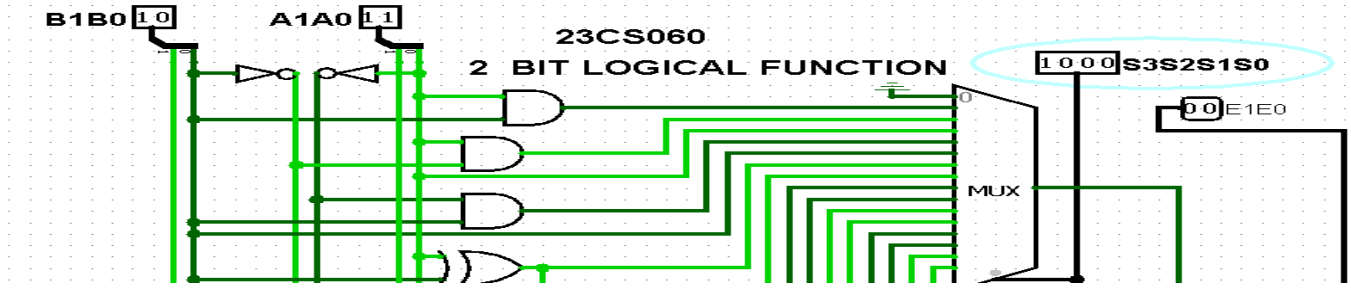

B1B0 1 0
A1A0 1 1
23CS060
2 BIT LOGICAL FUNCTION
0 0 1 0 S3S2S1S0
0 1 E1E0
MUX

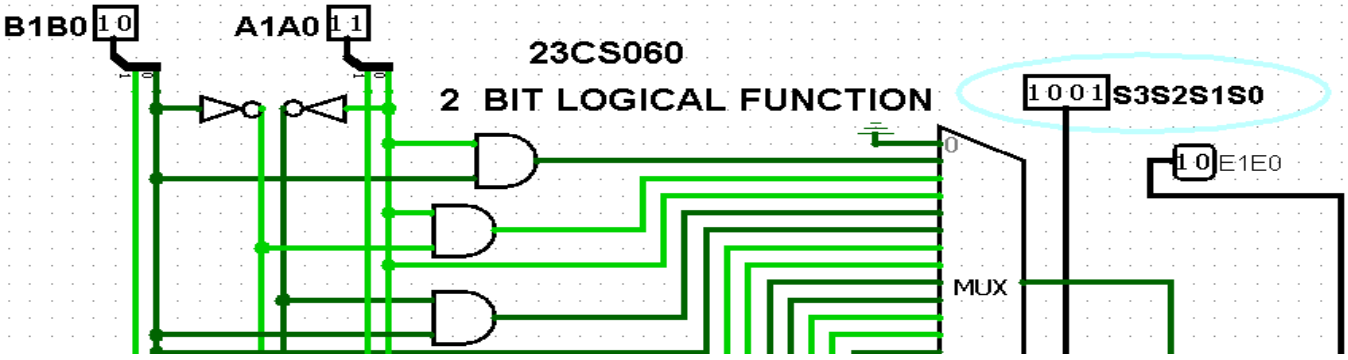

B1B0 1 0
A1A0 1 1
23CS060
2 BIT LOGICAL FUNCTION
0 0 1 1 S3S2S1S0
1 1 E1E0
MUX

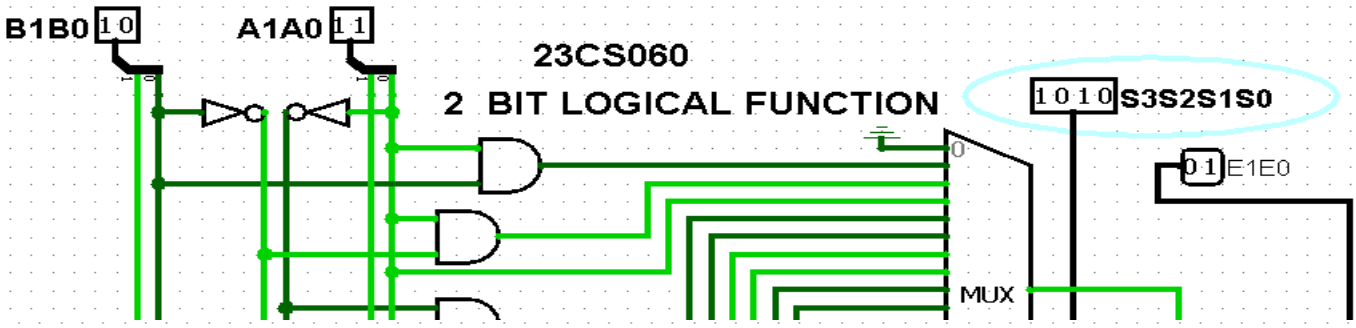

B1B0 1 0
A1A0 1 1
23CS060
2 BIT LOGICAL FUNCTION
0 1 0 0 S3S2S1S0
0 0 E1E0
MUX

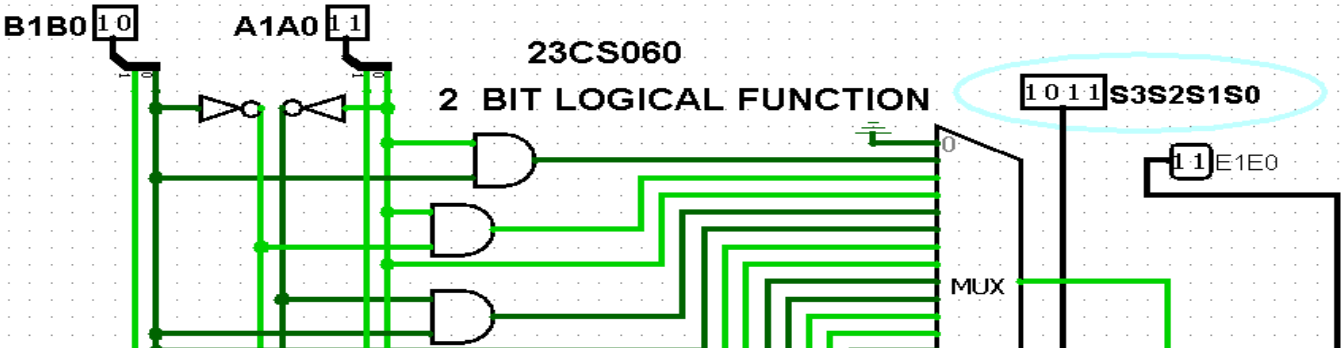

B1B0 1 0
A1A0 1 1
23CS060
2 BIT LOGICAL FUNCTION
0 1 0 1 S3S2S1S0
1 0 E1E0
MUX

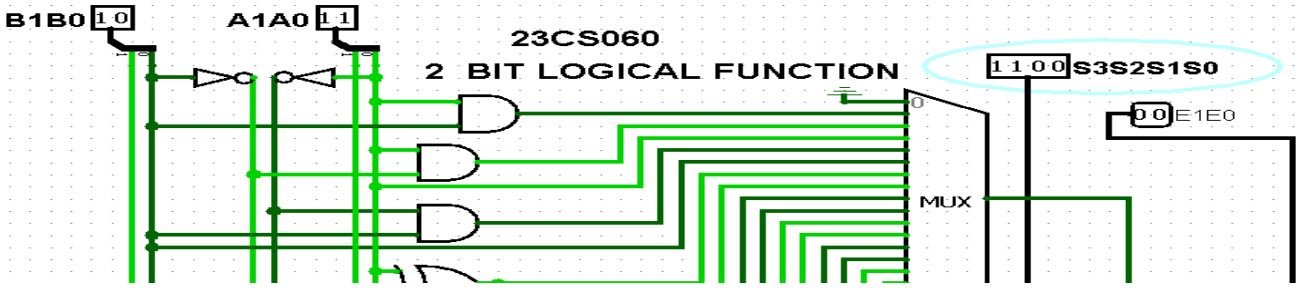

B1B0 1 0
A1A0 1 1
23CS060
2 BIT LOGICAL FUNCTION
0 1 1 1 S3S2S1S0
1 1 E1E0
MUX

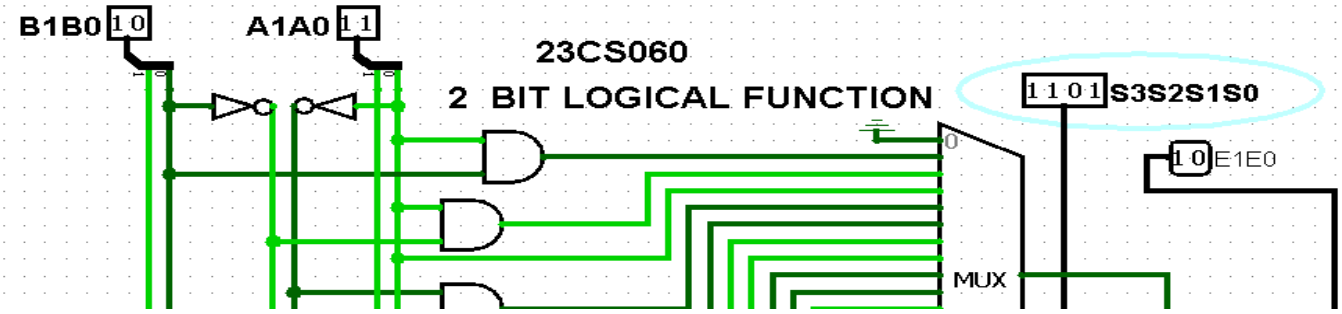

B1B0 10
A1A0 11
23CS060
2 BIT LOGICAL FUNCTION
1000 S3S2S1S0
00 E1E0
MUX

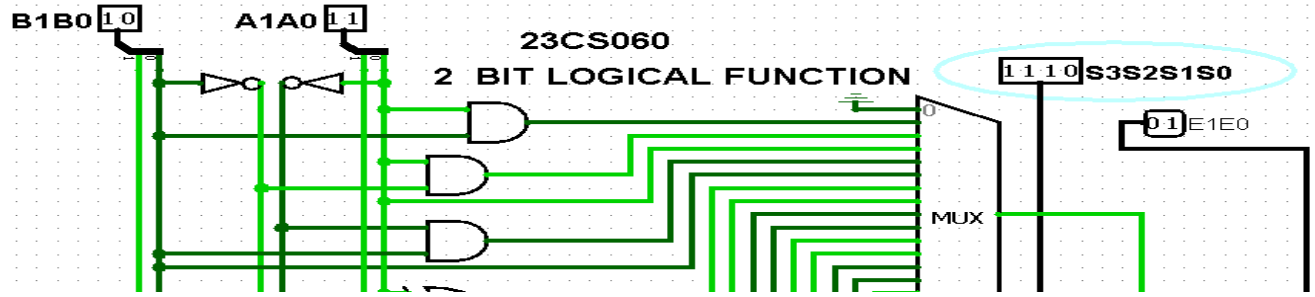

B1B0 10
A1A0 11
23CS060
2 BIT LOGICAL FUNCTION
1001 S3S2S1S0
10 E1E0
MUX

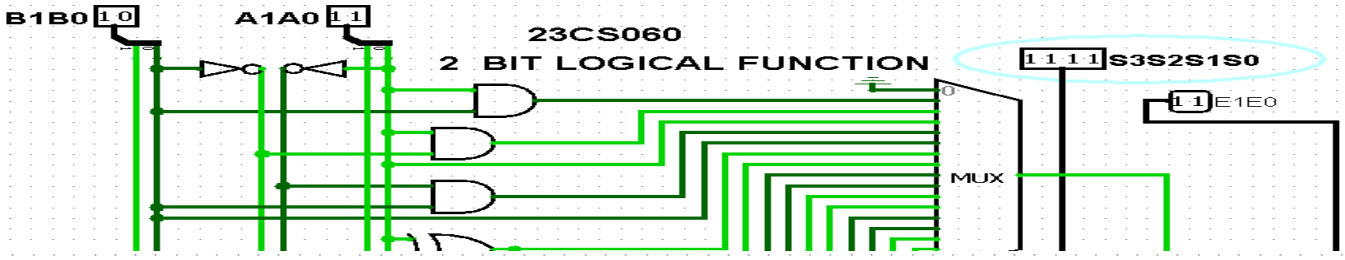

B1B0 10
A1A0 11
23CS060
2 BIT LOGICAL FUNCTION
1010 S3S2S1S0
01 E1E0
MUX

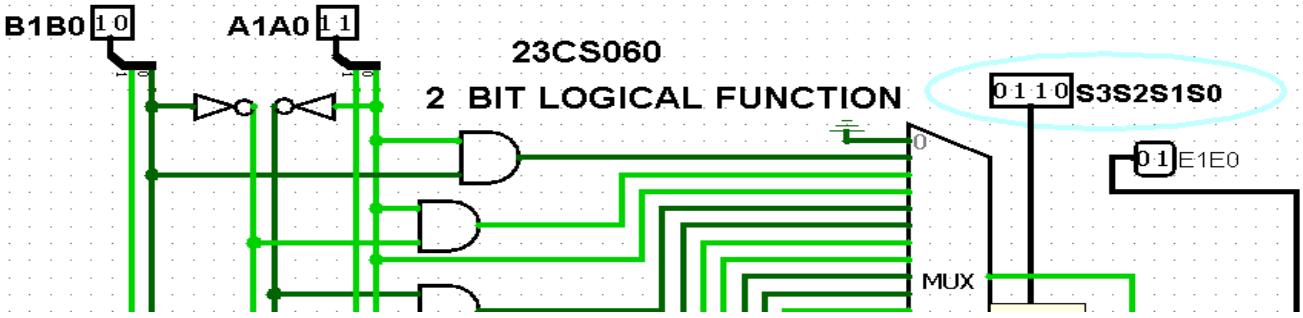

B1B0 10
A1A0 11
23CS060
2 BIT LOGICAL FUNCTION
1011 S3S2S1S0
11 E1E0
MUX

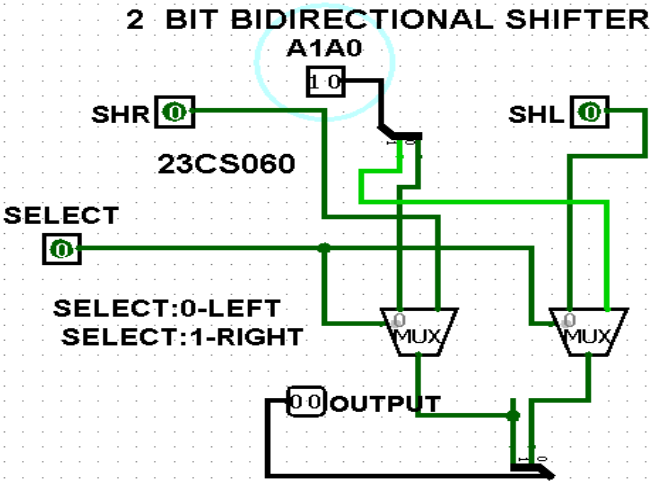

B1B0 10
A1A0 11
23CS060
2 BIT LOGICAL FUNCTION
1100 S3S2S1S0
00 E1E0
MUX

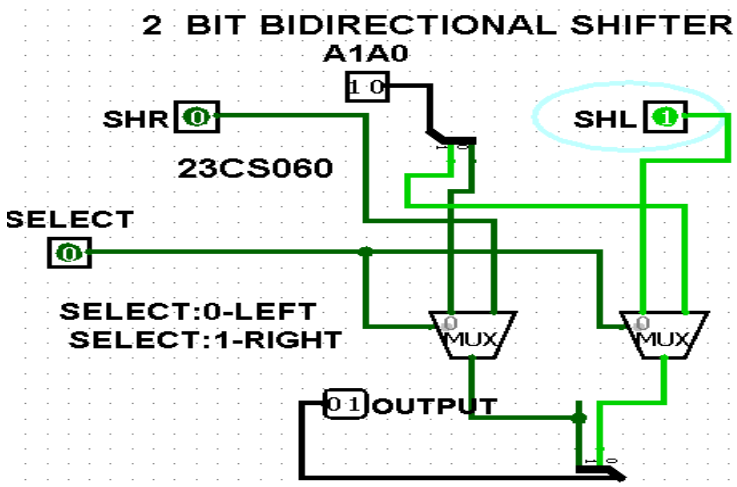

B1B0 10
A1A0 11
23CS060
2 BIT LOGICAL FUNCTION
1101 S3S2S1S0
10 E1E0
MUX

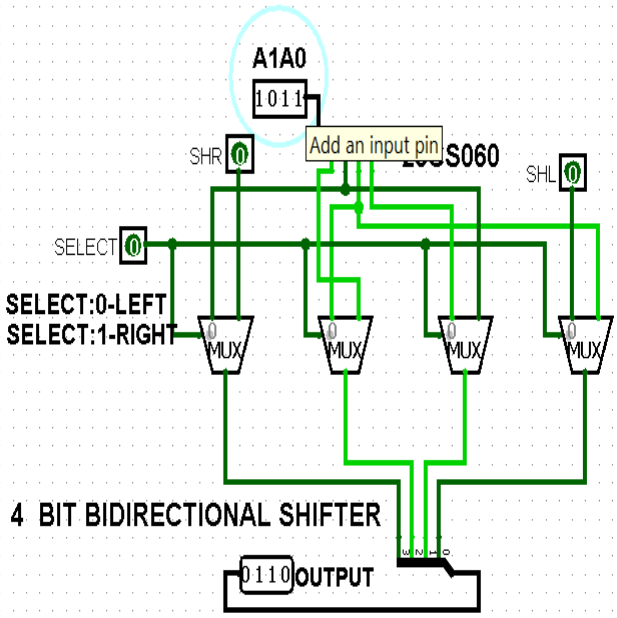

B1B0 10
A1A0 11
23CS060
2 BIT LOGICAL FUNCTION
1110 S3S2S1S0
01 E1E0
MUX

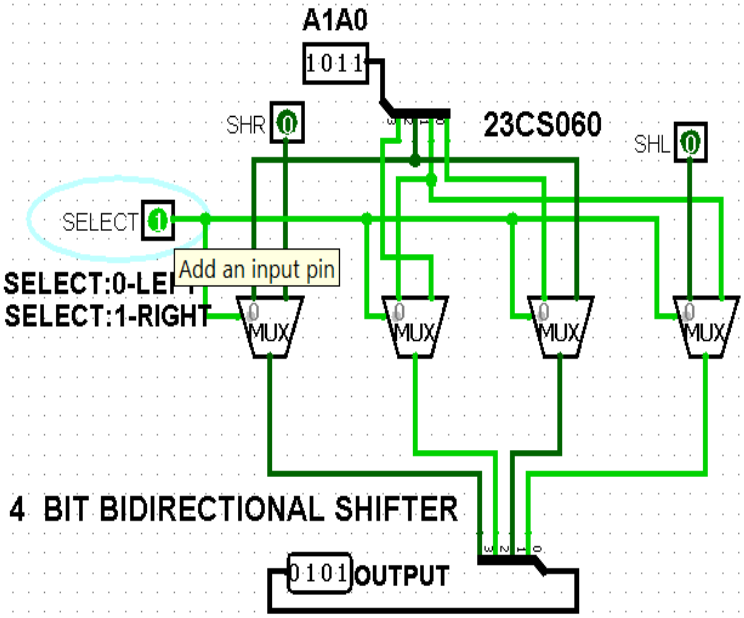

B1B0 10
A1A0 11
23CS060
2 BIT LOGICAL FUNCTION
1111 S3S2S1S0
11 E1E0
MUX

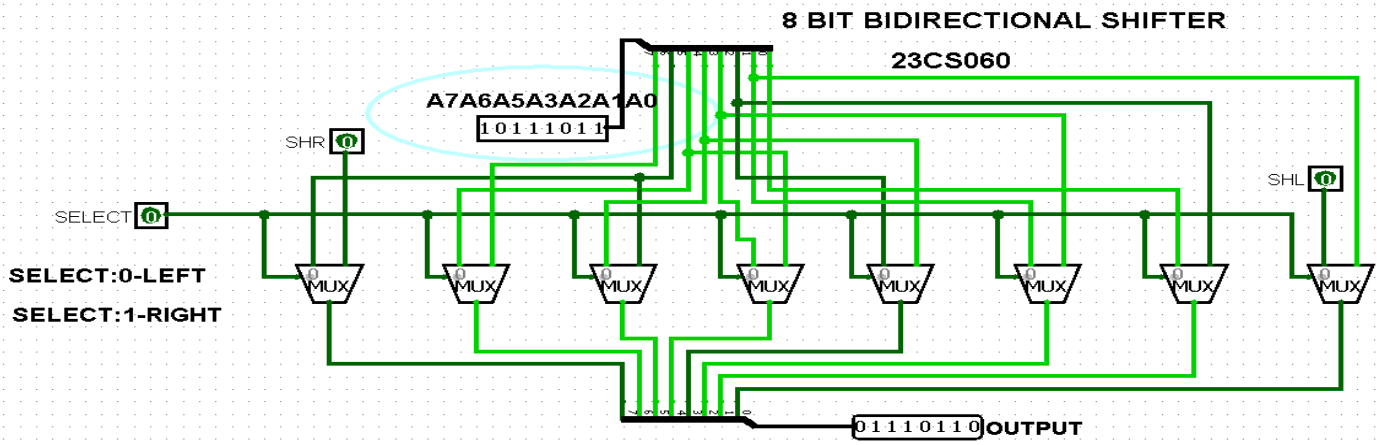

B1B0 10
A1A0 11
23CS060
2 BIT LOGICAL FUNCTION
0110 S3S2S1S0
01 E1E0
MUX

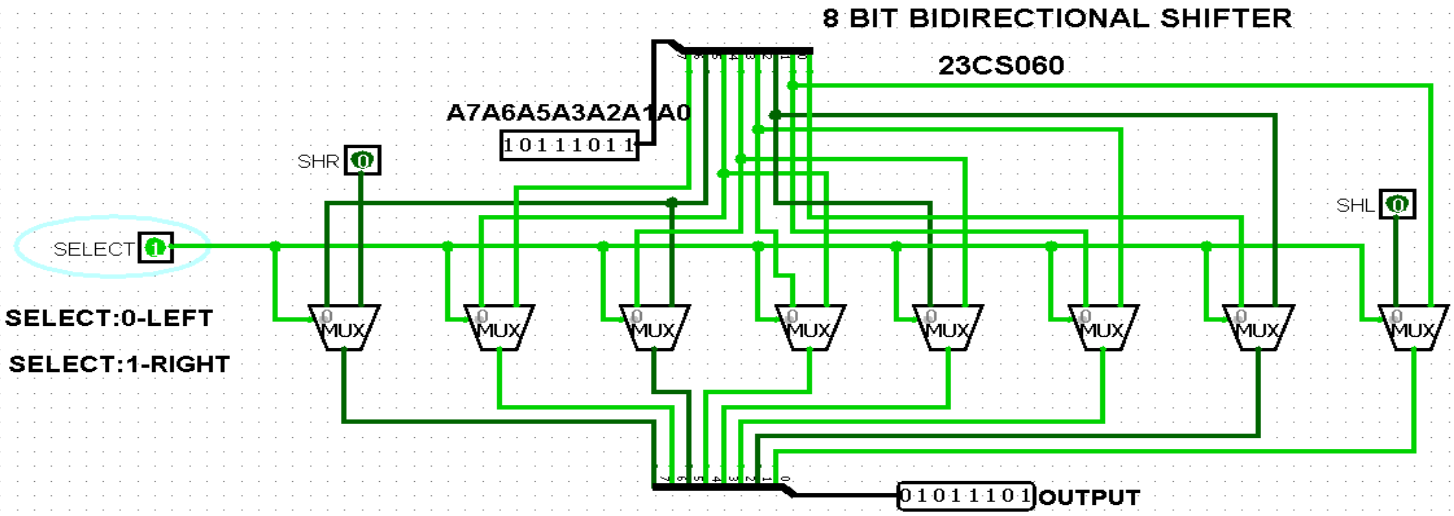

2 BIT BIDIRECTIONAL SHIFTER
A1A0
10
SHR 0
SHL 0
23CS060
SELECT
0
SELECT:0-LEFT
SELECT:1-RIGHT
MUX
MUX
00 OUTPUT

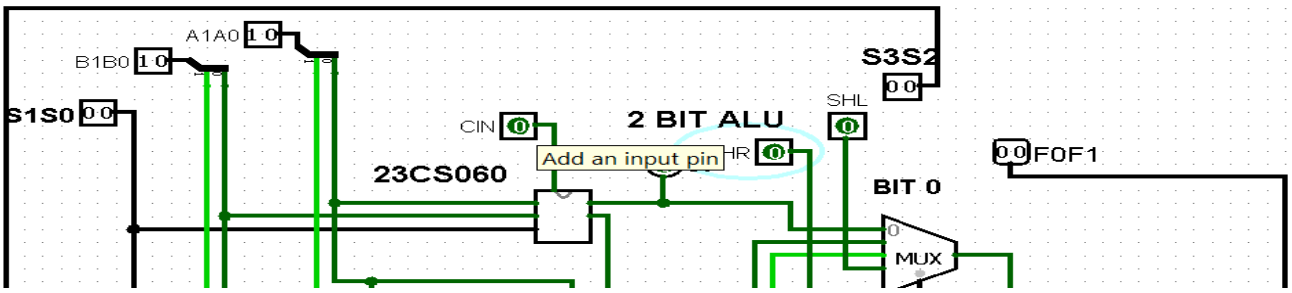

2 BIT BIDIRECTIONAL SHIFTER
A1A0
10
SHR 0
SHL 1
23CS060
SELECT
0
SELECT:0-LEFT
SELECT:1-RIGHT
MUX
MUX
01 OUTPUT

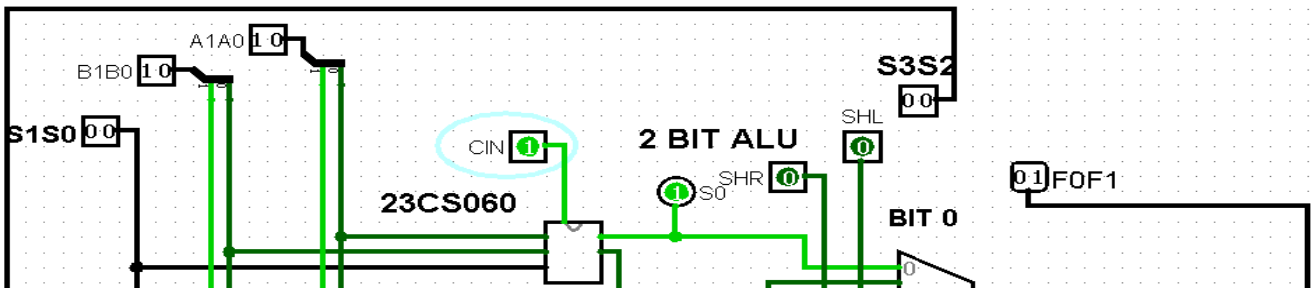

A1A0
1011
Add an input pin
SHR
SHL
SELECT
SELECT:0-LEFT
SELECT:1-RIGHT
MUX
4 BIT BIDIRECTIONAL SHIFTER
0110 OUTPUT

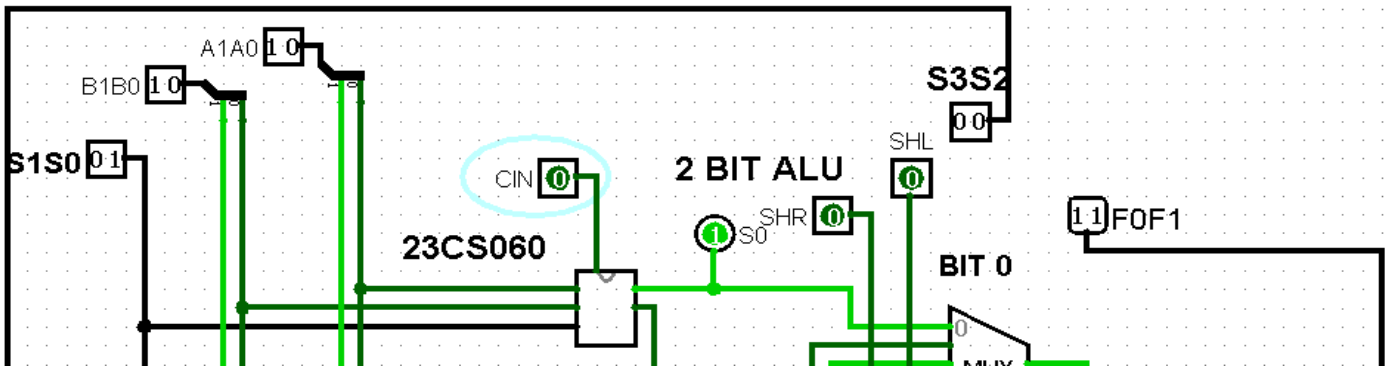

A1A0
1011
SHR
23CS060
SHL
SELECT
Add an input pin
SELECT:1-RIGHT
MUX
4 BIT BIDIRECTIONAL SHIFTER
0101 OUTPUT

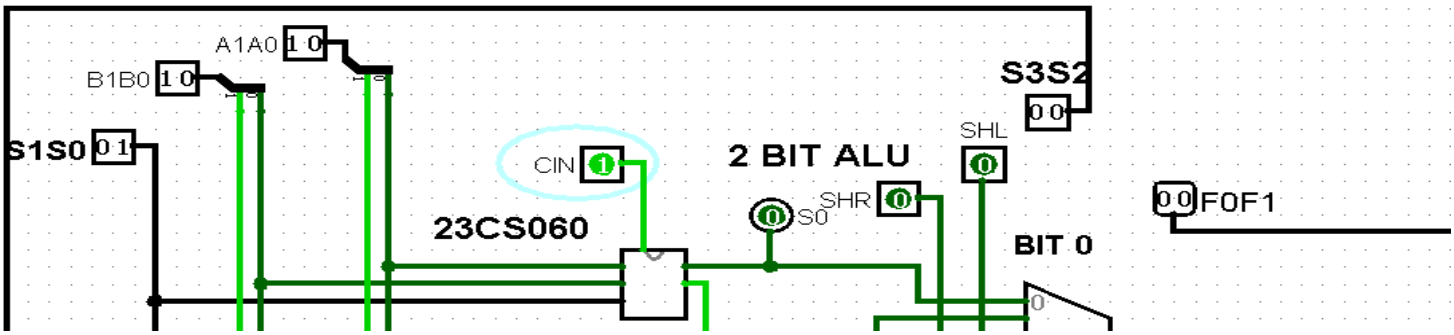

8 BIT BIDIRECTIONAL SHIFTER
23CS060
A7A6A5A3A2A1A0
10111011
SHR
SHL
SELECT
SELECT:0-LEFT
SELECT:1-RIGHT
MUX
01110110 OUTPUT

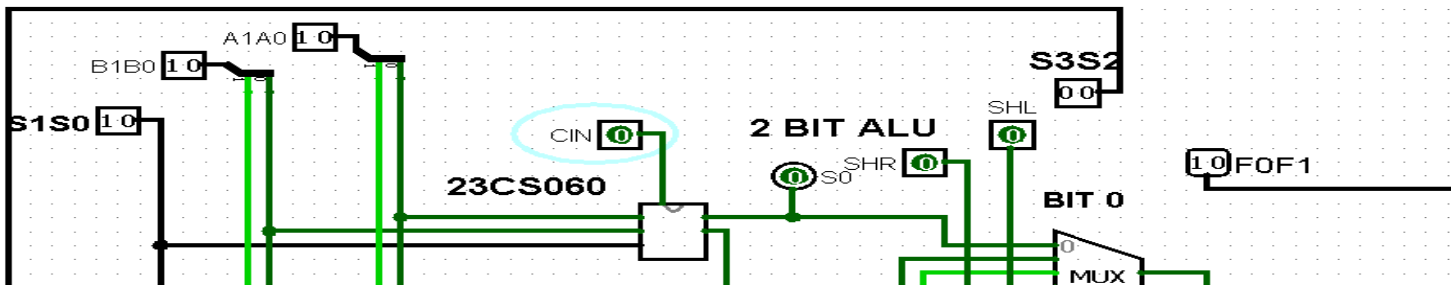

8 BIT BIDIRECTIONAL SHIFTER
23CS060
A7A6A5A3A2A1A0
10111011
SHR
SHL
SELECT
SELECT:0-LEFT
SELECT:1-RIGHT
MUX
01011101 OUTPUT

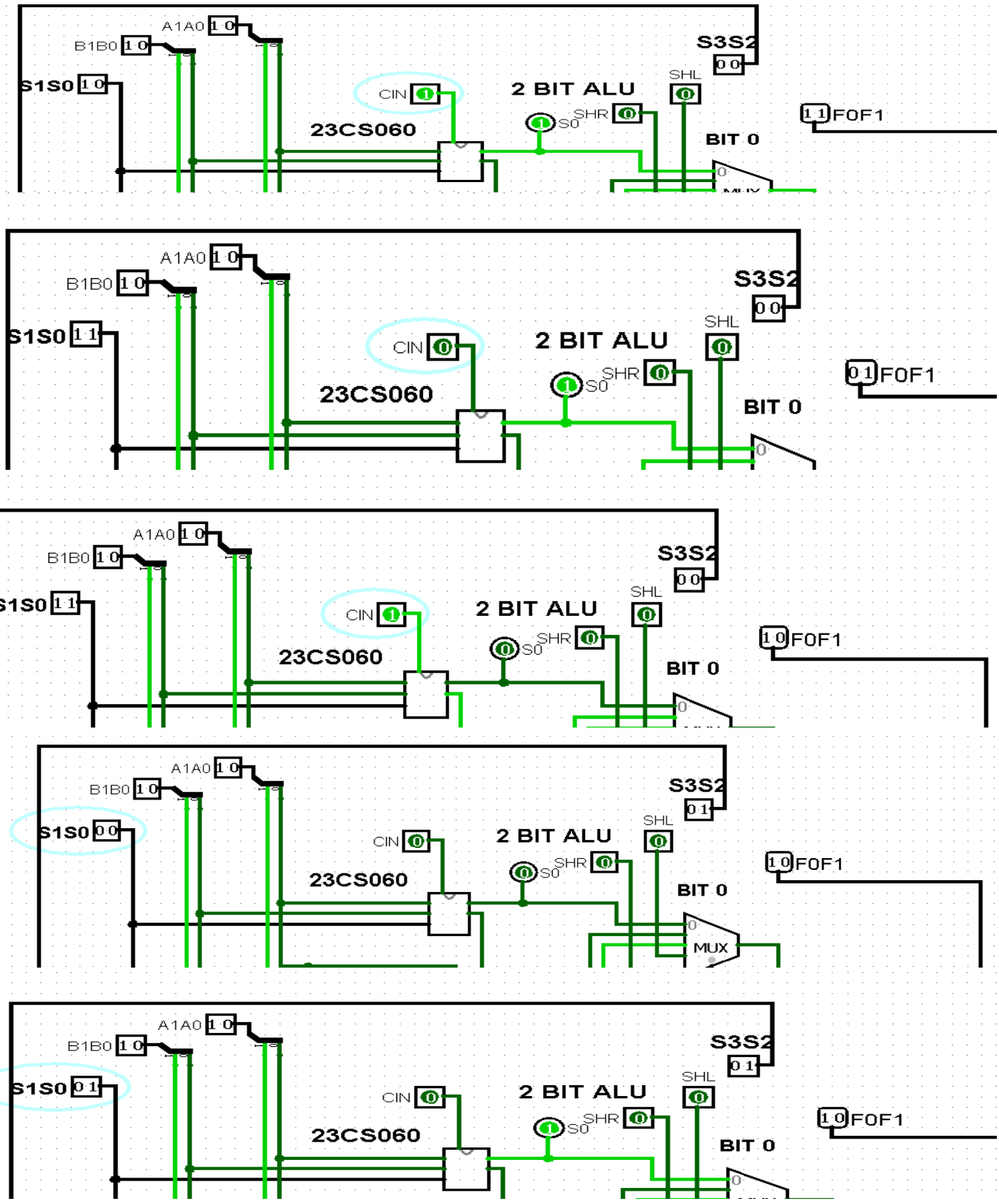

A1A0 1 0
B1B0 1 0
S1S0 0 0
CIN 0
2 BIT ALU
Add an input pin
SHR 0
SHL 0
S3S2 0 0
23CS060
BIT 0
MUX
0 0 F0F1

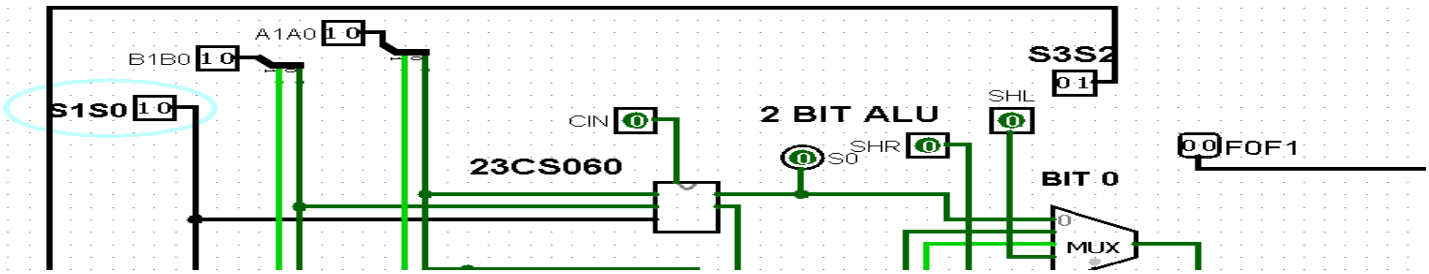

A1A0 1 0
B1B0 1 0
S1S0 0 0
CIN 1
2 BIT ALU
S0
SHR 0
SHL 0
S3S2 0 0
23CS060
BIT 0
0 1 F0F1

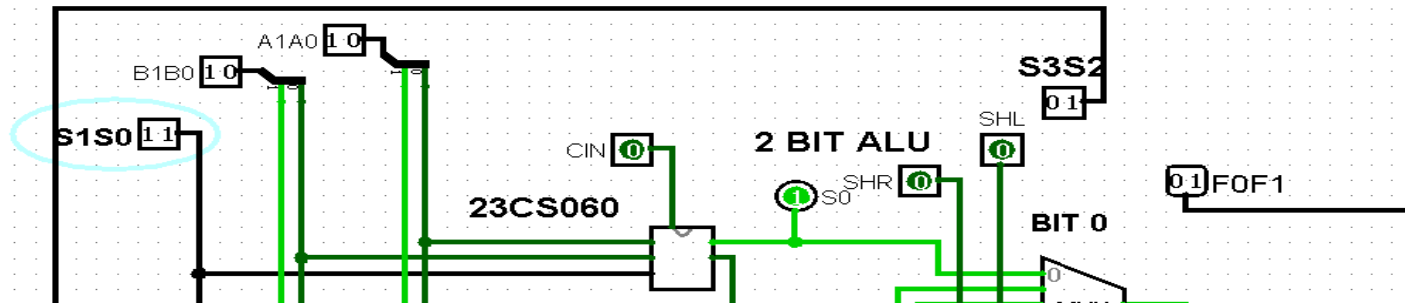

A1A0 1 0
B1B0 1 0
S1S0 0 1
CIN 0
2 BIT ALU
S0
SHR 0
SHL 0
S3S2 0 0
23CS060
BIT 0
1 1 F0F1

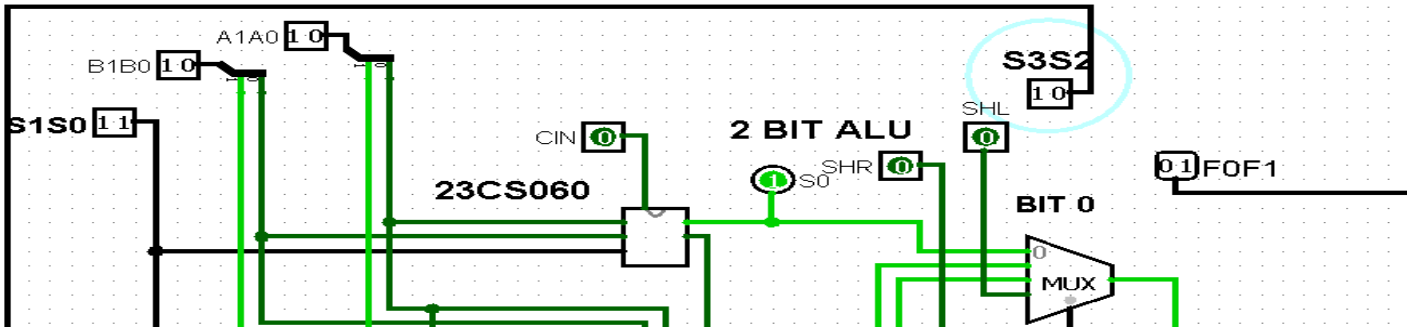

A1A0 1 0
B1B0 1 0
S1S0 0 1
CIN 1
2 BIT ALU
S0
SHR 0
SHL 0
S3S2 0 0
23CS060
BIT 0
0 0 F0F1

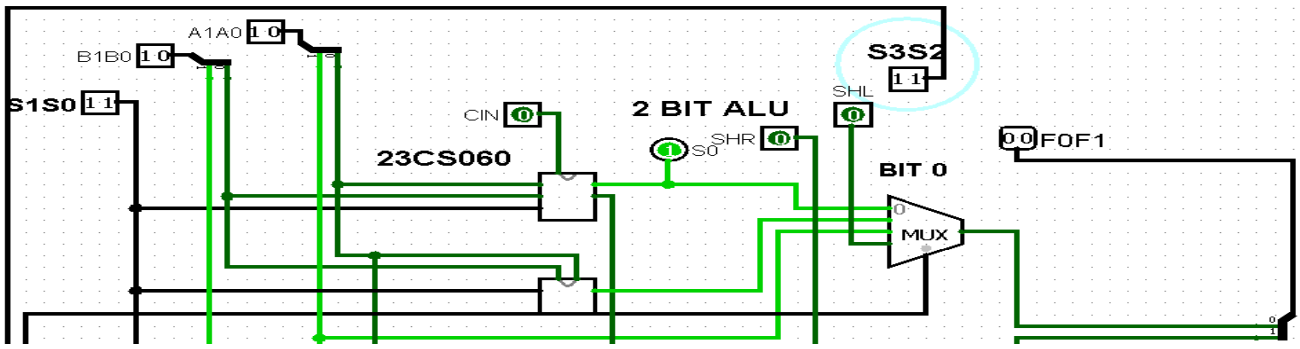

A1A0 1 0
B1B0 1 0
S1S0 1 0
CIN 0
2 BIT ALU
S0
SHR 0
SHL 0
S3S2 0 0
23CS060
BIT 0
MUX
1 0 F0F1

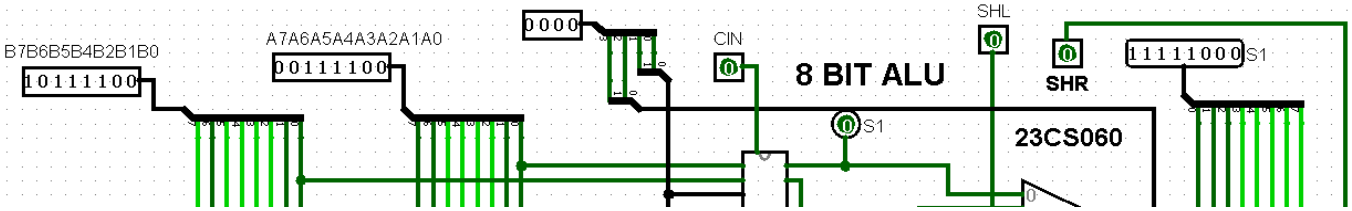

A1A0 1 0
B1B0 1 0
S1S0 1 0
CIN 1
23CS060
2 BIT ALU
S0
SHR 0
SHL 0
S3S2 0 0
BIT 0
0
MUX
1 1 FOF1
A1A0 1 0
B1B0 1 0
S1S0 1 1
CIN 0
23CS060
2 BIT ALU
S0
SHR 0
SHL 0
S3S2 0 0
BIT 0
0
0 1 FOF1
A1A0 1 0
B1B0 1 0
S1S0 1 1
CIN 1
23CS060
2 BIT ALU
S0
SHR 0
SHL 0
S3S2 0 0
BIT 0
0
1 0 FOF1
A1A0 1 0
B1B0 1 0
S1S0 0 0
CIN 0
23CS060
2 BIT ALU
S0
SHR 0
SHL 0
S3S2 0 1
BIT 0
0
MUX
1 0 FOF1
A1A0 1 0
B1B0 1 0
S1S0 0 1
CIN 0
23CS060
2 BIT ALU
S0
SHR 0
SHL 0
S3S2 0 1
BIT 0
0
1 0 FOF1

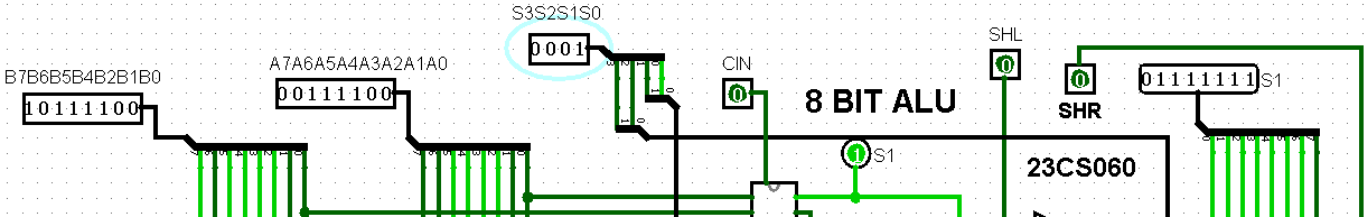

A1A0 1 0
B1B0 1 0
S1S0 1 0
CIN 0
2 BIT ALU
23CS060
S0
SHR 0
SHL 0
S3S2
0 1
BIT 0
MUX
0 0 FOF1

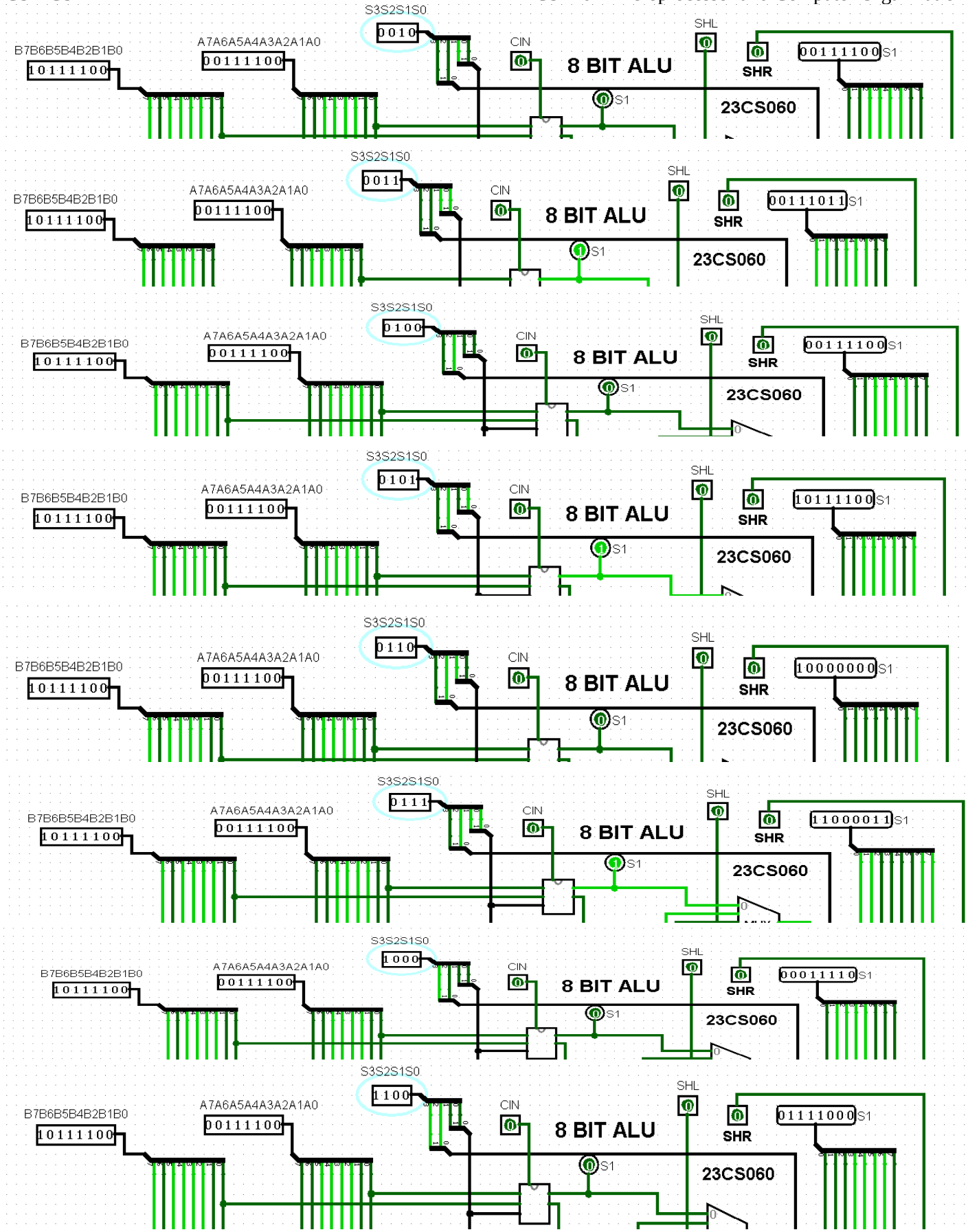

A1A0 1 0
B1B0 1 0
S1S0 1 1
CIN 0
2 BIT ALU
23CS060
S0
SHR 0
SHL 0
S3S2
0 1
BIT 0
0 1 FOF1

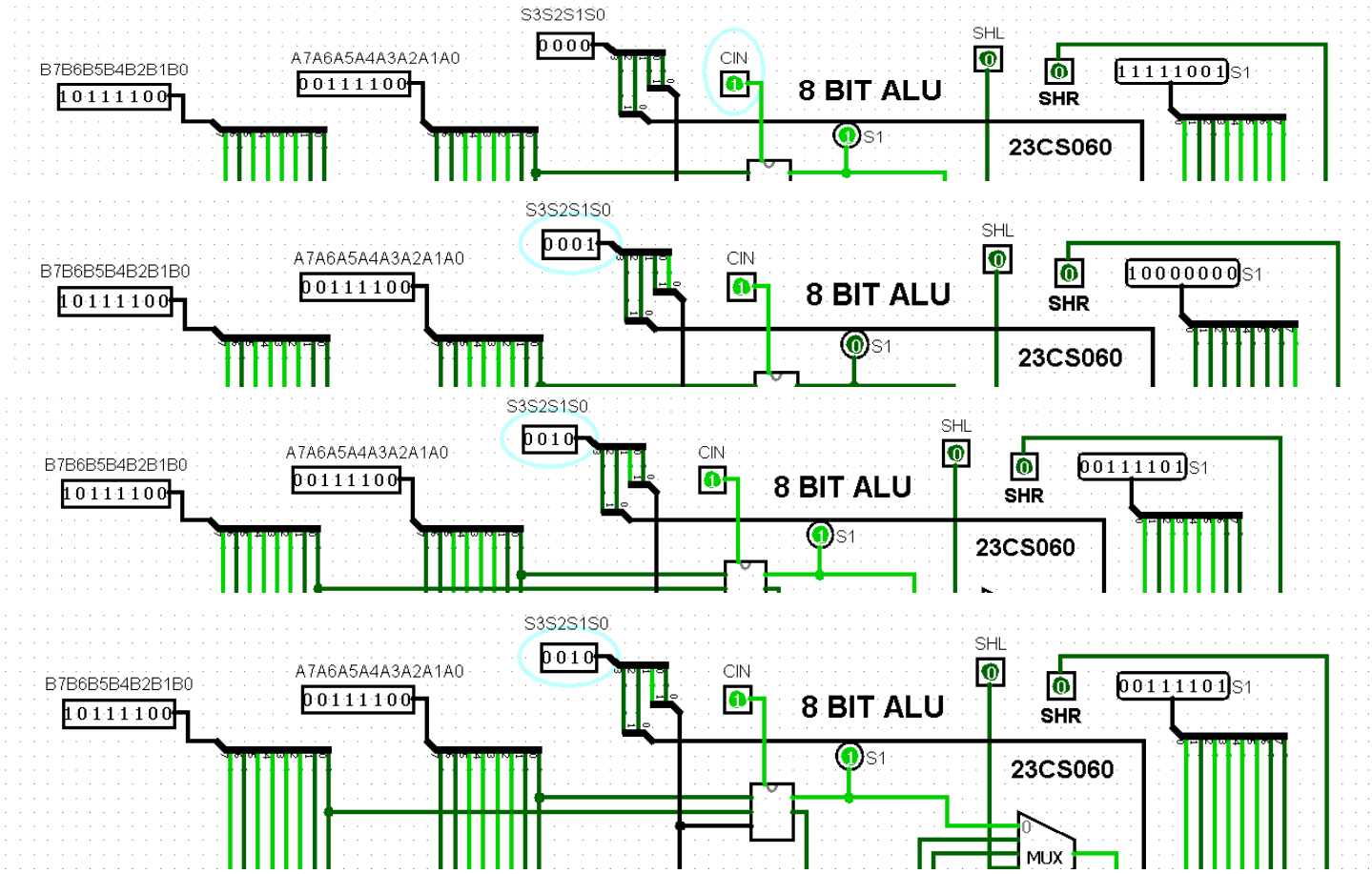

A1A0 1 0
B1B0 1 0
S1S0 1 1
CIN 0
2 BIT ALU
23CS060
S0
SHR 0
SHL 0
S3S2
1 0
BIT 0
MUX
0 1 FOF1


A1A0 1 0
B1B0 1 0
S1S0 1 1
CIN 0
2 BIT ALU
23CS060
S0
SHR 0
SHL 0
S3S2
1 1
BIT 0
MUX
0 0 FOF1


B7B6B5B4B2B1B0
1 0 1 1 1 1 0 0
A7A6A5A4A3A2A1A0
0 0 1 1 1 1 0 0
0 0 0 0
CIN 0
8 BIT ALU
23CS060
S1
SHR 0
SHL 0
1 1 1 1 1 0 0 0 S1


S3S2S1S0
0 0 0 1
B7B6B5B4B2B1B0
1 0 1 1 1 1 0 0
A7A6A5A4A3A2A1A0
0 0 1 1 1 1 0 0
CIN 0
8 BIT ALU
23CS060
S1
SHR 0
SHL 0
0 1 1 1 1 1 1 1 S1


S3S2S1S0
0010
B7B6B5B4B2B1B0
10111100
A7A6A5A4A3A2A1A0
00111100
CIN
8 BIT ALU
SHL
SHR
S1
23CS060
00111100S1
S3S2S1S0
0011
00111011S1
S3S2S1S0
0100
00111100S1
S3S2S1S0
0101
10111100S1
S3S2S1S0
0110
10000000S1
S3S2S1S0
0111
11000011S1
S3S2S1S0
1000
00011110S1
S3S2S1S0
1100
01111000S1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8 BIT ALU
S1
SHL
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23CS060
11111001 S1
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SHL
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S1
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8 BIT ALU
S1
SHL
SHR
23CS060
00111101 S1
0
MUX

Conclusion: