PRELIMINARY DATA SHEET

Revision: 0.1

Release date: 02 Feb 2017

RDA5995 WLAN SOC

Supports USB2.0 & SDIO for Connecting WLAN Activity to the host processor

1. General Description

RDA5995 is a low power MCU with IEEE802.11b/g/n MAC/PHY/radio integrated into one chip. TCP/IP protocols along with SSL are included, providing improved link robustness, extended range, and increased performance. For the highest integration level, the required board space has been minimized and customer cost has been reduced. Manufacturers can easily and fast integrate RDA5995 on their product to enable a rapid time to market.

RDA5995 supports generic interfaces including USB and SDIO for connecting WLAN activity to the host processor.

RDA5995 uses a compact 5×5mm² QFN package, 0.4mm pitch QFN-40.

1.1 WLAN Features

- CMOS single-chip fully-integrated radio, PHY and MAC
- 2.4GHz IEEE 802.11b/g/n
- Internal PA, LNA
- Data rates up to 150Mbps with 20/40 MHz bandwidth
- Dynamic TX power saving
- Low power listen mode
- Fast AGC control
- Support WPS,WMM
- Support WPA, WPA2,WEP,TKIP,CCMP
- Support STA, softAP, P2P, STA+softAp, STA+P2P
- Support A-MPDU,A-MSDU, HT-BA
- Light Weight TCP/IP protocol

1.2 MCU Features

- Integrated ARM-CM4 MCU
- Integrated MPU and mbed uvisor supported to isolate security domains
- Up to 448KBytes internal sram for WIFI protocol and application developments
- SDIO/SPI/UART/USB2.0 interface allows simple interfacing to host device
- UART with an AT command set
- Integrated hardware crypto accelerator AES/RSA
- Integrated True Random Number Generator(TRNG) and CRC accelerator
- Support external psram interface
- Integrated SPI flash in package, from 8Mbit to 64Mbit flash supported with internal cache for XIP(execute in place) and quick access.
- Integrated a bunch of configurable GPIOs with external level/edge trigger/wakeup
- Integrated UART×2/I2S×2/I2C×1/PWM×8/SPI×4/SDMMC×1/USB2.0×1
- Integrated 2 channels application ADC
- Integrated low power timer and watchdog
- 16×16 bits eFuse configuration
- Support freeRTOS/mbedOS5.1

1.3 Applications

- IoT device
- Mobile handset
- Wi-Fi dongle

2. Block Description

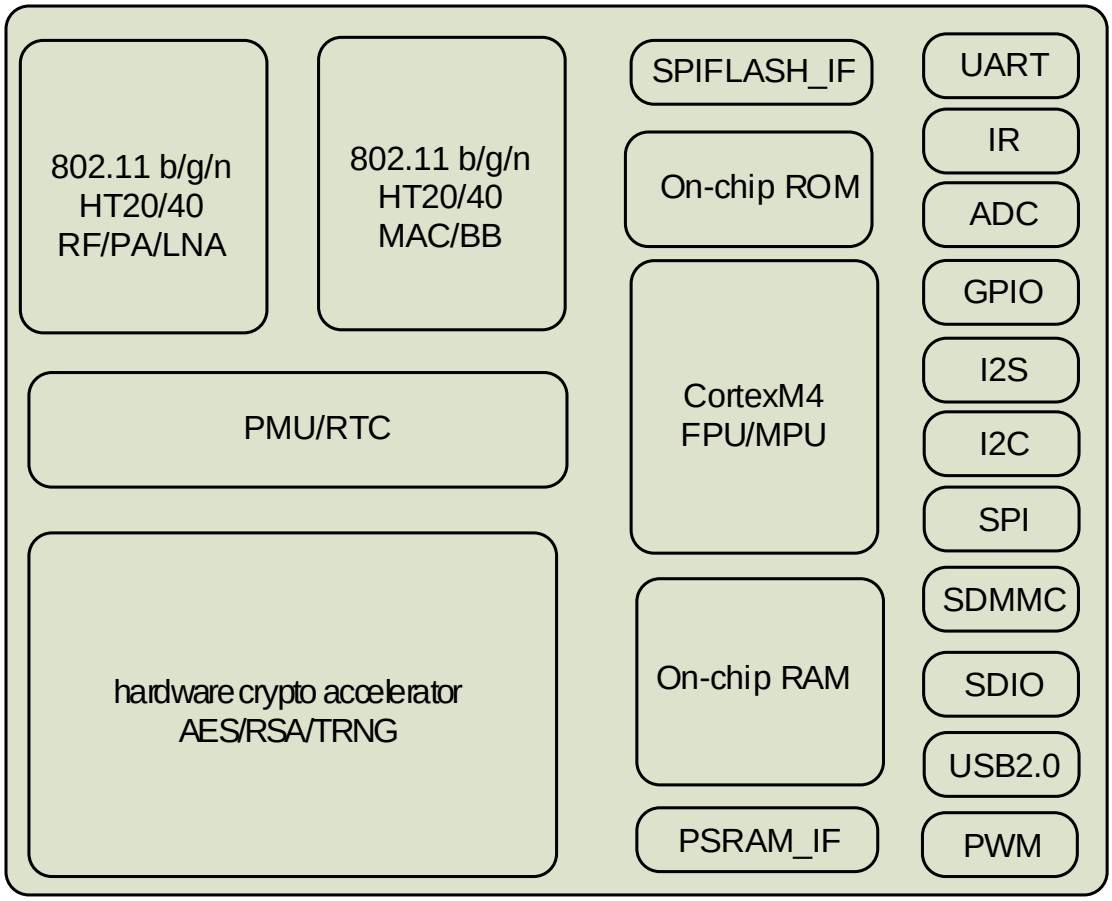


Figure2-1 RDA5995 Block Diagram

RDA5995 is a highly integrated IEEE 802.11n MCU Wi-Fi chip. RDA5995 supports USB 2.0 interface and SDIO interface for connecting WLAN activity to the host processor.

3. Functional Description

3.1 Memory System

RDA5995 integrates ROM, internal RAM, external flash and psram to provide applications with a variety of memory requirements.

▪ 3.1.1 Memory Map

Table 3-1 RDA5995 Memory Map

component	AddressRange	Size	comments
MEMORY			
Boot_ROM	**0x0000_0000-0x0000_FFFF**	**64K**	
I_SRAM	**0x0010_0000-0x0011_FFFF**	**128K**	
D_SRAM	**0x0018_0000-0x0019_7FFF**	**160K**	
PSRAM	**0x1000_0000-0x13FF_EFFF data**	**64M**	
FLASH	**0x1400_0000-0x17FF_EFFF FLASH data**	**64M**	
I-cache	**0x1800_0000-0x1FFF_FFFF I-cache**		
LOGIC			
SCU	**0x40000000-0x40000FFF**	**4K**	
GPIO	**0x40001000-0x40001FFF**	**4K**	
TIMER	**0x40002000-0x40002FFF**	**4K**	
I2C_master	**0x40003000-0x40003FFF**	**4K**	
PWM	**0x40004000-0x40004FFF**	**4K**	
PSRAM_CFG	**0x40005000-0x40005FFF**	**4K**	
SDMMC	**0x40006000-0x40006FFF**	**4K**	
I2C	**0x40010000-0x40010FFF**	**4K**	
UART1	**0x40012000-0x40012FFF**	**4K**	
AHB_EXIF	**0x40013000-0x40013FFF**	**4K**	
WIFI_PA	**0x40020000-0x40021FFF**	**8K**	
WIFI_CE	**0x40022000-0x40022FFF**	**4K**	
WLAN_MON	**0x40024000-0x40027FFF**	**20K**	
SDIO	**0x40030000-0x40030FFF**	**4K**	
USB	**0x40031000-0x40031FFF**	**4K**	
MEMC0	**0x40100000-0x4017FFFF**	**512k**	

UART2	**0x40180000-0x40180FFF**	**4K**	
DMA_CFG	**0x40181000-0x40181FFF**	**4K**	

- **3.1.2 Internal ROM**

  RDA5995 integrates internal ROM to provide basic functions:
  - eFuse functions
  - USB/SDIO/SPI interface initialization
  - MCU/Wi-Fi mode initialization

- **3.1.2 Internal RAM**

  RDA5995 integrates:
  - 448K Bytes SRAM
  - 32K Bytes icache

- **3.1.3 SPI Nor FLASH**

RDA5995 supports standard SPI mode and SPI-Quad mode. It supports up to 64M bits of flash.

3.2 GPIO Characteristics

Table 3-12 GPIO Configurable Function Summary Table

pad name	func0	func1	func2	func3	func4	func5	func7	
uart_rx	uart_rx	gpio_26		spi_cs_ex_2	pw_pwl0			pull up
uart_tx	uart_tx	gpio_27	intf_uart_rx	spi_cs_ex_3	pw3			pull down
sdio_intn	gpio_0	wifi_wakeup		sdmmc_cmd	pw2			pull down
agpio_0	gpio_1	ntrst		i2s_out_sd	pw_pwl1	uart2_rx	bt_prio	pull up
gpio_2	gpio_2	i2c_sda		i2s_out_ws	pw_lpg	uart2_tx	bt_state	pull up
gpio_3	gpio_3	i2c_sclk		i2s_out_bclk	pw_pwt	sdmmc_d_0	bt_freq	pull up
gpio_4	gpio_4	tms		i2s_in_sd	spi_clk_ex		wl_actvie	pull down
gpio_5	gpio_5	tck		i2s_in_ws	spi_cs_ex_1			pull down
gpadc0	gpio_6	intf_uart_rx		spi_mosi_ex	dm_psram	spi_data_ex	sdmmc_d_0	pull down
gpadc1	gpio_7	trigger_bit		spi_miso_ex	clk_psram	sdmmc_d_1		pull down
clk_req	gpio_8	tdo		i2s_in_bclk(spi_r	pw0			pull down
xin_32k	gpio_9	tdi		sdmmc_clk	clkb_psram			pull down
usb_dp	gpio_10	spi_cs1		-	-	-		pull up
usb_dn	gpio_11			-	-	-		pull up
i2c_scl	scl_sl1	gpio_12		sdmmc_d_2	dqs_psram	-		pull down
i2c_sda	sda_sl1	gpio_13		sdmmc_d_3	cs_psram	pw1		pull down
gpio_22	gpio_22	spi_clk_ex	ctsn_uart2	i2c_sda	pwm0			pull down
gpio_23	gpio_23	spi_cs_ex	rtsn_uart2	i2c_scl	pwm1			pull down
gpio_24	gpio_24	spi_mosi_ex	uart2_rx	spi_data_ex	pwm2			pull down
gpio_25	gpio_25	spi_miso_ex	uart2_tx		pwm3			pull down

3.3 UART Interface Characteristics

RDA5995 supports 2 UARTs with configurable baud rate from 1200bps to 4Mbps.

3.4 I2S Interface Characteristics

RDA5995 supports 2 I2S interface; the I2S master BCLK supports 96/192/384/512/ 44.1/88.2KHz. The interface supports 16/32 bit per channel, the data format can be configured as 16/20/24bit per channel or decided by software(up to 24bit per channel).

3.5 I2C Interface Characteristics

RDA5995 supports 1 I2C standard interface. It supports master or slave I2C operation and 3 standard speed mode:

1. Standard mode(<100Kb/s)
2. Fast mode(<400Kb/s)
3. High-speed mode (<3.4Mb/s)

3.6 PWM Interface Characteristics

RDA5995 supports 8 PWM interfaces. Period and Duty of PWM is programmable. The Duty of PWM/PWT/PWL can be flexible configured between 0~100. The accurate of duty is 1%.The period are programmable, the software can select different clock to product long Period.

Name	Number	Duty	Period	
PWM	4	1~100%	5us-256s	Standard PWM
PWT	1	1~100%	5us-4s	Standard PWM
LPG	1	<25%	<2s	The wave has a short pull up in a long period
PWL	2	1~100%	-	The wave is non-periodic, use for screen background light

Table 3-2 PWM Period & Duty

3.7 SPI Interface Characteristics

RDA5995 supports 4 SPI interfaces, master only. The SPI clock rate are programmable and up to 20MHz. The data length can be configure by the software, the max data length is 64bit.

3.8 SDMMC Interface Characteristics

RDA5995 supports 1 SDMMC interface.

3.9 USB Interface Characteristics

RDA5995 supports USB2.0 interface.

4. WLAN Section Electrical Characteristics

Table 4-1 DC Electrical Specification (Recommended Operation Conditions):

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
VBAT	Supply Voltage from battery or LDO	3.3	4.0	5.0	V
T_{amb}	Ambient Temperature	-20	27	+50	℃
V_{IL}	CMOS Low Level Input Voltage	0		0.3*VIO	V
V_{IH}	CMOS High Level Input Voltage	0.7*VIO		VIO	V
V_{TH}	CMOS Threshold Voltage		0.5*VIO		V

Table 4-2 DC Electrical Specification (Absolute Maximum Ratings):

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{amb}	Ambient Temperature	-20		+50	℃
I_{IN}	Input Current	-10		+10	mA
V_{IN}	Input Voltage	-0.3		VIO+0.3	V
V_{lna}	LNA Input Level			+10	dBm

5. PINS Description

Table 5-1 Pin Types

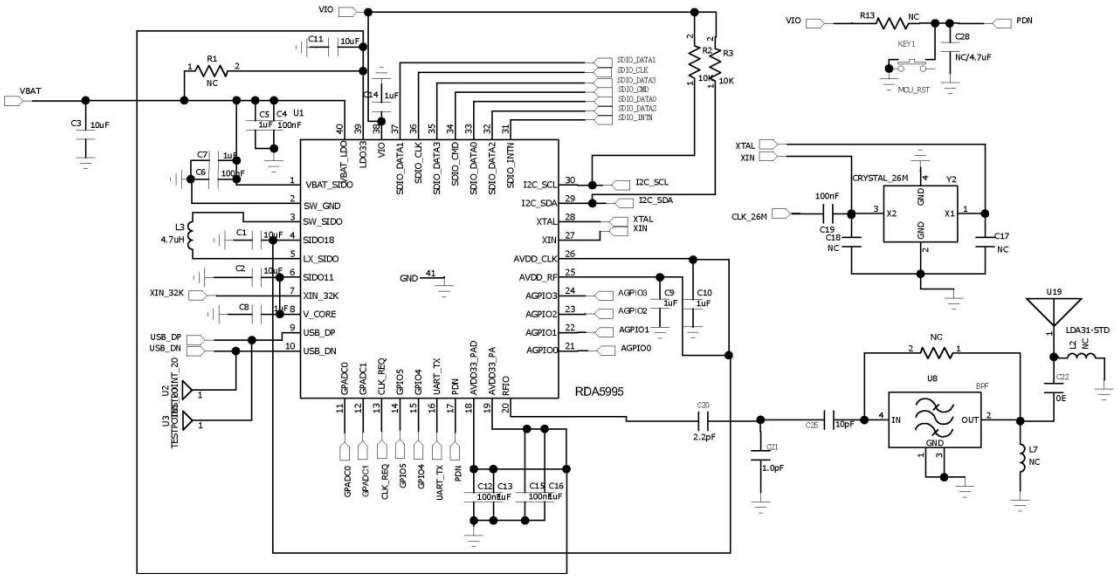
Pin Type	Description
I/O	Digital input/output
I	Digital input
O	Digital output
A,I	Analog input
A,O	Analog output
A,I/O	Analog input/output
PWR	Power
GND	Ground

Table 5-2 RDA5995 Pins Description

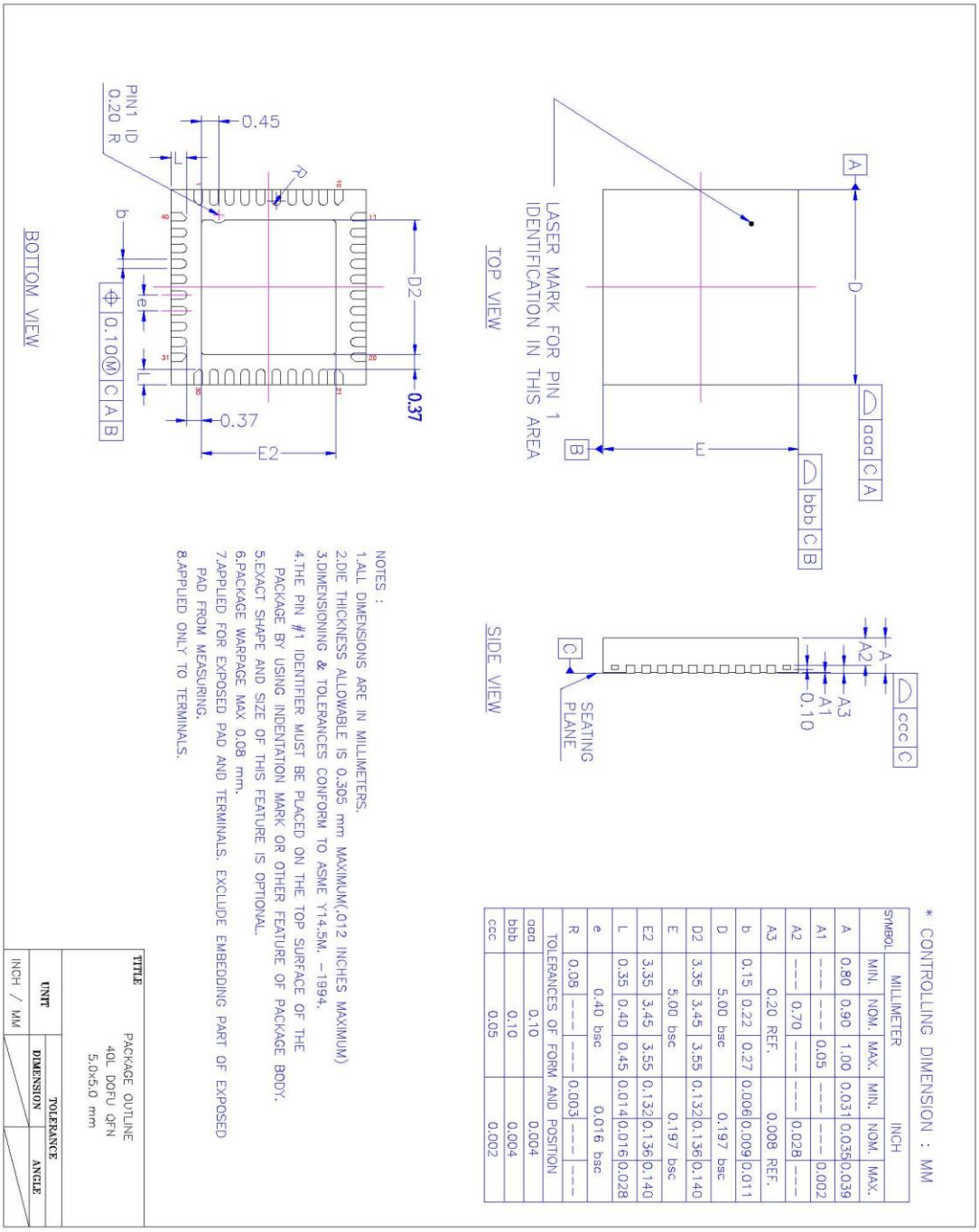
PIN	NO.	Type	DESCRIPTION
VBAT_SIDO	1	PWR	buck power supply
SW_GND	2	GND	buck ground
SW_SIDO	3	PWR	Switching node of buck
SIDO18	4	PWR	1.8V power output
LX_SIDO	5	PWR	Switching output
SIDO11	6	PWR	1.1V power output
XIN_32K	7	I/O	gpio_9/tdi/tdi/sdmmc_clk/clkb_psram
V_CORE	8	PWR	Digital core power in
USB_DP	9	A,I/O or I/O	USB positive input/gpio_10/spi_cs 1
USB_DN	10	A,I/O or I/O	USB negative output/gpio_11
GPADC0	11	I/O	gpio6/intf_uart_rx /spi_mosi_ex/dm_psram/spi_data_ex /sdmmc_d_0
GPADC1	12	I/O	gpio7/trigger_bit/spi_miso_ex/clk_psram/sdmmc_d_1
CLK_REQ	13	I/O	gpio8/tdo/i2s_in_bclk(spi_miso)/pw0
GPIO5	14	I/O	gpio_5/tck /i2s_in_ws/spi_cs_ex_1
GPIO4	15	I/O	gpio_4/tmsi2s_in_sd/spi_clk_ex/bist_tckwl_active
UART_TX	16	I/O	gpio_27/intf_uart_rx/spi_cs_ex_3/pw3
PDN	17	I	Reset signal of the chip
AVDD33_PAD	18	PWR	3.3V PA driver power in
AVDD33_PA	19	PWR	3.3V PA power in
RFIO	20	A,I/O	wifi transmitter output/receiver input
AGPIO0	21	I/O	gpio_1/ntrst /i2s_out_sd/pw_pwl1/uart2_rx/bt_prio
AGPIO1	22	I/O	gpio_2/i2c_sda/i2s_out_ws/pw_lpg_uart2_tx/bt_state
AGPIO2	23	I/O	gpio_3/i2c_sclk/i2s_out_bclk/pw_pwt/sdmmc_d_0/bt_freq
AGPIO3	24	I/O	Uart_rx/gpio_26/spi_cs_ex-2/pw_pwl0
AVDD_RF	25	PWR	1.8V RF power in
AVDD_CLK	26	PWR	1.8V clock power in
XIN	27	A,I	26M crystal input
XTAL	28	A,O	26M crystal output
I2C_SDA	29	I/O	gpi0_13/sda_sl/sdmmc_d_3/cs_psram/pw1
I2C_SCL	30	I/O	gpio_12/scl_sl1/ sdmmc_d_2/dqs_psram

SDIO_INIT	31	I/O	gpio_0/wifi_wakeup/ sdmmc_cmd/pw2
SDIO_D2	32	I/O	sdio_data_2/gpio_18/txon_test/spi_s2/sdmmc_d_2
SDIO_D0	33	I/O	sdio_data_0/gpio_16/agc_test_2/spi_s0/sdmmc_d_0
SDIO_CMD	34	I/O	sdio_cmd/gpio_15/agc_test_1/spi_cs0/sdmmc_cmd
SDIO_D3	35	I/O	sdio_data_3/gpio_19/rxon_test/spi_s3/sdmmc_d_3_
SDIO_CLK	36	I/O	sdio_clk/gpio_14/agc_test_0/spi_clk/sdmmc_clk
SDIO_D1	37	I/O	sdio_data_1/gpio_17/agc_test_3/spi_s1/sdmmc_d_1
VIO	38	PWR	I/O power supply and LDO power out (option)
LDO33	39	PWR	3.3V LDO output and USB power supply
VBAT_LDO	40	PWR	3.3V LDO and internal Vrtc power supply

6. Application Circuit



7. Package Physical Dimension



SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	----	----	0.05	----	----	0.002
A2	----	0.70	----	----	0.028	----
A3		0.20 REF.			0.008 REF.	
b	0.15	0.22	0.27	0.006	0.009	0.011
D		5.00 bsc			0.197 bsc	
D2	3.35	3.45	3.55	0.132	0.136	0.140
E		5.00 bsc			0.197 bsc	
E2	3.35	3.45	3.55	0.132	0.136	0.140
L	0.35	0.40	0.45	0.014	0.016	0.028
e		0.40 bsc			0.016 bsc	
R	0.08	----	0.003	----	----	
TOLERANCES OF FORM AND POSITION						
aaa		0.10			0.004	
bbb		0.10			0.004	
ccc		0.05			0.002	

8. Recommended Reflow Profile

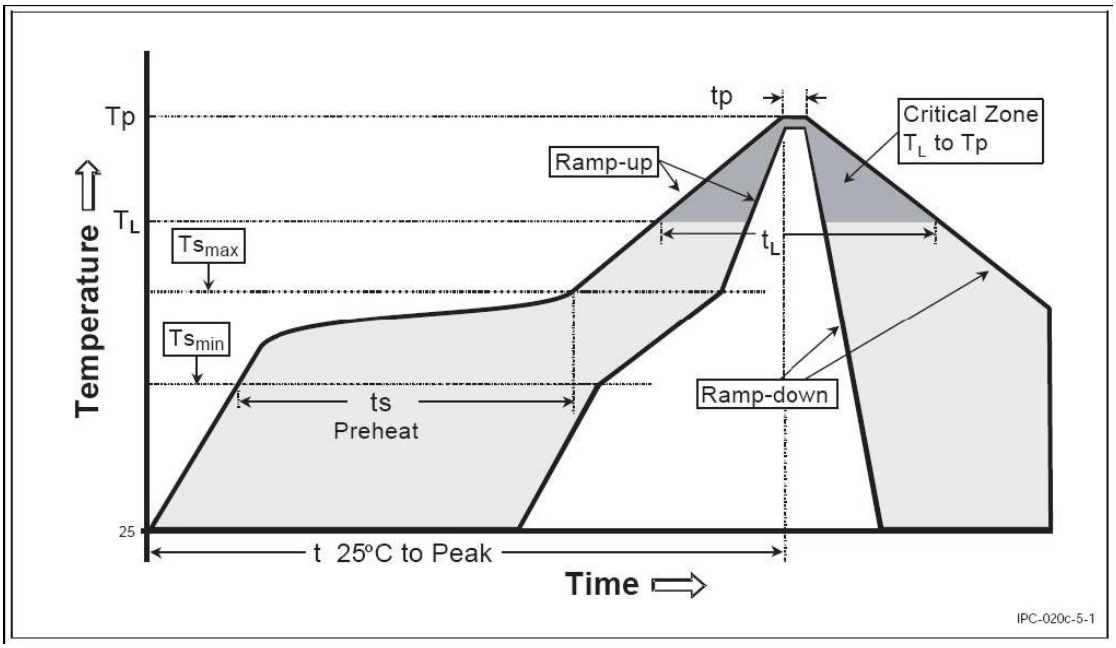


Figure.8-1 Classification Reflow Profile

Table 8-1 Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (TSmax to Tp)	3 ℃/second max.	3 ℃/second max.
Preheat -Temperature Min (Tsmin) -Temperature Max (Tsmax) -Time (tsmin to tsmax)	 100 ℃ 100 ℃ 60-120 seconds	 150 ℃ 200 ℃ 60-180 seconds
Time maintained above: -Temperature (TL) -Time (tL)	 183 ℃ 60-150seconds	 217℃ 60-150 seconds
Peak /Classification Temperature(Tp)	See Table 11-2	See Table 11-3
Time within 5 oC of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 ℃/second max.	6 ℃/seconds max.
Time 25 oC to Peak Temperature	6 minutes max.	8 minutes max.

Table 8-2 Sn-Pb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm3 <350	Volume mm3 ≥350
＜2.5mm	240 + 0/-5 ℃	225 + 0/-5 ℃
≥2.5mm	225 + 0/-5 ℃	225 + 0/-5 ℃

Table 8-3 Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm3 ＜350	Volume mm3 350-2000	Volume mm3 ＞2000
＜1.6mm	260 + 0 ℃ *	260 + 0 ℃ *	260 + 0 ℃ *
1.6mm – 2.5mm	260 + 0 ℃ *	250 + 0 ℃ *	245 + 0 ℃ *
≥2.5mm	250 + 0 ℃ *	245 + 0 ℃ *	245 + 0 ℃ *
*Tolerance : The device manufacturer/supplier shall assure process compatibility up to and including the stated classification temperature(this mean Peak reflow temperature + 0 ℃. For example 260+ 0 ℃) at the rated MSL Level.			

Note 1: All temperature refer topside of the package. Measured on the package body surface.

Note 2: The profiling tolerance is + 0 ℃, - X ℃ (based on machine variation capability)whatever is required to control the profile process but at no time will it exceed – 5 ℃. The producer assures process compatibility at the peak reflow profile temperatures defined in Table 8-3.

Note 3: Package volume excludes external terminals(balls, bumps, lands, leads) and/or non integral heat sinks.

Note 4: The maximum component temperature reached during reflow depends on package the thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD package maysill exist.

Note 5: Components intended for use in a “lead-free” assembly process shall be evaluated using the “lead free” classification temperatures and profiles defined in Table8-1, 8-2, 8-3 whether or not lead free.

9. Change List

The following table summarizes revisions to this document.

REV	DATE	AUTHER	CHANGE DESCRIPTION
V0.1			
V1.1			

10. RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominateddiphenyl ethers (PBDE), and are therefore considered RoHS compliant.

11. ESD Precautions

ESD protection circuitry is contended in this device, but special handling precautions are required.

12. Disclaimer

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