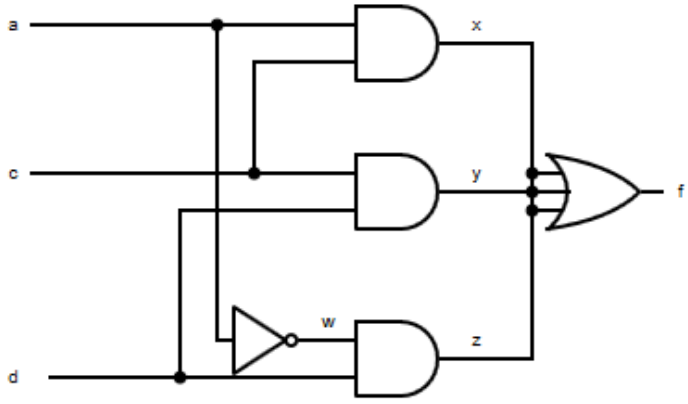
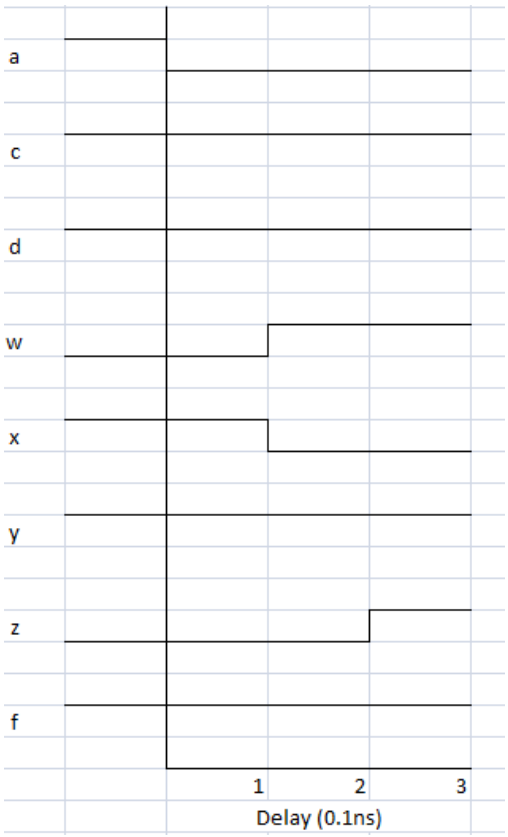
Austin Smothers
Professor Bustamante
CSC 137

Assignment 3

2.21 The prime implicants for $f(a, b, c, d) = \Sigma(1, 3, 5, 7, 10, 11, 14, 15)$ are $\bar{a}d + ac$ and cd. The timing diagram for its minimal expression $f = \bar{a}d + ac$ is shown in Fig. 2.25. Draw the circuit for the non-minimal $f = \bar{a}d + ac + cd$ which includes all its prime implicants, and label its internal signals. Draw a timing diagram for the new circuit when its input change from $acd = 111$ to $acd = 011$. Does the circuit produce a glitch?

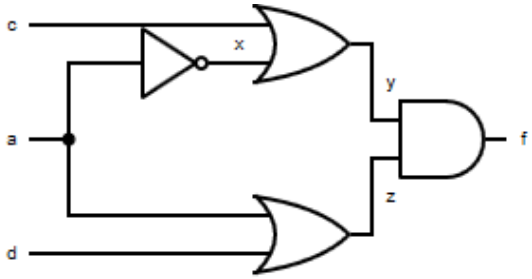


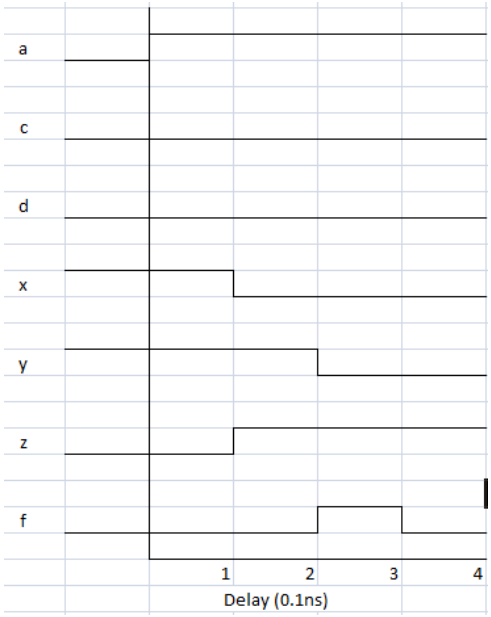


There is no glitch because the y circuit stays "on" the entire time (since c and d don't change values). The result is that f is always "on".

2.22 The minimal POS expression for $f(a, b, c, d) = (0, 2, 4, 6, 8, 9, 12, 13)$ has two essential prime implicants $(a + d)$ and $(\bar{a} + c)$ and a non-essential prime implicant $(c + d)$.

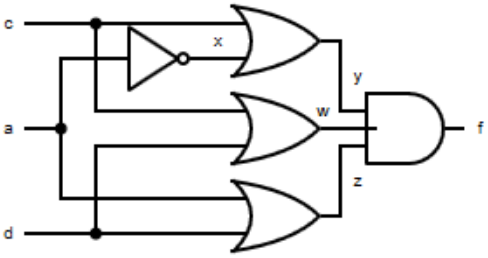
a. Draw a timing for minimal $f = (a + d)(\bar{a} + c)$ when its inputs change from $acd = 000$ to $acd = 100$. Does the circuit produce a glitch?

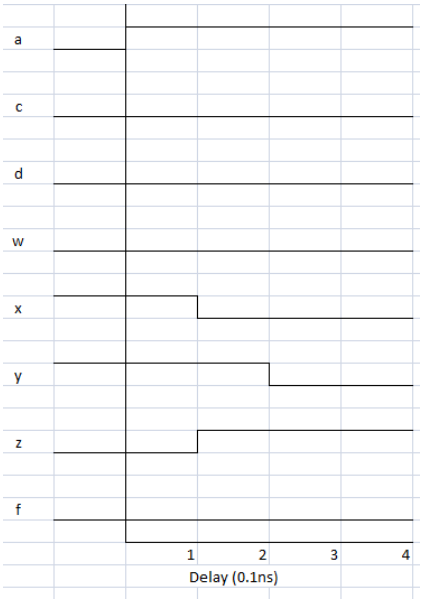




Yes there is a 0-hazard glitch, as y and z both briefly become 1, causing f to flip. Then y registers as 0, and f becomes 0, causing a glitch.

b. Draw a timing for the non-minimal $f = (a + d)(\bar{a} + c)(c + d)$ when its inputs change from $acd = 000$ to $acd = 100$. Note f includes all its prime implicants. Is there a 1-hazard?





No, there are no hazards in this circuit.

```
[smothera@titan:37]> simv
Chronologic VCS simulator copyright 1991-2014
Contains Synopsys proprietary information.
Compiler version I-2014.03-2; Runtime version I-2014.03-2;  Jun 16 14:34 2019
-------------------------
| t(ns) | a b ci | co s |
-------------------------
|   1 | 0 0 0 | 0 0 |
|   2 | 0 0 1 | 0 1 |
|   3 | 0 1 0 | 0 1 |
|   4 | 0 1 1 | 1 0 |
|   5 | 1 0 0 | 0 1 |
|   6 | 1 0 1 | 1 0 |
|   7 | 1 1 0 | 1 0 |
|   8 | 1 1 1 | 1 1 |
-------------------------
          V C S   S i m u l a t i o n   R e p o r t
Time: 8000 ps
CPU Time:      0.190 seconds;       Data structure size:   0.0Mb
Sun Jun 16 14:34:29 2019
[smothera@titan:47]> simv
Chronologic VCS simulator copyright 1991-2014
Contains Synopsys proprietary information.
Compiler version I-2014.03-2; Runtime version I-2014.03-2;  Jun 16 15:02 2019
------------------------------
t(ns)| a b ci | co s | w1 w2 w3
------------------------------
   1 | 0 0 0 | 0 0 | 0 1 1
   2 | 0 0 1 | 0 1 | 0 1 1
   3 | 0 1 0 | 0 1 | 1 1 1
   4 | 0 1 1 | 1 0 | 1 0 1
   5 | 1 0 0 | 0 1 | 1 1 1
   6 | 1 0 1 | 1 0 | 1 0 1
   7 | 1 1 0 | 1 0 | 0 1 0
   8 | 1 1 1 | 1 1 | 0 1 0
------------------------------
------Above we used $display statements for each input combination---------

---Below we use a single $monitor statement to report every time the inputs change---
------------------------------
T(ns)| A B Ci | Co S | W1 W2 W3 inputs to 7 -> 0 now
------------------------------
   8 | 1 1 1 | 1 1 | 0 1 0
  10 | 1 1 0 | 1 0 | 0 1 0
  11 | 1 0 1 | 1 0 | 1 0 1
  12 | 1 0 0 | 0 1 | 1 1 1
  13 | 0 1 1 | 1 0 | 1 0 1
  14 | 0 1 0 | 0 1 | 1 1 1
  15 | 0 0 1 | 0 1 | 0 1 1
------------------------------
  16 | 0 0 0 | 0 0 | 0 1 1
          V C S   S i m u l a t i o n   R e p o r t
Time: 16000 ps
CPU Time:      0.190 seconds;       Data structure size:   0.0Mb
Sun Jun 16 15:02:13 2019
```

3) How does full_adder_wires[_tb].v Verilog circuit allow for the internal signals w1, w2, w3 to be visible on the test bench?

We declared the wires as parameters in the output portlist instead of in the "logic" file and then output them.