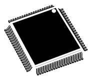
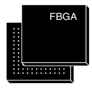
STM32F767xx STM32F768Ax STM32F769xx

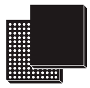
ARM®-based Cortex®-M7 32b MCU+FPU, 462DMIPS, up to 2MB Flash/512+16+4KB RAM, USB OTG HS/FS, ethernet, 18 TIMs, 3 ADCs, 28 com itf, cam, LCD, DSI

Data brief


LQFP100 (14 × 14 mm)
LQFP144 (20 × 20 mm)
LQFP176 (24 × 24 mm)
LQFP208 (28 x 28 mm)



UFBGA176 (10 x 10 mm)
TFBGA216 (13 x 13 mm)


WLCSP180
(0.4 mm pitch)

Features

- Core: ARM® 32-bit Cortex®-M7 CPU with DPFPU, ART Accelerator™ and L1-cache: 16 KB I/D cache, allowing 0-wait state execution from embedded Flash and external memories, up to 216 MHz, MPU, 462 DMIPS/2.14 DMIPS/MHz (Dhrystone 2.1), and DSP instructions.
- Memories
  - Up to 2 MB of Flash memory organized into two banks allowing read-while-write
  - SRAM: 512 KB (including 128 KB of data TCM RAM for critical real-time data) + 16 KB of instruction TCM RAM (for critical real-time routines) + 4 KB of backup SRAM
  - Flexible external memory controller with up to 32-bit data bus: SRAM, PSRAM, SDRAM/LPSDR SDRAM, NOR/NAND memories
- Dual mode Quad-SPI
- Graphics
  - Chrom-ART Accelerator™ (DMA2D), graphical hardware accelerator enabling enhanced graphical user interface
  - Hardware JPEG codec
  - LCD-TFT controller supporting up to XGA resolution
  - MIPI® DSI host controller supporting up to 720p 30 Hz resolution
- Clock, reset and supply management
  - 1.7 V to 3.6 V application supply and I/Os
  - POR, PDR, PVD and BOR
  - Dedicated USB power
  - 4-to-26 MHz crystal oscillator
  - Internal 16 MHz factory-trimmed RC (1% accuracy)
  - 32 kHz oscillator for RTC with calibration
  - Internal 32 kHz RC with calibration
- Low-power
  - Sleep, Stop and Standby modes
  - V_{BAT} supply for RTC, 32×32 bit backup registers + 4 KB backup SRAM
- 3×12-bit, 2.4 MSPS ADC: up to 24 channels
- Digital filters for sigma delta modulator (DFSDM)
- 2×12-bit D/A converters
- General-purpose DMA: 16-stream DMA controller with FIFOs and burst support
- Up to 18 timers: up to thirteen 16-bit (1x low-power 16-bit timer available in Stop mode) and two 32-bit timers, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input. All 15 timers running up to 216 MHz. 2x watchdogs, SysTick timer
- Debug mode
  - SWD & JTAG interfaces
  - Cortex®-M7 Trace Macrocell™
- Up to 168 I/O ports with interrupt capability
  - Up to 164 fast I/Os up to 108 MHz
  - Up to 166 5 V-tolerant I/Os
- Up to 28 communication interfaces
  - Up to 4 I²C interfaces (SMBus/PMBus)
  - Up to 4 USARTs/4 UARTs (27 Mbit/s, ISO7816 interface, LIN, IrDA, modem control)
  - Up to 6 SPIs (up to 50 Mbit/s), 3 with muxed simplex I²S for audio
  - 2 x SAIs (serial audio interface)
  - 3 × CANs (2.0B Active) and 2x SDMMCs
  - SPDIFRX interface
  - HDMI-CEC
  - MDIO slave interface
- Advanced connectivity
  - USB 2.0 full-speed device/host/OTG controller with on-chip PHY
  - USB 2.0 high-speed/full-speed device/host/OTG controller with dedicated DMA, on-chip full-speed PHY and ULPI
  - 10/100 Ethernet MAC with dedicated DMA: supports IEEE 1588v2 hardware, MII/RMII
- 8- to 14-bit camera interface up to 54 Mbyte/s
- True random number generator
- CRC calculation unit
- RTC: subsecond accuracy, hardware calendar
- 96-bit unique ID

Table 1. Device summary

Reference	Part number
STM32F767xx	STM32F767BG, STM32F767BI, STM32F767IG, STM32F767II, STM32F767NG, STM32F767NI, STM32F767VG, STM32F767VI, STM32F767ZG, STM32F767ZI
STM32F768Ax	STM32F768AI
STM32F769xx	STM32F769AG, STM32F769AI, STM32F769BG, STM32F769BI, STM32F769IG, STM32F769II, STM32F769NG, STM32F769NI

Contents

List of tables

List of figures

1 Description

The STM32F767xx, STM32F768Ax and STM32F769xx devices are based on the high-performance ARM® Cortex®-M7 32-bit RISC core operating at up to 216 MHz frequency. The Cortex®-M7 core features a floating point unit (FPU) which supports ARM® double-precision and single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32F767xx, STM32F768Ax and STM32F769xx devices incorporate high-speed embedded memories with a Flash memory up to 2 Mbytes, 512 Kbytes of SRAM (including 128 Kbytes of Data TCM RAM for critical real-time data), 16 Kbytes of instruction TCM RAM (for critical real-time routines), 4 Kbytes of backup SRAM available in the lowest power modes, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses, a 32-bit multi-AHB bus matrix and a multi layer AXI interconnect supporting internal and external memories access.

All the devices offer three 12-bit ADCs, two DACs, a low-power RTC, twelve general-purpose 16-bit timers including two PWM timers for motor control, two general-purpose 32-bit timers, a true random number generator (RNG). They also feature standard and advanced communication interfaces.

- Up to four I^2Cs
- Six SPIs, three I^2Ss in half-duplex mode. To achieve audio class accuracy, the I^2S peripherals can be clocked via a dedicated internal audio PLL or via an external clock to allow synchronization.
- Four USARTs plus four UARTs
- An USB OTG full-speed and a USB OTG high-speed with full-speed capability (with the ULPI)
- Three CANs
- Two SAI serial audio interfaces
- Two SDMMC host interfaces
- Ethernet and camera interfaces
- LCD-TFT display controller
- Chrom-ART Accelerator™
- SPDIFRX interface
- HDMI-CEC

Advanced peripherals include two SDMMC interfaces, a flexible memory control (FMC) interface, a Quad-SPI Flash memory interface, a camera interface for CMOS sensors. Refer to *Table 2: STM32F767xx, STM32F768Ax and STM32F769xx features and peripheral counts* for the list of peripherals available on each part number.

The STM32F767xx, STM32F768Ax and STM32F769xx devices operate in the –40 to +105 °C temperature range from a 1.7 to 3.6 V power supply. Dedicated supply inputs for USB (OTG_FS and OTG_HS) and SDMMC2 (clock, command and 4-bit data) are available on all packages except LQFP100 for greater power supply choice.

The supply voltage can drop to 1.7 V with the use of an external power supply supervisor (refer to *Section 2.18.2: Internal reset OFF*). A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F767xx, STM32F768Ax and STM32F769xx devices offer devices in 10 packages ranging from 100 pins to 216 pins. The set of included peripherals changes with the device chosen.

These features make the STM32F767xx, STM32F768Ax and STM32F769xx microcontrollers suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances
- Mobile applications, Internet of Things
- Wearable devices: smartwatches.

Figure 2 shows the general block diagram of the device family

Table 2. STM32F767xx, STM32F768Ax and STM32F769xx features and peripheral counts

Peripherals		STM32F76xVx		STM32F76xZx		STM32F769Ax		STM32F768Ax	STM32F76xIx		STM32F76xBx		STM32F76xNx	
Flash memory in Kbytes		1024	2048	1024	2048	1024	2048	2048	1024	2048	1024	2048	1024	2048
SRAM in Kbytes	System	512(368+16+128)												
	Instruction	16												
	Backup	4												
FMC memory controller		Yes(1)												
Quad-SPI		Yes												
Ethernet		Yes				No			Yes					
Timers	General-purpose	10												
	Advanced-control	2												
	Basic	2												
	Low-power	1												
Random number generator		Yes												
Communication interfaces	SPI / I^{2}S	4/3 (simplex)(2)		6/3 (simplex)(2)										
	I^{2}C	4												
	USART/UART	4/4												
	USB OTG FS	Yes												
	USB OTG HS	Yes												
	CAN	3												
	SAI	2												
	SPDIFRX	4 inputs												
	SDMMC1	Yes												
	SDMMC2	Yes(3)												
Camera interface		Yes												
MIPI-DSI Host(4)		No				Yes								
LCD-TFT		Yes												
Chrom-ART Accelerator™ (DMA2D)		Yes												
JPEG codec		Yes												
GPIOs		82		114					140		168			

Table 2. STM32F767xx, STM32F768Ax and STM32F769xx features and peripheral counts (continued)

Peripherals	STM32F76xVx	STM32F76xZx	STM32F769Ax	STM32F768Ax	STM32F76xIx	STM32F76xBx	STM32F76xNx
12-bit ADC	3						
Number of channels	16	24					
12-bit DAC Number of channels	Yes 2						
Maximum CPU frequency	216 MHz[5]						
Operating voltage	1.7 to 3.6 V[6]						
Operating temperatures	Ambient temperatures: –40 to +85 °C /–40 to +105 °C						
	Junction temperature: –40 to + 125 °C						
Package	LQFP100	LQFP144	WLCSP180		UFBGA176[7] LQFP176	LQFP208	TFBGA216

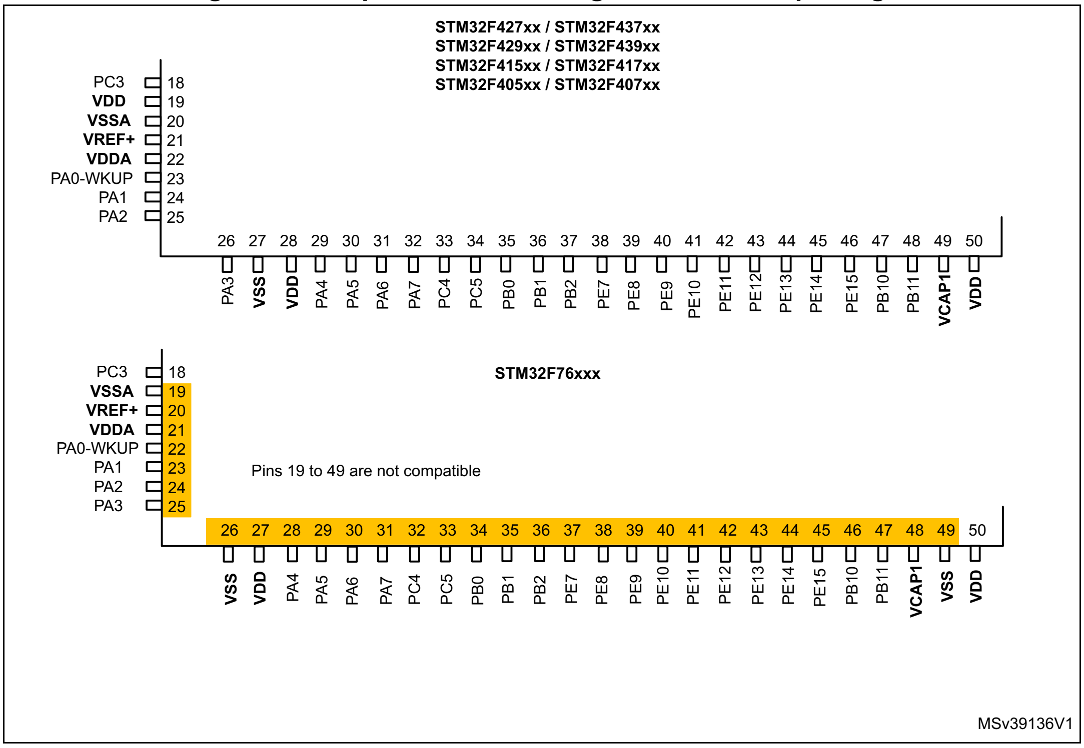
1. For the LQFP100 package, only FMC Bank1 is available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select.
2. The SPI1, SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.
3. SDMMC2 supports a dedicated power rail for clock, command and data 0..4 lines, feature available starting from 144 pin package.
4. DSI host interface is only available on STM32F769x sales types.
5. 216 MHz maximum frequency for - 40°C to + 85°C ambient temperature range (200 MHz maximum frequency for - 40°C to + 105°C ambient temperature range).
6. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the internal reset is OFF (refer to *Section 2.18.2: Internal reset OFF*).
7. UFBGA176 is not available for STM32F769x sales types.

1.1 Full compatibility throughout the family

The STM32F767xx, STM32F768Ax and STM32F769xx devices are fully pin-to-pin, compatible with the STM32F4xxxx devices, allowing the user to try different peripherals, and reaching higher performances (higher frequency) for a greater degree of freedom during the development cycle.

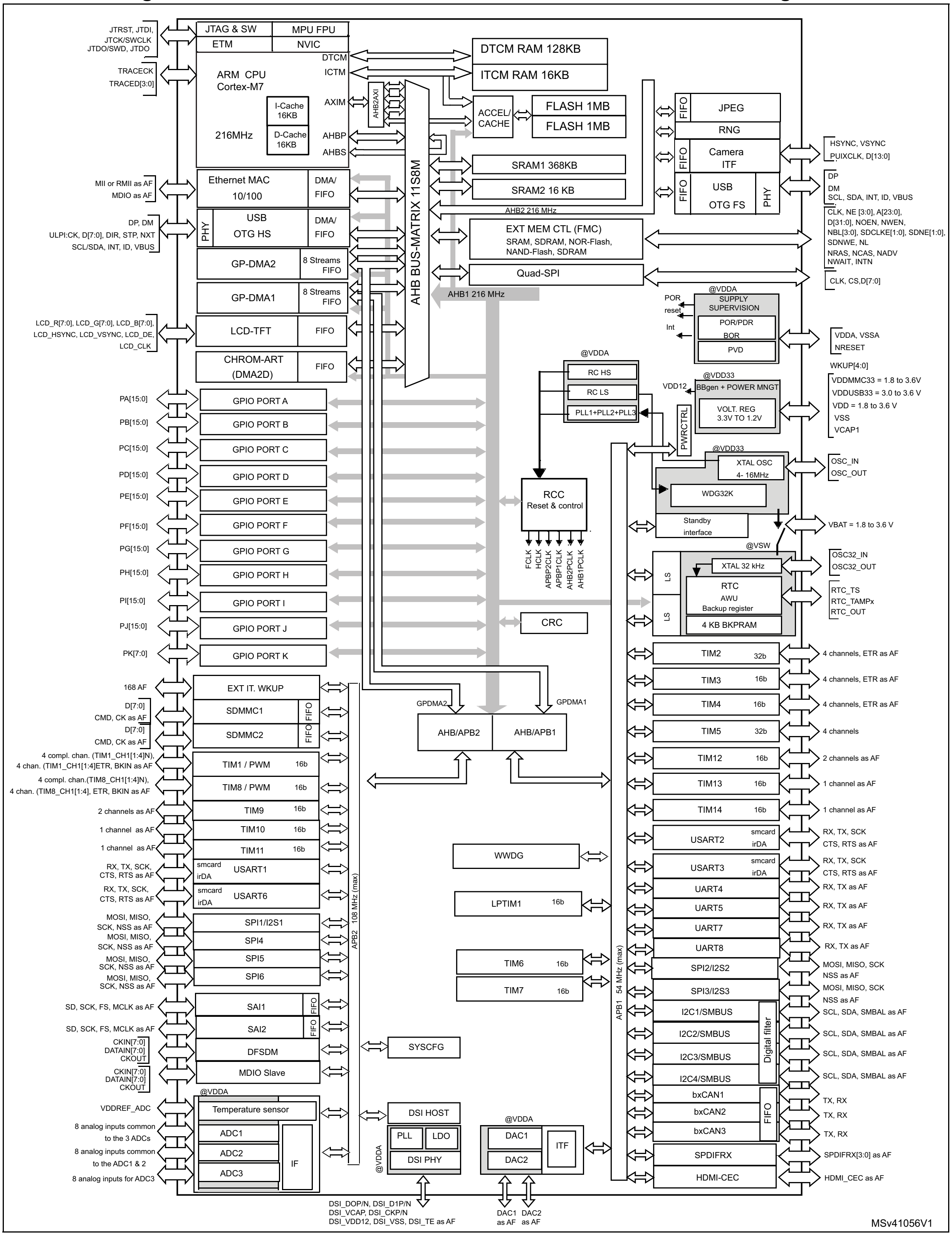
Figure 1 give compatible board designs between the STM32F7xx and STM32F4xx families.

Figure 1. Compatible board design for LQFP100 package



The STM32F76x LQFP144, LQFP176, LQFP208, TFBGA216, UFBGA176 packages are fully pin to pin compatible with STM32F4xx devices.

Figure 2. STM32F767xx, STM32F768Ax and STM32F769xx block diagram



1. The timers connected to APB2 are clocked from TIMxCLK up to 216 MHz, while the timers connected to APB1 are clocked from TIMxCLK either up to 108 MHz or 216 MHz depending on TIMPRE bit configuration in the RCC_DCKCFGR register.

2 Functional overview

2.1 ARM® Cortex®-M7 with FPU

The ARM® Cortex®-M7 with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and low interrupt latency.

The Cortex®-M7 processor is a highly efficient high-performance featuring:

- Six-stage dual-issue pipeline
- Dynamic branch prediction
- Harvard caches (16 Kbytes of I-cache and 16 Kbytes of D-cache)
- 64-bit AXI4 interface
- 64-bit ITCM interface
- 2x32-bit DTCM interfaces

The processor supports the following memory interfaces:

- Tightly Coupled Memory (TCM) interface.
- Harvard instruction and data caches and AXI master (AXIM) interface.
- Dedicated low-latency AHB-Lite peripheral (AHBP) interface.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

It supports single and double precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

Figure 2 shows the general block diagram of the STM32F76xxx family.

Note: Cortex®-M7 with FPU core is binary compatible with the Cortex®-M4 core.

2.2 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

2.3 Embedded Flash memory

The STM32F767xx, STM32F768Ax and STM32F769xx devices embed a Flash memory of up to 2 Mbytes available for storing programs and data.

2.4 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.5 Embedded SRAM

All the devices feature:

- System SRAM up to 512 Kbytes:
  - SRAM1 on AHB bus Matrix: 368 Kbytes
  - SRAM2 on AHB bus Matrix: 16 Kbytes
  - DTCM-RAM on TCM interface (Tighly Coupled Memory interface): 128 Kbytes for critical real-time data.
- Instruction RAM (ITCM-RAM) 16 Kbytes:
  - It is mapped on TCM interface and reserved only for CPU Execution/Instruction useful for critical real-time routines.

The Data TCM RAM is accessible by the GP-DMAs and peripherals DMAs through specific AHB slave of the CPU.The instruction TCM RAM is reserved only for CPU. It is accessed at CPU clock speed with 0 wait states.

- 4 Kbytes of backup SRAM

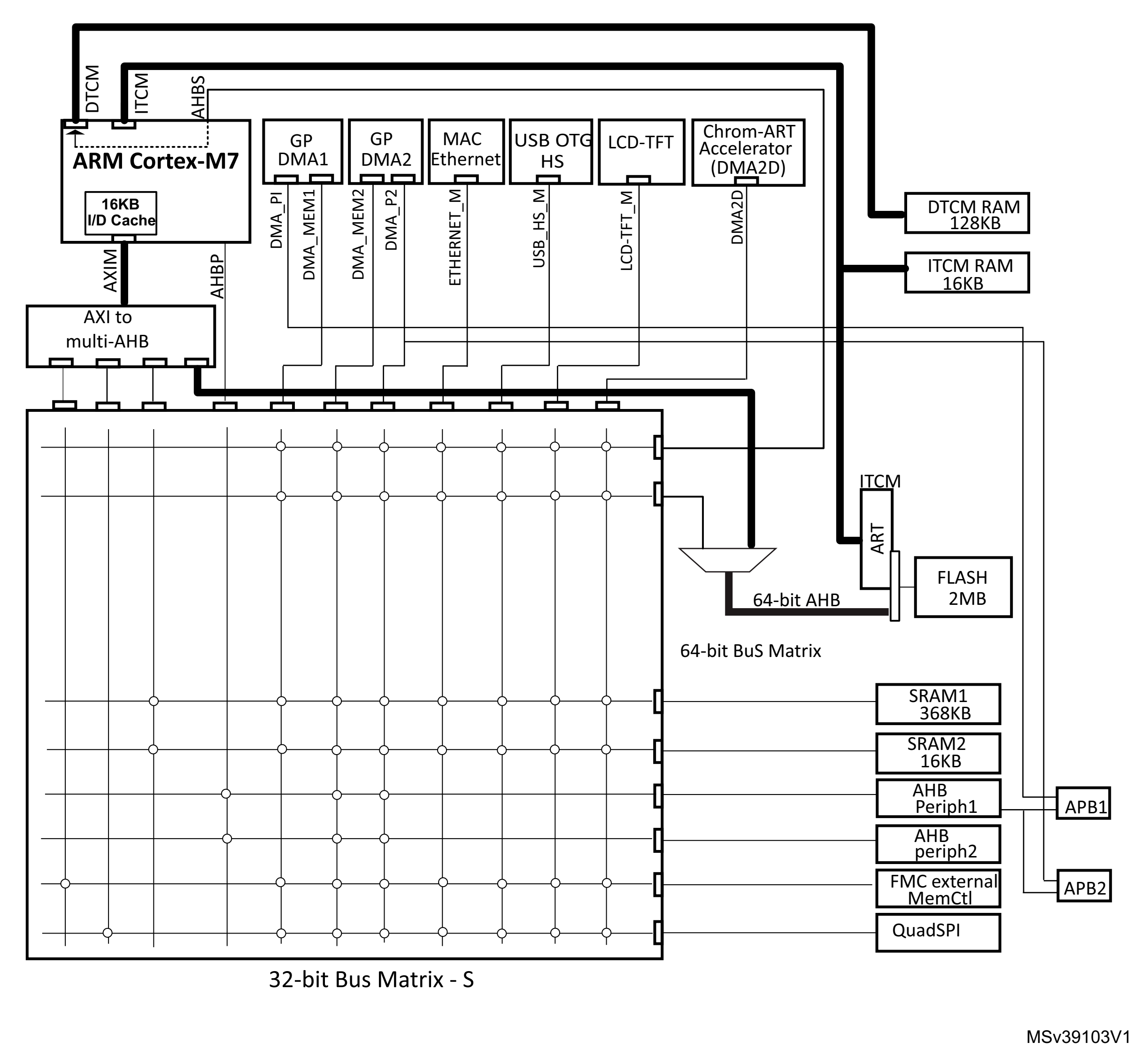
  This area is accessible only from the CPU. Its content is protected against possible unwanted write accesses, and is retained in Standby or V_{BAT} mode.

2.6 AXI-AHB bus matrix

The STM32F767xx, STM32F768Ax and STM32F769xx system architecture is based on 2 sub-systems:

- An AXI to multi AHB bridge converting AXI4 protocol to AHB-Lite protocol:
  - 3x AXI to 32-bit AHB bridges connected to AHB bus matrix
  - 1x AXI to 64-bit AHB bridge connected to the embedded Flash memory
- A multi-AHB Bus-Matrix
  - The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, Ethernet, USB HS, LCD-TFT, and DMA2D) and the slaves (Flash memory, RAM, FMC, Quad-SPI, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 3. STM32F767xx, STM32F768Ax and STM32F769xx AXI-AHB bus matrix architecture(1)



1. The above figure has large wires for 64-bits bus and thin wires for 32-bits bus.

2.7 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals:
- SPI and I^2S
- I^2C
- USART
- General-purpose, basic and advanced-control timers TIMx
- DAC
- SDMMC
- Camera interface (DCMI)
- ADC
- SAI
- SPDIFRX
- Quad-SPI
- HDMI-CEC
- JPEG codec
- DFSDM

2.8 Flexible memory controller (FMC)

The Flexible memory controller (FMC) includes three memory controllers:
- The NOR/PSRAM memory controller
- The NAND/memory controller
- The Synchronous DRAM (SDRAM/Mobile LPSDR SDRAM) controller

The main features of the FMC controller are the following:
- Interface with static-memory mapped devices including:
  - Static random access memory (SRAM)
  - NOR Flash memory/OneNAND Flash memory
  - PSRAM (4 memory banks)
  - NAND Flash memory with ECC hardware to check up to 8 Kbytes of data
- Interface with synchronous DRAM (SDRAM/Mobile LPSDR SDRAM) memories
- 8-,16-,32-bit data bus width
- Independent Chip Select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO
- Read FIFO for SDRAM controller
- The maximum FMC_CLK/FMC_SDCLK frequency for synchronous accesses is HCLK/2

LCD parallel interface

The FMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

2.9 Quad-SPI memory interface (QUADSPI)

All the devices embed a Quad-SPI memory interface, which is a specialized communication interface targetting Single, Dual or Quad-SPI Flash memories. It can work in:

- Direct mode through registers
- External flash status register polling mode
- Memory mapped mode.

Up to 256 Mbytes external flash are memory mapped, supporting 8, 16 and 32-bit access. Code execution is supported.

The opcode and the frame format are fully programmable. Communication can be either in Single Data Rate or Dual Data Rate.

2.10 LCD-TFT controller

The LCD-TFT display controller provides a 24-bit parallel digital RGB (Red, Green, Blue) and delivers all signals to interface directly to a broad range of LCD and TFT panels up to XGA (1024x768) resolution with the following features:

- 2 display layers with dedicated FIFO (64x32-bit)
- Color Look-Up table (CLUT) up to 256 colors (256x24-bit) per layer
- Up to 8 input color formats selectable per layer
- Flexible blending between two layers using alpha value (per pixel or constant)
- Flexible programmable parameters for each layer
- Color keying (transparency color)
- Up to 4 programmable interrupt events

2.11 Chrom-ART Accelerator™ (DMA2D)

The Chrom-Art Accelerator™ (DMA2D) is a graphic accelerator which offers advanced bit blitting, row data copy and pixel format conversion. It supports the following functions:

- Rectangle filling with a fixed color
- Rectangle copy
- Rectangle copy with pixel format conversion
- Rectangle composition with blending and pixel format conversion

Various image format coding are supported, from indirect 4bpp color mode up to 32bpp direct color. It embeds dedicated memory to store color lookup tables.

An interrupt can be generated when an operation is complete or at a programmed watermark.

All the operations are fully automatized and are running independently from the CPU or the DMAs.

2.12 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 110 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M7 with FPU core.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

2.13 JPEG codec (JPEG)

The JPEG codec provides an fast and simple hardware compressor and decompressor of JPEG images with full management of JPEG headers.

The JPEG codec main features:

- 8-bit/channel pixel depths
- Single clock per pixel encoding and decoding
- Support for JPEG header generation and parsing
- Up to four programmable quantization tables
- Fully programmable Huffman tables (two AC and two DC)
- Fully programmable minimum coded unit (MCU)
- Encode/decode support (non simultaneous)
- Single clock Huffman coding and decoding
- Two-channel interface: Pixel/Compress In, Pixel/Compressed Out
- Stallable design
- Support for single, greyscale component
- Functionality to enable/disable header processing
- Internal register interface
- Fully synchronous design
- Configured for high-speed decode mode

2.14 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 25 edge-detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 168 GPIOs can be connected to the 16 external interrupt lines.

2.15 Clocks and startup

On reset the 16 MHz internal HSI RC oscillator is selected as the default CPU clock. The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy. The application can then select as system clock either the RC oscillator or an external 4-26 MHz clock source. This clock can be monitored for failure. If a failure is detected, the system automatically switches back to the internal RC oscillator and a software interrupt is generated (if enabled). This clock source is input to a PLL thus allowing to increase the frequency up to 216 MHz. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example if an indirectly used external oscillator fails).

Several prescalers allow the configuration of the two AHB buses, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the two AHB buses is 216 MHz while the maximum frequency of the high-speed APB domains is 108 MHz. The maximum allowed frequency of the low-speed APB domain is 54 MHz.

The devices embed two dedicated PLL (PLLI2S and PLLSAI) which allow to achieve audio class performance. In this case, the I^2S and SAI master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

2.16 Boot modes

At startup, the boot memory space is selected by the BOOT pin and BOOT_ADDx option bytes, allowing to program any boot memory address from 0x0000 0000 to 0x3FFF FFFF which includes:

- All Flash address space mapped on ITCM or AXIM interface
- All RAM address space: ITCM, DTCM RAMs and SRAMs mapped on AXIM interface
- The System memory bootloader

The boot loader is located in system memory. It is used to reprogram the Flash memory through a serial interface. Refer to *STM32 microcontroller system memory boot mode* application note (AN2606) for details.

2.17 Power supply schemes

- V_{DD} = 1.7 to 3.6 V: external power supply for I/Os and the internal regulator (when enabled), provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 1.7 to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- VDDUSB can be connected either to VDD or an external independent power supply (3.0 to 3.6V) for USB transceivers. For example, when device is powered at 1.8V, an independent power supply 3.3V can be connected to VDDUSB.
- VDDSDMMC can be connected either to VDD or an external independent power supply (1.8 to 3.6V) for SDMMC2 pins (clock, command, and 4-bit data). For example, when device is powered at 1.8V, an independent power supply 2.7V can be connected to VDDSDMMC.
- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

Note: V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the internal reset is OFF (refer to Section 2.18.2: Internal reset OFF). Refer to Table 3: Voltage regulator configuration mode versus device operating mode to identify the packages supporting this option.

2.18 Power supply supervisor

2.18.1 Internal reset ON

On packages embedding the PDR_ON pin, the power supply supervisor is enabled by holding PDR_ON high. On the other packages, the power supply supervisor is always enabled.

The device has an integrated power-on reset (POR)/ power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry. At power-on, POR/PDR is always active and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is reached, the option byte loading process starts, either to confirm or modify default BOR thresholds, or to disable BOR permanently. Three BOR thresholds are available through option bytes. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for an external reset circuit.

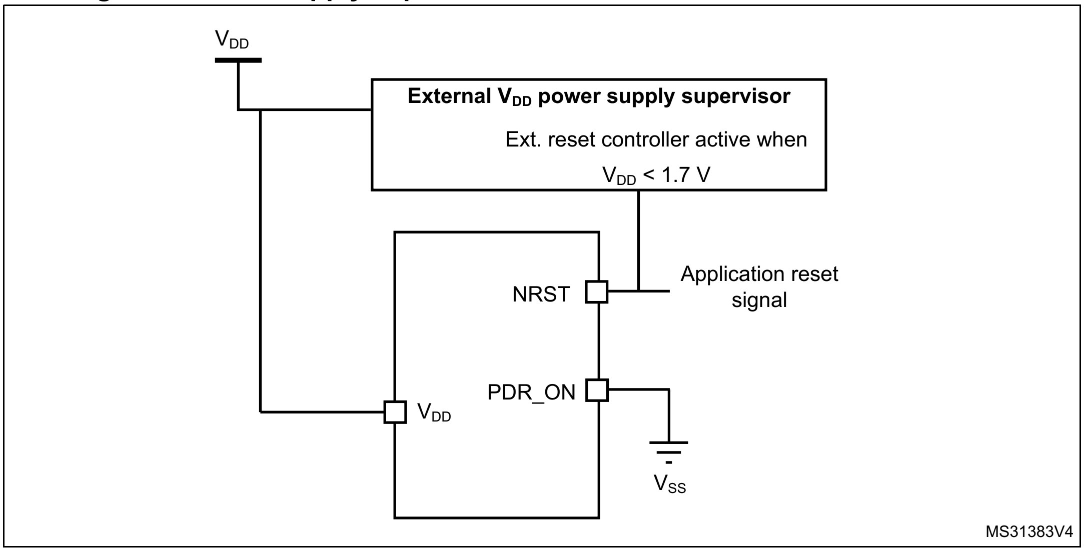
The device also features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

2.18.2 Internal reset OFF

This feature is available only on packages featuring the PDR_ON pin. The internal power-on reset (POR) / power-down reset (PDR) circuitry is disabled through the PDR_ON pin.

An external power supply supervisor should monitor V_{DD} and NRST and should maintain the device in reset mode as long as V_{DD} is below a specified threshold. PDR_ON should be connected to V_{SS}. Refer to *Figure 4: Power supply supervisor interconnection with internal reset OFF*.

Figure 4. Power supply supervisor interconnection with internal reset OFF



The V_{DD} specified threshold, below which the device must be maintained under reset, is 1.7 V (see *Figure 5*).

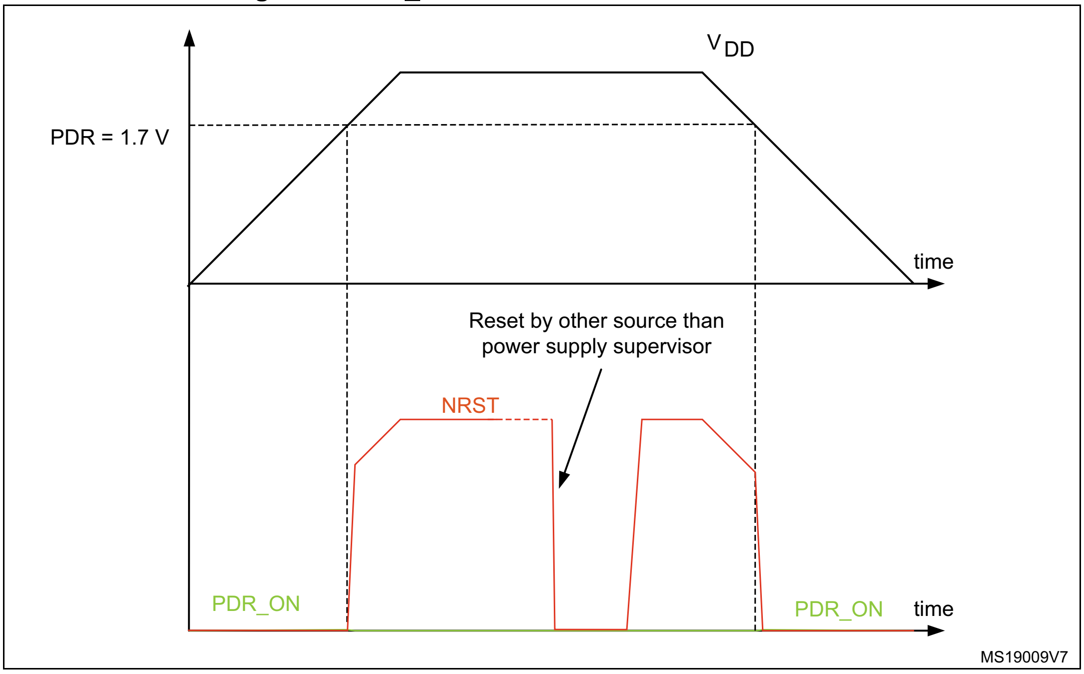
A comprehensive set of power-saving mode allows to design low-power applications.

When the internal reset is OFF, the following integrated features are no more supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled
- The brownout reset (BOR) circuitry must be disabled
- The embedded programmable voltage detector (PVD) is disabled
- V_{BAT} functionality is no more available and V_{BAT} pin should be connected to V_{DD}.

All the packages, except for the LQFP100, allow to disable the internal reset through the PDR_ON signal when connected to V_{SS}.

Figure 5. PDR_ON control with internal reset OFF



2.19 Voltage regulator

The regulator has four operating modes:

- Regulator ON
  - Main regulator mode (MR)
  - Low power regulator (LPR)
  - Power-down
- Regulator OFF

2.19.1 Regulator ON

On packages embedding the BYPASS_REG pin, the regulator is enabled by holding BYPASS_REG low. On all other packages, the regulator is always enabled.

There are three power modes configured by software when the regulator is ON:

- MR mode used in Run/sleep modes or in Stop modes
  - In Run/Sleep modes

    The MR mode is used either in the normal mode (default mode) or the over-drive mode (enabled by software). Different voltages scaling are provided to reach the best compromise between maximum frequency and dynamic power consumption. The over-drive mode allows operating at a higher frequency than the normal mode for a given voltage scaling.

– In Stop modes

  The MR can be configured in two ways during stop mode:

  MR operates in normal mode (default mode of MR in stop mode)

  MR operates in under-drive mode (reduced leakage mode).

- LPR is used in the Stop modes:

  The LP regulator mode is configured by software when entering Stop mode.

  Like the MR mode, the LPR can be configured in two ways during stop mode:

  – LPR operates in normal mode (default mode when LPR is ON)
  – LPR operates in under-drive mode (reduced leakage mode).
- Power-down is used in Standby mode.

  The Power-down mode is activated only when entering in Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption. The contents of the registers and SRAM are lost.

Refer to *Table 3* for a summary of voltage regulator modes versus device operating modes.

Two external ceramic capacitors should be connected on V_{CAP_1} and V_{CAP_2} pin.

All packages have the regulator ON feature.

Table 3. Voltage regulator configuration mode versus device operating mode(1)

Voltage regulator configuration	Run mode	Sleep mode	Stop mode	Standby mode
Normal mode	MR	MR	MR or LPR	-
Over-drive mode(2)	MR	MR	-	-
Under-drive mode	-	-	MR or LPR	-
Power-down mode	-	-	-	Yes

1. ‘-’ means that the corresponding configuration is not available.
2. The over-drive mode is not available when V_{DD} = 1.7 to 2.1 V.

2.19.2 Regulator OFF

This feature is available only on packages featuring the BYPASS_REG pin. The regulator is disabled by holding BYPASS_REG high. The regulator OFF mode allows to supply externally a V_{12} voltage source through V_{CAP_1} and V_{CAP_2} pins.

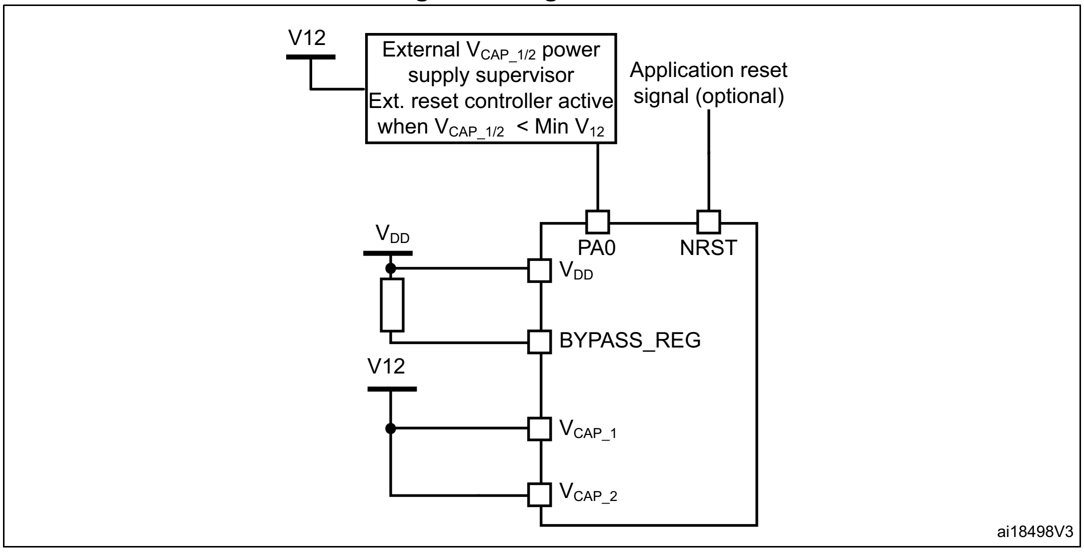
Since the internal voltage scaling is not managed internally, the external voltage value must be aligned with the targeted maximum frequency.The two 2.2 µF ceramic capacitors should be replaced by two 100 nF decoupling capacitors.

When the regulator is OFF, there is no more internal monitoring on V_{12}. An external power supply supervisor should be used to monitor the V_{12} of the logic power domain. PA0 pin should be used for this purpose, and act as power-on reset on V_{12} power domain.

In regulator OFF mode, the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset a part of the V_{12} logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used under power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection under reset or pre-reset is required.
- The over-drive and under-drive modes are not available.
- The Standby mode is not available.

Figure 6. Regulator OFF

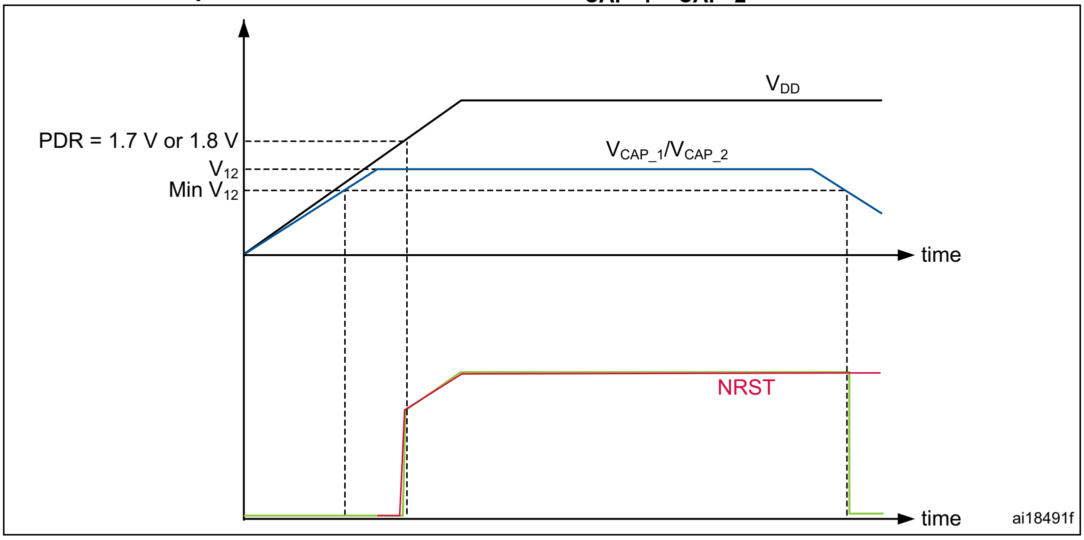


The following conditions must be respected:

- V_{DD} should always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains.
- If the time for V_{CAP_1} and V_{CAP_2} to reach V_{12} minimum value is faster than the time for V_{DD} to reach 1.7 V, then PA0 should be kept low to cover both conditions: until V_{CAP_1} and V_{CAP_2} reach V_{12} minimum value and until V_{DD} reaches 1.7 V (see *Figure 7*).
- Otherwise, if the time for V_{CAP_1} and V_{CAP_2} to reach V_{12} minimum value is slower than the time for V_{DD} to reach 1.7 V, then PA0 could be asserted low externally (see *Figure 8*).
- If V_{CAP_1} and V_{CAP_2} go below V_{12} minimum value and V_{DD} is higher than 1.7 V, then a reset must be asserted on PA0 pin.

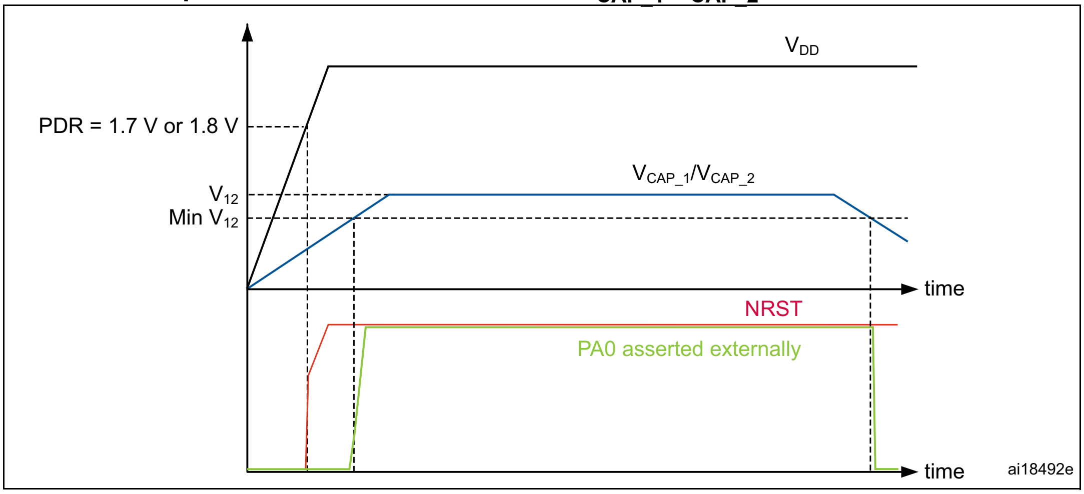
Note: The minimum value of V_{12} depends on the maximum frequency targeted in the application.

Figure 7. Startup in regulator OFF: slow V_{DD} slope - power-down reset risen after V_{CAP_1}/V_{CAP_2} stabilization



1. This figure is valid whatever the internal reset mode (ON or OFF).

Figure 8. Startup in regulator OFF mode: fast V_{DD} slope - power-down reset risen before V_{CAP_1}/V_{CAP_2} stabilization



1. This figure is valid whatever the internal reset mode (ON or OFF).

2.19.3 Regulator ON/OFF and internal reset ON/OFF availability

Table 4. Regulator ON/OFF and internal reset ON/OFF availability

<table>
<tr><th>Package</th><th>Regulator ON</th><th>Regulator OFF</th><th>Internal reset ON</th><th>Internal reset OFF</th></tr>
<tr><td>LQFP100</td><td rowspan="2">Yes</td><td rowspan="2">No</td><td>Yes</td><td>No</td></tr>
<tr><td>LQFP144, LQFP208</td><td rowspan="3">Yes
PDR_ON set to V_{DD}</td><td rowspan="3">Yes
PDR_ON set to V_{SS}</td></tr>
<tr><td>LQFP176, UFBGA176, TFBGA216</td><td>Yes
BYPASS_REG set to V_{SS}</td><td>Yes
BYPASS_REG set to V_{DD}</td></tr>
<tr><td>WLCSP180</td><td colspan="2">Yes(1)</td></tr>
</table>

1. Available only on dedicated part number. Refer to *Section 6: Part numbering*.

2.20 Real-time clock (RTC), backup SRAM and backup registers

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to V_{BAT} mode.
- 17-bit auto-reload wakeup timer (WUT) for periodic events with programmable resolution and period.

The RTC and the 32 backup registers are supplied through a switch that takes power either from the V_{DD} supply when present or from the V_{BAT} pin.

The backup registers are 32-bit registers used to store 128 bytes of user application data when VDD power is not present. They are not reset by a system or power reset, or when the device wakes up from Standby mode.

The RTC clock sources can be:

- A 32.768 kHz external crystal (LSE)
- An external resonator or oscillator(LSE)
- The internal low power RC oscillator (LSI, with typical frequency of 32 kHz)
- The high-speed external clock (HSE) divided by 32

The RTC is functional in V_{BAT} mode and in all low-power modes when it is clocked by the LSE. When clocked by the LSI, the RTC is not functional in V_{BAT} mode, but is functional in all low-power modes.

All RTC events (Alarm, WakeUp Timer, Timestamp or Tamper) can generate an interrupt and wakeup the device from the low-power modes.

2.21 Low-power modes

The devices support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

  The Stop mode achieves the lowest power consumption while retaining the contents of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled.

  The voltage regulator can be put either in main regulator mode (MR) or in low-power mode (LPR). Both modes can be configured as follows (see *Table 5: Voltage regulator modes in stop mode*):

  – Normal mode (default mode when MR or LPR is enabled)

  – Under-drive mode.

  The device can be woken up from the Stop mode by any of the EXTI line (the EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm / wakeup / tamper / time stamp events, the USB OTG FS/HS wakeup or the Ethernet wakeup and LPTIM1 asynchronous interrupt).

Table 5. Voltage regulator modes in stop mode

Voltage regulator configuration	Main regulator (MR)	Low-power regulator (LPR)
Normal mode	MR ON	LPR ON
Under-drive mode	MR in under-drive mode	LPR in under-drive mode

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering

Standby mode, the SRAM and register contents are lost except for registers in the backup domain and the backup SRAM when selected.

The device exits the Standby mode when an external reset (NRST pin), an IWDG reset, a rising or falling edge on one of the 6 WKUP pins (PA0, PA2, PC1, PC13, PI8, PI11), or an RTC alarm / wakeup / tamper /time stamp event occurs.

The Standby mode is not supported when the embedded voltage regulator is bypassed and the 1.2 V domain is controlled by an external power.

2.22 V_{BAT} operation

The V_{BAT} pin allows to power the device V_{BAT} domain from an external battery, an external supercapacitor, or from V_{DD} when no external battery and an external supercapacitor are present.

V_{BAT} operation is activated when V_{DD} is not present.

The V_{BAT} pin supplies the RTC, the backup registers and the backup SRAM.

Note: When the microcontroller is supplied from V_{BAT}, external interrupts and RTC alarm/events do not exit it from V_{BAT} operation.

When PDR_ON pin is connected to V_{SS} (Internal Reset OFF), the V_{BAT} functionality is no more available and V_{BAT} pin should be connected to VDD.

2.23 Timers and watchdogs

The devices include two advanced-control timers, eight general-purpose timers, two basic timers and two watchdog timers.

All timer counters can be frozen in debug mode.

Table 6 compares the features of the advanced-control, general-purpose and basic timers.

Table 6. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary output	Max interface clock (MHz)	Max timer clock (MHz)(1)
Advanced -control	TIM1, TIM8	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	Yes	108	216
General purpose	TIM2, TIM5	32-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	54	108/216
	TIM3, TIM4	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	54	108/216
	TIM9	16-bit	Up	Any integer between 1 and 65536	No	2	No	108	216
	TIM10, TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No	108	216
	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No	54	108/216
	TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No	54	108/216
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No	54	108/216

1. The maximum timer clock is either 108 or 216 MHz depending on TIMPRE bit configuration in the RCC_DCKCFGR register.

2.23.1 Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1, TIM8) can be seen as three-phase PWM generators multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as 16-bit PWM generators, they have full modulation capability (0-100%).

The advanced-control timer can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

TIM1 and TIM8 support independent DMA request generation.

2.23.2 General-purpose timers (TIMx)

There are ten synchronizable general-purpose timers embedded in the STM32F76xxx devices (see *Table 6* for differences).

- **TIM2, TIM3, TIM4, TIM5**

  The STM32F76xxx include 4 full-featured general-purpose timers: TIM2, TIM5, TIM3, and TIM4.The TIM2 and TIM5 timers are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. The TIM3 and TIM4 timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

  The TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8 via the Timer Link feature for synchronization or event chaining.

  Any of these general-purpose timers can be used to generate PWM outputs.

  TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

- **TIM9, TIM10, TIM11, TIM12, TIM13, and TIM14**

  These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10, TIM11, TIM13, and TIM14 feature one independent channel, whereas TIM9 and TIM12 have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers. They can also be used as simple time bases.

2.23.3 Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger and waveform generation. They can also be used as a generic 16-bit time base.

TIM6 and TIM7 support independent DMA request generation.

2.23.4 Low-power timer (LPTIM1)

The low-power timer has an independent clock and is running also in Stop mode if it is clocked by LSE, LSI or an external clock. It is able to wakeup the devices from Stop mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous / one-shot mode
- Selectable software / hardware input trigger
- Selectable clock source:
- Internal clock source: LSE, LSI, HSI or APB clock
- External clock source over LPTIM input (working even with no internal clock source running, used by the Pulse Counter Application)
- Programmable digital glitch filter
- Encoder mode

2.23.5 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

2.23.6 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

2.23.7 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

2.24 Inter-integrated circuit interface (I^2C)

The device embeds 4 I2C. Refer to table *Table 7: I2C implementation* for the features implementation.

The I^2C bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- I^2C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System Management Bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (Packet Error Checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power System Management Protocol (PMBus™) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming.
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 7. I2C implementation

I2C features(1)	I2C1	I2C2	I2C3	I2C4
Standard-mode (up to 100 kbit/s)	X	X	X	X
Fast-mode (up to 400 kbit/s)	X	X	X	X
Fast-mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X	X	X	X
Programmable analog and digital noise filters	X	X	X	X
SMBus/PMBus hardware support	X	X	X	X
Independent clock	X	X	X	X

1. X: supported.

2.25 Universal synchronous/asynchronous receiver transmitters (USART)

The device embeds USART. Refer to *Table 8: USART implementation* for the features implementation.

The universal synchronous asynchronous receiver transmitter (USART) offers a flexible means of full-duplex data exchange with external equipment requiring an industry standard NRZ asynchronous serial data format.

The USART peripheral supports:

- Full-duplex asynchronous communications
- Configurable oversampling method by 16 or 8 to give flexibility between speed and clock tolerance
- Dual clock domain allowing convenient baud rate programming independent from the PCLK reprogramming
- A common programmable transmit and receive baud rate of up to 27 Mbit/s when USART clock source is system clock frequency (max is 216 MHz) and oversampling by 8 is used.
- Auto baud rate detection
- Programmable data word length (7 or 8 or 9 bits) word length
- Programmable data order with MSB-first or LSB-first shifting
- Progarmmable parity (odd, even, no parity)
- Configurable stop bits (1 or 1.5 or 2 stop bits)
- Synchronous mode and clock output for synchronous communications
- Single-wire half-duplex communications
- Separate signal polarity control for transmission and reception
- Swappable Tx/Rx pin configuration
- Hardware flow control for modem and RS-485 transceiver
- Multiprocessor communications
- LIN master synchronous break send capability and LIN slave break detection capability
- IrDA SIR encoder decoder supporting 3/16 bit duration for normal mode
- Smartcard mode (T=0 and T=1 asynchronous protocols for Smartcards as defined in the ISO/IEC 7816-3 standard)
- Support for Modbus communication

The table below summarizes the implementation of all U(S)ARTs instances

Table 8. USART implementation

features(1)	USART1/2/3/6	UART4/5/7/8
Data Length	7, 8 and 9 bits	
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous mode	X	-

Table 8. USART implementation (continued)

features[(1)]	USART1/2/3/6	UART4/5/7/8
Smartcard mode	X	-
Single-wire half-duplex communication	X	X
IrDA SIR ENDEC block	X	X
LIN mode	X	X
Dual clock domain	X	X
Receiver timeout interrupt	X	X
Modbus communication	X	X
Auto baud rate detection	X	X
Driver Enable	X	X

1. X: supported.

2.26 Serial peripheral interface (SPI)/inter- integrated sound interfaces (I2S)

The devices feature up to six SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1, SPI4, SPI5, and SPI6 can communicate at up to 50 Mbit/s, SPI2 and SPI3 can communicate at up to 25 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable from 4 to 16 bits. The SPI interfaces support NSS pulse mode, TI mode and Hardware CRC calculation. All SPIs can be served by the DMA controller.

Three standard I^2S interfaces (multiplexed with SPI1, SPI2 and SPI3) are available. They can be operated in master or slave mode, in simplex communication modes, and can be configured to operate with a 16-/32-bit resolution as an input or output channel. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I^2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

All I2Sx can be served by the DMA controller.

2.27 Serial audio interface (SAI)

The devices embed two serial audio interfaces.

The serial audio interface is based on two independent audio subblocks which can operate as transmitter or receiver with their FIFO. Many audio protocols are supported by each block: I2S standards, LSB or MSB-justified, PCM/DSP, TDM, AC’97 and SPDIF output, supporting audio sampling frequencies from 8 kHz up to 192 kHz. Both subblocks can be configured in master or in slave mode.

In master mode, the master clock can be output to the external DAC/CODEC at 256 times of the sampling frequency.

The two sub-blocks can be configured in synchronous mode when full-duplex mode is required.

SAI1 and SAI2 can be served by the DMA controller

2.28 SPDIFRX Receiver Interface (SPDIFRX)

The SPDIFRX peripheral, is designed to receive an S/PDIF flow compliant with IEC-60958 and IEC-61937. These standards support simple stereo streams up to high sample rate, and compressed multi-channel surround sound, such as those defined by Dolby or DTS (up to 5.1).

The main features of the SPDIFRX are the following:

- Up to 4 inputs available
- Automatic symbol rate detection
- Maximum symbol rate: 12.288 MHz
- Stereo stream from 32 to 192 kHz supported
- Supports Audio IEC-60958 and IEC-61937, consumer applications
- Parity bit management
- Communication using DMA for audio samples
- Communication using DMA for control and user channel information
- Interrupt capabilities

The SPDIFRX receiver provides all the necessary features to detect the symbol rate, and decode the incoming data stream. The user can select the wanted SPDIF input, and when a valid signal will be available, the SPDIFRX will re-sample the incoming signal, decode the manchester stream, recognize frames, sub-frames and blocks elements. It delivers to the CPU decoded data, and associated status flags.

The SPDIFRX also offers a signal named spdif_frame_sync, which toggles at the S/PDIF sub-frame rate that will be used to compute the exact sample rate for clock drift algorithms.

2.29 Audio PLL (PLLI2S)

The devices feature an additional dedicated PLL for audio I^2S and SAI applications. It allows to achieve error-free I^2S sampling clock accuracy without compromising on the CPU performance, while using USB peripherals.

The PLLI2S configuration can be modified to manage an I^2S/SAI sample rate change without disabling the main PLL (PLL) used for CPU, USB and Ethernet interfaces.

The audio PLL can be programmed with very low error to obtain sampling rates ranging from 8 KHz to 192 KHz.

In addition to the audio PLL, a master clock input pin can be used to synchronize the I^2S/SAI flow with an external PLL (or Codec output).

2.30 Audio and LCD PLL (PLLSAI)

An additional PLL dedicated to audio and LCD-TFT is used for SAI1 peripheral in case the PLLI2S is programmed to achieve another audio sampling frequency (49.152 MHz or 11.2896 MHz) and the audio application requires both sampling frequencies simultaneously.

The PLLSAI is also used to generate the LCD-TFT clock.

2.31 SD/SDIO/MMC card host interface (SDMMC)

SDMMCs host interface are available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit.

The interface allows data transfer at up to 50 MHz, and is compliant with the SD Memory Card Specification Version 2.0.

The SDMMC Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDMMC/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

The SDMMC can be served by the DMA controller

2.32 Ethernet MAC interface with dedicated DMA and IEEE 1588 support

The devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard medium-independent interface (MII) or a reduced medium-independent interface (RMII). The microcontroller requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). The PHY is connected to the device MII port using 17 signals for MII or 9 signals for RMII, and can be clocked using the 25 MHz (MII) from the microcontroller.

The devices include the following features:

- Supports 10 and 100 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers between the dedicated SRAM and the descriptors
- Tagged MAC frame support (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames) support
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 2 Kbytes.
- Supports hardware PTP (precision time protocol) in accordance with IEEE 1588 2008 (PTP V2) with the time stamp comparator connected to the TIM2 input
- Triggers interrupt when system time becomes greater than target time

2.33 Controller area network (bxCAN)

The three CANs are compliant with the 2.0A and B (active) specifications with a bit rate up to 1 Mbit/s. They can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three transmit mailboxes, two receive FIFOS with 3 stages and 28 shared scalable filter banks (all of them can be used even if one

CAN is used). 256 bytes of SRAM are allocated for CAN1 and CAN2. 512 bytes of SRAM are dedicated for CAN3.

2.34 Universal serial bus on-the-go full-speed (OTG_FS)

The device embeds an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 2.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

The major features are:

- Combined Rx and Tx FIFO size of 1.28 Kbytes with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 1 bidirectional control endpoint + 5 IN endpoints + 5 OUT endpoints
- 12 host channels with periodic OUT support
- Software configurable to OTG1.3 and OTG2.0 modes of operation
- OTG 2.0 Supports ADP (Attach detection Protocol)
- USB 2.0 LPM (Link Power Management) support
- Battery Charging Specification Revision 1.2 support
- Internal FS OTG PHY support
- HNP/SNP/IP inside (no need for any external resistor)

For OTG/Host modes, a power switch is needed in case bus-powered devices are connected

2.35 Universal serial bus on-the-go high-speed (OTG_HS)

The device embeds a USB OTG high-speed (up to 480 Mbit/s) device/host/OTG peripheral. The USB OTG HS supports both full-speed and high-speed operations. It integrates the transceivers for full-speed operation (12 Mbit/s) and features a UTMI low-pin interface (ULPI) for high-speed operation (480 Mbit/s). When using the USB OTG HS in HS mode, an external PHY device connected to the ULPI is required.

The USB OTG HS peripheral is compliant with the USB 2.0 specification and with the OTG 2.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

The major features are:

- Combined Rx and Tx FIFO size of 4 Kbytes with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 8 bidirectional endpoints
- 16 host channels with periodic OUT support
- Software configurable to OTG1.3 and OTG2.0 modes of operation
- OTG 2.0 Supports ADP (Attach detection Protocol)
- USB 2.0 LPM (Link Power Management) support
- Battery Charging Specification Revision 1.2 support

- Internal FS OTG PHY support
- External HS or HS OTG operation supporting ULPI in SDR mode. The OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output.
- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- for OTG/Host modes, a power switch is needed in case bus-powered devices are connected

2.36 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The device embeds a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI-CEC controller to wakeup the MCU from Stop mode on data reception.

2.37 Digital camera interface (DCMI)

The devices embed a camera interface that can connect with camera modules and CMOS sensors through an 8-bit to 14-bit parallel interface, to receive video data. The camera interface can sustain a data transfer rate up to 54 Mbyte/s in 8-bit mode at 54 MHz. It features:

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication can be 8-, 10-, 12- or 14-bit
- Supports 8-bit progressive video monochrome or raw bayer format, YCbCr 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Supports continuous mode or snapshot (a single frame) mode
- Capability to automatically crop the image

2.38 Management Data Input/Output (MDIO) slaves

The device embed a MDIO slave interface it includes the following features:

- 32 MDIO Registers addresses, each of which is managed using separate input and output data registers:
  - 32 x 16-bit firmware read/write, MDIO read-only output data registers
  - 32 x 16-bit firmware read-only, MDIO write-only input data registers
- Configurable slave (port) address
- Independently maskable interrupts/events:
  - MDIO Register write
  - MDIO Register read
  - MDIO protocol error
- Able to operate in and wake up from STOP mode

2.39 Random number generator (RNG)

All the devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

2.40 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allowing maximum I/O toggling up to 108 MHz.

2.41 Analog-to-digital converters (ADCs)

Three 12-bit analog-to-digital converters are embedded and each ADC shares up to 16 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold

The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1, TIM2, TIM3, TIM4, TIM5, or TIM8 timer.

2.42 Digital filter for Sigma-Delta Modulators (DFSDM)

The device embeds one DFSDM with 4 digital filters modules and 8 external input serial channels (transceivers) or alternately 8 internal parallel inputs support. The DFSDM peripheral is dedicated to interface the external ΣΔ modulators to microcontroller and then to perform digital filtering of the received data streams (which represent analog value on ΣΔ modulators inputs). DFSDM can also interface PDM (Pulse Density Modulation) microphones and perform PDM to PCM conversion and filtering in hardware. DFSDM features optional parallel data stream inputs from microcontrollers memory (through DMA/CPU transfers into DFSDM). DFSDM transceivers support several serial interface formats (to support various ΣΔ modulators). DFSDM digital filter modules perform digital processing according user selected filter parameters with up to 24-bit final ADC resolution.

The DFSDM peripheral supports:

- 8 multiplexed input digital serial channels:
  - Configurable SPI interface to connect various SD modulator(s)
  - Configurable Manchester coded 1 wire interface support
  - PDM (Pulse Density Modulation) microphone input support
  - Maximum input clock frequency up to 20 MHz (10 MHz for Manchester coding)
  - Clock output for SD modulator(s): 0..20 MHz
- Alternative inputs from 8 internal digital parallel channels (up to 16 bit input resolution):
  - internal sources: device memory data streams (DMA)
- 4 digital filter modules with adjustable digital signal processing:
  - Sincxfilter: filter order/type (1..5), oversampling ratio (up to 1..1024)
  - integrator: oversampling ratio (1..256)
- Up to 24-bit output data resolution, signed output data format
- Automatic data offset correction (offset stored in register by user)
- Continuous or single conversion
- Start-of-conversion triggered by:
  - Software trigger
  - Internal timers
  - External events
  - Start-of-conversion synchronously with first digital filter module (DFSDM0)
- Analog watchdog feature:
  - Low value and high value data threshold registers
  - Dedicated configurable Sincx digital filter (order = 1..3, oversampling ratio = 1..32)
  - Input from final output data or from selected input digital serial channels
  - Continuous monitoring independently from standard conversion
- Short circuit detector to detect saturated analog input values (bottom and top range):
  - Up to 8-bit counter to detect 1..256 consecutive 0’s or 1’s on serial data stream
  - Monitoring continuously each input serial channel
- Break signal generation on analog watchdog event or on short circuit detector event
- Extremes detector:
  - Storage of minimum and maximum values of final conversion data
  - Refreshed by software

- DMA capability to read the final conversion data
- Interrupts: end of conversion, overrun, analog watchdog, short circuit, input serial channel clock absence
- “regular” or “injected” conversions:
  - “regular” conversions can be requested at any time or even in continuous mode without having any impact on the timing of “injected” conversions
  - “injected” conversions for precise timing and with high conversion priority

2.43 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 1.7 V and 3.6 V. The temperature sensor is internally connected to the same input channel as V_{BAT}, ADC1_IN18, which is used to convert the sensor output voltage into a digital value. When the temperature sensor and V_{BAT} conversion are enabled at the same time, only V_{BAT} conversion is performed.

As the offset of the temperature sensor varies from chip to chip due to process variation, the internal temperature sensor is mainly suitable for applications that detect temperature changes instead of absolute temperatures. If an accurate temperature reading is needed, then an external temperature sensor part should be used.

2.44 Digital-to-analog converter (DAC)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference V_{REF+}

Eight DAC trigger inputs are used in the device. The DAC channels are triggered through the timer update outputs that are also connected to different DMA streams.

2.45 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with

SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

2.46 Embedded Trace Macrocell™

The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F76xxx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

2.47 DSI Host (DSIHOST)

The DSI Host is a dedicated peripheral for interfacing with MIPI® DSI compliant displays. It includes a dedicated video interface internally connected to the LTDC and a generic APB interface that can be used to transmit information to the display.

These interfaces are as follows:

- LTDC interface:
  - Used to transmit information in Video mode, in which the transfers from the host processor to the peripheral take the form of a real-time pixel stream (DPI).
  - Through a customized for mode, this interface can be used to transmit information in full bandwidth in the Adapted Command mode (DBI).
- APB slave interface:
  - Allows the transmission of generic information in Command mode, and follows a proprietary register interface.
  - Can operate concurrently with either LTDC interface in either Video mode or Adapted Command mode.
- Video mode pattern generator:
  - Allows the transmission of horizontal/vertical color bar and D-PHY BER testing pattern without any kind of stimuli.

The DSI Host main features:

- Compliant with MIPI® Alliance standards
- Interface with MIPI® D-PHY
- Supports all commands defined in the MIPI® Alliance specification for DCS:
  - Transmission of all Command mode packets through the APB interface
  - Transmission of commands in low-power and high-speed during Video mode
- Supports up to two D-PHY data lanes
- Bidirectional communication and escape mode support through data lane 0
- Supports non-continuous clock in D-PHY clock lane for additional power saving
- Supports Ultra Low-power mode with PLL disabled
- ECC and Checksum capabilities

- Support for End of Transmission Packet (EoTp)
- Fault recovery schemes
- 3D transmission support
- Configurable selection of system interfaces:
  - AMBA APB for control and optional support for Generic and DCS commands
  - Video Mode interface through LTDC
  - Adapted Command mode interface through LTDC
- Independently programmable Virtual Channel ID in
  - Video mode
  - Adapted Command mode
  - APB Slave

Video Mode interfaces features:

- LTDC interface color coding mappings into 24-bit interface:
  - 16-bit RGB, configurations 1, 2, and 3
  - 18-bit RGB, configurations 1 and 2
  - 24-bit RGB
- Programmable polarity of all LTDC interface signals
- Extended resolutions beyond the DPI standard
- Maximum resolution of 800x480 pixels:
- Maximum resolution is limited by available DSI physical link bandwidth:
  - Number of lanes: 2
  - Maximum speed per lane: 500 Mbps1Gbps

Adapted interface features

Support for sending large amounts of data through the memory_write_start(WMS) and memory_write_continue(WMC) DCS commands

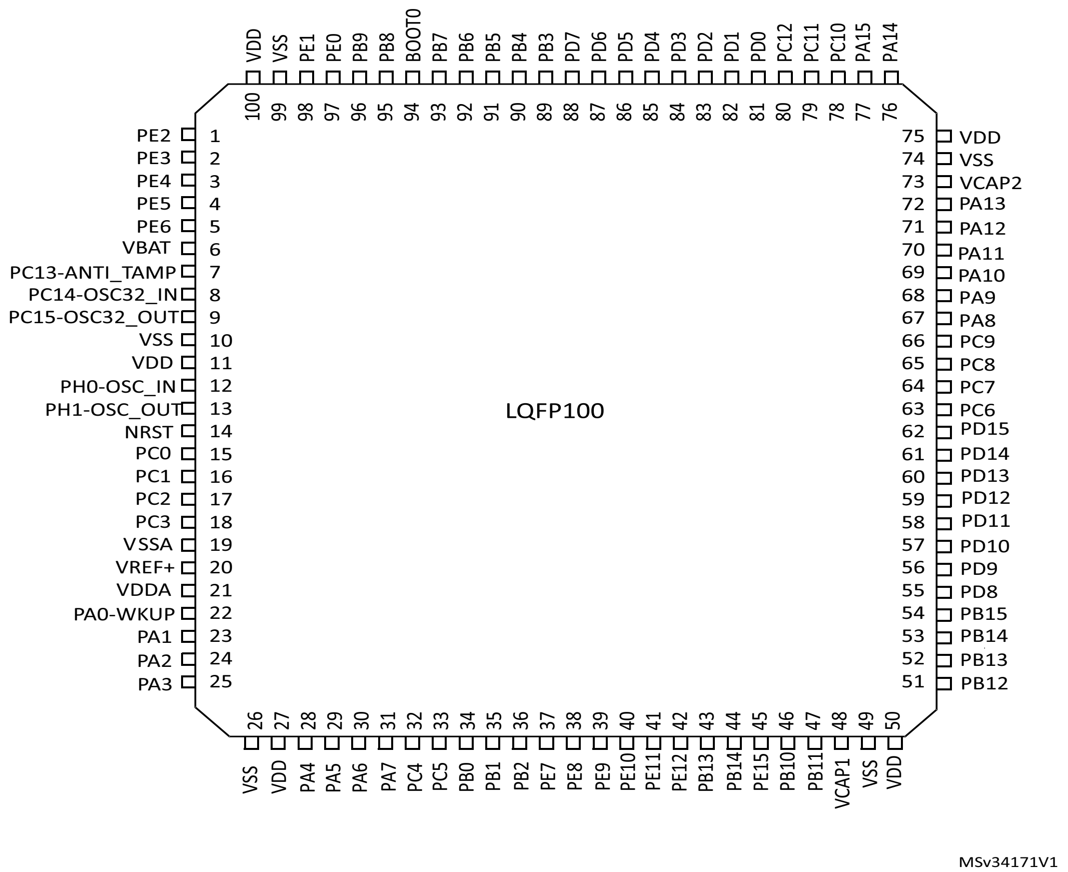
- LTDC interface color coding mappings into 24-bit interface:
  - 16-bit RGB, configurations 1, 2, and 3
  - 18-bit RGB, configurations 1 and 2
  - 24-bit RGB

Video mode pattern generator:

- Vertical and horizontal color bar generation without LTDC stimuli
- BER pattern without LTDC stimuli

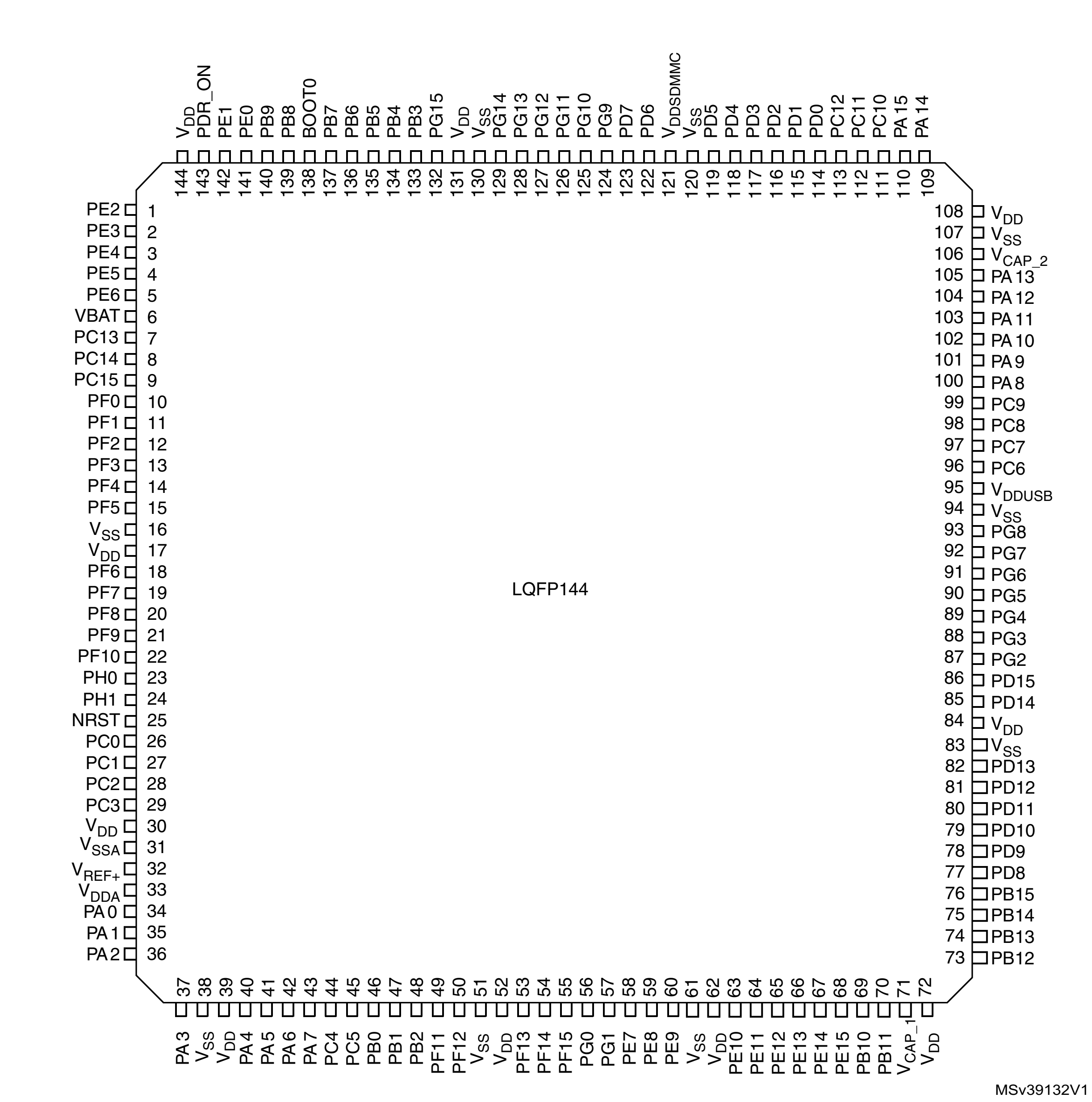
3 Pinouts and pin description

Figure 9. STM32F767xx LQFP100 pinout



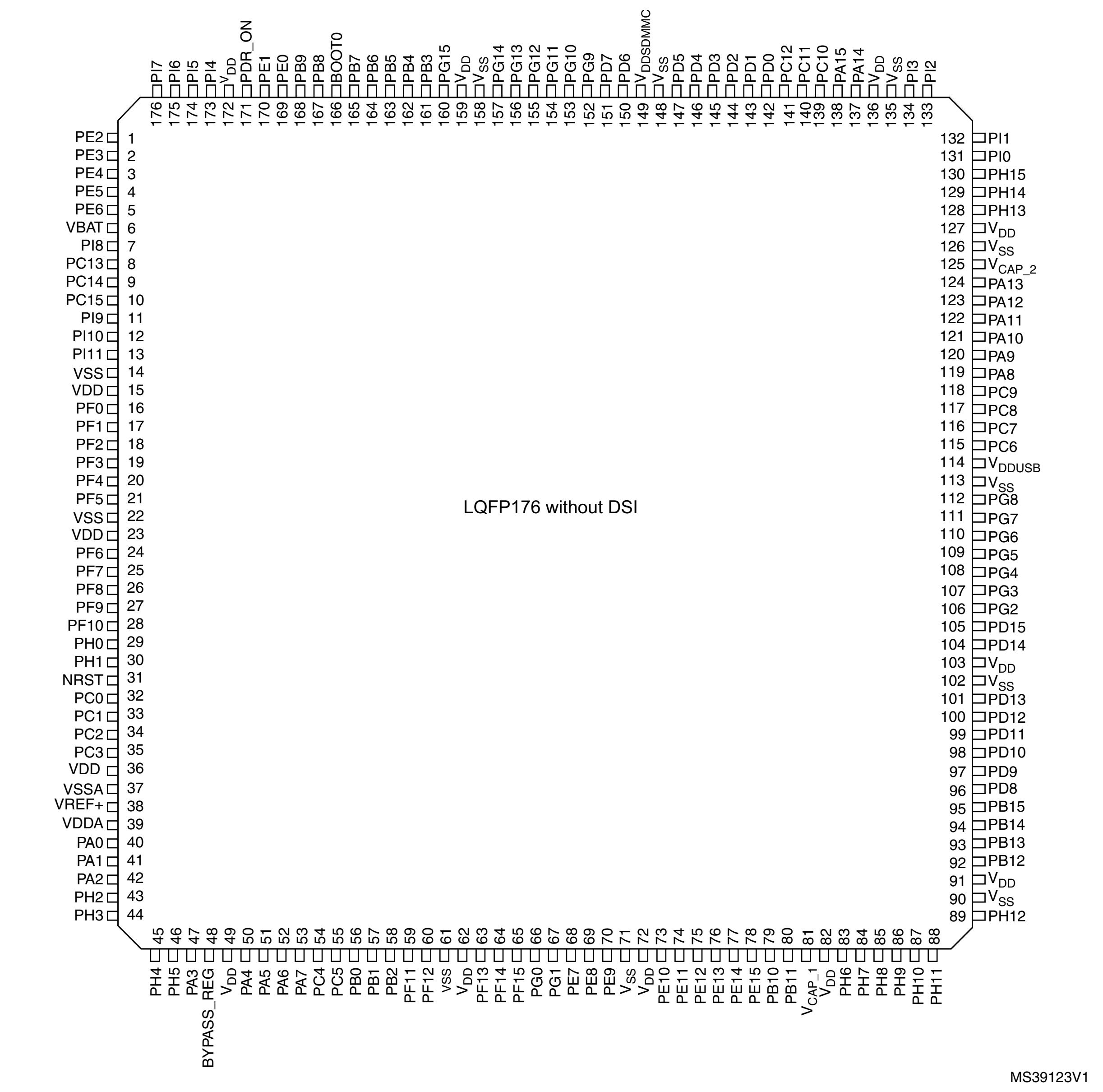
1. The above figure shows the package top view.

Figure 10. STM32F767xx LQFP144 pinout



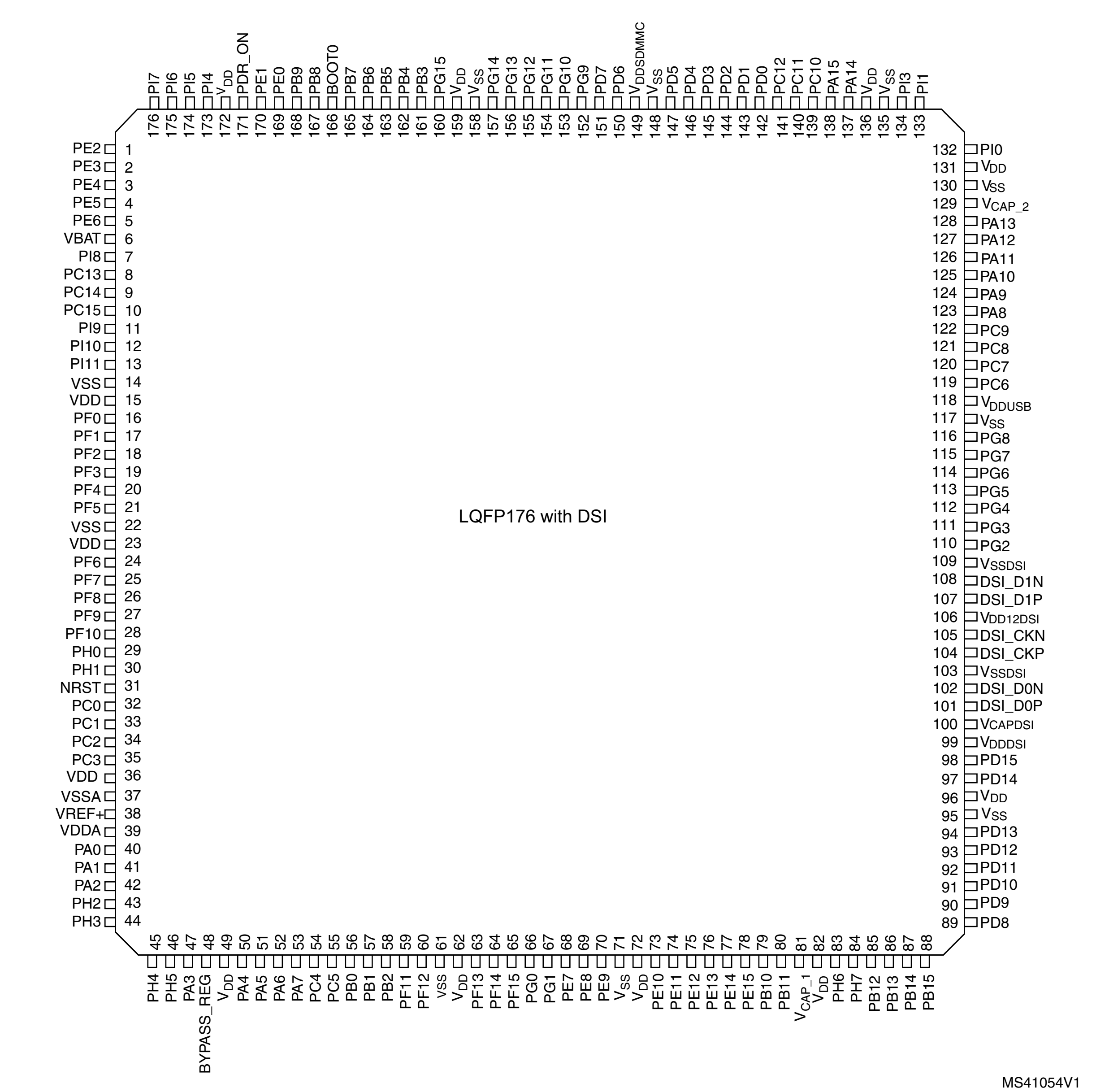
1. The above figure shows the package top view.

Figure 11. STM32F767xx LQFP176 pinout



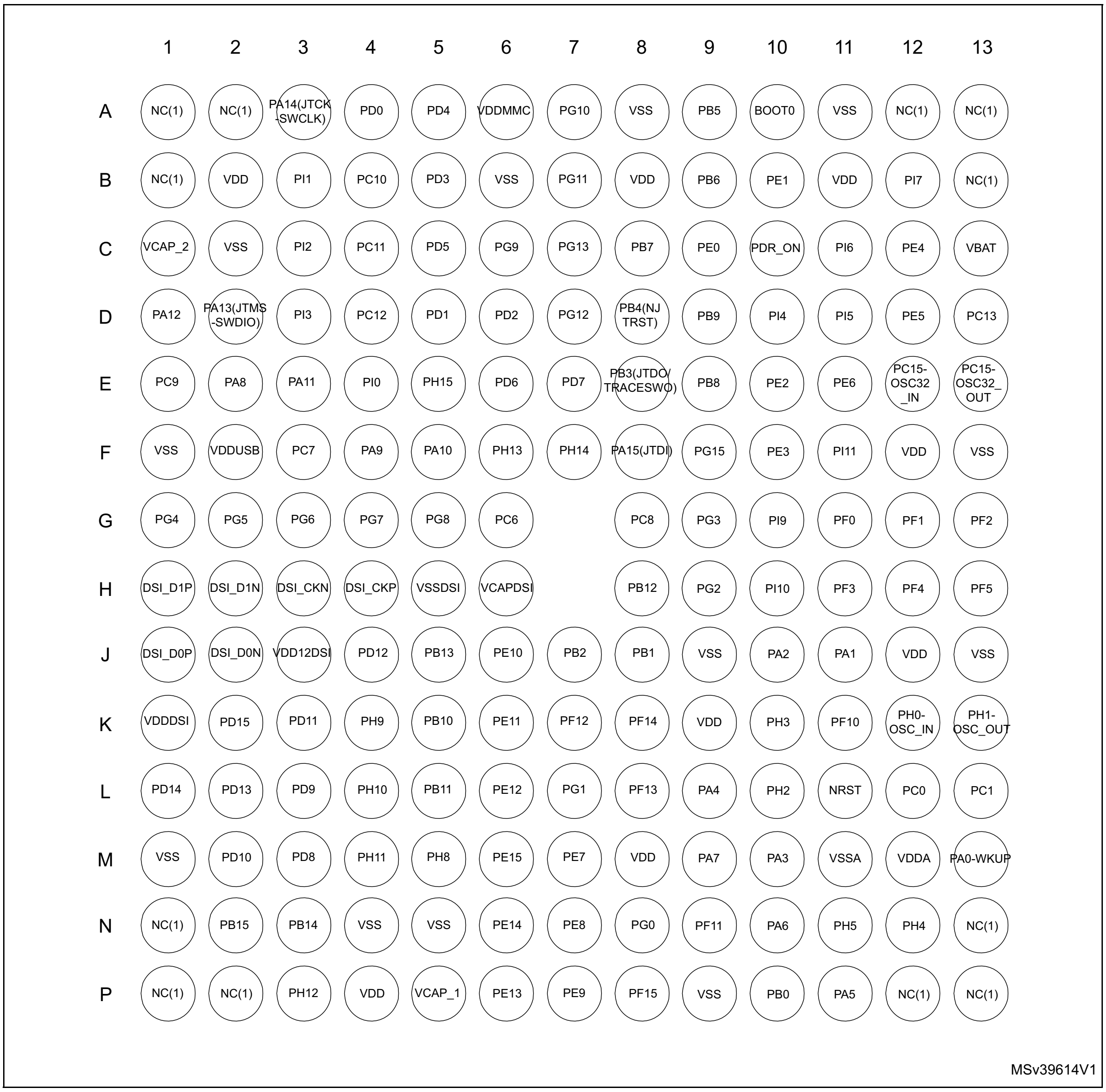
1. The above figure shows the package top view.

Figure 12. STM32F769xx LQFP176 pinout



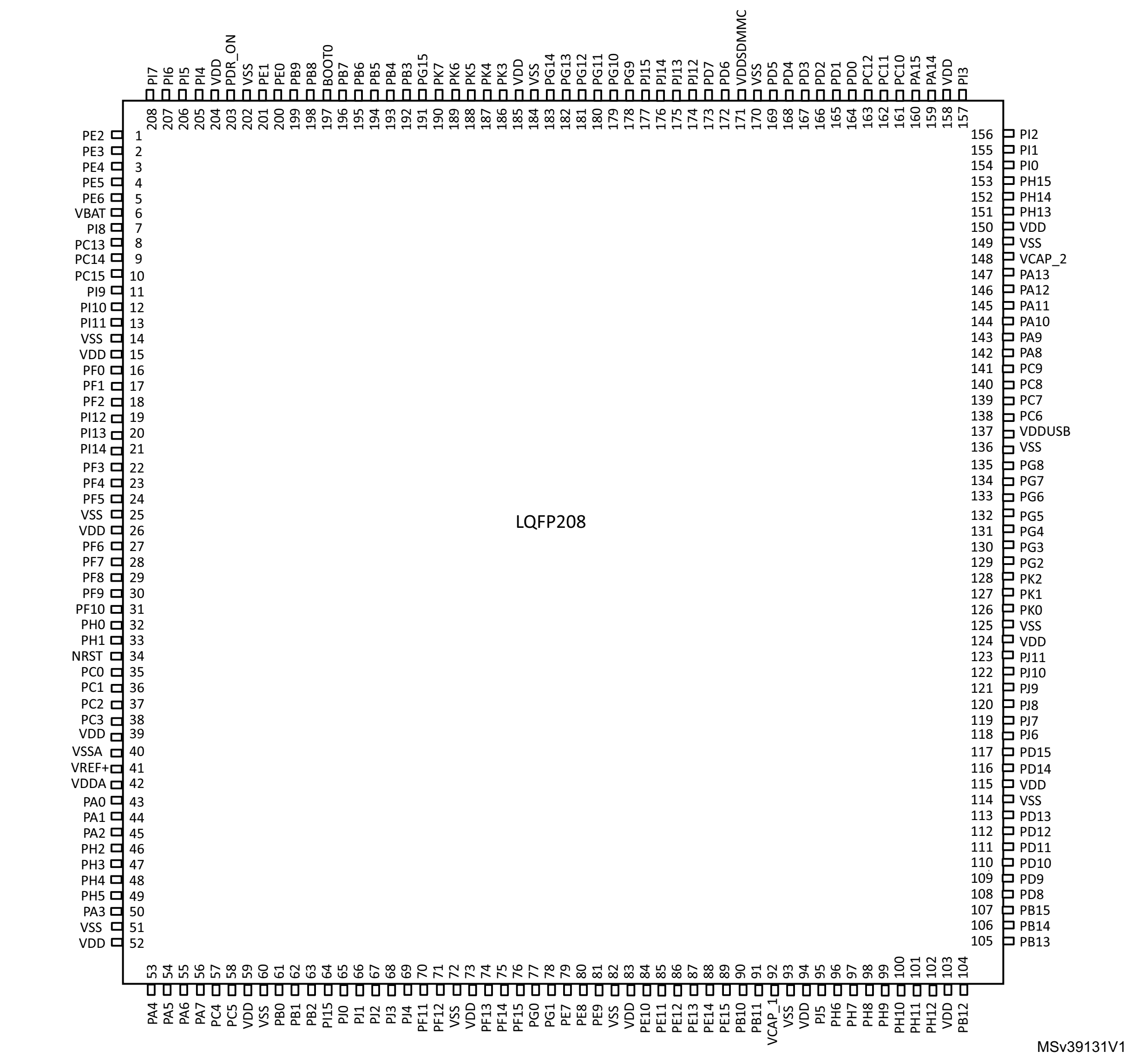
1. The above figure shows the package top view.

Figure 13. STM32F769xx/STM32F768Ax WLCSP180 ballout



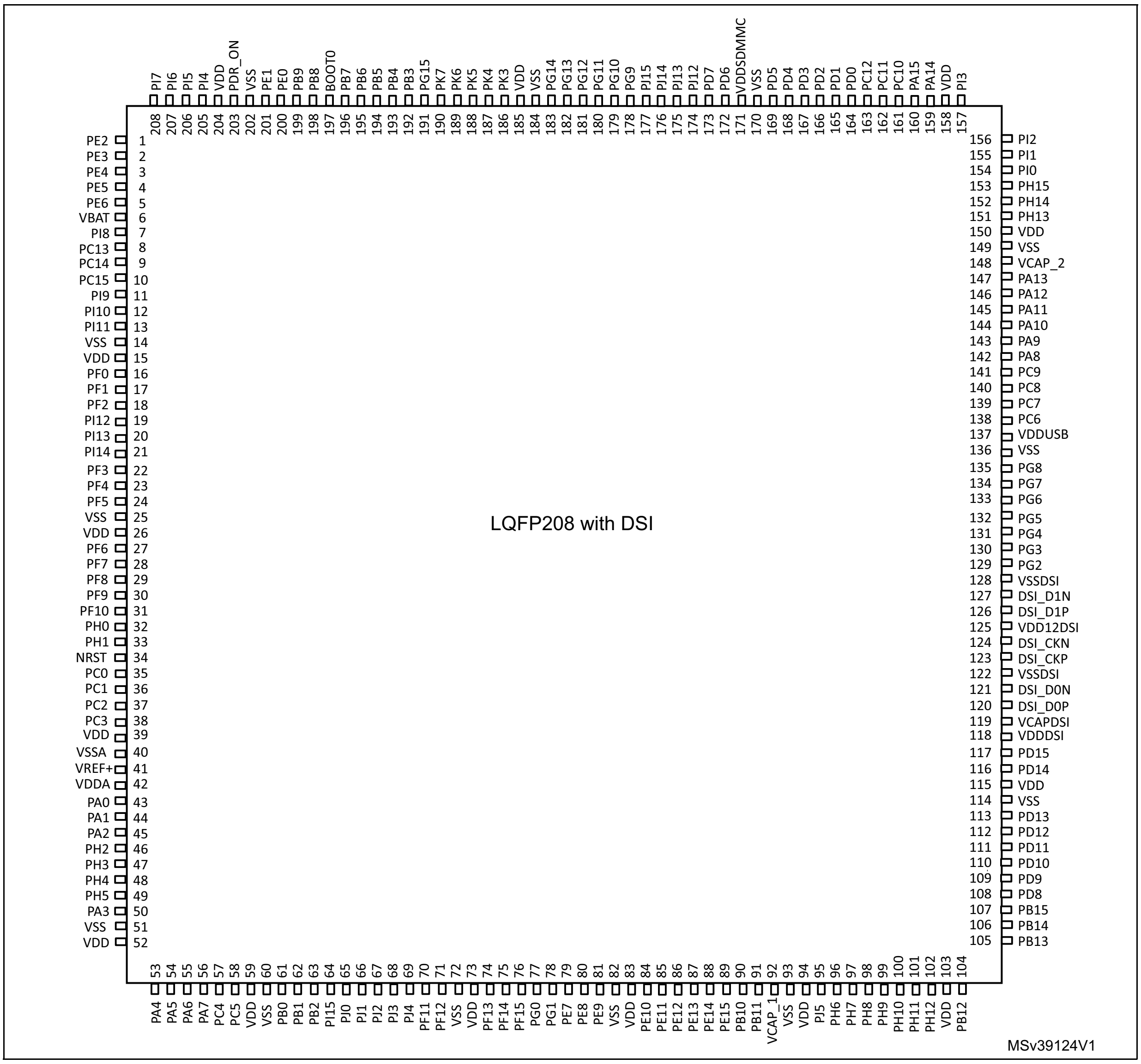
1. NC ball must not be connected to GND nor too VDD.
2. The above figure shows the package top view.

Figure 14. STM32F767xx LQFP208 pinout



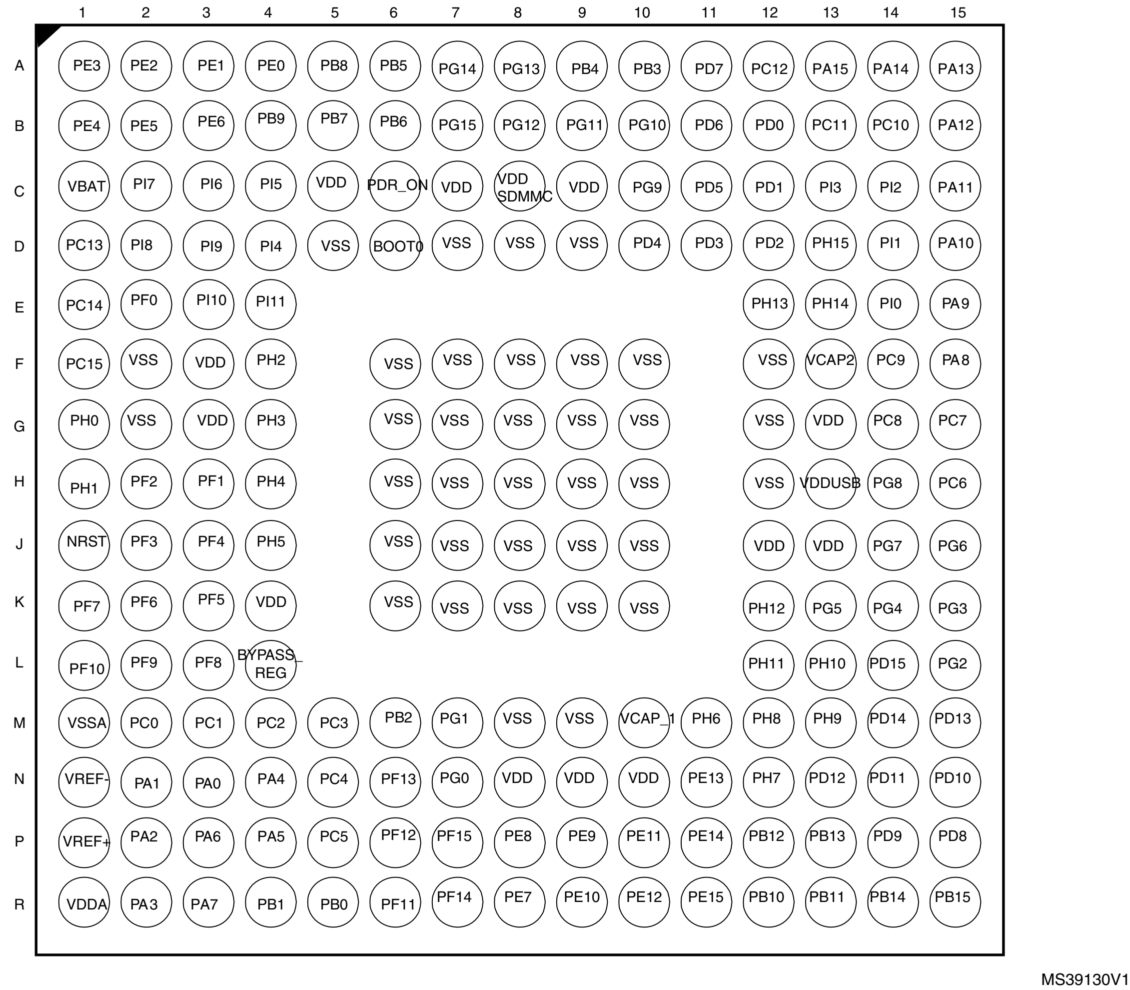
1. The above figure shows the package top view.

Figure 15. STM32F769xx LQFP208 pinout



1. The above figure shows the package top view.

Figure 16. STM32F767xx UFBGA176 ballout



1. The above figure shows the package top view.

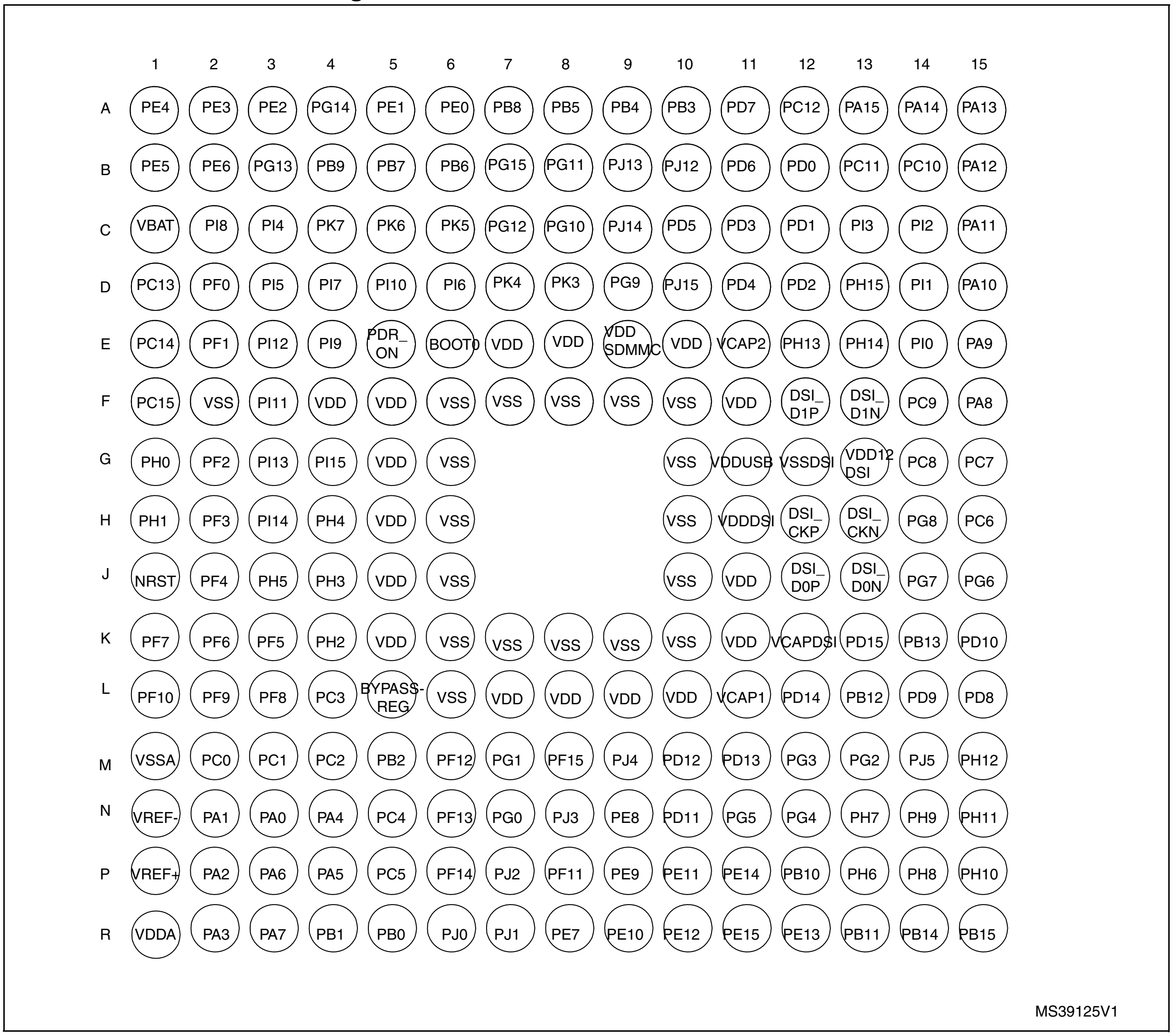
Figure 17. STM32F767xx TFBGA216 ballout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	PE4	PE3	PE2	PG14	PE1	PE0	PB8	PB5	PB4	PB3	PD7	PC12	PA15	PA14	PA13
B	PE5	PE6	PG13	PB9	PB7	PB6	PG15	PG11	PJ13	PJ12	PD6	PD0	PC11	PC10	PA12
C	VBAT	PI8	PI4	PK7	PK6	PK5	PG12	PG10	PJ14	PD5	PD3	PD1	PI3	PI2	PA11
D	PC13	PF0	PI5	PI7	PI10	PI6	PK4	PK3	PG9	PJ15	PD4	PD2	PH15	PI1	PA10
E	PC14	PF1	PI12	PI9	PDR_ ON	BOOT0	VDD	VDD	VDD SDMMC	VDD	VCAP2	PH13	PH14	PI0	PA9
F	PC15	VSS	PI11	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VDD	PK1	PK2	PC9	PA8
G	PH0	PF2	PI13	PI15	VDD	VSS				VSS	VDDUSB	PJ11	PK0	PC8	PC7
H	PH1	PF3	PI14	PH4	VDD	VSS				VSS	VDD	PJ8	PJ10	PG8	PC6
J	NRST	PF4	PH5	PH3	VDD	VSS				VSS	VDD	PJ7	PJ9	PG7	PG6
K	PF7	PF6	PF5	PH2	VDD	VSS	VSS	VSS	VSS	VSS	VDD	PJ6	PD15	PB13	PD10
L	PF10	PF9	PF8	PC3	BYPASS-REG	VSS	VDD	VDD	VDD	VDD	VCAP1	PD14	PB12	PD9	PD8
M	VSSA	PC0	PC1	PC2	PB2	PF12	PG1	PF15	PJ4	PD12	PD13	PG3	PG2	PJ5	PH12
N	VREF-	PA1	PA0	PA4	PC4	PF13	PG0	PJ3	PE8	PD11	PG5	PG4	PH7	PH9	PH11
P	VREF+	PA2	PA6	PA5	PC5	PF14	PJ2	PF11	PE9	PE11	PE14	PB10	PH6	PH8	PH10
R	VDDA	PA3	PA7	PB1	PB0	PJ0	PJ1	PE7	PE10	PE12	PE15	PE13	PB11	PB14	PB15

MS39129V1

1. The above figure shows the package top view.

Figure 18. STM32F769xx TFBGA216 ballout



1. The above figure shows the package top view.

Table 9. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	TTa	3.3 V tolerant I/O directly connected to ADC
	B	Dedicated BOOT pin
	RST	Bidirectional reset pin with weak pull-up resistor
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Alternate functions	Functions selected through GPIOx_AFR registers	
Additional functions	Functions directly selected/enabled through peripheral registers	

Table 10. STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180	LQFP176	LQFP208	TFBGA216						
1	1	A2	1	1	A3	E10	1	1	A3	PE2	I/O	FT	-	TRACECLK, SPI4_SCK, SAI1_MCLK_A, QUADSPI_BK1_IO2, ETH_MII_TXD3, FMC_A23, EVENTOUT	-
2	2	A1	2	2	A2	F10	2	2	A2	PE3	I/O	FT	-	TRACED0, SAI1_SD_B, FMC_A19, EVENTOUT	-

Table 10. STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180	LQFP176	LQFP208	TFBGA216						
3	3	B1	3	3	A1	C12	3	3	A1	PE4	I/O	FT	-	TRACED1, SPI4_NSS, SAI1_FS_A, DFSDM_DATIN3, FMC_A20, DCMI_D4, LCD_B0, EVENTOUT	-
4	4	B2	4	4	B1	D12	4	4	B1	PE5	I/O	FT	-	TRACED2, TIM9_CH1, SPI4_MISO, SAI1_SCK_A, DFSDM_CKIN3, FMC_A21, DCMI_D6, LCD_G0, EVENTOUT	-
5	5	B3	5	5	B2	E11	5	5	B2	PE6	I/O	FT	-	TRACED3, TIM1_BKIN2, TIM9_CH2, SPI4_MOSI, SAI1_SD_A, SAI2_MCLK_B, FMC_A22, DCMI_D7, LCD_G1, EVENTOUT	-
-	-	-	-	-	G6	-	-	-	G6	VSS	S	-	-	-	-
-	-	-	-	-	F5	-	-	-	F5	VDD	S	-	-	-	-
6	6	C1	6	6	C1	C13	6	6	C1	VBAT	S	-	-	-	-
-	-	D2	7	7	C2	-	7	7	C2	PI8	I/O	FT	(1)	EVENTOUT	RTC_TAMP2/ RTC_TS/WKUP5
7	7	D1	8	8	D1	D13	8	8	D1	PC13	I/O	FT	(1)	EVENTOUT	RTC_TAMP1/ RTC_TS/ RTC_OUT/ WKUP4
8	8	E1	9	9	E1	E12	9	9	E1	PC14-OSC32_IN	I/O	FT	(1) (2)	EVENTOUT	OSC32_IN
9	9	F1	10	10	F1	E13	10	10	F1	PC15-OSC32_OUT	I/O	FT	(1) (2)	EVENTOUT	OSC32_OUT
-	-	-	-	-	G5	-	-	-	G5	VDD	S	-	-	-	-

Table 10. STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180	LQFP176	LQFP208	TFBGA216						
-	-	D3	11	11	E4	G10	11	11	E4	PI9	I/O	FT	-	UART4_RX, CAN1_RX, FMC_D30, LCD_VSYNC, EVENTOUT	-
-	-	E3	12	12	D5	H10	12	12	D5	PI10	I/O	FT	-	ETH_MII_RX_ER, FMC_D31, LCD_HSYNC, EVENTOUT	-
-	-	E4	13	13	F3	F11	13	13	F3	PI11	I/O	FT	-	LCD_G6, OTG_HS_ULPI_DIR, EVENTOUT	WKUP6
-	-	F2	14	14	F2	F13	14	14	F2	VSS	S	-	-	-	-
-	-	F3	15	15	F4	F12	15	15	F4	VDD	S	-	-	-	-
-	10	E2	16	16	D2	G11	16	16	D2	PF0	I/O	FT	-	I2C2_SDA, FMC_A0, EVENTOUT	-
-	11	H3	17	17	E2	G12	17	17	E2	PF1	I/O	FT	-	I2C2_SCL, FMC_A1, EVENTOUT	-
-	12	H2	18	18	G2	G13	18	18	G2	PF2	I/O	FT	-	I2C2_SMBA, FMC_A2, EVENTOUT	-
-	-	-	-	19	E3	-	-	19	E3	PI12	I/O	FT	-	LCD_HSYNC, EVENTOUT	-
-	-	-	-	20	G3	-	-	20	G3	PI13	I/O	FT	-	LCD_VSYNC, EVENTOUT	-
-	-	-	-	21	H3	-	-	21	H3	PI14	I/O	FT	-	LCD_CLK, EVENTOUT	-
-	13	J2	19	22	H2	H11	19	22	H2	PF3	I/O	FT	-	FMC_A3, EVENTOUT	ADC3_IN9
-	14	J3	20	23	J2	H12	20	23	J2	PF4	I/O	FT	-	FMC_A4, EVENTOUT	ADC3_IN14
-	15	K3	21	24	K3	H13	21	24	K3	PF5	I/O	FT	-	FMC_A5, EVENTOUT	ADC3_IN15
10	16	G2	22	25	H6	J13	22	25	H6	VSS	S	-	-	-	-
11	17	G3	23	26	H5	J12	23	26	H5	VDD	S	-	-	-	-
-	18	K2	24	27	K2	-	24	27	K2	PF6	I/O	FT	-	TIM10_CH1, SPI5_NSS, SAI1_SD_B, UART7_RX, QUADSPI_BK1_IO3, EVENTOUT	ADC3_IN4

Table 10. STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180	LQFP176	LQFP208	TFBGA216						
-	19	K1	25	28	K1	-	25	28	K1	PF7	I/O	FT	-	TIM11_CH1, SPI5_SCK, SAI1_MCLK_B, UART7_TX, QUADSPI_BK1_IO2, EVENTOUT	ADC3_IN5
-	20	L3	26	29	L3	-	26	29	L3	PF8	I/O	FT	-	SPI5_MISO, SAI1_SCK_B, UART7_RTS, TIM13_CH1, QUADSPI_BK1_IO0, EVENTOUT	ADC3_IN6
-	21	L2	27	30	L2	-	27	30	L2	PF9	I/O	FT	-	SPI5_MOSI, SAI1_FS_B, UART7_CTS, TIM14_CH1, QUADSPI_BK1_IO1, EVENTOUT	ADC3_IN7
-	22	L1	28	31	L1	K11	28	31	L1	PF10	I/O	FT	-	QUADSPI_CLK, DCMI_D11, LCD_DE, EVENTOUT	ADC3_IN8
12	23	G1	29	32	G1	K12	29	32	G1	PH0-OSC_IN	I/O	FT	(2)	EVENTOUT	OSC_IN
13	24	H1	30	33	H1	K13	30	33	H1	PH1-OSC_OUT	I/O	FT	(2)	EVENTOUT	OSC_OUT
14	25	J1	31	34	J1	L11	31	34	J1	NRST	I/O	RST	-	-	-
15	26	M2	32	35	M2	L12	32	35	M2	PC0	I/O	FT	-	DFSDM_CKIN0, DFSDM_DATIN4, SAI2_FS_B, OTG_HS_ULPI_STP, FMC_SDNWE, LCD_R5, EVENTOUT	ADC1_IN10, ADC2_IN10, ADC3_IN10
16	27	M3	33	36	M3	L13	33	36	M3	PC1	I/O	FT	-	TRACED0, DFSDM_DATIN0, SPI2_MOSI/I2S2_SD, SAI1_SD_A, DFSDM_CKIN4, ETH_MDC, MDIOS_MDC, EVENTOUT	ADC1_IN11, ADC2_IN11, ADC3_IN11, RTC_TAMP3/WKUP3

Table 10. STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180	LQFP176	LQFP208	TFBGA216						
17	28	M4	34	37	M4	-	34	37	M4	PC2	I/O	FT	-	DFSDM_CKIN1, SPI2_MISO, DFSDM_CKOUT, OTG_HS_ULPI_DIR, ETH_MII_TXD2, FMC_SDNE0, EVENTOUT	ADC1_IN12, ADC2_IN12, ADC3_IN12
18	29	M5	35	38	L4	-	35	38	L4	PC3	I/O	FT	-	DFSDM_DATIN1, SPI2_MOSI/I2S2_SD, OTG_HS_ULPI_NXT, ETH_MII_TX_CLK, FMC_SDCKE0, EVENTOUT	ADC1_IN13, ADC2_IN13, ADC3_IN13
-	30	-	36	39	J5	-	36	39	J5	VDD	S	-	-	-	-
-	-	-	-	-	J6	-	-	-	J6	VSS	S	-	-	-	-
19	31	M1	37	40	M1	M11	37	40	M1	VSSA	S	-	-	-	-
-	-	N1	-	-	N1	-	-	-	N1	VREF-	S	-	-	-	-
20	32	P1	38	41	P1	-	38	41	P1	VREF+	S	-	-	-	-
21	33	R1	39	42	R1	M12	39	42	R1	VDDA	S	-	-	-	-
22	34	N3	40	43	N3	M13	40	43	N3	PA0-WKUP	I/O	FT	(3)	TIM2_CH1/TIM2_ETR, TIM5_CH1, TIM8_ETR, USART2_CTS, UART4_TX, SAI2_SD_B, ETH_MII_CRS, EVENTOUT	ADC1_IN0, ADC2_IN0, ADC3_IN0, WKUP1
23	35	N2	41	44	N2	J11	41	44	N2	PA1	I/O	FT	-	TIM2_CH2, TIM5_CH2, USART2_RTS, UART4_RX, QUADSPI_BK1_IO3, SAI2_MCLK_B, ETH_MII_RX_CLK/ETH_RMII_REF_CLK, LCD_R2, EVENTOUT	ADC1_IN1, ADC2_IN1, ADC3_IN1

Table 10. STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180	LQFP176	LQFP208	TFBGA216						
24	36	P2	42	45	P2	J10	42	45	P2	PA2	I/O	FT	-	TIM2_CH3, TIM5_CH3, TIM9_CH1, USART2_TX, SAI2_SCK_B, ETH_MDIO, MDIOS_MDIO, LCD_R1, EVENTOUT	ADC1_IN2, ADC2_IN2, ADC3_IN2, WKUP2
-	-	F4	43	46	K4	L10	43	46	K4	PH2	I/O	FT	-	LPTIM1_IN2, QUADSPI_BK2_IO0, SAI2_SCK_B, ETH_MII_CRS, FMC_SDCKE0, LCD_R0, EVENTOUT	-
-	-	G4	44	47	J4	K10	44	47	J4	PH3	I/O	FT	-	QUADSPI_BK2_IO1, SAI2_MCLK_B, ETH_MII_COL, FMC_SDNE0, LCD_R1, EVENTOUT	-
-	-	H4	45	48	H4	N12	45	48	H4	PH4	I/O	FT	-	I2C2_SCL, LCD_G5, OTG_HS_ULPI_NXT, LCD_G4, EVENTOUT	-
-	-	J4	46	49	J3	N11	46	49	J3	PH5	I/O	FT	-	I2C2_SDA, SPI5_NSS, FMC_SDNWE, EVENTOUT	-
25	37	R2	47	50	R2	M10	47	50	R2	PA3	I/O	FT	-	TIM2_CH4, TIM5_CH4, TIM9_CH2, USART2_RX, LCD_B2, OTG_HS_ULPI_D0, ETH_MII_COL, LCD_B5, EVENTOUT	ADC1_IN3, ADC2_IN3, ADC3_IN3
26	38	-	-	51	K6	J9	-	51	K6	VSS	S	-	-	-	-
-	-	L4	48	-	L5	-(4)	48	-	L5	BYPASS_REG	I	FT	-	-	-
27	39	K4	49	52	K5	K9	49	52	K5	VDD	S	-	-	-	-

Table 10. STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180	LQFP176	LQFP208	TFBGA216						
28	40	N4	50	53	N4	L9	50	53	N4	PA4	I/O	TTa	-	SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, SPI6_NSS, OTG_HS_SOF, DCMI_HSYNC, LCD_VSYNC, EVENTOUT	ADC1_IN4, ADC2_IN4, DAC_OUT1
29	41	P4	51	54	P4	P11	51	54	P4	PA5	I/O	TTa	-	TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK/I2S1_CK, SPI6_SCK, OTG_HS_ULPI_CK, LCD_R4, EVENTOUT	ADC1_IN5, ADC2_IN5, DAC_OUT2
30	42	P3	52	55	P3	N10	52	55	P3	PA6	I/O	FT	-	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO, SPI6_MISO, TIM13_CH1, MDIOS_MDC, DCMI_PIXCLK, LCD_G2, EVENTOUT	ADC1_IN6, ADC2_IN6
31	43	R3	53	56	R3	M9	53	56	R3	PA7	I/O	FT	-	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI/I2S1_SD, SPI6_MOSI, TIM14_CH1, ETH_MII_RX_DV/ETH_RMII_CRS_DV, FMC_SDNWE, EVENTOUT	ADC1_IN7, ADC2_IN7
32	44	N5	54	57	N5	-	54	57	N5	PC4	I/O	FT	-	DFSDM_CKIN2, I2S1_MCK, SPDIF_RX2, ETH_MII_RXD0/ETH_RMII_RXD0, FMC_SDNE0, EVENTOUT	ADC1_IN14, ADC2_IN14
33	45	P5	55	58	P5	-	55	58	P5	PC5	I/O	FT	-	DFSDM_DATIN2, SPDIF_RX3, ETH_MII_RXD1/ETH_RMII_RXD1, FMC_SDCKE0, EVENTOUT	ADC1_IN15, ADC2_IN15
-	-	-	-	59	L7	-	-	59	L7	VDD	S	-	-	-	-

Table 10. STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180	LQFP176	LQFP208	TFBGA216						
-	-	-	-	60	L6	-	-	60	L6	VSS	S	-	-	-	-
34	46	R5	56	61	R5	P10	56	61	R5	PB0	I/O	FT	-	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, DFSDM_CKOUT, UART4_CTS, LCD_R3, OTG_HS_ULPI_D1, ETH_MII_RXD2, LCD_G1, EVENTOUT	ADC1_IN8, ADC2_IN8
35	47	R4	57	62	R4	J8	57	62	R4	PB1	I/O	FT	-	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, DFSDM_DATIN1, LCD_R6, OTG_HS_ULPI_D2, ETH_MII_RXD3, LCD_G0, EVENTOUT	ADC1_IN9, ADC2_IN9
36	48	M6	58	63	M5	J7	58	63	M5	PB2	I/O	FT	-	SAI1_SD_A, SPI3_MOSI/I2S3_SD, QUADSPI_CLK, DFSDM_CKIN1, EVENTOUT	-
-	-	-	-	64	G4	-	-	64	G4	PI15	I/O	FT	-	LCD_G2, LCD_R0, EVENTOUT	-
-	-	-	-	65	R6	-	-	65	R6	PJ0	I/O	FT	-	LCD_R7, LCD_R1, EVENTOUT	-
-	-	-	-	66	R7	-	-	66	R7	PJ1	I/O	FT	-	LCD_R2, EVENTOUT	-
-	-	-	-	67	P7	-	-	67	P7	PJ2	I/O	FT	-	DSI_TE, LCD_R3, EVENTOUT	-
-	-	-	-	68	N8	-	-	68	N8	PJ3	I/O	FT	-	LCD_R4, EVENTOUT	-
-	-	-	-	69	M9	-	-	69	M9	PJ4	I/O	FT	-	LCD_R5, EVENTOUT	-
-	49	R6	59	70	P8	N9	59	70	P8	PF11	I/O	FT	-	SPI5_MOSI, SAI2_SD_B, FMC_SDNRAS, DCMI_D12, EVENTOUT	-
-	50	P6	60	71	M6	K7	60	71	M6	PF12	I/O	FT	-	FMC_A6, EVENTOUT	-
-	51	M8	61	72	K7	P9	61	72	K7	VSS	S		-	-	-
-	52	N8	62	73	L8	M8	62	73	L8	VDD	S		-	-	-

Table 10. STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180	LQFP176	LQFP208	TFBGA216						
-	53	N6	63	74	N6	L8	63	74	N6	PF13	I/O	FT	-	I2C4_SMBA, DFSDM_DATIN6, FMC_A7, EVENTOUT	-
-	54	R7	64	75	P6	K8	64	75	P6	PF14	I/O	FT	-	I2C4_SCL, DFSDM_CKIN6, FMC_A8, EVENTOUT	-
-	55	P7	65	76	M8	P8	65	76	M8	PF15	I/O	FT	-	I2C4_SDA, FMC_A9, EVENTOUT	-
-	56	N7	66	77	N7	N8	66	77	N7	PG0	I/O	FT	-	FMC_A10, EVENTOUT	-
-	57	M7	67	78	M7	L7	67	78	M7	PG1	I/O	FT	-	FMC_A11, EVENTOUT	-
37	58	R8	68	79	R8	M7	68	79	R8	PE7	I/O	FT	-	TIM1_ETR, DFSDM_DATIN2, UART7_RX, QUADSPI_BK2_IO0, FMC_D4, EVENTOUT	-
38	59	P8	69	80	N9	N7	69	80	N9	PE8	I/O	FT	-	TIM1_CH1N, DFSDM_CKIN2, UART7_TX, QUADSPI_BK2_IO1, FMC_D5, EVENTOUT	-
39	60	P9	70	81	P9	P7	70	81	P9	PE9	I/O	FT	-	TIM1_CH1, DFSDM_CKOUT, UART7_RTS, QUADSPI_BK2_IO2, FMC_D6, EVENTOUT	-
-	61	M9	71	82	K8	-	71	82	K8	VSS	S	-	-	-	-
-	62	N9	72	83	L9	-	72	83	L9	VDD	S	-	-	-	-
40	63	R9	73	84	R9	J6	73	84	R9	PE10	I/O	FT	-	TIM1_CH2N, DFSDM_DATIN4, UART7_CTS, QUADSPI_BK2_IO3, FMC_D7, EVENTOUT	-

Table 10. STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180	LQFP176	LQFP208	TFBGA216						
41	64	P10	74	85	P10	K6	74	85	P10	PE11	I/O	FT	-	TIM1_CH2, SPI4_NSS, DFSDM_CKIN4, SAI2_SD_B, FMC_D8, LCD_G3, EVENTOUT	-
42	65	R10	75	86	R10	L6	75	86	R10	PE12	I/O	FT	-	TIM1_CH3N, SPI4_SCK, DFSDM_DATIN5, SAI2_SCK_B, FMC_D9, LCD_B4, EVENTOUT	-
43	66	N11	76	87	R12	P6	76	87	R12	PE13	I/O	FT	-	TIM1_CH3, SPI4_MISO, DFSDM_CKIN5, SAI2_FS_B, FMC_D10, LCD_DE, EVENTOUT	-
44	67	P11	77	88	P11	N6	77	88	P11	PE14	I/O	FT	-	TIM1_CH4, SPI4_MOSI, SAI2_MCLK_B, FMC_D11, LCD_CLK, EVENTOUT	-
45	68	R11	78	89	R11	M6	78	89	R11	PE15	I/O	FT	-	TIM1_BKIN, FMC_D12, LCD_R7, EVENTOUT	-
46	69	R12	79	90	P12	K5	79	90	P12	PB10	I/O	FT	-	TIM2_CH3, I2C2_SCL, SPI2_SCK/I2S2_CK, DFSDM_DATIN7, USART3_TX, QUADSPI_BK1_NCS, OTG_HS_ULPI_D3, ETH_MII_RX_ER, LCD_G4, EVENTOUT	-
47	70	R13	80	91	R13	L5	80	91	R13	PB11	I/O	FT	-	TIM2_CH4, I2C2_SDA, DFSDM_CKIN7, USART3_RX, OTG_HS_ULPI_D4, ETH_MII_TX_EN/ETH_RMII_TX_EN, DSI_TE, LCD_G5, EVENTOUT	-
48	71	M10	81	92	L11	P5	81	92	L11	VCAP_1	S	-	-	-	-
49	-	-	-	93	K9	N5	-	93	K9	VSS	S	-	-	-	-
50	72	N10	82	94	L10	P4	82	94	L10	VDD	S	-	-	-	-

Table 10. STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180	LQFP176	LQFP208	TFBGA216						
-	-	-	-	95	M14	-	-	95	M14	PJ5	I/O	FT	-	LCD_R6, EVENTOUT	-
-	-	M11	83	96	P13	-	83	96	P13	PH6	I/O	FT	-	I2C2_SMBA, SPI5_SCK, TIM12_CH1, ETH_MII_RXD2, FMC_SDNE1, DCMI_D8, EVENTOUT	-
-	-	N12	84	97	N13	-	84	97	N13	PH7	I/O	FT	-	I2C3_SCL, SPI5_MISO, ETH_MII_RXD3, FMC_SDCKE1, DCMI_D9, EVENTOUT	-
-	-	M12	85	98	P14	M5	-	98	P14	PH8	I/O	FT	-	I2C3_SDA, FMC_D16, DCMI_HSYNC, LCD_R2, EVENTOUT	-
-	-	M13	86	99	N14	K4	-	99	N14	PH9	I/O	FT	-	I2C3_SMBA, TIM12_CH2, FMC_D17, DCMI_D0, LCD_R3, EVENTOUT	-
-	-	L13	87	100	P15	L4	-	100	P15	PH10	I/O	FT	-	TIM5_CH1, I2C4_SMBA, FMC_D18, DCMI_D1, LCD_R4, EVENTOUT	-
-	-	L12	88	101	N15	M4	-	101	N15	PH11	I/O	FT	-	TIM5_CH2, I2C4_SCL, FMC_D19, DCMI_D2, LCD_R5, EVENTOUT	-
-	-	K12	89	102	M15	P3	-	102	M15	PH12	I/O	FT	-	TIM5_CH3, I2C4_SDA, FMC_D20, DCMI_D3, LCD_R6, EVENTOUT	-
-	-	H12	90	-	K10	N4	-	-	K10	VSS	S		-	-	-
-	-	J12	91	103	K11	-	-	103	K11	VDD	S		-	-	-

Table 10. STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180	LQFP176	LQFP208	TFBGA216						
51	73	P12	92	104	L13	H8	85	104	L13	PB12	I/O	FT	-	TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, DFSDM_DATIN1, USART3_CK, UART5_RX, CAN2_RX, OTG_HS_ULPI_D5, ETH_MII_TXD0/ETH_RMII_TXD0, OTG_HS_ID, EVENTOUT	-
52	74	P13	93	105	K14	J5	86	105	K14	PB13	I/O	FT	-	TIM1_CH1N, SPI2_SCK/I2S2_CK, DFSDM_CKIN1, USART3_CTS, UART5_TX, CAN2_TX, OTG_HS_ULPI_D6, ETH_MII_TXD1/ETH_RMII_TXD1, EVENTOUT	OTG_HS_VBUS
53	75	R14	94	106	R14	N3	87	106	R14	PB14	I/O	FT	-	TIM1_CH2N, TIM8_CH2N, USART1_TX, SPI2_MISO, DFSDM_DATIN2, USART3_RTS, UART4_RTS, TIM12_CH1, SDMMC2_D0, OTG_HS_DM, EVENTOUT	-
54	76	R15	95	107	R15	N2	88	107	R15	PB15	I/O	FT	-	RTC_REFIN, TIM1_CH3N, TIM8_CH3N, USART1_RX, SPI2_MOSI/I2S2_SD, DFSDM_CKIN2, UART4_CTS, TIM12_CH2, SDMMC2_D1, OTG_HS_DP, EVENTOUT	-
55	77	P15	96	108	L15	M3	89	108	L15	PD8	I/O	FT	-	DFSDM_CKIN3, USART3_TX, SPDIF_RX1, FMC_D13, EVENTOUT	-
56	78	P14	97	109	L14	L3	90	109	L14	PD9	I/O	FT	-	DFSDM_DATIN3, USART3_RX, FMC_D14, EVENTOUT	-

Table 10. STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180	LQFP176	LQFP208	TFBGA216						
57	79	N15	98	110	K15	M2	91	110	K15	PD10	I/O	FT	-	DFSDM_CKOUT, USART3_CK, FMC_D15, LCD_B3, EVENTOUT	-
58	80	N14	99	111	N10	K3	92	111	N10	PD11	I/O	FT	-	I2C4_SMBA, USART3_CTS, QUADSPI_BK1_IO0, SAI2_SD_A, FMC_A16/FMC_CLE, EVENTOUT	-
59	81	N13	100	112	M10	J4	93	112	M10	PD12	I/O	FT	-	TIM4_CH1, LPTIM1_IN1, I2C4_SCL, USART3_RTS, QUADSPI_BK1_IO1, SAI2_FS_A, FMC_A17/FMC_ALE, EVENTOUT	-
60	82	M15	101	113	M11	L2	94	113	M11	PD13	I/O	FT	-	TIM4_CH2, LPTIM1_OUT, I2C4_SDA, QUADSPI_BK1_IO3, SAI2_SCK_A, FMC_A18, EVENTOUT	-
-	83	-	102	114	J10	M1	95	114	J10	VSS	S		-	-	-
-	84	J13	103	115	J11	-	96	115	J11	VDD	S		-	-	-
61	85	M14	104	116	L12	L1	97	116	L12	PD14	I/O	FT	-	TIM4_CH3, UART8_CTS, FMC_D0, EVENTOUT	-
62	86	L14	105	117	K13	K2	98	117	K13	PD15	I/O	FT	-	TIM4_CH4, UART8_RTS, FMC_D1, EVENTOUT	-
-	-	-	-	118	K12	-	-	-	-	PJ6	I/O	FT	-	LCD_R7, EVENTOUT	-
-	-	-	-	119	J12	-	-	-	-	PJ7	I/O	FT	-	LCD_G0, EVENTOUT	-
-	-	-	-	120	H12	-	-	-	-	PJ8	I/O	FT	-	LCD_G1, EVENTOUT	-
-	-	-	-	121	J13	-	-	-	-	PJ9	I/O	FT	-	LCD_G2, EVENTOUT	-
-	-	-	-	122	H13	-	-	-	-	PJ10	I/O	FT	-	LCD_G3, EVENTOUT	-
-	-	-	-	123	G12	-	-	-	-	PJ11	I/O	FT	-	LCD_G4, EVENTOUT	-

Table 10. STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180	LQFP176	LQFP208	TFBGA216						
-	-	-	-	124	H11	-	-	-	-	VDD	S	-	-	-	-
-	-	-	-	-	-	K1	99	118	H11	VDDDSI	S	-	-	-	-
-	-	-	-	125	H10	-	-	-	H10	VSS	S	-	-	-	-
-	-	-	-	-	-	H6	100	119	K12	VCAPDSI	S	-	-	-	-
-	-	-	-	-	-	J3	-	-	G13	VDD12DSI	S	-	-	-	-
-	-	-	-	-	-	J1	101	120	J12	DSI_D0P	A	-	-	-	-
-	-	-	-	-	-	J2	102	121	J13	DSI_D0N	A	-	-	-	-
-	-	-	-	-	-	H5	103	122	G12	VSSDSI	S	-	-	-	-
-	-	-	-	-	-	H4	104	123	H12	DSI_CKP	A	-	-	-	-
-	-	-	-	-	-	H3	105	124	H13	DSI_CKN	A	-	-	-	-
-	-	-	-	-	-	-	106	125	-	VDD12DSI	S			-	-
-	-	-	-	-	-	H1	107	126	F12	DSI_D1P	A		-	-	-
-	-	-	-	-	-	H2	108	127	F13	DSI_D1N	A		-	-	-
-	-	-	-	-	-	-	109	128	-	VSSDSI	S		-	-	-
-	-	-	-	126	G13	-	-	-	-	PK0	I/O	FT	-	LCD_G5, EVENTOUT	-
-	-	-	-	127	F12	-	-	-	-	PK1	I/O	FT	-	LCD_G6, EVENTOUT	-
-	-	-	-	128	F13	-	-	-	-	PK2	I/O	FT	-	LCD_G7, EVENTOUT	-
-	87	L15	106	129	M13	H9	110	129	M13	PG2	I/O	FT	-	FMC_A12, EVENTOUT	-
-	88	K15	107	130	M12	G9	111	130	M12	PG3	I/O	FT	-	FMC_A13, EVENTOUT	-
-	89	K14	108	131	N12	G1	112	131	N12	PG4	I/O	FT	-	FMC_A14/FMC_BA0, EVENTOUT	-
-	90	K13	109	132	N11	G2	113	132	N11	PG5	I/O	FT	-	FMC_A15/FMC_BA1, EVENTOUT	-

Table 10. STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180	LQFP176	LQFP208	TFBGA216						
-	91	J15	110	133	J15	G3	114	133	J15	PG6	I/O	FT	-	FMC_NE3, DCMI_D12, LCD_R7, EVENTOUT	-
-	92	J14	111	134	J14	G4	115	134	J14	PG7	I/O	FT	-	SAI1_MCLK_A, USART6_CK, FMC_INT, DCMI_D13, LCD_CLK, EVENTOUT	-
-	93	H14	112	135	H14	G5	116	135	H14	PG8	I/O	FT	-	SPI6_NSS, SPDIF_RX2, USART6_RTS, ETH_PPS_OUT, FMC_SDCLK, LCD_G7, EVENTOUT	-
-	94	G12	113	136	G10	F1	117	136	G10	VSS	S		-	-	-
-	95	H13	114	137	G11	F2	118	137	G11	VDDUSB	S		-	-	-
63	96	H15	115	138	H15	G6	119	138	H15	PC6	I/O	FT	-	TIM3_CH1, TIM8_CH1, I2S2_MCK, DFSDM_CKIN3, USART6_TX, FMC_NWAIT, SDMMC2_D6, SDMMC1_D6, DCMI_D0, LCD_HSYNC, EVENTOUT	-
64	97	G15	116	139	G15	F3	120	139	G15	PC7	I/O	FT	-	TIM3_CH2, TIM8_CH2, I2S3_MCK, DFSDM_DATIN3, USART6_RX, FMC_NE1, SDMMC2_D7, SDMMC1_D7, DCMI_D1, LCD_G6, EVENTOUT	-
65	98	G14	117	140	G14	G8	121	140	G14	PC8	I/O	FT	-	TRACED1, TIM3_CH3, TIM8_CH3, UART5_RTS, USART6_CK, FMC_NE2/FMC_NCE, SDMMC1_D0, DCMI_D2, EVENTOUT	

Table 10. STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180	LQFP176	LQFP208	TFBGA216						
66	99	F14	118	141	F14	E1	122	141	F14	PC9	I/O	FT	-	MCO2, TIM3_CH4, TIM8_CH4, I2C3_SDA, I2S_CKIN, UART5_CTS, QUADSPI_BK1_IO0, LCD_G3, SDMMC1_D1, DCMI_D3, LCD_B2, EVENTOUT	--
67	100	F15	119	142	F15	E2	123	142	F15	PA8	I/O	FT	-	MCO1, TIM1_CH1, TIM8_BKIN2, I2C3_SCL, USART1_CK, OTG_FS_SOF, CAN3_RX, UART7_RX, LCD_B3, LCD_R6, EVENTOUT	-
68	101	E15	120	143	E15	F4	124	143	E15	PA9	I/O	FT	-	TIM1_CH2, I2C3_SMBA, SPI2_SCK/I2S2_CK, USART1_TX, DCMI_D0, LCD_R5, EVENTOUT	OTG_FS_VBUS
69	102	D15	121	144	D15	F5	125	144	D15	PA10	I/O	FT	-	TIM1_CH3, USART1_RX, LCD_B4, OTG_FS_ID, MDIOS_MDIO, DCMI_D1, LCD_B1, EVENTOUT	-
70	103	C15	122	145	C15	E3	126	145	C15	PA11	I/O	FT	-	TIM1_CH4, SPI2_NSS/I2S2_WS, UART4_RX, USART1_CTS, CAN1_RX, OTG_FS_DM, LCD_R4, EVENTOUT	-
71	104	B15	123	146	B15	D1	127	146	B15	PA12	I/O	FT	-	TIM1_ETR, SPI2_SCK/I2S2_CK, UART4_TX, USART1_RTS, SAI2_FS_B, CAN1_TX, OTG_FS_DP, LCD_R5, EVENTOUT	-
72	105	A15	124	147	A15	D2	128	147	A15	PA13(JTMS-SWDIO)	I/O	FT	-	JTMS-SWDIO, EVENTOUT	-

Table 10. STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180	LQFP176	LQFP208	TFBGA216						
73	106	F13	125	148	E11	C1	129	148	E11	VCAP_2	S	-	-	-	-
74	107	F12	126	149	F10	C2	130	149	F10	VSS	S	-	-	-	-
75	108	G13	127	150	F11	B2	131	150	F11	VDD	S	-	-	-	-
-	-	E12	128	151	E12	F6	-	151	E12	PH13	I/O	FT	-	TIM8_CH1N, UART4_TX, CAN1_TX, FMC_D21, LCD_G2, EVENTOUT	-
-	-	E13	129	152	E13	F7	-	152	E13	PH14	I/O	FT	-	TIM8_CH2N, UART4_RX, CAN1_RX, FMC_D22, DCMI_D4, LCD_G3, EVENTOUT	-
-	-	D13	130	153	D13	E5	-	153	D13	PH15	I/O	FT	-	TIM8_CH3N, FMC_D23, DCMI_D11, LCD_G4, EVENTOUT	-
-	-	E14	131	154	E14	E4	132	154	E14	PI0	I/O	FT	-	TIM5_CH4, SPI2_NSS/I2S2_WS, FMC_D24, DCMI_D13, LCD_G5, EVENTOUT	-
-	-	D14	132	155	D14	B3	133	155	D14	PI1	I/O	FT	-	TIM8_BKIN2, SPI2_SCK/I2S2_CK, FMC_D25, DCMI_D8, LCD_G6, EVENTOUT	-
-	-	C14	133	156	C14	C3	-	156	C14	PI2	I/O	FT	-	TIM8_CH4, SPI2_MISO, FMC_D26, DCMI_D9, LCD_G7, EVENTOUT	-
-	-	C13	134	157	C13	D3	134	157	C13	PI3	I/O	FT	-	TIM8_ETR, SPI2_MOSI/I2S2_SD, FMC_D27, DCMI_D10, EVENTOUT	-
-	-	D9	135	-	F9	-	135	-	F9	VSS	S	-	-	-	
-	-	C9	136	158	E10	-	136	158	E10	VDD	S	-	-	-	--

Table 10. STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180	LQFP176	LQFP208	TFBGA216						
76	109	A14	137	159	A14	A3	137	159	A14	PA14(JTCK-SWCLK)	I/O	FT	-	JTCK-SWCLK, EVENTOUT	-
77	110	A13	138	160	A13	F8	138	160	A13	PA15(JTDI)	I/O	FT	-	JTDI, TIM2_CH1/TIM2_ETR, HDMI_CEC, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, SPI6_NSS, UART4_RTS, CAN3_TX, UART7_TX, EVENTOUT	-
78	111	B14	139	161	B14	B4	139	161	B14	PC10	I/O	FT	-	DFSDM_CKIN5, SPI3_SCK/I2S3_CK, USART3_TX, UART4_TX, QUADSPI_BK1_IO1, SDMMC1_D2, DCMI_D8, LCD_R2, EVENTOUT	-
79	112	B13	140	162	B13	C4	140	162	B13	PC11	I/O	FT	-	DFSDM_DATIN5, SPI3_MISO, USART3_RX, UART4_RX, QUADSPI_BK2_NCS, SDMMC1_D3, DCMI_D4, EVENTOUT	-
80	113	A12	141	163	A12	D4	141	163	A12	PC12	I/O	FT	-	TRACED3, SPI3_MOSI/I2S3_SD, USART3_CK, UART5_TX, SDMMC1_CK, DCMI_D9, EVENTOUT	-
81	114	B12	142	164	B12	A4	142	164	B12	PD0	I/O	FT	-	DFSDM_CKIN6, DFSDM_DATIN7, UART4_RX, CAN1_RX, FMC_D2, EVENTOUT	-
82	115	C12	143	165	C12	D5	143	165	C12	PD1	I/O	FT	-	DFSDM_DATIN6, DFSDM_CKIN7, UART4_TX, CAN1_TX, FMC_D3, EVENTOUT	--

Table 10. STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180	LQFP176	LQFP208	TFBGA216						
83	116	D12	144	166	D12	D6	144	166	D12	PD2	I/O	FT	-	TRACED2, TIM3_ETR, UART5_RX, SDMMC1_CMD, DCMI_D11, EVENTOUT	-
84	117	D11	145	167	C11	B5	145	167	C11	PD3	I/O	FT	-	DFSDM_CKOUT, SPI2_SCK/I2S2_CK, DFSDM_DATIN0, USART2_CTS, FMC_CLK, DCMI_D5, LCD_G7, EVENTOUT	-
85	118	D10	146	168	D11	A5	146	168	D11	PD4	I/O	FT	-	DFSDM_CKIN0, USART2_RTS, FMC_NOE, EVENTOUT	-
86	119	C11	147	169	C10	C5	147	169	C10	PD5	I/O	FT	-	USART2_TX, FMC_NWE, EVENTOUT	-
-	120	D8	148	170	F8	B6	148	170	F8	VSS	S	-	-	-	-
-	121	C8	149	171	E9	A6	149	171	E9	VDDSDMMC	S	-	-	-	-
87	122	B11	150	172	B11	E6	150	172	B11	PD6	I/O	FT	-	DFSDM_CKIN4, SPI3_MOSI/I2S3_SD, SAI1_SD_A, USART2_RX, DFSDM_DATIN1, SDMMC2_CK, FMC_NWAIT, DCMI_D10, LCD_B2, EVENTOUT	-
88	123	A11	151	173	A11	E7	151	173	A11	PD7	I/O	FT	-	DFSDM_DATIN4, SPI1_MOSI/I2S1_SD, DFSDM_CKIN1, USART2_CK, SPDIF_RX0, SDMMC2_CMD, FMC_NE1, EVENTOUT	-
-	-	-	-	174	B10	-	-	174	B10	PJ12	I/O	FT	-	LCD_G3, LCD_B0, EVENTOUT	-
-	-	-	-	175	B9	-	-	175	B9	PJ13	I/O	FT	-	LCD_G4, LCD_B1, EVENTOUT	-

Table 10. STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180	LQFP176	LQFP208	TFBGA216						
-	-	-	-	176	C9	-	-	176	C9	PJ14	I/O	FT	-	LCD_B2, EVENTOUT	-
-	-	-	-	177	D10	-	-	177	D10	PJ15	I/O	FT	-	LCD_B3, EVENTOUT	-
-	124	C10	152	178	D9	C6	152	178	D9	PG9	I/O	FT	-	SPI1_MISO, SPDIF_RX3, USART6_RX, QUADSPI_BK2_IO2, SAI2_FS_B, SDMMC2_D0, FMC_NE2/FMC_NCE, DCMI_VSYNC, EVENTOUT	-
-	125	B10	153	179	C8	A7	153	179	C8	PG10	I/O	FT	-	SPI1_NSS/I2S1_WS, LCD_G3, SAI2_SD_B, SDMMC2_D1, FMC_NE3, DCMI_D2, LCD_B2, EVENTOUT	-
-	126	B9	154	180	B8	B7	154	180	B8	PG11	I/O	FT	-	SPI1_SCK/I2S1_CK, SPDIF_RX0, SDMMC2_D2, ETH_MII_TX_EN/ETH_RMII_TX_EN, DCMI_D3, LCD_B3, EVENTOUT	-
-	127	B8	155	181	C7	D7	155	181	C7	PG12	I/O	FT	-	LPTIM1_IN1, SPI6_MISO, SPDIF_RX1, USART6_RTS, LCD_B4, SDMMC2_D3, FMC_NE4, LCD_B1, EVENTOUT	-
-	128	A8	156	182	B3	C7	156	182	B3	PG13	I/O	FT	-	TRACED0, LPTIM1_OUT, SPI6_SCK, USART6_CTS, ETH_MII_TXD0/ETH_RMII_TXD0, FMC_A24, LCD_R0, EVENTOUT	-
-	129	A7	157	183	A4	-	157	183	A4	PG14	I/O	FT	-	TRACED1, LPTIM1_ETR, SPI6_MOSI, USART6_TX, QUADSPI_BK2_IO3, ETH_MII_TXD1/ETH_RMII_TXD1, FMC_A25, LCD_B0, EVENTOUT	-

Table 10. STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180	LQFP176	LQFP208	TFBGA216						
-	130	D7	158	184	F7	A8	158	184	F7	VSS	S	-	-	-	-
-	131	C7	159	185	E8	B8	159	185	E8	VDD	S	-	-	-	-
-	-	-	-	186	D8	-	-	186	D8	PK3	I/O	FT	-	LCD_B4, EVENTOUT	-
-	-	-	-	187	D7	-	-	187	D7	PK4	I/O	FT	-	LCD_B5, EVENTOUT	-
-	-	-	-	188	C6	-	-	188	C6	PK5	I/O	FT	-	LCD_B6, EVENTOUT	-
-	-	-	-	189	C5	-	-	189	C5	PK6	I/O	FT	-	LCD_B7, EVENTOUT	-
-	-	-	-	190	C4	-	-	190	C4	PK7	I/O	FT	-	LCD_DE, EVENTOUT	-
-	132	B7	160	191	B7	F9	160	191	B7	PG15	I/O	FT	-	USART6_CTS, FMC_SDNCAS, DCMI_D13, EVENTOUT	-
89	133	A10	161	192	A10	E8	161	192	A10	PB3 (JTDO/ TRACES WO)	I/O	FT	-	JTDO/TRACESWO, TIM2_CH2, SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, SPI6_SCK, SDMMC2_D2, CAN3_RX, UART7_RX, EVENTOUT	-
90	134	A9	162	193	A9	D8	162	193	A9	PB4(NJT RST)	I/O	FT	-	NJTRST, TIM3_CH1, SPI1_MISO, SPI3_MISO, SPI2_NSS/I2S2_WS, SPI6_MISO, SDMMC2_D3, CAN3_TX, UART7_TX, EVENTOUT	-
91	135	A6	163	194	A8	A9	163	194	A8	PB5	I/O	FT	-	UART5_RX, TIM3_CH2, I2C1_SMBA, SPI1_MOSI/I2S1_SD, SPI3_MOSI/I2S3_SD, SPI6_MOSI, CAN2_RX, OTG_HS_ULPI_D7, ETH_PPS_OUT, FMC_SDCKE1, DCMI_D10, LCD_G7, EVENTOUT	-

Table 10. STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180	LQFP176	LQFP208	TFBGA216						
92	136	B6	164	195	B6	B9	164	195	B6	PB6	I/O	FT	-	UART5_TX, TIM4_CH1, HDMI_CEC, I2C1_SCL, DFSDM_DATIN5, USART1_TX, CAN2_TX, QUADSPI_BK1_NCS, I2C4_SCL, FMC_SDNE1, DCMI_D5, EVENTOUT	-
93	137	B5	165	196	B5	C8	165	196	B5	PB7	I/O	FT	-	TIM4_CH2, I2C1_SDA, DFSDM_CKIN5, USART1_RX, I2C4_SDA, FMC_NL, DCMI_VSYNC, EVENTOUT	-
94	138	D6	166	197	E6	A10	166	197	E6	BOOT0	I	B	-	-	VPP
95	139	A5	167	198	A7	E9	167	198	A7	PB8	I/O	FT	-	I2C4_SCL, TIM4_CH3, TIM10_CH1, I2C1_SCL, DFSDM_CKIN7, UART5_RX, CAN1_RX, SDMMC2_D4, ETH_MII_TXD3, SDMMC1_D4, DCMI_D6, LCD_B6, EVENTOUT	-
96	140	B4	168	199	B4	D9	168	199	B4	PB9	I/O	FT	-	I2C4_SDA, TIM4_CH4, TIM11_CH1, I2C1_SDA, SPI2_NSS/I2S2_WS, DFSDM_DATIN7, UART5_TX, CAN1_TX, SDMMC2_D5, I2C4_SMBA, SDMMC1_D5, DCMI_D7, LCD_B7, EVENTOUT	-
97	141	A4	169	200	A6	C9	169	200	A6	PE0	I/O	FT	-	TIM4_ETR, LPTIM1_ETR, UART8_RX, SAI2_MCLK_A, FMC_NBL0, DCMI_D2, EVENTOUT	-

Table 10. STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180	LQFP176	LQFP208	TFBGA216						
98	142	A3	170	201	A5	B10	170	201	A5	PE1	I/O	FT	-	LPTIM1_IN2, UART8_TX, FMC_NBL1, DCMI_D3, EVENTOUT	-
99	-	D5	-	202	F6	A11	-	202	F6	VSS	S	-	-	-	-
-	143	C6	171	203	E5	C10	171	203	E5	PDR_ON	S	-	-	-	-
100	144	C5	172	204	E7	B11	172	204	E7	VDD	S	-	-	-	-
-	-	D4	173	205	C3	D10	173	205	C3	PI4	I/O	FT	-	TIM8_BKIN, SAI2_MCLK_A, FMC_NBL2, DCMI_D5, LCD_B4, EVENTOUT	-
-	-	C4	174	206	D3	D11	174	206	D3	PI5	I/O	FT	-	TIM8_CH1, SAI2_SCK_A, FMC_NBL3, DCMI_VSYNC, LCD_B5, EVENTOUT	-
-	-	C3	175	207	D6	C11	175	207	D6	PI6	I/O	FT	-	TIM8_CH2, SAI2_SD_A, FMC_D28, DCMI_D6, LCD_B6, EVENTOUT	-
-	-	C2	176	208	D4	B12	176	208	D4	PI7	I/O	FT	-	TIM8_CH3, SAI2_FS_A, FMC_D29, DCMI_D7, LCD_B7, EVENTOUT	-
-	-	F6	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	F7	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	F8	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	F9	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	F10	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	G6	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	G7	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	G8	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	G9	-	-	-	-	-	-	-	VSS	S	-	-	-	-

Table 10. STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions (continued)

Pin Number										Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32F767xx						STM32F768Ax STM32F769xx									
LQFP100	LQFP144	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP180	LQFP176	LQFP208	TFBGA216						
-	-	G10	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	H6	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	H7	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	H8	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	H9	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	H10	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	J6	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	J7	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	J8	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	J9	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	J10	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	K6	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	K7	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	K8	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	K9	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	K10	-	-	-	-	-	-	-	VSS	S	-	-	-	-

1. PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited: - The speed should not exceed 2 MHz with a maximum load of 30 pF. - These I/Os must not be used as a current source (e.g. to drive an LED).
2. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).
3. If the device is in regulator OFF/internal reset ON mode (BYPASS_REG pin is set to VDD), then PA0 is used as an internal reset (active low).
4. Internally connected to VDD or VSS depending on part number.

Table 11. FMC pin definition

Pin name	NOR/PSRAM/SRAM	NOR/PSRAM Mux	NAND16	SDRAM
PF0	A0	-	-	A0
PF1	A1	-	-	A1
PF2	A2	-	-	A2
PF3	A3	-	-	A3
PF4	A4	-	-	A4
PF5	A5	-	-	A5
PF12	A6	-	-	A6
PF13	A7	-	-	A7
PF14	A8	-	-	A8
PF15	A9	-	-	A9
PG0	A10	-	-	A10
PG1	A11	-	-	A11
PG2	A12	-	-	A12
PG3	A13	-	-	-
PG4	A14	-	-	BA0
PG5	A15	-	-	BA1
PD11	A16	A16	CLE	-
PD12	A17	A17	ALE	-
PD13	A18	A18	-	-
PE3	A19	A19	-	-
PE4	A20	A20	-	-
PE5	A21	A21	-	-
PE6	A22	A22	-	-
PE2	A23	A23	-	-
PG13	A24	A24	-	-
PG14	A25	A25	-	-
PD14	D0	DA0	D0	D0
PD15	D1	DA1	D1	D1
PD0	D2	DA2	D2	D2
PD1	D3	DA3	D3	D3
PE7	D4	DA4	D4	D4
PE8	D5	DA5	D5	D5
PE9	D6	DA6	D6	D6
PE10	D7	DA7	D7	D7

Table 11. FMC pin definition (continued)

Pin name	NOR/PSRAM/SRAM	NOR/PSRAM Mux	NAND16	SDRAM
PE11	D8	DA8	D8	D8
PE12	D9	DA9	D9	D9
PE13	D10	DA10	D10	D10
PE14	D11	DA11	D11	D11
PE15	D12	DA12	D12	D12
PD8	D13	DA13	D13	D13
PD9	D14	DA14	D14	D14
PD10	D15	DA15	D15	D15
PH8	D16	-	-	D16
PH9	D17	-	-	D17
PH10	D18	-	-	D18
PH11	D19	-	-	D19
PH12	D20	-	-	D20
PH13	D21	-	-	D21
PH14	D22	-	-	D22
PH15	D23	-	-	D23
PI0	D24	-	-	D24
PI1	D25	-	-	D25
PI2	D26	-	-	D26
PI3	D27	-	-	D27
PI6	D28	-	-	D28
PI7	D29	-	-	D29
PI9	D30	-	-	D30
PI10	D31	-	-	D31
PD7	NE1	NE1	-	-
PG6	NE3	-	-	-
PG9	NE2	NE2	NCE	-
PG10	NE3	NE3	-	-
PG11	-	-	-	-
PG12	NE4	NE4	-	-
PD3	CLK	CLK	-	-
PD4	NOE	NOE	NOE	-
PD5	NWE	NWE	NWE	-
PD6	NWAIT	NWAIT	NWAIT	-

Table 11. FMC pin definition (continued)

Pin name	NOR/PSRAM/SRAM	NOR/PSRAM Mux	NAND16	SDRAM
PB7	NADV	NADV	-	-
PF6	-	-	-	-
PF7	-	-	-	-
PF8	-	-	-	-
PF9	-	-	-	-
PF10	-	-	-	-
PG6	-	-	-	-
PG7	-	-	INT	-
PE0	NBL0	NBL0	-	NBL0
PE1	NBL1	NBL1	-	NBL1
PI4	NBL2	-	-	NBL2
PI5	NBL3	-	-	NBL3
PG8	-	-	-	SDCLK
PC0	-	-	-	SDNWE
PF11	-	-	-	SDNRAS
PG15	-	-	-	SDNCAS
PH2	-	-	-	SDCKE0
PH3	-	-	-	SDNE0
PH6	-	-	-	SDNE1
PH7	-	-	-	SDCKE1
PH5	-	-	-	SDNWE
PC2	-	-	-	SDNE0
PC3	-	-	-	SDCKE0
PC6	NWAIT	NWAIT	NWAIT	-
PB5	-	-	-	SDCKE1
PB6	-	-	-	SDNE1

Table 12. STM32F767xx, STM32F768Ax and STM32F769xx alternate function mapping

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	**I2C4/UART5/TIM1/2**	**TIM3/4/5**	**TIM8/9/10/11/LPTIM1/DFSDM/CEC**	**I2C1/2/3/4/USART1/CEC**	**SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6**	**SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4/DFSDM**	**SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5/DFSDM/SPDIF**	**SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS/SPDIF**	**CAN1/2/TIM12/13/14/QUADSPI/FMC/LCD**	**SAI2/QUADSPI/SDMMC2/DFSDM/OTG2_HS/OTG1_FS/LCD**	**I2C4/CAN3/SDMMC2/ETH**	**UART7/FMC/SDMMC1/MDIOS/OTG2_FS**	**DCMI/LCD/DSI**	**LCD**	**SYS**
Port A	PA0	-	TIM2_CH1/TIM2_ETR	TIM5_CH1	TIM8_ETR	-	-	-	USART2_CTS	UART4_TX	-	SAI2_SD_B	ETH_MII_CRS	-	-	-	EVENTOUT
	PA1	-	TIM2_CH2	TIM5_CH2	-	-	-	-	USART2_RTS	UART4_RX	QUADSPI_BK1_IO3	SAI2_MCK_B	ETH_MII_RX_CLK/ETH_RMII_REF_CLK	-	-	LCD_R2	EVENTOUT
	PA2	-	TIM2_CH3	TIM5_CH3	TIM9_CH1	-	-	-	USART2_TX	SAI2_SCK_B	-	-	ETH_MDIO	MDIOS_MDIO	-	LCD_R1	EVENTOUT
	PA3	-	TIM2_CH4	TIM5_CH4	TIM9_CH2	-	-	-	USART2_RX	-	LCD_B2	OTG_HS_ULPI_D0	ETH_MII_COL	-	-	LCD_B5	EVENTOUT
	PA4	-	-	-	-	-	SPI1_NSS/I2S1_WS	SPI3_NSS/I2S3_WS	USART2_CK	SPI6_NSS	-	-	-	OTG_HS_SOF	DCMI_HSYNC	LCD_VSYNC	EVENTOUT
	PA5	-	TIM2_CH1/TIM2_ETR	-	TIM8_CH1N	-	SPI1_SCK/I2S1_CK	-	-	SPI6_SCK	-	OTG_HS_ULPI_CK	-	-	-	LCD_R4	EVENTOUT
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	-	SPI1_MISO	-	-	SPI6_MISO	TIM13_CH1	-	-	MDIOS_MDC	DCMI_PIXCLK	LCD_G2	EVENTOUT
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	-	SPI1_MOSI/I2S1_SD	-	-	SPI6_MOSI	TIM14_CH1	-	ETH_MII_RX_DV/ETH_RMII_CRS_DV	FMC_SDNWE	-	-	EVENTOUT
	PA8	MCO1	TIM1_CH1	-	TIM8_BKIN2	I2C3_SCL	-	-	USART1_CK	-	-	OTG_FS_SOF	-	UART7_RX	LCD_B3	LCD_R6	EVENTOUT
	PA9	-	TIM1_CH2	-	-	I2C3_SMBA	SPI2_SCK/I2S2_CK	-	USART1_TX	-	-	-	-	-	DCMI_D0	LCD_R5	EVENTOUT
	PA10	-	TIM1_CH3	-	-	-	-	-	USART1_RX	-	LCD_B4	OTG_FS_ID	-	MDIOS_MDIO	DCMI_D1	LCD_B1	EVENTOUT

Table 12. STM32F767xx, STM32F768Ax and STM32F769xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/UART5/TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/DFSDM/CEC	I2C1/2/3/4/USART1/CEC	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6	SPI2/I2S2/SPI3/SAI1/I2C4/UART4/DFSDM	SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5/DFSDM/SPDIF	SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS/SPDIF	CAN1/2/TIM12/13/14/QUADSPI/FMC/LCD	SAI2/QUADSPI/SDMMC2/DFSDM/OTG2_HS/OTG1_FS/LCD	I2C4/CAN3/SDMMC2/ETH	UART7/FMC/SDMMC1/MDIOS/OTG2_FS	DCMI/LCD/DSI	LCD	SYS
Port A	PA11	-	TIM1_CH4	-	-	-	SPI2_NSS/I2S2_WS	UART4_RX	USART1_CTS	-	CAN1_RX	OTG_FS_DM	-	-	-	LCD_R4	EVENTOUT
	PA12	-	TIM1_ETR	-	-	-	SPI2_SCK/I2S2_CK	UART4_TX	USART1_RTS	SAI2_FS_B	CAN1_TX	OTG_FS_DP	-	-	-	LCD_R5	EVENTOUT
	PA13	JTMS-SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA14	JTCK-SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA15	JTDI	TIM2_CH1/TIM2_ETR	-	-	HDMI-CEC	SPI1_NSS/I2S1_WS	SPI3_NSS/I2S3_WS	SPI6_NSS	UART4_RTS	-	-	CAN3_TX	UART7_TX	-	-	EVENTOUT
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	-	DFSDM_CKOUT	-	UART4_CTS	LCD_R3	OTG_HS_ULPI_D1	ETH_MII_RXD2	-	-	LCD_G1	EVENTOUT
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	DFSDM_DATIN1	-	-	LCD_R6	OTG_HS_ULPI_D2	ETH_MII_RXD3	-	-	LCD_G0	EVENTOUT
	PB2	-	-	-	-	-	-	SAI1_SD_A	SPI3_MOSI/I2S3_SD		QUADSPI_CLK	DFSDM_CKIN1	-	-	-	-	EVENTOUT
	PB3	JTDO/TRACESWO	TIM2_CH2	-	-	-	SPI1_SCK/I2S1_CK	SPI3_SCK/I2S3_CK	-	SPI6_SCK	-	SDMMC2_D2	CAN3_RX	UART7_RX	-	-	EVENTOUT
	PB4	NJTRST	-	TIM3_CH1	-	-	SPI1_MISO	SPI3_MISO	SPI2_NSS/I2S2_WS	SPI6_MISO	-	SDMMC2_D3	CAN3_TX	UART7_TX	-	-	EVENTOUT
	PB5	-	UART5_RX	TIM3_CH2	-	I2C1_SMBA	SPI1_MOSI/I2S1_SD	SPI3_MOSI/I2S3_SD	-	SPI6_MOSI	CAN2_RX	OTG_HS_ULPI_D7	ETH_PPS_OUT	FMC_SDCKE1	DCMI_D10	LCD_G7	EVENTOUT
	PB6	-	UART5_TX	TIM4_CH1	HDMI-CEC	I2C1_SCL	-	DFSDM_DATIN5	USART1_TX	-	CAN2_TX	QUADSPI_BK1_NCS	I2C4_SCL	FMC_SDNE1	DCMI_D5	-	EVENTOUT

Table 12. STM32F767xx, STM32F768Ax and STM32F769xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/UART5/TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/DFSDM/CEC	I2C1/2/3/4/USART1/CEC	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6	SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4/DFSDM	SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5/DFSDM/SPDIF	SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS/SPDIF	CAN1/2/TIM12/13/14/QUADSPI/FMC/LCD	SAI2/QUADSPI/SDMMC2/DFSDM/OTG2_HS/OTG1_FS/LCD	I2C4/CAN3/SDMMC2/ETH	UART7/FMC/SDMMC1/MDIOS/OTG2_FS	DCMI/LCD/DSI	LCD	SYS
Port B	PB7	-	-	TIM4_CH2	-	I2C1_SDA	-	DFSDM_CKIN5	USART1_RX	-	-	-	I2S4_SDA	FMC_NL	DCMI_VSYNC	-	EVENTOUT
	PB8	-	I2C4_SCL	TIM4_CH3	TIM10_CH1	I2C1_SCL	-	DFSDM_CKIN7	UART5_RX	-	CAN1_RX	SDMMC2_D4	ETH_MII_TXD3	SDMMC_D4	DCMI_D6	LCD_B6	EVENTOUT
	PB9	-	I2S4_SDA	TIM4_CH4	TIM11_CH1	I2C1_SDA	SPI2_NSS/I2S2_WS	DFSDM_DATIN7	UART5_TX	-	CAN1_TX	SDMMC2_D5	I2C4_SMBA	SDMMC_D5	DCMI_D7	LCD_B7	EVENTOUT
	PB10	-	TIM2_CH3	-	-	I2C2_SCL	SPI2_SCK/I2S2_CK	DFSDM_DATIN7	USART3_TX	-	- QUADSPI_BK1_NCS	OTG_HS_ULPI_D3	ETH_MII_RX_ER	-	-	LCD_G4	EVENTOUT
	PB11	-	TIM2_CH4	-	-	I2C2_SDA	-	DFSDM_CKIN7	USART3_RX	-	-	OTG_HS_ULPI_D4	ETH_MII_TX_EN/ETH_RMII_TX_EN	-	DSI_TE	LCD_G5	EVENTOUT
	PB12	-	TIM1_BKIN	-	-	I2C2_SMBA	SPI2_NSS/I2S2_WS	DFSDM_DATIN1	USART3_CK	UART5_RX	CAN2_RX	OTG_HS_ULPI_D5	ETH_MII_TXD0/ETH_RMII_TXD0	OTG_HS_ID	-	-	EVENTOUT
	PB13	-	TIM1_CH1N	-	-	-	SPI2_SCK/I2S2_CK	DFSDM_CKIN1	USART3_CTS	UART5_TX	CAN2_TX	OTG_HS_ULPI_D6	ETH_MII_TXD1/ETH_RMII_TXD1	-	-	-	EVENTOUT
	PB14	-	TIM1_CH2N	-	TIM8_CH2N	USART1_TX	SPI2_MISO	DFSDM_DATIN2	USART3_RTS	UART4_RTS	TIM12_CH1	SDMMC2_D0	-	OTG_HS_DM	-	-	EVENTOUT
	PB15	RTC_REFIN	TIM1_CH3N	-	TIM8_CH3N	USART1_RX	SPI2_MOSI/I2S2_SD	DFSDM_CKIN2	-	UART4_CTS	TIM12_CH2	SDMMC2_D1	-	OTG_HS_DP	-	-	EVENTOUT

Table 12. STM32F767xx, STM32F768Ax and STM32F769xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/UART5/TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/DFSDM/CEC	I2C1/2/3/4/USART1/CEC	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6	SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4/DFSDM	SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5/DFSDM/SPDIF	SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS/SPDIF	CAN1/2/TIM12/13/14/QUADSPI/FMC/LCD	SAI2/QUADSPI/SDMMC2/DFSDM/OTG2_HS/OTG1_FS/LCD	I2C4/CAN3/SDMMC2/ETH	UART7/FMC/SDMMC1/MDIOS/OTG2_FS	DCMI/LCD/DSI	LCD	SYS
Port C	PC0	-	-	-	DFSDM_CKIN0	-	-	DFSDM_DATIN4	-	SAI2_FS_B	-	OTG_HS_ULPI_STP	-	FMC_SDNWE	-	LCD_R5	EVENTOUT
	PC1	TRACED0	-	-	DFSDM_DATAIN0	-	SPI2_MOSI/I2S2_SD	SAI1_SD_A	-	-	-	DFSDM_CKIN4	ETH_MDC	MDIOS_MDC	-	-	EVENTOUT
	PC2	-	-	-	DFSDM_CKIN1	-	SPI2_MISO	DFSDM_CKOUT	-	-	-	OTG_HS_ULPI_DIR	ETH_MII_TXD2	FMC_SDNE0	-	-	EVENTOUT
	PC3	-	-	-	DFSDM_DATAIN1	-	SPI2_MOSI/I2S2_SD	-	-	-	-	OTG_HS_ULPI_NXT	ETH_MII_TX_CLK	FMC_SDCKE0	-	-	EVENTOUT
	PC4	-	-	-	DFSDM_CKIN2	-	I2S1_MCK	-	-	SPDIF_RX2	-	-	ETH_MII_RXD0/ETH_RMII_RXD0	FMC_SDNE0	-	-	EVENTOUT
	PC5	-	-	-	DFSDM_DATAIN2	-	-	-	-	SPDIF_RX3	-	-	ETH_MII_RXD1/ETH_RMII_RXD1	FMC_SDCKE0	-	-	EVENTOUT
	PC6	-	-	TIM3_CH1	TIM8_CH1	-	I2S2_MCK	-	DFSDM_CKIN3	USART6_TX	FMC_NWAIT	SDMMC2_D6	-	SDMMC_D6	DCMI_D0	LCD_HSYNC	EVENTOUT
	PC7	-	-	TIM3_CH2	TIM8_CH2	-	-	I2S3_MCK	DFSDM_DATAIN3	USART6_RX	FMC_NE1	SDMMC2_D7	-	SDMMC_D7	DCMI_D1	LCD_G6	EVENTOUT
	PC8	TRACED1	-	TIM3_CH3	TIM8_CH3	-	-	-	UART5_RTS	USART6_CK	FMC_NE2/FMC_NCE	-	-	SDMMC_D0	DCMI_D2	-	EVENTOUT
	PC9	MCO2	-	TIM3_CH4	TIM8_CH4	I2C3_SDA	I2S_CKIN	-	UART5_CTS	-	QUADSPI_BK1_IO0	LCD_G3	-	SDMMC_D1	DCMI_D3	LCD_B2	EVENTOUT
	PC10	-	-	-	DFSDM_CKIN5	-	-	SPI3_SCK/I2S3_CK	USART3_TX	UART4_TX	QUADSPI_BK1_IO1	-	-	SDMMC_D2	DCMI_D8	LCD_R2	EVENTOUT

Table 12. STM32F767xx, STM32F768Ax and STM32F769xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/UART5/TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/DFSDM1/CEC	I2C1/2/3/4/USART1/CEC	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6	SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4/DFSDM	SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5/DFSDM/SPDIF	SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS/SPDIF	CAN1/2/TIM12/13/14/QUADSPI/FMC/LCD	SAI2/QUADSPI/SDMMC2/DFSDM/OTG2_HS/OTG1_FS/LCD	I2C4/CAN3/SDMMC2/ETH	UART7/FMC/SDMMC1/MDIOS/OTG2_FS	DCMI/LCD/DSI	LCD	SYS
Port C	PC11	-	-	-	DFSDM_DATAIN5	-	-	SPI3_MISO	USART3_RX	UART4_RX	QUADSPI_BK2_NCS	-	-	SDMMC_D3	DCMI_D4	-	EVENTOUT
	PC12	TRACED3	-	-	-	-	-	SPI3_MOSI/I2S3_SD	USART3_CK	UART5_TX	-	-	-	SDMMC_CK	DCMI_D9	-	EVENTOUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
Port D	PD0	-	-	-	DFSDM_CKIN6	-	-	DFSDM_DATAIN7	-	UART4_RX	CAN1_RX	-	-	FMC_D2	-	-	EVENTOUT
	PD1	-	-	-	DFSDM_DATAIN6	-	-	DFSDM_CKIN7	-	UART4_TX	CAN1_TX	-	-	FMC_D3	-	-	EVENTOUT
	PD2	TRACED2	-	TIM3_ETR	-	-	-	-	-	UART5_RX	-	-	-	SDMMC_CMD	DCMI_D11	-	EVENTOUT
	PD3	-	-	-	DFSDM_CKOUT	-	SPI2_SCK/I2S2_CK	DFSDM_DATAIN0	USART2_CTS	-	-	-	-	FMC_CLK	DCMI_D5	LCD_G7	EVENTOUT
	PD4	-	-	-	-	-	-	DFSDM_CKIN0	USART2_RTS	-	-	-	-	FMC_NOE	-	-	EVENTOUT
	PD5	-	-	-	-	-	-	-	USART2_TX	-	-	-	-	FMC_NWE	-	-	EVENTOUT
	PD6	-	-	-	DFSDM_CKIN4	-	SPI3_MOSI/I2S3_SD	SAI1_SD_A	USART2_RX	-	-	DFSDM_DATAIN1	SDMMC2_CK	FMC_NWAIT	DCMI_D10	LCD_B2	EVENTOUT
	PD7	-	-	-	DFSDM_DATAIN4	-	SPI1_MOSI/I2S1_SD	DFSDM_CKIN1	USART2_CK	SPDIF_RX0	-	-	SDMMC2_CMD	FMC_NE1	-	-	EVENTOUT
	PD8	-	-	-	DFSDM_CKIN3	-	-	-	USART3_TX	SPDIF_RX1	-	-	-	FMC_D13	-	-	EVENTOUT

Table 12. STM32F767xx, STM32F768Ax and STM32F769xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/UART5/TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/DFSDM/CEC	I2C1/2/3/4/USART1/CEC	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6	SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4/DFSDM	SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5/DFSDM/SPDIF	SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS/SPDIF	CAN1/2/TIM12/13/14/QUADSPI/FMC/LCD	SAI2/QUADSPI/SDMMC2/DFSDM/OTG2_HS/OTG1_FS/LCD	I2C4/CAN3/SDMMC2/ETH	UART7/FMC/SDMMC1/MDIOS/OTG2_FS	DCMI/LCD/DSI	LCD	SYS
Port D	PD9	-	-	-	DFSDM_DATAIN3	-	-	-	USART3_RX	-	-	-	-	FMC_D14	-	-	EVENTOUT
	PD10	-	-	-	DFSDM_CKOUT	-	-	-	USART3_CK	-	-	-	-	FMC_D15	-	LCD_B3	EVENTOUT
	PD11	-	-	-	-	I2C4_SMBA	-	-	USART3_CTS	-	QUADSPI_BK1_IO0	SAI2_SD_A	-	FMC_A16/FMC_CLE	-	-	EVENTOUT
	PD12	-	-	TIM4_CH1	LPTIM1_IN1	I2C4_SCL	-	-	USART3_RTS	-	QUADSPI_BK1_IO1	SAI2_FS_A	-	FMC_A17/FMC_ALE	-	-	EVENTOUT
	PD13	-	-	TIM4_CH2	LPTIM1_OUT	I2C4_SDA	-	-	-	-	QUADSPI_BK1_IO3	SAI2_SCK_A	-	FMC_A18	-	-	EVENTOUT
	PD14	-	-	TIM4_CH3	-	-	-	-	-	UART8_CTS	-	-	-	FMC_D0	-	-	EVENTOUT
	PD15	-	-	TIM4_CH4	-	-	-	-	-	UART8_RTS	-	-	-	FMC_D1	-	-	EVENTOUT
Port E	PE0	-	-	TIM4_ETR	LPTIM1_ETR	-	-	-	-	UART8_Rx	-	SAI2_MCK_A	-	FMC_NBL0	DCMI_D2	-	EVENTOUT
	PE1	-	-	-	LPTIM1_IN2	-	-	-	-	UART8_Tx	-	-	-	FMC_NBL1	DCMI_D3	-	EVENTOUT
	PE2	TRACECLK	-	-	-	-	SPI4_SCK	SAI1_MCLK_A	-	-	QUADSPI_BK1_IO2	-	ETH_MII_TXD3	FMC_A23	-	-	EVENTOUT
	PE3	TRACED0	-	-	-	-	-	SAI1_SD_B	-	-	-	-	-	FMC_A19	-	-	EVENTOUT
	PE4	TRACED1	-	-	-	-	SPI4_NSS	SAI1_FS_A	-	-	-	DFSDM_DATAIN3	-	FMC_A20	DCMI_D4	LCD_B0	EVENTOUT
	PE5	TRACED2	-	-	TIM9_CH1	-	SPI4_MISO	SAI1_SCK_A	-	-	-	DFSDM_CKIN3	-	FMC_A21	DCMI_D6	LCD_G0	EVENTOUT
	PE6	TRACED3	TIM1_BKIN2	-	TIM9_CH2	-	SPI4_MOSI	SAI1_SD_A	-	-	-	SAI2_MCK_B	-	FMC_A22	DCMI_D7	LCD_G1	EVENTOUT

Table 12. STM32F767xx, STM32F768Ax and STM32F769xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/UART5/TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/DFSDM/CEC	I2C1/2/3/4/USART1/CEC	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6	SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4/DFSDM	SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5/DFSDM/SPDIF	SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS/SPDIF	CAN1/2/TIM12/13/14/QUADSPI/FMC/LCD	SAI2/QUADSPI/SDMMC2/DFSDM/OTG2_HS/OTG1_FS/LCD	I2C4/CAN3/SDMMC2/ETH	UART7/FMC/SDMMC1/MDIOS/OTG2_FS	DCMI/LCD/DSI	LCD	SYS
Port E	PE7	-	TIM1_ETR	-	-	-	-	DFSDM_DATAIN2	-	UART7_Rx	-	QUADSPI_BK2_IO0	-	FMC_D4	-	-	EVENTOUT
	PE8	-	TIM1_CH1N	-	-	-	-	DFSDM_CKIN2	-	UART7_Tx	-	QUADSPI_BK2_IO1	-	FMC_D5	-	-	EVENTOUT
	PE9	-	TIM1_CH1	-	-	-	-	DFSDM_CKOUT	-	UART7_RTS	-	QUADSPI_BK2_IO2	-	FMC_D6	-	-	EVENTOUT
	PE10	-	TIM1_CH2N	-	-	-	-	DFSDM_DATAIN4	-	UART7_CTS	-	QUADSPI_BK2_IO3	-	FMC_D7	-	-	EVENTOUT
	PE11	-	TIM1_CH2	-	-	-	SPI4_NSS	DFSDM_CKIN4	-	-	-	SAI2_SD_B	-	FMC_D8	-	LCD_G3	EVENTOUT
	PE12	-	TIM1_CH3N	-	-	-	SPI4_SCK	DFSDM_DATAIN5	-	-	-	SAI2_SCK_B	-	FMC_D9	-	LCD_B4	EVENTOUT
	PE13	-	TIM1_CH3	-	-	-	SPI4_MISO	DFSDM_CKIN5	-	-	-	SAI2_FS_B	-	FMC_D10	-	LCD_DE	EVENTOUT
	PE14	-	TIM1_CH4	-	-	-	SPI4_MOSI	-	-	-	-	SAI2_MCK_B	-	FMC_D11	-	LCD_CLK	EVENTOUT
	PE15	-	TIM1_BKIN	-	-	-	-	-	-	-	-	-	-	FMC_D12	-	LCD_R7	EVENTOUT
Port F	PF0	-	-	-	-	I2C2_SDA	-	-	-	-	-	-	-	FMC_A0	-	-	EVENTOUT
	PF1	-	-	-	-	I2C2_SCL	-	-	-	-	-	-	-	FMC_A1	-	-	EVENTOUT
	PF2	-	-	-	-	I2C2_SMBA	-	-	-	-	-	-	-	FMC_A2	-	-	EVENTOUT
	PF3	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A3	-	-	EVENTOUT
	PF4	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A4	-	-	EVENTOUT
	PF5	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A5	-	-	EVENTOUT

Table 12. STM32F767xx, STM32F768Ax and STM32F769xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/UART5/TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/DFSDM1/CEC	I2C1/2/3/4/USART1/CEC	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6	SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4/DFSDM	SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5/DFSDM/SPDIF	SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS/SPDIF	CAN1/2/TIM12/13/14/QUADSPI/FMC/LCD	SAI2/QUADSPI/SDMMC2/DFSDM/OTG2_HS/OTG1_FS/LCD	I2C4/CAN3/SDMMC2/ETH	UART7/FMC/SDMMC1/MDIOS/OTG2_FS	DCMI/LCD/DSI	LCD	SYS
Port F	PF6	-	-	-	TIM10_CH1	-	SPI5_NSS	SAI1_SD_B	-	UART7_Rx	QUADSPI_BK1_IO3	-	-	-	-	-	EVENTOUT
	PF7	-	-	-	TIM11_CH1	-	SPI5_SCK	SAI1_MCLK_B	-	UART7_Tx	QUADSPI_BK1_IO2	-	-	-	-	-	EVENTOUT
	PF8	-	-	-	-	-	SPI5_MISO	SAI1_SCK_B	-	UART7_RTS	TIM13_CH1	QUADSPI_BK1_IO0	-	-	-	-	EVENTOUT
	PF9	-	-	-	-	-	SPI5_MOSI	SAI1_FS_B	-	UART7_CTS	TIM14_CH1	QUADSPI_BK1_IO1	-	-	-	-	EVENTOUT
	PF10	-	-	-	-	-	-	-	-	-	QUADSPI_CLK	-	-	-	DCMI_D11	LCD_DE	EVENTOUT
	PF11	-	-	-	-	-	SPI5_MOSI	-	-	-	-	SAI2_SD_B	-	FMC_SDNRAS	DCMI_D12	-	EVENTOUT
	PF12	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A6	-	-	EVENTOUT
	PF13	-	-	-	-	I2C4_SMBA	-	DFSDM_DATAIN6	-	-	-	-	-	FMC_A7	-	-	EVENTOUT
	PF14	-	-	-	-	I2C4_SCL	-	DFSDM_CKIN6	-	-	-	-	-	FMC_A8	-	-	EVENTOUT
	PF15	-	-	-	-	I2C4_SDA	-	-	-	-	-	-	-	FMC_A9	-	-	EVENTOUT
Port G	PG0	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A10	-	-	EVENTOUT
	PG1	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A11	-	-	EVENTOUT
	PG2	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A12	-	-	EVENTOUT
	PG3	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A13	-	-	EVENTOUT

Table 12. STM32F767xx, STM32F768Ax and STM32F769xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/UART5/TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/DFSDM1/CEC	I2C1/2/3/4/USART1/CEC	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6	SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4/DFSDM	SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5/DFSDM/SPDIF	SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS/SPDIF	CAN1/2/TIM12/13/14/QUADSPI/FMC/LCD	SAI2/QUADSPI/SDMMC2/DFSDM/OTG2_HS/OTG1_FS/LCD	I2C4/CAN3/SDMMC2/ETH	UART7/FMC/SDMMC1/MDIOS/OTG2_FS	DCMI/LCD/DSI	LCD	SYS
Port G	PG4	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A14/FMC_BA0	-	-	EVENTOUT
	PG5	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A15/FMC_BA1	-	-	EVENTOUT
	PG6	-	-	-	-	-	-	-	-	-	-	-	-	FMC_NE3	DCMI_D12	LCD_R7	EVENTOUT
	PG7	-	-	-	-	-	-	SAI1_MCLK_A	-	USART6_CK	-	-	-	FMC_INT	DCMI_D13	LCD_CLK	EVENTOUT
	PG8	-	-	-	-	-	SPI6_NSS	-	SPDIF_RX2	USART6_RTS	-	-	ETH_PPS_OUT	FMC_SDCLK	-	LCD_G7	EVENTOUT
	PG9	-	-	-	-	-	SPI1_MISO	-	SPDIF_RX3	USART6_RX	QUADSPI_BK2_IO2	SAI2_FS_B	SDMMC2_D0	FMC_NE2/FMC_NCE	DCMI_VSYNC	-	EVENTOUT
	PG10	-	-	-	-	-	SPI1_NSS/I2S1_WS	-	-	-	LCD_G3	SAI2_SD_B	SDMMC2_D1	FMC_NE3	DCMI_D2	LCD_B2	EVENTOUT
	PG11	-	-	-	-	-	SPI1_SCK/I2S1_CK	-	SPDIF_RX0	-	-	SDMMC2_D2	ETH_MII_TX_EN/ETH_RMII_TX_EN	-	DCMI_D3	LCD_B3	EVENTOUT
	PG12	-	-	-	LPTIM1_IN1	-	SPI6_MISO	-	SPDIF_RX1	USART6_RTS	LCD_B4	-	SDMMC2_D3	FMC_NE4	-	LCD_B1	EVENTOUT
	PG13	TRACED0	-	-	LPTIM1_OUT	-	SPI6_SCK	-	-	USART6_CTS	-	-	ETH_MII_TXD0/ETH_RMII_TXD0	FMC_A24	-	LCD_R0	EVENTOUT
	PG14	TRACED1	-	-	LPTIM1_ETR	-	SPI6_MOSI	-	-	USART6_TX	QUADSPI_BK2_IO3	-	ETH_MII_TXD1/ETH_RMII_TXD1	FMC_A25	-	LCD_B0	EVENTOUT
	PG15	-	-	-	-	-	-	-	-	USART6_CTS	-	-	-	FMC_SDNCAS	DCMI_D13	-	EVENTOUT

Table 12. STM32F767xx, STM32F768Ax and STM32F769xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/UART5/TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/DFSDM/CEC	I2C1/2/3/4/USART1/CEC	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6	SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4/DFSDM	SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5/DFSDM/SPDIF	SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS/SPDIF	CAN1/2/TIM12/13/14/QUADSPI/FMC/LCD	SAI2/QUADSPI/SDMMC2/DFSDM/OTG2_HS/OTG1_FS/LCD	I2C4/CAN3/SDMMC2/ETH	UART7/FMC/SDMMC1/MDIOS/OTG2_FS	DCMI/LCD/DSI	LCD	SYS
Port H	PH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH2	-	-	-	LPTIM1_IN2	-	-	-	-	-	QUADSPI_BK2_IO0	SAI2_SCK_B	ETH_MII_CRS	FMC_SDCKE0	-	LCD_R0	EVENTOUT
	PH3	-	-	-	-	-	-	-	-	-	QUADSPI_BK2_IO1	SAI2_MCK_B	ETH_MII_COL	FMC_SDNE0	-	LCD_R1	EVENTOUT
	PH4	-	-	-	-	I2C2_SCL	-	-	-	-	LCD_G5	OTG_HS_ULPI_NXT	-	-	-	LCD_G4	EVENTOUT
	PH5	-	-	-	-	I2C2_SDA	SPI5_NSS	-	-	-	-	-	-	FMC_SDNWE	-	-	EVENTOUT
	PH6	-	-	-	-	I2C2_SMBA	SPI5_SCK	-	-	-	TIM12_CH1	-	ETH_MII_RXD2	FMC_SDNE1	DCMI_D8	-	EVENTOUT
	PH7	-	-	-	-	I2C3_SCL	SPI5_MISO	-	-	-	-	-	ETH_MII_RXD3	FMC_SDCKE1	DCMI_D9	-	EVENTOUT
	PH8	-	-	-	-	I2C3_SDA	-	-	-	-	-	-	-	FMC_D16	DCMI_HSYNC	LCD_R2	EVENTOUT
	PH9	-	-	-	-	I2C3_SMBA	-	-	-	-	TIM12_CH2	-	-	FMC_D17	DCMI_D0	LCD_R3	EVENTOUT
	PH10	-	-	TIM5_CH1	-	I2C4_SMBA	-	-	-	-	-	-	-	FMC_D18	DCMI_D1	LCD_R4	EVENTOUT
	PH11	-	-	TIM5_CH2	-	I2C4_SCL	-	-	-	-	-	-	-	FMC_D19	DCMI_D2	LCD_R5	EVENTOUT
	PH12	-	-	TIM5_CH3	-	I2C4_SDA	-	-	-	-	-	-	-	FMC_D20	DCMI_D3	LCD_R6	EVENTOUT
	PH13	-	-	-	TIM8_CH1N	-	-	-	-	UART4_TX	CAN1_TX	-	-	FMC_D21	-	LCD_G2	EVENTOUT

Table 12. STM32F767xx, STM32F768Ax and STM32F769xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/UART5/TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/DFSDM/CEC	I2C1/2/3/4/USART1/CEC	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6	SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4/DFSDM	SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5/DFSDM/SPDIF	SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS/SPDIF	CAN1/2/TIM12/13/14/QUADSPI/FMC/LCD	SAI2/QUADSPI/SDMMC2/DFSDM/OTG2_HS/OTG1_FS/LCD	I2C4/CAN3/SDMMC2/ETH	UART7/FMC/SDMMC1/MDIOS/OTG2_FS	DCMI/LCD/DSI	LCD	SYS
Port H	PH14	-	-	-	TIM8_CH2N	-	-	-	-	UART4_RX	CAN1_RX	-	-	FMC_D22	DCMI_D4	LCD_G3	EVENTOUT
Port H	PH15	-	-	-	TIM8_CH3N	-	-	-	-	-	-	-	-	FMC_D23	DCMI_D11	LCD_G4	EVENTOUT
Port I	PI0	-	-	TIM5_CH4	-	-	SPI2_NSS/I2S2_WS	-	-	-	-	-	-	FMC_D24	DCMI_D13	LCD_G5	EVENTOUT
Port I	PI1	-	-	-	TIM8_BKIN2	-	SPI2_SCK/I2S2_CK	-	-	-	-	-	-	FMC_D25	DCMI_D8	LCD_G6	EVENTOUT
Port I	PI2	-	-	-	TIM8_CH4	-	SPI2_MISO	-	-	-	-	-	-	FMC_D26	DCMI_D9	LCD_G7	EVENTOUT
Port I	PI3	-	-	-	TIM8_ETR	-	SPI2_MOSI/I2S2_SD	-	-	-	-	-	-	FMC_D27	DCMI_D10	-	EVENTOUT
Port I	PI4	-	-	-	TIM8_BKIN	-	-	-	-	-	-	SAI2_MCK_A	-	FMC_NBL2	DCMI_D5	LCD_B4	EVENTOUT
Port I	PI5	-	-	-	TIM8_CH1	-	-	-	-	-	-	SAI2_SCK_A	-	FMC_NBL3	DCMI_VSYNC	LCD_B5	EVENTOUT
Port I	PI6	-	-	-	TIM8_CH2	-	-	-	-	-	-	SAI2_SD_A	-	FMC_D28	DCMI_D6	LCD_B6	EVENTOUT
Port I	PI7	-	-	-	TIM8_CH3	-	-	-	-	-	-	SAI2_FS_A	-	FMC_D29	DCMI_D7	LCD_B7	EVENTOUT
Port I	PI8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
Port I	PI9	-	-	-	-	-	-	-	-	UART4_RX	CAN1_RX	-	-	FMC_D30	-	LCD_VSYNC	EVENTOUT
Port I	PI10	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_RX_ER	FMC_D31	-	LCD_HSYNC	EVENTOUT
Port I	PI11	-	-	-	-	-	-	-	-	-	LCD_G6	OTG_HS_ULPI_DIR	-	-	-	-	EVENTOUT

Table 12. STM32F767xx, STM32F768Ax and STM32F769xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/UART5/TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/DFSDM/CEC	I2C1/2/3/4/USART1/CEC	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6	SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4/DFSDM	SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5/DFSDM/SPDIF	SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS/SPDIF	CAN1/2/TIM12/13/14/QUADSPI/FMC/LCD	SAI2/QUADSPI/SDMMC2/DFSDM/OTG2_HS/OTG1_FS/LCD	I2C4/CAN3/SDMMC2/ETH	UART7/FMC/SDMMC1/MDIOS/OTG2_FS	DCMI/LCD/DSI	LCD	SYS
Port I	PI12	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_HSYNC	EVENTOUT
	PI13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_VSYNC	EVENTOUT
	PI14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_CLK	EVENTOUT
	PI15	-	-	-	-	-	-	-	-	-	LCD_G2	-	-	-	-	LCD_R0	EVENTOUT
Port J	PJ0	-	-	-	-	-	-	-	-	-	LCD_R7	-	-	-	-	LCD_R1	EVENTOUT
	PJ1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R2	EVENTOUT
	PJ2	-	-	-	-	-	-	-	-	-	-	-	-	-	DSI_TE	LCD_R3	EVENTOUT
	PJ3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R4	EVENTOUT
	PJ4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R5	EVENTOUT
	PJ5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R6	EVENTOUT
	PJ6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R7	EVENTOUT
	PJ7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G0	EVENTOUT
	PJ8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G1	EVENTOUT
	PJ9	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G2	EVENTOUT
	PJ10	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G3	EVENTOUT

Table 12. STM32F767xx, STM32F768Ax and STM32F769xx alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	I2C4/UART5/TIM1/2	TIM3/4/5	TIM8/9/10/11/LPTIM1/DFSDM/CEC	I2C1/2/3/4/USART1/CEC	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6	SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4/DFSDM	SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5/DFSDM/SPDIF	SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS/SPDIF	CAN1/2/TIM12/13/14/QUADSPI/FMC/LCD	SAI2/QUADSPI/SDMMC2/DFSDM/OTG2_HS/OTG1_FS/LCD	I2C4/CAN3/SDMMC2/ETH	UART7/FMC/SDMMC1/MDIOS/OTG2_FS	DCMI/LCD/DSI	LCD	SYS
Port J	PJ11	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G4	EVENTOUT
	PJ12	-	-	-	-	-	-	-	-	-	LCD_G3	-	-	-	-	LCD_B0	EVENTOUT
	PJ13	-	-	-	-	-	-	-	-	-	LCD_G4	-	-	-	-	LCD_B1	EVENTOUT
	PJ14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B2	EVENTOUT
	PJ15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B3	EVENTOUT
Port K	PK0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G5	EVENTOUT
	PK1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G6	EVENTOUT
	PK2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_G7	EVENTOUT
	PK3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B4	EVENTOUT
	PK4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B5	EVENTOUT
	PK5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B6	EVENTOUT
	PK6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B7	EVENTOUT
	PK7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DE	EVENTOUT

4 Memory mapping

The memory map is shown in *Figure 19*.

Figure 19. Memory map

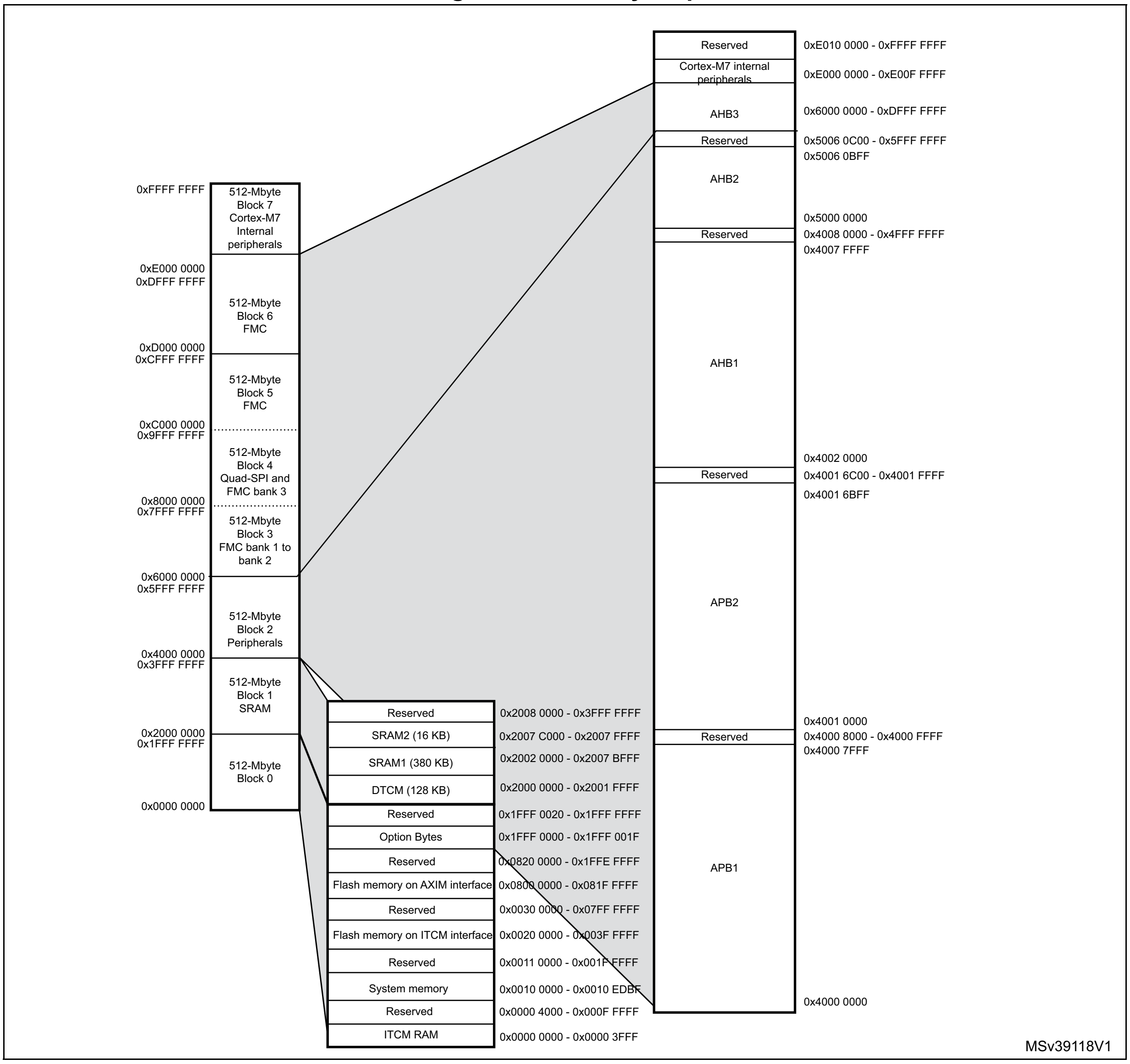


Table 13. STM32F767xx, STM32F768Ax and STM32F769xx register boundary addresses

Bus	Boundary address	Peripheral
	0xE00F FFFF - 0xFFFF FFFF	Reserved
Cortex-M7	0xE000 0000 - 0xE00F FFFF	Cortex-M7 internal peripherals
AHB3	0xD000 0000 - 0xDFFF FFFF	FMC bank 6
	0xC000 0000 - 0xCFFF FFFF	FMC bank 5
	0xA000 2000 - 0xBFFF FFFF	Reserved
	0xA000 1000 - 0xA000 1FFF	Quad-SPI control register
	0xA000 0000- 0xA000 0FFF	FMC control register
	0x9000 0000 - 0x9FFF FFFF	Quad-SPI
	0x8000 0000 - 0x8FFF FFFF	FMC bank 3
	0x7000 0000 - 0x7FFF FFFF	FMC bank 2
	0x6000 0000 - 0x6FFF FFFF	FMC bank 1
	0x5006 0C00- 0x5FFF FFFF	Reserved
AHB2	0x5006 0800 - 0x5006 0BFF	RNG
	0x5005 2000 - 0x5005 FFFF	Reserved
	0x5005 1000 - 0x5005 1FFF	JPEG codec
	0x5005 0000 - 0x5005 03FF	DCMI
	0x5004 0000- 0x5004 FFFF	Reserved
	0x5000 0000 - 0x5003 FFFF	USB OTG FS

Table 13. STM32F767xx, STM32F768Ax and STM32F769xx register boundary addresses (continued)

Bus	Boundary address	Peripheral
	0x4008 0000- 0x4FFF FFFF	Reserved
AHB1	0x4004 0000 - 0x4007 FFFF	USB OTG HS
	0x4002 BC00- 0x4003 FFFF	Reserved
	0x4002 B000 - 0x4002 BBFF	Chrom-ART (DMA2D)
	0x4002 9400 - 0x4002 AFFF	Reserved
	0x4002 9000 - 0x4002 93FF	ETHERNET MAC
	0x4002 8C00 - 0x4002 8FFF	
	0x4002 8800 - 0x4002 8BFF	
	0x4002 8400 - 0x4002 87FF	
	0x4002 8000 - 0x4002 83FF	
	0x4002 6800 - 0x4002 7FFF	Reserved
	0x4002 6400 - 0x4002 67FF	DMA2
	0x4002 6000 - 0x4002 63FF	DMA1
	0x4002 5000 - 0X4002 5FFF	Reserved
	0x4002 4000 - 0x4002 4FFF	BKPSRAM
	0x4002 3C00 - 0x4002 3FFF	Flash interface register
	0x4002 3800 - 0x4002 3BFF	RCC
	0X4002 3400 - 0X4002 37FF	Reserved
	0x4002 3000 - 0x4002 33FF	CRC
	0x4002 2C00 - 0x4002 2FFF	Reserved
	0x4002 2800 - 0x4002 2BFF	GPIOK
	0x4002 2400 - 0x4002 27FF	GPIOJ
	0x4002 2000 - 0x4002 23FF	GPIOI
	0x4002 1C00 - 0x4002 1FFF	GPIOH
	0x4002 1800 - 0x4002 1BFF	GPIOG
	0x4002 1400 - 0x4002 17FF	GPIOF
	0x4002 1000 - 0x4002 13FF	GPIOE
	0X4002 0C00 - 0x4002 0FFF	GPIOD
	0x4002 0800 - 0x4002 0BFF	GPIOC
	0x4002 0400 - 0x4002 07FF	GPIOB
	0x4002 0000 - 0x4002 03FF	GPIOA

Table 13. STM32F767xx, STM32F768Ax and STM32F769xx register boundary addresses (continued)

Bus	Boundary address	Peripheral
	0x4001 7C00 - 0x4001 FFFF	Reserved
APB2	0x4001 7800 - 0x4001 7BFF	MDIOS
	0x4001 7400 - 0x4001 77FF	DFSDM
	0x4001 6C00 - 0x4001 73FF	DSI Host
	0x4001 6800 - 0x4001 6BFF	LCD-TFT
	0x4001 6000 - 0x4001 67FF	Reserved
	0x4001 5C00 - 0x4001 5FFF	SAI2
	0x4001 5800 - 0x4001 5BFF	SAI1
	0x4001 5400 - 0x4001 57FF	SPI6
	0x4001 5000 - 0x4001 53FF	SPI5
	0x4001 4C00 - 0x4001 4FFF	Reserved
	0x4001 4800 - 0x4001 4BFF	TIM11
	0x4001 4400 - 0x4001 47FF	TIM10
	0x4001 4000 - 0x4001 43FF	TIM9
	0x4001 3C00 - 0x4001 3FFF	EXTI
	0x4001 3800 - 0x4001 3BFF	SYSCFG
	0x4001 3400 - 0x4001 37FF	SPI4
	0x4001 3000 - 0x4001 33FF	SPI1/I2S1
	0x4001 2C00 - 0x4001 2FFF	SDMMC1
	0x4001 2400 - 0x4001 2BFF	Reserved
	0x4001 2000 - 0x4001 23FF	ADC1 - ADC2 - ADC3
	0x4001 1C00 - 0x4001 1FFF	SDMMC2
	0x4001 1800 - 0x4001 1BFF	Reserved
	0x4001 1400 - 0x4001 17FF	USART6
	0x4001 1000 - 0x4001 13FF	USART1
	0x4001 0800 - 0x4001 0FFF	Reserved
	0x4001 0400 - 0x4001 07FF	TIM8
	0x4001 0000 - 0x4001 03FF	TIM1

Table 13. STM32F767xx, STM32F768Ax and STM32F769xx register boundary addresses (continued)

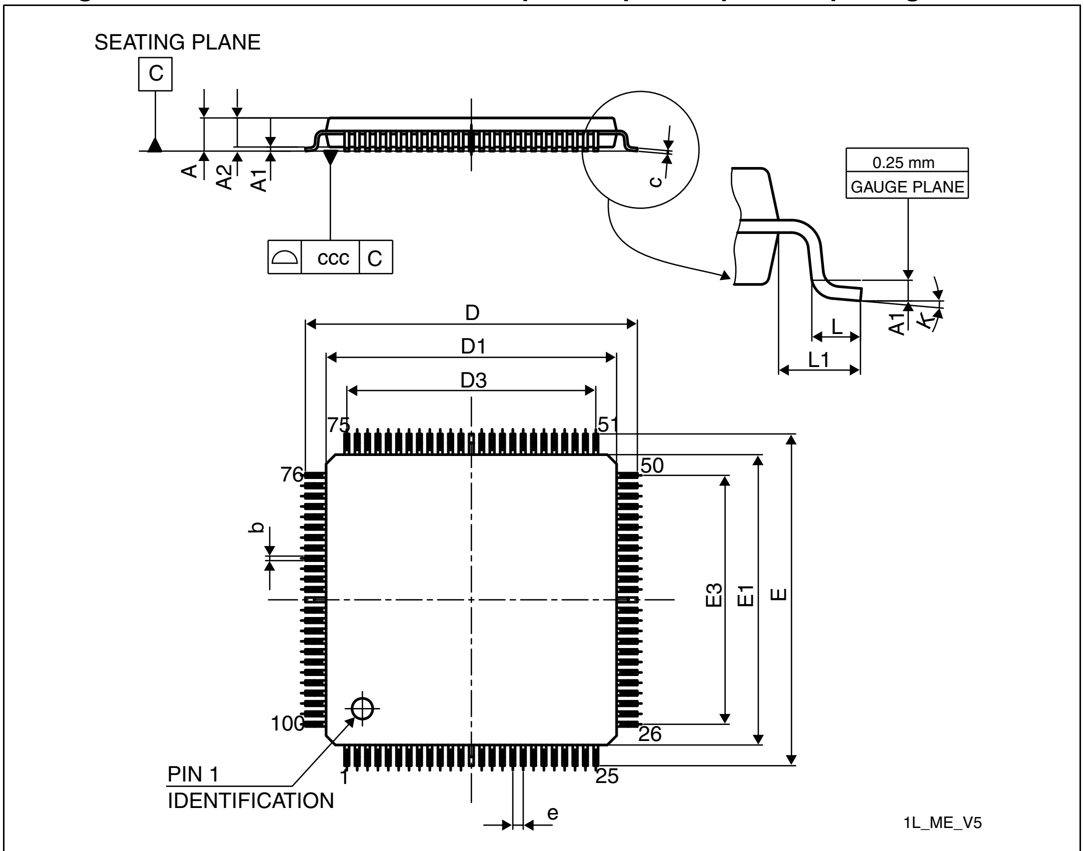
Bus	Boundary address	Peripheral
	0x4000 8000- 0x4000 FFFF	Reserved
APB1	0x4000 7C00 - 0x4000 7FFF	UART8
	0x4000 7800 - 0x4000 7BFF	UART7
	0x4000 7400 - 0x4000 77FF	DAC
	0x4000 7000 - 0x4000 73FF	PWR
	0x4000 6C00 - 0x4000 6FFF	HDMI-CEC
	0x4000 6800 - 0x4000 6BFF	CAN2
	0x4000 6400 - 0x4000 67FF	CAN1
	0x4000 6000 - 0x4000 63FF	I2C4
	0x4000 5C00 - 0x4000 5FFF	I2C3
	0x4000 5800 - 0x4000 5BFF	I2C2
	0x4000 5400 - 0x4000 57FF	I2C1
	0x4000 5000 - 0x4000 53FF	UART5
	0x4000 4C00 - 0x4000 4FFF	UART4
	0x4000 4800 - 0x4000 4BFF	USART3
	0x4000 4400 - 0x4000 47FF	USART2
	0x4000 4000 - 0x4000 43FF	SPDIFRX
	0x4000 3C00 - 0x4000 3FFF	SPI3 / I2S3
	0x4000 3800 - 0x4000 3BFF	SPI2 / I2S2
	0x4000 3400 - 0x4000 37FF	CAN3
	0x4000 3000 - 0x4000 33FF	IWDG
	0x4000 2C00 - 0x4000 2FFF	WWDG
	0x4000 2800 - 0x4000 2BFF	RTC & BKP Registers
	0x4000 2400 - 0x4000 27FF	LPTIM1
	0x4000 2000 - 0x4000 23FF	TIM14
	0x4000 1C00 - 0x4000 1FFF	TIM13
	0x4000 1800 - 0x4000 1BFF	TIM12
	0x4000 1400 - 0x4000 17FF	TIM7
	0x4000 1000 - 0x4000 13FF	TIM6
	0x4000 0C00 - 0x4000 0FFF	TIM5
	0x4000 0800 - 0x4000 0BFF	TIM4
	0x4000 0400 - 0x4000 07FF	TIM3
	0x4000 0000 - 0x4000 03FF	TIM2

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

5.1 LQFP100 14x 14 mm, low-profile quad flat package information

Figure 20. LQFP100, 14 x 14 mm 100-pin low-profile quad flat package outline



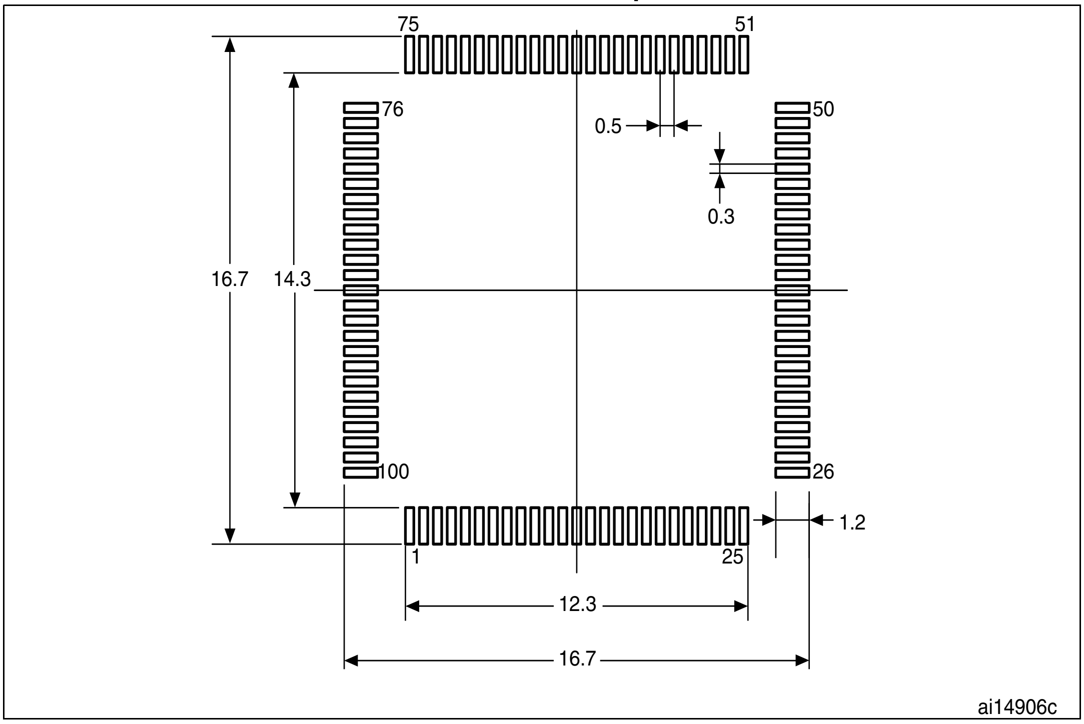
1. Drawing is not to scale.

Table 14. LQPF100, 14 x 14 mm 100-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 21. LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package recommended footprint

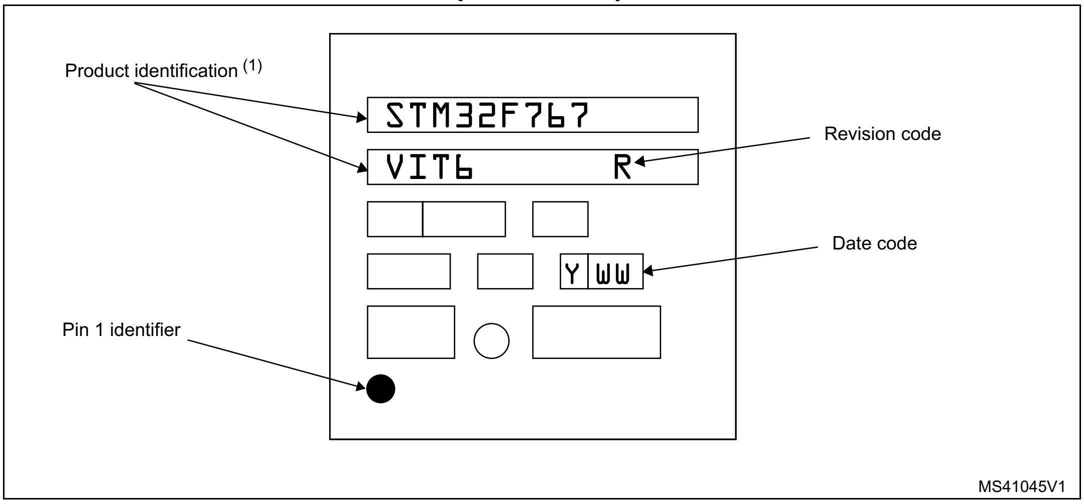


1. Dimensions are expressed in millimeters.

Marking of engineering samples

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

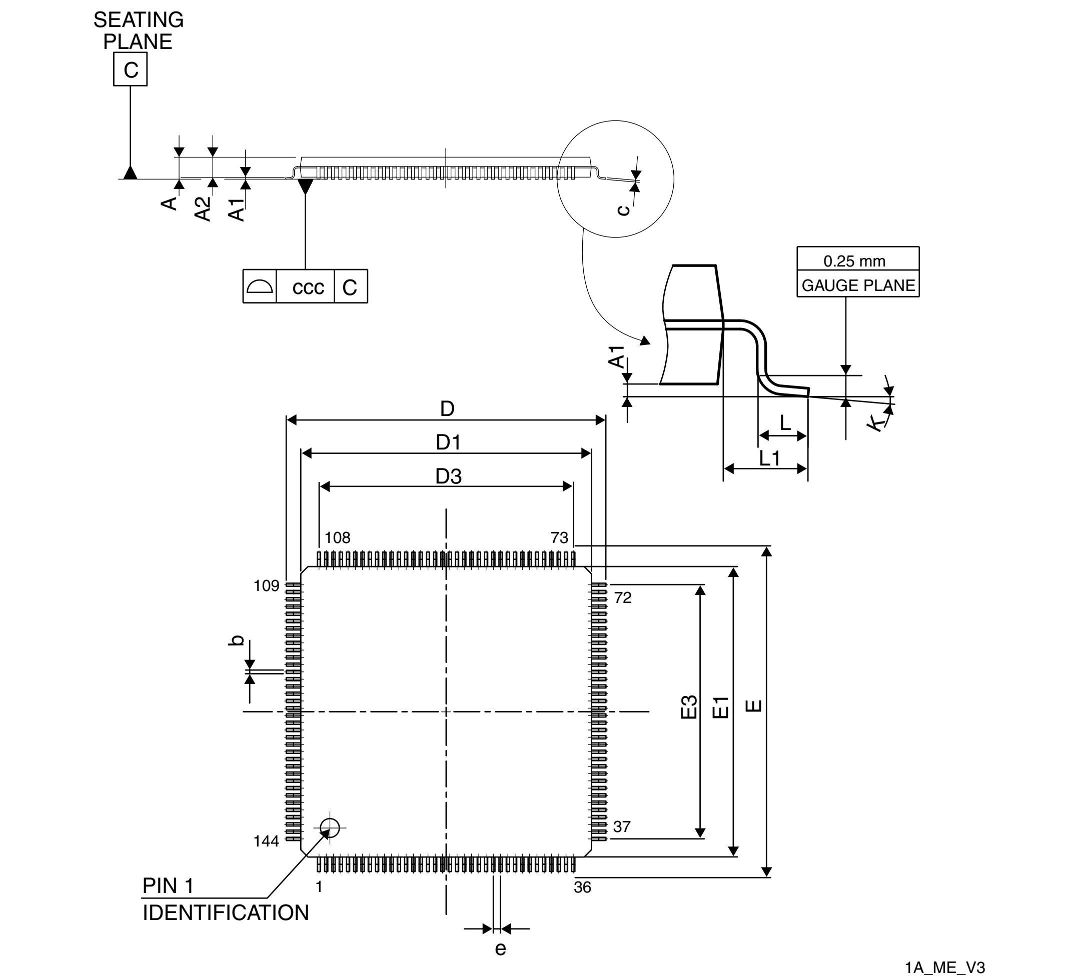
Figure 22. LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

5.2 LQFP144 20 x 20 mm, low-profile quad flat package information

Figure 23. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 15. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package mechanical data

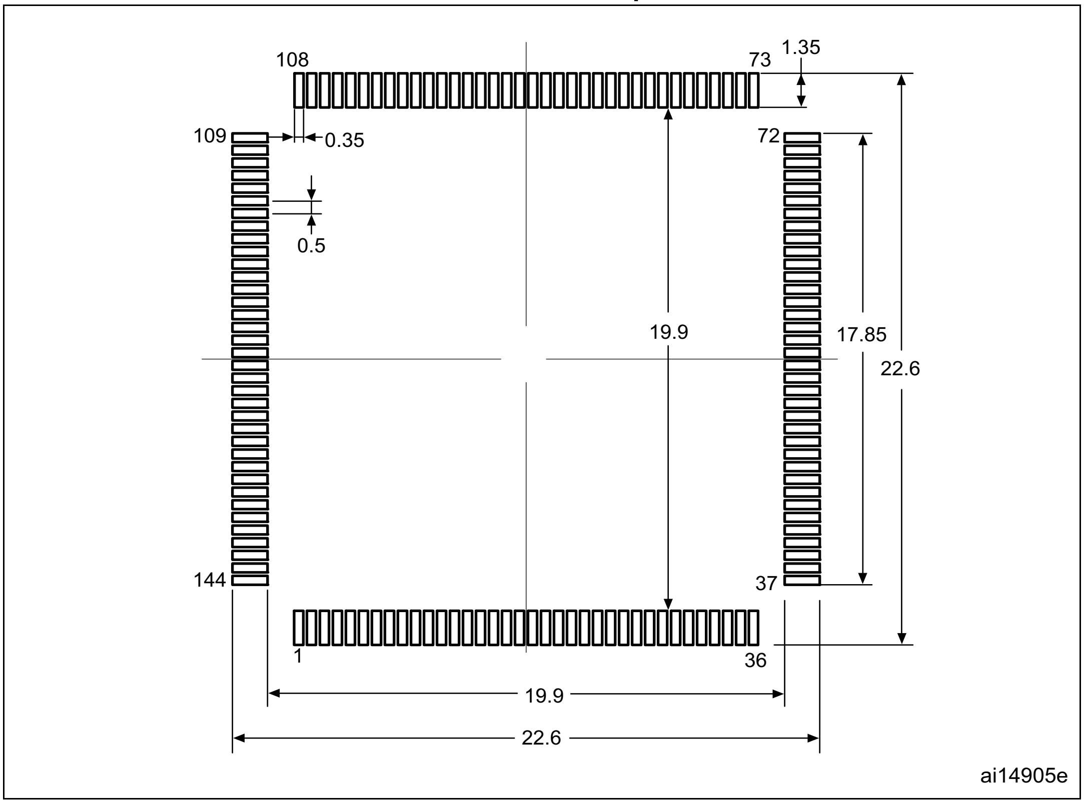
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.874

Table 15. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.689	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 24. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package recommended footprint

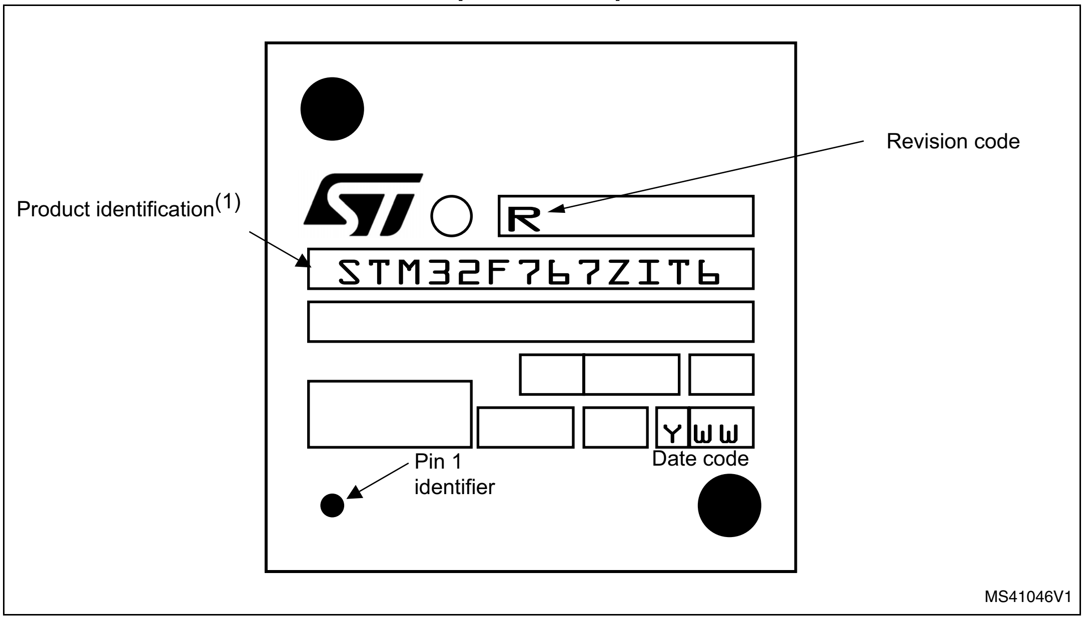


1. Dimensions are expressed in millimeters.

Marking of engineering samples

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

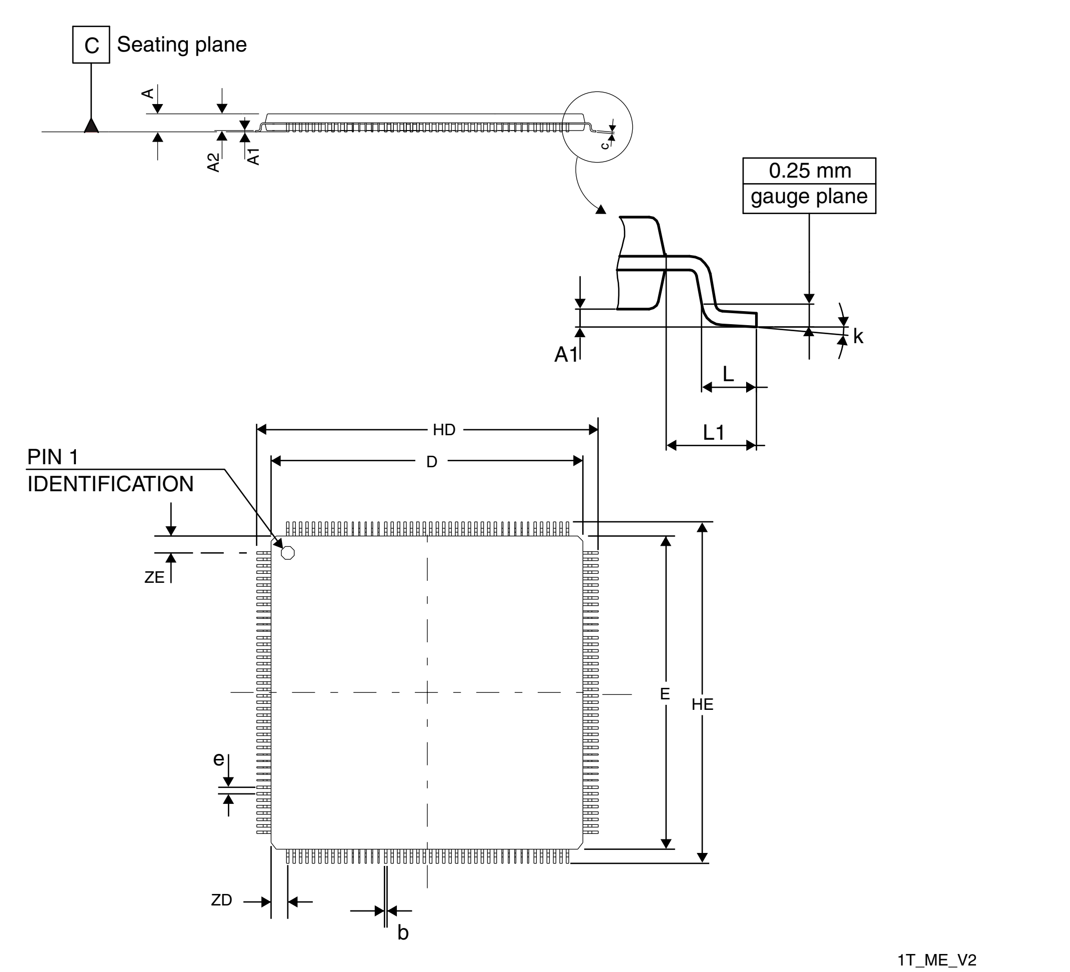
Figure 25. LQFP144, 20 x 20mm, 144-pin low-profile quad flat package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

5.3 LQFP176 24 x 24 mm, low-profile quad flat package information

Figure 26. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 16. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package mechanical data

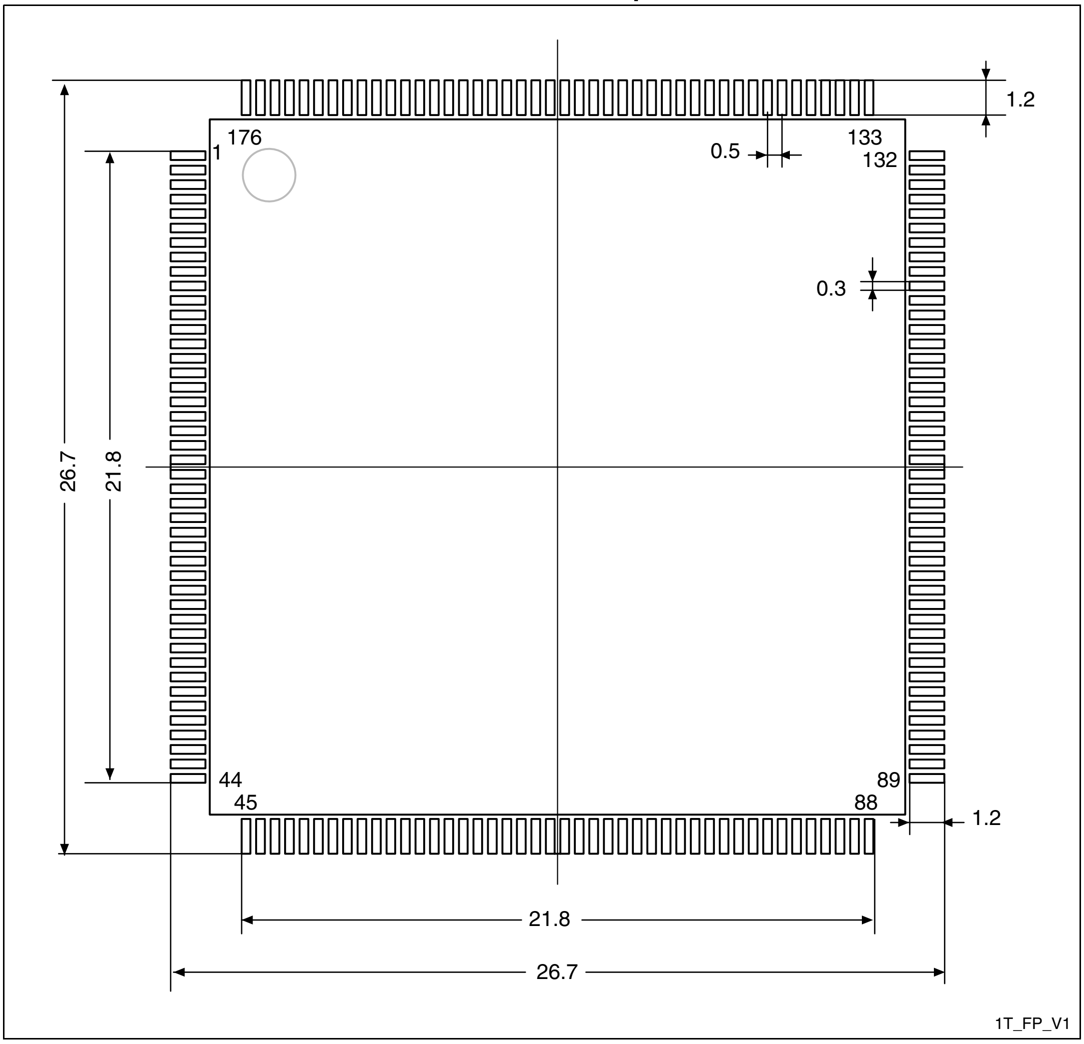
Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	-	1.450	0.0531	-	0.0060
b	0.170	-	0.270	0.0067	-	0.0106
C	0.090	-	0.200	0.0035	-	0.0079
D	23.900	-	24.100	0.9409	-	0.9488

Table 16. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
E	23.900	-	24.100	0.9409	-	0.9488
e	-	0.500	-	-	0.0197	-
HD	25.900	-	26.100	1.0200	-	1.0276
HE	25.900	-	26.100	1.0200	-	1.0276
L	0.450	-	0.750	0.0177	-	0.0295
L1	-	1.000	-	-	0.0394	-
ZD	-	1.250	-	-	0.0492	-
ZE	-	1.250	-	-	0.0492	-
ccc	-	-	0.080	-	-	0.0031
k	0 °	-	7 °	0 °	-	7 °

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 27. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package recommended footprint

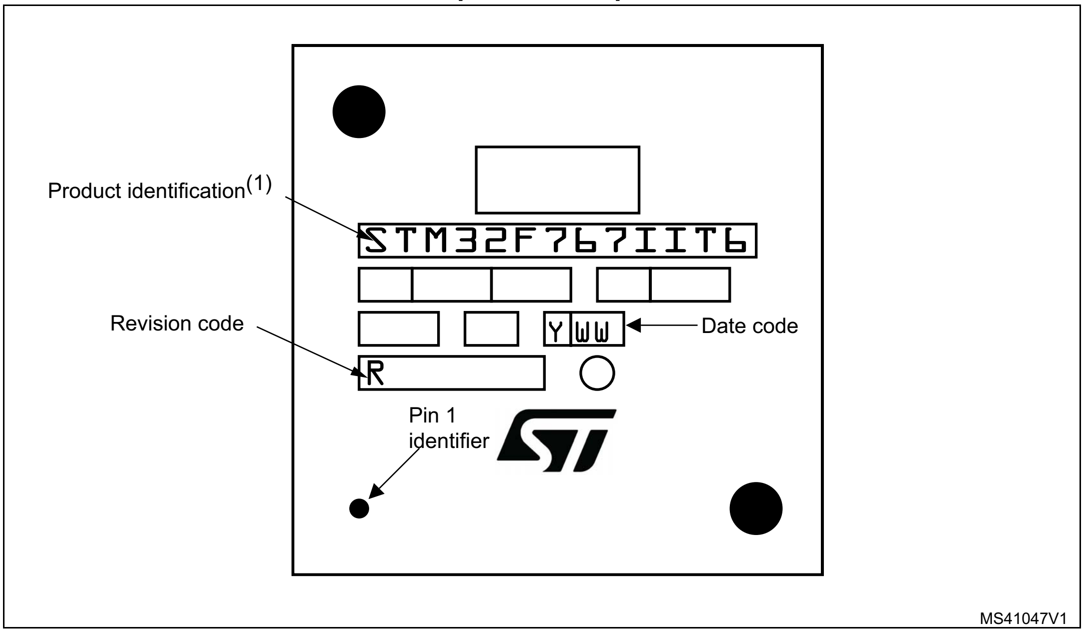


1. Dimensions are expressed in millimeters.

Marking of engineering samples

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

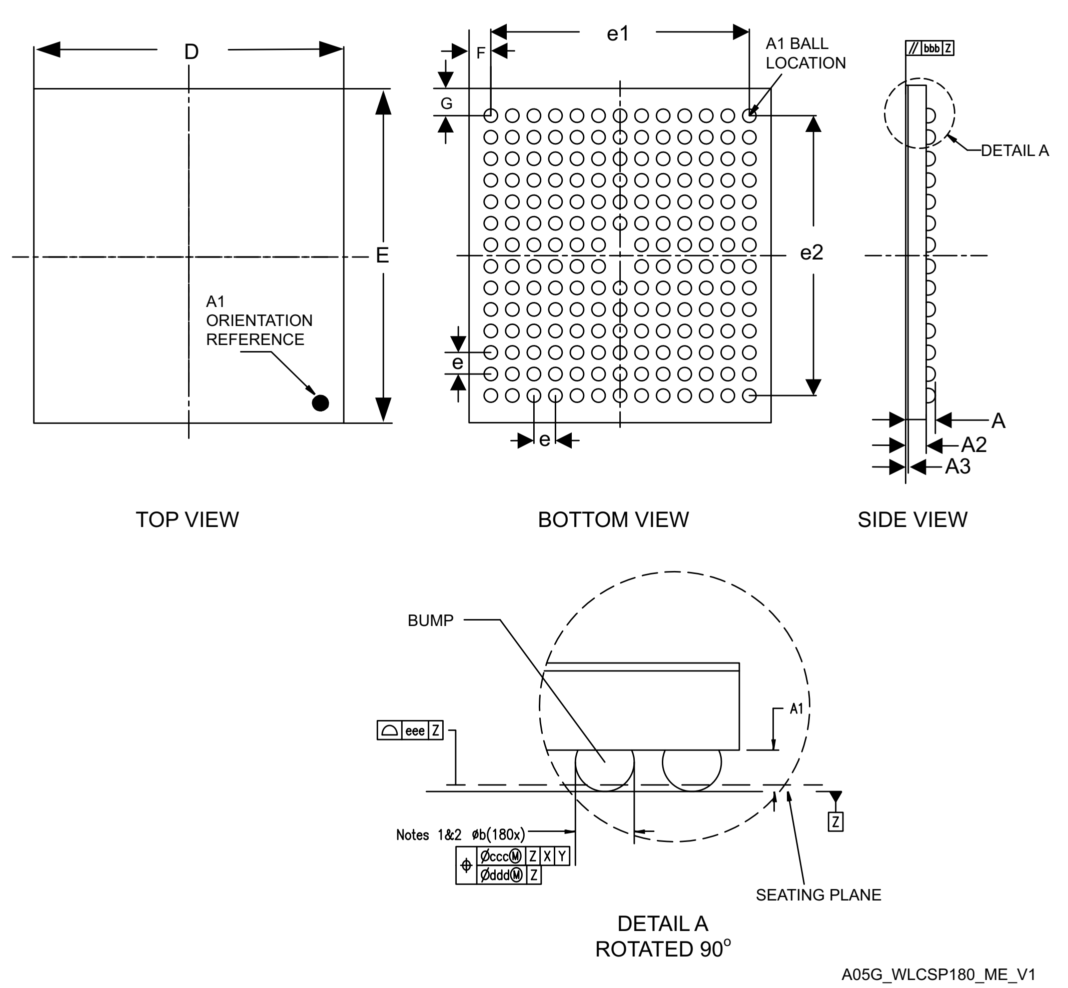
Figure 28. LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

5.4 WLCSP 180-bump, 5.5 x 6 mm, wafer level chip scale package information

Figure 29. WLCSP 180-bump, 5.5 x 6 mm, 0.4 mm pitch wafer level chip scale package outline



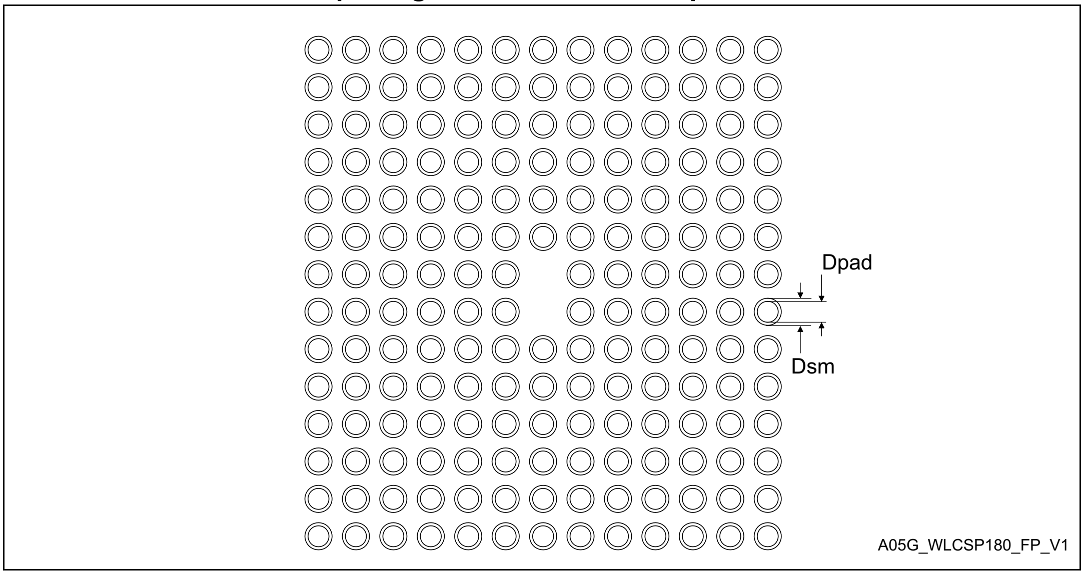
1. Drawing is not to scale.

Table 17. WLCSP 180-bump, 5.5 x 6 mm, 0.4 mm pitch wafer level chip scale package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.230
A1	-	0.175	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3	-	0.025	-	-	0.0010	-
b[2]	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	5.502	5.537	5.572	0.2166	0.2180	0.2194
E	6.060	6.095	6.130	0.2386	0.2400	0.2413
e	-	0.400	-	-	0.0157	-
e1	-	4.800	-	-	0.1890	-
e2	-	5.200	-	-	0.2047	-
F	-	0.368	-	-	0.0145	-
G	-	0.477	-	-	0.0188	-
aaa	-	0.110	-	-	0.0043	-
bbb	-	0.110	-	-	0.0043	-
ccc	-	0.110	-	-	0.0043	-
ddd	-	0.050	-	-	0.0020	-
eee	-	0.050	-	-	0.0020	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 30. WLCSP 180-bump, 5.5 x 6 mm, 0.4 mm pitch wafer level chip scale package recommended footprint



1. Dimensions are expressed in millimeters.

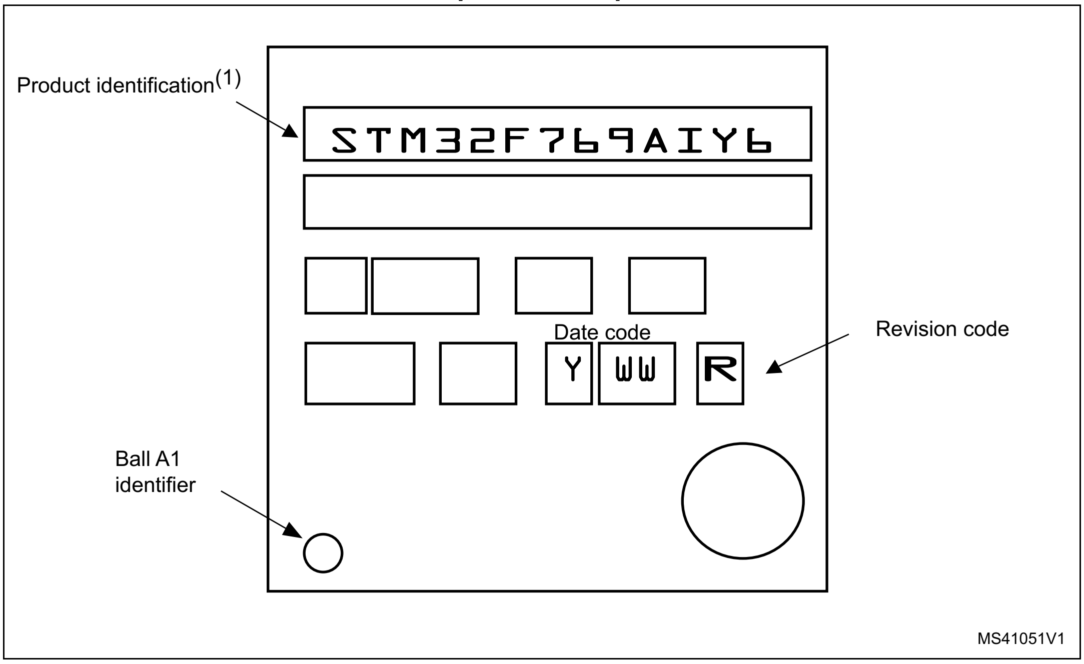
Table 18. WLCSP 180-bump, 5.5 x 6 mm, recommended PCB design rules (0.4 mm pitch)

Dimension	Recommended values
Pitch	0.4
Dpad	0.225 mm
Dsm	0.290 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.1 mm

Marking of engineering samples

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

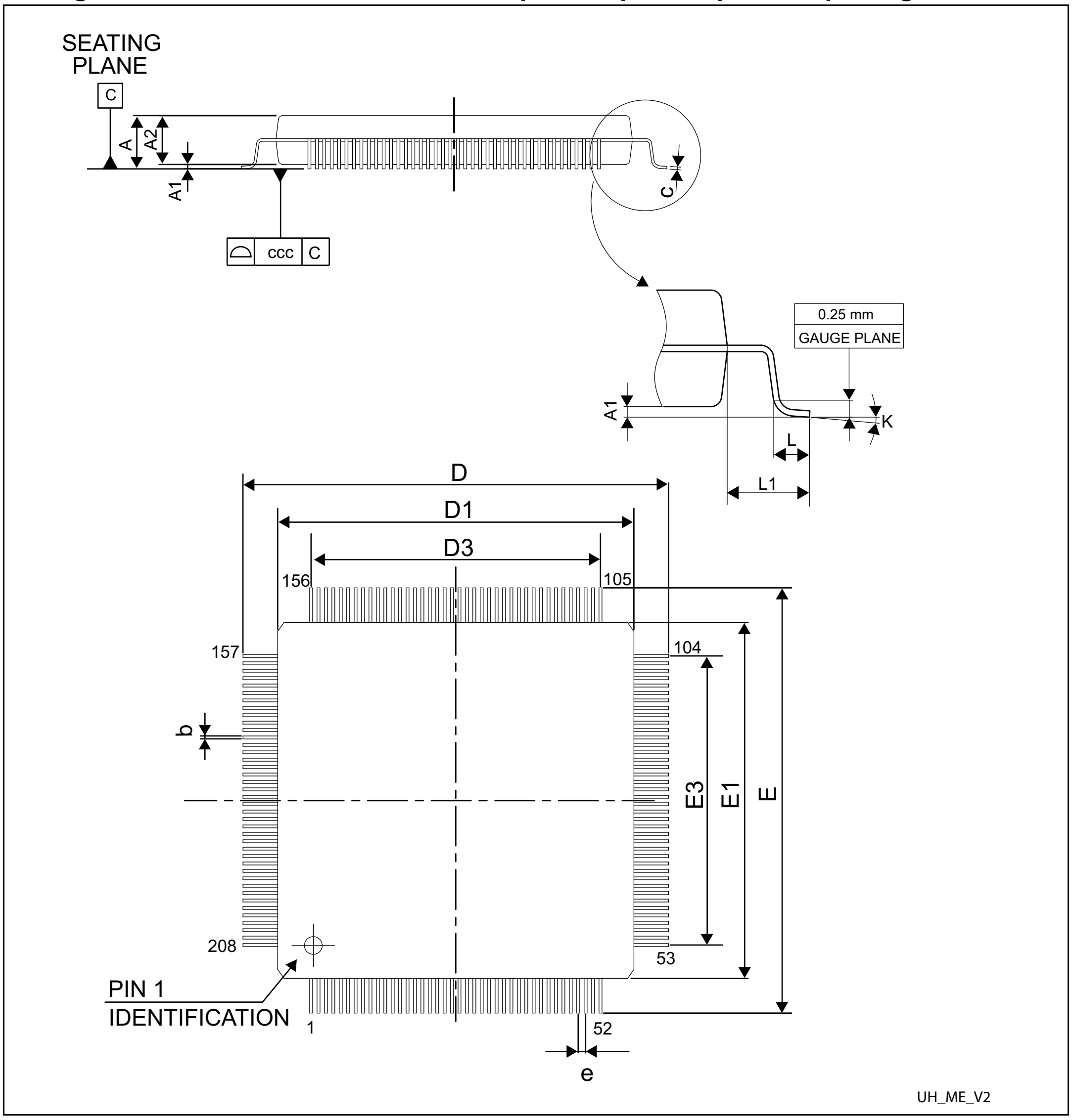
Figure 31. WLCSP180-bump, 5.5 x 6 mm, 0.4 mm pitch wafer level chip scale package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

5.5 LQFP208 28 x 28 mm low-profile quad flat package information

Figure 32. LQFP208, 28 x 28 mm, 208-pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 19. LQFP208, 28 x 28 mm, 208-pin low-profile quad flat package mechanical data

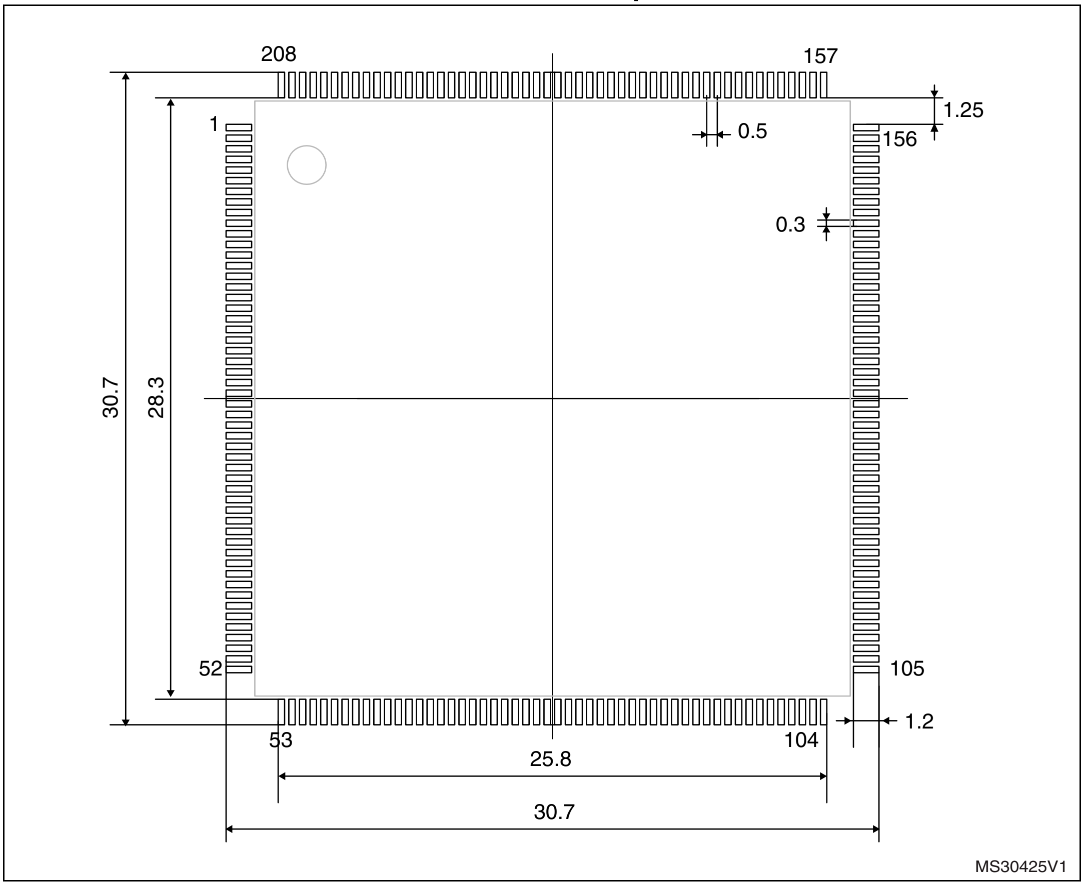
Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	--	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571

Table 19. LQFP208, 28 x 28 mm, 208-pin low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[(1)]		
	Min	Typ	Max	Min	Typ	Max
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	29.800	30.000	30.200	1.1732	1.1811	1.1890
D1	27.800	28.000	28.200	1.0945	1.1024	1.1102
D3	-	25.500	-	-	1.0039	-
E	29.800	30.000	30.200	1.1732	1.1811	1.1890
E1	27.800	28.000	28.200	1.0945	1.1024	1.1102
E3	-	25.500	-	-	1.0039	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7.0°	0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 33. LQFP208, 28 x 28 mm, 208-pin low-profile quad flat package recommended footprint

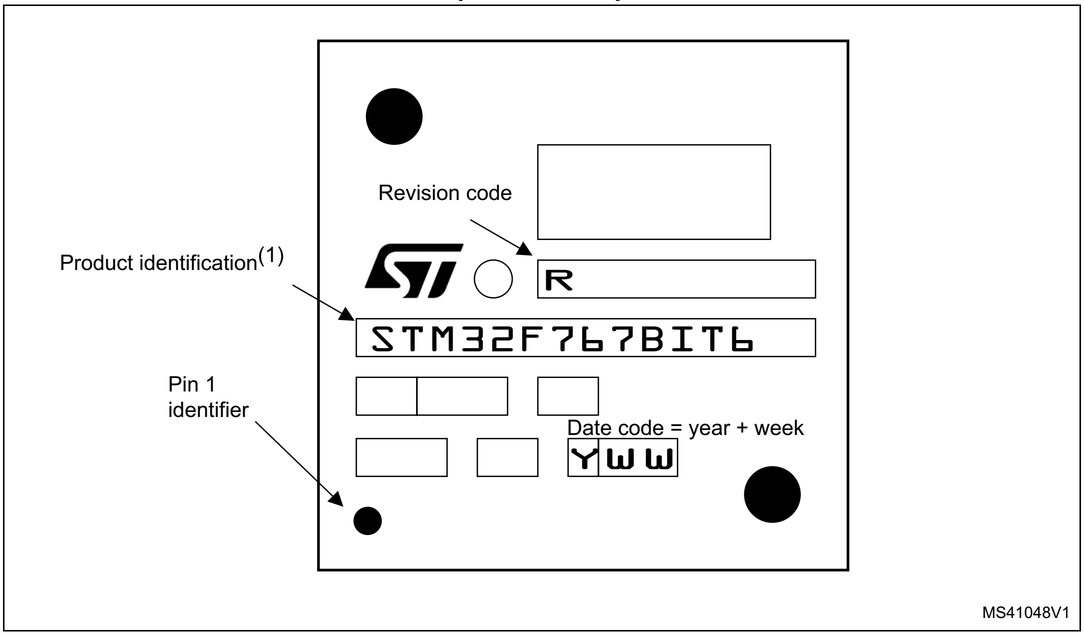


1. Dimensions are expressed in millimeters.

Marking of engineering samples

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

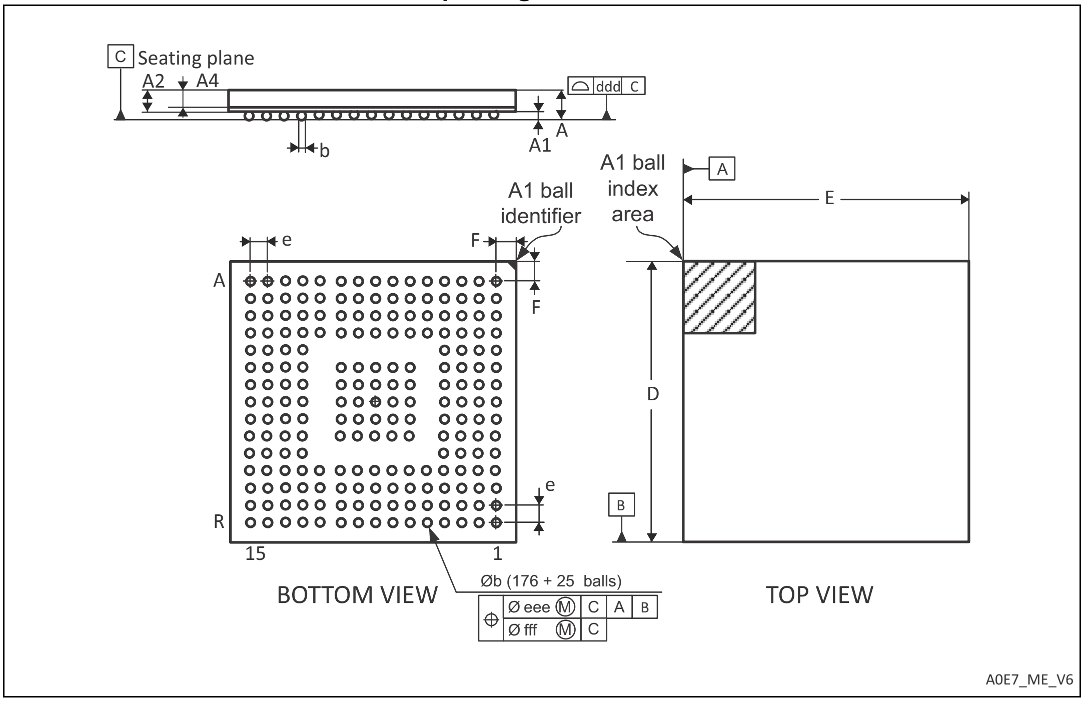
Figure 34. LQFP208, 28 x 28 mm, 208-pin low-profile quad flat package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

5.6 UFBGA176+25, 10 x 10, 0.65 mm ultra thin fine-pitch ball grid array package information

Figure 35. UFBGA176+25, 10 × 10 × 0.65 mm ultra thin fine-pitch ball grid array package outline



1. Drawing is not to scale.

Table 20. UFBGA176+25, 10 × 10 × 0.65 mm ultra thin fine-pitch ball grid array package mechanical data

Symbol	millimeters			inches[(1)]		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.002	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
b	0.230	0.280	0.330	0.0091	0.0110	0.0130
D	9.950	10.000	10.050	0.3917	0.3937	0.3957
E	9.950	10.000	10.050	0.3917	0.3937	0.3957
e	-	0.650	-	-	0.0256	-
F	0.400	0.450	0.500	0.0157	0.0177	0.0197
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 36. UFBGA176+25, 10 x 10 mm x 0.65 mm, ultra fine-pitch ball grid array package recommended footprint

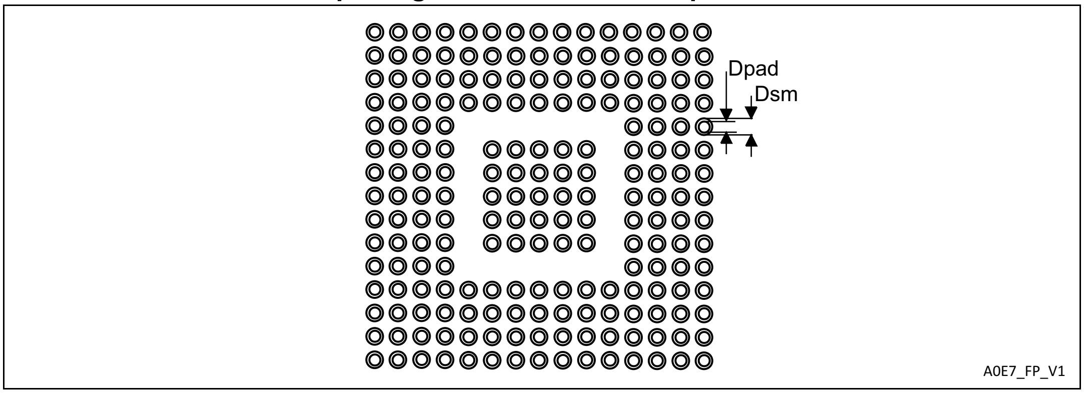


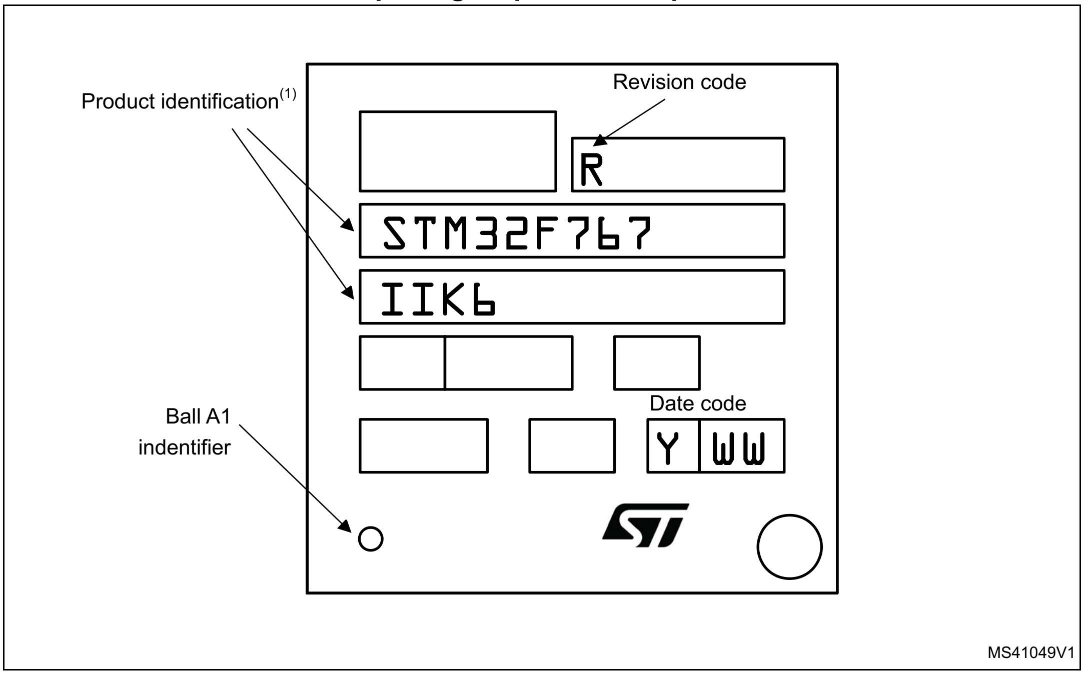
Table 21. UFBGA176+25 recommended PCB design rules (0.65 mm pitch BGA)

Dimension	Recommended values
Pitch	0.65 mm
Dpad	0.300 mm
Dsm	0.400 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.300 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm

Marking of engineering samples

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

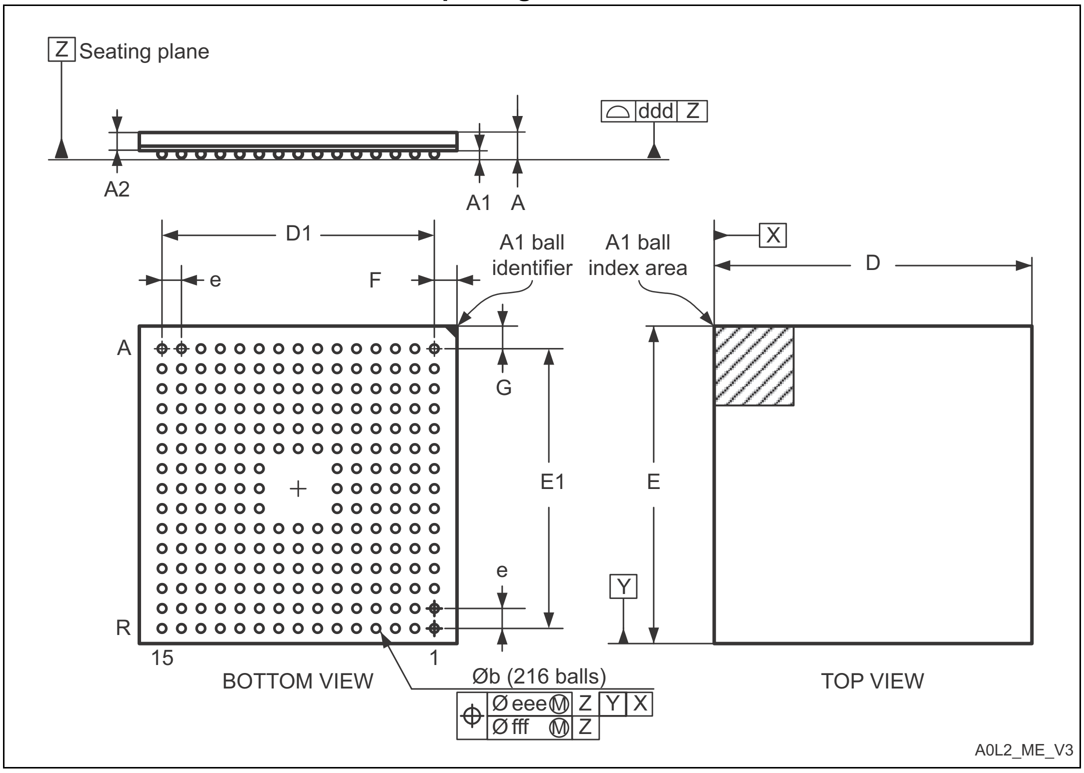
Figure 37. UFBGA176+25, 10 × 10 × 0.6 mm ultra thin fine-pitch ball grid array package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

5.7 TFBGA216, 13 x 13 x 0.8 mm thin fine-pitch ball grid array package information

Figure 38. TFBGA216, 13 × 13 × 0.8 mm thin fine-pitch ball grid array package outline



1. Drawing is not to scale.

Table 22. TFBGA216, 13 × 13 × 0.8 mm thin fine-pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.100	-	-	0.0433
A1	0.150	-	-	0.0059	-	-
A2	-	0.760	-	-	0.0299	-
b	0.350	0.400	0.450	0.0138	0.0157	0.0177
D	12.850	13.000	13.150	0.5118	0.5118	0.5177
D1	-	11.200	-	-	0.4409	-
E	12.850	13.000	13.150	0.5118	0.5118	0.5177
E1	-	11.200	-	-	0.4409	-
e	-	0.800	-	-	0.0315	-
F	-	0.900	-	-	0.0354	-

Table 22. TFBGA216, 13 × 13 × 0.8 mm thin fine-pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
G	-	0.900	-	-	0.0354	-
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 39. TFBGA216, 13 x 13 mm, 0.8 mm pitch, thin fine-pitch ball grid array package recommended footprint

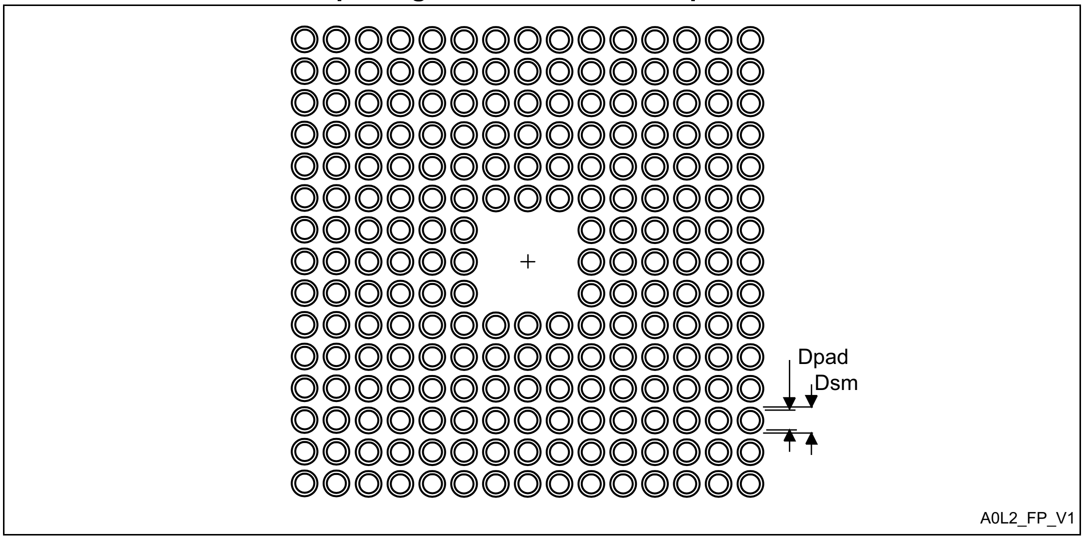


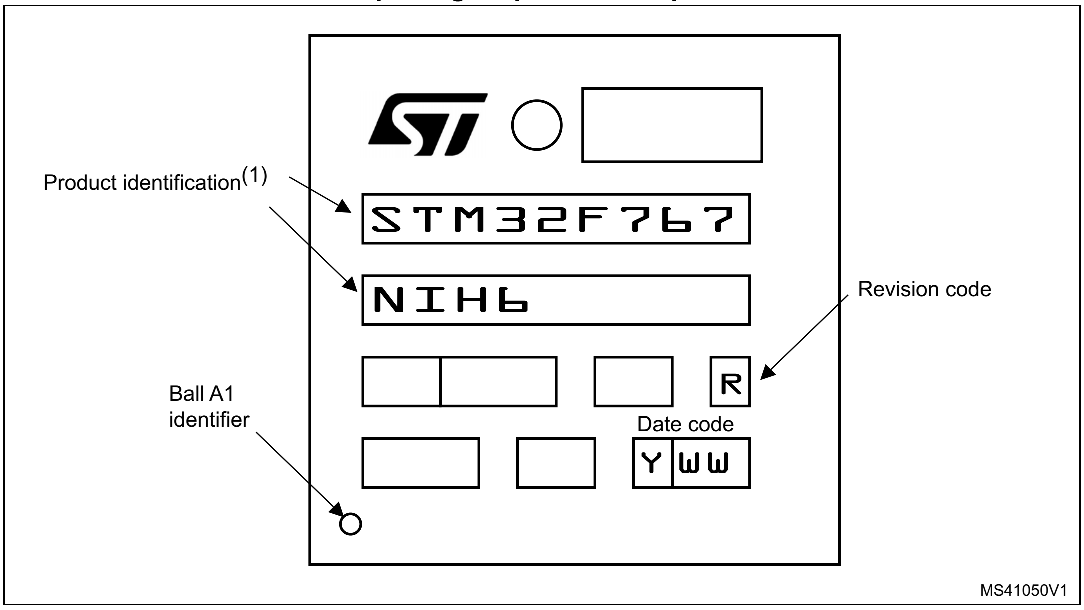
Table 23. TFBGA216 recommended PCB design rules (0.8 mm pitch BGA)

Dimension	Recommended values
Pitch	0.8
Dpad	0.400 mm
Dsm	0.470 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.400 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.120 mm

Marking of engineering samples

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Figure 40. TFBGA216, 13 × 13 × 0.8mm thin fine-pitch ball grid array package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

5.8 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

T_J max = T_A max + (P_D max x Θ_{JA})

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O}$ max = Σ (V_{OL} × I_{OL}) + Σ((V_{DD} – V_{OH}) × I_{OH}),

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 24. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP100 - 14 × 14 mm / 0.5 mm pitch	43	°C/W
	Thermal resistance junction-ambient WLCSP180 - 0.4 mm pitch	30	
	Thermal resistance junction-ambient LQFP144 - 20 × 20 mm / 0.5 mm pitch	40	
	Thermal resistance junction-ambient LQFP176 - 24 × 24 mm / 0.5 mm pitch	38	
	Thermal resistance junction-ambient LQFP208 - 28 × 28 mm / 0.5 mm pitch	19	
	Thermal resistance junction-ambient UFBGA176 - 10× 10 mm / 0.5 mm pitch	39	
	Thermal resistance junction-ambient TFBGA216 - 13 × 13 mm / 0.8 mm pitch	29	

Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

6 Part numbering

Table 25. Ordering information scheme

Example:	STM32	F	76x	V	G	T	6	xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

767= STM32F767xx, USB OTG FS/HS, camera interface, Ethernet, LCD-TFT
768 = STM32F768Ax, USB OTG FS/HS, camera interface, DSI host, WLCSP with internal regulator OFF
769= STM32F769xx, USB OTG FS/HS, camera interface, Ethernet, DSI host

Pin count

V = 100 pins
Z = 144 pins
I = 176 pins
A = 180 pins
B = 208 pins
N = 216 pins

Flash memory size

G = 1024 Kbytes of Flash memory
I = 2048 Kbytes of Flash memory

Package

T = LQFP
K = UFBGA
H = TFBGA
Y = WLCSP

Temperature range

6 = Industrial temperature range, –40 to 85 °C.
7 = Industrial temperature range, –40 to 105 °C.

Options

xxx = programmed parts
TR = tape and reel

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

Appendix A Recommendations when using internal reset OFF

When the internal reset is OFF, the following integrated features are no longer supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled
- The brownout reset (BOR) circuitry must be disabled
- The embedded programmable voltage detector (PVD) is disabled
- V_{BAT} functionality is no more available and VBAT pin should be connected to V_{DD}
- The over-drive mode is not supported

A.1 Operating conditions

Table 26. Limitations depending on the operating power supply range

Operating power supply range	ADC operation	Maximum Flash memory access frequency with no wait states ($f_{Flashmax}$)	Maximum Flash memory access frequency with wait states [1][2]	I/O operation	Possible Flash memory operations
V_{DD} =1.7 to 2.1 V[3]	Conversion time up to 1.2 Msps	20 MHz	168 MHz with 8 wait states and over-drive OFF	– No I/O compensation	8-bit erase and program operations only

1. Applicable only when the code is executed from Flash memory. When the code is executed from RAM, no wait state is required.
2. Thanks to the ART accelerator on ITCM interface and L1-cache on AXI interface, the number of wait states given here does not impact the execution speed from the Flash memory since the ART accelerator or L1-cache allows to achieve a performance equivalent to 0-wait state program execution.
3. V_{DD}/V_{DDA} minimum value of 1.7 V, with the use of an external power supply supervisor (refer to *Section 2.18.1: Internal reset ON*).

Revision history

Table 27. Document revision history

Date	Revision	Changes
27-Aug-2015	1	Initial release.
05-Oct-2015	2	Added WLCSP180 package: – Updated *Table 10: STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions*. – Updated figure in the cover page. – Added *Figure 13: STM32F769xx/STM32F768Ax WLCSP180 ballout*. – Updated *Table 4: Regulator ON/OFF and internal reset ON/OFF availability*. – Updated *Table 2: STM32F767xx, STM32F768Ax and STM32F769xx features and peripheral counts*. – Updated *Table 24: Package thermal characteristics*. – Updated *Table 25: Ordering information scheme* adding A for 180 pins. Updated *Section 2.24: Inter-integrated circuit interface (I2C)* adding Fast-mode plus.
05-Jan-2016	3	Updated *Section 2.25: Universal synchronous/asynchronous receiver transmitters (USART)*. Updated *Table 4: Regulator ON/OFF and internal reset ON/OFF availability* adding WLCSP180 information. Updated *Table 2: STM32F767xx, STM32F768Ax and STM32F769xx features and peripheral counts* STM32F76xAx by STM32F769Ax. Added *Section 5.4: WLCSP 180-bump, 5.5 x 6 mm, wafer level chip scale package information* package information. Updated *Table 10: STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions* adding note 1. Updated the whole databrief adding STM32F768Ax devices. Updated the whole databrief increasing the frequencies from 50 MHz, 100 MHz and 200MHz to 54 MHz, 108 MHz and 216 MHz respectively.

Table 27. Document revision history (continued)

Date	Revision	Changes
07-Jan-2016	4	Updated cover page replacing 12.5 Mbit/s by 27 Mbit/s.
03-Mar-2016	5	Updated *Table 24: Package thermal characteristics* adding WLCSP180 RTH. updated *Table 25: Ordering information scheme*. Added marking example for all packages. Updated *Table 2: STM32F767xx, STM32F768Ax and STM32F769xx features and peripheral counts* ethernet feature not available for WLCSP180 package. Updated *Section 2.17: Power supply schemes* replacing VDDMMC by VDDSDMMC. Updated *Table 10: STM32F767xx, STM32F768Ax and STM32F769xx pin and ball definitions* WKUP and WLCSP180 Qx pins. Updated *Figure 13: STM32F769xx/STM32F768Ax WLCSP180 ballout* replacing “Q” by “P” row. Updated *Figure 2: STM32F767xx, STM32F768Ax and STM32F769xx block diagram*. Added *Figure 12: STM32F769xx LQFP176 pinout* with DSI. Updated *Table 26: Limitations depending on the operating power supply range* changing note 3 and removing note 4. Updated *Section 2.33: Controller area network (bxCAN)* with SRAM allocation for CAN1, CAN2 and CAN3.