Circuit Theory and Electronics Fundamentals

Aerospace Engineering, Técnico, University of Lisbon

T4 Laboratory Report

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Contents

1 Introduction

The objective of this laboratory assignment is to study an audio amplifier. This circuit is made up of a gain stage and an output stage. The format of the circuit can be seen in Figure 1. And the provided circuit can be seen in Figure 2.

In Section 3, a theoretical analysis of the circuit is presented. In Section 2, the circuit is analysed by means of a ngspice simulation. The results are then compared to the theoretical results obtained in Section 3. The conclusions of this study are outlined in Section 4.

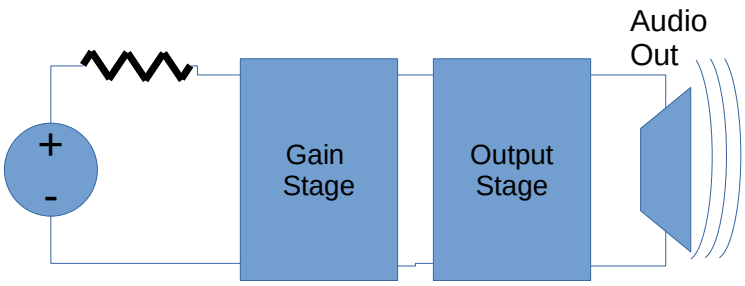


Figure 1: Assigned Circuit.

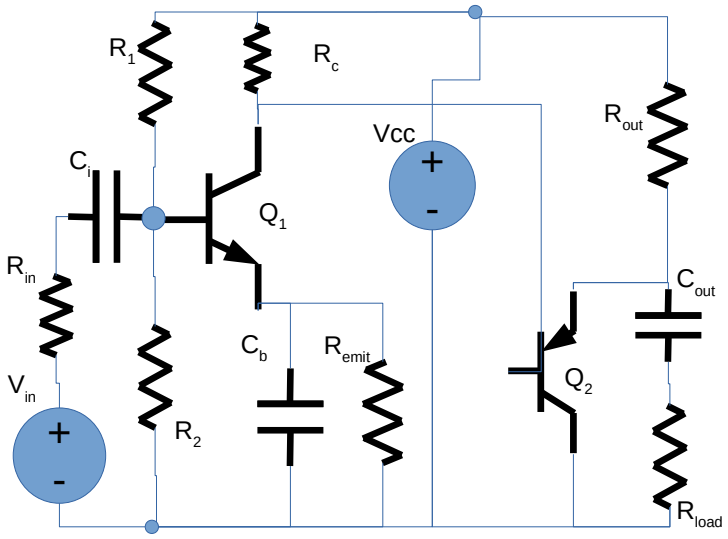


Figure 2: Chosen Circuit.

2 Simulation Analysis

2.1 Incremental Modifications

In order to maximize the M value, we used the provided circuit, and tried to make small changes and evaluate their results. The main changes were to the value of the parameters of the bypass and input capacitors.

Keeping in mind the effects of this changes, which was talked about in previous lectures, it was quick to obtain a set of values that are taken to be optimal.

2.1.1 Coupling capacitor

Since the source has 0V DC value which we do not want, there is a need to add a coupling capacitor, which blocks the 0V DC component of V_s, which will that act as an open circuit at low frequencies. This will lower the lower cut-off frequency, which will increase the bandwidth.

2.1.2 Bypass capacitor

The bypass capacitor, is a much needed component of the circuit, since it will function as an open circuit for low frequencies (DC) and a short circuit for higher frequencies(AC), this will solve the problem of using the resistor R_E, while keeping the benefits of stabilizing the gain in case of temperature variation in DC without the disadvantage of the decrease in the gain in higher frequencies. In medium to high frequencies most of the current will go through the capacitor, since it gets closer to an open circuit, increasing the gain.

2.1.3 Effect of Rc on the gain

Increasing Rc increases the gain of the circuit. This makes it similar gain controls in common analog appliances, where a knob potentiometer can be easily user controlled. Just as in common appliances, if we increase the gain too much the output starts to get ”muddy” or distorted, a sound that many enthusiasts enjoy. Increasing the Rc value increases the output impedance, which widens the gap between input and output impedences.

2.1.4 Cost

Component	Parameter Value
C_{in}	1 μF
R_1	80 kΩ
R_2	20 kΩ
R_C	1 kΩ
R_e	0.1 kΩ
C_b	80 μF
R_{out}	0.3 kΩ
C_o	35 μF
Transistors	0.1 MU (x2)
Total cost	217.6 MU

Table 1: Table of costs. Note that the total cost is sum of the the other values (in this units, with the number of diodes multiplied by 0.1).

2.2 Spice Results

Using the values stated above and using them in a simulated circuit in ngspice as shown in the circuit shown in Figure 2 we obtain the following results.

Parameter	Value
Voltage Gain	41.182360
lowerCutoffFreq	772.319000
higherCutoffFreq	1815086.000000
bandwith	1814313.681000
input impedence	-0.557916 + i0.106270 kohm
output impedence	7.937756 ohm
Cost	217.600000
M	444.598503

Table 2: Spice results. The M value and the cost were calculated by an additional octave script included in the git.

Note that the transistors are working in the F.A.R.. The operating point below shows that $V_{CE} > V_{BE}$ and $V_{EC} > V_{EB}$.

	V(v)
VCE	2.6265 V
VBE	0.708349 V

	V(v)
VEC	4.24296 V
VEB	0.746287 V

3 Theoretical Analysis

3.1 Operating Point

First transistor (npn)

The current through the base of the first transistor is given by

$$I_{B1} = (V_{eq} - V_{BEon})/(R_B + (1 + \beta_{FN}) \cdot R_{E1}$$

The current through the collector of the first transistor is given by

$$I_{C1} = \beta_{FN} \cdot I_{B1}$$

The current through the emitter of the first transistor is given by

$$I_{E1} = (1 + \beta_{FN}) \cdot I_{B1}$$

The voltage drop from the emitter to the collector of the first transistor is given by

$$V_{EC1} = V_{O1} - R_{E1} \cdot I_{E1}$$

The voltage drop from the emitter to the base of the first transistor is given by

$$V_{EB1} = V_{EBon}$$

By applying the previous formulas, one can obtain

	I (A)
IB1	0.000024
IC1	0.004345
IE1	0.004370

	V (V)
VBE1	0.700000
VCE1	6.343628

NGSpice results

	V(v)
VCE	2.6265 V
VBE	0.708349 V

Second transistor (pnp)

The current through the base of the first transistor is given by

$$I_{B2} = I_{E2} - I_{C2}$$

The current through the collector of the first transistor is given by

$$\beta_{FP}/(\beta_{FP} + 1) \cdot I_{E2}$$

The current through the emitter of the first transistor is given by

$$I_{E2} = (V_{CC} - V_{EBon} - V_{I2})/R_{E2}$$

The voltage drop from the emitter to the collector is given by

$$V_{EC2} = V_O$$

The voltage drop from the emitter to the base is given by

$$V_{EB2} = V_{EBon}$$

	I (A)
IB2	0.000053
IC2	0.012098
IE2	0.012151

	V (V)
VEB2	0.700000
VEC2	8.354556

NGSpice results

	V(v)
VEC	4.24296 V
VEB	0.746287 V

Comparation of OP

The values of V_{EB} are similar because it was an approximation of experimental results.

The values of V_{EC} are not as colse as the previous one, but the order of magnitude is the same in both cases.

Furthermore, in both cases, it is possible to conclude that the transistors are working in forward active region (F.A.R.), since $V_{CE} > V_{BE}$ and $V_{EC} > V_{EB}$.

3.2 Gain, Input and Output Impedances

The input and output impedances of the first transistor is given by, respectively,

$$Z_{i1} = \frac{1}{\frac{1/R_b+1}{((r_{o1}+R_{c1}+R_{e1})\cdot(r_{\pi1}+R_{e1})+g_{m1}\cdot R_{e1}\cdot r_{o1}\cdot r_{\pi1}-R_{e1}^2)/(r_{o1}+R_{c1}+R_{e1})}}$$

$$Z_{o1} = \frac{1}{1/r_{o1} + 1/R_{c1}}$$

The gain of the first transistor is given by

$$gain_1 = R_{sb}/R_s \cdot R_{c1} \cdot \frac{R_{e1} - g_{m1} \cdot r_{\pi1} \cdot r_{o1}}{(r_{o1} + R_{c1} + R_{e1}) \cdot (R_{sb} + r_{\pi1} + R_{e1}) + g_{m1} \cdot R_{e1} \cdot r_{o1} \cdot r_{\pi1} - R_{e1}^2}$$

The input and output impedances of the second transistor can be given by, respectively,

$$Z_{i2} = \frac{g_{m2} + g_{\pi2} + g_{o2} + g_{e2}}{g_{\pi2}/(g_{\pi2} + g_{o2} + g_{e2}}$$

$$Z_{o2} = 1/(g_{m2} + g_{\pi2} + g_{o2} + g_{e2})$$

The gain of the second transistor is given by

$$gain_2 = \frac{g_{m2}}{g_{m2} + g_{\pi 2} + g_{o2} + g_{e2}}$$

This yields,

	Z (ohm)
Zi1	966.016357
Zi2	39743.365908
Zi	966.016357
Zo1	941.313822
Zo2	2.041992
Zo	6.043845

Because the input impedance is 161 times bigger then the ouput impedance, they can be connected without significant signal loss.

3.3 Frequency Response

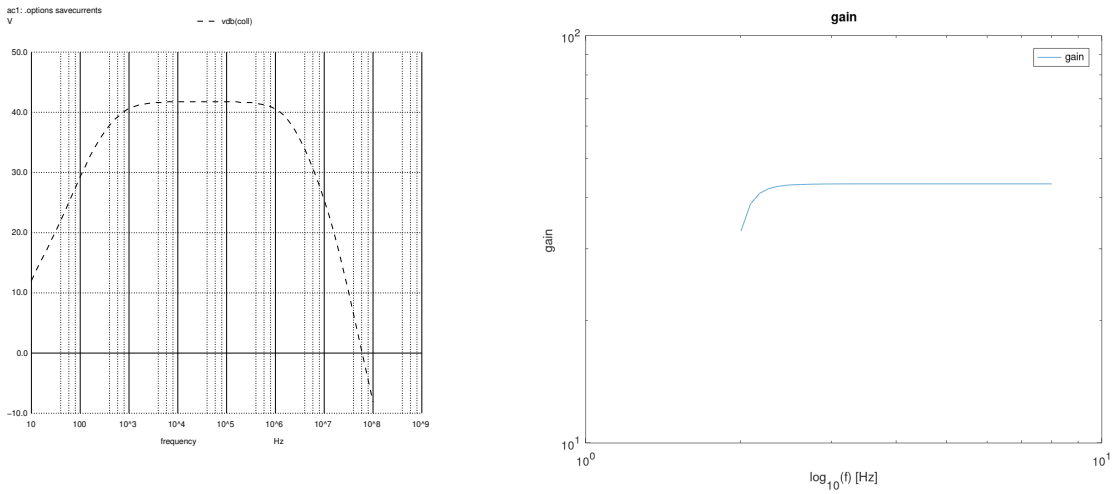
Gain Stage

The results differ a little bit in the first stage of the graphic and are similar after that, until it starts to decrease.

The reason for that is that it is assumed that for lower frequencies the capacitor in series with V_in acts as a short circuit when in reality it is not.

Nevertheless, the reason where the gain is increasing is approximately the same which is good.

The decrease at the end is not predicted is the theoretical model because it happens due to capacitors inside the transistors which are not being considered.



(a) Simulation Results (b) Theoretical Results

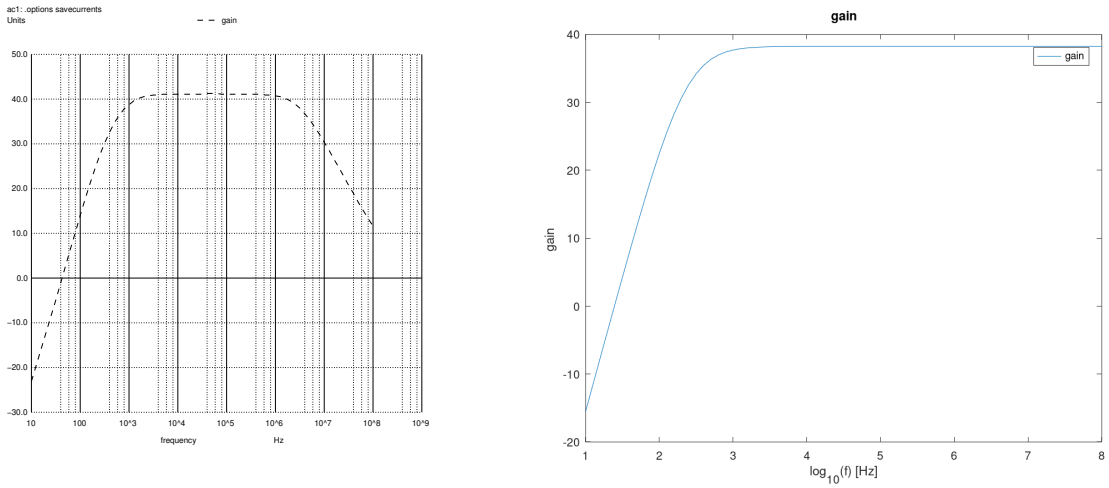
Figure 3: Gain stage's output voltage gain.

Entire Circuit

To analyse the gain of the entire circuit, we used the set of equations discussed in one of the posts in forum (https://groups.google.com/u/1/a/tecnico.ulisboa.pt/g/teoria-dos-circuitos-e-fundamentos-de-electrnica-tcfe/c/2oJaeUUFsTk), that can be obtained by using mesh analysis in the bellow circuit, in order to get a more accurate result

As it can be seen bellow, this was achieved and the theoretical model and the NGSpice one are really similar.

Once again, for higher frequencies the results differ because the capacitors inside the transistor are not being considered.



(a) Simulation Results

(b) Theoretical Results

Figure 4: Output stage's output voltage gain.

4 Conclusion

Similar to the previous laboratory, the results of the theoretical ant simulation analysis were not equal. However, we believe that the differences are not that significant and they can be explained by how NGSpice solves the circuit compared to how it was done in the theoretical analysis.

To solve the circuit, NGSpice used far more advanced simulation methods for the transistors, with many more parameters.

This way, the objective should have never been to have equal results, but rather, have results that are ”close enough”, which we believe it was achieved.

Furthermore, one detrimental goal was to analyse and choose values for the circuit's elements that assure it's best and most optimal performance, which by taking into consideration the obtained data, we believe it was achieved.