TÉCNICO LISBOA

Microelectronics

Lab 3

Current mirror design

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1 Introduction [1][2][3]

In this laboratory assignment, the main objective is to design and simulate a **current mirror** with two nMOS transistors, by using Virtuoso (version 6.1.7). For this purpose, the libraries `3rdlab` and `3rdlab_sim` were created. As shown in Table 1, the cell `currentmirror` in the first library contains the views `schematic` and `symbol`. The view `iout_vds` will be used to run DC sweep simulations of the drain voltage of one of the nMOS transistors (from 0 to $3.3V$), in order to obtain the variation of the output current (I_{out}) for different values of this voltage V_{DS}. This will allow conclusions to be made regarding, for instance, the variation of $V_{GS} = V_G$ (gate voltage, since $V_S = 0V$) and V_{TH} (threshold voltage) and the impact of the **channel length modulation**. Moreover, different values of the transistors' channel length (L) will be considered, while maintaining the W/L ratio. The designs developed in the views shown in Table 1 will be further discussed in section 2.

Library	Cell	View
3rdlab	currentmirror	schematic
		symbol
3rdlab_sim	currentmirror	iout_vds

Table 1: Libraries, cells and views created in Virtuoso

Current mirrors

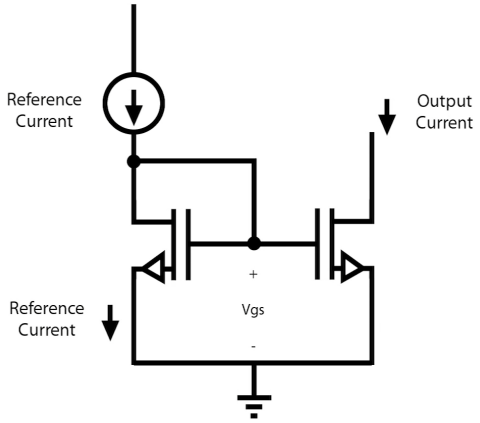


Figure 1: Simplified design of a current mirror [1]. In Virtuoso, the drain of the transistor on the right will be connected to a voltage source and the current source will also be connected to ground. The reference current is shown here to be the same as the source current of the transistor on the left, since $I_G \approx 0A$ (gate current).

MOS transistors have got various applications. The focus of this lab assignment is the use of nMOS transistors as **current sources**. The design of current sources in analog circuits is usually based on "copying" reference currents, with the assumption that one precisely-defined current source is already available. A circuit is used to generate a stable reference current, I_{REF}, which is then "cloned" to create many current sources in a system - on an IC chip with a number of amplifier stages, the reference current is then replicated at various other locations for biasing the various amplifier stages through a process known as "current steering".

To get MOS transistors to behave like current sources, a **current mirror** (shown in Figure 1) can be used. It consists of two nMOS transistors with their gates connected. One of the drains (D) is connected to the reference current and the gate (G). Since the gates are connected to each other and both sources (S) are connected to ground, the transistors have the same overdrive voltage, $V_{OD} = V_{GS} - V_{TH}$ (where V_{TH} is the threshold voltage), which is the value of V_{DS} (voltage between drain and source) which guarantees that the transistors operate in the saturation region.

As it was described in the first laboratory assignment [3], the nMOS transistors have three operating regions: the cut-off region, where $V_{GS} < V_{TH}$ and the drain current is given by $I_D = 0$; the triode (or ohmic) region, in which $V_{GS} \geq V_{TH}$ and $0 < V_{DS} < V_{GS} - V_{TH}$ - the drain current is given by equation 1; the saturation region, where $V_{GS} \geq V_{TH}$ and $V_{DS} \geq V_{GS} - V_{TH}$ - in this case, the current is given by equation 2. The parameters μ and C_{ox} are the mobility of carriers (in this case, electrons) and the oxide layer capacity, whereas W and L are the channel width and length of the transistor, respectively. In these two equations, the impact of the channel length modulation is not yet taken into account.

$$I_D = \mu C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \quad (1)$$

$$I_D = \frac{\mu C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH})^2 = \frac{\mu C_{ox}}{2} \cdot \frac{W}{L} \cdot V_{OD}^2 \quad (2)$$

The value of V_{TH} changes with temperature T according to equation $V_{TH} = V_{TH_0} - \alpha\,(T - T_0)$ (3),

where V_{TH_0} obtained for temperature T_0 should be the value of the threshold voltage indicated in the device's datasheet and $\alpha \approx 2.3mV/^oC$ [3].

In the transistor shown on the left in Figure 1, since its drain is shorted to its gate, it is forced to operate in the saturation mode. This happens because (supposing the system is being initially turned ON), V_{GS} starts at $0V$ and increases because I_{REF} charges the gate parasitic capacitance C_G; then, when $I_G \approx 0$, $I_D = I_{REF}$ and, since $V_{GS} = V_{DS}$ for this transistor, the condition $V_{DS} \geq V_{GS} - V_{TH}$ is verified. When V_{DS} for the other transistor reaches a certain value, it will also enter the saturation region. Thus, in these circumstances, both currents are given by equation 2. In a general case, the transistors don't need to have the same values of W and L, so the following relation is verified:

$$I_{out} = \frac{(W/L)_2}{(W/L)_1} \times I_{REF} \tag{4}$$

In which "1" and "2" are the transistors with drain currents I_{REF} and I_{out}, respectively. However, in this laboratory assignment, the ratios W/L are the same, thus $I_{out} = I_{REF}$ - the circuit simply replicates or **mirrors** the reference current in the output terminal. The key property of this topology is that it allows precise copying of the current with no dependence on process and temperature. The translation from I_{REF} to I_{out} merely involves the ratio of device dimensions, a quantity that can be controlled with reasonable accuracy.

Channel-length modulation

So far, the equations have neglected a crucial effect that occurs with transistors, which is specially relevant when the length is minimal - it is called **channel-length modulation**. Because of this, when the nMOS is operating in the saturation region, the drain current I_D does not remain constant as V_{DS} changes. As shown in Figure 2, there is a "pinch-off" of the channel at the drain end of the nMOS. The resistance of the channel is inversely proportional to its W/L ratio. Decreasing the length leads to a decrease in resistance and hence higher current from drain to source will flow. Thus, I_{DS} will increase (slightly) more as V_{DS} increases (to be noted that $I_{DS} \approx I_D$, since $I_G \approx 0$). This effect is more relevant for shorter channel lengths, since ΔL will make up for a larger portion of the channel.

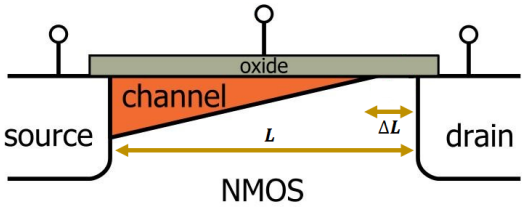


Figure 2: Representation of the **pinch-off** that occurs in nMOS transistors [4].

Because of this effect, the equations 1 and 2 are not verified. In these, L must be changed to $L - \Delta L$; by assuming that the incremental change is much less than the length of the physical channel (i.e., the distance between the source and drain regions), the equations that follow can be rearranged. Introducing $\lambda \approx \frac{\Delta L}{V_E L}$ (5) (where V_E is a fitting parameter), the equations 6 and 7 (respectively) are obtained. The parameter λ - which is called the **channel-length modulation parameter** - introduces a linear (nonzero) slope in the $I_D(V_{DS})$ curves (designated as g_{DS} in equation 7). It represents the relative variation in length for a given increment in V_{DS}. Therefore, for longer channels, λ is smaller.

$$I_D = \mu C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right] (1 + \lambda V_{DS}) \tag{6}$$

$$I_D = \frac{\mu C_{ox}}{2} \cdot \frac{W}{L} \cdot V_{OD}^2 \cdot (1 + \lambda V_{DS}) \tag{7}$$

2 Current mirror simulations

2.1 Theoretical preparation [2][5]

The first task to be developed in this laboratory assignment is to determine the value of W/L to use in the transistors. In order to do this, the input current is considered to be $I_{REF} = 10\mu A$ (the output current I_{out} will also have this value for some value of V_{DS}, since a current mirror is being studied) and the **overdrive voltage** is chosen to be $V_{OD} = V_{GS} - V_{TH} = 0.2V$. The value of the current in saturation increases with V_{GS}, but this higher voltage also means that the transistor works

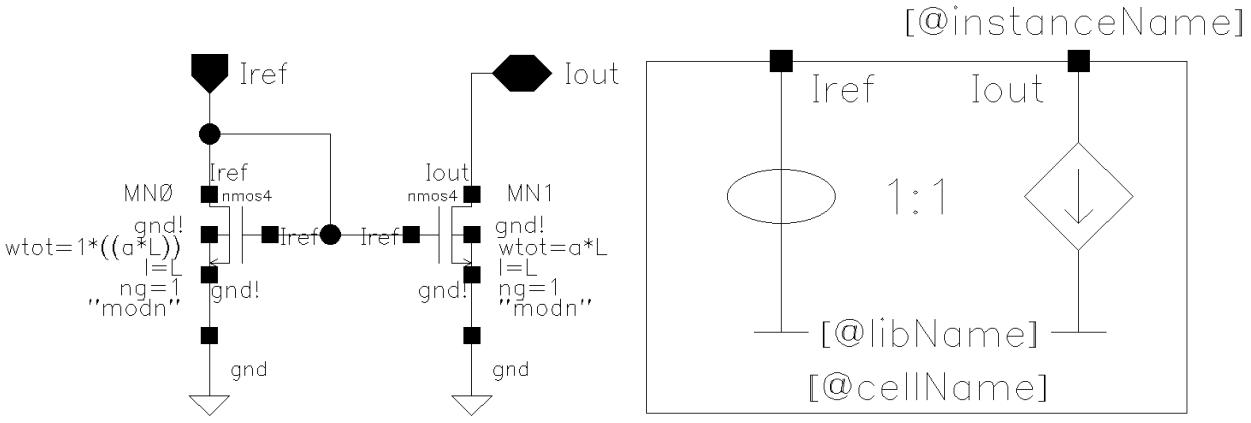
as a current source for a smaller range of V_{DS} (saturation range). On the other hand, a smaller value increases the sensitivity to V_{TH} - thus the usual design criteria of defining $V_{OD} = 200mV$ [3], used in this laboratory assignment.

In order to use equation 2, the product μC_{ox} is left to be obtained. The value of this parameter (**gain factor**), designated as KPN in the datasheet [6] of the technology used in Virtuoso , was thoroughly discussed in Lab 1 of this course. There, it was concluded that the value $KPN \equiv \mu_n C_{ox} = 170\mu A/V^2$ given in this datasheet was not appropriate for the nMOS transistors (used in that laboratory assignment). The value of KPN was determined for large transistors and, in particular, in the linear region. This value will have a much larger variability, depending on the length of the transistor and the values of V_{DS} being considered. Thus, the data collected in the first lab (in which a length of $L = 1\mu m$ was used for the nMOS transistors) led to the experimental value of $\mu C_{ox} \approx 73.990\mu A/V^2$, which will also be considered in this lab. Taking all this into account, by using equation 2, the following ratio (defined as a) is determined:

$$\frac{W}{L} = \frac{2 \cdot I_{ref}}{\mu C_{ox} \cdot V_{OD}^2} \equiv a \approx \textbf{6.758} \tag{8}$$

2.1.1 Current mirror design using Virtuoso

In order to design the current mirror, the library `3rdlab` was created. In the cell `currentmirror`, the views `schematic` and `symbol` were used in order to obtain the designs shown in **Figure** 3 (above). In `schematic`, two `nmos4` instances (from library PRIMLIB) were added, having the transistor on the left been rotated and flipped, so that the gates (G) of the transistors could be connected and its source (S) could be connected to an instance `gnd` in the bottom (as shown in Figure 3). Another `gnd` (from analogLib) was connected to the source of the other transistor. The bulk of each nMOS was connected to its respective source. Finally, the `input` and `inputOutput` pins designated as `Iref` and `Iout` were also included - these will be necessary in order to connect a constant current source or a voltage source (respectively); in the pin `Iout`, the current will also be measured. As the length L of the transistors will take different values throughout this laboratory assignment, it was defined as a variable, as well as the parameter a (defined in equation 8), from which the width (equal to the width stripe) was defined in Virtuoso (`wtot=a*L`). In the view `symbol`, the transistor whose drain current is I_{REF} is represented an ellipse, whereas the other nMOS as a controlled current source. In order to obtain the **value of the current** I_{out} **as a function of the voltage** V_{DS} of the same transistor, for different values of the length L, the circuit shown in Figure 3 (below) was designed in the view `iout_vds`. Here, the symbol from `3rdlab` was added. A constant current source (instance `idc` from library analogLib) of value $10\mu A$ was connected to the drain of the transistor on the left - this is the value of the reference current, I_{REF}. This current is necessary in order to generate the voltage $V_{GS} = V_G$ (same for both transistors), which will allow for current I_{out} to appear. Moreover, a DC voltage source (instance `vdc` from library analogLib) was connected to the drain of the other nMOS. Its value is set as $3.3V$, even though the simulations will be done by sweeping its value from 0 to $3.3V$ - this is the value of V_{DS} for this transistor and is also essential in order to obtain I_{out}.



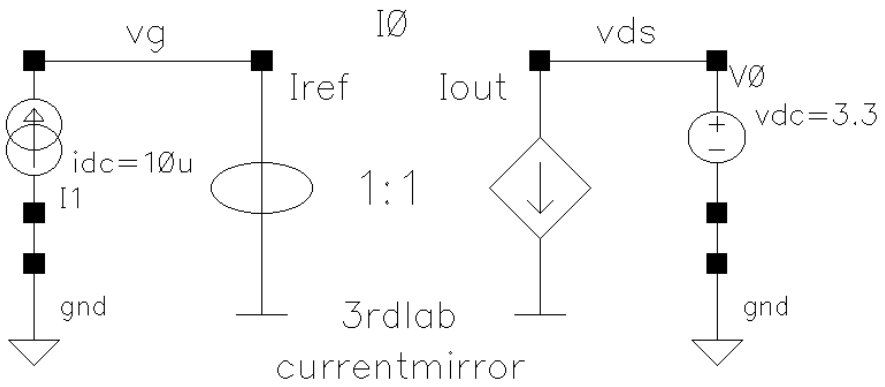


Figure 3: Views `schematic` [upper left] and `symbol` [upper right] (Cell `currentmirror`, Library `3rdlab`). Circuit for simulation in View `iout_vds` [below] (Cell `currentmirror`, Library `3rdlab_sim`) - in order to obtain the $I_{out}(V_{DS})$ curves (the voltage `vds` is swept from 0 to $3.3V$).

Throughout this report, unless one of the transistors is being specified, the voltage V_{DS} will refer to the voltage between drain and source of the nMOS transistor MN1 shown in Figure 3.

2.2 Simulation with fixed length L

Having designed the current mirror in Virtuoso, the circuit in cell `iout_vds` was simulated for a DC sweep of `vds` in the voltage range of 0 to $3.3V$ ($3.3V$ is the maximum voltage that the technology used in Virtuoso can support). In order to to this (and since a corner analysis will be made further ahead), the ADE GXL was launched. Here, a Test was created, in which the variables were defined as $L = 1\mu m$ and $a = W/L = 6.758$ (according to equation 8). Then, the DC analysis is selected; here, a linear sweep type is selected, in order to choose a step size of 0.025 - this was made because, in an Automatic sweep type, the step size was not small enough, since the curve $I_{out}(V_{DS})$ appeared with many "discontinuities" along its plot. By selecting `Iout` as the output, the plot shown in Figure 4 was obtained.

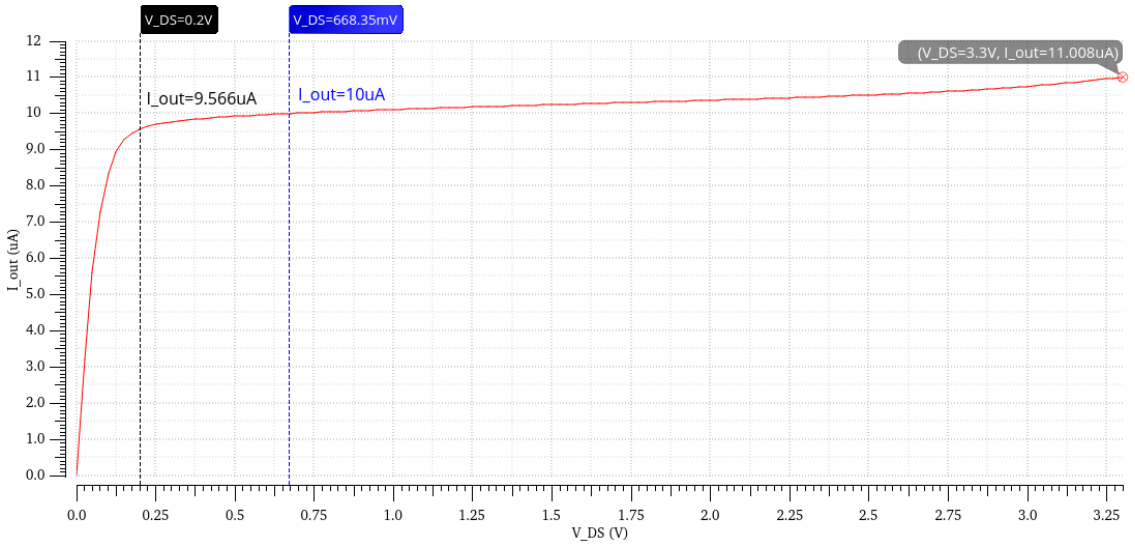


Figure 4: Simulation results of the curve $I_{out}(V_{DS})$ for $L = 1\mu m$, with V_{DS} being swept from 0 to $3.3V$. The vertical markers were drawn in order to determine the current at $V_{DS} = 0.2V$ and to indicate the voltage in which $I_{out} = 10\mu A$ (an horizontal marker was used to determine its value). A marker is also included at $V_{DS} = 3.3V$ in order to obtain the current value at this point.

In the curve shown in Figure 4, it is possible to identify the three operating regions of the transistor. The transistor is **OFF** only at $V_{DS} = 0V$, while the **saturation region** is reached at $V_{DS} = V_{GS} - V_{TH} = V_{OD}$, where I_{out} remains approximately constant, i.e, independent of V_{DS} - the nMOS works as a voltage controlled current source. As it was discussed in section 1, there is a

certain slope which is due to the channel-length modulation, thus the current varies with V_{DS}. In the **triode region** (which happens for $V_{DS} < V_{GS} - V_{TH}$), for lower values of V_{DS}, the curve showed a relatively linear behaviour - the transistor works as a voltage controlled resistor. For higher values of V_{DS} in this region, the term with V_{DS}^2 in equation 1 dominates and the curve becomes more parabolic. It is worth noting that, in this circuit, $V_{GS} > V_{TH}$, because the two transistors share the same gate (while both sources are connected to ground) and MN0 (in Figure 3) is always in the saturation region, as it was discussed in section 1.

By using a vertical marker in Virtuoso, the current value at $V_{DS} = 0.2V$ was determined; as it is shown in Table 2, $I_{out} < I_{REF} = 10\mu A$ - the relative difference between this current values, given by $(I_{out}(V_{DS} = 0.2V) - I_{REF})/I_{REF}$, is about -4.3%. This happens because of the channel-length modulation - as shown in equation 7, **the output current** (which is the drain current for transistor MN1 shown in the schematic of Figure 3) **will only be the same as the input current when** $V_{DS} = V_{GS}$. This is because, for the transistor MN0, $V_{DS_{MN0}} = V_G$, since its drain and gate are shorted to each other and $V_S = 0V$. Because I_D in equation 7 also depends on V_{DS}, this voltage needs to be the same for both transistors (assuming, of course, the same channel-length modulation parameter). By using an horizontal marker in Virtuoso, the voltage value for which $I_{out} = 10\mu A$ was determined (this is also shown in Table 2) - that is also the value of the gate voltage, V_G. Since $V_{OD} = V_{GS} - V_{TH} = V_G - V_{TH}$, it is obtained that $V_{TH} = 668.35 - 200 = 469.35mV$, whose relative difference to $0.46V$ (the threshold voltage given in the datasheet [6], also used in the first laboratory assignment) is of 2.0%, which indicates a considerable similarity.

V_{DS} (V)	I_{out} (μA)	I_{out} difference (%)
0.2	9.566	-4.3
668.35×10^{-3}	10	-
3.3	11.008	10.1

Table 2: V_{DS} and I_{out} values obtained from the curve in Figure 4 (for $L = 1\mu m$) - at voltage value $V_{DS} = V_{GS} - V_{TH} = 0.2V$, at current value $I_{out} = 10\mu A$ and at voltage value $V_{DS} = 3.3V$. Here, the third column represents the relative difference in the respective current values in relation to $I_{REF} = 10\mu A$.

Also in Table 2, the relative difference between I_{REF} and the output current at $3.3V$ (given by $(I_{out}(V_{DS} = 3.3V) - I_{REF})/I_{REF}$) is shown. This high value indicates that the channel width modulation has a great impact on the variation of the drain current in the saturation region - however, a length $L = 1\mu m$ was chosen in order to limit this effect at a certain level (for even lower values of L, the impact would be more significant, as it will be seen in subsection 2.4). In order to calculate the **channel-length modulation parameter**, a set of ten V_{DS} values in the saturation region ($V_{DS} > 0.2V$) and their respective output currents were fit to equation 7, using Fitteia - a web-based fitting platform and trademark of Instituto Superior Técnico. The values of V_{DS} were considered until $2.6V$ since, for larger values of this voltage, the linear equation did not fit the points as well - this is due to the closer proximity to the maximum voltage value of $3.3V$, in which the bigger than expected current variation is not predicted by the analytical model presented in section 1. The results are shown in Table 3, in which a slope with the same order of magnitude of $10^{-1}\mu A/V$ is shown. This will be particularly important for the comparisons done in subsections 2.3 and 2.4, in which the variation of the impact of the channel length modulation in different conditions can be analysed.

V_{DS} (V)	I_{out} (μA)	V_{DS} (V)	I_{out} (μA)
0.8	10.048	1.8	10.322
1.0	10.111	2.0	10.371
1.2	10.168	2.2	10.423
1.4	10.221	2.4	10.481
1.6	10.272	2.6	10.550

$g_{DS} = (\mu C_{ox}/2) \cdot (W/L) \cdot V_{OD}^2 \cdot \lambda$ $(\times 10^{-1} \mu A/V)$	λ (mV^{-1})
2.692	26.917

Table 3: Values obtained from the curve shown in Figure 4, for the saturation region and in order to determine the channel-length modulation parameter (λ), from the slope shown in the fifth column of this table and using equation 7 (with $\mu C_{ox} = 73.990 \mu A/V^2$).

2.3 Corner analysis

A similar DC sweep was made in order to perform corner analysis. For this purpose, the file `ams_corners.sdb` was created: in the Virtuoso terminal, the options `hitkit`→ `Simulation Utilities` → `Corner Analysis` were selected; then, the Model Group `cmos` was selected, as well as the variable `temperature`, in which the limits -40^oC and 125^oC were chosen. However, only `cmoswp` and `cmosws` were used in the CMOS corners, since no pMOS transistors are used in this laboratory assignment - the pairs WO/WP and WZ/WS have the same nMOS specifications. By importing this file into a new corner in the ADE and running the simulation with the option "Single Run, Sweeps and Corners", the plots shown in Figure 5 can be obtained.

Corner conditions	nMOS changes
WP (worst power)	$\mu \nearrow$ $V_{TH} \searrow$
WS (worst speed)	$\mu \searrow$ $V_{TH} \nearrow$
$T \nearrow$	$\mu \searrow$ $V_{TH} \searrow$
$T \searrow$	$\mu \nearrow$ $V_{TH} \nearrow$

Table 4: Characteristics used in corner analysis in subsection 2.3 - WP and WS (CMOS technology), increase and decrease in temperature T -, where μ is the carrier mobility and V_{TH} is the threshold voltage.

Parameter	corner_0	corner_1	corner_2	corner_3
cmos53.scs	cmoswp	cmoswp	cmosws	cmosws
temperature	-40	125	-40	125

Table 5: Characteristics of each corner simulated in Virtuoso. Here, the temperatures are in ^oC.

In Table 4, the two CMOS worst case parameter sets to be considered here are summarized, as well as the effects of changing the temperature in the mobility and threshold voltage. The **mobility of charge carriers in MOS devices increases at low temperatures**. At lower temperatures, carriers move more slowly, so there is more time for them to interact with charged impurities. The changes in V_{TH} can easily inferred from equation 3. Regarding the CMOS corners, for WO (worst case one) the mobility μ increases for the nMOS and decreases for the pMOS, while the opposite happens to the threshold voltage, V_{TH}, thus implying a faster nMOS and slower pMOS; in WZ (worst case zero), μ decreases for the nMOS and increases for the pMOS, while the opposite happens to V_{TH}, implying slower nMOS and faster pMOS. These two sets are not considered in the simulation done for this report. For **WP** (worst case power), μ increases for the nMOS and the pMOS, while the opposite happens to V_{TH}, implying faster nMOS and faster pMOS. For **WS** (worst case speed), μ decreases for both the nMOS and the pMOS, while the opposite happens to V_{TH}, implying slower nMOS and slower pMOS transistors. In Table 5, the characteristics of each corner used to obtain the plots in Figure 5 are indicated.

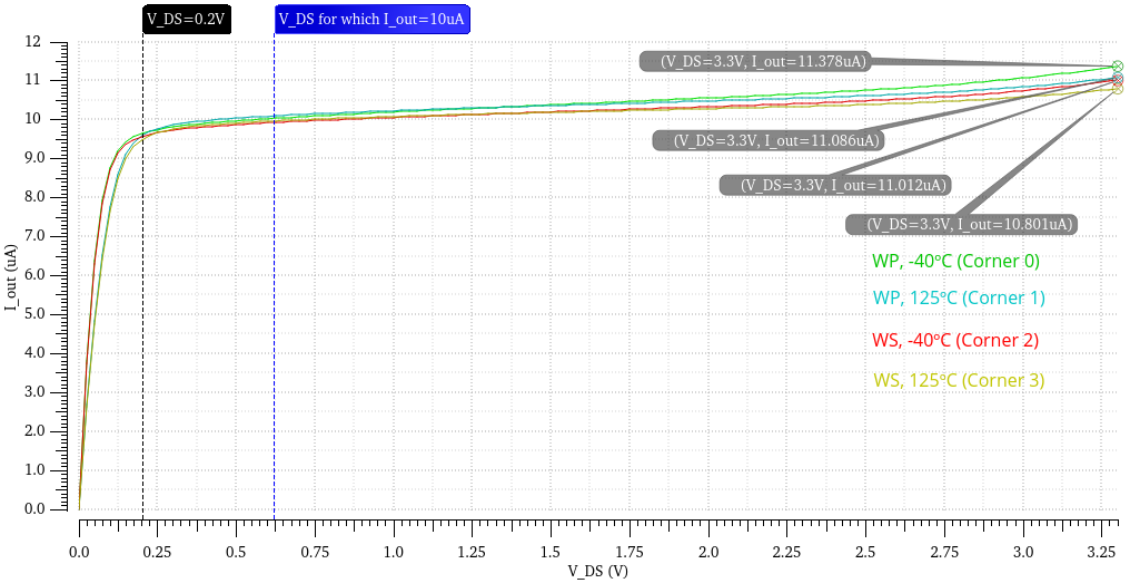


Figure 5: Simulation results of the curve $I_{out}(V_{DS})$ for $L = 1\mu m$, with V_{DS} being swept from 0 to $3.3V$ and for different CMOS parameters and temperatures (corners 0 to 3), as described in Table 5. The vertical markers were drawn in order to determine the current at $V_{DS} = 0.2V$ and to indicate the voltage in which $I_{out} = 10\mu A$ (an horizontal marker was used to determine its value). A marker is also included at $V_{DS} = 3.3V$ in order to obtain the current value at this point.

By looking at the curves shown in Figure 5, the **three operating regions** of the transistor (as described in subsection 2.2) are, once again, visible. However, the curves corresponding to corners 0 and 2 are above the curves for corners 1 and 3 in the triode region. In order to analyse this difference better, a more detailed behaviour in this region is shown in Figure 6 and will be discussed further ahead. However, in Figure 5, it is clear that the effect of the channel-length modulation is once again significant. Not only do the curves reach $I_{out} = 10\mu A$ at a voltage $V_{DS} \neq 0.2V$, but also a current increase can be seen in the saturation region. Once again, the current values at $V_{DS} = 0.2V$ and $V_{DS} = 3.3V$ were obtained, as well as the voltage value in which $I_{out} = I_{REF}$. These values are shown in Table 6, as well as the relative I_{out} differences from $10\mu A$, as done in subsection 2.2. It is worth noting that, in this case, since $V_{DS}(I_{out} = 10\mu A)$ is different for all corners, the average of these values was used in order to represent the blue vertical marker in Figure 5.

Many important conclusions can be drawn by analysing these results. Firstly, the relative difference in the output current for $3.3V$ is significantly larger for corner 0, which indicates a **higher impact of the channel-length modulation**, whereas the opposite happens for corner 3. The slope's value for the other corners should be in between the previous ones - this numerical analysis will be made alongside Table 7. The impact of λ is **more significant for WP**, since the I_{out} relative difference is bigger for corner 0, comparing with corner 2, and for corner 1 when compared with corner 3. This must happen because of the increase in μ and decrease in V_{TH}, which leads to higher currents, due to equation 7 - the opposite happens in WS (see Table 4). Even though the value of V_{GS} tends to change in order to stabilize the current in saturation at $10\mu A$, the change in these parameters is significant because the current continues to increase due to the channel-length modulation. Additionally, the **impact of this phenomenon is more significant for lower temperatures** (comparing corners 0 and 2 to 1 and 3, respectively) - this means that the change in mobility is predominant over the change in V_{TH} in increasing I_{out} (it is when T decreases that μ rises, even though V_{TH} also rises). This can be concluded because the I_{out} difference when $V_{DS} = 3.3V$ (shown in Table 6) is larger when $T = -40^oC$.

From Table 6, it is also noticeable that, for WP, the V_{DS} in which $I_{out} = I_{REF}$ (that is, when $V_{DS} = V_{GS}$) is smaller. These observations are all due to the **mobility** μ **increase and the threshold voltage** V_{TH} **decrease in WP** - the opposite happens in WS. Because of the circuit's design in a current mirror, the value of V_{GS} will vary and stabilize in order for the output current to have the value $I_{REF} = 10\mu A$ (not taking into account the channel-length modulation that will always occur). When the mobility μ rises and V_{TH} decreases, V_{GS} **must**, therefore, **decrease** (due to equation 2), thus the values seen in Table 6. When μ rises, V_{OD} decreases, due to equation 8. The current at $V_{DS} = 0.2V$ is higher for WP (rather and WS) and when T decreases; in both cases, μ increases, even though the change in V_{TH} is not the same, which indicates that the effect of the mobility is more impactful in this case - for the same $V_{DS} = 0.2V$, I_{out}'s value is larger. However, it is worth noting that $V_{GS} = V_{DS}(I_{out} = 10\mu A)$ **decreases** with higher temperatures - a lower V_{TH} is more important in decreasing V_{GS} than a higher μ (since μ is lower when T rises). Although this happens, the decrease in V_{GS} due to higher temperature is of -20.9% (corners 0→1) and -12.3% (corners 2→3), less significant than the decrease in V_{GS} due to WP (-32.0% and -38.7% in 2→0 and 3→1, respectively). This is because the variations in μ and V_{TH} in WP both produce the same effect in V_{GS} (reducing it).

Corner	V_{DS} (V)	I_{out} (mA)	I_{out} difference (%)
0 (WP, -40^oC)	0.2	9.642	-3.6
	544.379	10	-
	3.3	11.378	13.8
1 (WP, 125^oC)	0.2	9.589	-4.1
	430.581	10	-
	3.3	11.086	10.9
2 (WS, -40^oC)	0.2	9.569	-4.3
	800.650	10	-
	3.3	11.012	10.1
3 (WS, 125^oC)	0.2	9.481	-5.2
	702.045	10	-
	3.3	10.801	8.0

Table 6: V_{DS} and I_{out} values obtained from the curves in Figure 5 (for $L = 1\mu m$ and all four corners) - at voltage value $V_{DS} = 0.2V$, at current value $I_{out} = 10\mu A$ and at voltage value $V_{DS} = 3.3V$. The third column contains the relative difference in the respective current values in relation to $I_{REF} = 10\mu A$.

The different impacts of μ and V_{TH} variations will be further discussed with Figure 6. In order to further quantify the impact of the channel-length modulation, ten different points in each curve (in Figure 5) where again selected. **However**, as discussed before, the values of μC_{ox}, V_{GS} and V_{TH} can change significantly in corner analysis. Even though V_{GS} will change its value in order for the output current to be $I_{out} = 10\mu A$, this only happens at one point in the curves, because of the slope due to the channel-length modulation. Thus, the parameters shown in the last column of Table 7 cannot be the values of λ (since the values of μC_{ox} and $(V_{GS} - V_{TH})$ are now unknown) - λ could only be obtained for Table 3 of subsection 2.2. The values of the slopes allow us, however, to compare the impact of the channel-length modulation in the different corners.

As discussed above, alongside Table 6, the impact of the channel-length modulation is higher in corner 0, where the mobility μ rises due to WP and low temperature; the threshold voltage - less relevant when analysing the slope in the saturation region - decreases due to WP, but increases due to low temperature. The next highest slope is for corner 2, in which the mobility increases only because of $T = -40^oC$, but V_{TH} also increases - this means that the increase in μ due to temperature (rather than the CMOS parameters) is more impactful, since in corner 1, where μ only increases due to WP, the slope is lower (however, the difference here is not as significant as others). The lowest slope, however, happens for corner 3, in which the mobility decreases the most. In terms of percentages, there is a 44.8% increase in the slope from corner 1 to corner 0 and a 37.3% increase from corner 3 to corner 2 - T is what varies in these cases. Regarding WP/WS, the increases are of about 31.5% and 24.7% (regarding corners 2 $\rightarrow$ 0 and 3 $\rightarrow$ 1, respectively). The variations in temperature are, indeed, more significant than the variations in the CMOS specifications. In fact, the value of the slope shown in Table 3 (obtained in subsection 2.2) is smaller than the ones obtained for $T = -40^oC$, but higher than the values for $T = 125^oC$.

Corner	V_{DS} (V)	I_{out} (μA)	V_{DS} (V)	I_{out} (μA)	$g_{DS} = (\mu C_{ox}/2) \cdot (W/L) \cdot V_{OD}^2 \cdot \lambda$ $(\times 10^{-1} \mu A/V)$
0 (WP, -40^oC)	0.8	10.120	1.8	10.492	3.740
	1.0	10.201	2.0	10.563	
	1.2	10.277	2.2	10.637	
	1.4	10.350	2.4	10.588	
	1.6	10.421	2.6	10.811	
1 (WP, 125^oC)	0.8	10.171	1.8	10.439	2.582
	1.0	10.234	2.0	10.486	
	1.2	10.290	2.2	10.535	
	1.4	10.342	2.4	10.588	
	1.6	10.391	2.6	10.653	
2 (WS, -40^oC)	0.8	10.000	1.8	10.284	2.843
	1.0	10.064	2.0	10.337	
	1.2	10.122	2.2	10.393	
	1.4	10.178	2.4	10.455	
	1.6	10.231	2.6	10.529	
3 (WS, 125^oC)	0.8	10.031	1.8	10.250	2.070
	1.0	10.085	2.0	10.287	
	1.2	10.132	2.2	10.325	
	1.4	10.174	2.4	10.368	
	1.6	10.213	2.6	10.421	

Table 7: Values obtained from the curves in Figure 5 (with $L = 1\mu m$), for the saturation region and in order to determine the slopes (shown in the last column), given by equation 7.

At last, certain portions of the curves shown in Figure 5 have been highlighted in Figure 6. In the top, the curves are shown for the lower values of V_{DS} (up until $200mV$). Here, it is not only clear that the curves for $T = -40^oC$ sit above the other two, but also that the curves for WP are slightly above the respective (i.e., with the same temperature) WS curves - this was not clear in Figure 5. This also indicates that the **variation in mobility** must be more significant when T varies; the increase in μ leads to higher slopes (as inferred from equation 1), thus higher current values. Moreover, in the bottom of Figure 6, the areas in which the different curves cross each other are shown, between voltages $V_{DS} = 0.1V$ and $V_{DS} = 1.7V$. In the initial and final portions, the green curve (for corner 0)

stands above all others - this is because the mobility increases due to lower temperature and WP, thus its **slopes are the highest**. In the same portions, the yellow curve (corner 3) stands below all others, since μ is lower, due to higher temperature and WS.

However, the red curve (corner 2) stands above the blue curve (corner 1) in the initial portion, while their relative positions flip in the end. This must be because V_{TH} increases in corner 2 (due to both WS and $T = -40^oC$), while it decreases in corner 1 (WP and $T = 125^oC$); as mentioned previously, alongside Table 6, V_{TH} is quite relevant around the transition between triode and saturation regions. Because V_{TH} for corner 2 is higher, it reaches saturation first (lower V_{OD}), whereas the current in corner 1 continues to increase more significantly (triode region) - even though V_{GS} changes in order to have $I_{out} = 10\mu A$ at a certain point, the change in V_{TH} should dominate in these two cases; in corners 0 and 3 (in which V_{OD} respectively decreases and increases, due to the opposite change in μ and equation 8), the variation in V_{TH} is not clear (see Table 4). In $V_{DS} = 3.3V$, the difference between corners 1 and 2 is not very significant, because the slope in saturation is bigger for corner 2 (as shown in Table 7) - thus, the difference in I_{out} decreases with V_{DS}. The positions between the curves in the **intermediate** portion of Figure 6 (below) should also be due to V_{TH}. For corners 0 and 3, V_{TH} increases in the latter **only because** of WS, and only because of T in the former - thus, the influence of V_{TH} is not as significant as in the other two corners; because of this, corners 0 and 3' curves sit in-between the others in the intermediate region. For lower and higher V_{DS}, the impact of μ is the most important - thus the highest-mobility curve (corner 0) sits above all others, while the lowest-mobility curve (corner 3) below them.

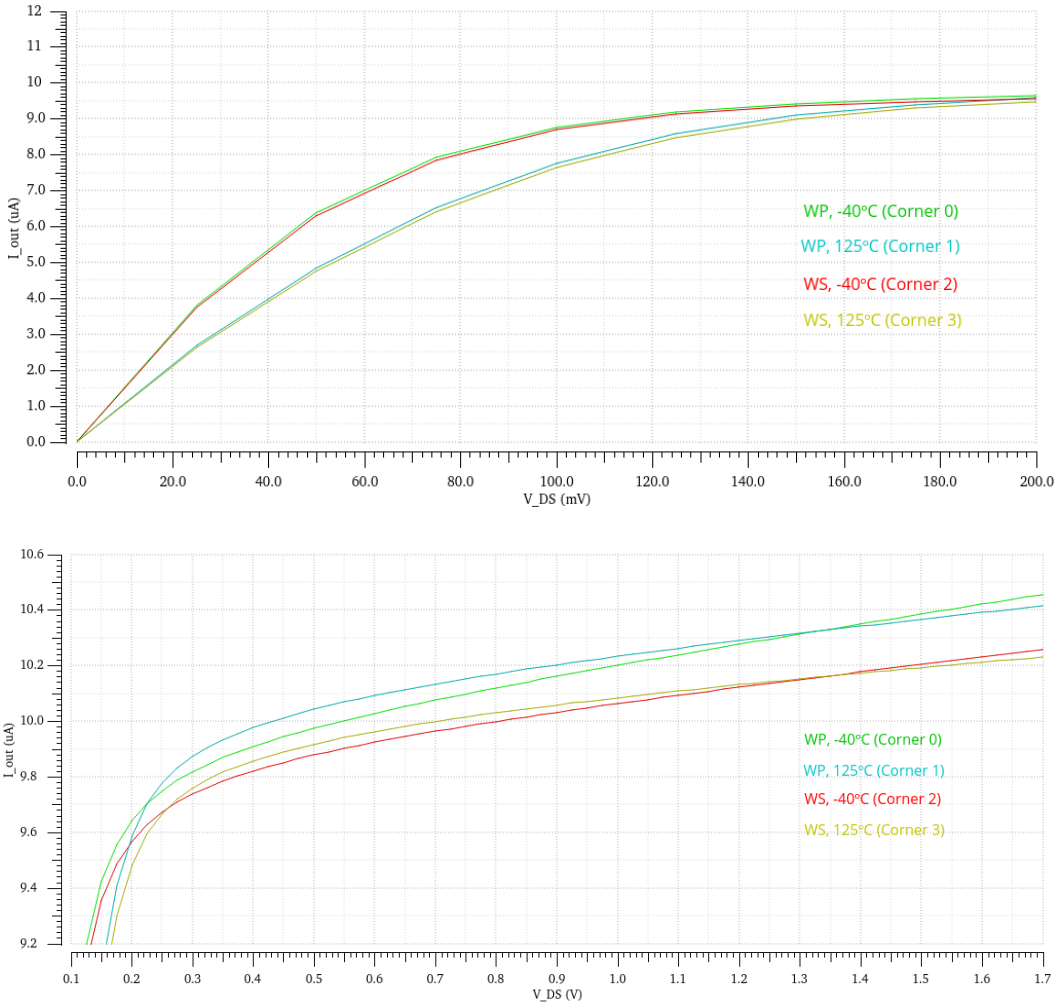


Figure 6: Simulation results for $I_{out}(V_{DS})$, with $L = 1\mu m$ and V_{DS} being swept from 0 to $3.3V$ and for different CMOS parameters and temperatures (Table 5); the results are shown for V_{DS} between $0V$ and $200mV$ [above] or $0.1V$ and $1.7V$ (for values of I_{out} between $9.2\mu A$ and $10.6\mu A$) [below]. These were made in order to observe particular details in the curves shown in Figure 5.

2.4 Simulation for various lengths L

Finally, keeping the same W/L, the circuit designed in Figure 3 was simulated for lengths $L = \{0.35\mu m,\ 1\mu m,\ 4\mu m\}$, by running the Test created in subsection 2.2 with a Parametric Analysis - in Run Mode "Parametric Set", the values of L were inserted and the graphs shown in Figure 7 were obtained. In this case, a corner analysis was not performed; instead, the simulations were made for typical conditions.

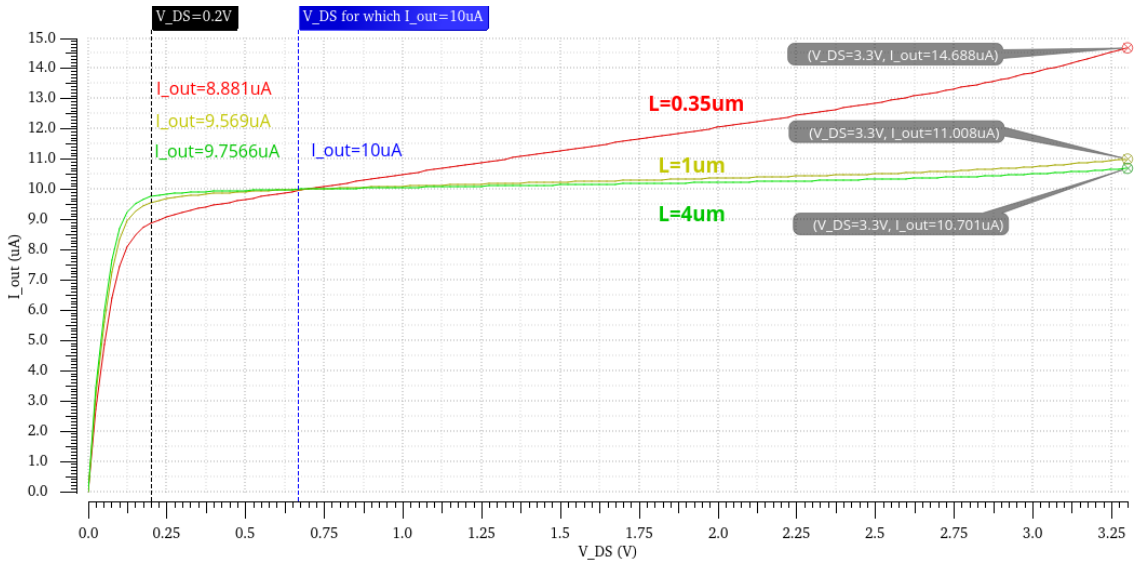


Figure 7: Simulation results of $I_{out}(V_{DS})$ for $L = \{0.35\mu m,\ 1\mu m,\ 4\mu m\}$, with V_{DS} swept from 0 to $3.3V$. The vertical markers were drawn in order to determine the current at $V_{DS} = 0.2V$ and to indicate the (average) voltage in which $I_{out} = 10\mu A$ (horizontal markers were used to determine these values). Markers were used at $V_{DS} = 3.3V$ in order to obtain the current values.

In Figure 7, it is perceptible that the **slope in saturation decreases as L increases**, thus the curves are closer to the ideal behaviour of a constant current source. This was to be expected, taking into account equation 5 - **as L increases, λ decreases**, because the variations ΔL due to pinch-off are less significant. Even though, as seen in Lab 1, μC_{ox} can increase (considerably) due to the increase in L (for that reason, KPN in the datasheet - obtained for large transistors - was not used), the results shown in Figure 7 mean that the variation in λ is quite impactful (there is also the W/L factor in equation 7, which will contradict the increase in μ...). Even if the high μC_{ox} could lead to larger currents, the considerable decrease in λ means that the I_{out} dependence on V_{DS} dies out partially. This relation is also notorious in Tables 2 (obtained in subsection 2.2) and 8, since the I_{out} relative difference in $V_{DS} = 3.3V$ is much more significant for $L = 0.35\mu m$. However, it is also worth noting that, even though there is a big jump from $L = 0.35\mu m$ to $L = 1\mu m$ (of about -36.8 percentage points), the difference is not as significant from the latter to $L = 4\mu m$ - even though the length quadruples, the variation is of about -3.1 percentage points. The same effect can be seen in Table 9, in which the slopes were calculated using Fitteia. Here, a change from the order of magnitude of $10^0 \mu A/V$ to that of $10^{-1} \mu A/V$ is observed; the slope increases in about 51.7% from $L = 4\mu m$ to $L = 1\mu m$, but in about 484.8% from the latter to $L = 0.35\mu m$. This indicates that, when producing an nMOS transistor, there isn't as much to gain in this aspect when the length is increased over a certain value. It is worth noting, that, as in subsection 2.3, the values of λ cannot be obtained - only the slopes of the curves -, since the variation in L will change μC_{ox} (and also V_{TH}, since the threshold voltage depends on the mobility), thus the actual values of these parameters are unknown.

Another thing to notice is that the slopes of the curves in the triode region have an opposite relation - as seen in Figure 7, the curves for $L = 4\mu m$ and $L = 0.35\mu m$ sit (respectively) above and below the others in the triode region. This happens because the value of μC_{ox} increases with L - as

seen in Lab 1. Even though, as seen in equation 6, the term W/L is present, the increase in μC_{ox} due to the increase in L should be much more significant. Moreover, even though the channel-length modulation parameter is present in this equation, the values of V_{DS} are small, thus it does not have a big impact. Taking equation 8 into account, since μ rises with L, V_{OD} decreases, thus the curves reach saturation for lower V_{DS}. Because of this, the values $I_{out}(V_{DS} = 0.2V)$ increase with L, whereas the values $V_{DS}(I_{out} = 10\mu A)$ (where saturation has been reached) decrease (slightly), as shown in Tables 2 and 8.

$L\ (\mu m)$	$V_{DS}\ (V)$	$I_{out}\ (\mu A)$	I_{out} difference (%)
0.35	0.2	8.881	-11.19
	692.19×10^{-3}	10	-
	3.3	14.688	46.9
4	0.2	9.757	-2.4
	638.83×10^{-3}	10	-
	3.3	10.701	7.0

Table 8: Voltage and current values obtained from the curves shown in Figure 7 (for $L = 0.35\mu m$ and $L = 4\mu m$) - at voltage value $V_{DS} = 0.2V$, at current value $I_{out} = 10\mu A$ and at voltage value $V_{DS} = 3.3V$. Here, the third column represents the relative difference in the respective current values in relation to $I_{REF} = 10\mu A$.

$L\ (\mu m)$	$V_{DS}\ (V)$	$I_{out}\ (\mu A)$	$V_{DS}\ (V)$	$I_{out}\ (\mu A)$	$g_{DS} = (\mu C_{ox}/2) \cdot (W/L) \cdot V_{OD}^2 \cdot \lambda\ (\times 10^{-1} \mu A/V)$
0.35	0.8	10.178	1.8	11.739	15.742
	1.0	10.498	2.0	12.049	
	1.2	10.812	2.2	12.364	
	1.4	11.122	2.4	12.691	
	1.6	11.431	2.6	13.039	
4	0.8	10.032	1.8	10.202	1.775
	1.0	10.068	2.0	10.236	
	1.2	10.102	2.2	10.271	
	1.4	10.136	2.4	10.312	
	1.6	10.169	2.6	10.362	

Table 9: V_{DS} and I_{out} values obtained from the curve in Figure 7 obtained with lengths $L = 0.35\mu m$ and $L = 4\mu m$, for the saturation region and in order to determine the slopes of the curves (shown in the last column), using equation 7.

3 Conclusion

In this laboratory assignment, a current mirror was designed in Virtuoso using two nMOS transistors, in which the ratio W/L was the same for both and remained fixed throughout the different analyses. This value was initially determined in order to have an overdrive voltage of $V_{OD} = 0.2V$ and a drain current in saturation of $I_D = 10\mu A$ at the output, having the value of $\mu_n C_{ox}$ determined in the first report of this course been considered.

Firstly, the curve $I_{out}(V_{DS})$ was obtained for a fixed channel length ($L = 1\mu m$) and by sweeping V_{DS} - the drain voltage of the MN1 transistor, in whose drain the output current is measured - from 0 to $3.3V$. This output current's value was obtained in different points and compared to the reference current's value of $I_{REF} = 10\mu A$, whilst the mobility, the voltages V_{GS} and V_{TH} and the impact of the channel-length modulation were also analysed. A corner analysis was made with the same voltage sweep and length L, by using the extreme conditions of temperature (-40^oC and 125^oC) and CMOS technology parameters (worst power and worst speed). Once again, the output current and the channel width modulation, as well as the threshold voltage, were analysed in detail. Finally, the DC voltage sweep was made for different values of the length L and for typical conditions. In this case, the impact of L on the output current and the channel width modulation parameter were commented on.

Throughout this report, most of the parameters - mobility μ, voltage V_{GS}, threshold voltage V_{TH}, channel-length modulation parameter λ and channel length L - varied simultaneously, thus the

predominance of certain ones over others for different voltage and current values were analysed in detail.

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