TÉCNICO LISBOA

Microelectronics

Lab 5

Current reference design

Bologna Degree in Physics Engineering (LEFT)
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1 Introduction [1][2][3]

In this laboratory assignment, the main objective is to design a circuit that outputs **four current references** of $1\mu A$ each. The drain voltage applied in the respective pMOS transistors will be swept in order to obtain their drain current curves. Moreover, **corner analysis** will be performed by changing the CMOS parameters, temperature T and supply voltage V_{DD}. These DC analyses will be performed in the views `id_vd` shown in Table 1. Finally, using the views `psrr_freq`, an AC voltage signal of amplitude $1V$ will be connected to V_{DD} and the change in the **power supply rejection ratio (PSRR)** with frequency will be evaluated.

Library	Cell	View
5thlab	current_reference	schematic
		symbol
	current_reference_low_voltage_cascode	schematic
		symbol
5thlab_sim	current_reference	id_vd
		psrr_freq
	current_reference_low_voltage_cascode	id_vd
		psrr_freq

Table 1: Libraries, cells and views created in Virtuoso

For this purpose, two different designs were considered. In the **original current reference design** (in cells `current_reference`), eight pMOS transistors are used. On the other hand, a low voltage cascode current mirror implementation is used in the **new current reference design** (in cells `current_reference_low_voltage_cascode`).

Voltage and **current references** are extensively incorporated in analog circuits - for instance, in differential pairs, to define common-mode levels in OPAMPs or in A/D and D/A converters. In fact, reference currents were used in the previous laboratory assignments, in which different current mirror designs were implemented - in practical terms, these current references need to be generated. These DC quantities should generally have a small dependence on the supply voltage and process parameters, as well as a well-defined dependence on the temperature (temperature-independent designs can also be used). In this laboratory assignment, however, well-established *bandgap* techniques based on CMOS technology will be used to provide current references which are only (ideally) **independent of the supply voltage**. In addition to the supply voltage, process parameters and temperature variation, other aspects generally need to be taken into account when designing current references - these include output impedance, output noise and power dissipation.

A very simple current source can be made by applying a voltage across a resistor. However, in order to arrive at a solution which is as independent as possible of the supply voltage V_{DD}, there must be a way for the circuit to bias itself, that is, I_{REF} must be derived from I_{out}, in a sort of loop design, as shown in Figure 1. The effect of transistors M_3 and M_4 is analogous to what was presented in the previous laboratory assignments, in which cascode current mirrors were designed; because of them and due to the same $(W/L)_P$ ratio (as indicated in Figure 1), the current will be copied, thus both drain currents in M_3 and M_4 should have the same value.

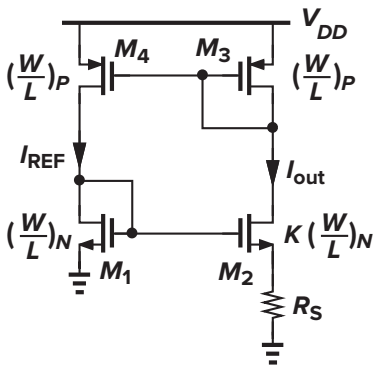

Figure 1: Current reference design considered in this laboratory assignment [1].

Since I_{out} and I_{REF} display little dependence on the supply voltage, their values are set by other parameters. The resistor R_S shown in Figure 1 is added between the source of M_2 and ground as another constraint, to uniquely define the currents. The current across M_2 decreases as a result of the voltage drop that arises from flowing the current through the resistor.

In order to obtain the equation for I_{out}, it must be firstly reminded that the drain current of a pMOS transistor in the saturation region is given by equations 1 and 2, in case the channel-length modulation is taken into account or not (respectively).

$$I_D = \frac{\mu_p C_{ox}}{2} \cdot \left(\frac{W}{L}\right)_p \cdot (V_{SG} - V_{TH})^2 \tag{1}$$

$$I_D = \frac{\mu_p C_{ox}}{2} \cdot \left(\frac{W}{L}\right)_p \cdot (V_{SG} - V_{TH})^2 \cdot (1 + \lambda V_{SD}) \tag{2}$$

In equations 1 and 2, μ_p is the mobility of the charge carriers (in this case, holes), V_{TH} the threshold voltage and $V_{OD} = V_{SG} - V_{TH}$ the overdrive voltage, whereas W and L are the channel width and length, respectively. Now, by writing the voltage equation for the mesh with R_S, M_1 and M_2 (shown in Figure 1), the relations shown below are obtained. In (a), body effect is neglected, thus V_{TH_1} and V_{TH_2} (for transistors M_1 and M_2, respectively) are considered to be the same in this simplification. Moreover, equation 1 is taken into account, thus channel-length modulation is also neglected here. The constant K is the ratio between the quotients W/L of transistors M_2 and M_1, as shown in Figure 1.

$$V_{GS_1} = V_{GS_2} + I_{D_2}R_S \Leftrightarrow \sqrt{\frac{2I_{out}}{\mu_n C_{ox}(W/L)_N}} + V_{TH_1} = \sqrt{\frac{2I_{out}}{\mu_n C_{ox}K(W/L)_N}} + V_{TH_2} + I_{out}R_S \overset{\text{(a)}}{\Longrightarrow}$$

$$\Rightarrow \sqrt{\frac{2I_{out}}{\mu_n C_{ox}(W/L)_N}}\left(1 - \frac{1}{\sqrt{K}}\right) = I_{out}R_S$$

Hence, equation 3 is obtained:

$$I_{out} = \frac{2}{\mu_n C_{ox}(W/L)_N} \cdot \frac{1}{R_S^2}\left(1 - \frac{1}{\sqrt{K}}\right) \tag{3}$$

As intended, the current is **independent of the supply voltage** V_{DD} (but **still a function of process parameters and temperature**, as will be analysed in section 3). The assumption $V_{TH_1} = V_{TH_2}$, however, introduces some error in the foregoing calculations, because the sources of M_1 and M_2 are at different voltages - only in the former the source is connected to its bulk.

In this context, it is worth indicating that, in nMOS and pMOS devices, the variation of the threshold voltage due to **body effect** is given by equation 4. For an nMOS, it increases when the source (S) is at a higher voltage than the body (B) ($V_{SB} > 0$), while in the pMOS it happens (in absolute value) when the source is at a lower voltage ($V_{BS} > 0$). The substrate is usually connected to the "most negative" power supply with an nMOS and the most positive with a pMOS, but the effect of $V_{SB} > 0$ on the channel of the nMOS device can be represented as a change in the threshold voltage V_{TH} (similarly for the pMOS). In equation 4, V_{TH_0} is the threshold voltage for $V_{SB/BS} = 0$, ϕ is the strong inversion surface potential and γ is the body-effect parameter.

$$V_{TH} = V_{TH_0} + \gamma\left[\sqrt{\phi + V_{SB/BS}} - \sqrt{\phi}\right] \tag{4}$$

2 Current reference designs and initial simulations in Virtuoso

The schematic designed in Virtuoso in cell `current_reference` (of library `5thlab`) is shown in Figure 2. Here, it can be seen that five different input pins were used - these were `vdd` (connected to the sources of all pMOS transistors) and the pins connected to the drains of transistors M_5 to M_8 (`vd_M5` to `vd_M8`, respectively). The first will be connected to a constant voltage source of $3.3V$ in section 2.1, whereas an AC voltage source will also be included in section 4.1. The other pins, on the other hand, will be connected to a voltage source which will be swept from 0 to $3.3V$ in DC analyses. The `pmos4` and `nmos4` instances shown in Figure 2 were input from library PRIMLIB, whereas the resistance `res` and the instances `gnd` from analogLib. The ratios $(W/L)_n$ and $(W/L)_p$ (for the nMOS and pMOS transistors, respectively) were defined as the variables `a_n` and `a_p`, respectively. Moreover, the channel length `L` and the `Rs` value of the resistance were also set as variables. These will be defined when the simulations are to be done. In Figure 2, the view `symbol` relative to the previously mentioned schematic is also shown. This will be inserted in the respective test benches created for the simulations.

A very important aspect to discuss in this schematic is the **number of gates** selected in each transistor. The number of gates was varied amongst pMOS and nMOS transistors in order to use the same (respective) ratios $(W/L)_p$ and $(W/L)_n$ (which will be determined in section 2.1), whilst obtaining the desired outputs from this design. For the pMOS transistors M_3 and M_4, 4 gates were

used, whereas only 2 gates were selected for the nMOS transistor M_1. This is due to the fact that the mobility of electrons is (normally, 2 to 4 times) higher than the mobility of holes ($\mu_n > \mu_p$), because electrons are less bounded in an atom than a hole - this relation was proved in the first laboratory assignment, in which the ratio $\mu_n/\mu_p \approx 3$ was obtained. Thus, the doubled number of gates in the pMOS compensates this in some way. The minimum number of gates used in the design is `ng=2` (in the nMOS transistor M_1); a single gate was not used in this case to allow for **matching** - for the same reason, an even number of gates was selected.

The main difference between the implementation shown in Figure 2 and the design introduced in section 1 (shown in Figure 1) is the inclusion of four other pMOS transistors on the right (M_5, M_6, M_7 and M_8). These will work similarly to M_3 and will have a specific drain current value (not considering the channel-length modulation). In this laboratory assignment, the objective is to **output four current references of $1\mu A$ each**, with a **maximum current for the current reference generation of $4\mu A$**. This last condition is verified in the way that each nMOS transistor (M_1 and M_2) will have a drain current of $2\mu A$ - for which the parameters in the circuit will be calculated in section 2.1. Considering these two currents, there is a total of $4\mu A$. On the other hand, since a drain current of $1\mu A$ is desired in each pMOS transistor on the right, M_5 and M_8 have only **2 gates** - half the gates of the other pMOS transistors. Finally, the **8 gates** selected for the nMOS transistor M_2 is also related to these current values - the current $4\mu A$ is given by $4 \times 1\mu A$, thus the number of gates in M_2 must be 4 times the number of gates in M_1. This means that the value of the constant shown in Figure 1 is $K = 4$.

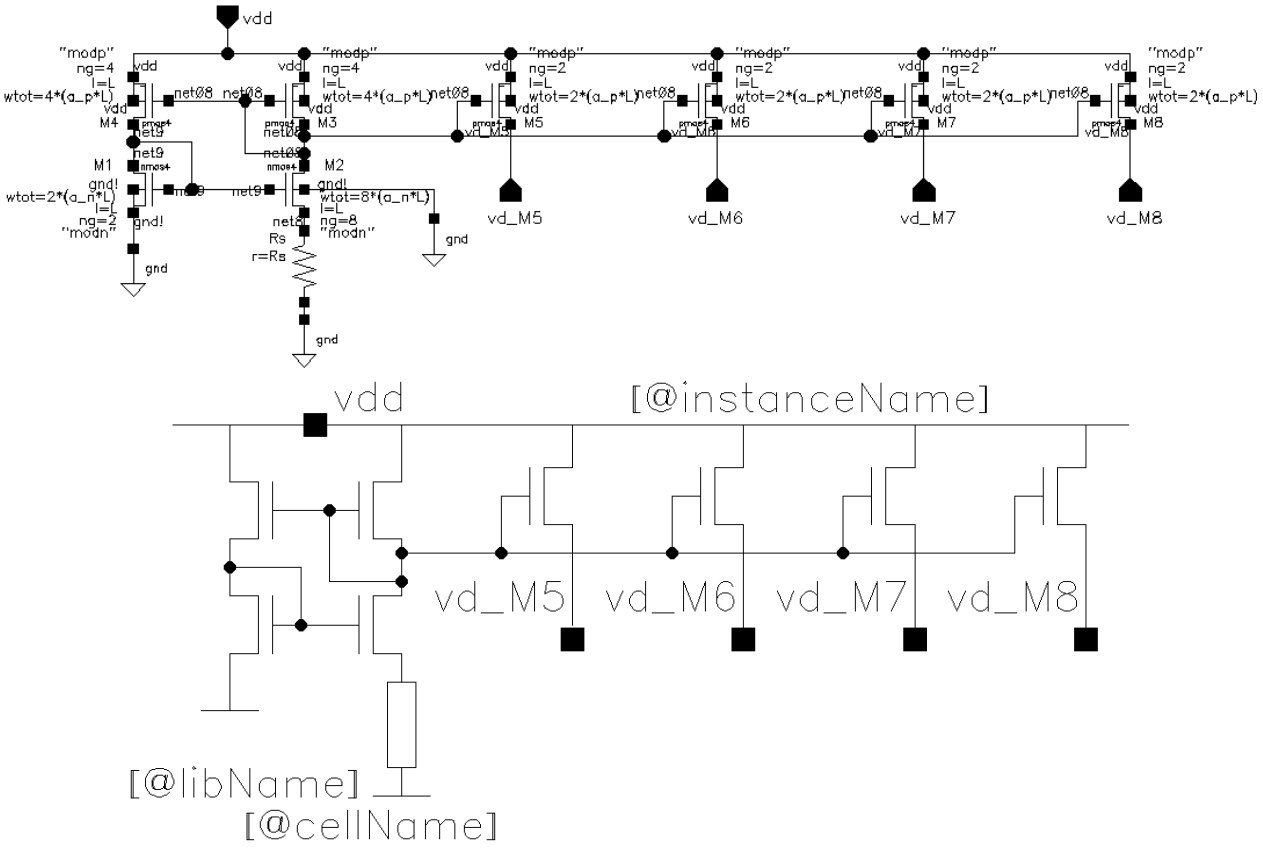

Figure 2: Views `schematic` [above] and `symbol` [below] (in cell `current_reference` and library `5thlab`), corresponding to the original current reference design.

It is expected that the effect of the channel-length modulation in the previous design will be significant, since only one pair of pMOS transistors is used to mirror the current. In the previous laboratory assignment, nMOS transistors were used to upgrade the current mirror design of Lab 3, thus obtaining a cascode current mirror and a low voltage cascode current mirror. In the latter two designs, the effect of the channel-length modulation was greatly reduced. However, the second

also had a higher saturation range, which was beneficial (even though the slope in saturation was slightly higher than in the cascode current mirror, the difference was not very significant).

In this laboratory assignment, a similar implementation to the low voltage cascode current mirror was applied in the current reference design. Thus, the views shown in Figure 3 were designed in Virtuoso and simulations will also be run with this new design, in order to discuss its improved results. As seen below, another pair of pMOS transistors with 4 gates was added on the left (M_9 and M_{10}), whereas four others with 2 gates were added on the right (M_{11}, M_{12}, M_{13} and M_{14}). It is important to beware that, since pMOS transistors are used (instead of nMOS), the configuration of the low voltage cascode current mirror here is "inverted", when compared with the one in Lab 4. For instance, the input pin `vcasp` is now connected to the gates of the lower pMOS transistors and the gate of $\mathrm{M}_{9/10}$ is connected to the drain of M_3.

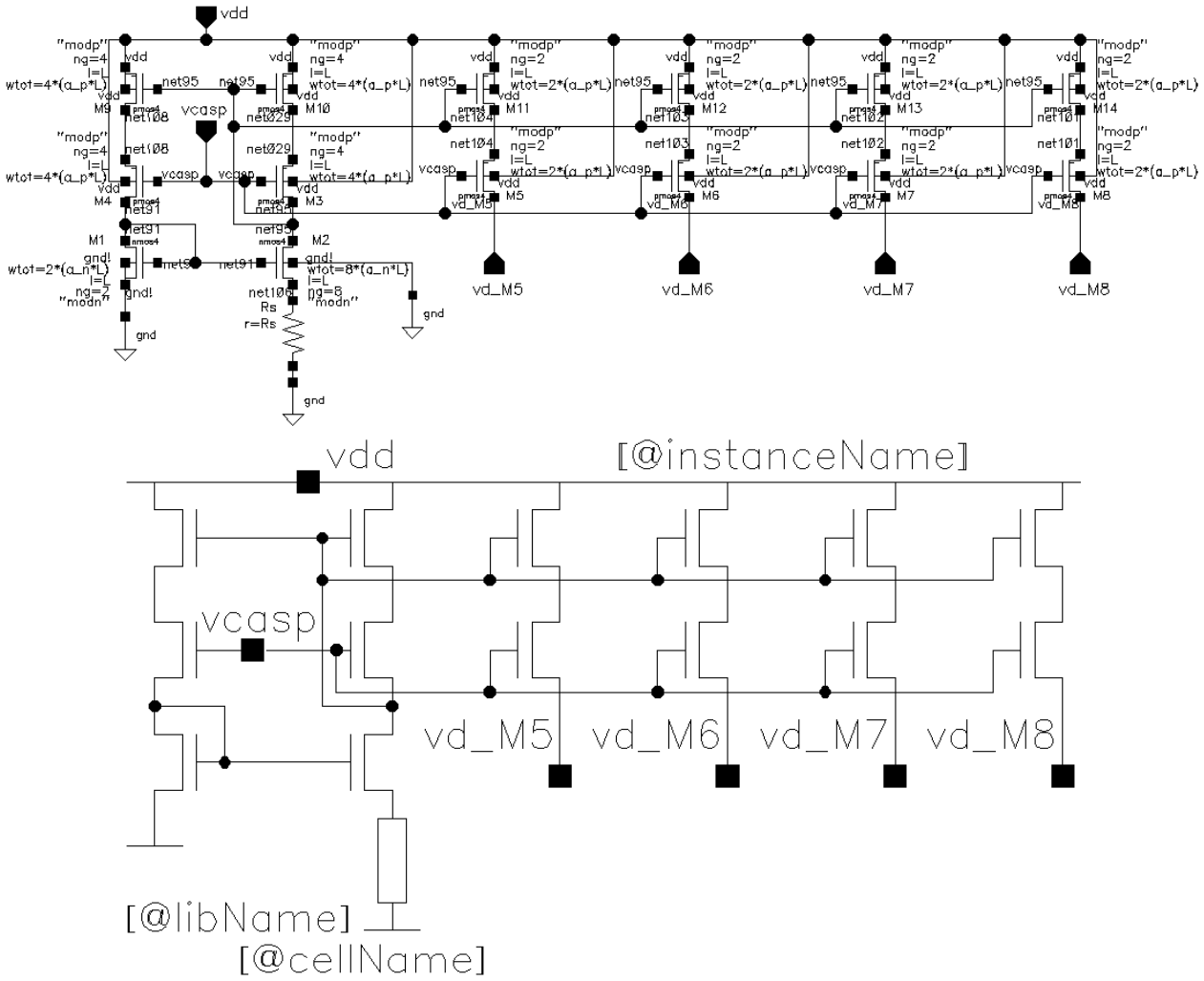

Figure 3: Views `schematic` [above] and `symbol` [below] (in cell `current_reference_low_-voltage_cascode` and library `5thlab`), corresponding to the new current reference design.

2.1 Initial simulations with the original design

In order to obtain the desired drain current curves for transistors M_5 to M_8, the proper ratios W/L for the nMOS and pMOS transistors need to be defined. For this purpose, equation 1 must be considered. The drain currents' values in transistors M_1 to M_4 should be $I_D = 2\mu A$ (as mentioned before) and the **overdrive voltage** $V_{OD} = 0.2V$ - the current in saturation increases with V_{GS} (for the nMOS), but this also means a smaller saturation range; a smaller value, however, increases the sensitivity to V_{TH}, thus the usual design criteria of defining this V_{OD}. As for $\mu_{n/p}C_{ox}$, these parameters were obtained in the first laboratory assignment, for transistors with lengths $\boldsymbol{L = 1\mu m}$

(thus, the same length will be considered in this report), since the respective parameters given in the datasheet were not valid for the conditions being used in the laboratory assignments - in Lab 1, the values $\boldsymbol{\mu_n C_{ox} = 73.9903 \mu A/V^2}$ and $\boldsymbol{\mu_p C_{ox} = 24.4777 \mu A/V^2}$ were obtained. The value of $L = 1\mu m$ for the length also limits the effect of the channel-length modulation to a certain extent, as seen in Lab 3.

Taking all this into account and considering the number of gates in the transistors, as described previously, the following ratios are obtained:

$$2\left(\frac{W}{L}\right)_n = \frac{I_D}{\frac{1}{2}\cdot\mu_n C_{ox}\cdot 0.2^2} \Leftrightarrow \boldsymbol{\left(\frac{W}{L}\right)_n \equiv a_n \approx 0.6758} \tag{5}$$

$$4\left(\frac{W}{L}\right)_p = \frac{I_D}{\frac{1}{2}\cdot\mu_p C_{ox}\cdot 0.2^2} \Leftrightarrow \boldsymbol{\left(\frac{W}{L}\right)_p \equiv a_p \approx 1.021} \tag{6}$$

Finally, using equation 3 with $K = 4$, the value of the resistance R_S is obtained in (7). However, it is worth noting that, due to the number of gates considered in transistor M_2, $(W/L)_N$ shown in equation 3 must be replaced by $8(W/L)_n = 8a_n$, where a_n is shown in (5). Moreover, $I_{out} = 1\mu A$, since this is the desired drain current values in transistors M_5 to M_8.

$$\boldsymbol{R_S = \sqrt{\frac{2}{\mu_n C_{ox}\cdot 8\left(\frac{W}{L}\right)_n \cdot I_{out}}\cdot\left(1-\frac{1}{\sqrt{K}}\right)} \approx 50\ k\Omega} \tag{7}$$

Having obtained these parameters, the schematic used for the initial simulations with the original current reference design was designed and is shown in Figure 4. Having inserted the symbol shown in Figure 2, the voltage sources `vdc` (from analogLib) were connected to the sources of the pMOS transistors or to the drains of the pMOS transistors on the right, having the values of $3.3V$ and $1.0V$ been selected, respectively; however, the value of the latter will actually be swept from 0 to $3.3V$, as mentioned before.

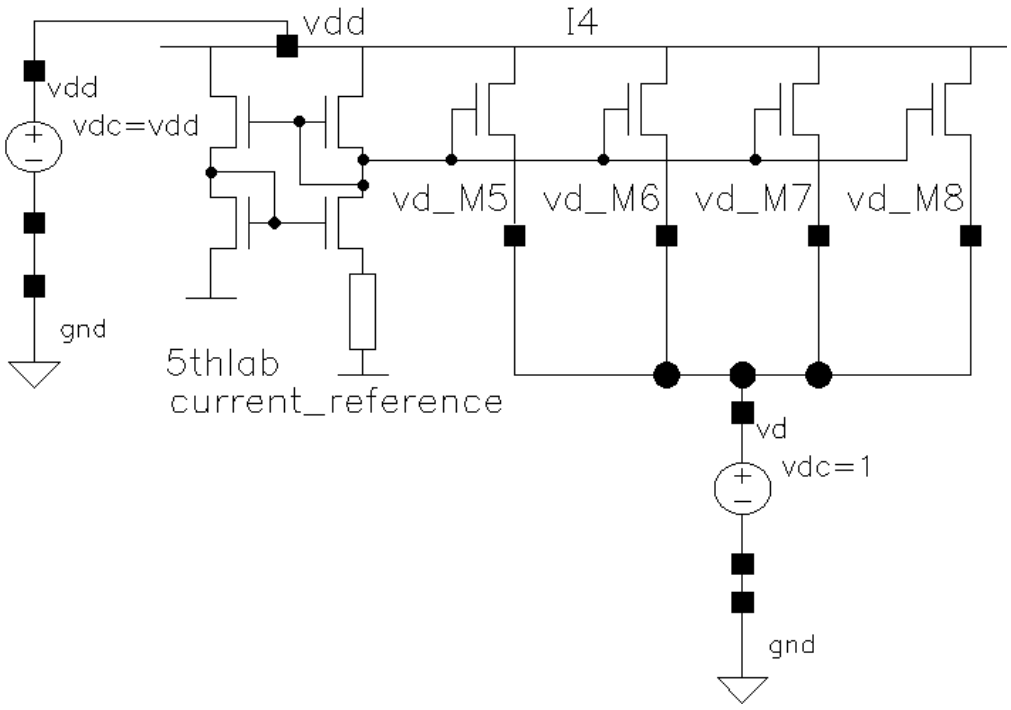

Figure 4: View `id_vd` (in cell `current_reference` and library `5thlab_sim`), used to obtain the drain current curves with the original current reference design.

Afterwards, ADE GXL was launched, since corner analysis will be performed in this test bench. Initially, a Test was added, in which the values mentioned previously were attributed to the variables R_S, L, a_p and a_n (and $3.3V$ to `vdd`). A DC analysis was selected with a step size of 0.025 and

the drain currents of the transistors M_5 to M_8 were selected - however, the curves for these four transistors are exactly the same, as expected; thus, only the I_D curves for transistor M_5 will be shown throughout this report.

By running the simulation, it could be seen that the current's (absolute) value in **saturation** differed significantly from $1\mu A$. This is (largely) due to the many **simplifications and approximations** considered in the theoretical model for this device. Thus, a Parametric Analysis was made, in which the value of R_S was changed in order to obtain the desired current value (or the closest possible) at $\boldsymbol{V_D = 1.0V}$. This voltage value was chosen since it is not too close to either limits of the saturation region; since the effect of the channel-length modulation is evident, the current will increase throughout this region, nevertheless. The curves obtained for some values of R_S are shown in Figure 5. Here, it can be seen that, as the value of R_S increases, the current's (absolute) value also increases and that the desired $I_D = -1\mu A$ occurs between $R_S = 42k\Omega$ and $R_S = 44k\Omega$. Having done further simulations with R_S changing between these two values, it was concluded that, with $\boldsymbol{R_S = 42.88k\Omega}$, the closest current value to $-1\mu A$ (with only a 0.2% difference) was obtained at $V_D = 1.0V$, thus this resistance value will be used with the original current reference design.

An important thing to take into account is that, throughout this report, the current values are negative. Therefore, the expected drain current in transistors M_3 and M_4 is $-2\mu A$, whereas this value is $-1\mu A$ for the other pMOS transistors (instead of $2\mu A$ and $1\mu A$, respectively). A similar argument applies to the other current reference design.

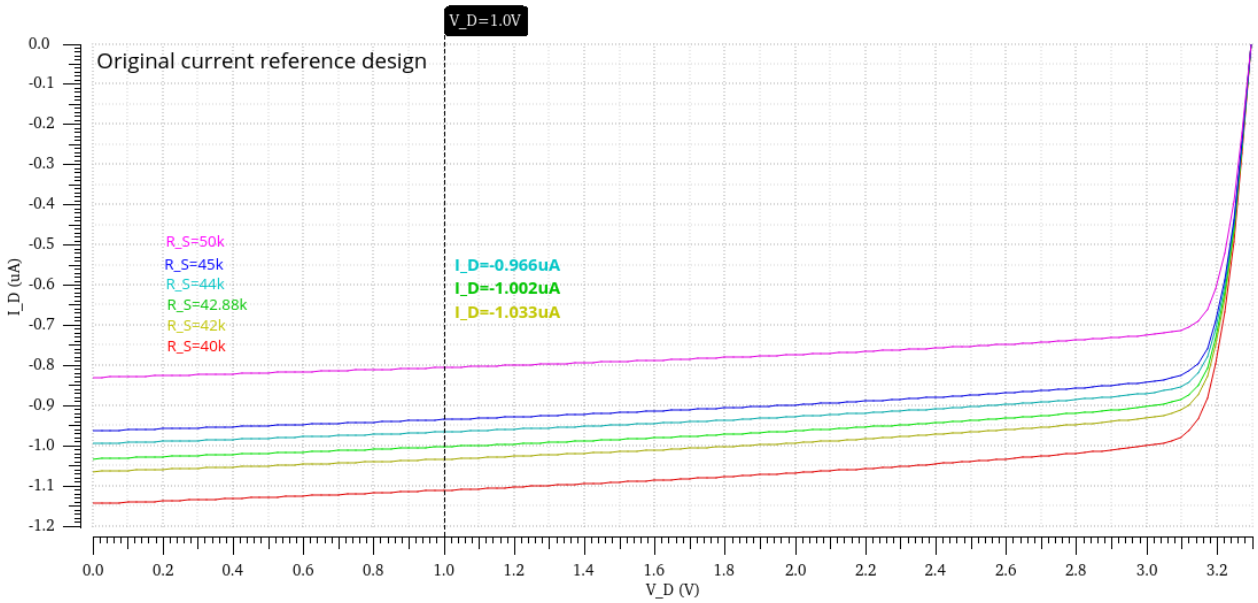

Figure 5: Simulations done in the view shown in Figure 4 with different values of R_S, indicated alongside the plot (in ohms). The closest I_D values to $-1\mu A$ at $V_D = 1.0V$ are also shown.

Using $R_S = 42.88k\Omega$, a DC analysis was made once again and the curve shown in Figure 6 was obtained, as well as the values indicated in Table 2. Using ten points in the saturation region (more specifically, from $V_D = 0.6V$ to $V_D = 2.4V$ with steps of $0.2V$), the slope of the blue curve was determined using Fitteia, a web-based fitting platform. The value of $\boldsymbol{g_{SD}}$ (which is the slope in equation 2) is also included here.

When $V_D = V_{DD} = 3.3V$, it can be seen that $I_D = 0A$ - this happens because $V_{SD} = 0V$ for M_5. The transistor is in the triode region until V_D decreases to $3.1V$, since V_{SD} reaches $V_{OD} = 0.2V$; for lower values of V_D, the transistor works in the saturation region, since $V_{SD} > V_{OD}$. It is worth noting that $V_{SG} = V_{DD} - V_D(\mathrm{M}_2) = 0.895V$ for M_5, which is higher than the threshold voltage $V_{TH} = 0.68V$ shown in the datasheet [4]. It can be seen, however, that the current increases (in absolute value) considerably in saturation, having a 16.8% increase from $V_D = 3.1V$ to $V_D = 0V$. Moreover, a slope

of the same order of magnitude as $10^{-8}A/V$ was obtained.

It can also be seen, in Table 2, that $|I_D(\mathrm{M}_3)| < |I_D(\mathrm{M}_4)|$, which was predicted in section 1, due to the use of the resistor R_S. Moreover, a total current for the current reference generation of $|I_D(\mathrm{M}_3)| + |I_D(\mathrm{M}_4)| = 3.913\mu A$ was obtained, which is desirably lower than the maximum $4\mu A$ defined for this circuit (the difference is of -2.2%).

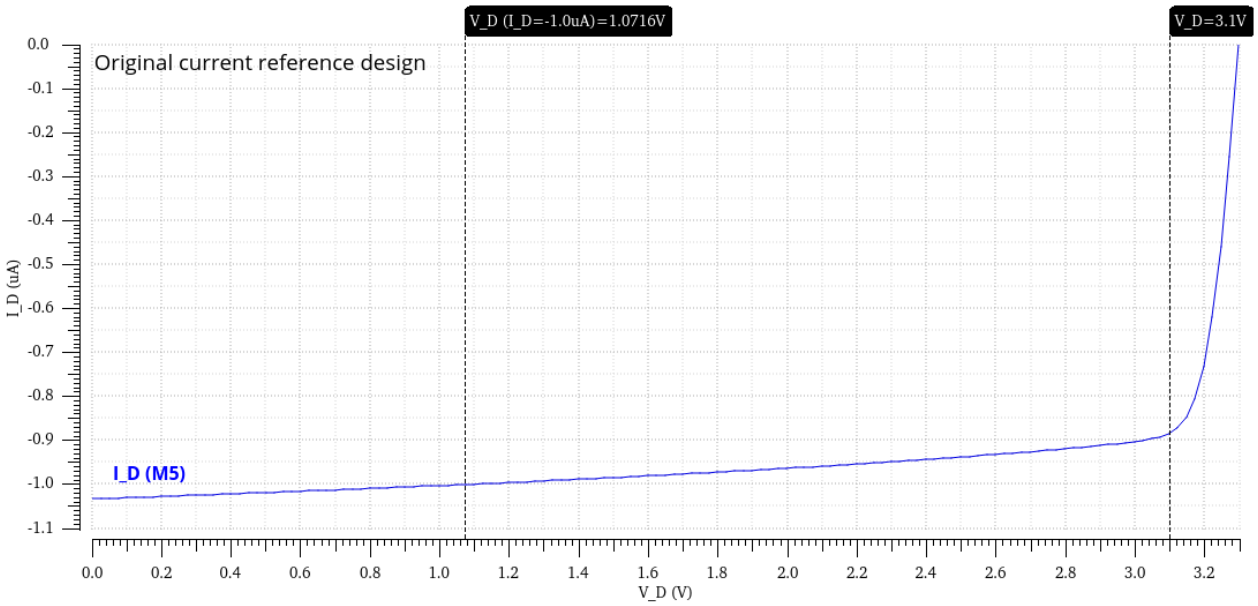

Figure 6: Drain current curve for transistor M_5 in the original current reference design. The two vertical markers identify the points in which $I_D = -1.0\mu A$ and $V_D = 3.1V \Leftrightarrow V_{SD} = V_{OD} = 0.2V$. At $V_D = 0,\ 3.1V$, the current values are $I_D = -1.033\mu A,\ -884.350nA$ (respectively).

$\boldsymbol{I_D(\mathrm{M_3})[\mu A]}$	$\boldsymbol{I_D(\mathrm{M_4})[\mu A]}$	$\boldsymbol{V_D(\mathrm{M_1})[mV]}$	$\boldsymbol{V_D(\mathrm{M_2})[V]}$	$\boldsymbol{V_{R_S}[mV]}$	$\boldsymbol{g_{SD}[nA/V]}$
-1.886 (-5.7%)	-2.027 (2.7%)	654.420	2.405	80.734	**42.054**

Table 2: Voltage and current values obtained in the DC simulation performed with the circuit shown in Figure 4. The values indicated in parenthesis are the relative differences between the experimental current values and $-2\mu A$. The slope given by equation 2 corresponds to g_{SD}.

2.2 Initial simulations with the new design

A similar simulation was made with the new current reference design presented in Figure 3. Once again, voltage sources were used for the supply voltage `vdd` and the drain voltages of the transistors on the right. However, in this case, another instance `vdc` (named `vx`) was connected between `vcasp` and `vdd` and its voltage value was defined as a variable with the same name. This test bench is shown in Figure 7.

In order to choose the value of V_{casp}, it must be realized that, in order for transistors M_4 and M_9 to work in saturation, the maximum voltage value must be $V_{casp} = V_{DD} - 2V_{OD} - V_{TH}$. With the design shown in Figure 3, it can be concluded that, starting at the supply voltage V_{DD}, there should be an initial voltage drop of $V_{OD} = V_{SD}(\mathrm{M}_9)$, followed by a voltage drop of $V_{SG}(\mathrm{M}_4) = V_{OD} + V_{TH}$, in which V_{TH} is the threshold voltage value for M_4. In the datasheet, the parameter $|V_{TH}| = 0.68V$ is shown (for pMOS with long channels, which leads to a better approximation of V_{TH} with $L = 1\mu m$, used in this laboratory assignment). Thus, a value of $V_{casp} = 2.22V$ would be considered. **However**, transistor M_4 suffers from **body effect**, because its bulk is not connected to its source (it is connected to V_{DD}) - therefore, $|V_{TH}|$ will increase.

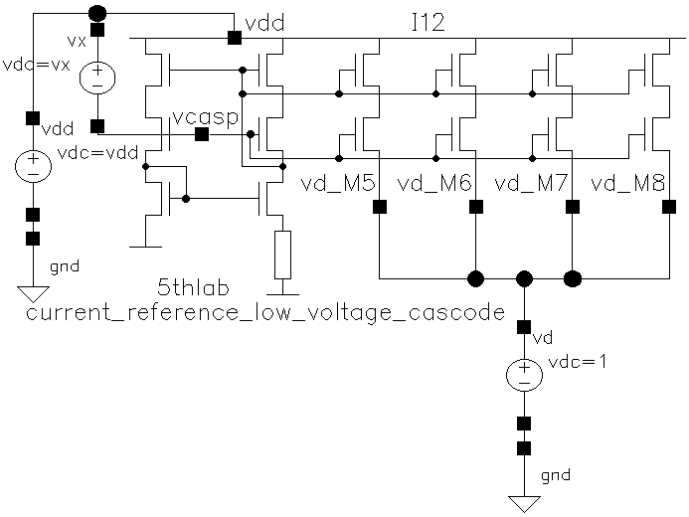

Figure 7: View `id_vd` (in cell `current_reference_low_voltage_cascode` and library `5thlab_sim`), used to obtain the drain current curves with the new current reference design.

In order to determine a proper value for V_{casp}, a DC sweep was made in a Parametric Analysis for different values of this voltage parameter. As shown in Figure 8, even though $\texttt{vcasp} = 2.2V$ lead to a proper behaviour of the circuit, there was still a relatively significant decrease in $|I_D|$ when `vcasp` was lowered to $2.1V$. However, decreases of such magnitude were not verified for even lower `vcasp` values. Thus, throughout this laboratory assignment, the value of $\boldsymbol{V_{casp} = 2.1V}$ was used. Considering $V_{casp} = V_{DD} - 2V_{OD} - V_{TH}$, this would lead to $V_{TH_{exp}} = 0.82V$, which has a 20.6% relative difference from $|V_{TH}| = 0.68V$ in the datasheet - as expected, due to the body effect described in equation 4.

Once again, a Parametric Analyis for different values of R_S was made, since using $R_S = 42.88k\Omega$ lead to current values relatively different from $-1\mu A$ in saturation. This makes sense, due to the simplifications of the theoretical model presented in section 1 and the considerable effect of channel-length modulation in the previous design. Some plots obtained for different R_S values are shown in Figure 9. Once again, by measuring I_D at $V_D = 1.0V$, it was determined that $\boldsymbol{R_S = 38.67k\Omega}$ allowed I_D to be as close to $-1\mu A$ as possible - this resistance value will be used in other simulations with the new current reference design.

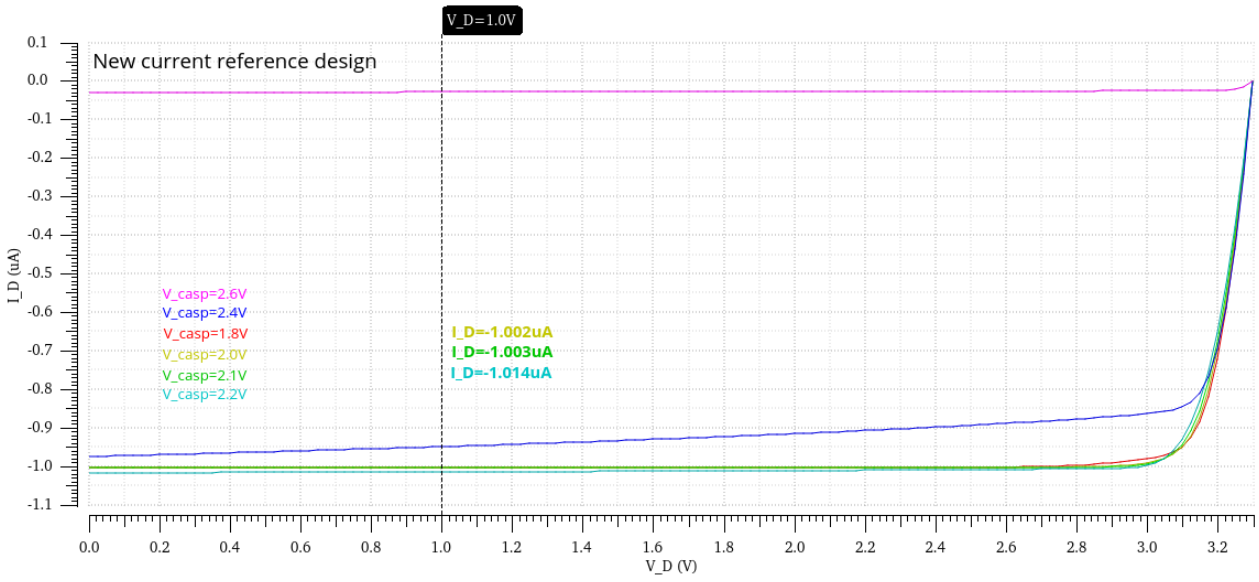

Figure 8: Simulations done in the view of Figure 7 with different V_{casp} (and $R_S = 38.67k\Omega$), indicated alongside the plot. The closest values to $I_D = -1\mu A$ at $V_D = 1.0V$ are also shown.

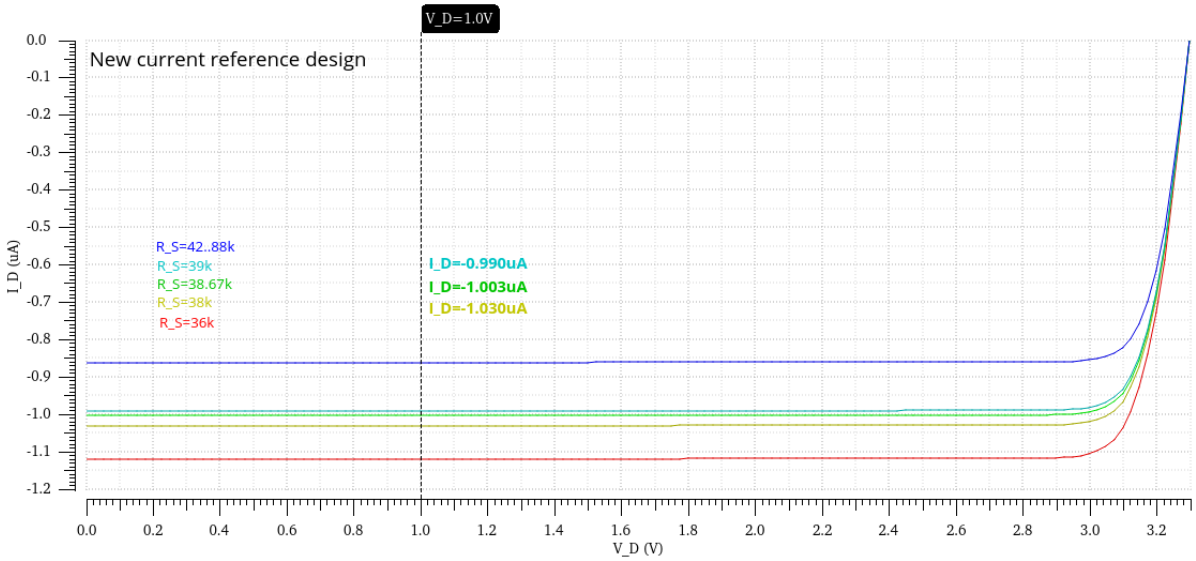

Figure 9: Simulations done in the view of Figure 7 with different R_S (and $V_{casp} = 2.1V$), indicated alongside the plot (in ohms). The closest values to $I_D = -1\mu A$ at $V_D = 1.0V$ are also shown.

Having obtained the values of R_S and V_{casp}, the drain voltage in the pMOS transistors was swept from 0 to $3.3V$ once again, having the plot in Figure 10 and the data in Table 3 been obtained. Once again, the triode and saturation regions are clear; in this case, however, saturation is reached when V_D lowers to (approximately) $2.9V$, since it would be expected that $V_{SD}(\mathrm{M}_{11}) = V_{OD}$, thus $V_S(\mathrm{M}_3) = 3.1V$. The relation $V_{SD}(\mathrm{M}_5) = V_{OD}$ would then be verified at $\boldsymbol{V_D = 2.9V}$.

In this case, the impact of channel-length modulation is much less significant, having a slope of the order of magnitude of $10^{-9}A/V$ been obtained - one order of magnitude lower than in the original current reference design. Moreover, $|I_D|$ only increases 0.3% from $V_D = 2.9V$ to $V_D = 0V$. In Table 2, it can be seen that the total current for the current reference generation can be given by $|I_D(\mathrm{M}_3)| + |I_D(\mathrm{M}_4)| = 4.011\mu A$, which differs in about 0.3% from the desired maximum $4\mu A$. This difference is less significant than in the previous design, although a higher current than $4\mu A$ was obtained here. It was also obtained that $V_{GS}(\mathrm{M}_1) = V_D(M_1) = 653.520mV$; assuming that $V_{GS} = V_{OD} + V_{TH_1}$ (with $V_{OD} = 0.2V$), the value $V_{TH_1} = 453.520mV$ is obtained - it differs in only about -0.8% from $V_{TH_{tab}} = 0.46V$ in the datasheet [4]. Moreover, $V_{GS_2} = V_D(\mathrm{M}_1) - V_{R_S} = 576.117mV$ is smaller than V_{GS_1}, as expected due to the theoretical analysis presented in section 1. Finally, it was determined that $V_S(\mathrm{M}_3)$ and $V_S(\mathrm{M}_4)$ do not differ considerably - only in $5mV$ - which makes sense due to the symmetry in voltages which characterizes the cascode current mirrors.

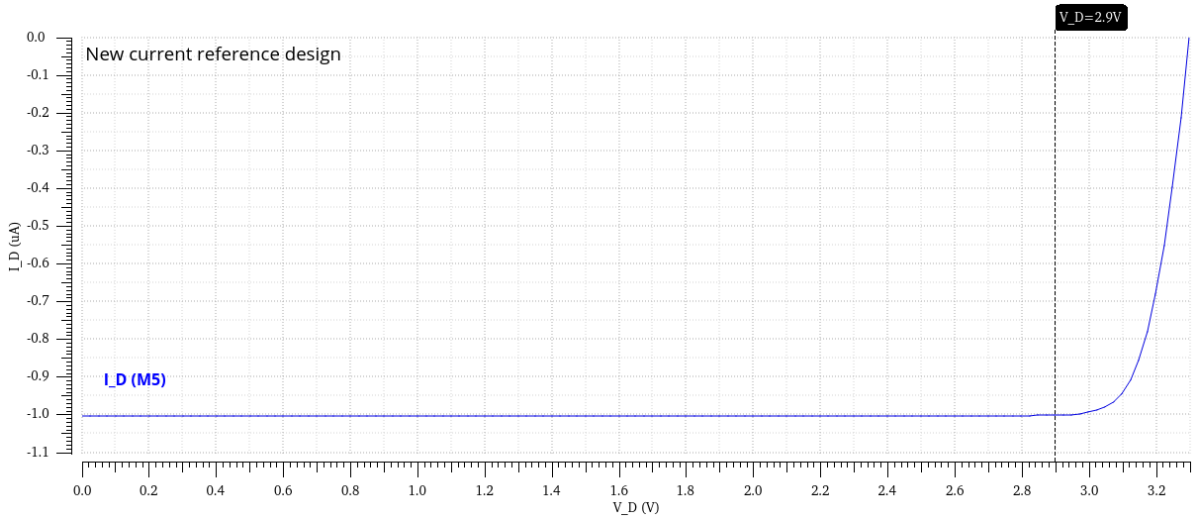

Figure 10: Drain current curve for transistor M_5 in the new current reference design. The vertical marker identifies the point in which $V_D = 2.9V \Leftrightarrow V_{SD} = V_{OD} = 0.2V$. At $V_D = 0,\ 2.930,\ 2.9V$, the current values are $I_D = -1.004,\ -1,\ -1.001\mu A$ (respectively).

$I_D(\mathrm{M_3})[\mu A]$	$I_D(\mathrm{M_4})[\mu A]$	$V_D(\mathrm{M_1})[mV]$	$V_D(\mathrm{M_2})[V]$	$V_S(\mathrm{M_3})[V]$	$V_S(\mathrm{M_4})[V]$	$V_{R_S}[mV]$	$g_{SD}[nA/V]$
-2.004 (0.2%)	-2.007 (0.4%)	653.520	2.396	3.058	3.053	77.403	**0.623**

Table 3: Voltage and current values obtained in the DC simulation performed with the circuit shown in Figure 7. The values indicated in parenthesis are the relative differences between the experimental current values and $-2\mu A$. The slope given by equation 2 corresponds to g_{SD}.

Regarding these simulations, the plots presented in Figure 11 (for some of the voltages in the circuit) were also obtained. It can be seen that, for higher values of V_D (thus, lower V_{SD} in transistor $\mathrm{M_5}$), the pMOS is in the triode region; as V_D decreases, it tends to the value of the drain voltages in transistors $\mathrm{M_9}$ and $\mathrm{M_{10}}$, due to the symmetry in voltages that occurs in a cascode current mirror implementation. However, a small slope exists in saturation - the resulting change in V_{SD} is what allows the channel-length modulation to still have some influence in the low voltage cascode current mirror, as described by equation 2.

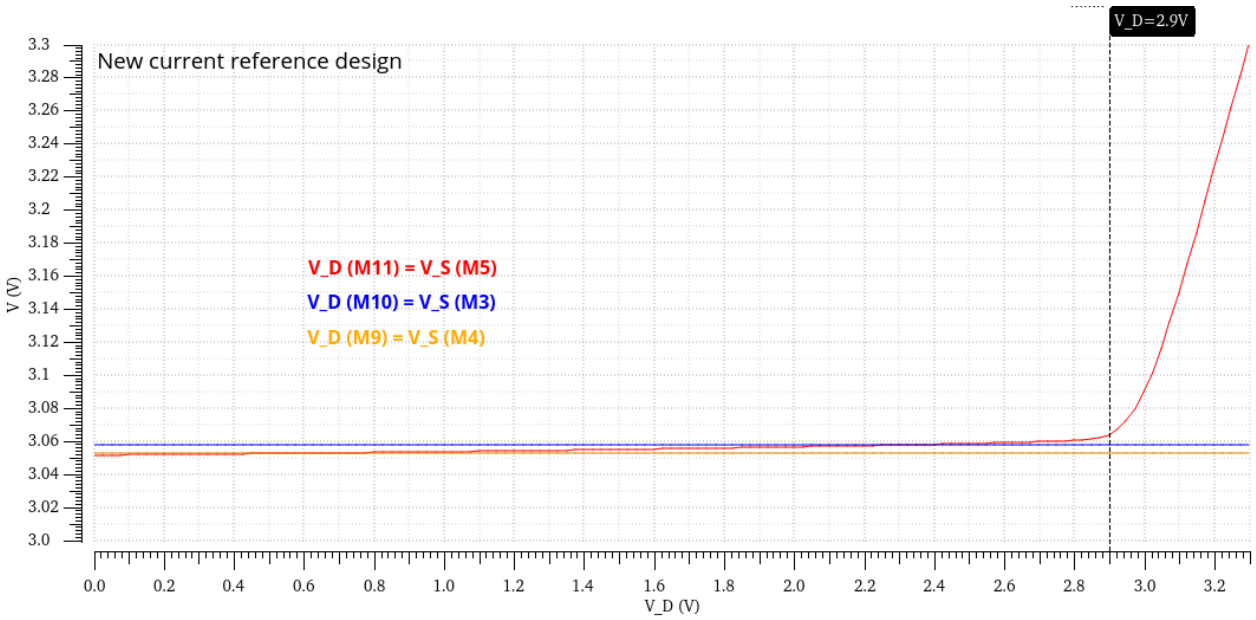

Figure 11: Voltage curves obtained in the DC simulation done with the new current reference design. The vertical marker identifies the point in which $V_D = 2.9V \Leftrightarrow V_{SD} = V_{OD} = 0.2V$.

3 Corner analysis

In order to perform corner analysis with the circuits shown in section 2, different `.sdb` files were created to run separate simulations for extreme temperatures -40^oC and 125^oC, extreme values for V_{DD} ($3.0V$ and $3.6V$, which correspond to a $\pm 10\%$ variation in $V_{DD} = 3.3V$) and process parameters. These files were named, respectively, `ams_corners_temperature`, `ams_corners_vdd` and `ams_corners_cmos`.

In Table 4, the changes in mobility and threshold voltage for each corner related with the process parameters are indicated. For WO (worst case one) the mobility μ increases for the nMOS and decreases for the pMOS, while the opposite happens to the threshold voltage, V_{TH}, thus implying a faster nMOS and slower pMOS. For WZ (worst case zero), μ decreases for the nMOS and increases for the pMOS, while the opposite happens to V_{TH}, implying slower nMOS and faster pMOS. For WP (worst case power), μ increases for the nMOS and the pMOS, while the opposite happens to V_{TH}, implying faster nMOS and faster pMOS. For WS (worst case speed), μ decreases for both the nMOS and the pMOS, while the opposite happens to V_{TH}, implying slower nMOS and slower pMOS transistors.

Designation	nMOS	pMOS
WO	$\mu \nearrow V_{TH} \searrow$	$\mu \searrow V_{TH} \nearrow$
WZ	$\mu \searrow V_{TH} \nearrow$	$\mu \nearrow V_{TH} \searrow$
WP	$\mu \nearrow V_{TH} \searrow$	$\mu \nearrow V_{TH} \searrow$
WS	$\mu \searrow V_{TH} \nearrow$	$\mu \searrow V_{TH} \nearrow$

Table 4: CMOS corners considered in the corner analysis made in Section 3 - worst case one (WO), worst case zero (WZ), worst case power (WP) and worst case speed (WS) - including the respective variations in carrier mobility μ and threshold voltage V_{TH}.

In the ADE GXL, the `.sdb` files were then imported and the simulations were run, once again, with the DC analysis explained in section 2. In each following subsection, three separate graphs are initially shown, in order to separately evaluate the effect of each extreme condition (temperature, V_{DD} or CMOS parameters).

3.1 Original design

For the original current reference design shown in Figure 2, the drain current curves for different process parameters are shown in Figure 12. Moreover, the current values obtained at $V_D = 0V$ (maximum current absolute values), $V_D = 1.0V$ (in which the current was defined to be as close as possible to $-1.0\mu A$) and $V_D = 3.1V$ (the border value between the triode and saturation regions) are shown. **To be noted that, throughout these analyses, the current values to be discussed are always the absolute current values (due to their negative signs), unless indicated otherwise.**

It can be seen that the highest absolute values of the current happen in WZ. This happens because, as shown in Table 4, the **mobility of electrons μ_n** decreases, whereas the **mobility of holes μ_p** increases. This leads to a higher drain current in transistor M_5, due to equations 3 (in which μ_n is in the denominator) and 2 (in which μ_p is in the numerator). Contrarily, the smallest current values occur in WO, in which the opposite changes in mobility occur (μ_n increases and μ_p decreases).

As shown in Figure 12, the curves for WO and WP are very close together. In WP, μ_p increases, which would lead to higher current values, due to equation 2. However, it can be concluded that the **change in mobility μ_n is more significant** in changing the current values, since, in both cases, μ_n increases. The same reason explains why, for WS and WZ, the curves are also closer together - in both of them, the decrease in μ_n leads to higher I_D values. This makes sense, since the main function of the pMOS transistors M_3 and M_4 is for the circuit to bias itself, thus being as independent as possible from V_{DD}, similarly to what was discussed in the previous laboratory assignment for cascode current mirrors.

Similar conclusions can be obtained form the data shown in Table 5. It can be seen that the highest deviations occur for WZ, except for $V_D = 3.1V$. Here, in fact, the deviation in WS is positive, while it is negative for WZ (this can be due to the increase in V_{TH} which occurs in WS - thus, saturation is reached for higher values of V_D; in WZ, the change in V_{TH} is not as significant, since it increases due to the nMOS, but decreases due to the pMOS).

On the other hand, the lowest (negative) deviations occurred for WO, except at $V_D = 3.1V$ - in a similar way, the change in V_{TH} with WO is not as significant, but it decreases in WP, thus saturation is reached first (i.e., for higher V_D) in WO. It can also be seen that, except for $V_D = 3.1V$, the highest absolute values of the deviations occurred in the pair WS/WP. In these two cases, there is a higher impact of channel-length modulation, with higher currents and thus higher **power consumption** in the circuit.

In these simulations, the highest total current for the current reference generation was $4.441\mu A$, which happened in WS and has a 11.0% deviation from the desired maximum $4\mu A$ - thus, even though WS does not produce the highest I_D values, the variations in this aspect are the most considerable. On the other hand, WO had the lowest value, with $3.740\mu A$ (its deviation is -6.5%).

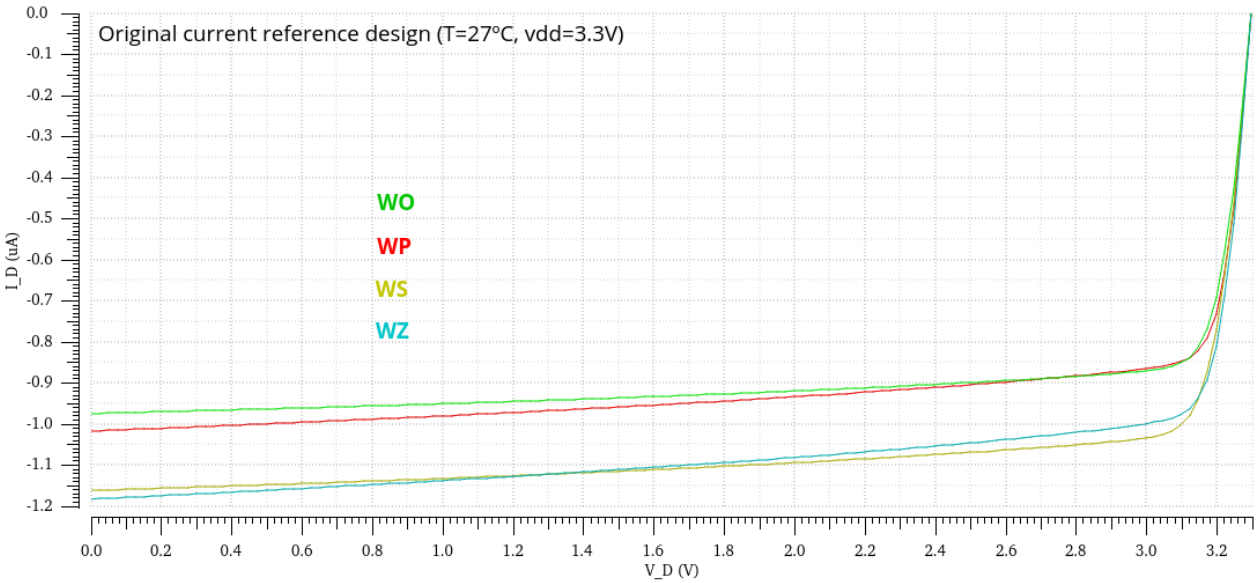

Figure 12: Drain current curves for transistor M_5 in the original current reference design (shown in Figure 2). Here, the effect of the process parameters is reflected.

$V_D(V)$	$I_D(WO)$ $[nA]$	Deviation (%)	$I_D(WP)$ $[\mu A]$	Deviation (%)	$I_D(WS)$ $[\mu A]$	Deviation (%)	$I_D(WZ)$ $[\mu A]$	Deviation (%)
0	-973.895	-2.6	-1.017	1.7	-1.161	16.1	-1.183	18.3
1.0	-950.414	-5.0	-0.980	-2.0	-1.132	13.2	-1.137	13.7
3.1	-852.046	-14.8	-0.849	-15.1	-1.004	0.4	-0.978	-2.2

Table 5: Current values in corner analysis for CMOS parameters performed with the original current reference design, as well as their respective relative variations from $-1\mu A$.

Regarding the plots made for temperature variations (shown in Figure 13), a considerable increase in current values occurs for $T = 125^oC$, reaching 41.1% at $V_D = 0V$. This occurs due to the **decrease in mobilities** at higher temperatures. At lower temperatures, on the contrary, carriers move more slowly, so there is more time for them to interact with charged impurities. As a result, generally, **as the temperature decreases, the mobility increases**. Because of this, the current values are lower at $T = -40^oC$, in which a -22.4% deviation occurs at $V_D = 1.0V$ (the value defined in section 2 to have a current of $-1.0\mu A$) - a more significant increase of 37.3% occurs at $T = 125^oC$.

These results shown, once again, that the change in $\boldsymbol{\mu_n}$ is more significant, since at lower temperatures both mobilities increase, but only the increase in μ_n leads to lower current values (due to equations 2 and 3); similarly, in higher temperatures both mobilities decrease and I_D is larger, even though the increase in μ_p would lead to lower currents.

Since the threshold voltage also decreases with the increase in temperature, the curve for $T = 125^oC$ should reach saturation for lower V_{SD} values (thus, higher V_D) - this can be noticed in Figure 13, in which the transition to a region with less variations in I_D clearly occurs at a lower V_D, the opposite happening for $T = -40^oC$. As seen in Table 6, the most significant deviations at $V = 0V$ and $V = 1.0V$ occur for $T = 125^oC$. The difference in I_{out} (in equation 3) is more significant when μ_n decreases because I_{out} is proportional to $1/\mu_n$ - in functions defined by $y = 1/x$, the increases in y due to increases in x are less significant than the decreases due to lower values of x.

Finally, the total currents for the current reference generation in these cases were $3.028\mu A$ in $T = -40^oC$ and $5.364\mu A$ in $T = 125^oC$ (its considerable deviations from $4\mu A$ are -24.3% and 34.1%, respectively).

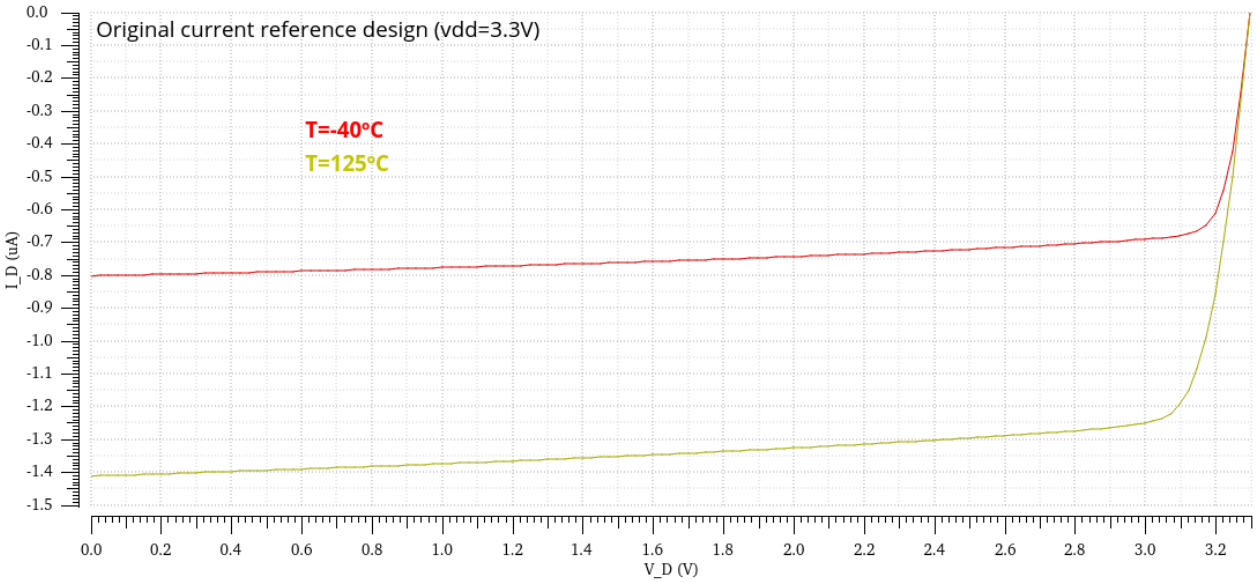

Figure 13: Drain current curves for transistor M_5 in the original current reference design (shown in Figure 2). Here, the effect of the temperature variations is reflected.

$V_D(V)$	$I_D(T=-40°C)$ $[nA]$	Deviation (%)	$I_D(T=125°C)$ $[\mu A]$	Deviation (%)
0	-801.361	-19.9	-1.411	41.1
1.0	-776.060	-22.4	-1.373	37.3
3.1	-678.606	-32.1	-1.195	19.5

Table 6: Current values in corner analysis for temperature performed with the original current reference design, as well as their respective relative variations from $-1\mu A$.

Finally, for the corner simulations done for $V_{DD} = 3.0,\ 3.6V$ (corresponding to a $\pm 10\%$ variation in the supply voltage), the results shown in Figure 14 and Table 7 were obtained. The graphs are only shown until $V_D = 3.0V$, in order not to have $V_D > V_{DD}$ in any circumstance (thus, V_{SD} in transistor M_5 does not become negative).

For lower values of V_D, it can be clearly seen that the current is quite similar between the two plots, having the deviations from $-1\mu A$ been different in 6.7 percentage points in $V_D = 0V$ and 6.9 percentage points for $V_D = 1.0V$ - much **smaller differences** than in the analysis for the process parameters and temperature. This makes sense, since this current reference design was made in order to be as independent of the supply as possible. Even then, this has not been achieved perfectly.

An incredibly higher difference between the two curves, however, happens for higher values of V_D. The reason why I_D remains more stable for all V_D values in the blue curve is that, since $V_{DD} = 3.6V$, transistors M_5 to M_8 will always work in the saturation region - because $V_D \leq 3.0V$, the relation $V_{SD} \geq 0.2V = V_{OD}$ is always true. The current changes nevertheless, however, due to the channel-length modulation.

On the other hand, for $V_{DD} = 3.0V$, a V_D value lower than $3.1V$ is required for the current to stabilize - in this case, it must be $\leq 2.8V$ to enter the saturation region (for this reason, the current values for $V_D = 2.8V$ are included in Table 7).

Finally, it is worth pointing out that the current values for $V_{DD} = 3.6V$ are always higher (in absolute value) in saturation, since the higher supply voltage leads to higher voltages in the transistors, which clearly leads to higher currents (as given by equation 2), thus leading to higher power consumption.

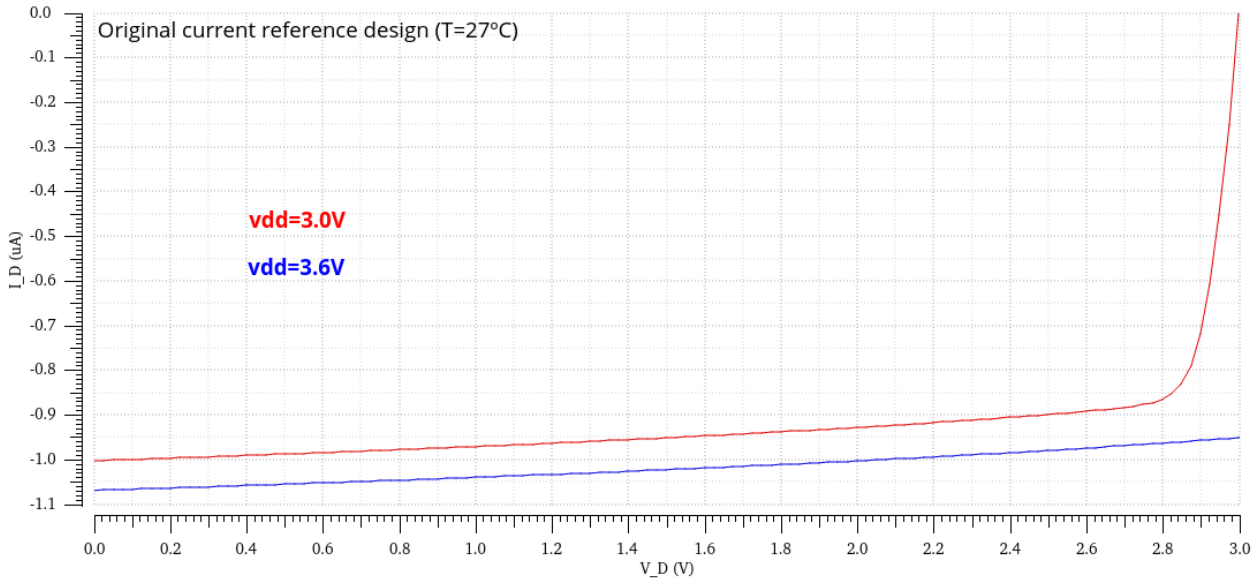

Figure 14: Drain current curves for transistor M_5 in the original current reference design (shown in Figure 2). Here, the effect of the supply voltage variations is reflected.

$V_D(V)$	$I_D(V_{DD} = 3.0V)$ $[\mu A]$	Deviation (%)	$I_D(V_{DD} = 3.6V)$ $[\mu A]$	Deviation (%)
0	-1.002	0.2	-1.069	6.9
1.0	-970.140$\times 10^{-3}$	-3.0	-1.039	3.9
2.8	-865.068$\times 10^{-3}$	-13.5	-962.490$\times 10^{-3}$	-3.8

Table 7: Current values in corner analysis for the supply voltage performed with the original current reference design, as well as their respective relative variations from $-1\mu A$.

Finally, a last simulation was made with the corners shown in Table 8, in which T and the process parameters were considered, since, in these cases, the higher current differences were observed previously. Using Figure 15 and Table 9, the best and worst combinations can be found - naturally, as seen in Figure 14, a lower V_{DD} will lead to slightly lower currents in saturation and vice-versa.

In this context, the highest drain currents occur in corners 3 and 7, in which μ_n not only decreases due to $T = 125^oC$, but also due to WS and WZ. In corner 3, an incredibly significant 67.7% deviation occurs at $V_D = 0V$ and a similarly worrying 63.9% at $V_D = 1.0V$. On the other hand, the lowest currents occur in corners 0 and 4, in which μ_n increases due to $T = -40^oC$ and WP or WO (respectively).

The lowest deviation of -33.4% occurs in corner 4 at $V_D = 3.1V$; once again, the deviations are much higher in the maximum $|I_D|$ situations, since a μ_n decrease will change I_{out} in equation 3 more significantly. These higher currents will lead to much higher power consumption, which can be critical in the functioning of this current reference design.

Parameter	**corner_0**	**corner_1**	**corner_2**	**corner_3**	**corner_4**	**corner_5**	**corner_6**	**corner_7**
cmos53.scs	cmoswp	cmoswp	cmosws	cmosws	cmoswo	cmoswo	cmoswz	cmoswz
temperature	-40	125	-40	125	-40	125	-40	125

Table 8: Characteristics of each corner simulated in Virtuoso. Here, the temperatures are in ^oC.

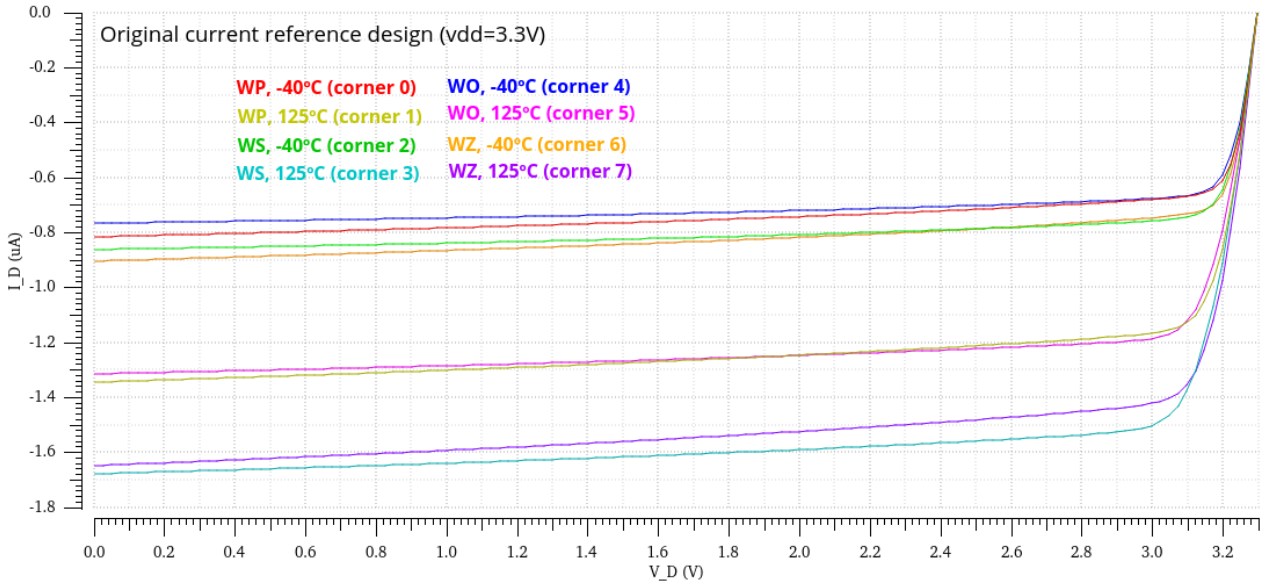

Figure 15: Drain current curves for transistor M_5 in the original current reference design (shown in Figure 2). Here, all eight corners described in Table 8 are taken into account.

$V_D(V)$	**Maximum $\lvert I_D\rvert$ (μA) (corner 3)**	Deviation (%)	**Minimum $\lvert I_D\rvert$ (nA) (corner 4)**	Deviation (%)
0	-1.677	67.7	-765.657	-23.4
1.0	-1.639	63.9	-746.184	-25.4
3.1	-1.376	37.6	-665.958	-33.4

Table 9: Maximum and minimum current values in corner analysis performed with the original current reference design for varying temperature and process parameters, as well as their respective relative variations from $-1\mu A$.

3.2 New design

The same corner analyses described in the beginning of section 3 were performed with the circuit shown in Figure 3. The results relative to the various process parameters are shown in Figure 16 and Table 10, in which a clear difference from the previous results is seen. In this case, WP and WO (in which μ_n increases) continue to result in lower current values in saturation; however, in this case, WP leads to lower values than WO, while the opposite happened in the original current reference design. Moreover, the positions of WZ and WS have also switched. This is because of the **lower impact of channel-length modulation**. In WP, μ_p **increases**, while it decreases in WO; therefore, as seen in Figure 12 (for the original design), the drain current for WP increased more significantly in saturation, even though the red and green curves had approximately the same value at $V_D = 3.1V$. **In this case**, however, since λ is not as significant (due to the cascode current mirror implementation), the current in WP does not increase significantly and remains above the WO curve. In WP, saturation is reached first (i.e., for higher V_D) due to the changes in V_{TH}.

In this new current reference design, the deviations are generally more significant in WP and WO than before, whereas the deviations were higher in the original current reference design for WZ and WS, which happened because the current increased significantly in the latter two cases due to channel-length modulation. In this case, WP and WO are worse in this regard since channel-length modulation loses its significance, thus the current value I_D when saturation begins does not change much, thus it remains far from the desired $1\mu A$ - in the previous design, even though I_D started smaller, as V_D decreased, that difference decreased.

Another important aspect to mention is that, in this case, the maximum total current for the current reference generation was $|I_D(\mathrm{M}_3)| + |I_D(\mathrm{M}_4)| = 4.06\mu A$ (for WS) which differs from $4\mu A$ in just 1.7% - a significant improvement from the 11.0% of the last design. The same can be said

about the minimum value $3.195\mu A$, much lower than the $3.740\mu A$ in the previous design - thus, with lower power consumption.

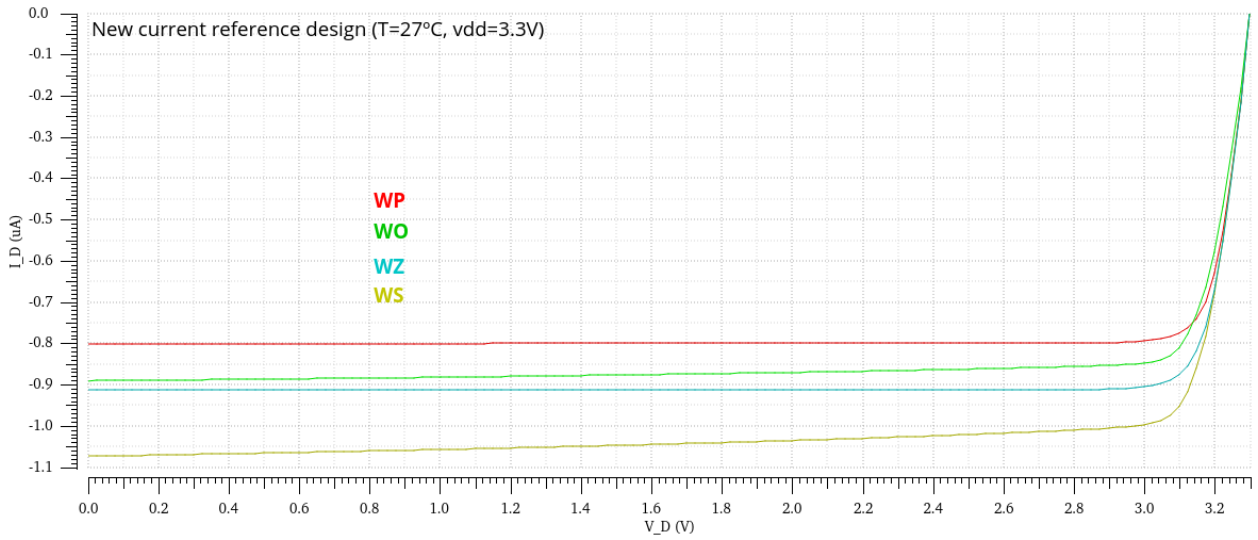

Figure 16: Drain current curves for transistor M_5 in the new current reference design (shown in Figure 3). Here, the effect of the process parameters is reflected.

$V_D(V)$	$I_D(WP)$ $[nA]$	Deviation (%)	$I_D(WO)$ $[nA]$	Deviation (%)	$I_D(WZ)$ $[nA]$	Deviation (%)	$I_D(WS)$ $[\mu A]$	Deviation (%)
0	-799.473	-20.1	-889.700	-11.0	-912.334	-8.8	-1.073	7.3
1.0	-799.216	-20.1	-881.108	-11.9	-911.955	-8.8	-1.056	5.6
2.9	-797.647	-20.2	-852.538	-14.7	-909.985	-9.0	-1.004	0.4

Table 10: Current values in corner analysis for CMOS parameters performed with the new current reference design, as well as their respective relative variations from $-1\mu A$.

Regarding the results for the temperature differences, once again a lower $T = -40^oC$ leads to lower I_D and vice-versa. This is because μ_n increases in the lower temperature, whereas an increase occurs for $T = 125^oC$. In this case, however, the most significant deviations occurs in the former - these deviations are even more considerable than in the original current reference design - which must be due to the lower impact of μ_p in the cascode current mirror. As described above, channel-length modulation progressively approximated the current values to $-1\mu A$ as V_D decreased.

In this case, the current values with $T = 125^oC$ are closer to $-1\mu A$; this should also occur because, now, the effect of the channel-length modulation has been diminished (thus, I_D does not increase as much). Finally, it is once again observed that the red curve reaches saturation for a higher V_D, due to the V_{TH} increase which occurs at lower temperatures (while the opposite happens in the yellow curve).

Once more, a significant improvement is achieved in this design in terms of $|I_D(\mathrm{M}_3)| + |I_D(\mathrm{M}_4)|$, which is $4.680\mu A$ at $T = 125^oC$ - it only differs in 17.0% regarding $4\mu A$, whereas this difference was of 34.1% previously. The minimum value is $2.684\mu A$, much lower than the respective value for the original design.

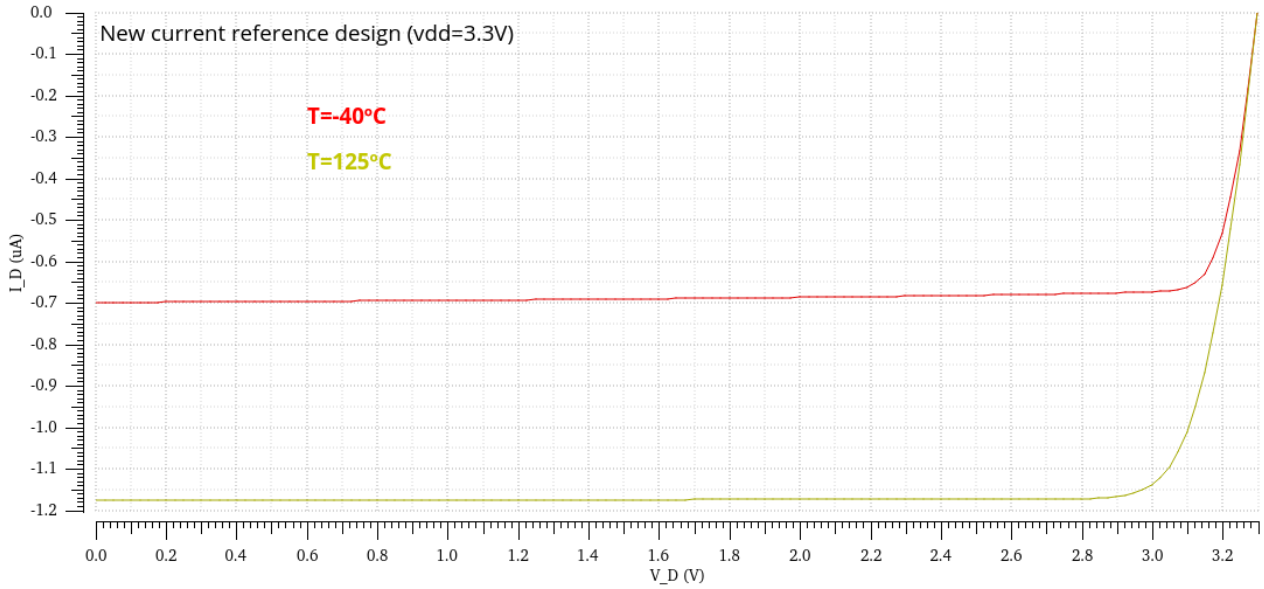

Figure 17: Drain current curves for transistor M_5 in the new current reference design (shown in Figure 3). Here, the effect of the temperature is reflected.

$V_D(V)$	$I_D(T=-40^oC)$ $[nA]$	Deviation (%)	$I_D(T=125^oC)$ $[\mu A]$	Deviation (%)
0	-698.057	-30.2	-1.175	17.5
1.0	-692.925	-30.7	-1.174	17.4
2.9	-674.895	-32.5	-1.166	16.6

Table 11: Current values in corner analysis for temperature performed with the new current reference design, as well as their respective relative variations from $-1\mu A$.

When V_{DD} changes, the current difference in saturation is once again not as significant. In this case, however, the difference in percentage points at $V_D = 0V$ and $V_D = 1.0V$ (which are both 2.8), are even lower than in the previous design, due to the implementation of the cascode current mirror. Once again, a higher V_{DD} leads to higher currents and higher power consumption, whilst the currents for $V_{DD} = 3.0V$ are always smaller than $1\mu A$. However, it is clear that this upgraded current reference design allowed for general lower power consumption. In this case, saturation is reached in the red curve once $V_D = 2.6V$.

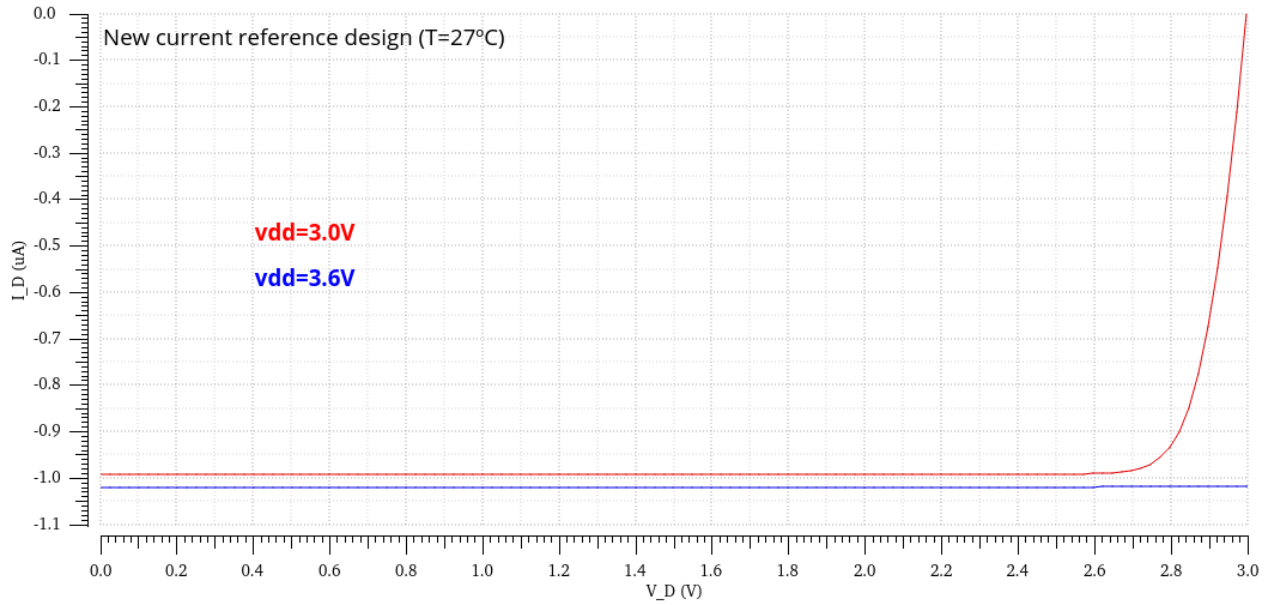

Figure 18: Drain current curves for transistor M_5 in the new current reference design (shown in Figure 3). Here, the effect of the supply voltage is reflected.

$V_D(V)$	$I_D(V_{DD} = 3.0V)$ $[nA]$	Deviation (%)	$I_D(V_{DD} = 3.6V)$ $[\mu A]$	Deviation (%)
0	-992.460	-0.8	-1.020	2.0
1.0	-991.994	-0.8	-1.020	2.0
2.6	-989.973	-1.0	-1.019	1.9

Table 12: Current values in corner analysis for the supply voltage performed with the new current reference design, as well as their respective relative variations from $-1\mu A$.

Finally, by simultaneously varying the CMOS parameters and temperature, the results shown in Figure 19 and Table 13 were obtained. The lowest currents in this case occur in corner 2. In this corner, **both** mobilities decrease due to WS, but they both **increase** due to the lower temperature - this means that the variation in μ due to lower T is more significant than the variation due to process parameters. However, it is worth noting that μ also decreases in corner 0 due to WP, even though this curve stands below the green curve; this should happen because V_{TH} decreases in WP, but increases in WS (thus saturation is reached first in the latter). Even though the stability of I_D is higher than in the previous design, the deviations in the minimum $|I_D|$ situation are higher in the new design, which is not favourable.

On the contrary, the highest currents (which lead to the highest power consumption) occur in corner 3 and the deviations are less significant now (regarding the two designs), in about 10 percentage points. In corner 3, the mobility μ_n decreases due to WS and $T = 125^oC$, therefore the current given by equation 3 is the highest.

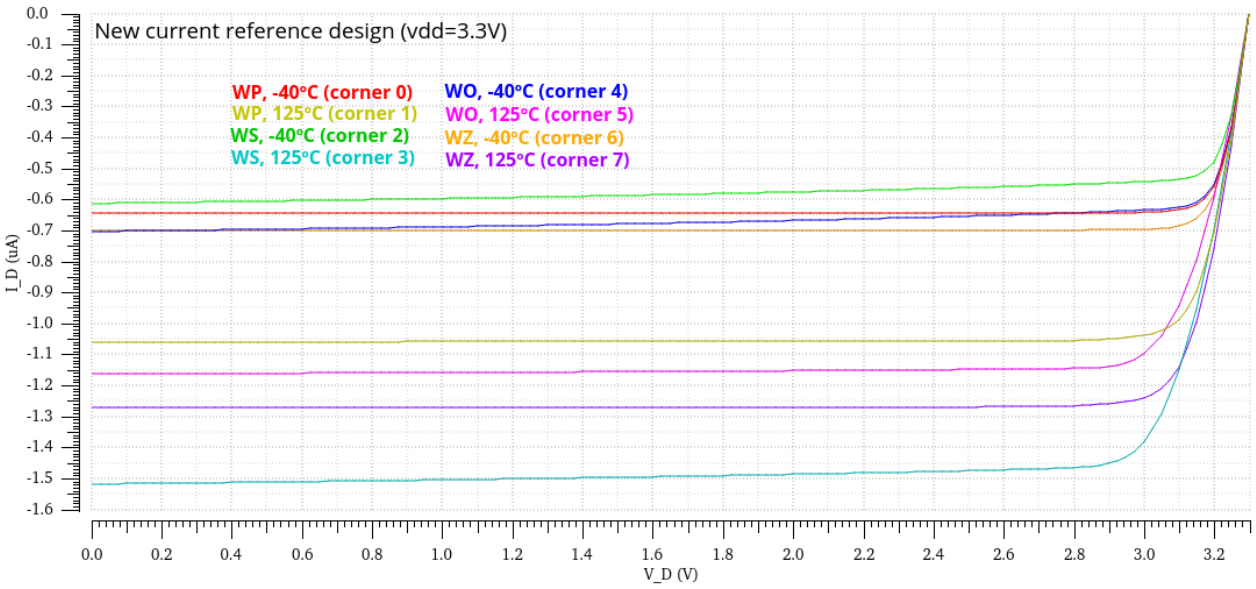

Figure 19: Drain current curves for transistor M_5 in the new current reference design (shown in Figure 3). Here, all eight corners described in Table 8 are taken into account.

$V_D(V)$	**Maximum $\|I_D\|$ $[\mu A]$ (corner 3)**	Deviation [%]	**Minimum $\|I_D\|$ $[nA]$ (corner 2)**	Deviation [%]
0	-1.517	51.7	-611.224	-38.9
1.0	-1.503	50.3	-595.572	-40.4
2.9	-1.452	45.2	-546.099	-45.4

Table 13: Maximum and minimum current values in corner analysis performed with the new current reference design for varying temperature and CMOS parameters, as well as their respective relative variations from $-1\mu A$.

4 AC analysis with noise at V_{DD}

In this section, instances `vsin` from library `analogLib` have been added to the test benches shown in Figures 4 and 7, connected to the constant voltage sources on the left and the sources of the upper pMOS transistors, having an amplitude of $1V$ been selected for this signal. By running an AC analysis and sweeping the frequency f from $10Hz$ to $1ZHz = 10^{21}Hz$, the plots of the drain currents are obtained with respect to the frequency. Since an amplitude of $1V$ was selected, the drain current's value will be the same as the **power supply rejection ratio (PSRR)**, although in different units - the latter in A/V, since it is given by $PSRR = I_D/(1V)$ (because a linear model is used in Virtuoso for this type of simulations). For each current reference design, a zoom in graph is shown, in which the initial values of the PSRR are clearer, as well as the range of frequencies for which they happen. In this laboratory assignment, the value of PSRR is not given in dB, since it relates two quantities in different units.

4.1 Original design

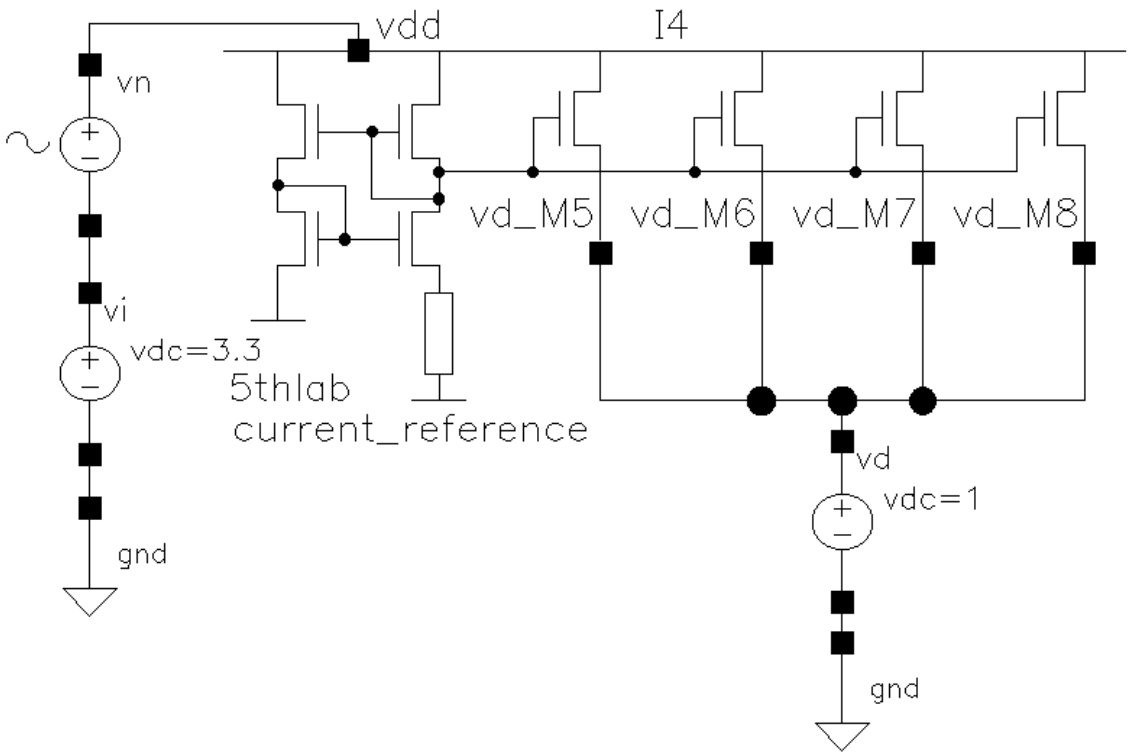

Figure 20: View `psrr_f` (in cell `current_reference` and library `5thlab_sim`), used to perform an AC analysis with the original current reference design (shown in Figure 2).

By running the AC simulation in the test bench shown in Figure 20, the plots of Figures 21 and 22 were obtained. For lower frequency values, PSRR had an approximately constant value close to $100nA/V$, which means that, for each volt of noise inserted in the supply voltage, a change in the drain current of approximately $\pm 100nA$ occurs. As the frequency increases, the PSRR changes significantly (starting at approximately $f = 10^{11}Hz$), reaching a stable value of $31.659mA/V$ at higher frequencies (for each volt of noise in the supply, the current changes $31.659mA$).

The reason why the PSRR is lower for lower frequencies is that the impedance of parasitic capacitances, given by $Z_C = 1/(j\omega C)$, is much higher. Therefore, they work similarly to open circuits, thus the noise does not affect the circuit too significantly. However, as f increases, the rejection of the noise becomes more limited, since the parasitic capacitances (in the transistors, for instance) provide alternating paths for the resulting currents - the gain of the device therefore decreases. As the frequency f becomes too large, the impedances Z_S of the parasitic capacitances of the transistors start filtering the noise; however, the PSRR remains high because of other parasitic

capacitances, such as the ones connected to the voltage source `vd` shown in Figure 2 - a voltage divider occurs with the impedances of the transistors of the pMOS transistors and the impedances due to this voltage source and the wiring itself.

In Figure 22, it can be seen that the value changes more significantly starting at $f \approx 10^6 Hz$, reaching a value of $8.55 \mu A/V$ with $f = 1GHz$, which means a very significant current variation for each volt of noise, taking into account the desired $1\mu A$ current in the outputs.

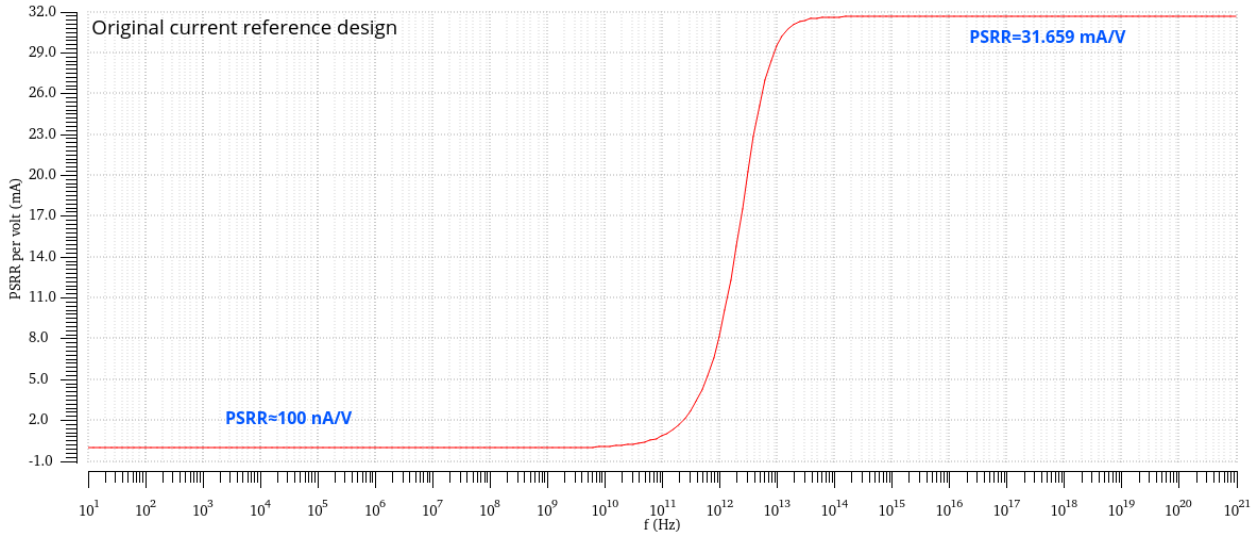

Figure 21: Plot obtained by running an AC analysis with the test bench shown in Figure 20, from $10Hz$ to $1ZHz$ and with 10 points per decade. The change of the power supply rejection ratio (PSRR) with frequency f is shown in units mA/V. At lower frequencies, $PSRR$ remained approximately at $100nA/V$.

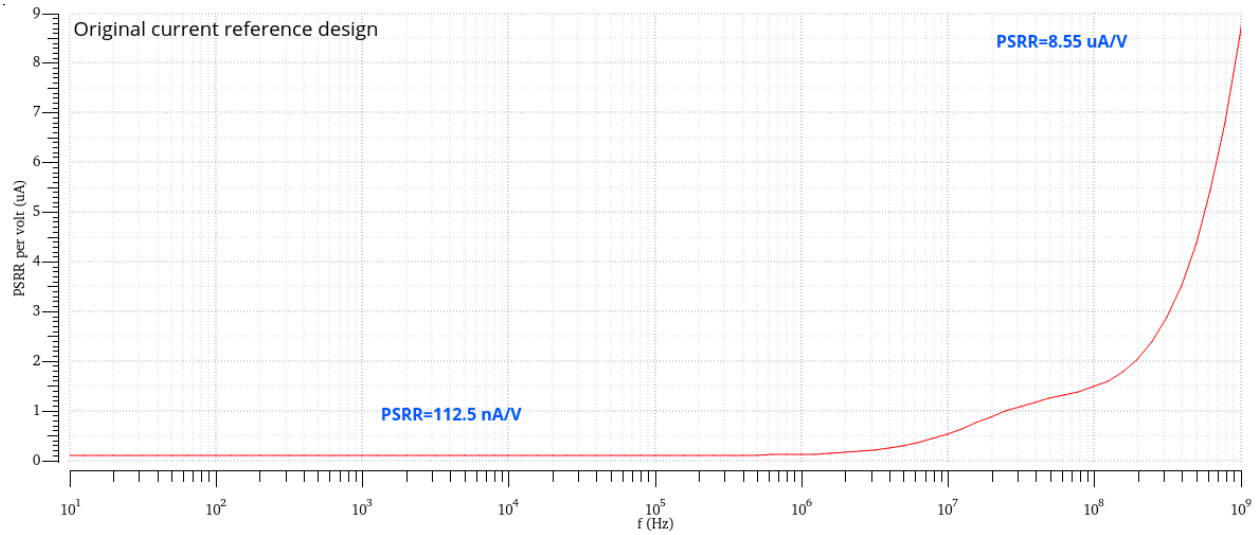

Figure 22: Detailed portion of the plot shown in Figure 21, in which the change in PSRR from the order of magnitude of $1\mu A$ to $10\mu A$ is clear. To do this, the frequency range between $10Hz$ and $1GHz$ was selected.

4.2 New design

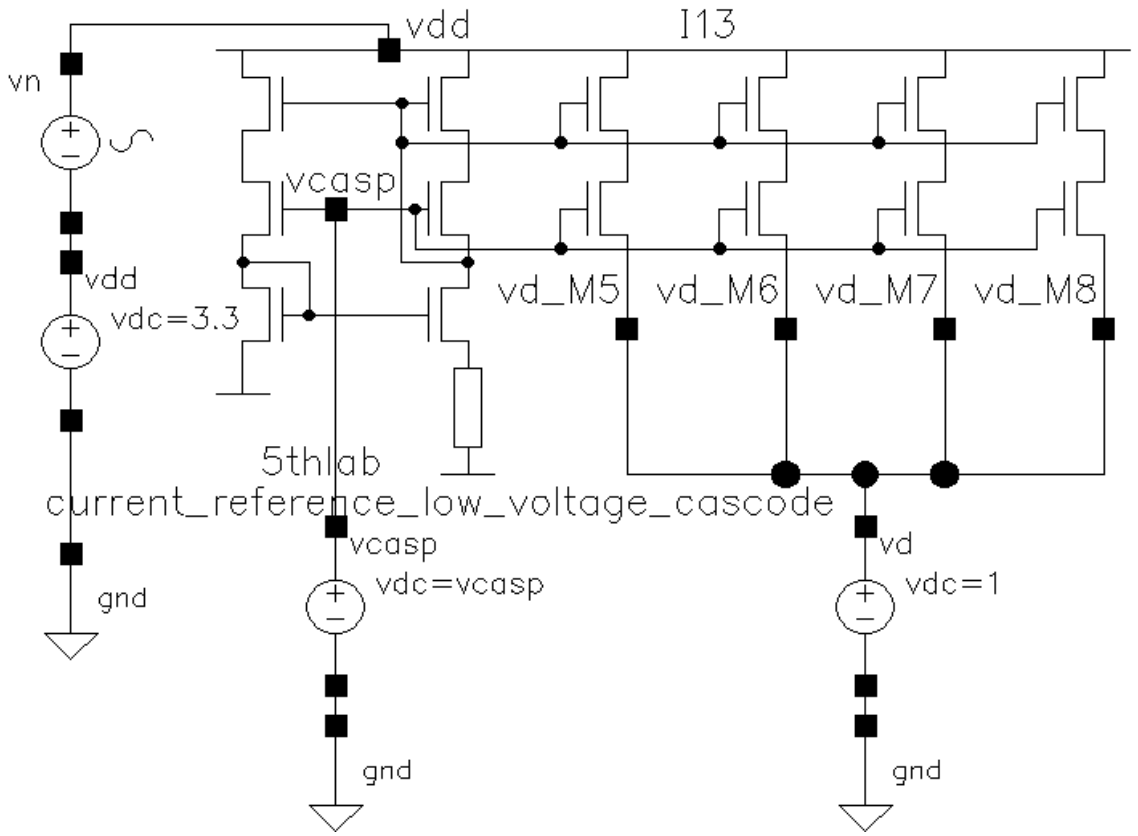

Figure 23: View `psrr_f` (in cell `current_reference_low_voltage_cascode` and library `5thlab_-sim`), used to perform an AC analysis with the new current reference design (shown in Figure 3).

Finally, the same simulation was made with the circuit shown in Figure 23, having the plots shown in Figure 24 and 25 been obtained. It was determined that the PSRR value at lower frequencies stayed approximately stable at $\approx 20nA/V$, which means a 82.2% decrease from the results shown in Figure 21 - thus, the output current is not as affected by the noise, which is an improvement regarding the original current reference design. Moreover, the constant value $PSRR = 26.172mA/V$ corresponds to a 17.3% decrease. Regarding the zoomed in detail, the more significant changes in PSRR start once again at $\approx 1MHz$, but in this case a higher value (in about $1\mu A/V$) is obtained for $f = 1GHz$.

The reason why, in this case, the values $PSRR \approx 20nA/V$ and $PSRR = 26.172mA/V$ are lower than the respective values in the previous design is that, in the cascode current mirror implementation, additional pMOS transistors are added above the ones introduced in the first design. Because of this, more parasitic capacitances, in series with the previous ones, exist. As a voltage divider can be applied with the impedances of the transistors in series (defined now as "Z_1") and the impedances due to the voltage source (and wires) "Z_2", the voltage divider law gives us the expression $Z_2/(Z_1 + Z_2)$ for the output, which decreases as Z_1 increases in the new current reference design - thus the lower PSRR at higher frequencies. At lower frequencies, the very high (additional) impedances $Z = 1/(j\omega C)$ make it even harder for noise to affect the output, thus a lower PSRR is also obtained. By taking this into account, it is clear that the implementation of the cascode current mirror is a significant improvement in terms of the capability of the electronic circuit to suppress power supply variations to its output signal.

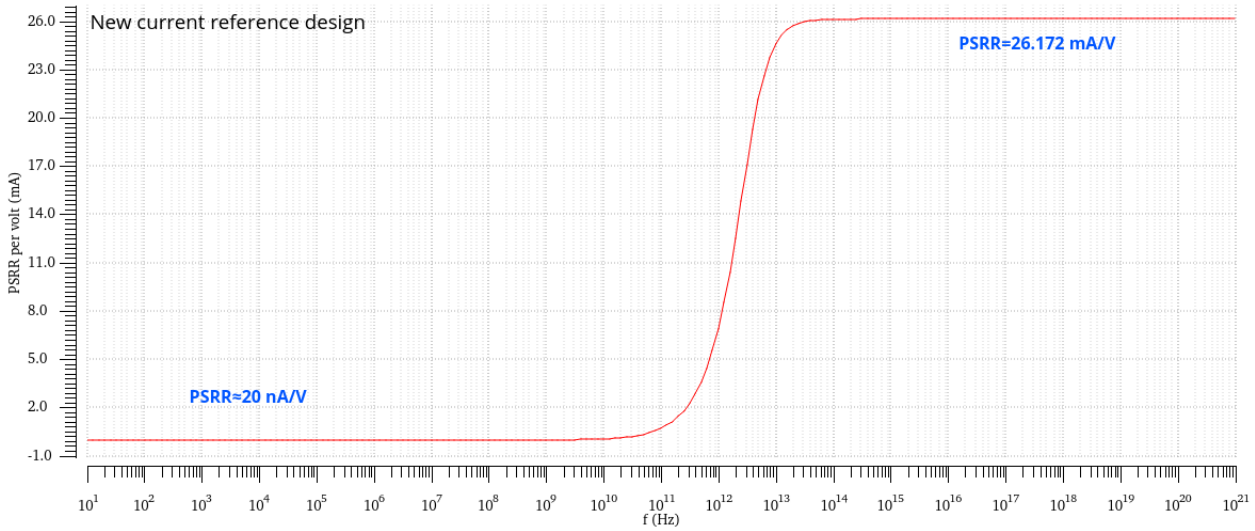

Figure 24: Plot obtained by running an AC analysis with the test bench shown in Figure 23, from $10Hz$ to $1ZHz$ and with 10 points per decade. The change of the power supply rejection ratio (PSRR) with frequency f is shown in units mA/V. At lower frequencies, $PSRR$ remained approximately at $20nA/V$.

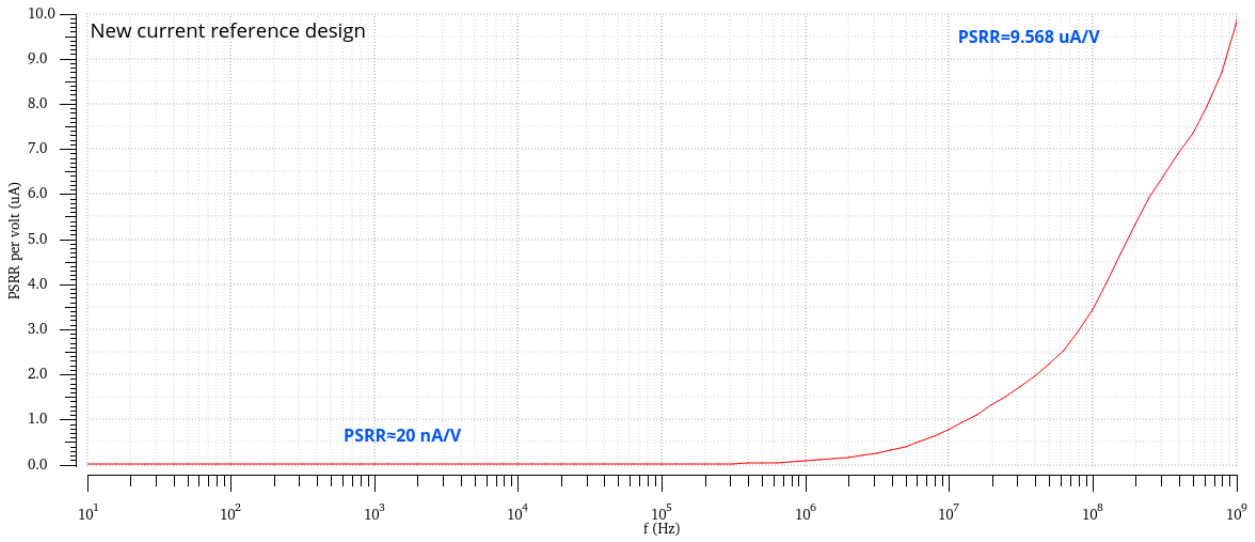

Figure 25: Detailed portion of the plot shown in Figure 24, in which the change in PSRR from the order of magnitude of $1\mu A$ to $10\mu A$ is clear. To do this, the frequency range between $10Hz$ and $1GHz$ was selected.

5 Conclusion

In this laboratory assignment, an initial current reference design was considered, in which a desired maximum current for the current generation was $4\mu A$. The outputs of this design were four currents of $1\mu A$ each, which corresponded to the drain currents of four different pMOS transistors. Firstly, a DC simulation was made, in which the drain voltage of these transistors was swept from 0 to $3.3V$ and the drain current curve was obtained. In order to have $1\mu A$ (in absolute value) at the output, the value of the resistance R_S had to be adjusted, due to the simplifications considered in the theoretical model. In this design, the effect of the channel-length modulation was apparent. After this, corner analysis was performed, by changing the process parameters, temperature and supply voltage (V_{DD}). The highest current values occurred for WZ and higher temperatures, due to the decrease in the mobility μ_n. When V_{DD} changed, the current did not change as significantly in

saturation, as intended.

Besides this, another current reference design was considered, in which a low voltage cascode current mirror implementation was used. After adjusting the values of V_{casp} and the resistance, the drain current curve was obtained, in which the impact of the channel-length modulation was not as apparent. In corner analysis, the highest current occurred once again for $T = 125^oC$, but also for WS, due to the lower significance of channel-length modulation.

Finally, an AC simulation was made with both designs, in which an AC noise signal of $1V$ in amplitude was added at the supply. The curves for the power supply rejection ratio (PSRR) in regards to frequency were obtained. In these, PSRR had a relatively stable value at lower frequencies, then increased significantly and remained constant for very high frequencies. In this report, the performances of both designs were analysed and compared bewteen each other, in terms of the PSRR and output current values (higher power consumption derived from higher values of these currents).

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