austriamicrosystems

0.35 µm CMOS C35 Process Parameters

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1. Introduction

1.1. Revision

Change Status of Pages (including short description of change)

Rev. 1	Affected pages:	1 to 62	(March 2002)
Subject of change: first version of process parameter specification			
Rev. 2	Affected pages:	1 to 62	(Feb. 2003)
Changed:	Parameters throughout the document due to parameter adjustments Chapter “Matching Parameter” taken out. All information about matching is included in the 0.35µm CMOS Matching Parameters document Eng – 228. SPICE Modelling.		
Added:	Tick metal module, MIM capacitor module, Poly fuses. MOS transistor threshold voltage measured in linear region. MIM capacitor in Wafer Cross Section.		

1.2. Process Family

This document is valid for the following 0.35µm CMOS processes:

Process name	No. of masks	CMOS core module *	POLY1-POLY2 capacitor module **	5 Volt module	High resistive poly module	Metal 4 module	Thick Metal module	MET2-METC capacitor module
C35B3C0	14	x	x					
C35B3C1	17	x	x	x				
C35B4C3	20	x	x	x	x	x		
C35B4M3	21	x	x	x	x		x	x

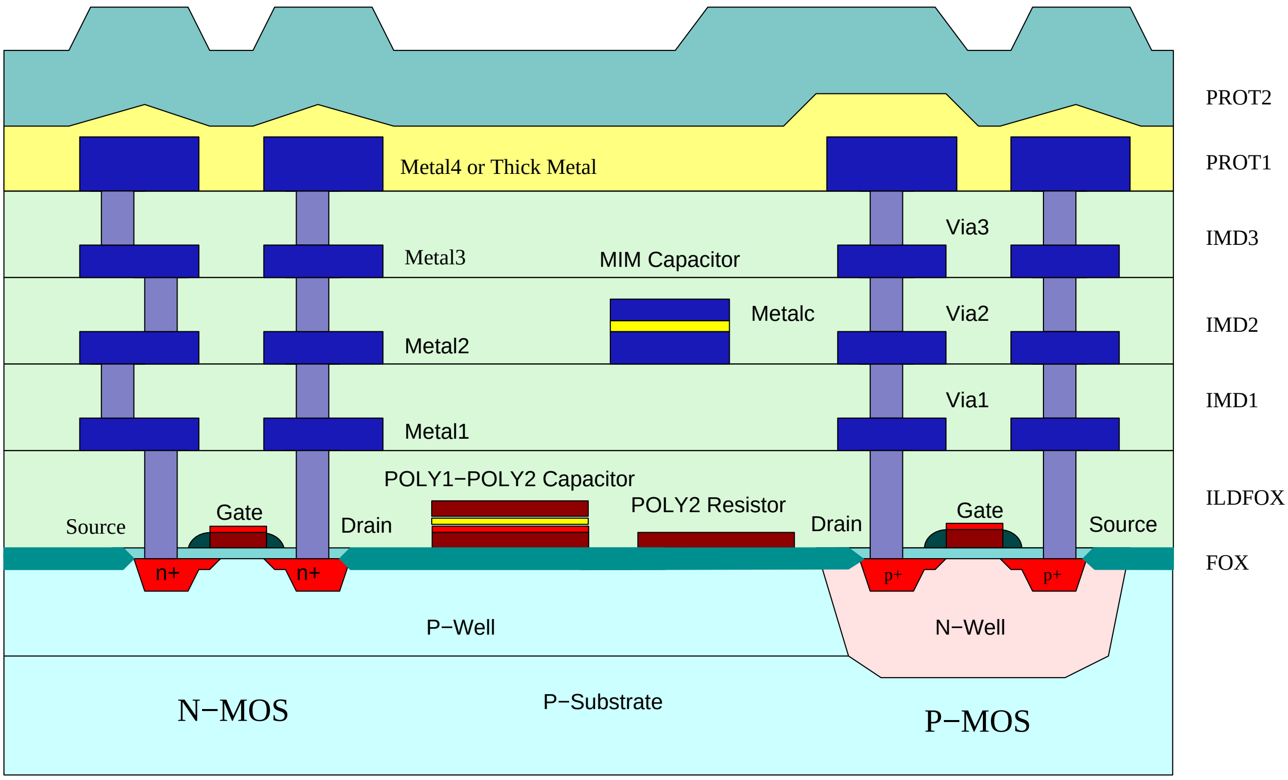
*) **CMOS core module**
consists of p-substrate, single poly, triple metal and 3.3 Volt process.
) **POLY1-POLY2 capacitor module
consists of p-substrate, double poly (RPOLY2 resistor), triple metal and 3.3 Volt process.

1.3. Related Documents

Description	Document Number
0.35µm CMOS C35 Design Rules	Eng - 183
0.35µm CMOS C35 Noise Parameters	Eng - 189
0.35µm CMOS C35 RF SPICE Models	Eng – 188
0.35µm CMOS Matching Parameters	Eng - 228

2. General

2.1. Wafer Cross – Section



2.2. Operating Conditions

2.2.1. Temperature Range

The processes described in this document are intended for the
Temperature range -40<=T<=125°C only.

2.2.2. Operating Voltage Range

The maximum operating voltages are specified in absolute values.
Note: The values in brackets denote absolute maximum ratings. These ratings are stress ratings only. Functional operation of the device at these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability (e.g. hot carrier degradation, oxide breakdown).

MOS Transistors	Device-name	max. VGS [V]	max. VDS [V]	max. VGB [V]	max. VDB [V]	max. VSB [V]	max. VBpsub [V]
3.3 Volt NMOS	NMOS	3.6 (5)	3.6 (5)	3.6 (5)	3.6 (5)	3.6 (5)	-
3.3 Volt PMOS	PMOS	3.6 (5)	3.6 (5)	3.6 (5)	3.6 (5)	3.6 (5)	5.5 (7)
5 Volt NMOS	NMOSM	5.5 (7)	5.5 (7)	5.5 (7)	5.5 (7)	5.5 (7)	-
5 Volt PMOS	PMOSM	5.5 (7)	5.5 (7)	5.5 (7)	5.5 (7)	5.5 (7)	5.5 (7)
high voltage NMOS (gate oxide)	NMOSH	3.6 (5)	15 (17)	3.6 (5)	15 (17)	3.6 (5)	-
high voltage NMOS (mid-oxide)	NMOSMH	5.5 (7)	15 (17)	5.5 (7)	15 (17)	5.5 (7)	-

PNP Bipolar Transistors	Device-name	max. VCE [V]	max. VEC [V]	max. VEB [V]	max. VBS [V]
vertical PNP (C = S)	VERT10	3.6 (5)	-	3.6 (5)	-
lateral PNP	LAT2	3.6 (5)	3.6 (5)	3.6 (5)	3.6 (5)

Capacitors	Device-name	max.Vterm-bulk [V]	max. Vterm1-term2 [V]
poly1-poly2	CPOLY	20 (30)*	5.5 (7)
MOS-Varactor	CVAR	3.6 (5)	3.6 (5)
metal2-metalC	CMIM	tbd	tbd

Operating Voltage Range (continued)

Resistors	Device-name	max. Vterm-bulk [V]
poly2	RPOLY2	20 (30)*
high resistive poly2	RPOLYH	20 (30)*
p+ diffusion	RDIFFP, RDIFFP3	5.5 (7)
n+ diffusion	RDIFFN, RDIFFN3	5.5 (7)
Low voltage n-well	RNWELL	13 (15)

*)An inversion layer is formed in the bulk underneath the poly if the poly-to-bulk voltage exceeds the field threshold voltage. The field threshold voltages are specified in section "Process Control Parameters".
Parasitics have the same maximum operating voltage as the primitive device they exist within. Please refer to section “2.3 Current Densities” as well.

2.3. Current Densities

Important application note:

The maximum allowed DC-current densities at 110°C are derived from reliability experiments. The specified values are also applicable as effective AC-current densities (RMS-values). In addition, the **peak AC-current densities must not exceed 30 times the specified DC-value**.

Parameter	Symbol	Min	Typ	Max	Unit
POLY1 current density	JPOLY			0.5	mA/µm
POLY2 current density	JPOLY2			0.3	mA/µm
MET1 current density	JMET			1.0	mA/µm
MET2 current density	JMET2			1.0	mA/µm
MET3 current density valid for triple metal process	JMET3T			1.6	mA/µm
MET3 current density valid for quadruple metal process	JMET3			1.0	mA/µm
MET4 current density	JMET4			1.6	mA/µm
METT thick metal current density	JMETT			tbd	mA/µm
CNT current density 0.4x0.4µm²	JCNT			0.94	mA/cnt
VIA current density 0.5x0.5µm²	JVIA			0.6	mA/via
VIA2 current density 0.5x0.5µm² valid for triple metal process	JVIA2T			0.9	mA/via
VIA2 current density 0.5x0.5µm² valid for quadruple metal process	JVIA2			0.6	mA/via
VIA3 current density 0.5x0.5µm²	JVIA3			0.96	mA/via
stack CNT/VIA current density 0.4x0.4µm² / 0.5x0.5µm²	JSTCNTVIA			0.6	mA/via
stack VIA1/2 current density 0.5x0.5µm²	JSTVIA12			0.4	mA/via
stack VIA2/3 current density 0.5x0.5µm²	JSTVIA23			0.64	mA/via
stack VIA1/2/3 current density 0.5x0.5µm²	JSTVIA123			0.64	mA/via

3. Process Control Parameters

3.1. Introduction

This section contains geometrical and electrical parameters which are measured for process control purposes. Temperature dependent parameters are extracted in the temperature range 25°C< T <125°C. All the other measurements are done at T0 = 27°C.

Process parameters are assigned to one of the following categories:

1. **PASS/FAIL PARAMETERS**
Pass/fail parameters are used for wafer selection during respectively after the wafer fabrication process. These parameters are extracted either from measurements within the fabrication process or from special process monitor test chips placed along the scribe line.
2. **INFORMATION PARAMETERS**
Information parameters are provided in order to increase the knowledge about the process behaviour. These parameters do not lead to wafer reject in case of failure.

CHARACTERISATION PARAMETERS are a special group of information parameters. They are not under 100% statistical control because they require extra large test structures (e.g. parasitic capacitors) or time consuming measurement procedures (e.g. temperature coefficients). These data are extracted from special process control monitor (PCM) test structures.

Note: It is strongly recommended that a design shall rely only on pass/fail parameters.

The electrical parameters are regularly extracted from the scribe line monitor (SLM) test structures on every wafer. This so-called **MAP (Manufacturing Acceptance Parameters) data** can be obtained from the Foundry Engineering group of austriamicrosystems AG in order to estimate if the fab run is more or less close to the typical mean process condition.

Important Note: The process control transistor parameters must not be used for circuit simulation purposes. They are extracted from simplified model equations in order to increase the speed of the measurements. Special circuit simulation transistor parameters are related to section "4. Simulation Model". Those are extracted from the complete set of model equations in order to give the best fit of the entire characteristic for all operating points. Therefore, process control transistor parameters may differ from their corresponding circuit simulation transistor parameters.

3.2. CMOS Core Module Parameters

3.2.1. Structural and Geometrical Parameters

PASS/FAIL PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
field oxide thickness	TFOX	260	290	320	nm	1
gate oxide thickness	TGOX	7.1	7.6	8.1	nm	2
poly1 thickness	TPOLY1	264	282	300	nm	1
metal1-poly oxide thickness (field region)	TILDFOX	395	645	895	nm	1
metal2-metal1 oxide thickness	TIMD1	620	1000	1380	nm	1
metal3-metal2 oxide thickness	TIMD2	620	1000	1380	nm	1
metal1 thickness	TMET1	565	665	765	nm	3
metal2 thickness	TMET2	540	640	740	nm	3
metal3 thickness (top metal)	TMET3T	775	925	1075	nm	3
passivation thickness 1	TPROT1	800	900	1000	nm	1
passivation thickness 2	TPROT2	800	1000	1200	nm	1
INFORMATION PARAMETERS						
metal1-poly oxide thickness (active region)	TILDDIFF	1140	1290	1440	nm	1
n+ junction depth	XJN		0.2		µm	4
p+ junction depth	XJP		0.2		µm	4
n-well junction depth	XJNW		2.0		µm	4
wafer substrate resistivity (non epi)	RSWAF	14	19	24	Ω cm	5
wafer thickness	TWAF	710		740	µm	5

3.2.2. MOS Electrical Parameters

3.2.2.1. MOS 3.3V N-Channel Electrical Parameters : NMOS

PASS/FAIL PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
threshold voltage long channel 10x10	VTO10X10N	0.36	0.46	0.56	V	6
threshold voltage short channel 10x0.35	VTO10X035N	0.40	0.50	0.60	V	6
threshold voltage short channel 10x0.35 (measured in linear region)	VT_N3	0.49	0.59	0.69	V	6
threshold voltage poly on field 0.6µm	VTFPN	15	> 20		V	9
effective channel length 0.35µm	LEFF035N	0.30	0.38	0.46	µm	10
effective channel width 0.4µm	WEFF04N	0.20	0.35	0.50	µm	11
body factor long channel 10x10	GAMMAN	0.48	0.58	0.68	$V^{1/2}$	12
gain factor	KPN	150	170	190	$\mu A/V^2$	7
drain-source breakdown 0.35µm	BVDS035N	7	> 8		V	14
saturation current 0.35µm	IDS035N	450	540	630	µA/µm	15
substrate current 0.35µm	ISUB035N		1.5	3	µA/µm	16
subthreshold leakage current 0.35µm	SLEAK035N		0.5	2	pA/µm	17
gate oxide breakdown	BVGOXN	7	> 8		V	18
INFORMATION PARAMETERS						
active channel length 0.35µm	LACT035N		0.29		µm	26
threshold voltage narrow channel 0.4x10	VTO04X10N		0.46		V	6
threshold voltage small channel 0.4x0.35	VTO04X035N		0.48		V	6
threshold voltage temperature coefficient	TCVTON		-1.1		mV/K	13
effective substrate doping	NSUBN		212		$10^{15}/cm^3$	12
effective mobility	UON		370		cm^2/Vs	8
mobility exponent	BEXN		-1.8		-	13

3.2.2.2. MOS 3.3V P-Channel Electrical Parameters : PMOS

Negative values are considered as absolute values for their Min/Max limits.

PASS/FAIL PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
threshold voltage long channel 10x10	VTO10X10P	-0.58	-0.68	-0.78	V	6
threshold voltage short channel 10x0.35	VTO10X035P	-0.55	-0.65	-0.75	V	6
threshold voltage short channel 10x0.35 (measured in linear region)	VT_P3	-0.62	-0.72	-0.82	V	6
threshold voltage poly on field 0.6µm	VTFPP	-15	< -20		V	9
effective channel length 0.35µm	LEFF035P	0.42	0.50	0.58	µm	10
effective channel width 0.4µm	WEFF04P	0.20	0.35	0.50	µm	11
body factor long channel 10x10	GAMMAP	-0.32	-0.40	-0.48	$V^{1/2}$	12
gain factor	KPP	48	58	68	$\mu A/V^2$	7
drain-source breakdown 0.35µm	BVDS035P	-7	< -8		V	14
saturation current 0.35µm	IDS035P	-180	-240	-300	µA/µm	15
subthreshold leakage current 0.35µm	SLEAK035P		-0.5	-2	pA/µm	17
gate oxide breakdown	BVGOXP	-7	< -8		V	18
INFORMATION PARAMETERS						
active channel length 0.35µm	LACT035P		0.31		µm	26
threshold voltage narrow channel 0.4x10	VTO04X10P		-0.90		V	6
threshold voltage small channel 0.4x0.35	VTO04X035P		-0.68		V	6
threshold voltage temperature coefficient	TCVTOP		1.8		mV/K	13
effective substrate doping	NSUBP		101		$10^{15}/cm^3$	12
effective mobility	UOP		126		cm^2/Vs	8
mobility exponent	BEXP		-1.30		-	13

3.2.2.3. MOS N-Channel High Voltage Electrical Parameters : NMOSH

PASS/FAIL PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
threshold voltage 3µm	VTO3NH	0.34	0.44	0.54	V	6
drain-source breakdown 3µm	BVDS3NH	15	19		V	14
on-resistance 3µm	RON3NH	9	13	17	kΩ µm	19
INFORMATION PARAMETERS						
saturation current 3µm	IDS3NH	160	200	240	µA/µm	15
substrate current 3µm	ISUB3NH		1.5	3	µA/µm	16

3.2.3. Sheet Resistances

3.2.3.1. NWELL - Resistor: RNWELL

PASS/FAIL PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
NWELL field sheet resistance	RNWELL	0.8	1.0	1.2	kΩ/□	20
NWELL field eff. width 1.7 µm	WNWELL	0.30	0.55	0.80	µm	20
INFORMATION PARAMETERS						
NWELL field temp. coefficient	TCNWELL		6.2		10^{-3}/K	22

Sheet Resistances (continued)

PASS/FAIL PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
POLY1 sheet resistance	RPOLY		8	15	Ω/□	20
INFORMATION PARAMETERS						
POLY1 gate sheet resistance	RGATE		8		Ω/□	20
POLY1 effective width 0.35 µm	WPOLY		0.32		µm	20
POLY1 gate effective width 0.35 µm	WGPOLY		0.35		µm	20
POLY1 temperature coefficient	TCPOLY		0.9		10^{-3}/K	22

Sheet Resistances (continued)

PASS/FAIL PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
NDIFF sheet resistance	RDIFFN	55	70	85	Ω/□	20
NDIFF effective width 0.3 µm	WDIFFN	0.25	0.40	0.55	µm	20
INFORMATION PARAMETERS						
NDIFF temperature coefficient	TCDIFFN		1.5		10^{-3}/K	22
PASS/FAIL PARAMETERS						
PDIFF sheet resistance	RDIFFP	100	130	160	Ω/□	20
PDIFF effective width 0.3 µm	WDIFFP	0.25	0.40	0.55	µm	20
INFORMATION PARAMETERS						
PDIFF temperature coefficient	TCDIFFP		1.5		10^{-3}/K	22
PASS/FAIL PARAMETERS						
MET1 sheet resistance	RMET		80	150	mΩ/□	21
INFORMATION PARAMETERS						
MET1 effective width 0.5 µm	WMET		0.5		µm	20
MET1 temperature coefficient	TCMET		3.3		10^{-3}/K	22
PASS/FAIL PARAMETERS						
MET2 sheet resistance	RMET2		80	150	mΩ/□	21
INFORMATION PARAMETERS						
MET2 effective width 0.6 µm	WMET2		0.5		µm	20
MET2 temperature coefficient	TCMET2		3.4		10^{-3}/K	22
PASS/FAIL PARAMETERS						
MET3 sheet resistance (top metal)	RMET3T		40	100	mΩ/□	21
INFORMATION PARAMETERS						
MET3 effective width 0.6 µm (top metal)	WMET3T		0.6		µm	20
MET3 temperature coefficient (top metal)	TCMET3T		3.5		10^{-3}/K	22

Please refer to section ”2.3 Current Densities” as well.

3.2.4. Contact Resistances

PASS/FAIL PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
MET1-NDIFF cont. resistance 0.4x0.4µm²	RCNTMDN		30	100	Ω/cnt	23
MET1-PDIFF cont. resistance 0.4x0.4µm²	RCNTMDP		60	150	Ω/cnt	23
MET1-POLY1 cont. resistance 0.4x0.4µm²	RCNTMP		2	10	Ω/cnt	23
VIA resistance 0.5x0.5µm²	RVIA		1.2	3	Ω/via	23
VIA2 resistance 0.5x0.5µm²	RVIA2		1.2	3	Ω/via	23

Please refer to section ”2.3 Current Densities” as well.

3.2.5. Poly Fuses

INFORMATION PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
Poly1 Resistor W/L=0.35/1.8 (non-fused)	RPFUSE0		50		Ω	46
Poly1 Resistor W/L=0.35/1.8 (fused)	RPFUSE1		1.0		MΩ	46

3.2.6. Capacitances

Capacitance values except CGOX are characterisation parameters (refer to section "1 Introduction").

3.2.6.1. MOS Varactor: CVAR

INFORMATION PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
quality factor W/L=317/0.6 , 2.4 GHz	QMAX		72			43
tuning range	gamma		57		%	44

Capacitances (continued)

PASS/FAIL PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
POLY1 - DIFF (gate oxide)						
POLY1 - DIFF area	CGOX	4.26	4.54	4.86	fF/µm²	2
INFORMATION PARAMETERS						
POLY1 - DIFF (gate oxide)						
GATE – NDIFF overlap	CGSDON	0.105	0.120	0.134	fF/µm	26
GATE - PDIFF overlap	CGSDOP	0.075	0.086	0.096	fF/µm	26
GATE - BULK overlap	CGBO	0.10	0.11	0.12	fF/µm	27
POLY1 – LDD (gate oxide)						
GATE – LDD overlap	CGSDLN	0.115	0.131	0.147	fF/µm	26
GATE – LDD overlap	CGSDLP	0.095	0.108	0.121	fF/µm	26
POLY1 – WELL (field oxide)						
POLY1 – WELL (field oxide) area	CPFOX	0.108	0.119	0.133	fF/µm²	24
POLY1 – WELL (field oxide) perimeter	CPFOXF	0.051	0.053	0.055	fF/µm	25
MET1 - WELL (active region)						
MET1 - WELL (active region) area	CMDIFF	0.020	0.023	0.025	fF/µm²	24
MET1 - WELL (active region) perimeter	CMDIFFF	0.039	0.041	0.043	fF/µm	25
MET1 – WELL (field region)						
MET1 – WELL (field region) area	CMFOX	0.023	0.029	0.038	fF/µm²	24
MET1 – WELL (field region) perimeter	CMFOXF	0.040	0.044	0.049	fF/µm	25
MET1 - POLY1 (active region), MET1 - POLY2 (active region, without POLY1)						
MET1 - POLY1 (active region) area	CMPDIFF	0.025	0.027	0.031	fF/µm²	24
MET1 - POLY1 (active region) perimeter	CMPDIFFF	0.041	0.044	0.046	fF/µm	25
MET1 - POLY1 (field region), MET1 - POLY2 (field region, without POLY1)						
MET1 - POLY1 (field region) area	CMPFOX	0.040	0.055	0.090	fF/µm²	24
MET1 - POLY1 (field region) perimeter	CMPFOXF	0.047	0.053	0.063	fF/µm	25

Capacitances (continued)

MET2 – WELL						
MET2 – WELL area	CM2FOX	0.010	0.012	0.017	fF/µm²	24
MET2 – WELL perimeter	CM2FOXF	0.032	0.035	0.039	fF/µm	25
MET2 - POLY1, MET2 – POLY2 (without POLY1)						
MET2 - POLY1 area	CM2P	0.012	0.016	0.023	fF/µm²	24
MET2 - POLY1 perimeter	CM2PF	0.034	0.037	0.042	fF/µm	25
MET2 - MET1						
MET2 - MET1 area	CM2M	0.026	0.036	0.059	fF/µm²	24
MET2 - MET1 perimeter	CM2MF	0.042	0.048	0.056	fF/µm	25
MET3T – WELL						
MET3T – WELL area	CM3TFOX	0.006	0.008	0.011	fF/µm²	24
MET3T – WELL perimeter	CM3TFOXF	0.029	0.032	0.036	fF/µm	25
MET3T – POLY1, MET3 – POLY2 (without POLY1)						
MET3T – POLY1 area	CM3TP	0.007	0.009	0.013	fF/µm²	24
MET3T – POLY1 perimeter	CM3TPF	0.030	0.034	0.038	fF/µm	25
MET3T - MET1						
MET3T - MET1 area	CM3TM	0.010	0.014	0.020	fF/µm²	24
MET3T - MET1 perimeter	CM3TMF	0.034	0.039	0.044	fF/µm	25
MET3T - MET2						
MET3T - MET2 area	CM3TM2	0.026	0.036	0.059	fF/µm²	24
MET3T - MET2 perimeter	CM3TM2F	0.046	0.053	0.062	fF/µm	25
COUPLING CAPACITANCES						
POLY1 - POLY1 coupling	CP1P1		0.039		fF/µm	28
MET1 - MET1 coupling	CM1M1		0.087		fF/µm	28
MET2 - MET2 coupling	CM2M2		0.084		fF/µm	28
MET3T - MET3T coupling (top metal)	CM3TM3T		0.108		fF/µm	28

3.2.7. Diode Parameters

Diode parameters except breakdown voltages and Zener diode parameters are characterisation parameters (refer to section "Introduction").

NDIFF - PWELL

PASS/FAIL PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
breakdown voltage	BVN	7	9		V	30
INFORMATION PARAMETERS						
area junction capacitance	CJN		0.94		fF/µm²	29
area grading coefficient	MJN		0.34		-	29
junction potential	PBN		0.69		V	29
sidewall junction capacitance	CJSWN		0.25		fF/µm	29
sidewall grading coefficient	MJSWN		0.23		-	29
area leakage current	JSN		0.01		fA/µm²	31
sidewall leakage current	JSSWN		0.13		fA/µm	31

PDIFF - NWELL

PASS/FAIL PARAMETERS						
breakdown voltage	BVP	-7	-9		V	30
INFORMATION PARAMETERS						
area junction capacitance	CJP		1.36		fF/µm²	29
area grading coefficient	MJP		0.56		-	29
junction potential	PBP		1.02		V	29
sidewall junction capacitance	CJSWP		0.32		fF/µm	29
sidewall grading coefficient	MJSWP		0.43		-	29
area leakage current	JSP		0.09		fA/µm²	31
sidewall leakage current	JSSWP		0.61		fA/µm	31

Diode Parameters (continued)

NWELL – PWELL/PSUB

PASS/FAIL PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
breakdown voltage	BVNW	25	34		V	30
INFORMATION PARAMETERS						
area junction capacitance	CJNW		0.08		fF/µm²	29
area grading coefficient	MJNW		0.39		-	29
junction potential	PBNW		0.53		V	29
sidewall junction capacitance	CJSWNW		0.51		fF/µm	29
sidewall grading coefficient	MJSWNW		0.27		-	29
area leakage current	JSNW		0.06		fA/µm²	31
sidewall leakage current	JSSWNW		0.27		fA/µm	31

3.2.8. Zener Diode Parameters:ZD2SM24

INFORMATION PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
Zener breakdown voltage 50µA	VZENER50	1.5	2.5	3.5	V	32
Zener breakdown voltage 2µA	VZENER2		1.5		V	32
Zener diode leakage current	LZENER		0.3		µA	33
zapped Zener diode voltage	VZAP			tbd	V	34
Zener breakdown voltage 50µA temperature coefficient	TCVZENER50		tbd		mV/K	35

3.2.9. Bipolar Parameters

3.2.9.1. Lateral PNP Bipolar Transistor: LAT2

PASS/FAIL PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
lateral PNP base-emitter voltage 2x2µm²@1µA	VBEL	600	650	700	mV	37
lateral PNP current gain 2x2µm²@1µA	BETAL1	30	140	380	-	37
INFORMATION PARAMETERS						
lateral PNP current gain 2x2µm²@10µA	BETAL10		30		-	37
lateral PNP Early voltage 2x2µm²	VAFL	8	15		V	38
lateral PNP - parasitic vertical current gain 2x2µm²	BETAVL		14		-	37

3.2.9.2. Vertical PNP Bipolar Transistor: VERT10

PASS/FAIL PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
vertical PNP base-emitter voltage 10x10µm²	VBEV	650	680	710	mV	36
vertical PNP current gain 10x10µm²@10µA	BETAV	2.0	5.0	8	-	36
INFORMATION PARAMETERS						
vertical PNP Early voltage 10x10µm²	VAFV		>80		V	38
vertical PNP half gain current 10x10µm²	ICHBV		120		µA	36

3.3. Poly1-Poly2 Capacitor Module Parameters

Please refer to "1.2 Process Family" for information on the processes where this module is implemented.

3.3.1. Structural and Geometrical Parameters

PASS/FAIL PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
CPOLY equivalent oxide thickness	TPOX	37	41	45	nm	2
poly2 thickness	TPOLY2	185	200	215	nm	1
INFORMATION PARAMETERS						
poly2-well oxide thickness (field region)	TP2FOX	285	335	385	nm	1
metal1-poly2 oxide thickness (field region, with poly1)	TMP2FOXP1	600	700	800	nm	1

3.3.2. Poly2 Sheet Resistance: RPOLY2

PASS/FAIL PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
POLY2 sheet resistance	RPOLY2	40	50	60	Ω/□	20
POLY2 effective width 0.65 µm	WPOLY2	0.30	0.40	0.50	µm	20
INFORMATION PARAMETERS						
POLY2 sheet resistance temp. coefficient	TCPOLY2		0.7		10^{-3}/K	22

3.3.3. Contact Resistance

PASS/FAIL PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
MET1-POLY2 cont. resistance 0.4x0.4µm²	RCNTMP2		20	40	Ω/cnt	23

3.3.4. POLY1-POLY2 Capacitor: CPOLY

PASS/FAIL PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
CPOLY area capacitance	CPOX	0.78	0.86	0.96	fF/µm²	2
CPOLY breakdown voltage high voltage on POLY2	BVPOX	15	30		V	39
CPOLY breakdown voltage high voltage on POLY1	BVPOXH	15	30		V	39
INFORMATION PARAMETERS						
CPOLY perimeter capacitance	CPOXF	0.083	0.086	0.089	fF/µm	25
CPOLY linearity	VCPOX		85		ppm/V	40
CPOLY leakage current	LKCPOX			1	aA/µm²	42
CPOLY temperature coefficient	TCPOX		0.03		10^{-3}/K	41

The values specified above are only valid for the poly1-poly2 module.

3.3.5. Capacitances

INFORMATION PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
POLY2 - WELL (field region)						
POLY2 - WELL (field region) area	CP2FOX	0.095	0.105	0.117	fF/µm²	24
POLY2 - WELL (field region) perimeter	CP2FOXF	0.049	0.050	0.052	fF/µm	25
MET1 - POLY2 (field region, with POLY1)						
MET1 - POLY2 area	CMP2FOXP1	0.044	0.051	0.059	fF/µm²	24
MET1 - POLY2 perimeter	CMP2FOXP1F	0.048	0.052	0.055	fF/µm	25
MET2 - POLY2 (field region, with POLY1)						
MET2 - POLY2 area	CM2P2FOXP1	0.013	0.017	0.027	fF/µm²	24
MET2 - POLY2 perimeter	CM2P2FOXP1F	0.035	0.039	0.044	fF/µm	25
MET3T – POLY2 (field region, with POLY1)						
MET3T(top metal) – POLY2 area	CM3TP2FOXP1	0.007	0.010	0.014	fF/µm²	24
MET3T(top metal) – POLY2 perimeter	CM3TP2FOXP1F	0.031	0.035	0.036	fF/µm	25
COUPLING CAPACITANCES						
POLY2 - POLY2 coupling	CP2P2		0.022		fF/µm	28

3.4. Metal2-MetalC Capacitor Module Parameters

Please refer to "1.2.Process Family" for information on the processes where this module is implemented.

3.4.1. Structural and Geometrical Parameters

PASS/FAIL PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
CMIM area capacitance	CMIM	1.00	1.25	1.50	fF/µm²	2
CMIM equivalent oxide thickness	TMIM	23	29	34	nm	2
CMIM breakdown voltage high voltage on MET2	BVM2	10	40		V	18
CMIM breakdown voltage high voltage on METC	BVMC	10	40		V	18
INFORMATION PARAMETERS						
CMIM perimeter capacitance	CMIMF	0.110	0.114	0.117	fF/µm	25
CMIM linearity	VCMIM			110	ppm/V	40
CMIM leakage current	LKCMIM		10		aA/µm²	42
CMIM temperature coefficient	TCMIM		30		10^{-3}/K	41
METC thickness	TMETC		150		nm	3
METC sheet resistance	RMETC		7.5		Ω/□	21
METC effective width 4µm	WMETC		4.2		µm	20

3.4.2. Contact Resistance

PASS/FAIL PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
MET3-METC via resistance 0.5x0.5µm²	RVIA2C		1.5	6	Ω/via	23

3.5. 5 Volt Module Parameters

Please refer to "1.2 Process Family" for information on the processes where this module is implemented.
The transistors NMOSM, PMOSM and NMOSMH use mid-oxide as gate insulator.

3.5.1. Structural and Geometrical Parameters

PASS/FAIL PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
Mid-oxide thickness	TMOX	14	15	16	nm	2

3.5.2. MOS Electrical Parameters

3.5.2.1. MOS 5V N-Channel Electrical Parameters : NMOSM

PASS/FAIL PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
threshold voltage long channel 10x10	VTO10X10NM	0.60	0.70	0.80	V	6
threshold voltage short channel 10x0.5	VTO10X05NM	0.60	0.70	0.80	V	6
threshold voltage short channel 10x0.5 (measured in linear region)	VT_5N3	0.69	0.79	0.89	V	6
effective channel length 0.5µm	LEFF05NM	0.35	0.45	0.55	µm	10
effective channel width 0.4µm	WEFF04NM	0.20	0.35	0.50	µm	11
body factor long channel 10x10	GAMMANM	0.90	1.05	1.20	$V^{1/2}$	12
gain factor	KPNM	80	100	120	µA/V²	7
drain-source breakdown 0.5µm	BVDS05NM	7	> 9		V	14
saturation current 0.5µm	IDS05NM	400	470	540	µA/µm	15
substrate current 0.5µm	ISUB05NM		2	5	µA/µm	16
subthreshold leakage current 0.5µm	SLEAK05NM		0.1	1	pA/µm	17
gate oxide breakdown	BVGOXNM	12	> 15		V	18

MOS 5V N-Channel Electrical Parameters: NMOSM (continued)

INFORMATION PARAMETERS						
active channel length 0.5µm	LACT05NM		0.30		µm	26
threshold voltage narrow channel 0.4x10	VTO04X10NM		0.63		V	6
threshold voltage small channel 0.4x0.5	VTO04X05NM		0.63		V	6
threshold voltage temperature coefficient	TCVTONM		-1.5		mV/K	13
effective substrate doping	NSUBNM		173		$10^{15}/cm^3$	12
effective mobility	UONM		435		cm^2/Vs	8
mobility exponent	BEXNM		-1.76		-	13

3.5.2.2. MOS 5V P-Channel Electrical Parameters: PMOSM

Negative values are considered as absolute values for their Min/Max limits.

PASS/FAIL PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
threshold voltage long channel 10x10	VTO10X10PM	-0.85	-0.97	-1.09	V	6
threshold voltage short channel 10x0.5	VTO10X05PM	-0.85	-0.97	-1.09	V	6
threshold voltage short channel 10x0.5 (measured in linear region)	VT_5P3	-0.88	-1.03	-1.18	V	6
effective channel length 0.5µm	LEFF05PM	0.58	0.68	0.78	µm	10
effective channel width 0.4µm	WEFF04PM	0.20	0.35	0.50	µm	11
body factor long channel 10x10	GAMMAPM	-0.53	-0.63	-0.73	$V^{½}$	12
gain factor	KPPM	25	31	37	$µA/V^2$	7
drain-source breakdown 0.5µm	BVDS05PM	-7	< -8		V	14
saturation current 0.5µm	IDS05PM	-150	-200	-250	µA/µm	15
subthreshold leakage current 0.5µm	SLEAK05PM		-0.01	-0.1	pA/µm	17
gate oxide breakdown	BVGOXPM	-12	< -15		V	18

MOS 5V P-Channel Electrical Parameters: PMOSM (continued)

INFORMATION PARAMETERS						
active channel length 0.5µm	LACT05PM		0.45		µm	26
threshold voltage narrow channel 0.4x10	VTO04X10PM		-1.25		V	6
threshold voltage small channel 0.4x0.5	VTO04X05PM		-0.90		V	6
threshold voltage temperature coefficient	TCVTOPM		2.0		mV/K	13
effective substrate doping	NSUBPM		63		$10^{15}/cm^3$	12
effective mobility	UOPM		135		cm^2/Vs	8
mobility exponent	BEXPM		-1.3		-	13

3.5.2.3. MOS N-Channel High Voltage Electrical Parameters : NMOSMH

PASS/FAIL PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
threshold voltage 3µm	VTO3NMH	0.55	0.67	0.79	V	6
drain-source breakdown 3µm	BVDS3NMH	17	22		V	14
on-resistance 3µm	RON3NMH	7	11	15	kΩ µm	19
INFORMATION PARAMETERS						
saturation current 3µm	IDS3NMH	180	220	260	µA/µm	15
substrate current 3µm	ISUB3NMH		1	5	µA/µm	16

3.5.3. Capacitances

PASS/FAIL PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
POLY1 - DIFF (mid-oxide) area	CMOX	2.16	2.30	2.46	$fF/µm^2$	2
INFORMATION PARAMETERS						
POLY1 - DIFF (mid-oxide)						
GATE – NDIFF overlap	CGSDOMN	0.095	0.108	0.121	fF/µm	26
GATE - PDIFF overlap	CGSDOMP	0.080	0.091	0.102	fF/µm	26
GATE - BULK overlap	CGBOM	0.10	0.11	0.12	fF/µm	27
POLY1 – LDD (mid oxide)						
GATE – LDD overlap	CGSDLMN	0.200	0.227	0.254	fF/µm	26
GATE – LDD overlap	CGSDLMP	0.052	0.060	0.068	fF/µm	26

3.6. Metal 4 Module Parameters

Please refer to "1.2 Process Family" for information on the processes where this module is implemented.

Important application note:
Implementation of metal 4 module results in changing of several CMOS core module parameters. Parameters of this section override corresponding parameters of section “CMOS Core Module Parameters”.

3.6.1. Structural and Geometrical Parameters

PASS/FAIL PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
metal3 thickness	TMET3	540	640	740	nm	3
metal3-metal4 metal oxide thickness	TIMD3	620	1000	1380	nm	1
metal4 thickness	TMET4	775	925	1075	nm	3

3.6.2. Sheet Resistances

PASS/FAIL PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
MET3 sheet resistance	RMET3		80	150	mΩ/☐	21
MET4 sheet resistance	RMET4		40	100	mΩ/☐	21
VIA3 resistance 0.5x0.5µm²	RVIA3		1.2	3	Ω/via	23
INFORMATION PARAMETERS						
MET3 effective width 0.6 µm	WMET3		0.5		µm	20
MET4 effective width 0.6 µm	WMET4		0.6		µm	20
MET3 temperature coefficient	TCMET3		3.4		10^{-3}/K	22
MET4 temperature coefficient	TCMET4		3.5		10^{-3}/K	22

3.6.3. Capacitances

INFORMATION PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
MET3 – WELL						
MET3 – WELL area	CM3FOX	0.006	0.008	0.011	fF/µm²	24
MET3 – WELL perimeter	CM3FOXF	0.028	0.031	0.034	fF/µm	25
MET3 - POLY1/POLY2						
MET3 - POLY1/POLY2 area	CM3P	0.007	0.009	0.013	fF/µm²	24
MET3 - POLY1/POLY2 perimeter	CM3PF	0.029	0.032	0.036	fF/µm	25
MET3 - MET1						
MET3 - MET1 area	CM3M	0.010	0.014	0.020	fF/µm²	24
MET3 - MET1 perimeter	CM3MF	0.033	0.036	0.041	fF/µm	25
MET3 - MET2						
MET3 - MET2 area	CM3M2	0.026	0.036	0.059	fF/µm²	24
MET3 - MET2 perimeter	CM3M2F	0.043	0.048	0.056	fF/µm	25
MET4 – WELL						
MET4 – WELL area	CM4FOX	0.005	0.006	0.008	fF/µm²	24
MET4 – WELL perimeter	CM4FOXF	0.027	0.029	0.032	fF/µm	25
MET4 - POLY1/POLY2						
MET4 - POLY1/POLY2 area	CM4P	0.005	0.006	0.009	fF/µm²	24
MET4 - POLY1/POLY2 perimeter	CM4PF	0.027	0.030	0.034	fF/µm	25
MET4 - MET1						
MET4 - MET1 area	CM4M	0.006	0.008	0.012	fF/µm²	24
MET4 - MET1 perimeter	CM4MF	0.030	0.033	0.037	fF/µm	25
MET4 - MET2						
MET4 - MET2 area	CM4M2	0.010	0.014	0.020	fF/µm²	24
MET4 - MET2 perimeter	CM4M2F	0.034	0.039	0.044	fF/µm	25

Capacitances (continued)

INFORMATION PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
MET4 – MET3						
MET4 – MET3 area	CM4M3	0.026	0.036	0.059	fF/µm²	24
MET4 – MET3 perimeter	CM4M3F	0.046	0.053	0.062	fF/µm	25
COUPLING CAPACITANCES						
MET3 – MET3 coupling	CM3M3		0.085		fF/µm	28
MET4 – MET4 coupling	CM4M4		0.109		fF/µm	28

3.7. Thick Metal Module Parameters

Please refer to Section "1.2.Process Family" for information on the processes where this module is implemented.

Important application note:
Implementation of thick metal module results in changing of several CMOS core module and metal 4 module parameters. Parameters of this section override corresponding parameters of section “3.2.CMOS Core Module Parameters” and of section “3.6 Metal 4 Module Parameters”.

3.7.1. Structural and Geometrical Parameters

PASS/FAIL PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
metal3 thickness	TMET3	540	640	740	nm	3
thick metal-metal3 oxide thickness	TIMDT	600	1000	1200	nm	1
thick metal thickness	TMETT	2000	2500	3000	nm	3
passivation thickness 1	TPROT1T	210	230	250	nm	1
passivation thickness 2	TPROT2T	500	550	600	nm	1

3.7.2. Sheet Resistances

PASS/FAIL PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
MET3 sheet resistance	RMET3		80	150	mΩ/□	21
METT sheet resistance	RMETT		15	tbd	mΩ/□	21
VIA3 resistance 0.5x0.5µm²	RVIA3T		1.2	3	Ω/via	23
INFORMATION PARAMETERS						
MET3 effective width 0.6 µm	WMET3		0.5		µm	20
MET3 temperature coefficient	TCMET3		3.4		10^{-3}/K	22
METT effective width 2.5µm	WMETT		2.5		µm	20
METT temperature coefficient	TCMETT		tbd		10^{-3}/K	22

3.7.3. Capacitances

INFORMATION PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
MET3 – WELL						
MET3 – WELL area	CM3FOXT	0.006	0.008	0.011	fF/µm²	24
MET3 – WELL perimeter	CM3FOXFT	0.030	0.032	0.036	fF/µm	25
MET3 – POLY1						
MET3 – POLY area	CM3PT	0.007	0.009	0.013	fF/µm²	24
MET3 - POLY perimeter	CM3PFT	0.031	0.033	0.038	fF/µm	25
MET3 - MET1						
MET3 - MET1 area	CM3MT	0.010	0.014	0.020	fF/µm²	24
MET3 - MET1 perimeter	CM3MFT	0.034	0.037	0.043	fF/µm	25
MET3 - MET2						
MET3 - MET2 area	CM3M2T	0.026	0.036	0.059	fF/µm²	24
MET3 - MET2 perimeter	CM3M2FT	0.044	0.049	0.057	fF/µm	25

Capacitances (continued)

INFORMATION PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
METT – WELL						
METT – WELL area	CMTFOX	0.005	0.006	0.008	fF/µm²	24
METT – WELL perimeter	CMTFOXF	0.033	0.038	0.046	fF/µm	25
METT - POLY1/POLY2						
METT - POLY area	CMTP	0.005	0.006	0.009	fF/µm²	24
METT - POLY perimeter	CMTPF	0.034	0.039	0.048	fF/µm	25
METT - MET1						
METT - MET1 area	CMTM	0.007	0.008	0.012	fF/µm²	24
METT - MET1 perimeter	CMTMF	0.037	0.043	0.054	fF/µm	25
METT - MET2						
METT - MET2 area	CMTM2	0.011	0.014	0.021	fF/µm²	24
METT - MET2 perimeter	CMTM2F	0.044	0.052	0.064	fF/µm	25
METT – MET3						
METT – MET3 area	CMTM3	0.030	0.036	0.061	fF/µm²	24
METT – MET3 perimeter	CMTM3F	0.063	0.073	0.093	fF/µm	25
COUPLING CAPACITANCES						
MET3 – MET3 coupling	CM3M3		0.085		fF/µm	28
METT – METT coupling	CMTMT		0.103		fF/µm	28

3.8. High Resistive Poly Module Parameters

Please refer to "1.2 Process Family" for information on the processes where this module is implemented.

PASS/FAIL PARAMETERS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Note**
RPOLYH sheet resistance	RPOLYH	0.9	1.2	1.5	kΩ/□	20
RPOLYH effective width 0.8 µm	WPOLYH	0.45	0.60	0.75	µm	20
MET1-RPOLYH contact resistance 0.4x0.4µm²	RCNTMPH		70	150	Ω/cnt	23
INFORMATION PARAMETERS						
RPOLYH temperature coefficient	TCPOLYH		-0.4		10^{-3}/K	22
RPOLYH voltage coefficient	VCRPOLYH		-0.8		10^{-3}/V	45
RPOLYH extrinsic sheet resistance (contact region)	RPOLYHE		150		Ω/□	20

3.9. Notes / Measurement Conditions

Note 1 **Oxide, nitride and polysilicon thickness monitoring**
is performed by optical interference or ellipsometry at large area structures within the wafer process or on monitor wafers. The parameter values describe the oxide, nitride and polysilicon thickness of fully prepared wafers.

Note 2 **Oxide capacitance / oxide thickness**
The capacitance per area COX of a large area capacitor is measured. The oxide thickness TOX is calculated from:

$$TOX = \frac{\varepsilon_0 \cdot \varepsilon_{ox}}{COX}$$

with $\varepsilon_{FOX,GOX,MOX,MIM} = 3.9$, $\varepsilon_{POX} = 4.0$, $\varepsilon_0 = 8.85.10^{-12}$ F/m

Note 3 **Metal thickness**
is monitored by resistivity on monitor wafer or by mechanical step measurement. The specified value describes the thickness of all layers which finally generate the corresponding metal layer.

Note 4 **Junction depth**
is extracted from SIMS or SRS measurements. The measurements are performed on fully processed wafers.

Note 5 **Wafer substrate resistivity and wafer thickness**
Wafer substrate resistivity and wafer thickness is given in reference to wafer supplier specification.

Note 6 **Threshold voltage VTO10X10, VTO10X035, VTO04X10, VTO04X035, VTO10X05, VTO04X05**
The linearly extrapolated threshold voltage with zero substrate bias is measured in saturation: Gate and drain are connected to one voltage source, source and bulk are connected to ground. The voltage is swept in order to find the maximum slope of the square root of the drain current as a function of the gate voltage. A linear regression is performed around this operating point:

$$\sqrt{IDS} = \sqrt{\frac{KP}{2} \cdot \frac{Weff}{Leff}} \cdot (VGS - VTO)$$

Threshold voltage VT_N3, VT_P3, VT_5N3, VT_5P3
The linearly extrapolated threshold voltage with zero substrate bias is measured in the linear region: Source and bulk are connected to ground, drain is set to VD=0.1V. The gate voltage is swept in order to find the maximum gm

$$IDS = KP \cdot \frac{Weff}{Leff} \cdot VDS \cdot \left(VGS - VTH - \frac{VDS}{2} \right)$$

The voltage sweep is positive for n-channel devices and negative for p-channel devices. The intercept with the x-axis is taken as VTO.

Note 7 **Gain factor**

KP is measured from the slope of the large transistor, where Weff / Leff ~ W/L.
The drain voltage is forced to 0.1V, source and bulk are connected to ground. The gate voltage is swept to find the maximum slope of the drain current as a function of the gate voltage. A linear regression is performed around this operating point:

$$IDS = KP \cdot \frac{Weff}{Leff} \cdot VDS \cdot (VGS - VTO - \frac{VDS}{2})$$

The voltage sweep is positive for n-channel devices and negative for p-channel devices.

Note 8 **Mobility**

The mobility UO is calculated from KP (refer to note 7) and COX (refer to note 2):

$$UO = \frac{KP}{COX}$$

Note 9 **Field threshold**

Drain is set to 3.3V. Source and bulk are connected to ground. The voltage at the gate is swept in a binary search within the voltage limits 10V ≤ VTFP(N/P) ≤ 50V until the current reaches 10nA/µm.
The voltage sweep is positive for n-channel devices and negative for p-channel devices.

Note 10 **Effective channel length**

The effective channel length is calculated from two wide transistors of different length.

Drain is set to V_d = 0.1V, source and bulk are connected to ground.

The gate Voltage V_{gm} is determined, where the slope of drain current I_d on gate voltage V_g is a maximum. Then the gate is forced to $V_g = V_{gm}$, $(V_{gm} + V_{cc})/2$, and V_{cc} respectively, and the drain current I_{ds} is recorded.

From a fit to

$$I_{DS} = \frac{\eta(V_{GS} - V_{TH}) \cdot V_{DS}}{1 + \alpha(V_{GS} - V_{TH})}$$

the parameters η, α and V_{th} are obtained. The effective channel length L_{eff} and source-drain resistance R_{DS} is calculated by

$$L_{eff} = \frac{\eta_L (L_S - L_L)}{\eta_L - \eta_S} \qquad R_{DS} = \frac{\alpha_L - \alpha_S}{\eta_L - \eta_S}$$

with subscript L and S denoting the long and short transistor respectively.

Note 11 **Effective channel width**

The effective gain factor KP' = KP · Weff / Leff is measured for a W - array of long transistors according to threshold voltage measurement (refer to note 7 and note 6). The width reduction DW = W - Weff is calculated from the x-intercept of the linear regression:

$$KP' = \frac{KP}{Leff} \cdot (W - DW)$$

Note 12 **Body effect and effective substrate doping concentration**

The threshold voltages VTH as a function of substrate bias voltage from 0 to -2V (+2V for p-channel) are extracted by linear regressions as described in note 6 . The body factor GAMMA is then extracted from the slope of VTH as a function of $(2\cdot \text{PHI} - \text{VBS})^{1/2}$ by another linear regression:

$$\text{VTH} = \text{VTO} + \text{GAMMA} \cdot \left(\sqrt{2 \cdot PHI - VBS} - \sqrt{2 \cdot \text{PHI}} \right)$$

The effective substrate doping concentration NSUB is calculated from GAMMA and COX (refer to note 2):

$$\text{GAMMA} = \frac{\sqrt{2 \cdot \varepsilon_0 \cdot \varepsilon_{si} \cdot q \cdot \text{NSUB}}}{\text{COX}} \qquad \varepsilon_{SI} = 11.7$$

The surface potential PHI is a function of the doping concentration NSUB and the intrinsic carrier concentration NI

$$\text{PHI} = \frac{kT}{q} \ln\left(\frac{\text{NSUB}}{\text{NI}} \right)$$

PHI is recalculated using the extracted value of NSUB. This updated value of PHI is then used again in the extraction of GAMMA and NSUB in an iterative procedure.

Note 13 **Temperature coefficient of threshold voltage**
Temperature exponent of mobility

The threshold voltage VTO (refer to note 6) and the gain factor KP (refer to note 7) are measured as a function of the temperature T from 25°C to 125°C. The temperature coefficient of the threshold voltage TCV and the temperature exponent of the mobility BEX are calculated from the slope of the following linear regressions:

$$\text{VTO}(\text{T}) = \text{VTO}(\text{T0}) + \text{TCV} \cdot (\text{T} - \text{T0})$$

$$\ln[\text{KP}(\text{T})] = \ln[\text{KP}(\text{T0})] + \text{BEX} \cdot [\ln(\text{T}) - \ln(\text{T0})]$$

Note 14 **Drain-source breakdown voltage**

Gate, source and bulk are connected to ground. The drain voltage is swept until the current reaches 10 nA/µm (referred to transistor width) at the breakdown voltage BVDS or until the voltage limit is reached.

Note 15 **Saturation current**

Source and bulk are connected to ground. Gate and drain are set to

gate: 3.3V	drain: 3.3V	for NMOS
gate: -3.3V	drain: -3.3V	for PMOS
gate: 5V	drain: 5V	for NMOSM
gate: -5V	drain: -5V	for PMOSM
gate: 3.3V	drain: 15V	for NMOSH
gate: 5V	drain: 15V	for NMOSMH

The transistor saturation current IDS is measured at the drain. IDS is specified per drawn transistor width.

Note 16 **Substrate current**

Source and bulk are forced to 0V. The drain is set to

3.3V	for NMOS
5V	for NMOSM
15V	for NMOSH and NMOSMH

The gate voltage is swept within the allowed operating range in order to find the maximum substrate current ISUB. ISUB is specified per drawn transistor width.

Note 17 **Sub-threshold leakage current**

The drain is set to 3.3V, source and bulk are connected to ground. The drain current as a function of VGS is measured within the sub-threshold region. A linear regression of log(ID)=f(VGS) is performed. The intercept with log(ID)-axis is taken as SLEAK. SLEAK is specified per drawn transistor width.

Note 18 **Gate oxide breakdown**

The voltage at the capacitor is swept until a current of 10 nA/µm² is reached at the breakdown voltage BV.

Note 19 **On-resistance**

The drain is set to 0.2V, the gate is forced to 3.3V for NMOSH and 5V for NMOSMH, source and bulk are connected to ground. The drain current IDS is measured. The drain resistance RON = 0.2V/IDS is calculated. RON is referred to drawn transistor width.

Note 20 **Sheet resistance and effective resistor width**

A voltage VRES is applied to one terminal. The second terminal is connected to ground. In case of diffusion or well resistor measurements substrate or well is also connected to ground. The current IRES is measured at the first terminal. The measurements are performed for an array of widths W of long resistors (Leff ~ L). The sheet resistance per square R is calculated from the slope and the width reduction DW = W - Weff is calculated from the x-intercept of the linear regression:

$$\frac{\mathrm{IRES}}{\mathrm{VRES}} = \frac{1}{\mathrm{R} \cdot \mathrm{Leff}} \cdot \left(\mathrm{W} - \mathrm{DW} \right)$$

Note 21 **Metal sheet resistance**

A minimum width metal line (width Wmin and length L) over most critical topography is measured and the resistance RMET is calculated by dividing the total resistor value RM by the number of drawn squares:

RMET = RM / (L / Wmin)

Note 22 **Temperature coefficient of sheet resistance**

The sheet resistance R (refer to note 20 and 21) is measured as a function of the temperature T from 25°C to 125°C. The temperature coefficient of the resistance TCR is calculated from the slope of the following linear regression:

$$\frac{\mathrm{R(T)}}{\mathrm{R(T0)}} = 1 + \mathrm{TCR} \cdot \left(\mathrm{T} - \mathrm{T0} \right)$$

Note 23 **Contact resistances**

The contact resistances RCNTMDN, RCNTMDP, RCNTMP and RCNTMP2 are measured on single contacts. The contact resistances RVIA, RVIA2, RVIA3 and RVIA2C are calculated from the resistance of a long contact string divided by the number of contacts.

Note 24 **Area capacitance**

The dielectric thickness TOX is measured optically (refer to note 1). The capacitance per area COX of a large area capacitor is calculated from:

$$\mathrm{COX} = \frac{\varepsilon 0 \cdot \varepsilon \mathrm{ox}}{\mathrm{TOX}}$$

with

ε_{ox} = 3.9 … TFOX, TPROT1

ε_{ox} = 4.0 … TILDFOX, TILDDIFF, TPOX

ε_{ox} = 4.1 … TIMD1, TIMD2, TIMD3

ε_{ox} = 7.9 … TPROT2

$\varepsilon_0 = 8.85 \cdot 10^{-12}$ F/m

Note 25 **Fringing capacitance**

The fringing capacitance per length (one edge) of a single minimum width interconnect line is calculated with the FEM simulator SCAP (Institute for Microelectronics, University Vienna). Adjacent structures reduce this value.

Note 26 **Active channel length and MOS overlap capacitance to source/drain**

The bias dependent lightly doped source/drain MOS overlap capacitance CGSDL and the bias independent non LDD MOS overlap capacitance CGSDO per width (one edge) is extracted from gate to source/drain capacitance $C_{Gate\text{-}SD}$ measurements of long perimeter gate structures (W/L >> 1).

$$\left(C_{\text{Gate-SD}}\right)\Big|_{\text{VGS=VFB}} - \left(C_{\text{Gate-SD}}\right)\Big|_{\text{Accumulation}} = 2 \cdot W \cdot L_{ov} \cdot C_{OX'} \cdot \frac{\gamma_{ov}}{\gamma_{ov} + \sqrt{2 \cdot \Phi_t}}$$

$$\gamma_{ov} = \frac{\sqrt{2 \cdot q \cdot N_{LDD} \varepsilon_0 \varepsilon_{Si}}}{C_{OX'}}$$

$\gamma_{ov(NMOS)}$ =3.326 $V^{-1/2}$ $\gamma_{ov\,(PMOS)}$=1.159 $V^{-1/2}$

$\gamma_{ov\,(NMOSM)}$ =2.229 $V^{-1/2}$ $\gamma_{ov\,(PMOSM)}$=2.301 $V^{-1/2}$

$$C_{GSDL} = C_{OX'} \cdot L_{OV}$$

$$C_{GSDO} = \frac{1}{2}\left(C_{\text{Gate-SD}}\right)\Big|_{\text{Accumulation}}$$

$$L_{ACTIVE} = L - 2 \cdot L_{ov}$$

Note 27 **MOS overlap capacitance to bulk**

The MOS overlap capacitance per length (both edges) is calculated from:

$$CGBO = 2 \cdot \left(WD \cdot CPFOX + CPFOXF \right)$$

The results are in conformity with experimental capacitance measurements of long perimeter gate structures (W/L <<1).

Note 28 **Coupling capacitance**

The coupling capacitance per length of adjacent metal or poly lines with minimum spacing and minimum width is calculated by using the FEM simulator SCAP (Institute for Microelectronics, University Vienna).
Note, that in case of adjacent lines the fringing capacitance (refer to note 25) is reduced by about 80% (of the coupling capacitance, if the coupling capacitance is less than the fringing capacitance).

Note 29 **Junction capacitances**

The junction capacitances C of an array of diodes with different area to perimeter ratios are measured as a function of the reverse bias voltage V. The junction capacitance per drawn area CJ, the junction capacitance per drawn perimeter CJSW, the junction potential PB, the area junction grading coefficient MJ and the sidewall junction grading coefficient MJSW are then extracted from:

$$C = \frac{W \cdot L \cdot CJ}{\left(1 + \frac{V}{PB}\right)^{MJ}} + \frac{2 \cdot (W + L) \cdot CJSW}{\left(1 + \frac{V}{PB}\right)^{MJSW}}$$

Note 30 **Diode breakdown voltage**

The diode reverse voltage is swept until the diode reverse current reaches 10 nA/µm² at the breakdown voltage BV.
Note: The well to substrate breakdown is dominated by the diffusion to substrate breakdown if the well enclosure of the diffusion is not sufficient.

Note 31 **Diode leakage**

Leakage currents IS of a large area diode (W=L) and of a long perimeter diode (W<<L) are measured at 3.3 V reverse bias voltage. The leakage current density per drawn area JS and the leakage current density per drawn perimeter JSSW are calculated from

$$IS = JS \cdot W \cdot L + JSSW \cdot \left(2 \cdot W + 2 \cdot L \right)$$

Note 32 **Zener diode breakdown voltage**

The diode reverse voltage is swept until the diode reverse current reaches 50 µA (2 µA) at the breakdown voltage VZENER.

Note 33 **Zener diode reverse leakage**

The Zener diode reverse leakage current LZENER is measured at 1 V reverse bias voltage.

Note 34 **Zapped Zener diode voltage**

The Zener diode is zapped according to the zapping conditions specified in doc. 9991070. The reverse voltage VZAP of the zapped Zener diode is measured at 50 µA reverse current.

Note 35 **Temperature coefficient Zener diode breakdown voltage**

VZENER50 is measured as a function of temperature from 25°C to 125°C as described in note 32. TCVZENER50 is calculated from the slope of the following linear regression:

$$VZENER50(T) = VZENER50(T0) + TCVZENER50 \cdot (T-T0)$$

Note 36 **Vertical PNP**

The current gain of the CMOS vertical PNP bipolar transistor (PDIFF - NWELL - p-substrate) with the specified emitter area is measured as follows:
Base and substrate are connected to 0 V. A current IE = 10µA is forced into the emitter. The base-emitter voltage VBEV is measured. The current IB is measured at the base. The current gain BETAV is calculated:

$$BETAV = -\frac{IE}{IB} - 1$$

The emitter current is then swept to higher values until current gain is reduced to half of the value of BETA. The half gain collector current ICHB is calculated from:

$$ICHB = -IE - IB$$

Note 37 **Lateral PNP**

The current gain of the CMOS lateral PNP bipolar transistor (PDIFF - NWELL - PDIFF) with the specified emitter area is measured as follows:
Base, collector and substrate (= vertical parasitic collector) are connected to 0 V. The GATE is connected to 2V. The specified emitter current IE is forced into the emitter. The base-emitter voltage VBEL is measured. The current IB is measured at the base and the current IC is measured at the collector. The current gain BETAL is calculated from:

$$BETAL = \frac{IC}{IB}$$

The parasitic vertical current gain at IE = 1µA is calculated from:

$$BETAVL = -\frac{IE}{IB} - BETAL - 1$$

Note 38 **Early voltage**

The current IB, which has been measured for the calculation of the current gain BETA is forced into the base. The substrate is connected to 0V. The collector is connected to 0V and the gate is connected to 3.3V for the lateral transistor. The emitter voltage is swept to find the minimum slope of the emitter current as a function of the emitter voltage. The Early voltage VAF is taken from the x-intercept of a linear regression which is performed around this operating point.

Note 39 **Capacitor oxide breakdown**

The voltage at the capacitor is swept until a current of 10 nA/µm² at the breakdown voltage BV is reached.

Note 40 **Capacitance linearity**

The terminal voltage is swept from –5V to +5V and the corresponding capacitance value C is measured at f=100kHz. The linearity is calculated from:

$$VCPOX = \frac{dC}{dV} \cdot \frac{1E6}{C(0V)}$$

Note 41 **Capacitance temperature dependence**

Capacitance is measured from 0°C to 175°C and the slope TCPOX is calculated by linear regression method.

$$TCPOX = \frac{d(\Delta C)}{dT} \cdot \frac{1E6}{C(25°C)}$$

Note 42 **Capacitor leakage**

Leakage current ILEAK of a large area capacitor is measured at ±3.3V at T=125°C. The leakage current density per drawn area LKCPOX is calculated from:

$$LKCPOX = \frac{ILEAK}{A}$$

Note 43 **Varactor CVAR: quality factor QF**

The quality factor QF for 1 pF is extracted from 2 port s-parameter measurements at 2.4 GHz:

$$QF = \frac{Im|Z_1|}{Re|Z_1|}$$

Note 44 **Varactor CVAR: tuning range gamma**

The tuning range gamma for 1 pF is extracted from 2 port s-parameter measurements at 2.4 GHz:

$$gamma = \frac{C_{max} - C_{min}}{C_{max} + C_{min}} \cdot 100$$

Note 45 **Voltage coefficient RPOLYH**

The voltage coefficient of a poly resistor is measured by applying bias voltage on to the bulk substrate. The slope of RPOLYH is then calculated by linear regression method.

Note 46 **Poly Fuse Resistor**

RPFUSE is measured at a voltage of 100mV. The fusing of the resistor is done by connecting the source of the waffle transistor to ground and setting the fuse voltage to 3V. Then the gate of the waffle transistor is set to 3V for 10µs..

4. Simulation Model

4.1. Introduction

This section presents a summary of circuit simulation models for MOS transistors, CMOS compatible bipolar transistors, resistors and capacitors.

The simulation parameters are intended for use with the following circuit simulators: Spectre, Eldo, HSPICE, PSPICE, SABER, SMASH, ADS or any other simulation program which contains SPICE compatible models. Technology files for other circuit simulation tools are available on request.
All parameters and technology files can be downloaded from the technical web server: http://asic.austriamicrosystems.com.

4.2. Parameter Extraction

High precision mixed analog and digital circuit simulation requires good parameter extraction strategies and accurate models. In general, the quality of a parameter extraction procedure depends on the selection of measured data (1), on the parameter extraction program (2) and on the simulation model (3).

The Input Data
We use measured current-voltage and conductance-voltage characteristics of a matrix of element geometry under all operating conditions. The geometry and the operating points are carefully selected in order to fulfil the requirements of typical mixed analog-digital design applications.

The Parameter Extraction Program
This program contains tools for extracting and optimising the SPICE model parameters. The non-linear least-square-fit routine can optimise multiple devices with respect to multiple bias conditions in order to reduce the error between the simulated data and the measured data.

4.3. The Simulation Model

MOS Transistor Model:

We supply SPICE parameters for the BSIM3v3 model. They are applicable for analog design because of a special parameter extraction strategy which includes gm, gds and gmb fitting as well as operating points in weak inversion.
In particular, the moderate inversion region and the transition from linear to saturation region are modeled more accurately.

Bipolar Transistor Model

Two parasitic bipolar devices are inherently available for design in any CMOS technology:

1. The **vertical bipolar transistor** (VERT10) uses the substrate as the (common) collector, the well as the base and a diffusion as the emitter. We supply a set of model parameters for the standard SPICE Gummel-Poon model for a given emitter size.

2. The CMOS-compatible **lateral bipolar transistor** (LAT2) consists of a diffusion square as the emitter, a diffusion ring around it as the collector and a well as the base. Emitter and collector are separated by gate area. We supply a set of model parameters for the standard SPICE Gummel-Poon model for the fixed layout.

Well Resistor Model

Field well resistors (covered by field oxide) are available for design. Well resistors have a non-linear terminal-voltage and bulk-voltage dependence of their resistance due to the resistor-to-bulk diodes which cannot be described by the 2-terminal resistor model in SPICE. Therefore, we supply model parameters for the 3-terminal SPICE JFET model. The substrate is the gate of the JFET.

Zener Diode Model

A p-diffusion to n-diffusion in n-well Zener diode is available as a programmable element. It is modeled as a sub-circuit of four diodes and a voltage source. In addition, the model includes the parasitic n-well diode and a series resistor plus a programmable parallel resistor for zapping.

4.4. Summary of Simulation Models

Please refer to further application notes within the actual model files.
The following devices are available for design:

CORE PROCESS			
Device	**Device Name**	**Model Name**	**Model Rev.**
3.3 Volt NMOS	NMOS	modn	2.0
3.3 Volt PMOS	PMOS	modp	2.0
high voltage NMOS (gate oxide)	NMOSH	modnh	2.0
Vertical PNP bipolar transistor	VERT10	vert10	2.0
Lateral PNP bipolar transistor	LAT2	lat2	2.0
Diode NDIFF / PSUB	SUBDIODE	nd	2.0
Diode PDIFF / NWELL	WELLDIODE	pd	2.0
Diode NWELL / PSUB	NWD	nwd	2.0
Zener diode	ZD2SM24	zd2sm24	2.0
POLY1-DIFF capacitor	NGATECAP	ngatecap	2.0
MOS Varactor	CVAR	cvar	2.0
PDIFF resistor	RDIFFP, RDIFFP3	rdiffp (model R) rdiffp3 (model JFET)	2.0
NDIFF resistor	RDIFFN, RDIFFN3	rdiffn (model R) rdiffn3 (model JFET)	2.0
NWELL resistor	RNWELL	rnwell	2.0

CPOLY MODULE			
Device	**Device Name**	**Model Name**	**Model Rev.**
POLY2 resistor	RPOLY2	rpoly2	2.0
CPOLY capacitor	CPOLY	cpoly	2.0

RPOLYH MODULE			
Device	**Device Name**	**Model Name**	**Model Rev.**
POLYH resistor	RPOLYH	rpolyh	2.0

CMIM MODULE			
Device	**Device Name**	**Model Name**	**Model Rev.**
METAL2-METALC capacitor	CMIM	cmim	2.0

5 VOLT MODULE			
Device	**Device Name**	**Model Name**	**Model Rev.**
5 Volt NMOS	NMOSM	Modnm	2.0
5 Volt PMOS	PMOSM	Modpm	2.0
high voltage NMOS (mid-oxide)	NMOSMH	Modnmh	2.0

Note: The SPICE models for the devices listed in this document are intended for analog/mixed signal applications only.
For RF applications dedicated devices and corresponding models are supported.
They are defined in the RF-SPICE Modeling Document (refere ”1.3 Related Documents”).

Note: Minor changes of the simulation models might be generated due to continuous improvement of device and circuit simulation. Minor changes of models are described within the actual model data files and within the intranet austriamicrosystems AG.

4.5. Circuit Simulators and Models

The models are supported and qualified for the specified simulator revision. Previous simulator versions are also supported, for detailled questions please contact us at support@austriamicrosystems.com .

Simulator	MOS Model	
	BSIM3v3 level 53	**Monte Carlo & Matching**
Eldo	5.6	5.6
Spectre	4.4.6	4.4.6
HSPICE	2001.4 (level 49)	
Saber	4.3	-
Smash	4.3.5 (level 8)	-
Pspice	V9.1	-
Smartspice	2.0.8.C	-
Agilent - ADSsim	v2001	-

The following models are supported for all simulators mentioned above:

bipolar transistors: BJT Gummel-Poon
diodes : D level 1
resistors : R / JFET level 1
capacitors : C
Zener diode: SUBCKT
Updates of model revision:
http://asic.austriamicrosystems.com/hitkit/parameters/index.html

Updates of netlist format:
http://asic.austriamicrosystems.com/hitkit/circuit_sim/netlist_format.html

Updates of simulation parameters/download area:
http://asic.austriamicrosystems.com/download/parameters.html

4.5.1. Notes on MOS Models and MOS Simulation Parameters

We supply typical mean (TM) parameters, which have been extracted from typical wafers. Additionally, the worst case tolerances of the main parameters are given. They can be used to establish worst case parameter sets. Four predefined worst case parameter sets are available: WP=worst case power=fast NMOS & fast PMOS, WS=worst case speed=slow NMOS & slow PMOS, WO=worst case one=fast NMOS & slow PMOS, WZ=worst case zero=slow NMOS & fast PMOS. Statistical parameter sets for Monte Carlo simulations (MC) are available on request.

Please note that parameters do not vary independently:
NMOS and PMOS transistors of the same wafer should have the same TOX, XW, etc.
Even for one type of transistor, most parameters are correlated. In principle only the four parameters TOX, XL, XW and VTH0 are linearly independent and their tolerances are related to process variations. We have additionally specified the tolerances of the first-order parameters NSUB, NCH and UO although they are correlated with VTH0. On the other hand we have neglected all variations of parameters describing second order effects.
The worst case tolerances of K1 and K2 are calculated from the worst case tolerances of TOX, NSUB, NCH.

Note: The circuit simulation parameters are extracted from the complete set of model equations in order to give the best fit of the entire characteristic for all operating points. The process control parameters are extracted from simplified model equations. Hence, circuit simulation parameters may differ from their corresponding process control transistor parameters.

Note: MOS transistor models are valid only up to a frequency of 1GHz. For higher frequencies special RF-models are available and documented in the RF SPICE Models document.

Note: The high voltage transistor is only intended for use in periphery cells. It is modeled as a sub-circuit of MOS transistors and resistors in order to include the n-well drain resistor.

4.5.2. Notes on Bipolar Transistor Models and Bipolar Simulation Parameters

We supply parameters which represent the typical mean (TM) process condition. Additionally, the worst case tolerances of the main parameters are available. They can be used to establish worst case parameter sets. Three predefined worst case parameter sets are available: HS = high speed & high beta, LB = low speed & low beta, HB = low speed & high beta. Statistical parameter sets for Monte Carlo simulations (MC) are also available on request.

Note: The collector current of LAT2 (lateral PNP bipolar transistor) is a function of the gate voltage. The circuit simulation parameters are valid for a positive gate-emitter voltage VGE of about 1 V. For zero or negative gate-emitter voltages, the collector current is increased considerably by the parasitic MOS current. This effect is not included in the circuit simulation model.

Note: Lateral and vertical PNP transistor models are valid only up to a frequency of 800MHz. For higher frequencies special RF-models are available and documented in the RF SPICE Models document.

Note: The circuit simulation parameters are extracted from the complete set of model equations in order to give the best fit of the entire characteristic for all operating points. The process control parameters are extracted from simplified model equations. Hence, the circuit simulation parameters BF, IKF and VAF may differ from their corresponding process control transistor parameters BETA, ICHB and VAF.

4.5.3. Notes on Resistor Models and Resistor Simulation Parameters

Note: The model parameters of the resistor models are functions of the width and the length of the resistor. Hence, they cannot be used in standard SPICE without pre-processing. However, many SPICE-like programs (e.g. ELDO, Spectre, HSPICE, SABER) allow model parameters to contain variables for an automated parameter calculation for the selected geometry.

Model parameters for the diffusion resistors RDIFFN3 and RDIFFP3 are available. These resistors are only intended for use in periphery cells. RDIFFN3 and RDIFFP3 are modeled as 3-terminal devices in order to include the resistor-to-well/substrate diodes.

The following linear resistor is available for design:

RPOLY2
RPOLYH

The following non-linear resistor is available for design:

RNWELL

Note: RNWELL is a field n-well resistor (covered by field oxide). Device n-well resistors (covered by gate oxide) are not supported.

Note: The JFET noise model in SPICE is only valid in saturation. Therefore, it is recommended to replace n-well resistors by standard resistors for correct simulation of the thermal noise.

Note: The model is only valide up to |5V|.

4.5.4. Notes on Diode Models and Diode Simulation Parameters

Diode models are only intended for the simulation of reverse leakage current and junction capacitance. It is not recommended to use ND, PD, NWD in forward operation.
The Zener diode ZD2SM24 is available as a programmable element. ZD2SM24 must not be used as a voltage reference.

4.5.5. Notes on Capacitans Models and Capacitans Simulation Parameters

Voltage dependency (VCPOX, VCMIM) and thermal modelling (TCPOX, TCMIM) for PiP capacitor
CPOLY and MIM capacitor CMIM is applied for the following circuit simulators: Spectre and ELDO.

5. Characteristic Curves

5.1. Introduction

This section contains characteristic curves for MOS transistors, CMOS compatible bipolar transistors, well resistors and the poly1 - poly2 capacitor which have been measured on typical wafers. The circuit simulation parameters for the typical mean process condition (refer to section "4. Simulation Model") have been extracted from the same wafers.

The characteristic curves are intended for checking the correct implementation of the SPICE models and SPICE parameters in a particular simulator. In addition, the accuracy of the different models is compared and the quality of the parameter extraction is shown.

MOS Transistors

Output characteristics of several transistor geometriy for zero bulk voltage and several gate voltages are shown. The figures contain the measured and the simulated drain current for the BSIM3 version 3 model.

Note: The characteristics of all transistor geometry have been simulated with a single set of SPICE parameters.

The accuracy of the on-resistance for high VGS and the output conductance in saturation for small VGS are important requirements for typical mixed analog-digital applications. Due to a special parameter extraction strategy, the modeled characteristics are especially accurate in these operating regions. As a trade-off, the maximum error of the model occurs if both VGS and VDS are high which is a relatively non-critical operating region.

Bipolar Transistors

Gummel plots and current gain plots of vertical and lateral bipolar transistors for several collector voltages are shown. The figures contain the measured and the simulated current for the SPICE Gummel-Poon model.

Well Resistors

Resistance characteristics of several resistor geometry for several bulk voltages are shown. The figures contain the measured and the simulated resistance for the SPICE JFET model.

Poly1-Poly2 Capacitors

The linearity of the CPOLY capacitor characteristics of several temperatures is shown. The figures contain the measured and the extracted capacitances.

5.2. MOS Transistor Characteristics

5.2.1. 3.3V MOS Transistor Characteristics

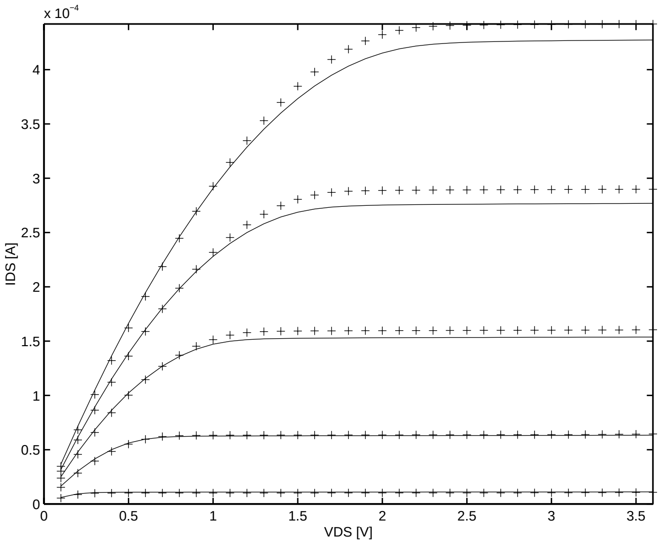


Fig.5.1 NMOS output characteristic **of a typical wafer. W/L = 10/10, VGS=0.9,1.5,2.1,2.7,3.3 V; VBS = 0 V, + = measured, — = BSIM3v3 model**

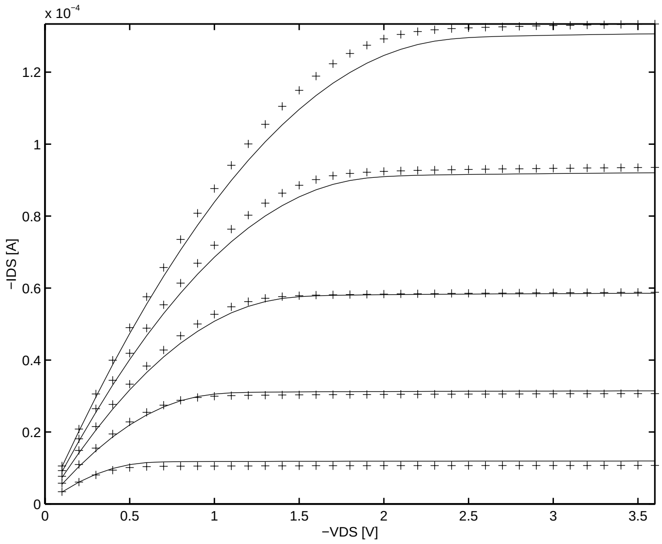


Fig. 5.2 PMOS output characteristic **of a typical wafer. W/L = 10/10, VGS=-1.4,-1.875,-2.35,-2.825,-3.3 V; VBS = 0 V, + = measured, — = BSIM3v3 model**

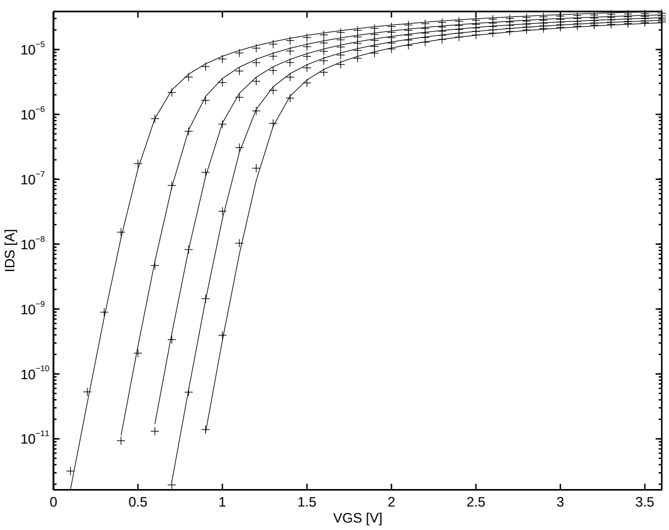


Fig. 5.3 NMOS transfer characteristic **of a typical wafer. W/L = 10/10, VBS =0,-0.9,-1.8,-2.7,-3.6 V, VDS = 0.1 V + = measured, — = BSIM3v3 model**

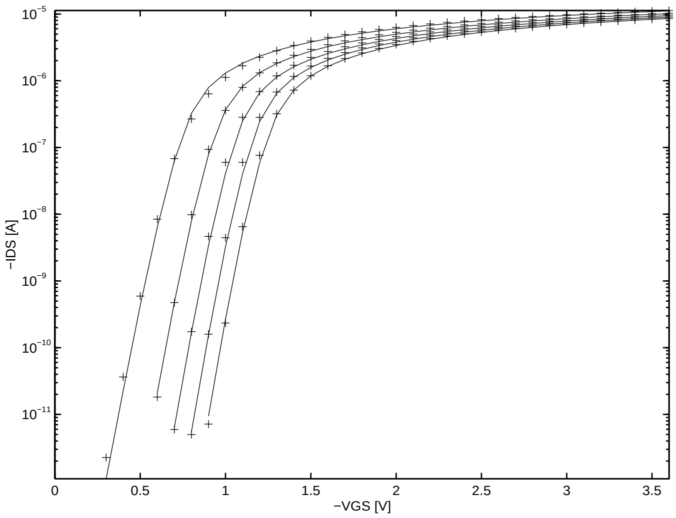


Fig. 5.4 PMOS transfer characteristic **of a typical wafer. W/L = 10/10, VBS =0,0.9,1.8,2.7,3.6 V, VDS = -0.1 V + = measured, — = BSIM3v3 model**

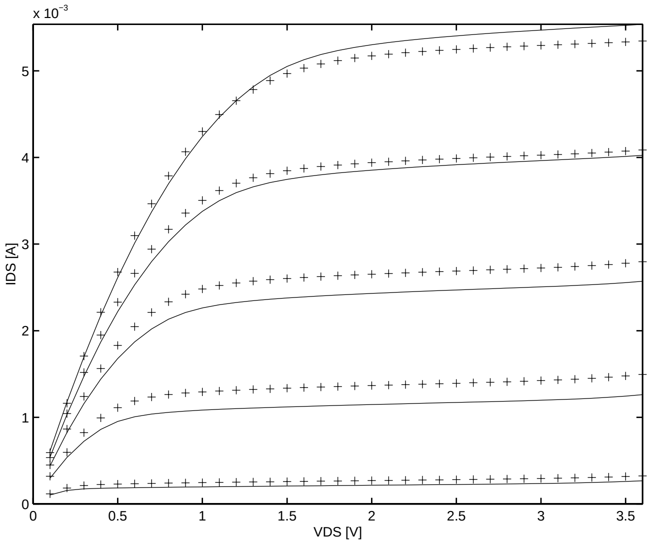


Fig. 5.5 NMOS output characteristic **of a typical wafer. W/L = 10/0.35, VGS=0.9,1.5,2.1,2.7,3.3 V; VBS = 0 V, + = measured, — = BSIM3v3 model**

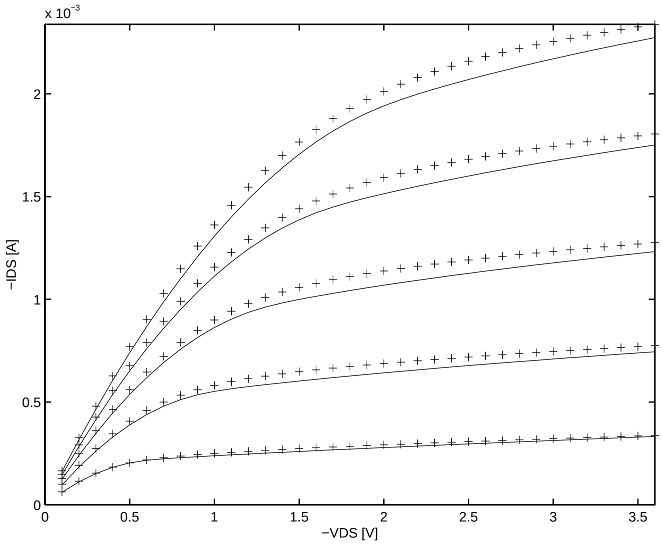


Fig. 5.6 PMOS output characteristic **of a typical wafer. W/L = 10/0.35, VGS=-1.4,-1.875,-2.35,-2.825,-3.3 V; VBS = 0 V, + = measured, — = BSIM3v3 model**

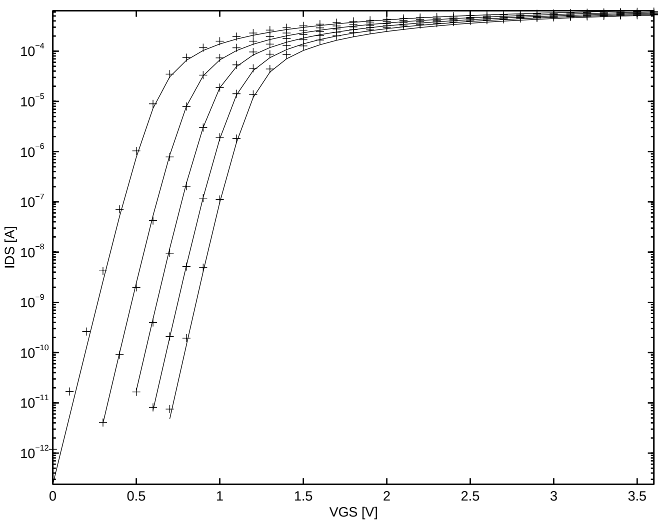


Fig. 5.7 NMOS transfer characteristic **of a typical wafer. W/L = 10/0.35, VBS =0,-0.9,-1.8,-2.7,-3.6 V, VDS = 0.1 V + = measured, — = BSIM3v3 model**

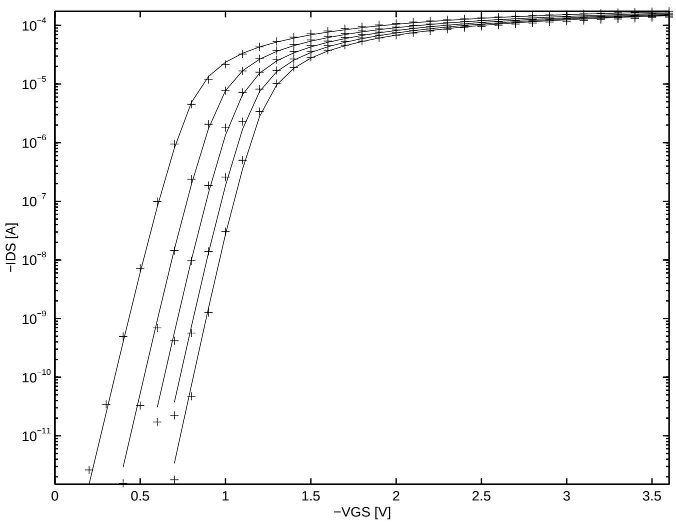


Fig. 5.8 PMOS transfer characteristic **of a typical wafer. W/L = 10/0.35, VBS =0,0.9,1.8,2.7,3.6 V, VDS = -0.1 V + = measured, — = BSIM3v3 model**

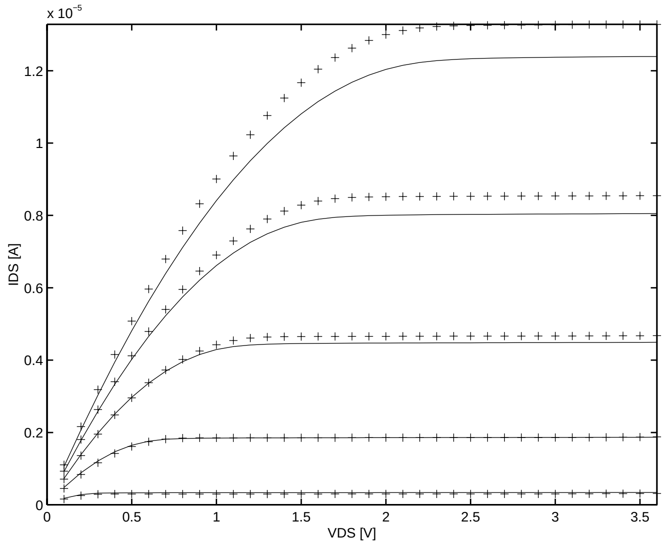


Fig. 5.9 NMOS output characteristic **of a typical wafer. W/L = 0.4/10,**

VGS=0.9,1.5,2.1,2.7,3.3 V; VBS = 0 V,

+ = measured, –– = BSIM3v3 model

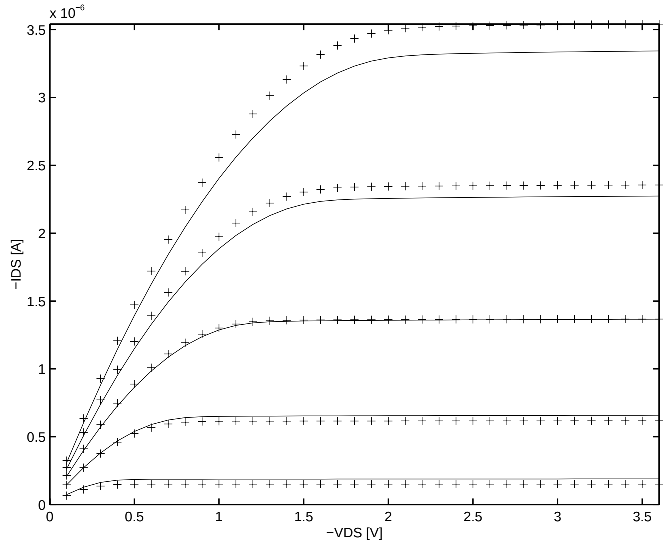


Fig. 5.10 PMOS output characteristic **of a typical wafer. W/L = 0.4/10,**

VGS=-1.4,-1.875,-2.35,-2.825,-3.3 V; VBS = 0 V,

+ = measured, –– = BSIM3v3 model

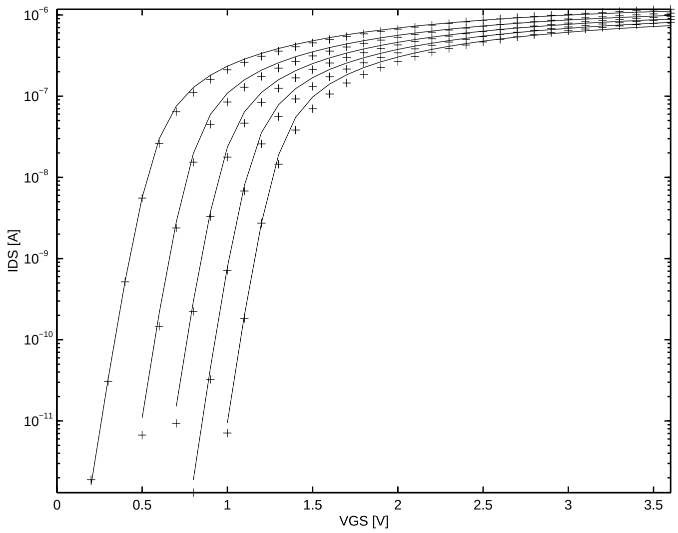


Fig. 5.11 NMOS transfer characteristic **of a typical wafer. W/L = 0.4/10,**

VBS =0,-0.9,-1.8,-2.7,-3.6 V, VDS = 0.1 V

+ = measured, –– = BSIM3v3 model

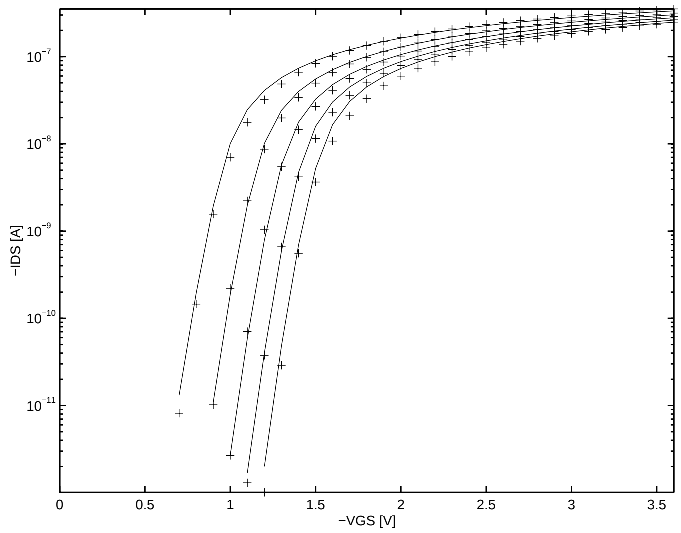


Fig. 5.12 PMOS transfer characteristic **of a typical wafer. W/L = 0.4/10,**

VBS =0,0.9,1.8,2.7,3.6 V, VDS = -0.1 V

+ = measured, –– = BSIM3v3 model

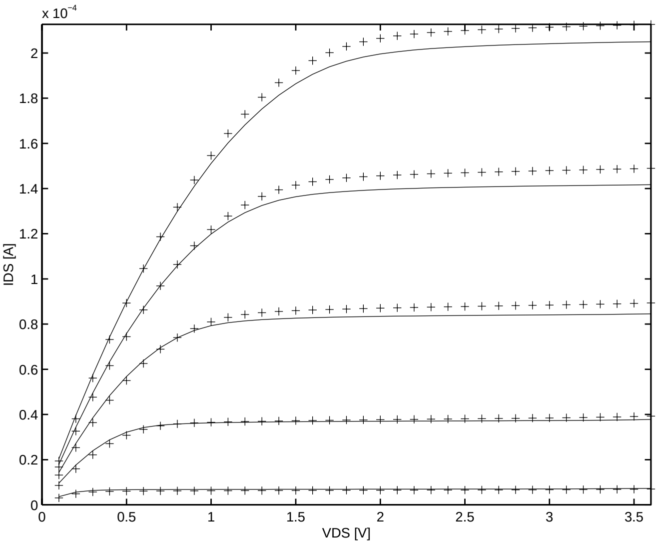


Fig. 5.13 NMOS output characteristic **of a typical wafer. W/L = 0.8/1.0, VGS=0.9,1.5,2.1,2.7,3.3 V; VBS = 0 V, + = measured, — = BSIM3v3 model**

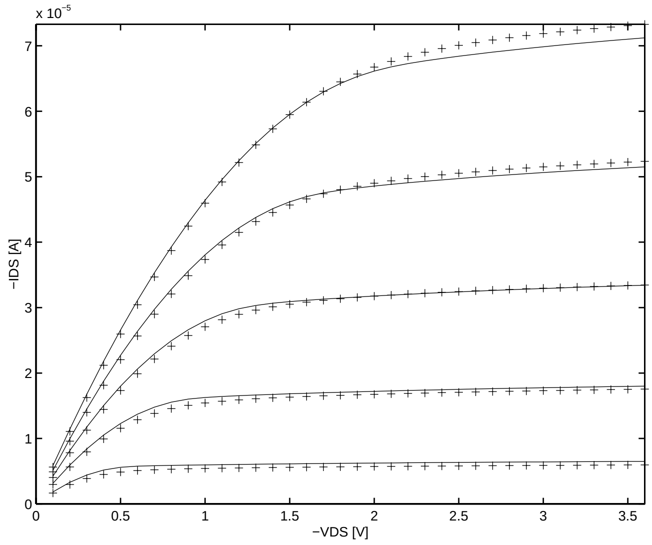


Fig. 5.14 PMOS transfer characteristic **of a typical wafer. W/L = 0.8/1.0, VBS =0,0.9,1.8,2.7,3.6 V, VDS = -0.1 V + = measured, — = BSIM3v3 model**

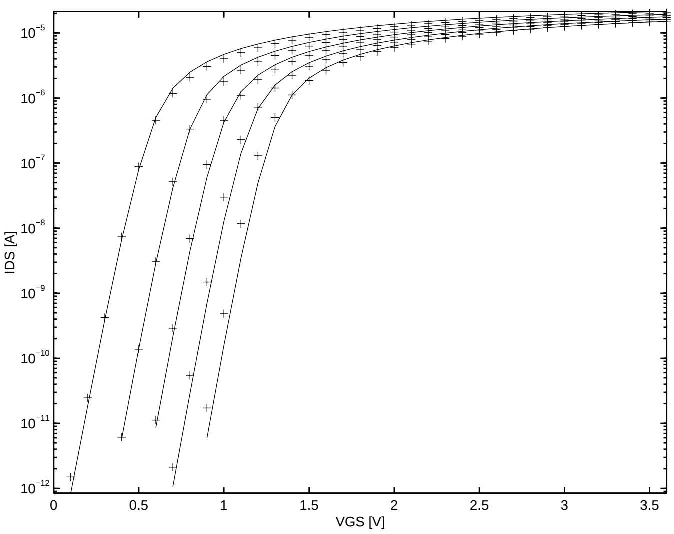


Fig. 5.15 NMOS transfer characteristic **of a typical wafer. W/L = 0.8/1.0, VBS =0,-0.9,-1.8,-2.7,-3.6 V, VDS = 0.1 V + = measured, — = BSIM3v3 model**

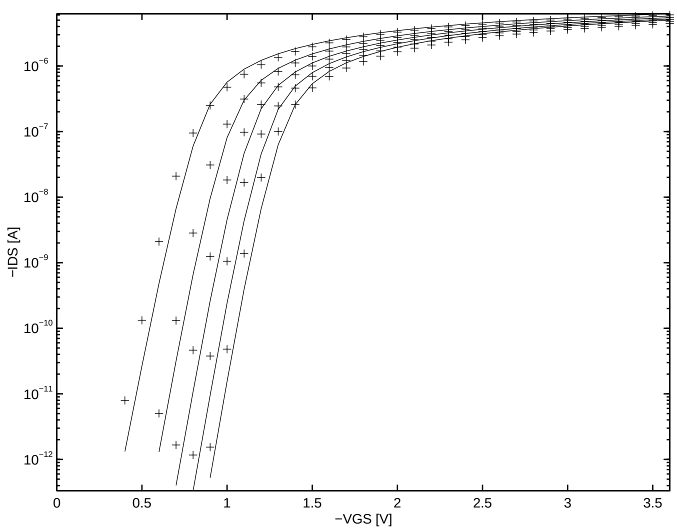


Fig. 5.16 PMOS output characteristic **of a typical wafer. W/L = 0.8/1.0, VGS=-1.4,-1.875,-2.35,-2.825,-3.3 V; VBS = 0 V, + = measured, — = BSIM3v3 model**

5.2.2. 3.3V HV-MOS Transistor Characteristics

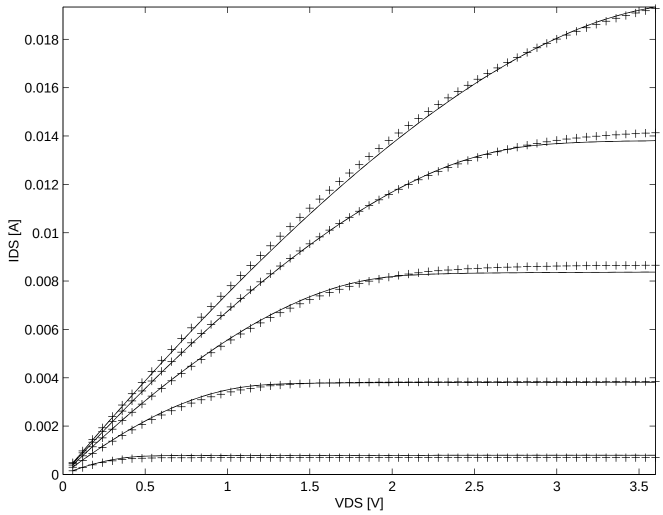


Fig. 5.17 NMOSH output characteristic **of a typical wafer. W/L = 40/3,**

VGS = 0.9,1.5,2.1,2.7,3.3 V, VBS = 0 V

+ = measured, — = BSIM3v3 model

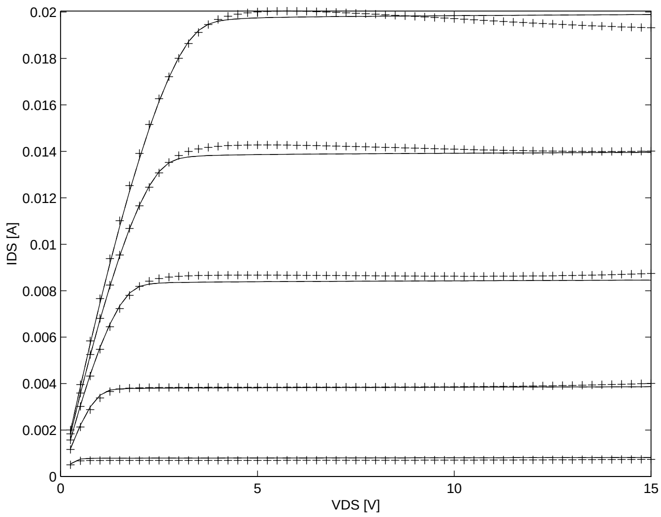


Fig. 5.18 NMOSH output characteristic **of a typical wafer. W/L = 40/3,**

VGS = 0.9,1.5,2.1,2.7,3.3 V, VBS = 0 V

+ = measured, — = BSIM3v3 model

5.2.3. 5V MOS Transistor Characteristics

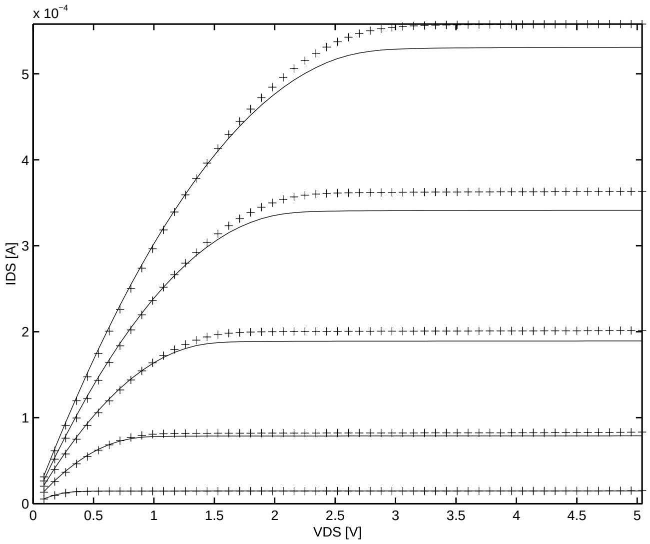


Fig. 5.19 NMOSM output characteristic **of a typical wafer. W/L = 10/10,**
VGS = 1.4,2.3,3.2,4.1,5 V, VBS = 0 V
+ = measured, — = BSIM3v3 model

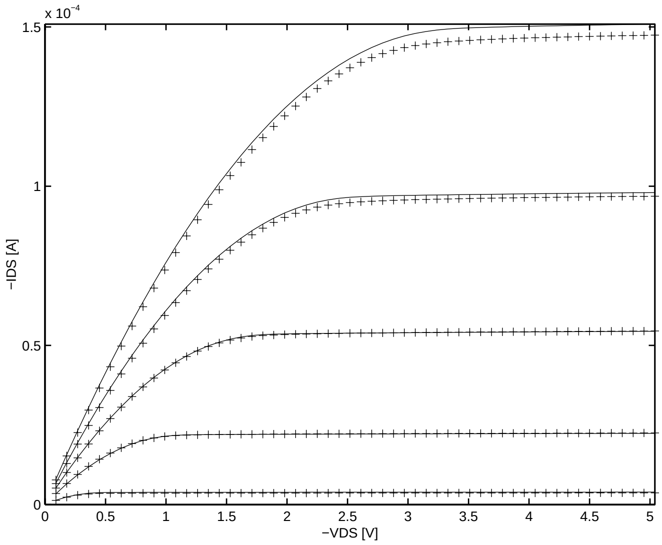


Fig. 5.20 PMOSM output characteristic **of a typical wafer. W/L = 10/10,**
VGS = -1.4,-2.3,-3.2,-4.1,-5 V, VBS = 0 V
+ = measured, — = BSIM3v3 model

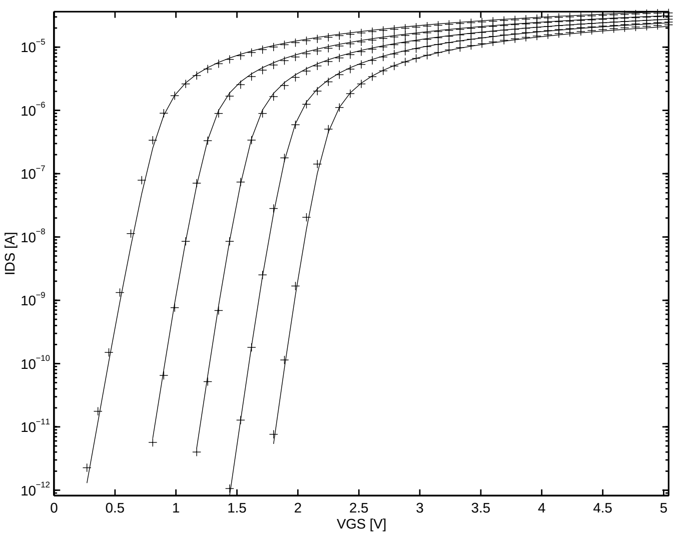


Fig. 5.21 NMOSM transfer characteristic **of a typical wafer. W/L = 10/10,**
VBS =-1,-2,-3,-4 V, VDS = 0.1 V
+ = measured, — = BSIM3v3 model

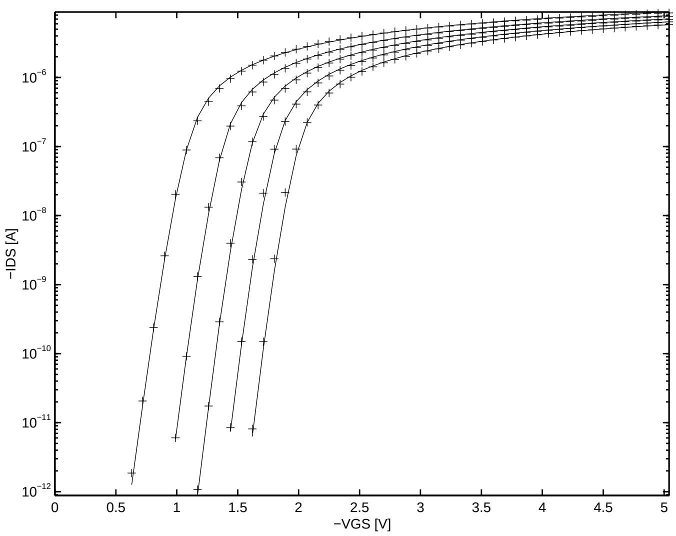


Fig. 5.22 PMOSM transfer characteristic **of a typical wafer. W/L = 10/10,**
VBS =1,2,3,4 V, VDS =-0.1 V
+ = measured, — = BSIM3v3 model

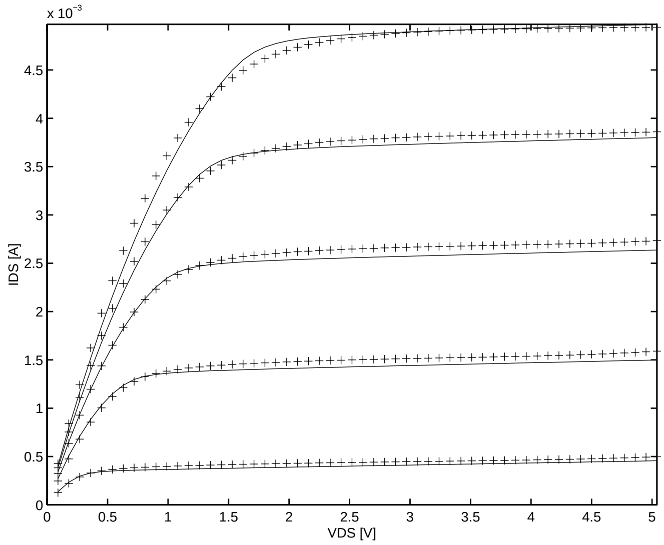


Fig. 5.23 NMOSM output characteristic **of a typical wafer. W/L = 10/0.5, VGS = 1.4,2.3,3.2,4.1,5 V, VBS = 0 V**

+ = measured, — = BSIM3v3 model

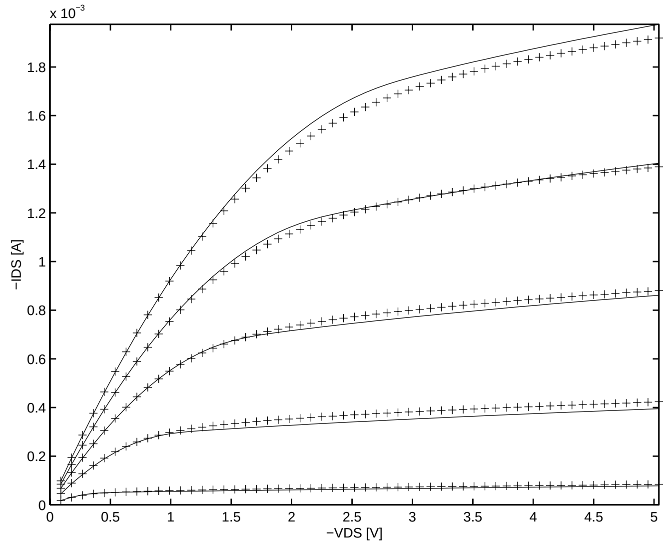


Fig. 5.24 PMOSM output characteristic **of a typical wafer. W/L = 10/0.5, VGS = -1.4,-2.3,-3.2,-4.1,-5 V, VBS = 0 V**

+ = measured, — = BSIM3v3 model

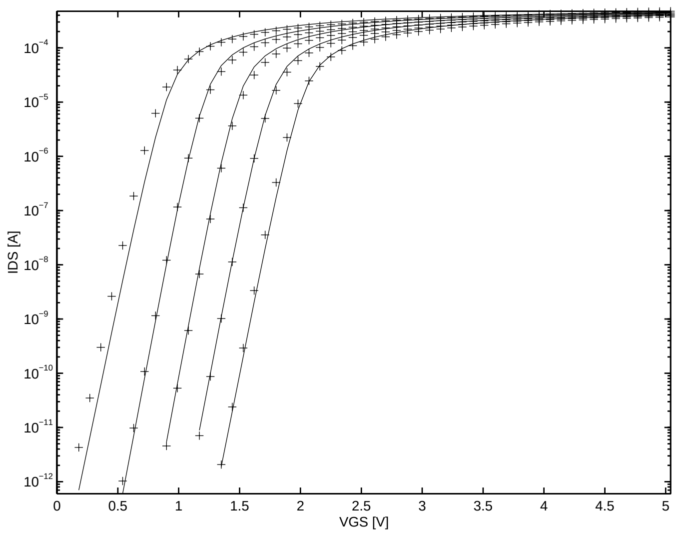


Fig. 5.25 NMOSM transfer characteristic **of a typical wafer. W/L = 10/0.5, VBS =-1,-2,-3,-4 V, VDS = 0.1 V**

+ = measured, — = BSIM3v3 model

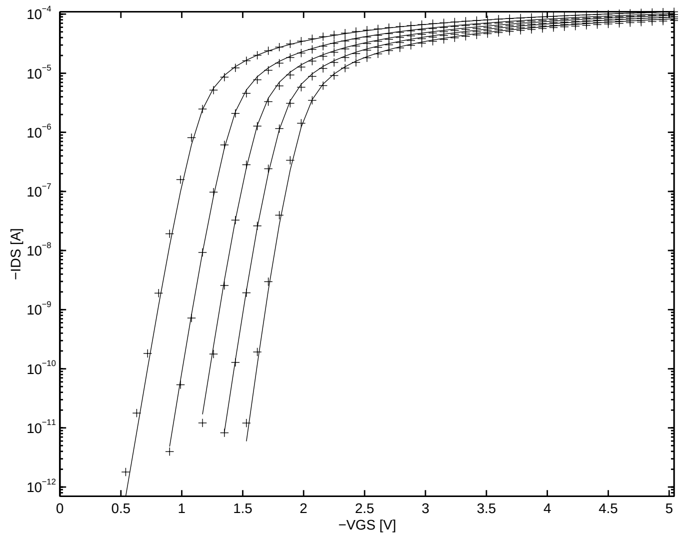


Fig. 5.26 PMOSM transfer characteristic **of a typical wafer. W/L = 10/0.5, VBS =1,2,3,4 V, VDS =-0.1 V**

+ = measured, — = BSIM3v3 model

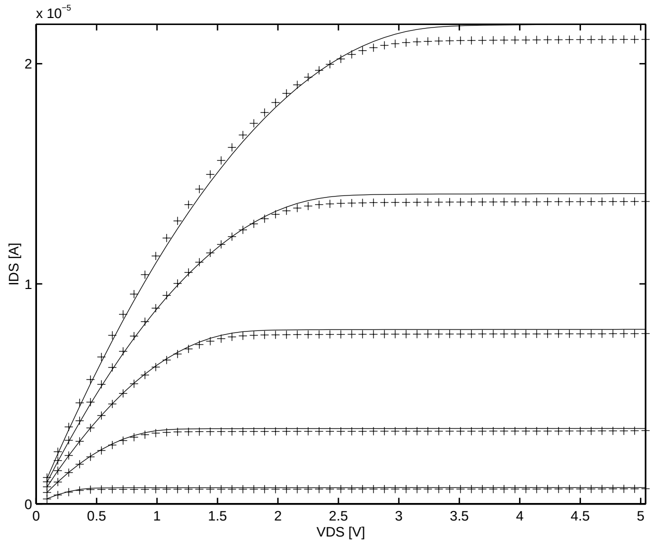


Fig. 5.27 NMOSM output characteristic **of a typical wafer. W/L = 0.4/10,**

VGS = 1.4,2.3,3.2,4.1,5 V, VBS = 0 V

+ = measured, — = BSIM3v3 model

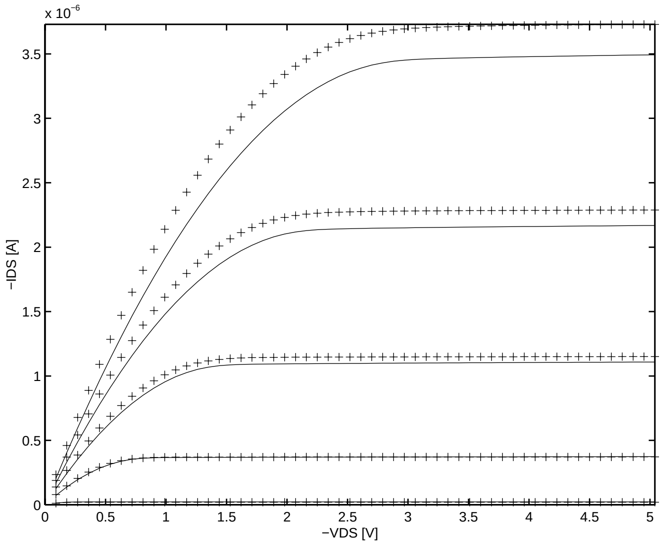


Fig. 5.28 PMOSM output characteristic **of a typical wafer. W/L = 0.4/10,**

VGS = -1.4,-2.3,-3.2,-4.1,-5 V, VBS = 0 V

+ = measured, — = BSIM3v3 model

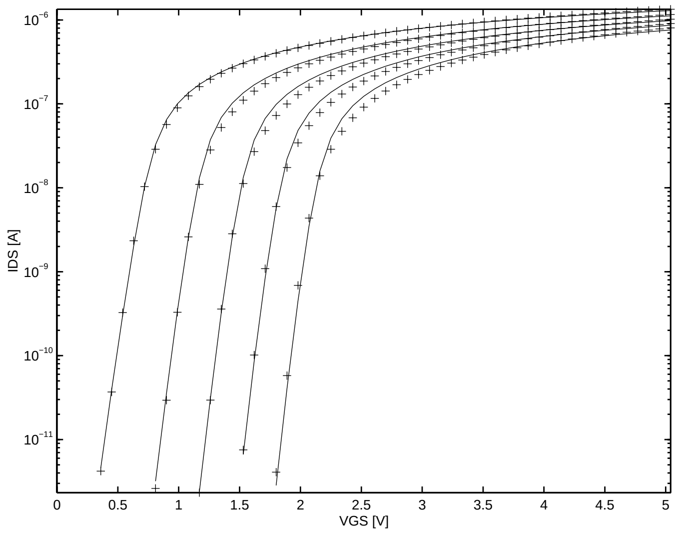


Fig. 5.29 NMOSM transfer characteristic **of a typical wafer. W/L = 0.4/10,**

VBS =-1,-2,-3,-4 V, VDS = 0.1 V

+ = measured, — = BSIM3v3 model

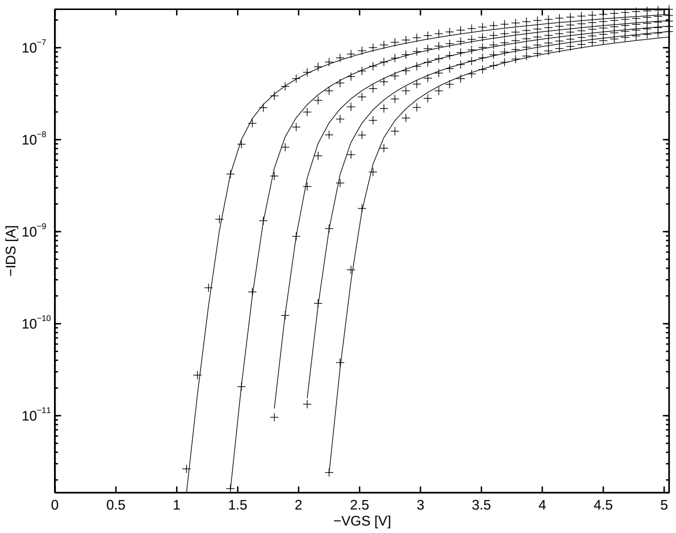


Fig. 5.30 PMOSM transfer characteristic **of a typical wafer. W/L = 0.4/10,**

VBS =1,2,3,4 V, VDS =-0.1 V

+ = measured, — = BSIM3v3 model

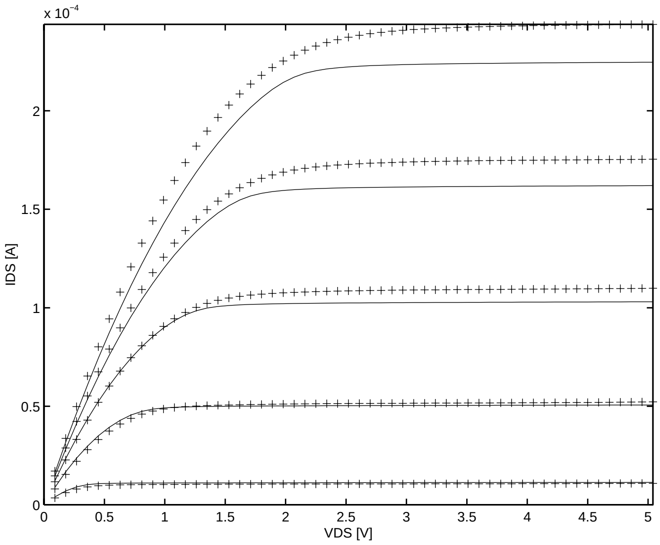


Fig. 5.31 NMOSM output characteristic **of a typical wafer. W/L = 0.8/1.0, VGS = 1.4,2.3,3.2,4.1,5 V, VBS = 0 V**

+ = measured, — = BSIM3v3 model

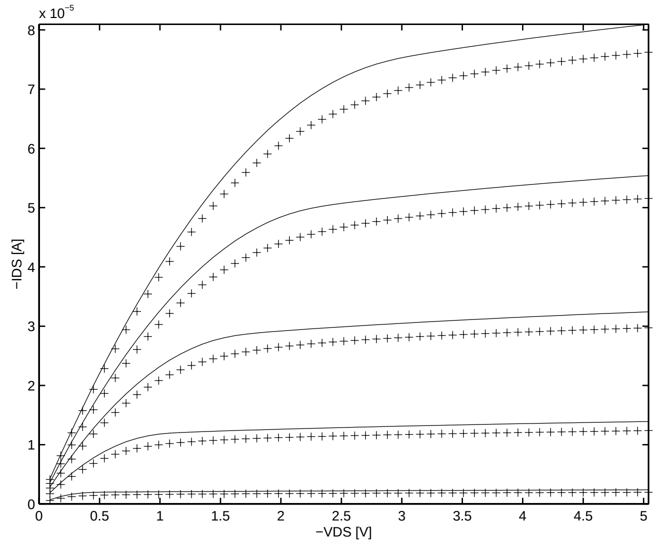


Fig. 5.32 PMOSM output characteristic **of a typical wafer. W/L = 0.8/1.0, VGS = -1.4,-2.3,-3.2,-4.1,-5 V, VBS = 0 V**

+ = measured, — = BSIM3v3 model

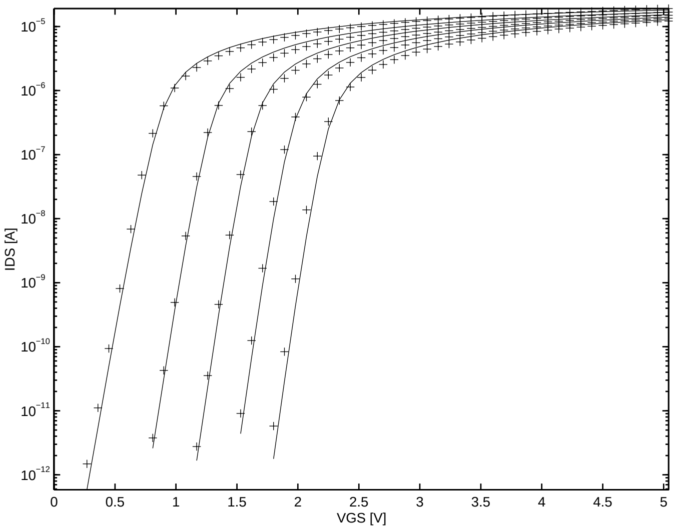


Fig. 5.33 NMOSM transfer characteristic **of a typical wafer. W/L = 0.8/1.0, VBS =-1,-2,-3,-4 V, VDS = 0.1 V**

+ = measured, — = BSIM3v3 model

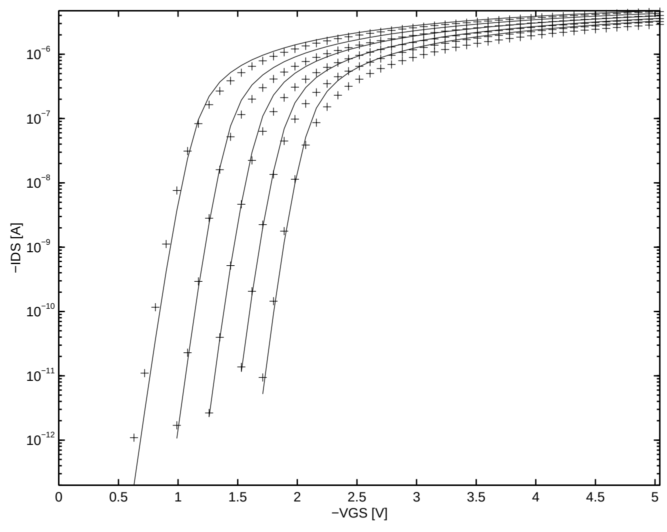


Fig. 5.34 PMOSM transfer characteristic **of a typical wafer. W/L = 0.8/1.0, VBS =1,2,3,4 V, VDS =-0.1 V**

+ = measured, — = BSIM3v3 model

5.2.4. 5V HV-MOS Transistor Characteristics

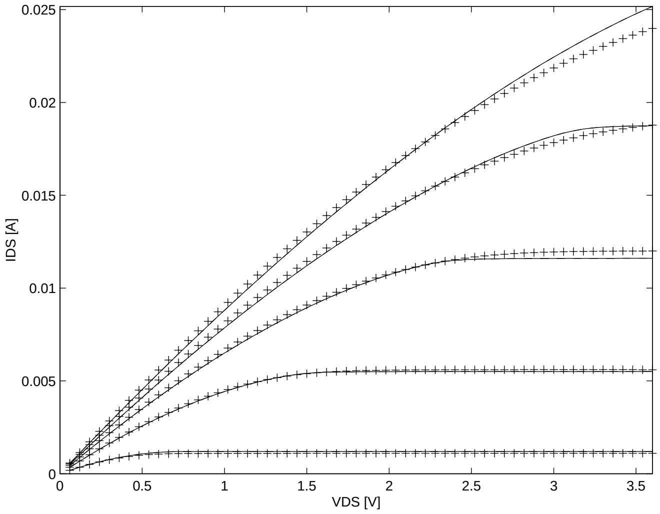


Fig. 5.35 NMOSMH output characteristic **of a typical wafer. W/L = 40/3, VGS = 1.4,2.4,3.4,4.4,5.4 V, VBS = 0 V**
+ = measured, — = BSIM3v3 model

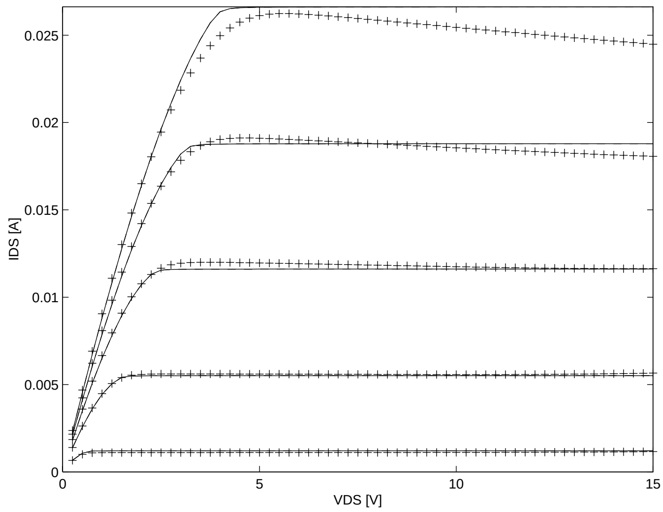


Fig. 5.36 NMOSMH output characteristic **of a typical wafer. W/L = 40/3, VGS = 1.4,2.4,3.4,4.4,5.4 V, VBS = 0 V**
+ = measured, — = BSIM3v3 model

5.3. Bipolar Transistor Characteristics

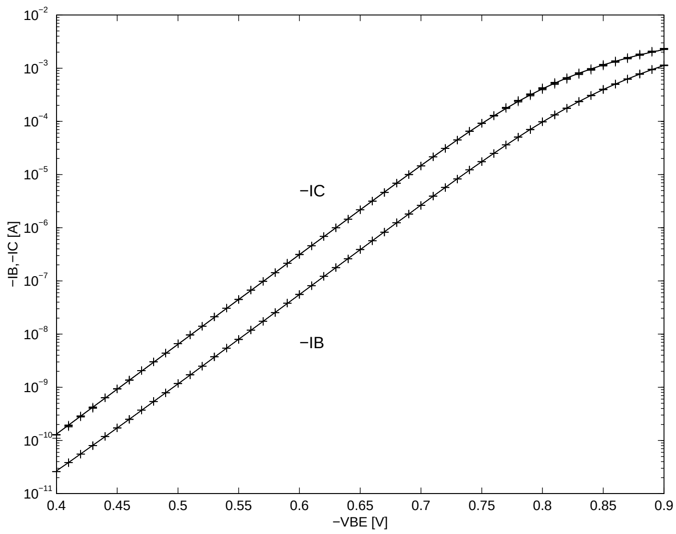


Fig. 5.37 Gummel plot of vertical PNP bipolar transistor (VERT10) for a typical wafer.

VBC = 0,0.5,1,1.5,2 V, + = measured, — = SPICE model

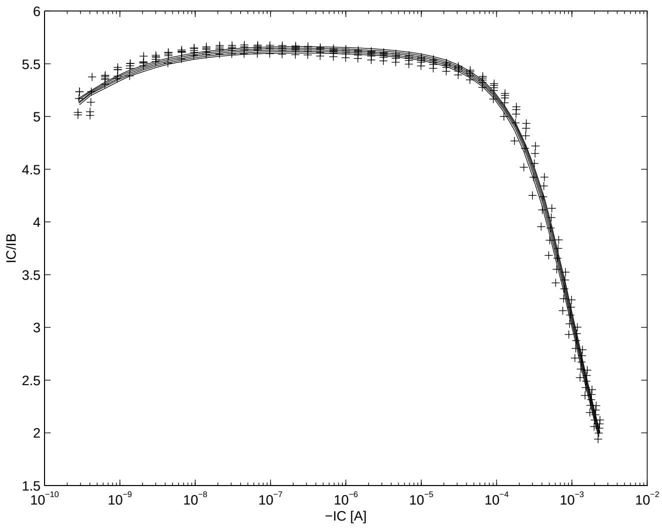


Fig. 5.38 Current gain of vertical PNP bipolar transistor (VERT10) for a typical wafer.

VBC = 0,0.5,1,1.5,2 V, + = measured, — = SPICE model

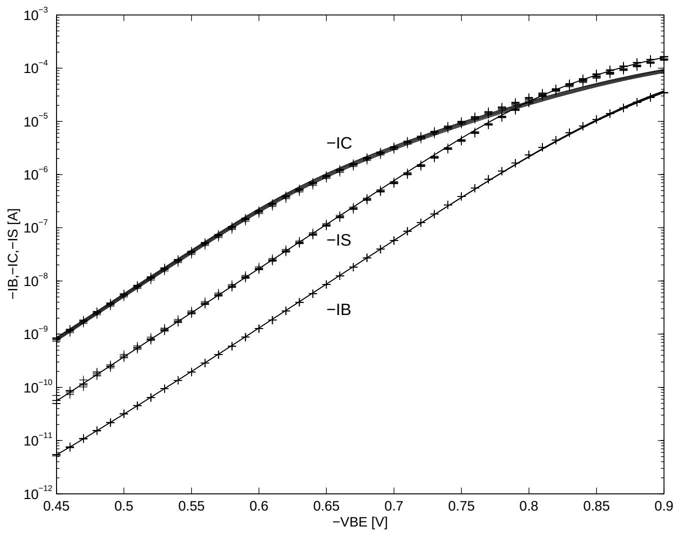


Fig. 5.39 Gummel plot of lateral PNP bipolar transistor (LAT2) for a typical wafer.

VBC = 0,0.5,1,1.5,2 V, + = measured, — = SPICE model

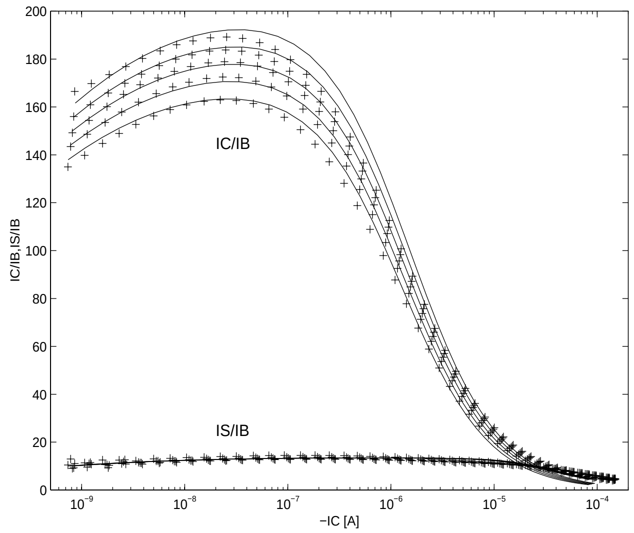


Fig. 5.40 Current gain of lateral PNP bipolar transistor (LAT2) for a typical wafer.

VBC = 0,0.5,1,1.5,2 V, + = measured, — = SPICE model

5.4. Well Resistor Characteristics

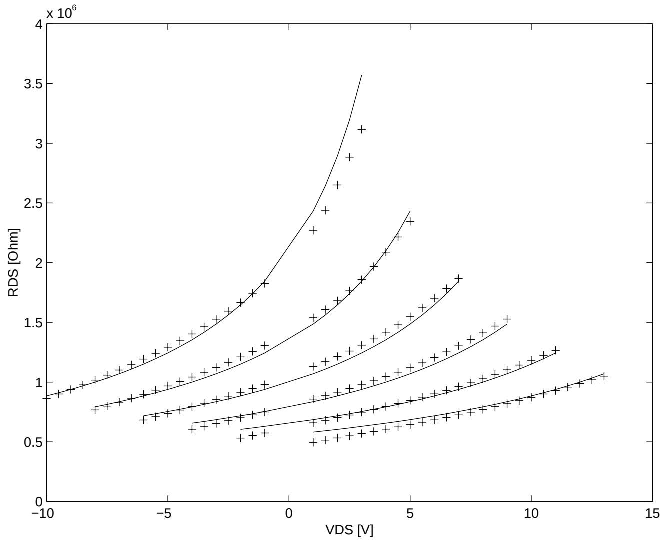


Fig. 5.41 N-well resistor characteristic **of a typical wafer. W/L = 1.7/200, -VBS = 0,2,4,6,8,10 V, + = measured, — = SPICE JFET model**

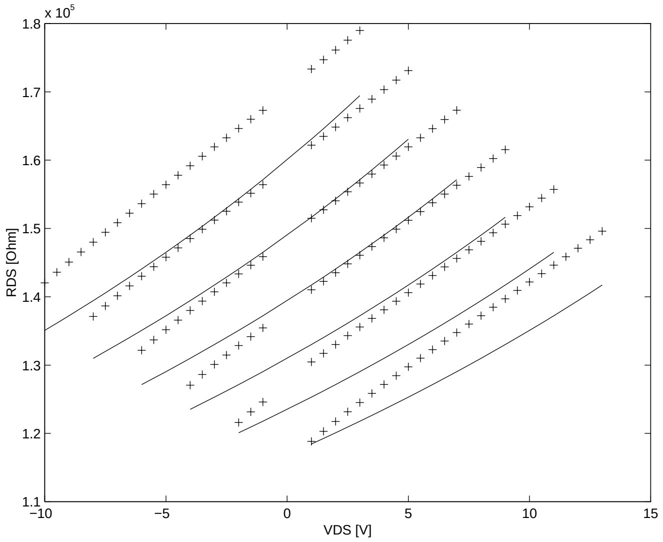


Fig. 5.42 N-well resistor characteristic **of a typical wafer. W/L = 3/200 -VBS = 0,2,4,6,8,10 V, + = measured, — = SPICE JFET model**

5.5. Capacitor Characteristics

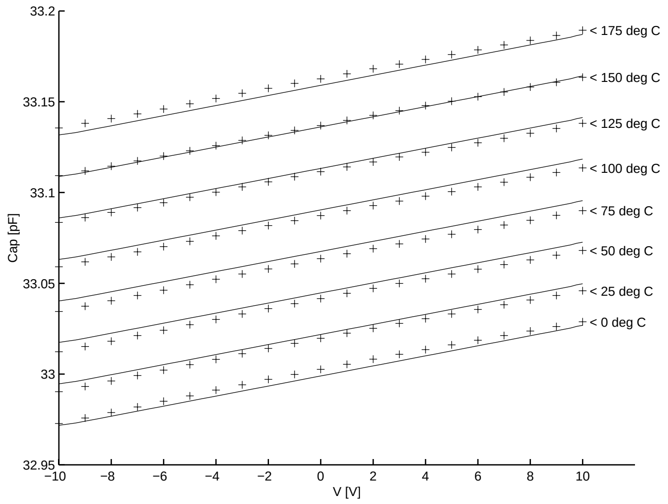


Fig. 5.43 CPOLY characteristic **of a typical wafer.**
+ = measured, — = SPICE Cap model

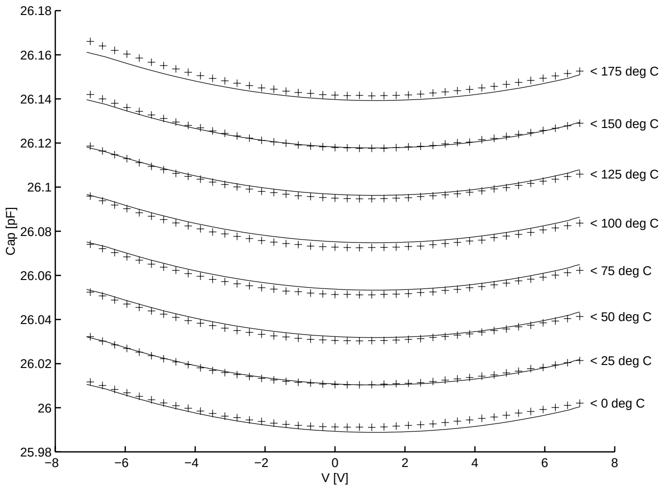


Fig. 5.44 CMIM characteristic **of a typical wafer.**
+ = measured, — = SPICE Cap model

6. Support

For questions on process parameters please refer to:

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