Electrical modeling of monolithically integrated GMR based current sensors

M.D. Cubells-Beltrán, C. Reig
Dept. of Electronic Engineering
Universitat de València
Burjassot, Spain
candid.reig@uv.es

A. De Marcellis
Dept. of Ind. & Infor. Eng & Econ.
University of L'Aquila
L'Aquila, Italy

S. Cardoso, P.P. Freitas
INESC-MN and IST
Universidade de Lisboa
Lisboa, Portugal

***Abstract*— We report on the electrical compact model, using Verilog-A, of a monolithically integrated giant magneto-resistance (GMR) based electrical current sensors. For this purpose, a specifically designed ASIC (AMS 0.35µm technology) has been considered, onto which such sensors have been patterned and fabricated, following a two-steps procedure. This work is focused on the DC regime model extraction, giving evidences of its good performance and stating the bases for subsequent model improvements.**

Keywords—Verilog A, analytical compact modelling, giant magnetoresistance (GMR).

I. INTRODUCTION

Magnetic sensors based on the Giant Magnetoresistance (GMR) and Tunnel Magnetoresistance (TMR) effects have already overcome their initial definition stage and they have become the primary option in many applications requiring the measurement of low magnetic field with very small sensors, at room temperature [1]. Once flash memories have shadowed their main field of application as head readers in massive storage hard disk drives, current research trends are in the direction of fixing and improving some critical parameters for specific sensing (analogue) applications. In this sense, biotechnology is one of the subject which has better taken advance of the inherent properties of these sensors: high sensitivity, high level of integration and compatibility with standard CMOS processes. Nowadays, measurement of nervous signals or monitoring of magnetically labelled molecules and cells have been successfully achieved by using GMR sensors. Complementarily, novel industrial applications have emerged based on this technology. As a representative example, in electrical current monitoring, GMR sensors have been scaled down from A to µA regimes in the last two decades, mainly favoured by recent advances in GMR-CMOS integration processes [2]. Chronologically, the use of GMR sensors for electrical current monitoring (several amps) was well established in 2004 [3]. First measurements of currents in the mA range was demonstrated in 2005 and developed in 2009 [4]. Sub-mA currents were measured with this kind of sensors in 2014 [5] and they were successfully integrated with a dedicated ASIC from a standard CMOS technology (AMS 0.35µm) in 2017 [6]. Consequently, GMR (and TMR) sensors can actually being used as basic design devices in the development of highly complex instruments, in different fields such as microelectronics world, biotechnology or the automobile industry, if we want to mention a few.

In this sense, a major effort has been carried last years in order to state general electrical models of these devices which can be used in easing design processes. Several approaches have been reported in the literature, ranging from the physical point of view (finite element method) [7] to behavioural compact development [8]. The present work focuses on the last. From an electrical point of view, such kind of structures can be perfectly understood as a quadrupole with a transfer function which relates its output resistance to the applied magnetic field (if conventional magnetic sensors are involved) or directly to the driven electrical current (if electrical current sensors are specifically considered), as depicted in Fig. 1. In this scheme, R, at the output terminals (1') and (2') represents the sensor resistance, depending on the driven current I (see Eq. 1), while r, connected to the input terminals (1) and (2) represents the input resistance of the current sensor, due to the current strip.

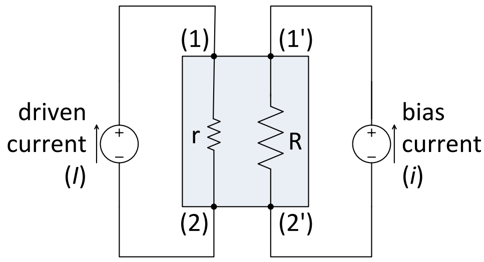

Fig. 1. Scheme describing the quadrupole nature of a typical current sensor.

A handicap arises from the fact that for the most SPICE-like based circuit simulators, resistances are native devices, so they cannot be reformulated without modifying the source code [9]. A 'universal' HSPICE macro-model for GMR memory bits was claimed in [10] as one of the preliminary attempts for developing electrical models of GMR based devices. In this reference work, the presented model was realized as a four-terminals sub-circuit, taking account of quasi-static effects for digital/memory applications. A similar approach was followed in [11], also for digital/memory applications, but with TMR based devices. The development of models for TMR sensors is actually a matter of concern [12]. The hysteresis effects were incorporated to the model by including bi-stable memory elements, voltage controlled sources and switches in the developed sub-circuit. In fact, modelling hysteretic effects in magnetic sensors is a major issue that is still a matter of concern [13], [14].

When dealing with analogue sensing applications, magnetic sensors usually operate in linear regimes, far from saturation states, where hysteresis effects are often negligible. A common example is found in crossed-axis spin-valves, a particular implementation of GMR sensors, which are currently used in many microelectronics current monitoring applications due to their high sensitivity and low hysteresis. In these scenarios, linear models usually fit the sensors behaviour, at least in their quasi-static regimes, and for low field conditions. Under these constrains, compact analogue behavioural models have been developed for GMR based electrical current sensors at the integrated circuit (IC) level. To do it, the use of high level description languages is

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absolutely recommendable. Among other currently available hardware definition languages (HDL), Verilog-A has emerged as a powerful and flexible standard for the analysis and design of systems, circuits and analogue devices, including sensors [8]. Verilog-A displays two major advantages (when compared to SPICE-like simulators): first, pseudo-electrical mechanisms can be included in the model; and on the other hand, a Verilog-A model can be directly interfaced to any circuit simulator owing an appropriate compiler. In this regard, a Verilog-A analytical compact model of GMR based current sensors was developed in [15], and it was applied to the analysis of electrical power consumption at the mA currents range. The design and fabrication processes of these sensors, in which conductive electrical current microstrips where integrated together with the GMR sensing structures, arranged as full Wheatstone bridges, can be found in [4]. As an additional advantage, the use of high level description languages allows the development of well-structured models, open for subsequent behavioural updates. In this sense, the thermal response of the previously refereed sensors, including self-heating, was incorporated to the model in [8].

With the aim to go a step forward, we present in this contribution the development, by using Verilog-A, of the lineal quasi-static analytical compact model of the GMR based electrical current sensors which were integrated in the ASIC reported in [6].

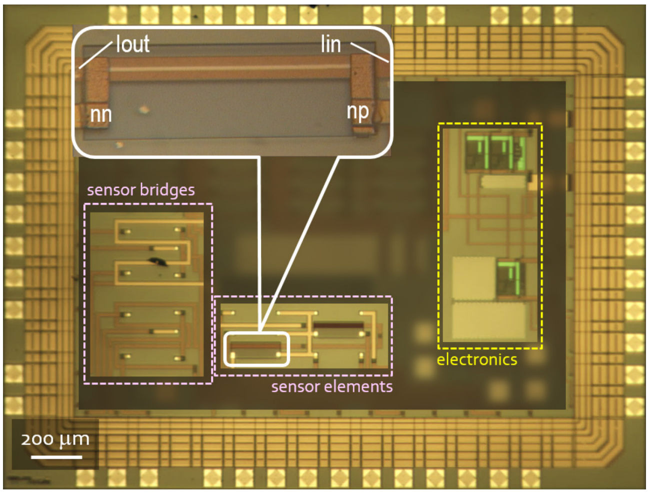

Fig. 2. (a) Microphotograph of the chip considered for this study, with the most important details.

II. Model Extraction

The micrograph of the considered ASIC, with the main important structures highlighted, is displayed in Fig. 2. As observed, we can find sensors consisting of a unique sensing GMR element and also arrangements of Wheatstone sensors. From the magnified layout of one of the elemental sensors included in Fig. 2, the scheme of Fig. 1 can be easily derived. The equation describing its behaviour is as simple as:

$$R = R_0 + MR \cdot I \tag{1}$$

where R_0 is the resistance of the sensor at null current and MR is the tangent of the dependence of the resistance as a function of the driven current (I) within the lineal range. As measured in [4], the lineal range of these sensors is of the order of ±100 mA. Regarding the of the sensor bridges, their full character is achieved with the serpentine design of the current strip, as explained in [4], and each arm can be individually described with an equation like Eq. 1. a General Purpose Interface Bus (GPIB) controlled setup was used, which included a personal computer, a power supply (PS2521G, Tektronix), a current source (220, Keithley), a data acquisition switch unit (34970A, Agilent), and a multimeter (34401A, Agilent).

A. Elemental sensors

Elemental sensors were firstly analysed. In this case, the range of interest of the considered current was set to ±1 mA. For the measurements, a General Purpose Interface Bus (GPIB) controlled setup was used, which included a personal computer, a power supply (PS2521G, Tektronix), a current source (220, Keithley), a data acquisition switch unit (34970A, Agilent), and a multimeter (34401A, Agilent). So obtained results for a typical case are shown in Fig 3, together with the fitting parameters required for constructing the model following Eq. 1.

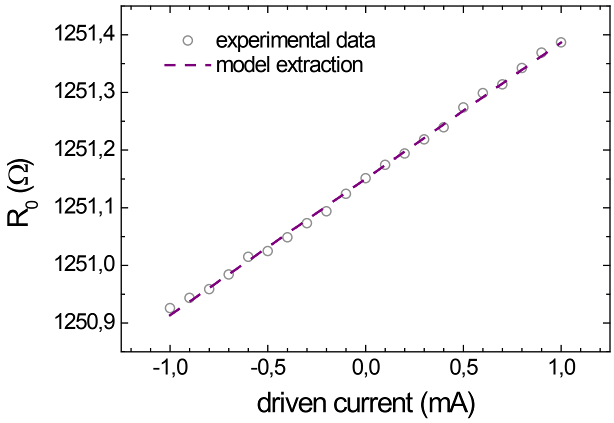

Fig. 3. (a) Microphotograph of the chip considered for this study. A single sensor is magnified to explain the model (b).

B. Sensor bridges

For the bridges, the resistances of the branches have been measured as a function of the driven current. Then, the parameters, considered individually, have been extracted from series-parallel considerations. So obtained results are collected in Fig. 4. As complementary result, the set of extracted parameters is detailed in Tab. I. The full bridge behaviour can be clearly observed in this figure, as well as in the changing sign of the *MR* parameters in the table. These results are in good accordance with those reported in [4].

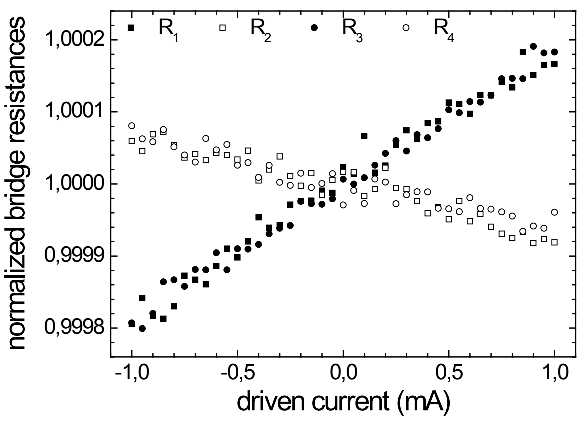

Fig. 4. Model parameter extraction of the bridge sensors.

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TABLE I. EXTRACTED PARAMETERS FOR A TYPICAL BRIDGE SENSOR

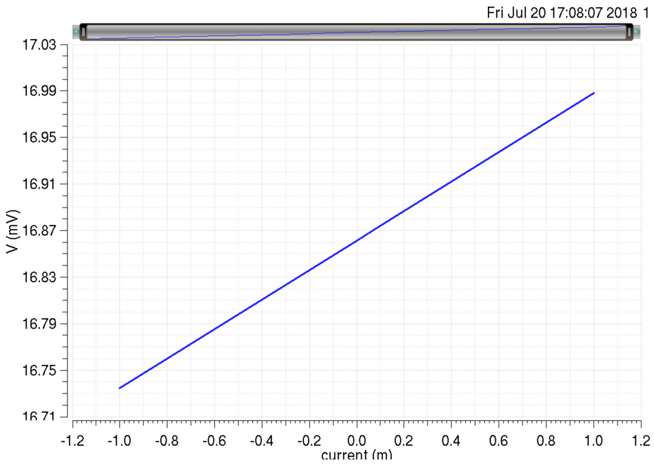
	R_0 (Ω)	MR (Ω/mA)
R_1	2073,644±0,004	+0,387±0,009
R_2	1925,835±0,007	-0.138±0,007
R_3	2057,098±0,003	+0.384±0,006
R_4	2070,463±0,004	-0,129±0,007

III. RESULTS

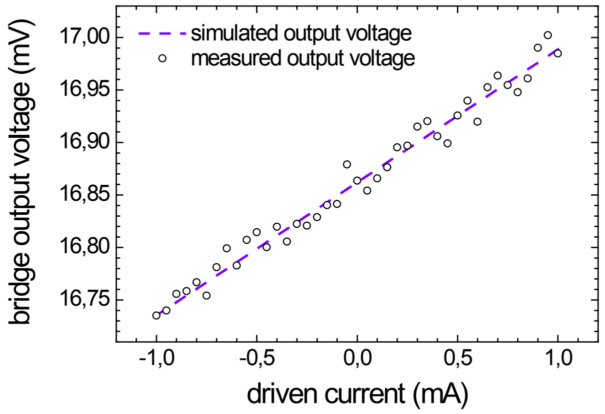
For testing the extracted model, a typical sensor bridge was biased with a DC current of 1 mA, and the differential output voltage was both simulated and measured. Fig. 5 (a) shows simulation results, as obtained from Cadence by using the corresponding Verilog-A model, while Fig. 5 (b) shows the comparison between measured and simulated results. As observed, a good agreement is found.

IV. CONCLUSIONS

An analytical compact model of a GMR based electrical current sensor has deployed with the Cadence IC suit, and then integrated with the design of an ASIC in standard CMOS 0.35 µm technology, so opening the door of a huge range of derived applications.



(a)



(b)

Fig. 5. (a) Simulated output voltage in a bridge sensor; (b) Simulated vs. measured results.

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