TÉCNICO LISBOA

Microelectronics

Lab 1

$I_D(V_{GS})$ and $I_D(V_{DS})$ simulation with Virtuoso

Bologna Degree in Physics Engineering (LEFT)
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Group 4
Duarte Miguel de Aguiar Pinto e Morais Marques | 96523
Francisco Tavares Braz Mêda | 96530
José Rocha | 98839

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1 Introduction [3] [5]

In this laboratory assignment, the MOSFET operation regions are studied in detail. The *software* Cadence Virtuoso (version 6.1.7) is used in order to run simulations and obtain the curves of the drain current - $I_D(V_{GS})$ and $I_D(V_{DS})$ for an nMOS transistor; $I_D(V_{SG})$ and $I_D(V_{SD})$ for a pMOS transistor. For this purpose, the different views shown in Table 1 were created. The library `1stlab` contains the schematics and symbols for the nMOS and pMOS transistors. The simulations are run in the views of the library `1stlab_sim`. The contents of these libraries are explained in further detail in Sections 2 and 3.

Library	Cell	View
1stlab	nmos	schematic
		symbol
	pmos	schematic
		symbol
1stlab_sim	nmos	id_vgs
		id_vds
	pmos	id_vsg
		id_vsd

Table 1: Libraries, cells and views created in Virtuoso.

The **Field Effect Transistor (FET)** is one of the main types of transistors and it can be used as a controlled current source. It is a 4-pin device, with gate (G), source (S), drain (D) and body. In this laboratory activity, the MOSFET (Metal Oxide Semiconductor Field Effect Transistor) - in which the channel is not physically present (as opposed to JFETs) - is considered. The MOSFETs can have an n-channel or a p-channel - they are thus designated nMOS or pMOS transistors, respectively.

In Figure 1, the **nMOS transistor** symbol is represented. The minimum voltage between gate and source (V_{GS}) for which there is a drain current I_D is called the threshold voltage, V_{TH}. For $V_{GS} < V_{TH}$, the device is said to be turned off (**cut-off region**). Once $V_{GS} \geq V_{TH}$ and $0 < V_{DS} < V_{GS} - V_{TH}$, the MOSFET is in the **triode or ohmic region**, in which the drain current is given by equation 1. The device can behave like a V_{GS} controlled resistor.

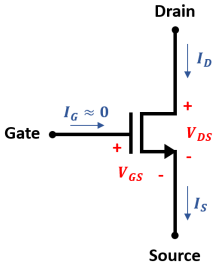


Figure 1: nMOS transistor symbol

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \tag{1}$$

On the other hand, when the nMOS transistor is in the **saturation region**, $V_{GS} \geq V_{TH}$ and $V_{DS} \geq V_{GS} - V_{TH}$. It behaves like a V_{GS} controlled current source and the drain current's value is given by equation 2.

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \tag{2}$$

In reality, the drain current in the saturation region does not remain constant, but instead varies with a certain slope, due to the channel length modulation parameter (λ_n), according to the following equation:

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda_n V_{DS}) \tag{3}$$

The transition between the triode and saturation regions happens when $V_{DS} = V_{GS} - V_{TH}$. Substituting this equality into equation 2, an expression for the current at which the transition occurs, given a fixed V_{GS}, is obtained:

$$I_{D_t} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} V_{DS}^2 \tag{4}$$

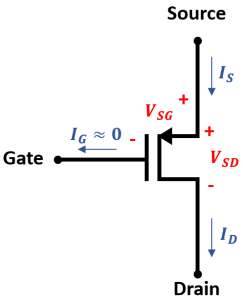


Figure 2: pMOS transistor symbol

The **pMOS transistor**'s behaviour follows similar equations and conditions. However, since carriers are now holes, the current is now I_S and the voltages are reversed (V_{SG} and V_{SD} are considered). The threshold voltage, V_{TH}, usually has different values for pMOS transistors. In the triode region, $V_{SG} \geq V_{TH}$, $0 < V_{SD} < V_{SG} - V_{TH}$ and the source current is given by equation 5.

$$I_S = \mu_n C_{ox} \frac{W}{L} \left[(V_{SG} - V_{TH}) V_{SD} - \frac{1}{2} V_{SD}^2 \right] \tag{5}$$

For the saturation region, in which $V_{SG} \geq V_{TH}$ and $V_{SD} \geq V_{SG} - V_{TH}$, the source current is given by equation 6.

$$I_S = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{SG} - V_{TH})^2 \tag{6}$$

Once again, the current in the saturation region does not actually remain constant. Instead, it varies according to equation 7, due to the effect of the channel length modulation parameter, λ_p.

$$I_S = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{SG} - V_{TH})^2(1 + \lambda_p V_{SD}) \tag{7}$$

The transition current[1] for a fixed V_{SG} is now given by equation 8.

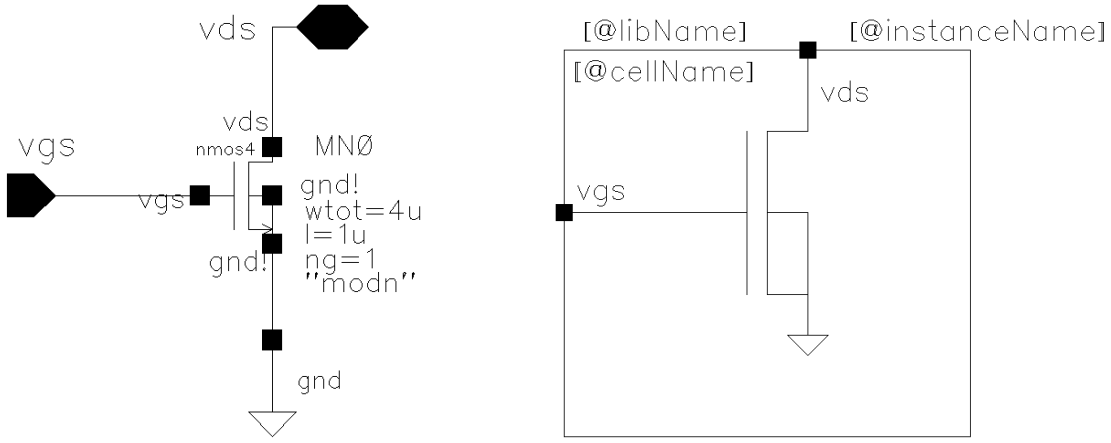
$$I_{S_{transition}} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{SD}^2 \tag{8}$$

The equations presented in this section are obtained by considering a first model approximation for the nMOS and pMOS transistors.

2 Simulations for the nMOS transistor

In order to obtain the curve $I_D(V_{GS})$ for the nMOS transistor, the tutorials available in the subject's webpage were repeated [2] [4]. Having enabled the use of the afs disk space, configured the appropriate vpn and installed the Xming and PuTTY softwares, Cadence Virtuoso can be accessed via the PuTTY terminal. A script from austriamicrosystems is used to initialize the Cadence Custom IC Design tools with the process technology C35B4C3 and the Command Interpreter Window is started in mode Front-To-Back Design.

In the library `1stlab`, in which the schematics and symbols of the transistors (which will be added as Instances in the simulation views) are present, the cell `nmos` contains the mentioned views for the nMOS transistor. In `schematic`, the `nmos4` transistor of 1 gate, length "1uM" and width "4uM" from the library PRIMLIB is added. Additionally, an input `vgs` and an inputOutput `vds` are connected to the respective terminals - this will be necessary in the simulation, in which a voltage source will be connected to each terminal. Moreover, the source is connected to ground. The symbol view is needed for the schematic. The designs in both views are shown in Figure 3.



[1] It is considered that the value of I_G is negligible, thus $I_S \approx I_D$ and only curves for I_D will be obtained.

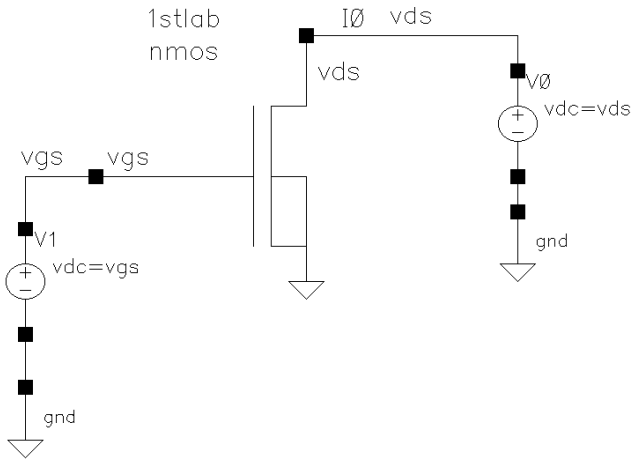


Figure 3: Views `schematic` [upper left] and `symbol` [upper right] (Cell `nmos`, Library `1stlab`). Circuit for simulation in Views `id_vds` and `id_vgs` [below] (Cell `nmos`, Library `1stlab_sim`) - in order to obtain the $I_D(V_{DS})$ and $I_D(V_{GS})$ curves (respectively), only the voltage `vgs` or `vds` is set as a variable in the schematic (the other voltage is swept from 0 to 3.3V).

The simulation schematics created for the nMOS transistor (also shown in Figure 3) are `id_vgs` and `id_vds`, in which the $I_D(V_{GS})$ and $I_D(V_{DS})$ curves (respectively) are obtained. Having added the nMOS symbol created previously, voltage sources (from the library analogLib) are connected to the gate and the drain. A DC analysis is made in both cases, with V_{GS} or V_{DS} (resp.) being swept from 0 to 3.3V, since 3.3V is the maximum voltage which the technology can withstand. The other voltage is then selected in Parametric Analysis. In `id_vgs`, the simulation is done for $V_{DS} = \{1, 2, 3\}\ [V]$ (as shown in the video tutorial); in `id_vds`, the curve is simulated for $V_{GS} = \{0, 0.8, 1.6, 2.4, 3.2\}\ [V]$. The plots obtained in the simulations are shown in Figure 4.

In the curves shown in Figure 4, it is possible to identify the three operating regions of the transistor. In $I_D(V_{DS})$, the curve for $V_{GS} = 0V$ remains (approximately) at zero, because $V_{GS} < V_{TH}$ [1], thus the transistor is permanently **OFF**. For the other curves, the transistor is **OFF** only at $V_{DS} = 0V$, while the **saturation region** is reached at $V_{DS} = V_{GS} - V_{TH}$, where I_D remains (approximately) constant (independent of V_{DS} - the nMOS works as a voltage controlled current source). In the **triode region** (which happens for $V_{DS} < V_{GS} - V_{TH}$), for lower values of V_{DS}, the curve showed a relatively linear behaviour - the transistor works as a voltage controlled resistor. For higher values of V_{DS} in this region, the term with V_{DS}^2 in equation 1 dominates and the curve becomes more parabolic. As expected, the value of the current in saturation increases with V_{GS}, but this higher voltage also means that the transistor works as a current source for a smaller range of V_{DS} (saturation range). On the other hand, a smaller value increases the sensitivity to V_{TH} - thus the usual design criteria of defining $V_{DS_{sat}} = 200mV$ [2]. By analysing Figure 4, it is also noticeable that, even once the saturation region is reached, at $V_{DS} = V_{GS} - V_{TH}$, the drain current continues to increase with a small slope. This might suggest the effect of a (small) channel length modulation parameter λ_n, which doesn't allow the current in saturation to remain constant.

As for the $I_D(V_{GS})$ curve, the transistor remains in the **cut-off region** until $V_{GS} = V_{TH}$; as it is seen in Figure 4, the drain current remains close to zero until that voltage value is reached (in fact, in this subthreshold interval, there is an exponential behaviour [2]). It is also apparent that, when $V_{TH} < V_{GS} < V_{DS} + V_{TH}$, the current follows a square law - this happens in the **saturation region**. Once $V_{GS} \geq V_{DS} + V_{TH}$, the transistor enters the **triode region**, in which the curve is (almost) linear. It is important to notice that, for the green curve ($V_{DS} = 3V$), the saturation region is not seen, since V_{GS} is swept only until $3.3V (< V_{DS} + V_{TH})$. Another important aspect to notice is that, in the saturation region, the current is almost the same for the different curves - thus, independent of V_{DS}. This was correctly predicted by equation 2. However, as V_{DS} increases, a slight variation is more easily detected, as expected due to equation 3 - the effect of λ_n can be noticed.

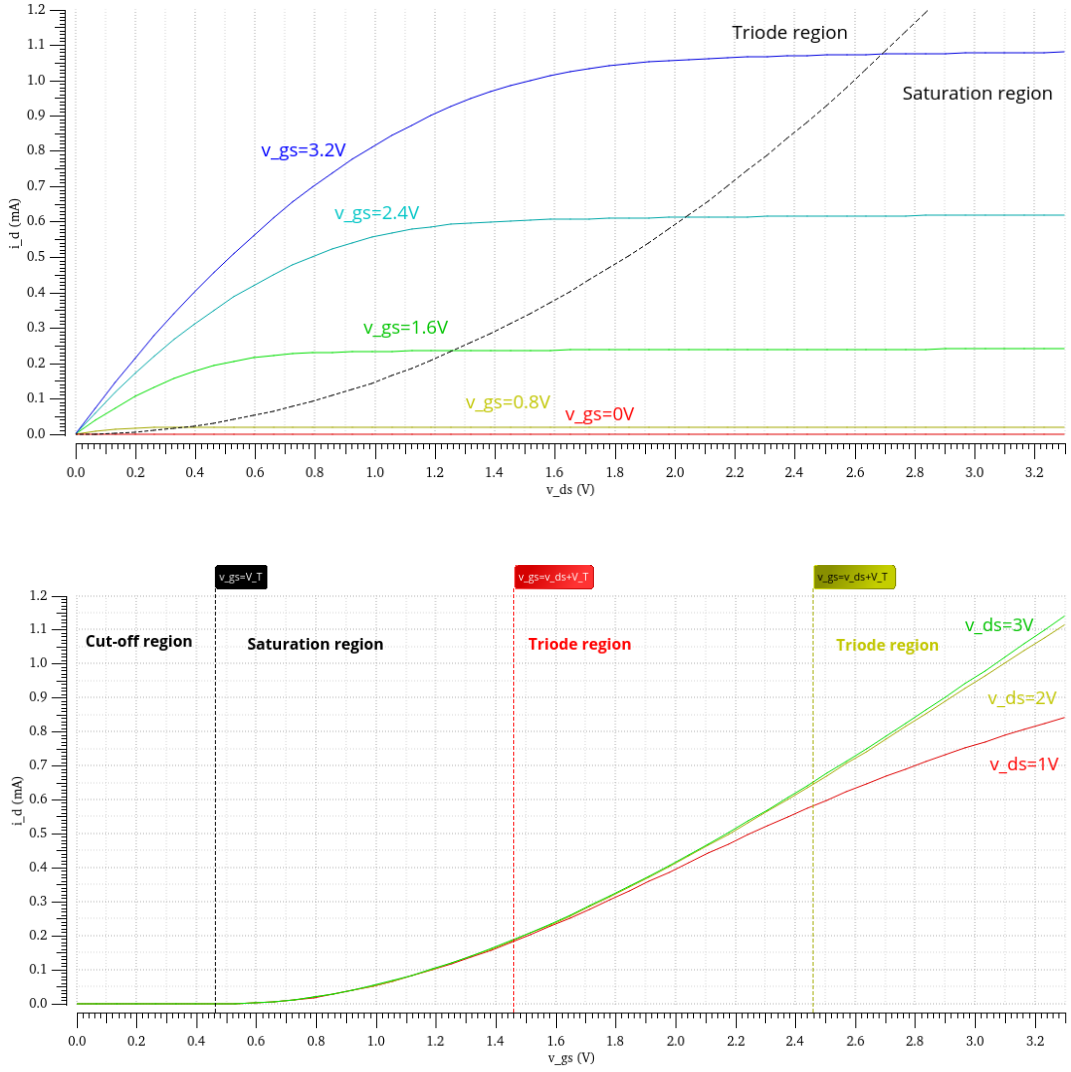


Figure 4: nMOS: Simulation results of the curves $I_D(V_{DS})$ for $V_{GS} = \{0, 0.8, 1.6, 2.4, 3.2\}\ [V]$ [above] and $I_D(V_{GS})$ for $V_{DS} = \{1, 2, 3\}\ [V]$ [below]. In $I_D(V_{DS})$, the curve given by equation 4 is plotted in a dashed line. In $I_D(V_{GS})$, the different operating regions indicated begin in the closest vertical line to their left. The labels always refer to the respective curves with the same colours.

In order to plot equation 4 in the curve $I_D(V_{DS})$ above, the value $KPN \equiv \mu_n C_{ox} = 170\ \mu A/V^2$, available in `austriamicrosystem`'s datasheet [1], was initially considered, as well as the threshold voltage, given by $V_{TH} = 0.46V$. All technology parameters are characterized statistically, by normal distributions, but the average values were considered for KPN and V_{TH}, since the simulations in Virtuoso use these values. The value of the threshold voltage was obtained for transistors with long channels, which is more adequate to the nMOS transistor used in the simulation (with length $1\mu m$), instead of the values of V_{TH} for short channels (also shown in the datasheet). Moreover, it is very important to mention that the value of KPN was also determined for large transistors and, in particular, in the linear region. This value will have a much larger variability, depending on the length of the transistor and the values of V_{DS} being considered.

Because of the conditions in which KPN was obtained, while plotting equation 4 into the first curve shown in Figure 4, the values of V_{DS} for the intersection were not close to their expected values $V_{GS} - V_{TH}$. Thus, in order to plot the parabolic curve, vertical lines with $V_{DS} = V_{GS} - V_{TH}$ were used in Virtuoso to determine the points of intersection with the curves, from which a fit was performed with equation 4, using Fitteia - a web-based fitting platform and trademark of Instituto Superior Técnico. These results are shown in Table 2. Moreover, regarding the effect of the channel length modulation parameter, the values of the drain current were also measured for $V_{DS} = 3.3V$, in

order to quantify the variation of I_D in the saturation region.

V_{GS} (V)	$V_{GS} - V_T$ (V)	I_{D_t} (μA)	$\mu_n C_{ox}$ $(\mu A/V^2)$	I_D $(V = 3.3\ V)$ (μA)	I_D variation (%)
0.8	0.34	18.8133	73.9903	20.7206	10.1
1.6	1.14	235.469		242.614	3.0
2.4	1.94	612.641		620.442	1.3
3.2	2.74	1075.56		1080.76	0.5

Table 2: Numerical values obtained from the $I_D(V_{DS})$ curve in Figure 4. The value I_{D_t} is the transition current between the triode and saturation regions measured in the curve for $V_{DS} = V_{GS} - V_{TH}$, where $V_{TH} = 0.46\ V$ [1]. The value of $\mu_n C_{ox}$ was obtained by fitting equation 4 to the points $(V_{GS} - V_{TH}, I_{D_t})$ using Fitteia. The final column corresponds to the increase in the drain current's value from I_{D_t} to $I_D(V = 3.3\ V)$.

The value of $\mu_n C_{ox}$ shown in Table 2 is less than half (in specific, $\approx 43.5\%$) of KPN given in the datasheet, which indicates that, in fact, this parameter must be very dependant on the channel length of the transistor, as well as the values of V_{DS} in which it is measured. Thus, it is not valid to consider KPN for the transistor of length $1\mu m$ used in this simulation. Regarding the I_D variation, given by $[I_D(V_{DS} = 3.3V) - I_{D_t}]/I_D(V_{DS} = 3.3V)$, it is increasingly less significant as V_{GS} increases, since the current values are higher. A value of λ_n could have been estimated by calculating the slope of the curve in the saturation region and using equation 3. However, the value of $\mu_n C_{ox}$ would have to be used; as it's been discussed, this parameter varies a lot with the channel length and V_{DS}, thus the validity of its use for higher values of V_{DS} would not be guaranteed.

Finally, the points of intersection between the $I_D(V_{GS})$ curves and the vertical lines shown in Figure 4 are presented in Table 3. According to the theoretical model, the drain current in the cut-off region should be zero. However, this does not happen, even though I_D has a small order of magnitude in this voltage interval - of $10^{-7}A$ in $V_{GS} = V_T$, as shown below. On the other hand, the current from which the transistor is in the triode region increases significantly as V_{DS} increases, as expected and as it was also possible to see in the $I_D(V_{DS})$ curves.

V_{DS} (V)	I_D $(V_{GS} = V_{TH})$ (nA)	V_{DS}+V_{TH} (V)	I_D $(V_{GS} = V_{DS} + V_{TH})$ (μA)
1	110.571	1.46	183.388
2	116.716	2.46	645.147
3	124.871	3.46	-

Table 3: Numerical values obtained from the $I_D(V_{GS})$ curve in Figure 4. The drain currents shown in the second and fourth columns were measured in $V = V_{TH}$ and $V = V_{DS} + V_T$ (respectively), where $V_{TH} = 0.46\ V$ [1]. No current value is shown in the final column for $V_{DS} = 3V$, since the voltage value is larger than 3.3V.

3 Simulations for the pMOS transistor

The simulations made in Section 2 were recreated in the cell `pmos` for the pMOS transistor, using the views `id_vsg` and `id_vsd`. In this case, in the view `schematic` of the library `1stlab`, the `pmos4` transistor (1 gate, length "1uM" and width "4uM" - same as before) from the library PRIMLIB was included. The designs in the library `1stlab` are shown in Figure 5. In the same figure, the simulation schematic (present in library `1stlab_sim` and cell `pmos`) used for the pMOS transistor is shown. Having added the pMOS symbol created previously, the voltage sources (from the library analogLib) for V_{SG} and V_{SD} between the source and the gate or drain, respectively, are also used. In this case, the pin that must be selected in the transistor (drain) in order to run the simulations in `id_vsg` and `id_vsd` is connected to ground.

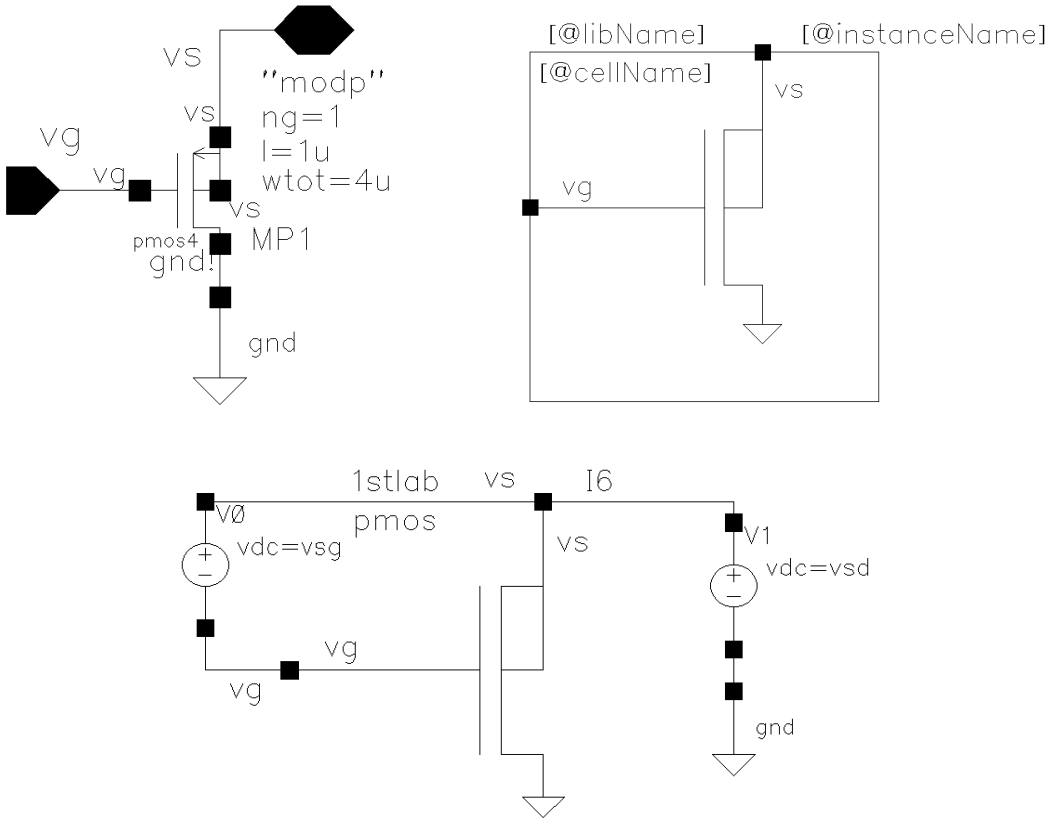


Figure 5: Views `schematic` [upper left] and `symbol` [upper right] (Cell `pmos`, Library `1stlab`). Circuit for simulation in Views `id_vsd` and `id_vsg` [below] (Cell `pmos`, Library `1stlab_sim`) - in order to obtain the $I_D(V_{SD})$ and $I_D(V_{SG})$ curves (respectively), only the voltage `vsg` or `vsd` is set as a variable in the schematic (the other voltage is swept from 0 to 3.3V).

Once again, a DC analysis is made, with V_{SD} or V_{SG} being swept from 0 to 3.3V, in order to obtain the curves $I_D(V_{SD})$ and $I_D(V_{SG})$ (resp.), shown in Figure 6. In the view `id_vsd`, the curve is simulated for $V_{SG} = \{0, 0.8, 1.6, 2.4, 3.2\}\ [V]$; in `id_vsg`, the simulation is done for $V_{SD} = \{1, 2, 3\}\ [V]$.

The analysis made for the drain current curves of the nMOS transistor is similar for the pMOS. In this case, we can consider that in both the curves for $V_{SG} = 0,\ 0.8V$ the transistor remains **OFF**, since the drain current is (approximately) zero for all V_{SD} values. This happens because the threshold voltage in the pMOS is higher - if $V_{SG} < V_{TH}$, the transistor remains in this region; in this case, $V_{TH} = 0.68V$ (in absolute value) is given in the datasheet, which is bigger than $0V$ and very close to $0.8V$ (the value in the datasheet is determined in saturation and for a channel of length $10\mu m$ [1], thus the threshold voltage for the pMOS transistor used in the simulation should be different). In the other three plots, the pMOS transistor is **OFF** only for $V_{SD} = 0V$ and the **saturation region** begins in the points of intersection between them and the parabolic curve in Figure 6 - in this region, I_D is approximately constant. The **triode region** occurs before that, when $V_{SG} \geq V_{TH}$ and $V_{SD} < V_{SG} - V_{TH}$, where the current has a linear behaviour for small values of V_{SD} and parabolic for higher values of this voltage (as predicted by equation 5). The parabolic curve in a dashed line was determined the same way as in section 2 - this is shown in Table 4. Once again, a small slope is registered in the saturation region, which indicates the effect of the channel length modulation parameter. As for the $I_D(V_{SG})$ curve, the **cut-off** region occurs for $0 \leq V_{SG} < V_{TH}$, the **saturation region** (square law) until $V_{SG} = V_{SD} + V_{TH}$, from which the **triode region** begins (linear behaviour). Once again, the curve for $V_{SD} = 3V$ does not reach the triode region before $V_{SG} = 3.3V$. The current in the saturation region is not very different between the three curves; however, it is worth noting that there is a more significant difference than in Figure 4, which might indicate a larger value of the parameter λ for the pMOS transistor - this will be further discussed ahead.

However, one key noticeable difference is the fact that the **currents** obtained for the pMOS transistor are much **smaller**. The main reason for this is that the **mobility of electrons** (n-type carriers) is higher than the **mobility of holes** (p-type carriers), because electrons are less bounded in an atom than a hole. Electron mobility μ_n is usually higher by a factor of 2 to 4 than the hole mobility μ_p [5], resulting in nMOS transistors having greater gains and speeds of operation than pMOS devices. In fact, pMOS technology originally dominated MOS integrated-circuit manufacturing and the original microprocessors utilized pMOS transistors. As the technological difficulties of fabricating nMOS transistors were solved, nMOS supplanted pMOS.

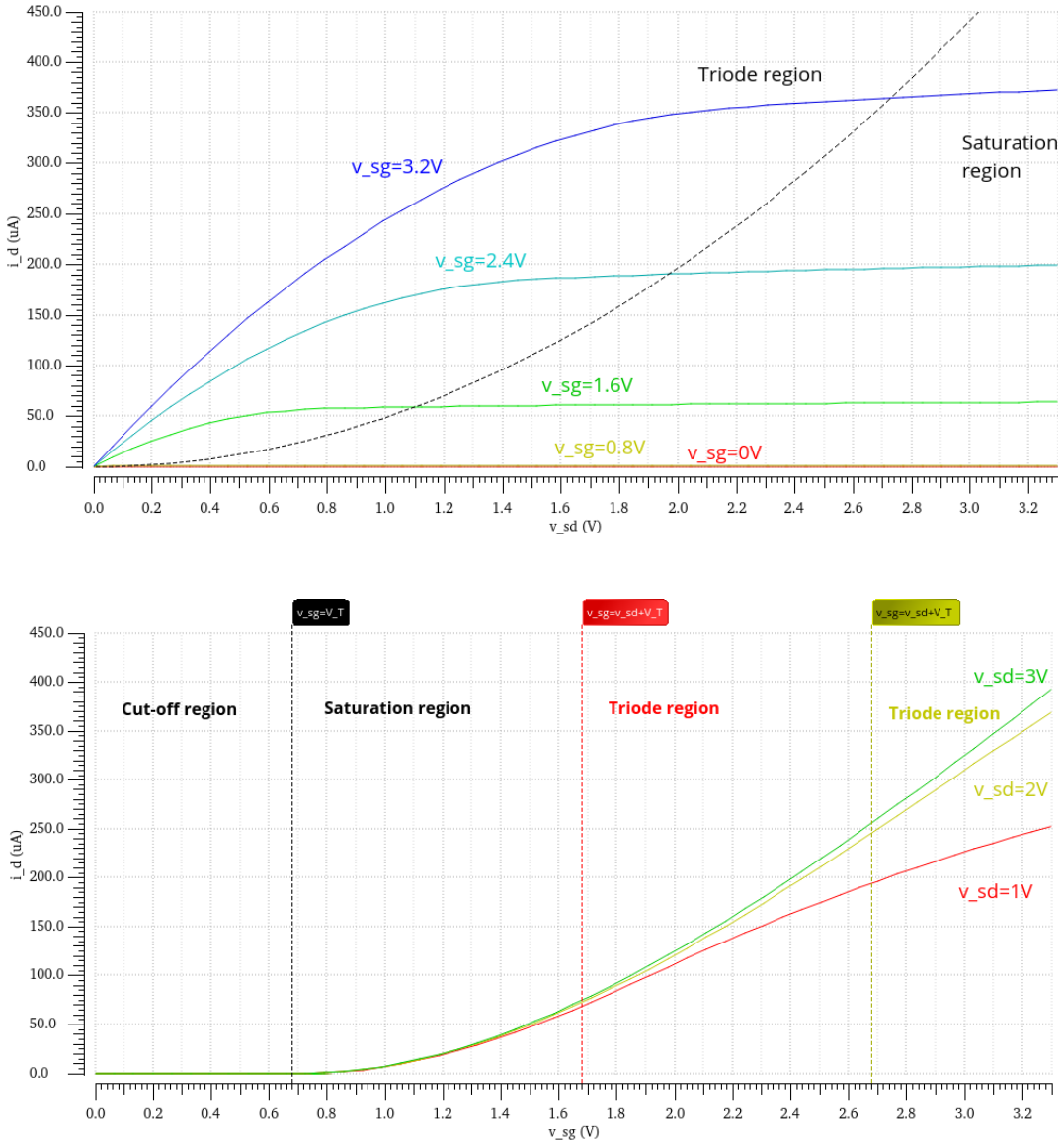


Figure 6: pMOS: Simulation results of the curves $I_D(V_{SD})$ for $V_{SG} = \{0, 0.8, 1.6, 2.4, 3.2\}\ [V]$ [above] and $I_D(V_{SG})$ for $V_{SD} = \{1, 2, 3\}\ [V]$ [below]. In $I_D(V_{SD})$, the curve given by equation 8 is plotted in a dashed line. In $I_D(V_{SG})$, the different operating regions indicated begin in the closest vertical line to their left. The labels always refer to the respective curves with the same colours.

For the pMOS transistor, the datasheet has a value of $KPP = 58\mu A/V^2$ for the gain factor, which, once again, leads to a parabolic curve (equation 8) which doesn't intersect the $I_D(V_{SD})$ curves in the expected $V_{SD} = V_{SG} - V_{TH}$ values. Therefore, the values shown in Table 4 were obtained in order to determine an experimental value for $\mu_p C_{ox}$. In this table, the measurements of the current for $V_{SD} = 3.3V$ are also shown, along with the current variation in the saturation region, given by $[I_D(V_{SD} = 3.3V) - I_{D_t}]/I_D(V_{SD} = 3.3V)$.

V_{SG} (V)	$V_{SG} - V_T$ (V)	I_{D_t} (μA)	$\mu_p C_{ox}$ $(\mu A/V^2)$	I_D $(V = 3.3\ V)$ (μA)	I_D variation $(\%)$
1.6	1.14	59.37154	24.4777	64.09390	8.0
2.4	1.94	190.338		199.7642	5.0
3.2	2.74	365.2202		372.8036	2.1

Table 4: Numerical values obtained from the $I_D(V_{SD})$ curve in Figure 6. The value I_{D_t} is the transition current between the triode and saturation regions measured in the curve for $V_{SD} = V_{SG} - V_{TH}$, where $V_{TH} = 0.68\ V$ [1]. The value of $\mu_p C_{ox}$ was obtained by fitting equation 8 to the points $(V_{SG} - V_{TH}, I_{D_t})$ using Fitteia. The final column corresponds to the increase in the drain current's value from I_{D_t} to $I_D(V = 3.3\ V)$.

Once again, the experimental value for $\mu_p C_{ox}$ is less than half ($\approx 42.2\%$) of the value given in the datasheet, which indicates that it varies significantly with the channel length and V_{SD}. It is also possible to conclude that, since the oxide layer capacity C_{ox} should not differ significantly between the nMOS and pMOS transistors, $\mu_n/\mu_p \approx 3$, which indicates that the **mobility of electrons is about 3 times higher than the mobility of holes** (between 2 and 4 times, as expected [5]). This explains why the drain currents for the pMOS transistor (represented in Figure 6) are smaller than the ones showed in Figure 4 for the nMOS transistor.

Besides the fact that the I_D variation $(\%)$ decreases with V_{SG} (same for the nMOS transistor), the measurements in Table 4 also indicate that the channel length modulation parameter for the pMOS (λ_p) should verify the relation $\lambda_p > \lambda_n$, since the drain current's variations $(\%)$ for a given $V_{GS/SG}$ are higher for this transistor. This goes according to expectations, since typical values for this parameter are $\lambda_n = 0.01V^{-1}$ and $\lambda_p = 0.02V^{-1}$ [2].

Finally, the values obtained from the $I_D(V_{SG})$ curves are shown in Table 5, in which it is clear that the currents in the cut-off region continue to have an order of magnitude of $10^{-7}A$ and that the current from which the transistor is in the triode region increases significantly as V_{SD} increases.

V_{SD} (V)	I_D $(V_{SG} = V_{TH})$ (nA)	V_{SD}+V_{TH} (V)	I_D $(V_{SG} = V_{SD} + V_{TH})$ (μA)
1	83.12993	1.68	68.77843
2	87.56474	2.68	245.048
3	91.13074	3.68	-

Table 5: Numerical values obtained from the $I_D(V_{SG})$ curve in Figure 6. The drain currents shown in the second and fourth columns were measured in $V = V_{TH}$ and $V = V_{SD} + V_{TH}$ (respectively), where $V_{TH} = 0.68\ V$ [1]. No current value is shown in the final column for $V_{SD} = 3V$, since the voltage value is larger than 3.3V.

4 Conclusion

In this laboratory assignment, the curves of the drain current for an nMOS and a pMOS transistor were successfully simulated using Virtuoso. For this purpose, in the library `1stlab`, the views `schematic` and `symbol` were defined. Moreover, two other schematics were created for each transistor in the library `1stlab_sim`, in which the simulations were run. The simulations of $I_D(V_{GS})$ and $I_D(V_{SG})$ were made for three different (fixed) values of V_{DS} and V_{SD}, respectively, whereas five (fixed) values of V_{GS} or V_{SG} were used in the other simulations.

The curves were analysed and the three operation regions of the transistors (cut-off, triode and saturation) were identified. The value of μC_{ox} for each transistor was determined experimentally using the currents in which the transition between the triode and saturation regions occurred. These experimental parameters varied significantly from the respective values shown in the datasheet, due to the different channel lengths and voltage values in which they were determined. Moreover, it was concluded that the electron mobility for the transistors used in this laboratory activity is about

three times higher than the hole mobility - thus higher values of the drain current were measured for the pMOS transistor.

Even though some discrepancies between the first order theoretical model and the experimental results were verified (for instance, the fact that the drain current was not constantly zero in the cut-off regions), the separations between the three operating regions of the devices were clear. The equations presented in section 1 successfully predicted the general behaviour of the drain current for different voltage values in the transistors.

References

[1] austriamicrosystems. *0.35 um CMOS C35 Process Parameters*. Document Number: ENG-182, Revision number 2.0. 2003.

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