Circuit Theory and Electronics Fundamentals

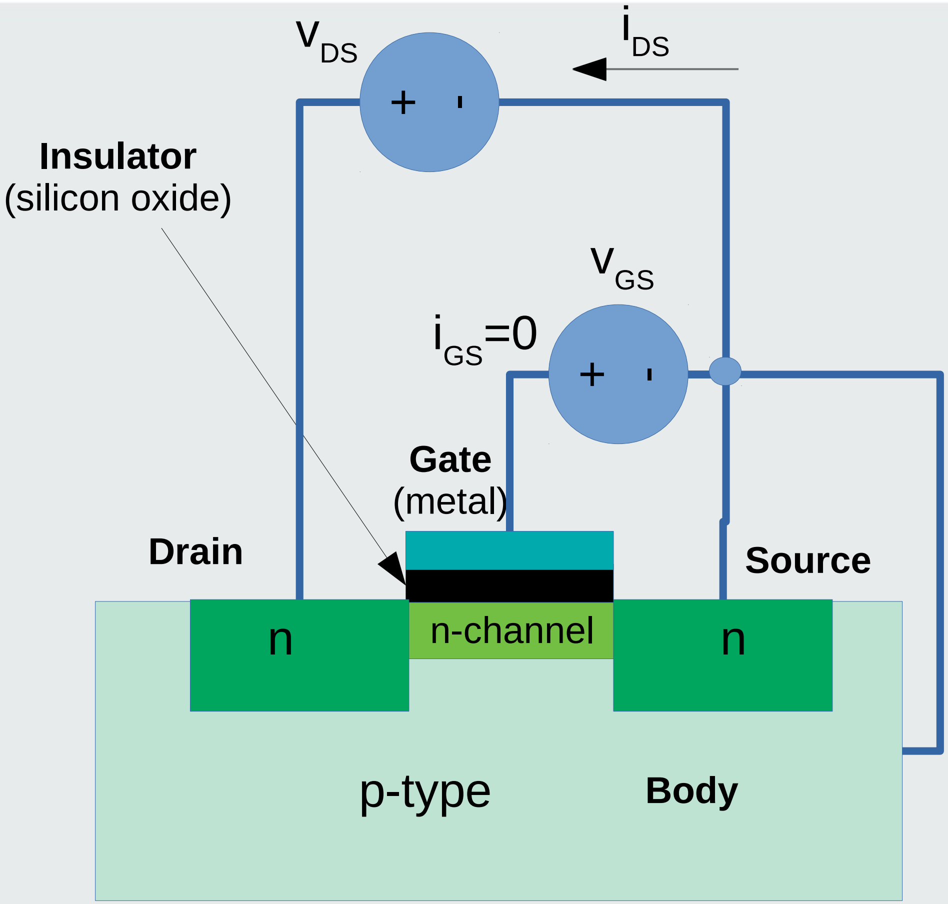
Lecture 18: The Metal Oxide Semiconductor Field Effect Transistor

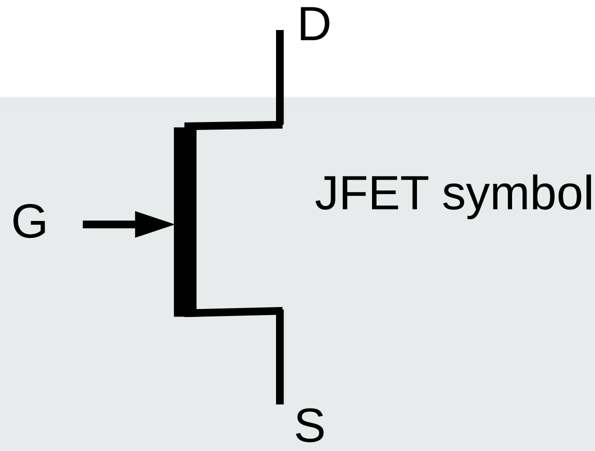
- Field Effect Transistors
- The Metal Oxide Semiconductor Field Effect Transistor (MOSFET):
  - Operation regions
  - Large signal model (DC)
  - Small signal model (AC)
  - Spice model
  - Comparison with BJT

The Field Effect Transistor

- The Field Effect Transistor (FET) is another way to realize a controlled current source
- Unipolar device: only one type of carrier (hole or electron) contributes electric current
- FET types:
  - Junction FET (JFET)
  - Metal Oxide Semiconductor FET (MOSFET)
- 4-pin device: Gate, Source, Drain and Body

The JFET



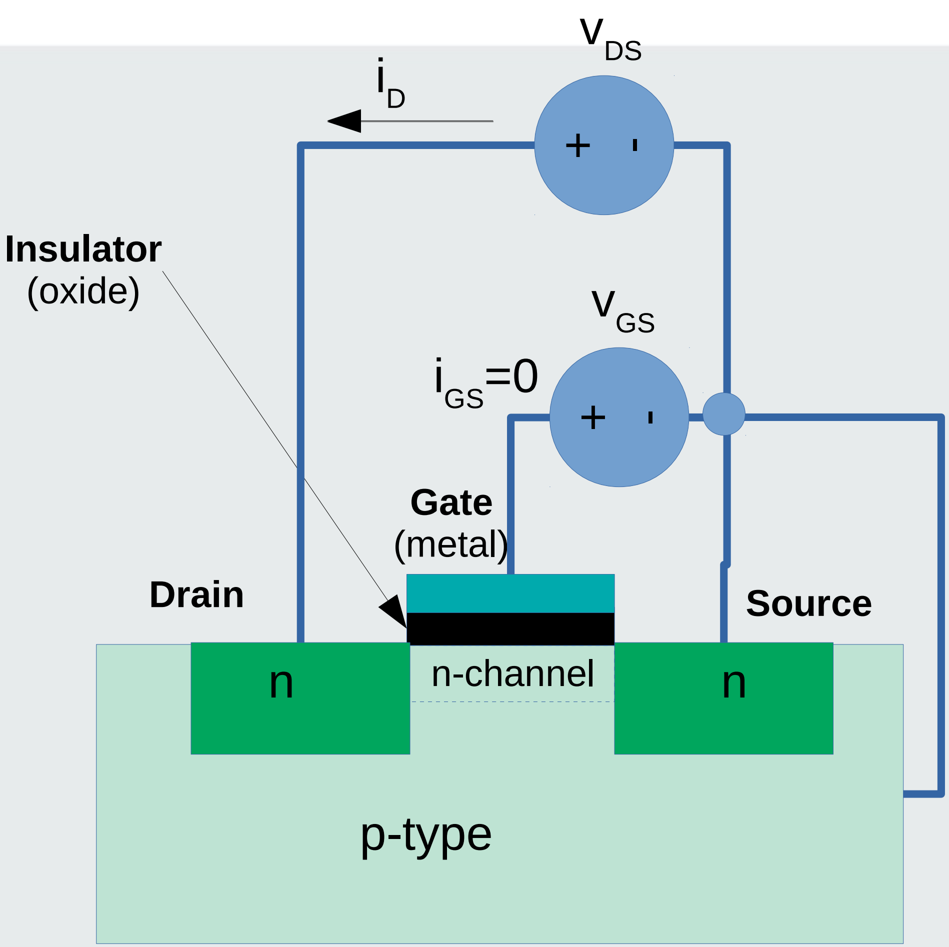


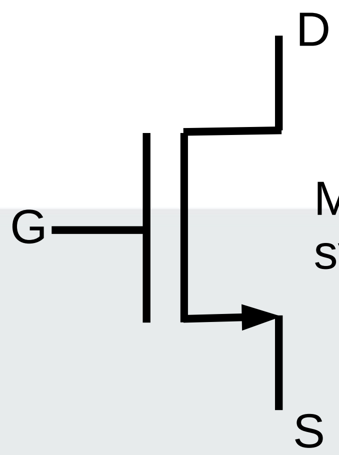
The Body is always always connected
to lowest voltage in chip

How the JFET works

- Channel physically present
- Current flows when positive v_{DS} applied
- A negative v_{GS} will deplete the channel and decrease the current until cut off
- For constant v_{GS} the current saturates with increasing v_{DS}

The MOSFET





MOSFET symbol

How the MOSFET works

- Channel **not** physically present
- Channel is created when high enough v_{GS} applied
- Current flows when channel present and positive v_{DS} applied
- A negative or insuficcient v_{GS} will cut off the device
- For a constant v_{GS} the current saturates with increasing v_{DS}

The MOSFET operation regions

- **Source** and **drain** are physically indistinguishable if no electric field applied
- When an electric field is applied
  - the **drain** is the higher potential terminal
  - The **source** is the lower potential terminal
  - Electrons move from source to drain (current flows from drain to source)
- The **gate** controls the amount of current that flows
- If $v_{GS} < V_T$ the MOSFET is in the **CUT-OFF region** – no current
  - V_T is the threshold voltage for MOSFETs (not to be confused with Diode's and BJT's thermal voltage V_T!)
- If $v_{GS} \geq V_T$ and $v_{DS} \leq v_{GS} - V_T$ the MOSFET is in the **OHMIC** or **TRIODE region** and behaves like a v_{GS} controlled resistor
- If $v_{GS} \geq V_T$ and $v_{DS} \geq v_{GS} - V_T$ the MOSFET is in the **SATURATION region** and behaves like a v_{GS} controlled current source

The MOSFET large signal model

$$i_D = 0$$

Cut-off region

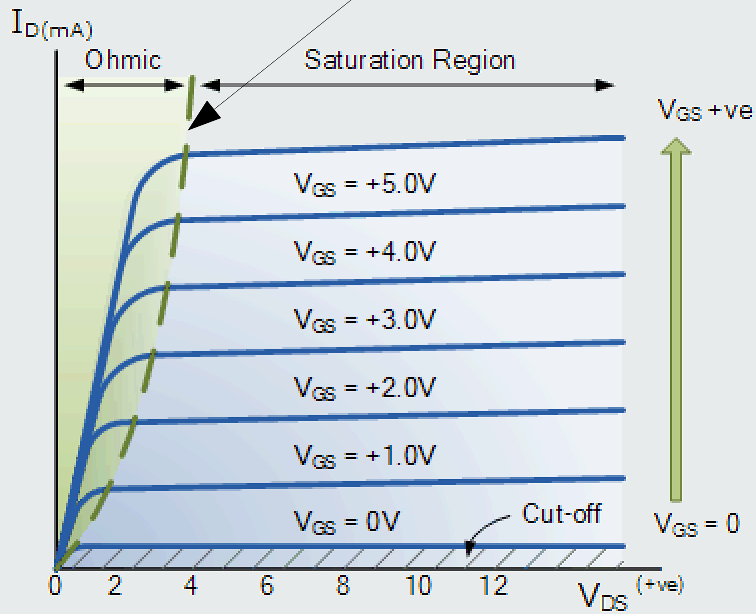
$$I_D = k\left[2\left(v_{GS} - V_T\right)v_{DS} - v_{DS}^2\right]$$

Triode or Ohmic region

$$v_{DS} = \left(v_{GS} - V_T\right)$$

$$I_D = k\left(v_{GS} - V_T\right)^2$$

Saturation region

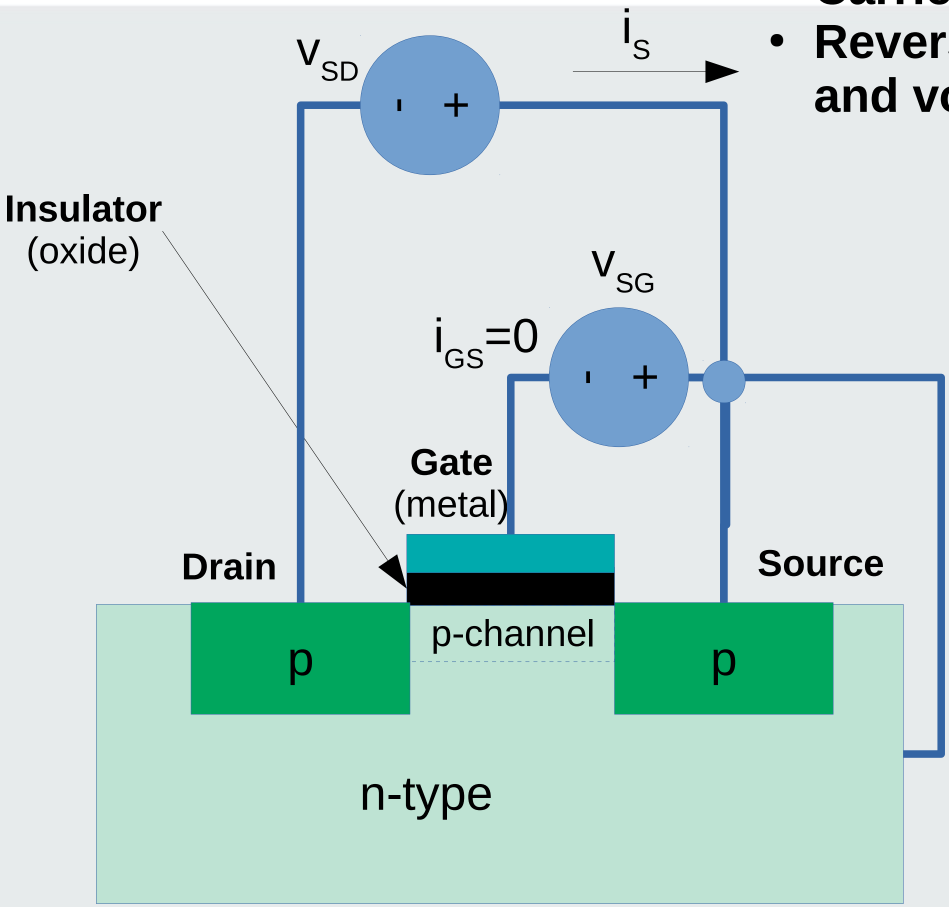


$$k = \frac{1}{2}\mu C_{ox}\frac{W}{L} \quad \left[AV^{-2}\right]$$

μ:	Carrier mobility
C_{ox}:	Oxide layer capacity
W:	Channel effective width
L:	Channel effective length

The p-channel MOSFET

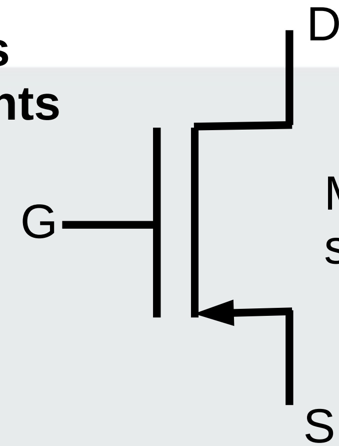
- **Carriers are holes**
- **Reverse all currents and voltages**



$i_D \rightarrow i_S$

$v_{GS} \rightarrow v_{SG}$

$v_{DS} \rightarrow v_{SD}$

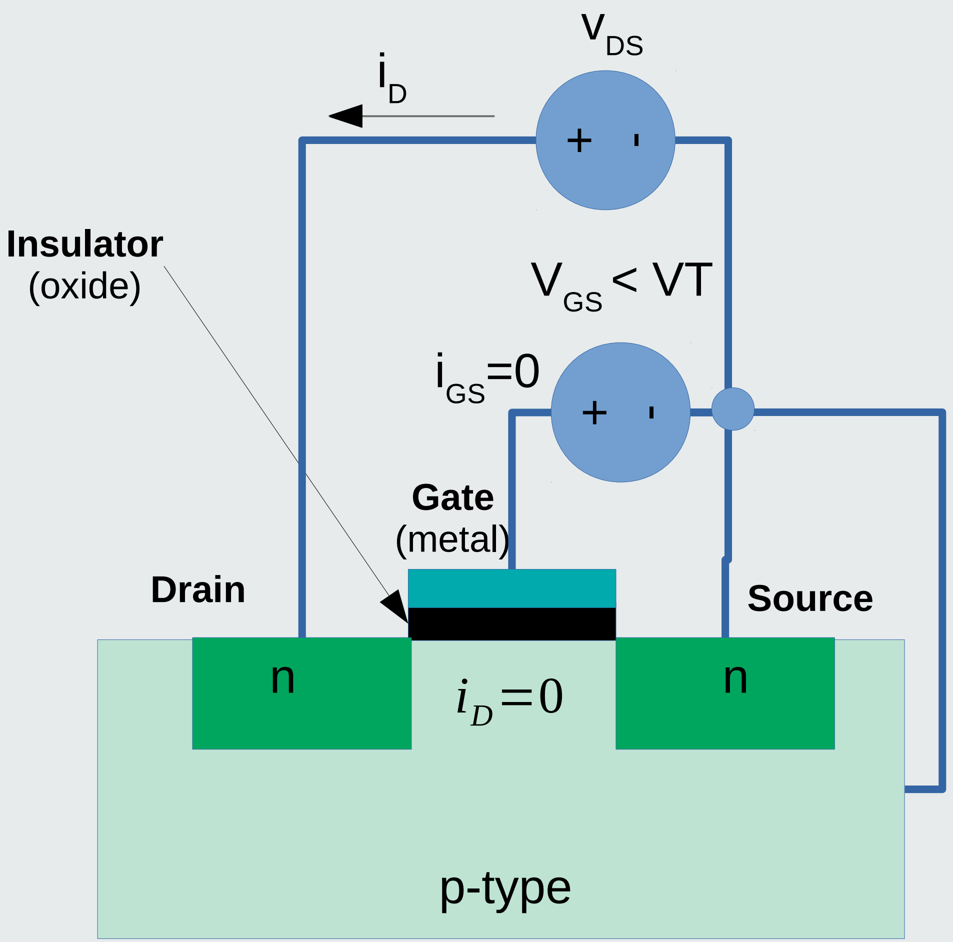


MOSFET symbol

$I_S=0$	Cut-Off
$I_S=k[2(v_{SG}-V_T)v_{SD}-v_{SD}^2]$	Triode
$I_S=k(v_{SG}-V_T)^2$	Saturation

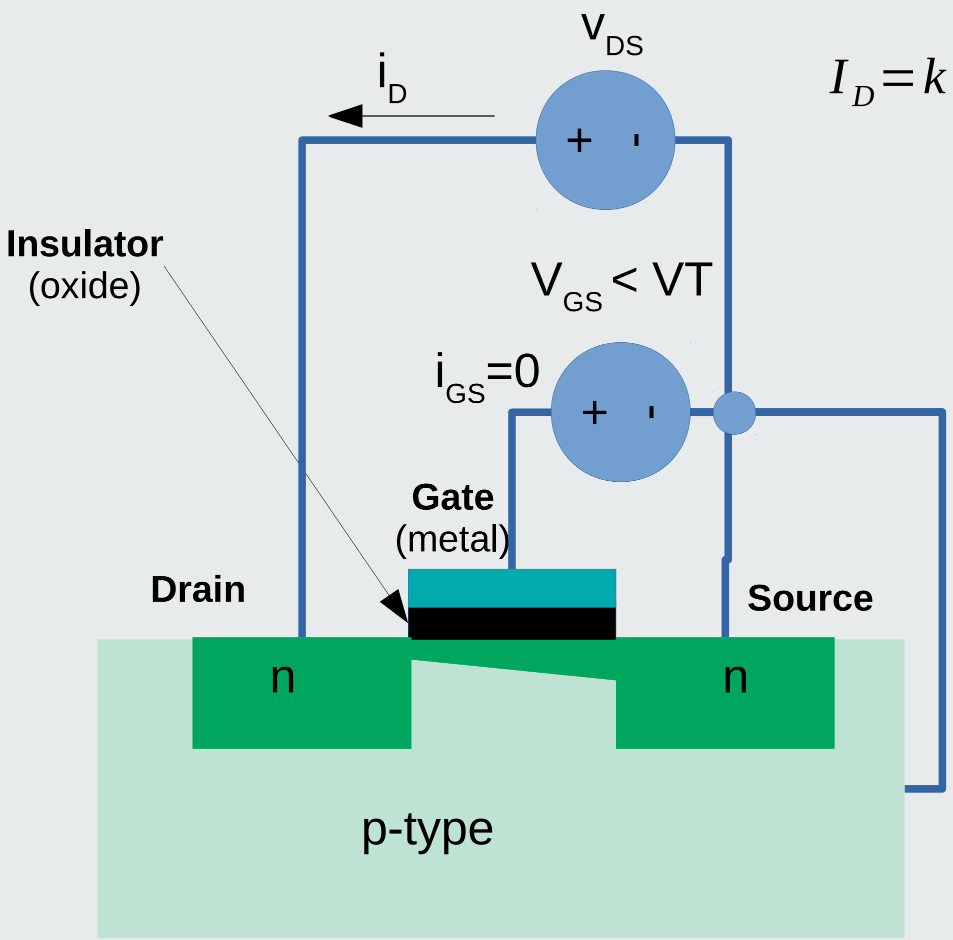
$$k=\frac{1}{2}\mu C_{ox}\frac{W}{L} \quad [AV^{-2}]$$

The MOSFET cut-off region – no channel



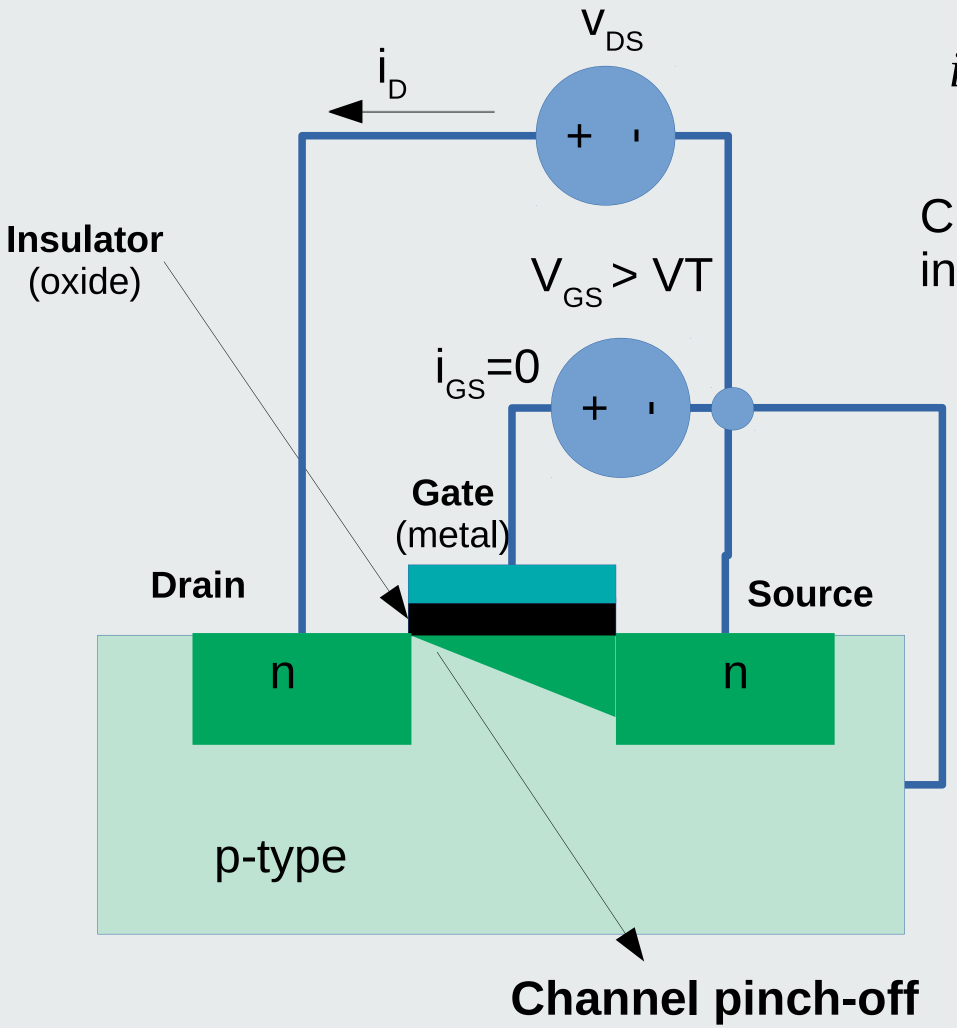
The MOSFET triode region – channel present

$$I_D = k\left[2\left(v_{GS} - V_T\right)v_{DS} - v_{DS}^2\right]$$



Channel also called Inversion region (from p to n)

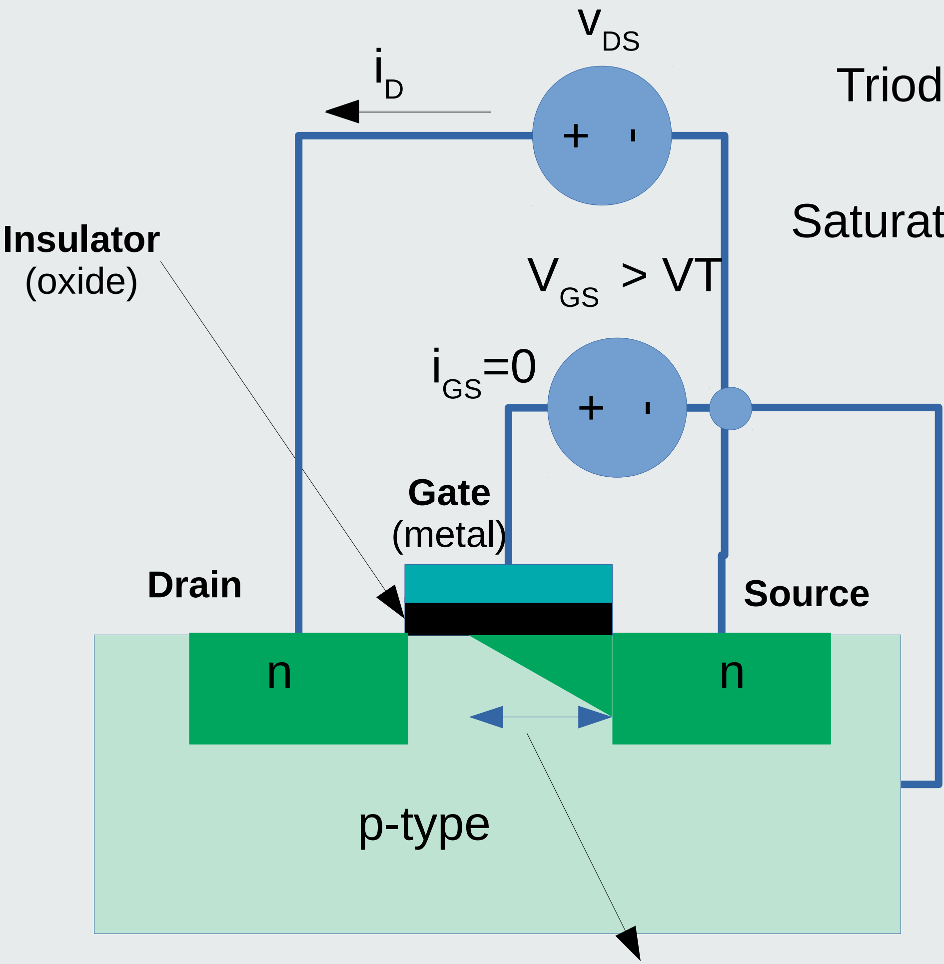
The MOSFET saturation region – channel pinch-off



$$i_S = k\left(v_{GS} - V_T\right)^2$$

Current no longer increases with V_{DS}

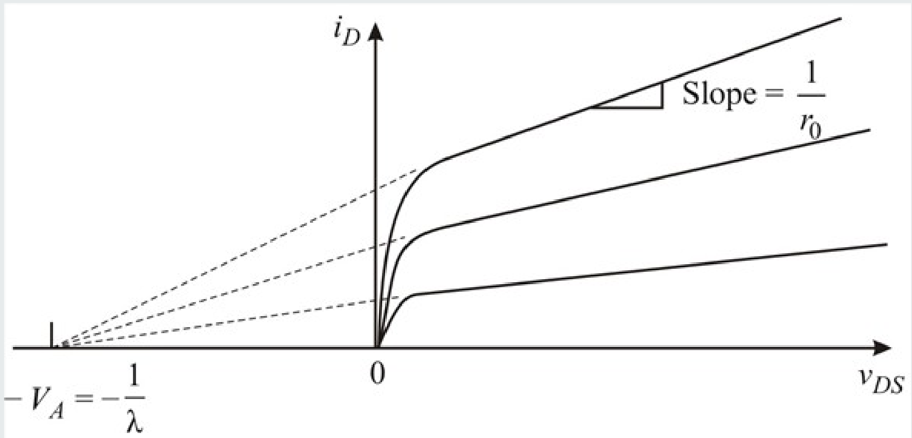
The MOSFET in saturation – channel length modulation



Triode $I_D = k[2(v_{GS} - V_T)v_{DS} - v_{DS}^2]\boxed{(1+\lambda V_{DS})}$

Saturation $I_D = k(v_{GS} - V_T)^2(1+\lambda V_{DS})$

λ: Channel modulation parameter

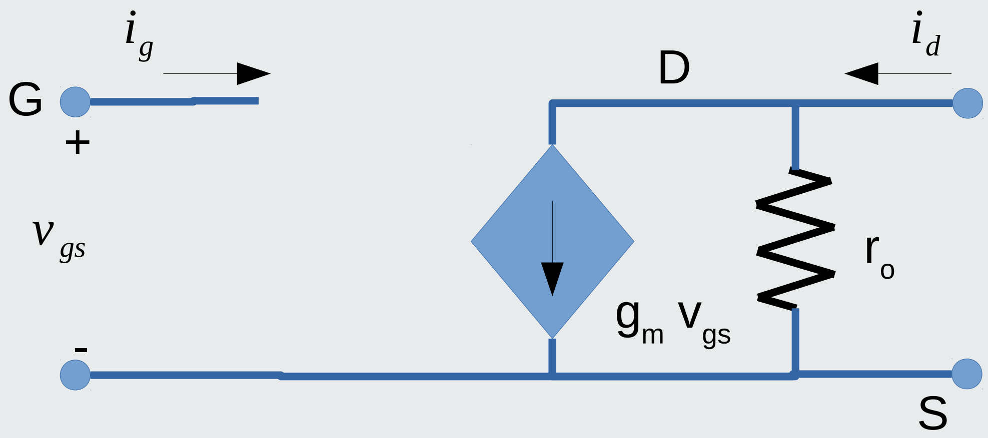


Similar to Early effect in BJTs: $V_A \leftrightarrow \lambda^{-1}$

Channel effective length shortens with V_{DS}

MOS transistor small signal model (AC)

Saturation region ONLY



$$g_m = \frac{\partial i_D}{\partial v_{GS}} = \frac{2 I_D}{V_{GS} - V_T}$$

$$r_o = \frac{\partial v_{DS}}{\partial i_D} = \frac{1 + \lambda V_{DS}}{\lambda I_D} \approx \frac{V_A}{I_D}$$

Nice feature:
Infinite input impedance!

Incremental parameters

g_m	Transconductance
r_o	Output impedance

Spice's MOS model

- Ngspice has very sophisticated MOS models
- Let's consider a reduced parameter set one
  - Level=1
  - Gamma= 0
  - Xj=0
  - Tox=1200n
  - Phi=.6
  - Rs=0
  - Kp=111u
  - Vto=1.4
  - Lambda=0.01
  - Rd=0
  - Cbd=2.0p
  - Cbs=2.0p
  - Pb=.8
  - Cgso=0.1p
  - Cgdo=0.1p
  - Is=16.64p N=1
- Check out l18.net: simulates $I_D(v_{DS})$ for constant v_{GS} using DC analysis (DC sweep) for a real commercial discrete MOS transistor: the CD4007

BJT versus MOS

Parameter	BJTs	MOS
Gain	High *	Medium
Input impedance	Low	High * (no gate current)
Output impedance	Low *	Medium
Size	Large	Small *
Cost	High	Low *
Power consumption	High	Low*

* is advantage

The table explains

why MOS rules!

Conclusion

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