TÉCNICO LISBOA

Microelectronics

Lab 4

Cascode current mirror design

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Group 4
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1 Introduction [1][2][3][4]

In this laboratory assignment, the main objective is to design and characterize a **cascode current mirror** and a **low voltage cascode current mirror**, using four nMOS transistors in each one and by resorting to the software Virtuoso (version 6.1.7). In order to achieve this, the libraries `4thlab` and `4thlab_sim` were created, while the library `3rdlab` from the previous laboratory assignment was also used (the library `3rdlab_sim` was also included here). As shown in Table 1, the cells `currentmirror_cascode` and `currentmirror_cascode_low_voltage` contain the views `schematic` and `symbol`. The cells with the same name on the library `4thlab_sim` can be used to run DC sweep simulations of the drain voltage of the transistor in which the output current (I_{out}) is measured. The DC sweep will be made from 0 to $3.3V$, in order to obtain the variation of the output current for different values of this voltage V_D. The voltages on the gates (G), sources (S) and drains (D) of the different transistors will be plotted as well. This study will serve as a comparison, not only between the cascode and low voltage cascode current mirror, but also regarding the current mirror designed in Lab 3.

Library	Cell	View
3rdlab	currentmirror	schematic
		symbol
3rdlab_sim	currentmirror	iout_vds
4thlab	currentmirror_cascode	schematic
		symbol
	currentmirror_cascode_low_voltage	schematic
		symbol
4thlab_sim	currentmirror_cascode	iout_vd
		iout_vd_all_schematics
	currentmirror_cascode_low_voltage	iout_vd

Table 1: Libraries, cells and views created in Virtuoso

Cascode current mirror and low voltage cascode current mirror

In this laboratory assignment, the focus is, once again, the use of nMOS transistors as **current sources**. Therefore, the base principles described in the previous report also apply here. The **drain current** of an nMOS transistor in the **saturation region** (in which $V_{GS} \geq V_{TH}$ and $V_{DS} \geq V_{GS} - V_{TH}$) can be given by equation 1. One of the main objectives of the previous laboratory assignment was to study the effect of the **channel-length modulation** (CLM). In this report, the advantages of the cascode current mirror regarding this aspect will be discussed. Taking this phenomenon into account, the drain current in an nMOS transistor is instead given by equation 2, where λ is the channel-length modulation parameter. In both equations, the parameters μ and C_{ox} are the mobility of carriers (in this case, electrons) and the oxide layer capacity, whereas W and L are the channel width and length of the transistor, respectively. On the other hand, in the cut-off region, $I_D = 0$ and $V_{GS} < V_{TH}$; in the triode (or ohmic) region, $V_{GS} \geq V_{TH}$ and $V_{DS} < V_{GS} - V_{TH}$. The transition between the triode and saturation regions in an nMOS transistor happens when its respective voltage between drain and source is given by $V_{DS} = V_{GS} - V_{TH} \equiv V_{OD}$ (overdrive voltage).

$$I_D = \frac{\mu C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH})^2 \tag{1}$$

$$I_D = \frac{\mu C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH})^2 \cdot (1 + \lambda V_{DS}) \tag{2}$$

As seen in equation 2, the current in saturation becomes dependent on V_{DS} (as it increases, so does I_D). The purpose of a **cascode current mirror** is to mitigate this effect. In order to do this, one should start from the basic current mirror, in which the transistor whose drain current is the reference current I_{REF} is called $\boldsymbol{M_1}$ and the transistor whose drain current is the output current I_{out} is designated as $\boldsymbol{M_2}$. To reduce the impact of CLM, $V_{DS_1} = V_{DS_2}$ should be verified and remain as constant as possible - a single cascode device is implemented, which shields the current source, thus reducing the voltage variations across it. This is achieved by placing another nMOS transistor ($\boldsymbol{M_3}$) with its drain connected to I_{out} and its source to the drain of transistor $\boldsymbol{M_2}$ (as shown in Figure 1). This channel-length modulation mitigation condition (i.e., V_{DS} being the same on both transistors M_1 and M_2) can also be written by using other voltages in the transistors (shown in Figure 1):

$$\boldsymbol{V_{S_3}} = V_{DS_2} = V_{DS_1} = \boldsymbol{V_{GS_1}} \Leftrightarrow V_{G_3} - V_{GS_3} = V_{GS_1} \Leftrightarrow \boldsymbol{V_{G_3}} = \boldsymbol{V_{GS_3}} + \boldsymbol{V_{GS_1}} \tag{3}$$

To guarantee this, another nMOS transistor ($\boldsymbol{M_0}$) is placed in such a way that its drain current is

I_{REF} and its source is connected to the drain of $\boldsymbol{M_1}$; this allows the conditions given in (4) to be verified and thus the structure of a cascode current mirror is obtained [1].

$$V_{GS_0} + V_{GS_1} = V_{GS_3} + V_{GS_2} \Leftrightarrow V_{GS_0} + V_{GS_1} = V_{GS_3} + V_{GS_1} \Leftrightarrow \boldsymbol{V_{GS_0} = V_{GS_3}} \quad (4)$$

In a **cascode current mirror**, the reference current I_{REF} is applied in the drain of M_0. Since, in an nMOS transistor, the gate current is given by $I_G \approx 0$, the drain current in M_1 will also be I_{REF}. This will generate a voltage drop V_{GS_1} in transistor M_1 which will be the same as the one on V_{GS_2}, since the gates of M_1 and M_2 are shorted to each other and their sources are at $0V$. In turn, in the saturation region, a current with a value very similar to I_{REF} (and given by equation 2) will appear across M_2. The current I_{REF} will define voltages V_{GS} in such a way that M_0 and M_1 work in the saturation region, thus the relation $V_{GS} = V_{TH} + V_{OD}$ will be valid for each of these transistors. On the other hand, the voltage drops across M_2 and M_3 will be defined in order to have an output current of $I_{out} = I_{REF}$. However, a minimum applied voltage in the drain of M_3 is obviously required; as this input voltage V_{D_3} increases, the voltage drop V_{DS_3} will thus have to change significantly (because $V_{DS_1} \approx V_{DS_2}$ will be approximately constant) - this will be analysed in this laboratory assignment. Since the gates of M_3 and M_0 are shorted to each other and $V_{GS_1} = V_{DS_1} = V_{TH} + V_{OD}$ (because the drain and gate of M_1 are connected), the voltage drop V_{DS_2} will have this value. With this in mind, and knowing that $V_{DS} = V_{OD}$ is the condition at which M_2 and M_3 enter the saturation region, it is possible to infer that **the voltage at the drain of $\boldsymbol{M_3}$ must be at least $\boldsymbol{V_{TH} + 2V_{OD}}$**. The mentioned voltages and voltage drops are represented in Figure 1.

The cascode current mirror described above will decrease the impact of CLM, since V_{DS_2} will be (approximately) constant. However, this advantage can be maintained while requiring a lower minimum voltage V_{D_3} in order for M_3 and M_2 to enter the saturation region. This new design which allows **operation with lower voltages** is also shown in Figure 1, as well the respective voltages and voltage drops. Once again, the reference current I_{REF} defines $V_{GS_1} = V_{GS_2}$ in order for M_1 to work in saturation; however, V_{D_0} is now lower than before, since an external voltage designated as V_{casn} is applied; having a minimum value of $\boldsymbol{V_{casn} = V_{OD} + V_{GS_0}}$, it guarantees that M_0 and M_1 work in the saturation region. Again, because the gates of M_1 and M_2 are shorted to each other, a current very similar to I_{REF} will flow through M_2 when in saturation. Once the voltage V_{D_3} reaches $\boldsymbol{2V_{OD}}$, the transistors M_2 and M_3 will also work in the saturation region - since V_{D_2} has decreased from the former design, the minimum applied voltage is also lower. Once again, V_{DS} is (approximately) the same on M_1 and M_2, thus V_{DS_3} will have to change as V_{D_3} increases.

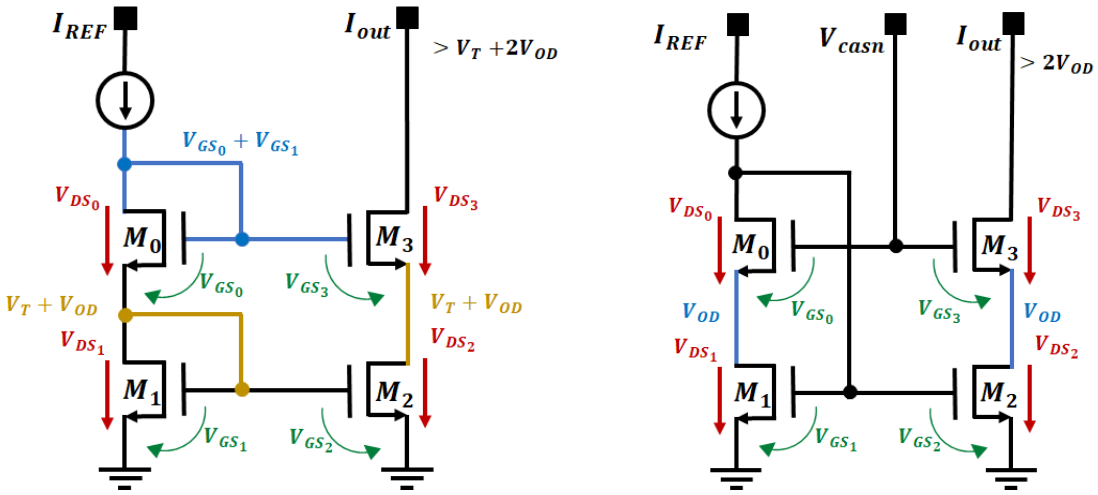

Figure 1: Designs of a cascode current mirror [on the left] and a low voltage cascode current mirror [on the right]. In both, the designations of the transistors are indicated, as well as the voltage values in their gates, sources and drains. The threshold voltage $V_T \equiv V_{TH}$ refers to the transistors M_1 and M_2, since this parameter will be higher for M_0 and M_3, which suffer from body effect.

Body effect

For an nMOS device, the **threshold voltage increases when the source is at a higher voltage than the body**. This change in threshold voltage is due to the **body effect**. In many applications, the source terminal is connected to the substrate (or body) terminal B. In integrated circuits, however, the substrate is usually common to many MOS transistors. In order to maintain the cutoff condition for all the substrate-to-channel junctions, the substrate is usually connected to the "most negative" power supply in an nMOS circuit (the most positive in a pMOS circuit). The resulting reverse-bias voltage between source and body (V_{SB} in an n-channel device) will have an effect on device operation. As the source potential rises above the bulk (substrate) potential, electrons are attracted towards the positive terminal of V_{SB} from the MOSFET's channel. To keep the surface inverted, a larger V_{GS} must be applied to the MOSFET. Thus, the effect of V_{SB} on the channel can be most conveniently represented as a change in the threshold voltage V_{TH}. Specifically, it has been shown that increasing the reverse substrate bias voltage V_{SB} results in an increase in $V_{TH} \equiv V_T$ according to equation 5, where V_{TH_0} is the threshold voltage for $V_{BS} = 0$, ϕ is the strong inversion surface potential (typical value of $\phi = 0.6V$) and γ is the body-effect parameter (it has the dimension of $\sqrt{V}$ and is typically $0.4V^{1/2}$ for the nMOS) [2].

$$V_{TH} = V_{TH_0} + \gamma \left[\sqrt{\phi + V_{SB}} - \sqrt{\phi} \right] \tag{5}$$

2 Cascode current mirror designs and simulation

In order to compare the current mirror with the cascode current mirrors, the views `schematic` and `symbol` from the cell `currentmirror` and library `3rdlab` were copied into a directory created for this laboratory assignment. The design of this current mirror with two nMOS transistors was presented and discussed in the report for the third laboratory assignment, thus it will not be repeated in detail here. Having done this, the library `4thlab` was created, in which the views `currentmirror_cascode` (for the **cascode current mirror**) and `currentmirror_cascode_low_voltage` (for the **cascode current mirror** which allows operation with **low voltage**) are present. In each cell, the views `schematic` and `symbol` were created.

In the schematic of the cascode current mirror, two transistors with lengths $L = 1\mu m$ and width $W = a \cdot L$ were added at the bottom - these are the nMOS transistors which will be designated as M_1 and M_2 throughout this report. This length L was chosen in order to limit the effect of the channel-length modulation. As it was seen in the previous laboratory assignment, by increasing L, the value of the channel-length modulation parameter λ decreases; however, after a certain L is reached, a further decrease will not change the impact of this phenomenon significantly. In Lab 3, it was seen that $L = 1\mu m$ was an acceptable value for the length of the channel in order to have a small enough impact. On the other hand, the value of the parameter '`a`' was also defined in the previous report. The experimental value (from the first laboratory assignment) of $\mu C_{ox} \approx 73.990\mu A/V^2$ is considered; the input current is $I_{REF} = 10\mu A$ (the output current I_{out} will also have this value in a certain point, since a current mirror is being studied) and the **overdrive voltage** is chosen to be $V_{OD} = V_{GS} - V_{TH} = 0.2V$. The value of the current in saturation increases with V_{GS}, but this higher voltage also means that the transistor works as a current source for a smaller range of V_{DS} (saturation range). On the other hand, a smaller value increases the sensitivity to V_{TH} - thus the usual design criteria of defining $V_{OD} = 200mV$ [4]. Taking all this into account, by using equation 1, the following ratio (designated as a) was defined:

$$\frac{W}{L} = \frac{2 \cdot I_{ref}}{\mu C_{ox} \cdot V_{OD}^2} \equiv a \approx \textbf{6.758} \tag{6}$$

The parameter '`a`', as well as '`L`', are set as variables in the schematic and their values will be selected once the simulation is to be done. The bulk of all transistors is connected to ground; since the sources of the transistors in the bottom (M_1 and M_2) are also connected to ground, the respective bulks were connected to the sources. Moreover, the gates of M_0 and M_3 were shorted

to each other (and to the drain of M_0), as well as the gates of M_1 and M_2 (and the source of M_0/drain of M_1). Besides the instances `gnd` from library analogLib, the pins `Iref` (input) and `Iout` (inputOutput) were added, in order to connect the constant current source to the drain of M_0 and the voltage source to the drain of M_3 (respectively). The designs are shown in Figure 2.

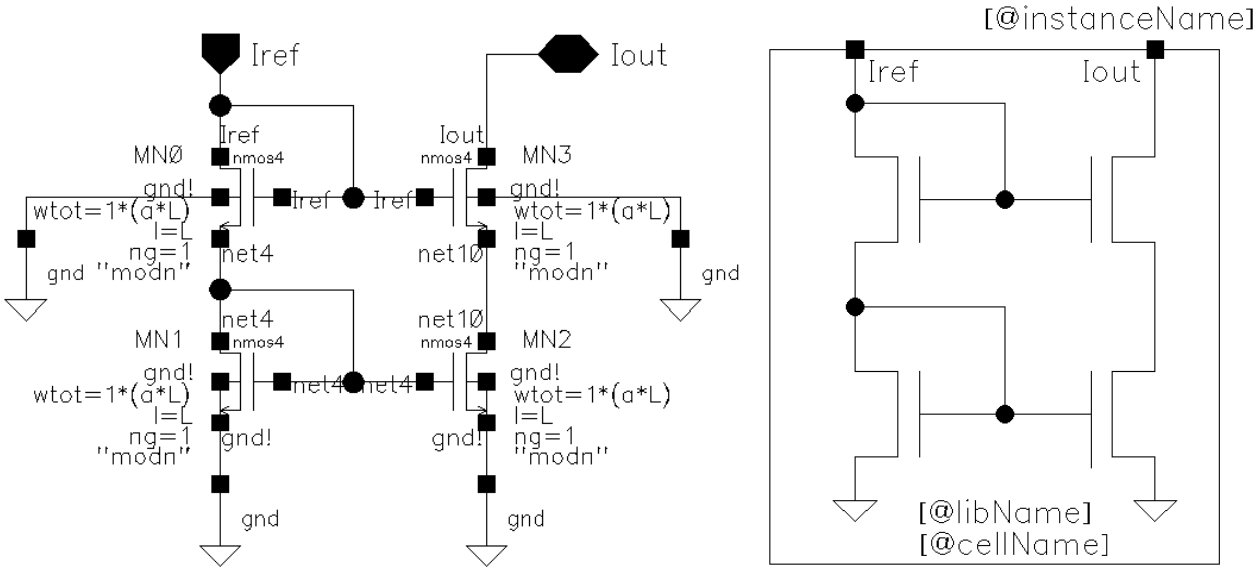

Figure 2: Views `schematic` [on the left] and `symbol` [on the right] (Cell `currentmirror_cascode`, Library `4thlab`), regarding the cascode current mirror.

Subsequently, the designs shown before were changed in order to allow operation with low voltage. In this case, the drain of M_0 is shorted to the gates of the nMOS transistors on the bottom, while an input pin `vcasn` was connected to the gates of M_0 and M_3, in order to later connect there a voltage source in the circuit. The views for this new cascode current mirror are shown in Figure 3.

It is worth noting that, throughout this report, the transistors designated by M_i ($i \in \{0, 1, 2, 3\}$) in Figure 1 correspond to the respective `MNi` transistors shown in Figures 2 and 3. Moreover, the designations V_{D_i}, V_{S_i} and V_{G_i} refer to the drain, source and gate voltages in the same transistors, respectively.

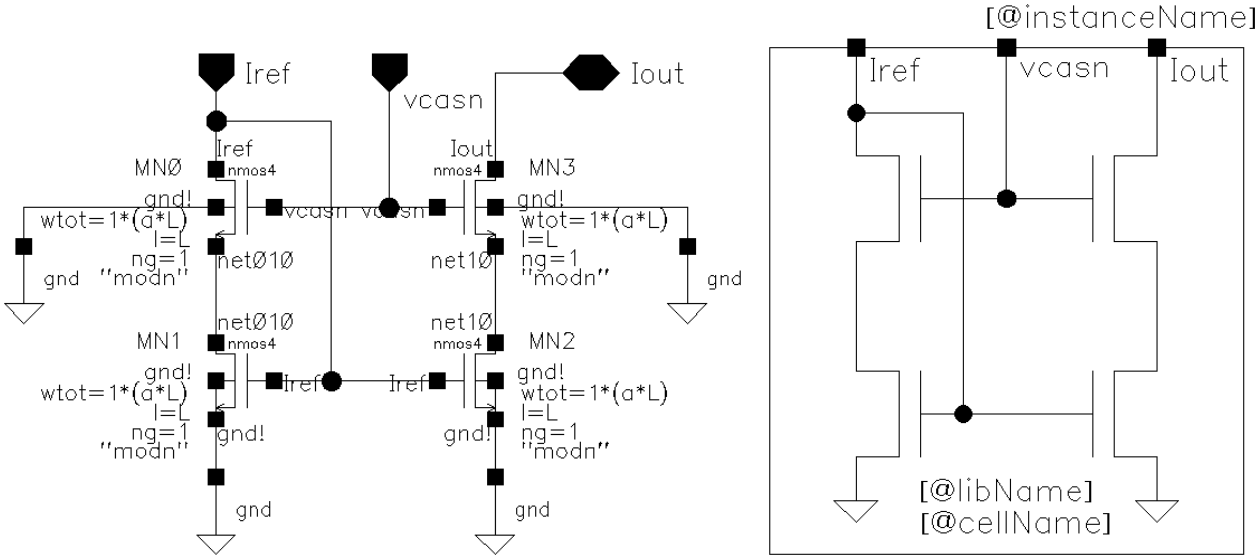

Figure 3: Views `schematic` [on the left] and `symbol` [on the right] (Cell `currentmirror_cascode_low_voltage`, Library `4thlab`), regarding the cascode current mirror which allows operation with low voltage (here, the pin `vcasn` is present).

In order to simultaneously run a simulation for all current mirror designs, the view `iout_vd_all_schematics` in cell `currentmirror_cascode` and library `4thlab_sim` was created. In the same cell, the view `iout_vd` can be used to run the simulations only for the design in `currentmirror_cascode`; moreover, the view with the same name in cell `currentmirror_cascode_low_voltage` can be used to run the simulations only for the respective low voltage cascode current mirror design and the view `iout_vds` in `3rdlab_sim` for the current mirror designed in Lab 3. These last three views were not used in this laboratory assignment to obtain any plots nor values, thus they are not shown in this report. Contrarily, the circuit in cell `iout_vd_all_schematics` is shown in Figure 4. Here, the symbols for all current mirror designs are included. A separate constant current source (instance `idc` from analogLib) with a current value of $10\mu A$ was connected to each pin `Iref`. Moreover, a voltage source (instance `vdc` from analogLib) was connected to all `Iout` pins; the value of $3.3V$ is shown in Figure 4, although the value of this drain voltage V_D will be swept from 0 to $3.3V$ in the simulations. Finally, another voltage source was connected to the pin `vcasn` of the low voltage cascode current mirror in the bottom; the voltage value is set as a variable with the same name.

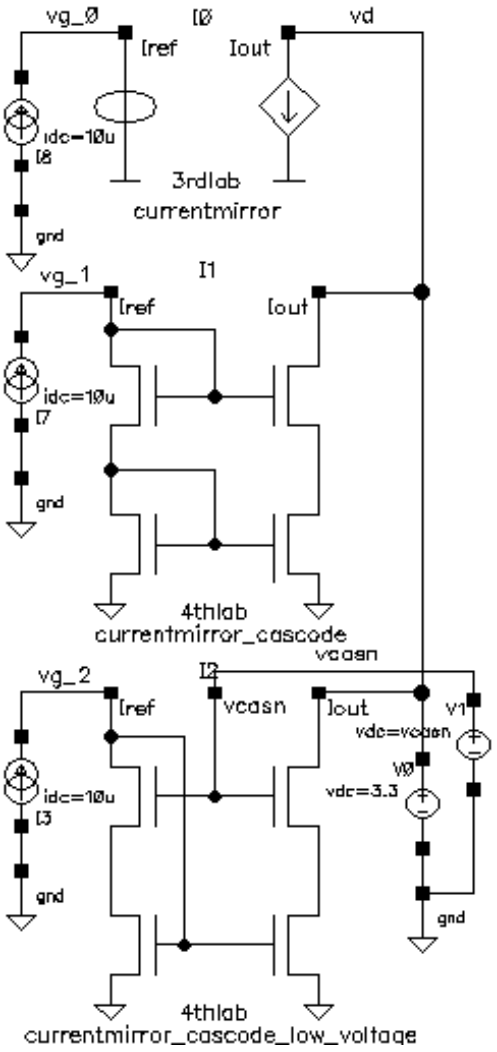

Figure 4: Circuit for simulation in View `iout_vd_all_schematics` (Cell `currentmirror_cascode`, Library `4thlab_sim`).

The first experimental results to be obtained are the curves $\boldsymbol{I_{out}(V_D)}$, which describe the change in the output current (measured in the drains of the transistors M_3 of the cascode current mirrors) due to the change in V_D (applied in these drains). To do this, the ADE L was launched in Virtuoso. The variables' values were defined as $a = 6.758$, $L = 1\mu m$ (these two have been explained above) and $vcasn = 1V$. The latter was defined because the minimum value of $vcasn$ should be equal to $2V_{OD}+V_{TH}$, as described in section 1. The overdrive voltage was defined as $0.2V$ and the threshold voltage in the datasheet [5] has a value of $V_{TH} = 0.46V$ for transistors with long channels (a better approximation for the V_{TH} with $L = 1\mu m$ rather than the threshold voltage for short channels, also shown in the datasheet). However, due to the body effect (described in section 1) which occurs in transistors M_0 and M_3, V_{TH} should increase to about $0.6V$ (the exact value will be obtained in this report), thus `vcasn` was defined as $V_{casn} = 2V_{OD} + V_{TH} = 1V$.

Having written these values, a DC analysis was selected, in which `vd` has a swept range of 0 to $3.3V$ and a step size of $0.025V$ was selected (in the swept type Linear), in order to minimize "discontinuities" in the curves. After selecting as outputs the currents `Iout` of all current mirrors, the results shown in Figure 5 were obtained. The dotted lines represent the minimum V_D for each case in order to keep the transistors in the respective devices in the saturation region. From analysing the plots, it can be concluded that the graph for the **current mirror** developed in the previous laboratory assignment (red curve) clearly has the **highest slope** in saturation. This is because, in that design, as the applied V_D increased, the voltage drop $V_{DS} = V_D$ also increased in the same manner. This does not occur with the cascode current mirrors, because the source voltage in M_3 is not connected to ground; in this case, even though the increase in the applied V_D leads to an increase in V_{DS_3}, this variation is not as significant, because $\boldsymbol{V_{D_3}}$ **also increases (slightly)**, as will be proved further ahead - moreover, the threshold voltage V_{TH_3} is larger, because M_3 suffers from body effect, thus reducing the slope given by equation 2 (and there could also be some slight decreases in V_{G_3} to compensate for the increase in V_{D_3}, in the case of the cascode current mirror without V_{casn}).

Another significant difference between the curves is the voltage at which the saturation region is reached. It is concluded that one big advantage of the simpler current mirror (red curve) is that the **saturation range** is bigger, especially regarding the cascode current mirror (green curve). Even though this V_D is still larger for the blue curve, the difference in this case is not as significant. Moreover, even though the impact of CLM is slightly higher for the latter (when compared with the green curve), it is still clearly much less significant than for the red curve. This would suggest, therefore, that the low voltage cascode current mirror would be the most optimized design for most applications. One considerable disadvantage, however, is that the external **voltage V_{casn} needs to be generated**; however, even when many of these devices are used, this only needs to happen once - the same V_{casn} is used in various low voltage cascode current mirrors.

Another thing to notice in Figure 5 is that the red curve stands above all others in the initial and final portions. Initially, it happens because it reaches saturation first, thus the increase in I_{out} towards $10\mu A$; for higher V_D, this happens because of the more significant impact of the channel-length modulation. The blue curve crosses the green curve before $V_D = V_{OD}$ because, even though the cascode current mirror enters the saturation region for a larger V_D, its CLM impact is even lower, thus its values of I_{out} remain below the others.

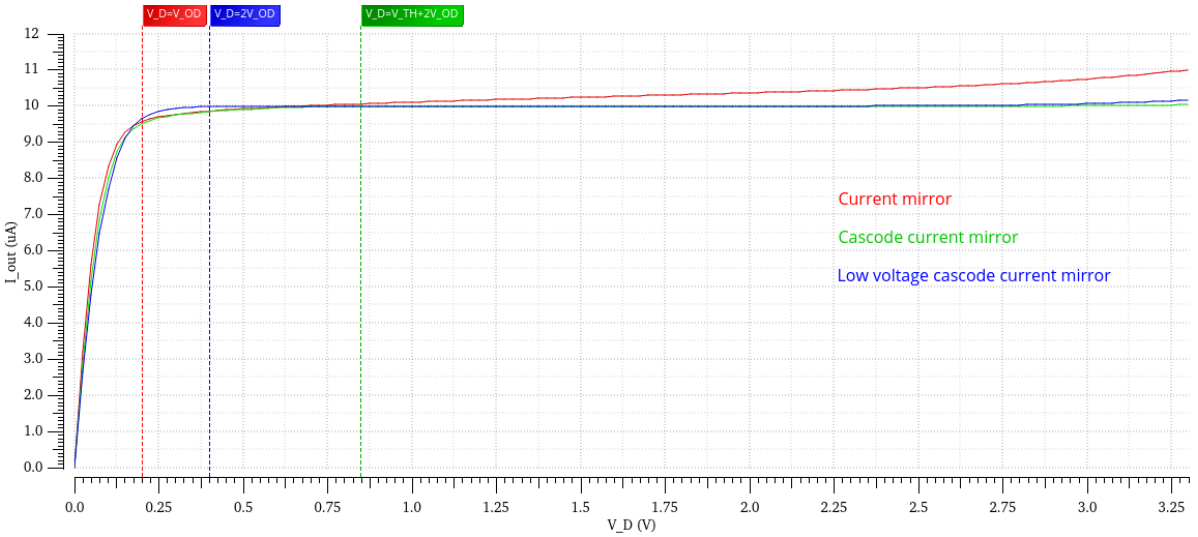

Figure 5: Curves $I_{out}(V_D)$ obtained by running a simulation in Virtuoso with the view shown in Figure 4. By sweeping V_D in a DC analysis from 0 to $3.3V$, the output current was obtained for the three different current mirror designs. The vertical markers indicate the points in which the respective saturation region is reached; here, $V_{OD} = 0.2V$ and $V_{TH} = 448.27mV$ (the latter for the cascode current mirror and due to the analysis made further ahead alongside Figure 6).

Using the plots shown above, the values of V_D and I_{out} in different points were obtained and are shown in Table 2. Here, it can be seen that the highest I_{out} relative difference with respect to $I_{REF} = 10\mu A$, at $V_D = 3.3V$ (the maximum voltage the technology used in Virtuoso can endure), occurs for the first current mirror - the difference is of 9.7 and 8.4 percentage points between this case and the cascode current mirror and low voltage cascode current mirror, respectively. However, the difference is only of 1.3 percentage points between the two cascode current mirrors. Regarding the values of $V_D(I_{out} = 10\mu A)$, the comparisons are similar to those indicated for V_D in which the saturation region begins. The difference between this voltage for the first and third devices (in the order of Table 2), relative to the former, is only of about 0.4%. For the second case, however, $I_{out} = 10\mu A$ is only reached at $V_D = 1.510V$; this is not only due to the higher V_D for which saturation is reached, but also because of the very low impact of CLM - I_{out} will be very close to $10\mu A$ for most V_D values. In fact, the relative I_{out} differences shown in Table 2 are always lower (in absolute value) for the cascode current mirror. It is worth noting that the threshold voltage value $V_{TH} = 448.27mV$, necessary to know the voltage value $V_D = 2V_{OD} + V_{TH}$ in which this device enters the saturation region, has been obtained in this report further ahead. From Table 2, we can also conclude that

$\boldsymbol{V_{GS} = 668.350mV}$ for the current mirror design of Lab 3, since, as discussed in the previous laboratory assignment, the currents I_{out} and I_{REF} are only the same when $V_D = V_{GS}$ (due to the channel-length modulation effect given in equation 2).

Schematic	V_D (V)	I_{out} (μA)	I_{out} difference (%)
Current mirror	0.2	9.569	-4.3
	668.350×10^{-3}	10	-
	3.3	11.008	10.1
Cascode current mirror	848.270×10^{-3}	9.998	-0.02
	1.510	10	-
	3.3	10.043	0.4
Low voltage cascode current mirror	0.4	9.991	-0.09
	670.876×10^{-3}	10	-
	3.3	10.169	1.7

Table 2: Values of V_D and I_{out} for certain points in the curves shown in Figure 5. For each schematic, the first row refers to the condition in which the transistor reaches the saturation region (at $V_D = V_{OD},\ V_{TH} + 2V_{OD}$ or $2V_{OD}$, respectively); the second row shows the voltage V_D at which $I_{out} = I_{REF} = 10\mu A$; the final row indicates the current values at $V_D = 3.3V$. The last column is given by $(I_{out} - 10\mu A)/(10\mu A)$ $(\%)$.

Additionally, in order to further quantify the impact of channel-length modulation, ten points in the saturation region for each curve were selected; these values were fit to equation 2 using Fitteia, a web-based fitting platform - the results are shown in Table 3. The values of V_D were considered until $2.7V$ since, for larger values of this voltage, the linear equation did not fit the points as well - this is due to the closer proximity to the maximum voltage value of $3.3V$, in which the bigger than expected current variation is not predicted by the analytical model presented in section 1.

By analysing Table 3, it can be seen that the **slope is higher for the current mirror**; in this device, the slope has the order of magnitude of $10^{-1}\mu A/V$, two orders of magnitude higher than in the other cases. In fact, the relative difference is of about 99.4% and 98.1%, when compared to the cascode current mirror and the low voltage cascode current mirror, respectively. Once again, this shows that the impact of the CLM is considerably higher for the basic current mirror and not as different between the cascode current mirrors.

Another important thing to conclude is the reason why the **slope is slightly larger for the low voltage cascode current mirror**, when compared to the other cascode currrent mirror (even though they have the same order of magnitude, the former is about 3 times higher). This happens because, as it is shown in Figure 3, the **gate voltage of transistor M_3** has a **constant** voltage value $V_{G_3} = \boldsymbol{V_{casn}}$, since the external constant voltage source V_{casn} is included. The voltage at the drain of M_2 (which is also the source of M_3) increases slightly, as the externally applied V_D increases, which leads to a lesser increase in V_{DS_3} and a lower impact of CLM - thus, the output current's value stays closer to the desired $I_{out} = 10\mu A$. However, the increase in V_D can also be compensated by (small) decreases in V_{G_3}, which, in turn, reduce V_{GS_3} and the slope of the drain current of transistor M_3, given by equation 2. However, this **cannot happen when $\boldsymbol{V_{casn}}$** is present, leading to slightly larger increases in V_{DS_3} and a higher slope given by equation 2. The fact that this increase in V_{DS} and decrease in V_{GS} lead to a more stable current around $10\mu A$ could also be explained graphically. As studied before [4], as this variations occur, the curves $I_D(V_{DS})$ of an nMOS transistor shift downwards. What happens here is that these successive variations "counteract" the effect of the channel-length modulation and make I_{out} closer to $10\mu A$ as V_D increases, by "lowering" the curves.

In order to further analyse the cascode current mirrors, two other similar simulations were run. The plots shown in Figure 6 were obtained by selecting the wires `Iref`, `net4` and `net10` (shown in Figure 2) as outputs. On the other hand, the results in Figure 7 were obtained by selecting the wires named `Iref`, `net010` and `net10` (in Figure 3) as outputs. By doing this, the voltage values in

the drains, sources and gates of the transistors which are not controlled in the simulation (those who are not $0V$, V_D swept in the simulations nor `vcasn`) are obtained for different values of V_D. The analysis of these results will be made below.

Schematic	V_D (V)	I_{out} (μA)	V_D (V)	I_{out} (μA)	g_{DS} $(\times 10^{-1} \mu A/V)$
Current mirror	0.8	10.048	1.8	10.322	2.692
	1.0	10.111	2.0	10.371	
	1.2	10.168	2.2	10.423	
	1.4	10.221	2.4	10.481	
	1.6	10.272	2.6	10.550	
Cascode current mirror	1.0	9.9994	2.0	10.000	0.016
	1.2	9.9997	2.2	10.000	
	1.4	9.9999	2.4	10.001	
	1.6	10.000	2.6	10.002	
	1.8	10.000	2.7	10.003	
Low voltage cascode current mirror	0.8	10.001	1.8	10.004	0.050
	1.0	10.002	2.0	10.006	
	1.2	10.002	2.2	10.007	
	1.4	10.003	2.3	10.008	
	1.6	10.004	2.4	10.010	

Table 3: Voltage and current values at ten different points (V_D, I_{out}) from each curve in Figure 5 and in the respective saturation regions, as well as the value of the slope $g_{DS} = \frac{\mu C_{ox}}{2} \cdot \frac{W}{L} \cdot V_{OD}^2 \cdot \lambda$ given by equation 2, obtained using Fitteia.

For the **cascode current mirror**, the voltage at the source of transistor M_0, which corresponds to $V_{OD} + V_{TH_1}$ according to the theoretical analysis, remains at the voltage value indicated in Figure 6 (green curve). Thus, an experimental value of $\boldsymbol{V_{TH_{1_{exp}}} = 448.27mV}$ is obtained (since $V_{OD} = 0.2V$), whose relative difference regarding the value $V_{TH_{tab}} = 0.46V$ given in the datasheet [5] is of about $\boldsymbol{-2.6\%}$. This close proximity was expected, taking into account that the transistor M_1 does not suffer from body effect - its bulk and source are connected to each other. For the same reason, this threshold voltage should also be valid for transistor M_2 (i.e., $V_{TH_1} = V_{TH_2}$).

The voltage for the blue curve, which corresponds to the drain voltage of transistor M_0 (shown in Figure 2) remained constant. Taking the theoretical analysis into account, it was expected that $V_D(MN0) = V_{GS_0} + V_{GS_1} = 2V_{OD} + V_{TH_0} + V_{TH_1}$. Using $V_{OD} = 0.2V$, $V_{TH_{1_{exp}}} = 448.27mV$ and the voltage value shown in the blue curve, the experimental value of $\boldsymbol{V_{TH_{0_{exp}}} = 661.23mV}$ is obtained. It differs in about 43.7% from the threshold voltage value $V_{TH_{tab}} = 0.46V$ given in the datasheet and 47.5% from $\boldsymbol{V_{TH_{1_{exp}}}}$. This higher experimental value for V_{TH_0} was expected, since the nMOS transistors M_0 and M_3 suffer from **body effect** (since their bulks are connected to ground, but not their sources, as explained in section 1). The change in the threshold voltage is given by equation 5 - in this case, since $V_{SB} > 0V$, it increases. Moreover, by checking that the voltage value of the blue curve remained constant (regarding only 4 decimal points), it is verified that, even though V_{G_3} variations could occur in order to "compensate" for the increase in V_D (as described before), these will not be very significant.

Regarding the source voltage in M_3, the results in Figure 6 show that it starts at $0V$ and increases until it reaches the source voltage of M_0. The **initial increase** occurs because the transistors M_2 and M_3 do not enter the saturation region until $V_{DS_2} = V_{D_2} = V_{OD}$ and $V_{DS_3} = V_{OD}$, respectively. It tends to the value of V_{D_1} due to the symmetry in voltages (and currents) described in section 1 for the cascode current mirrors. Moreover, as it was shown in Table 2, the output current I_{out} only reached $10\mu A$ at $V_D = 1.510V$; here, the same thing happens - the red curve shown below only crosses the green curve at this voltage value. This value is also extremely close to V_{D_0}, the voltage in the blue curve. This makes sense, taking equation 2 into account - the drain currents in transistors M_0 (the reference current I_{REF}) and M_3 (the output current I_{out}) will only be the same when $V_{D_0} = V_{D_3}$, since their gates are connected, their sources have approximately the same

voltage value and their threshold voltages should be the same (both suffer from body effect). Finally, even though V_{D_2} remains approximately constant in saturation, there is still a **small slope** - at $V_D = 3.3V$, it reaches $670.870mV$, which is 0.4% higher than the voltage for the green curve. As explained before, this is what allows the channel-length modulation to have a certain impact. As V_D increases, there is still some increase in the drain voltage of M_2, which leads to the increase in I_D seen in Figure 5, due to equation 2.

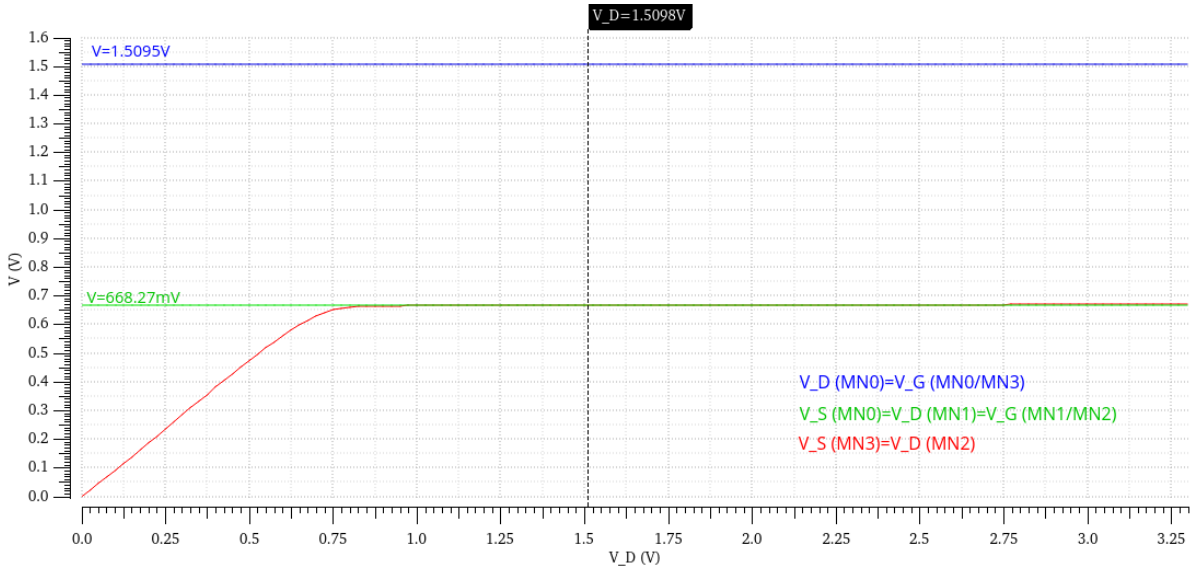

Figure 6: Voltage values at the drain, source and gate of different transistors shown in Figure 2 (cascode current mirror). The DC simulation was made by sweeping V_D (voltage at the drain of transistor M_3) from 0 to $3.3V$. The vertical marker indicates the value of V_D in which the red and green curves cross. At $V_D = 3.3V$, $V_S(M_3) = V_D(M_2) = 670.870mV$ (red curve).

For the **low voltage cascode current mirror**, similar plots were obtained for the voltages which were not at $0V$ nor defined in the simulation (`vcasn` and V_D). In the green curve, a constant voltage value has been obtained once again; this refers to the source voltage of the M_0 transistor. According to the theoretical analysis, this value should be equal to $V_{OD} = 0.2V$, thus a 29.5% relative difference exists. However, this high disparity only means that the value of `vcasn` selected for the simulation was too high. According to the theoretical analysis, the minimum value required for this voltage is $V_{casn} = 2V_{OD} + V_{TH_0}$. The overdrive voltage was defined as $V_{OD} = 0.2V$; the threshold voltage for the upper transistors (M_0 and M_3) in Figure 2 is given by $V_{TH} \approx 661.23mV$, as discussed above with Figure 6. Thus, $V_{casn} = 1.1V (\approx (2 \times 200 + 661.23)mV = 1.06V)$ was used initially in the simulations; however, it resulted in a green curve at an even higher voltage. Thus, V_{casn} was decreased to $1V$, but some difference is still visible. The difference that still exists, however, is not very relevant and could be eliminated by simply decreasing the value of `vcasn` even more.

In this case, the drain voltage $V_D(M_0)$ of the nMOS transistor M_0 (shown in Figure 3) should remain at $V_{GS_1} = V_{OD} + V_{TH_1}$. Thus, considering the voltage of the blue curve (shown below) and $V_{OD} = 0.2V$, the value $V_{TH_{1_{exp}}} = 470.702mV$ is obtained, which differs in about 2.3% from $V_{TH_{tab}} = 0.46V$ [5]. In this case, the body effect is not affecting this value, since, in this new design for the cascode current mirror, the drain of M_0 is shorted to the gates of transistors M_1 and M_2, whose bulks and sources are connected to each other. The reason why $V_{TH_{1_{exp}}}$ obtained with Figure 7 is higher than for Figure 6 is that, as mentioned above, the value of V_{casn} could be reduced even further, thus it would lead to the lower threshold voltage.

Lastly, the source voltage in transistor M_3 starts, once again, at $0V$ and increases towards the value of $V_S(M_0)$ - as expected, due to the symmetry of voltages in the low voltage cascode current mirror. After increasing significantly, the voltage remains approximately constant, since the transistor M_2 is finally working in the saturation region and the impact of the channel-length modulation is not

too significant. The small slope here leads to the small slope in the $I_{out}(V_D)$ curve shown before - at $V_D = 3.3V$, it reaches $342.623mV$, which is 32.3% higher than the voltage for the green curve (a much more significant difference than what was seen for Figure 7). A key difference between the curves in Figures 6 and 7 is that, in the latter, the saturation is reached for lower values of V_D - in this case, at $V_D = 2V_{OD} = 0.4V$, which means that the saturation range (values of V_D for which the transistor M_3 works in saturation) is increased. Moreover, the current $I_{out} = 10\mu A$ was reached at $V_D = 670.876mV$ (as seen in Table 2), approximately the same value as $V_D = 670.912mV$ in which $V_S(M_3) = V_S(M_0)$ (as shown in Figure 7) - the difference to the former is of about 0.005%. Once again, this is approximately the same voltage value for the blue curve (which, in this case, is $V_{D_0} = 670.702mV$, as indicated in Figure 7), because the drain currents in transistors M_0 and M_3 (I_{REF} and I_{out}, respectively) will only be the same when the respective drain voltages are also the same, due to equation 2 - their gates are shorted to each other (V_G is the same), $V_{TH_0} = V_{TH_3}$ (both transistors suffer from body effect) and $V_{S_0} \approx V_{S_3}$ for all V_D.

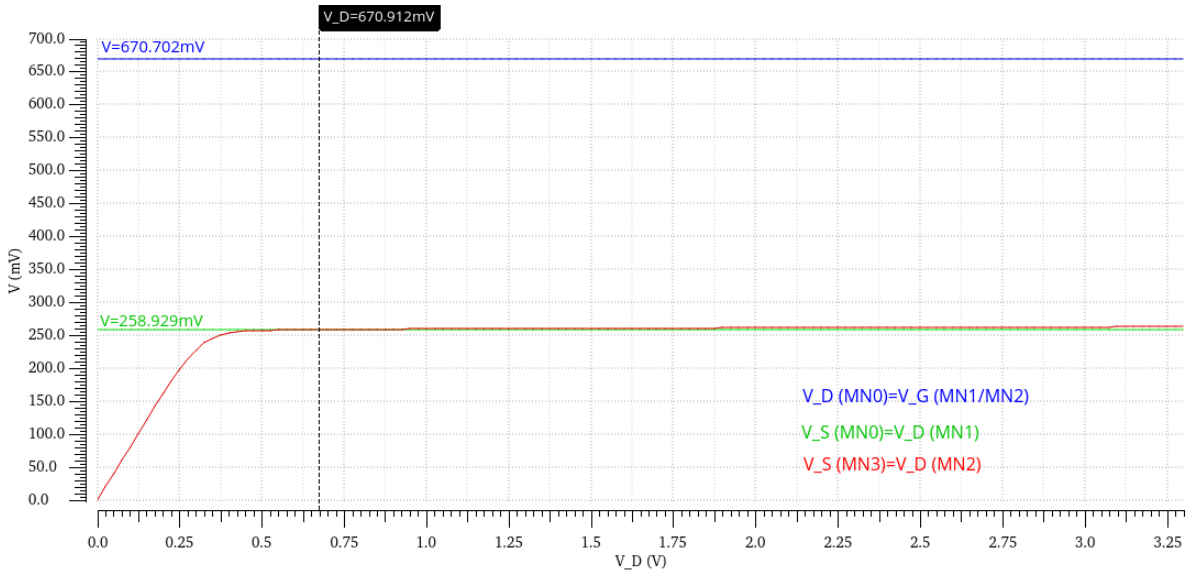

Figure 7: Voltage values at the drain, source and gate of different transistors shown in Figure 3 (cascode current mirror with `vcasn`). The DC simulation was made by sweeping V_D (voltage at the drain of transistor M_3) from 0 to $3.3V$. The vertical marker indicates the value of V_D in which the red and green curves cross. At $V_D = 3.3V$, $V_S(M_3) = V_D(M_2) = 342.623mV$ (red curve).

3 Conclusion

Starting from the cellview designed in Virtuoso for the previous laboratory assignment, in order to obtain a **cascode current mirror**. Another view was then created for a cascode current mirror which allows operation with **low voltage**. The advantages and disadvantages of the different currrent mirror designs were compared amongst each other.

These different current mirrors were simulated together in Virtuoso, in order to obtain its $I_{out}(V_D)$ curves, which showed the change in the output current for different values of the drain voltage in the transistor in which I_{out} is measured. Regarding these curves, the difference in the impact of the channel length modulation was compared between themselves. Moreover, the points in which $I_{out} = 10\mu A$ and the transistors entered the saturation region were analysed. It was concluded that, in the cascode current mirror designs, the impact of channel-length modulation is much less significant, even though it is slightly larger for the low voltage cascode current mirror. However, in this design, the voltage V_D in which the saturation is reached is lower, thus increasing the saturation range considerably.

Regarding the cascode current mirrors, the change in the voltages of the drains, sources and

gates of the different transistors (M_0 to M_3) for different values of V_D were also plotted. These results were then analysed by taking into account the expected values presented in the theoretical study of these designs, described in section 1. The slight change in the drain voltage of the transistor M_2 was observed and the threshold voltages for the upper and lower transistors were determined. Since the formers suffer from body effect, it was verified that V_{TH} was higher for these transistors.

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