# Microelectronics

## Laboratory activity

Marcelino Santos

Área Científica de Eletrónica
Departamento de Engenharia Eletrotécnica e de Computadores

Instituto Superior Técnico
Universidade de Lisboa

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Common points to **all** Lab activities:

Deliverables:

- Analytical study with the circuit design and operation principle
- Names of the libraries, cells and views used and description of their purpose
- Schematic and symbol capture for each cell (identifying the lib and cell name)
- Simulation results
- Comments on simulation results (values, edges, slopes) – comparison with 1st order model
- Image with the layout, LVS and DRC report (if applicable)

Main evaluation points:

- Comments on simulations
- Critical analysis of the circuit performance and limits for operational conditions
- Compliance with naming conventions (in virtuoso)
- Symbol quality (representation of the schematic contend)
- Waveforms (and all figures) quality (readability)

Lab 1 – ID(VGS) and ID(VDS) simulation with virtuoso

Available documentation:

- Previous courses with CMOS transistors: “Dispositivos Eletrónicos” and “Introdução aos Circuitos e Sistemas Eletrónicos”
- Course slides: “2 – Devices in CMOS Technology”
- Tutorial (pdf): “Microeletrónica – Full-Custom Design with Cadence Tutorial”
- Tutorial (vídeo): “Simulation of NMOS ID(VGS)” [1]

Activity:

- Autonomously repeat the tutorial “Simulation of NMOS ID(VGS)” as shown in the video (it may be useful to follow the steps with the pdf of tutorial “Microeletrónica – Full-Custom Design with Cadence Tutorial”) – just for training
- Analyze the ID(VGS) curves obtained and explain, for each VDS, the parts of the curve where the NMOS transistor is OFF, saturated or in triode region – for deliverable
- Create a different tesbench and simulate ID(VDS) for VGS={0, 0.8, 1,6, 2.4, 3.2}[V] – for deliverable
- Analyze the ID(VDS) curves obtained and explain, for each VGS, the parts of the curve where the NMOS transistor is OFF, saturated or in triode region – for deliverable
- Repeat the analysis with a PMOS transistor (create a different cell and a different testbench. Make sure to follow naming convention)

[1] https://educast.fccn.pt/vod/clips/245dnx1vq7/link_box_h?locale=en

Lab 2 – Design of a nand2 standard cell

Available documentation:

- Previous courses with CMOS transistors: “Dispositivos Eletrónicos” and “Introdução aos Circuitos e Sistemas Eletrónicos”
- Tutorial (pdf): “Microeletrónica – Full-Custom Design with Cadence Tutorial”
- Tutorial (vídeo): “Simulação típica e em corners”
- AMS 0.35um Process Parameters (pdf)
- Course slides: “5 – Digital Cells Design”

Activity:

- Autonomously repeat the tutorial “Microeletrónica – Full-Custom Design with Cadence Tutorial”)
- Copy the *inverter* cell to a new cell with name *nand2*
- Edit the schematic of the new nand2 to implement a two inputs NAND gate with the same driving strength of the inverter.
- Generate the symbol and perform the simulation of the cell *nand2*
- Design the layout of the *nand2*, keeping the supply rails size and position of the inverter cell.
- Perform the validation of the layout with DRC and LVS

Lab 3 – Current mirror design

Available documentation:

- Previous courses with CMOS transistors: “Dispositivos Eletrónicos” and “Introdução aos Circuitos e Sistemas Eletrónicos”
- Course slides: “3 – Functions of MOS transistors”, check in particular, section: - MOS transistor as a current source
- Process parameters of AMS 0.35um [2]

Activity:

- As a theoretical preparation, design a current mirror with two NMOS transistors.
- Assuming that the input current and the output current are the same (10uA), design the W and L of the NMOS transistors to have an overdrive voltage of 200mV.
- Design the current mirror in virtuoso schematic editor
- Simulate the current mirror with a DC sweep output voltage range of 0 to 3.3V
- Comment the simulation result referring in particular: the overdrive voltage, the VDS that ensures the output current identical to the input current, the channel length modulation impact
- Repeat the previous point but with corner analysis
- Keeping the same W/L, simulate, for typical conditions, the current mirror with MOS transistors with L={0.35um, 1um, 4um} and comment the channel length modulation impact of L

[2] “0.35 µm CMOS C35 Process Parameters”, Document Number: ENG -182, Revision#: 2.0

Lab 4 – Cascode current mirror design

Available documentation:

- Previous courses with CMOS transistors: “Dispositivos Eletrónicos” and “Introdução aos Circuitos e Sistemas Eletrónicos”
- Course slides: “3 – Functions of MOS transistors”, check in particular, section: - MOS transistor as a voltage clamp
- Book [3], Chap 5
- Process parameters of AMS 0.35um [2]

Activity:

- Add two NMOS transistors to the current mirror of Lab3 to obtain a cascode current mirror
- Perform the characterization of the cascode current mirror and compare it with the simple current mirror from Lab3
- Change the design of the cascode current mirror to allow operation with low voltage
- Characterize the low voltage cascode current mirror and compare it with the previously designed current mirrors

[3] Design Of Analog Cmos Integrated Circuits: Behzad Razavi 2017 Mc Graw Hill in https://drive.google.com/open?id=1G8ahcQs8ESKNZy_3whX-cU_aj4Tj5Hhg

Lab 5 – Current reference design

Available documentation:

- Previous courses with CMOS transistors: “Dispositivos Eletrónicos” and “Introdução aos Circuitos e Sistemas Eletrónicos”
- Book [3], Chap 11
- Process parameters of AMS 0.35um [2]

Activity:

- Based on the topology of Fig 11.3(a) in [3], design a circuit that outputs 4 current references of 1uA each (from PMOS). Assume a supply of 3.3V (+/- 10%) and that the maximum current for the current reference generation is 4uA.
- Evaluate the performance of the current reference in corners (minimum and maximum output current and power consumption and the PSRR).
- Evaluate possible circuits improvements using previous knowledge