Chapter II

Devices in CMOS Technology

- **MOS analytical models**
- Capacitors
- Bipolar PNP
- Resistors

MOS model

Triode:

$$i_{DS} = \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot \left[\left(v_{GS} - V_{TH} \right) \cdot v_{DS} - \frac{v_{DS}^2}{2} \right] \cdot \left(1 + \lambda \cdot v_{DS} \right) \qquad \text{para} \qquad 0 < v_{DS} < v_{GS} - V_{TH}$$

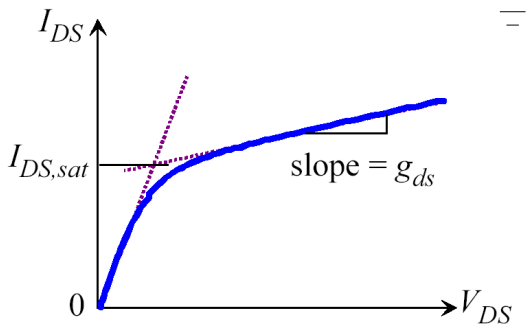
Voltage controlled resistor: $r_{DS} = v_{DS}/i_{DS} = [2K(v_{GS} - V_{TH})]^{-1}$

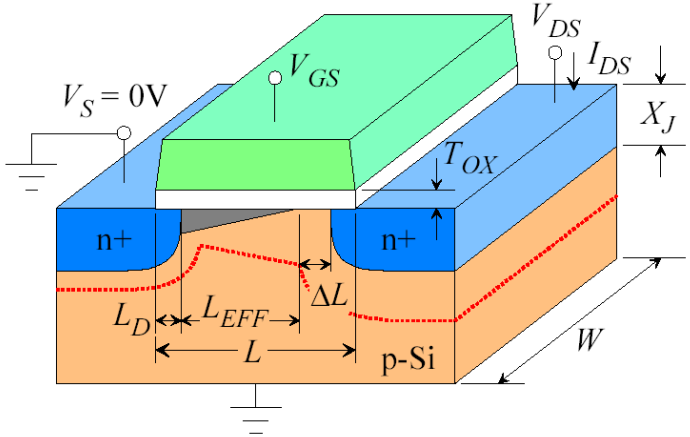
Saturation:

$$i_{DS} = \frac{\mu \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot \left(v_{GS} - V_{TH} \right)^2 \cdot \left(1 + \lambda \cdot v_{DS} \right) \qquad \text{para} \qquad v_{DS} > v_{GS} - V_{TH}$$

Voltage controlled current source:

λ- channel length modulation parameter
typical values NMOS: λ = 0,01 V^{-1}
PMOS: λ = 0,02 V^{-1}





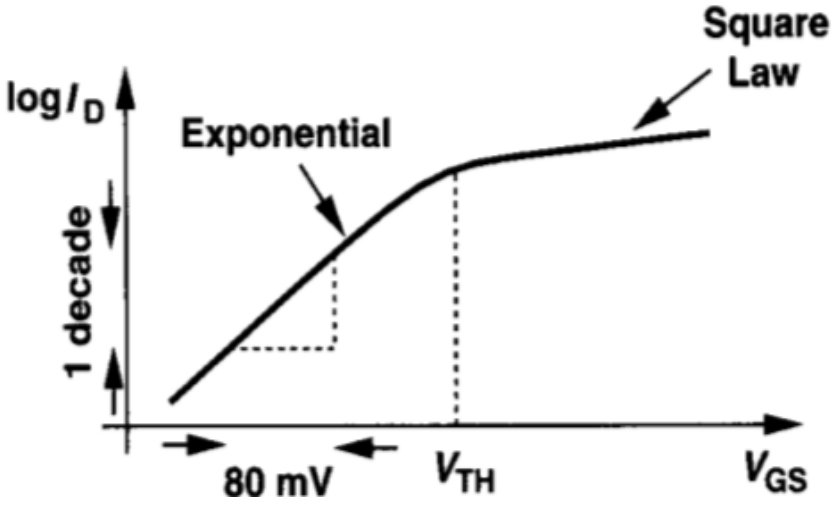
MOS model

OFF vs Subthreshold (weak inversion): $v_{GS} < V_{TH}$

$v_{DS} > 200mV$

$$I_D = I_0 \exp \frac{V_{GS}}{\zeta V_T}$$

$V_T = kT/q$



MOS model

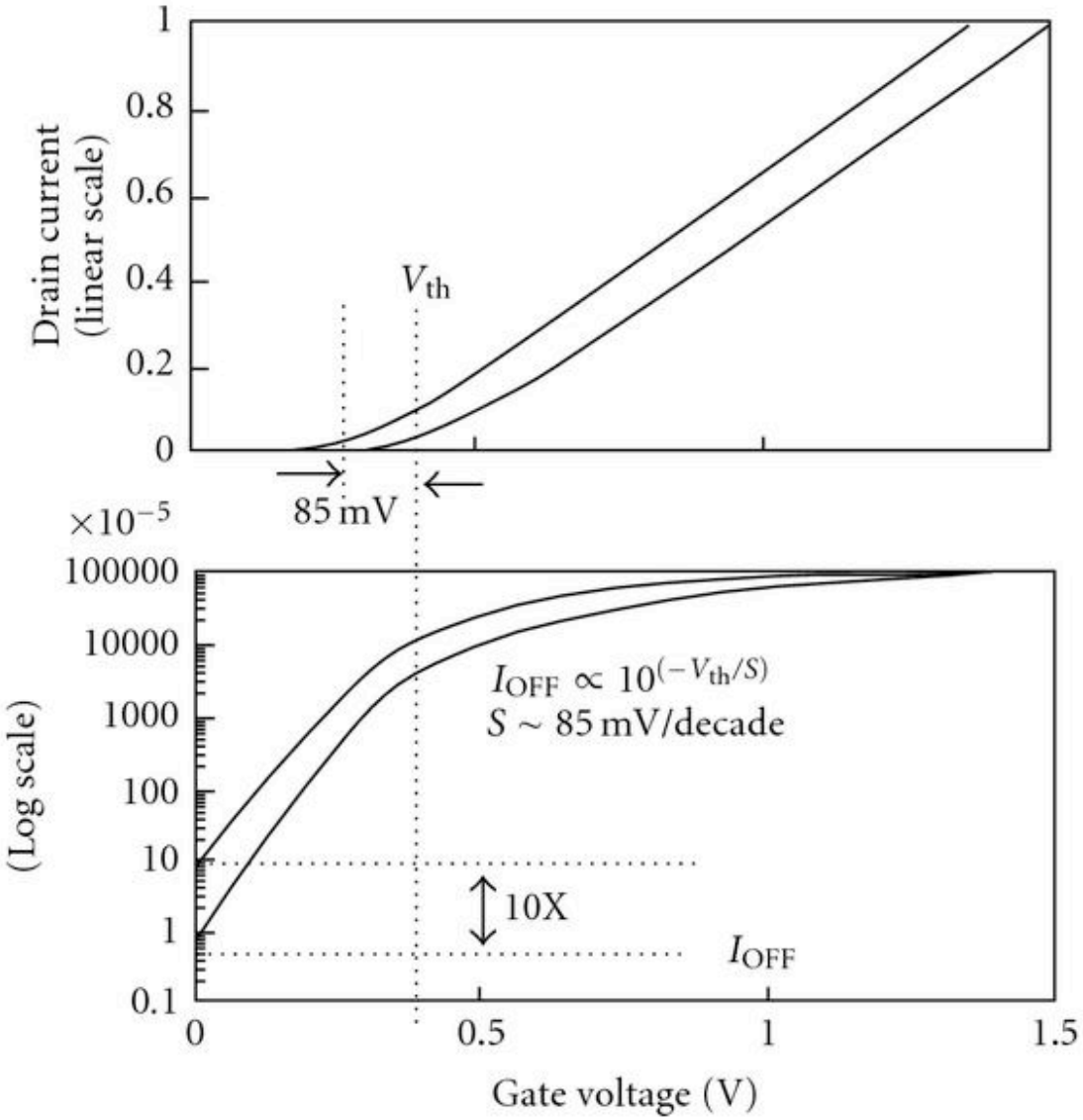
Subthreshold (weak inversion):

Bad news:

- leakage

Good news:

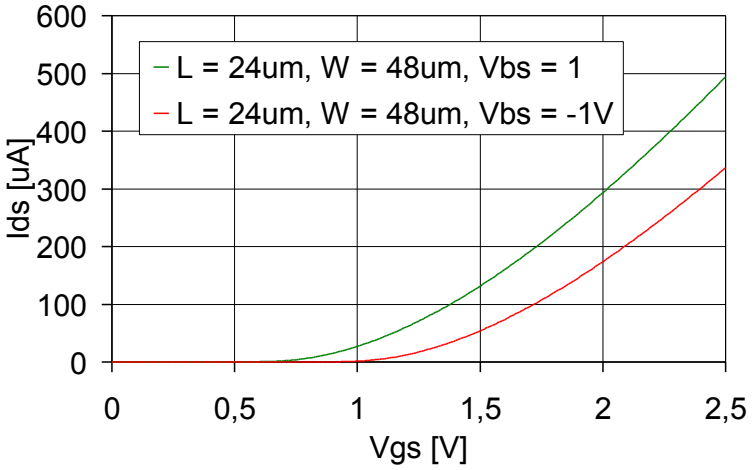
- ultra low power design
- high gm



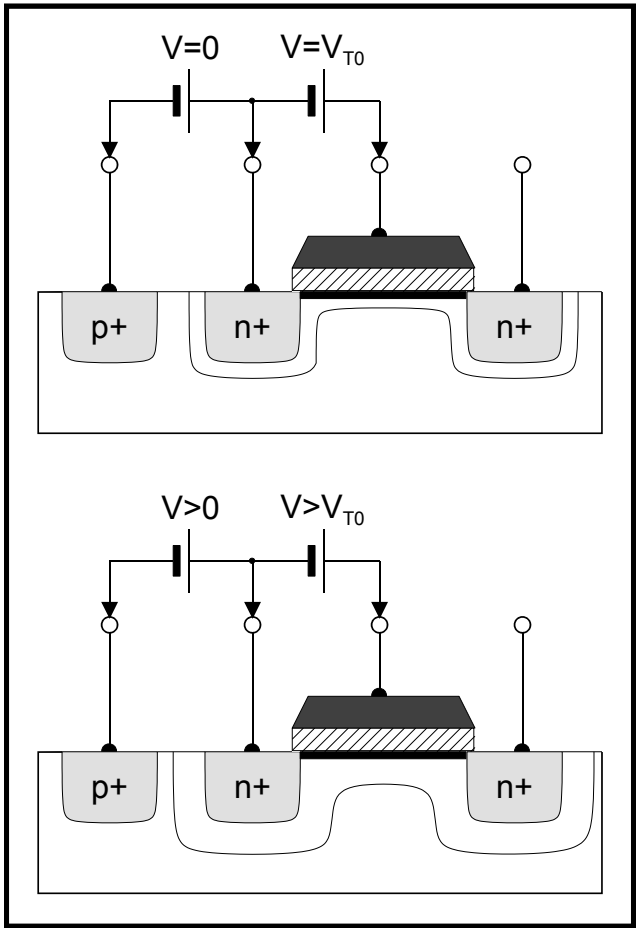
MOS model

Body effect - $V_{TH}(V_{SB})$

$$V_{TH} = V_{T0} + \gamma\left[\sqrt{\phi - V_{BS}} - \sqrt{\phi}\right]$$



V_{T0} represents V_{TH} with $V_{SB} = 0$



Technology parameters:

ϕ- strong inversion surface potential (typical value: ϕ = 0,6 V)

γ - bulk threshold parameter (typical NMOS: γ = 0,8 $V^{1/2}$, PMOS: γ = 0,4 $V^{1/2}$)

MOS model

Temperature influence

Mobility:

$$K' = K' \times \left(\frac{T}{T_0} \right)^{-\frac{3}{2}}$$

For digital circuits the mobility reduction is dominant

V_T:

$$V_T = V_{T0} - \alpha (T - T_0)$$

$$\alpha \approx 2{,}3 \ mV/^o C$$

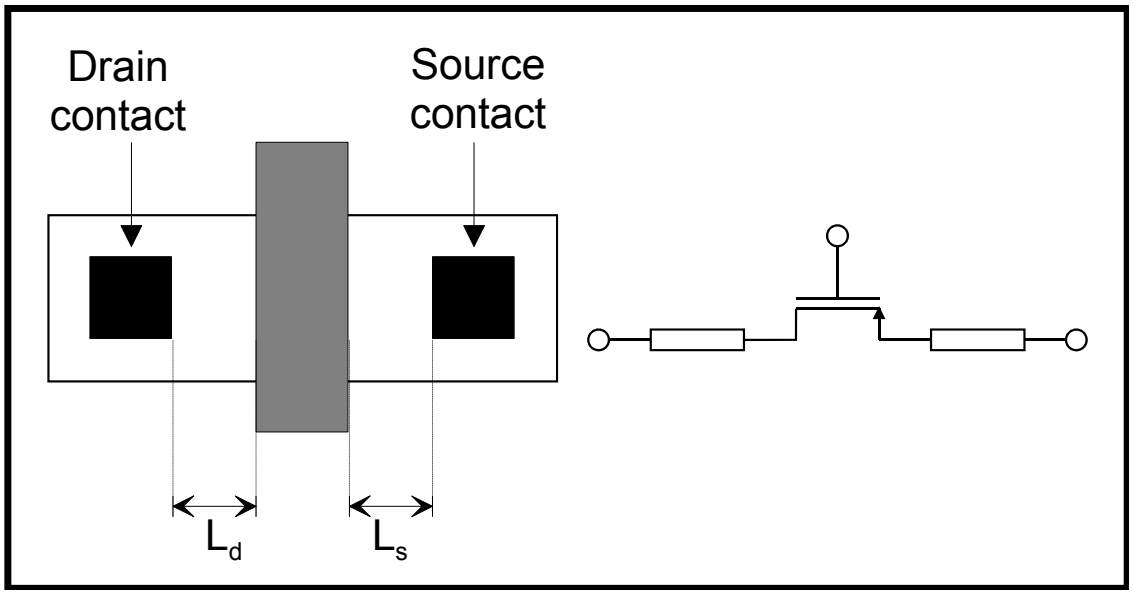
With v_{GS} near V_T, the V_T change is dominant

$$i_{DS} = \frac{\mu \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot \left(v_{GS} - V_{TH} \right)^2$$

MOS model

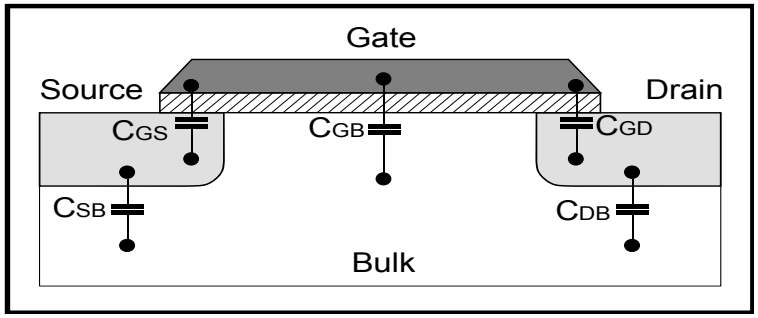
Drain and source resistence

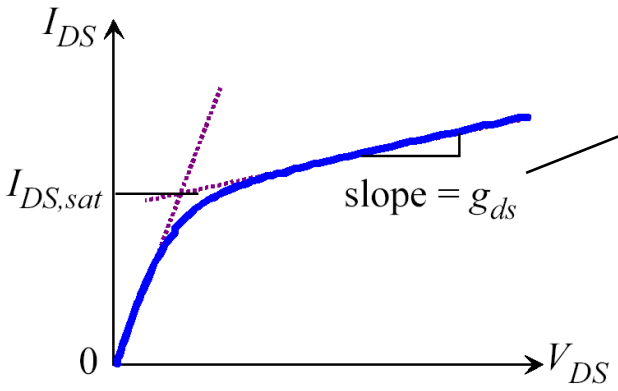
$$R_{S,D} = \frac{L_{s,d}}{W} \cdot R_{sq} + R_c$$

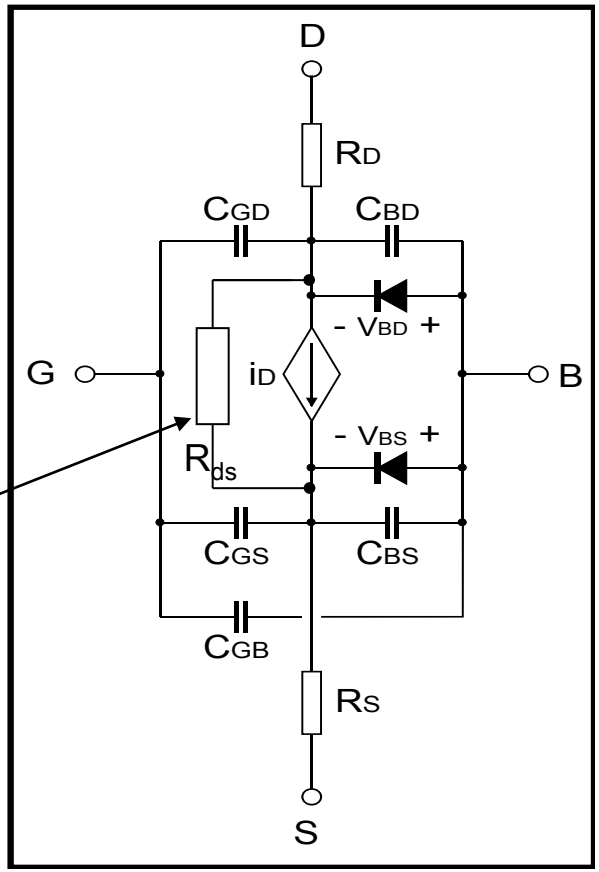


MOS model

High frequency model



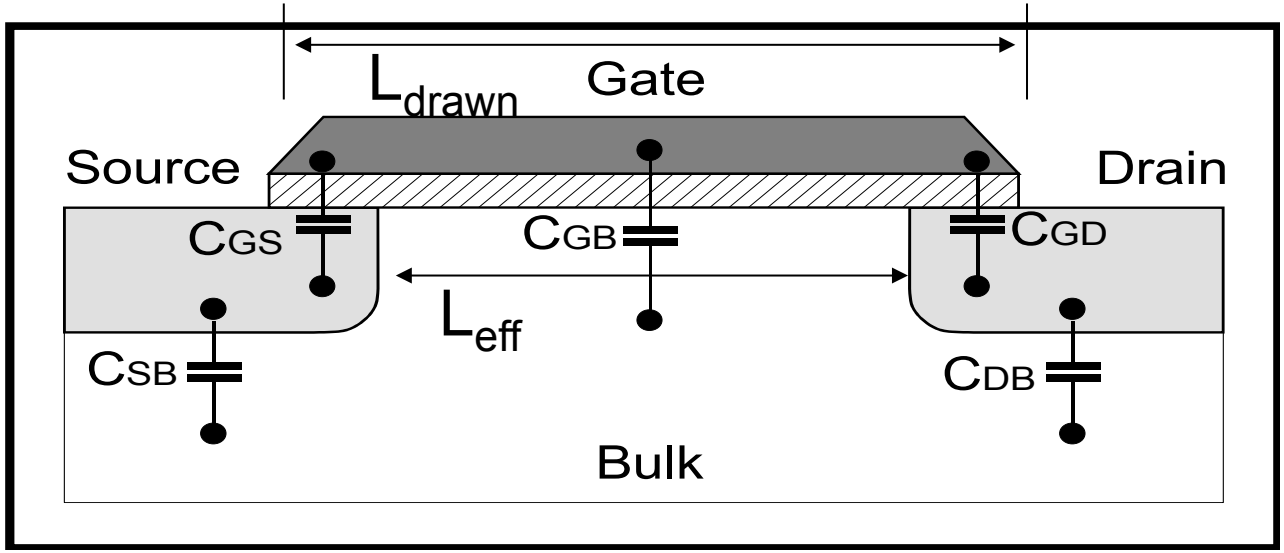




MOS model

Sources of MOS parasitic capacitances:

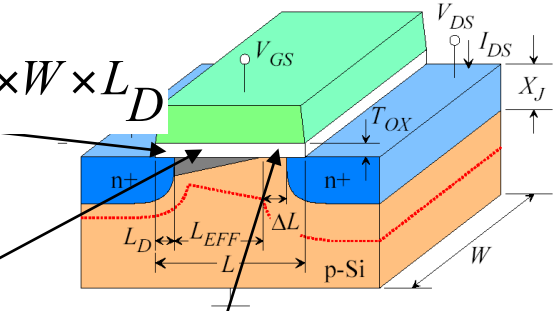
- Lateral diffusion
- Channel charge
- PN junctions

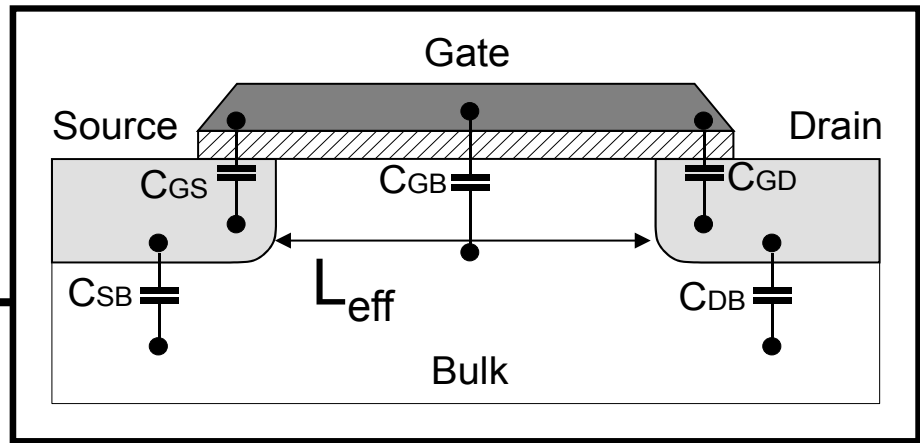


MOS model

Contributions to GS, GD:

- Lateral diffusion : $C_{GD,S} = C_{ox} \times W \times L_D$
- Channel charge :
  - ~~off~~
  - triode – $C_{GD,S} = \frac{1}{2} C_{ox} \times W \times L$
  - saturation – $C_{GS} = \frac{2}{3} C_{ox} \times W \times L$ $C_{GD} = 0$
- ~~PN junctions~~





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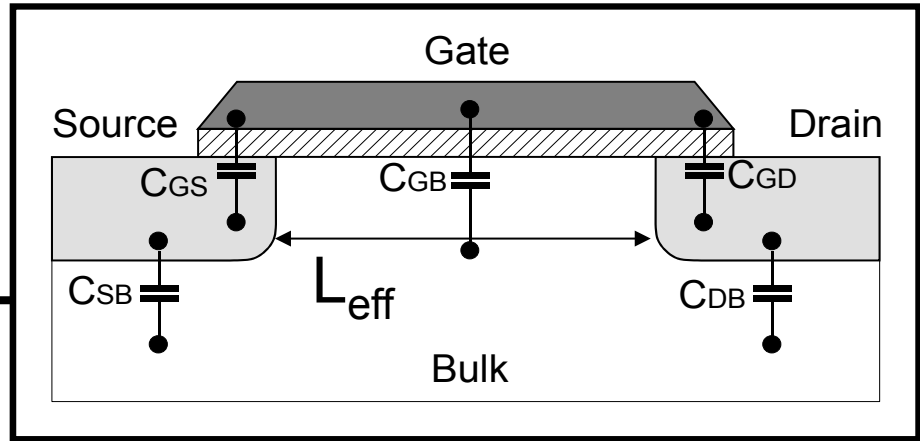
MOS model

Contributions to GB:

- Lateral diffusion:
- Channel charge :
  - off - $C_{GB} = C_{ox} \times W \times L_{eff}$
  - triode
  - saturation
- PN junctions



MOS model

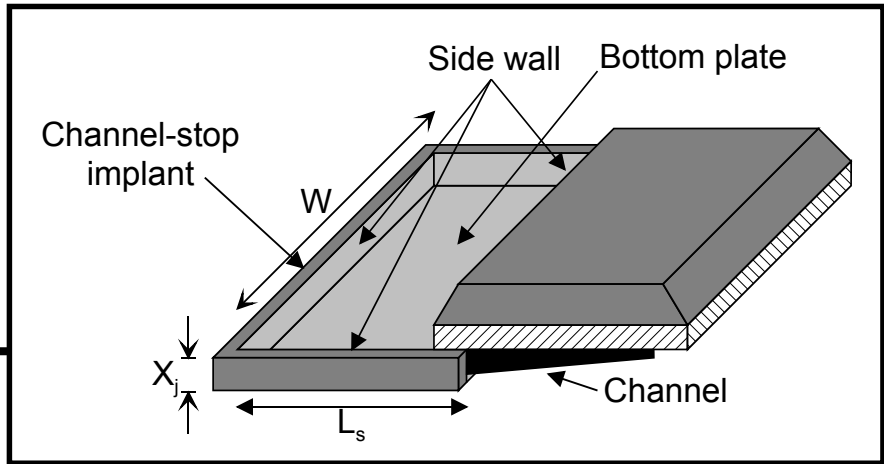
Contributions to SB, DB:

- Lateral diffusion
- Channel charge(C_{BC}: subs. - canal):
  - off
  - triode - $C_{SB} = \frac{C_{BC}}{2}$ $C_{DB} = \frac{C_{BC}}{2}$
  - saturation - $C_{SB} = \frac{2}{3} C_{BC}$ $C_{DB} = 0$
- PN junctions

$$C_{S,DB} = \frac{C_J A}{\left(1 - \frac{V_F}{\phi_B}\right)^{MJ}} + \frac{C_{JSW} P}{\left(1 - \frac{V_F}{\phi_B}\right)^{MJSW}}$$

$$C = \frac{C_{j0} A}{\left(1 - \frac{V_F}{\phi_B}\right)^{n}}$$

ϕ_B – barrier potential (0,7 V)
V_F – forward bias voltage
C_{j0} – capacitance density at 0 V
A – Junction area



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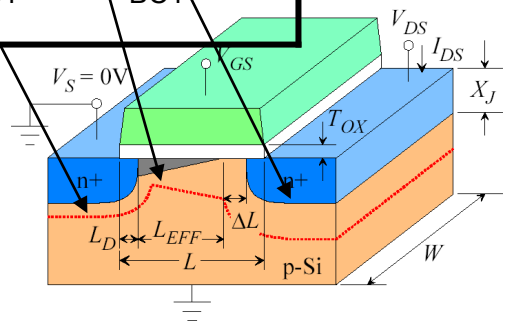
MOS model

	corte	tríodo	saturação
C_{GD}	$C_{ox}WL_D$	$C_{ox}WL_D$+½ $C_{ox}WL$	$C_{ox}WL_D$
C_{GS}	$C_{ox}WL_D$	$C_{ox}WL_D$ +½ $C_{ox}WL$	$C_{ox}WL_D$ +⅔ $C_{ox}WL$
C_{BG}	$C_{ox}WL$	0	0
C_{BD}	C_{BD1}	C_{BD1} +½ C_{BC1}	C_{BD1}
C_{BS}	C_{BS1}	C_{BS1} +½ C_{BC1}	C_{BS1} +⅔ C_{BC1}

Cap. subs.- source

Cap. subs.- channel



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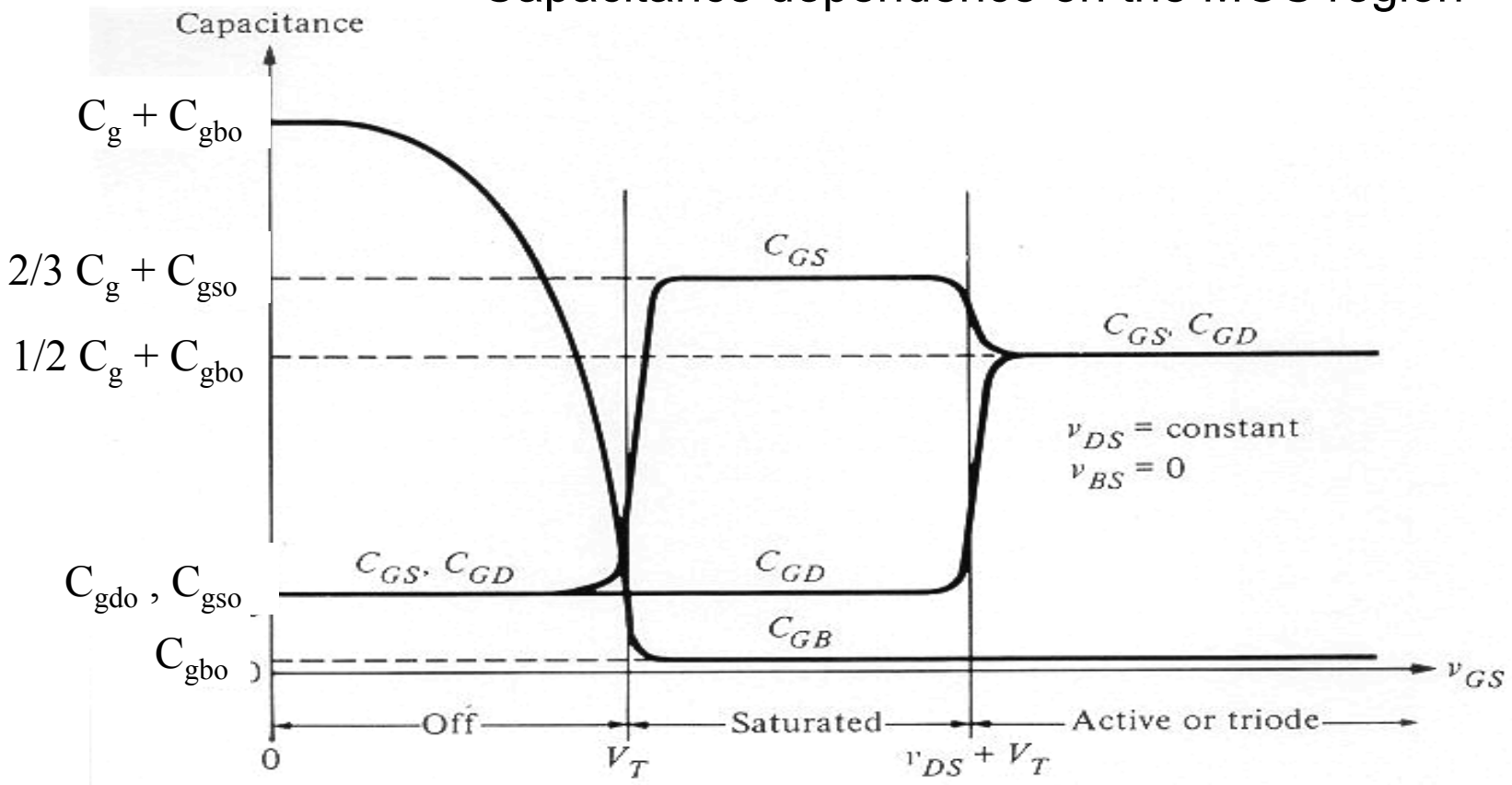
MOS model

Capacitance dependence on the MOS region



Chapter II

Devices in CMOS Technology

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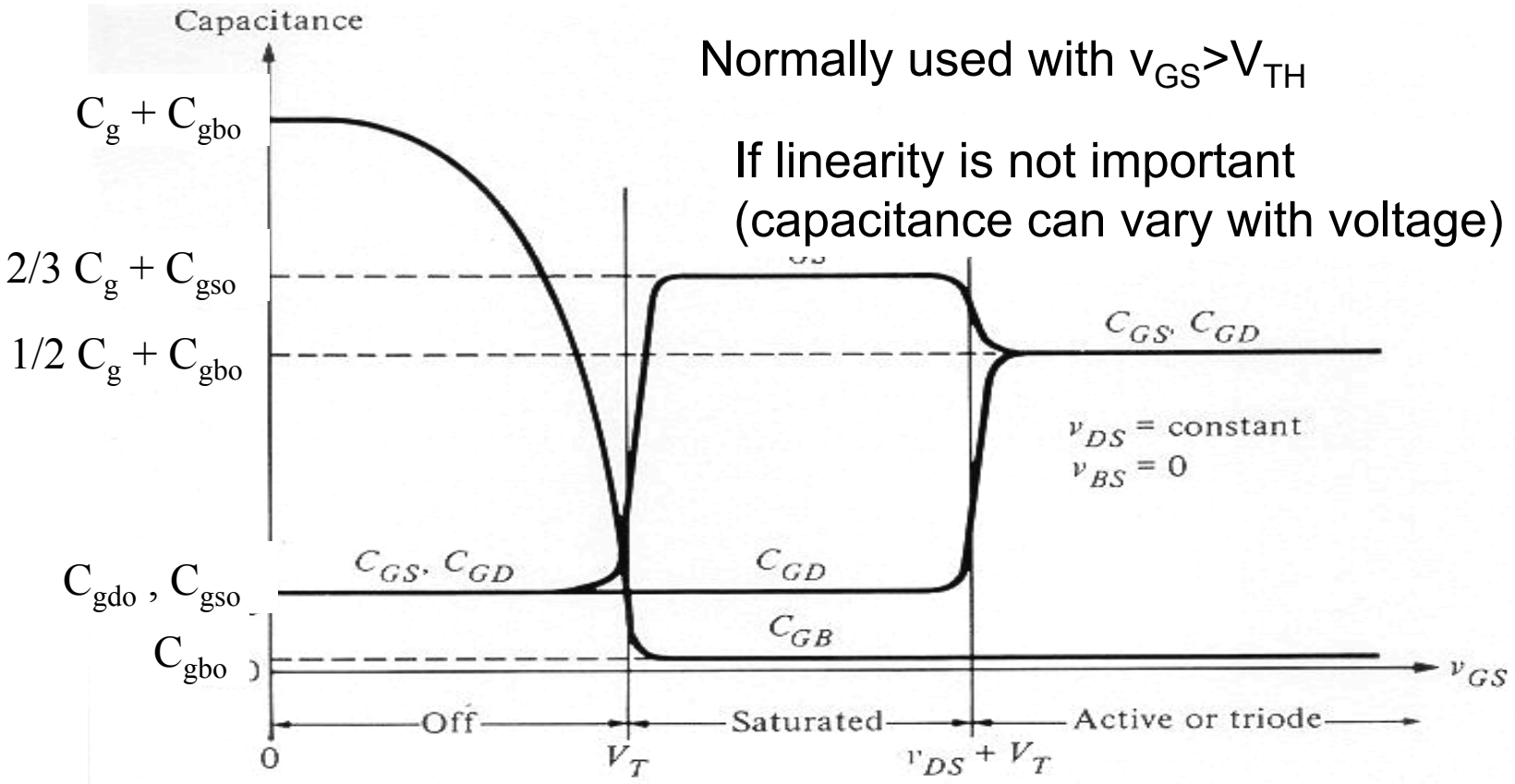
- **Capacitors**
- Bipolar PNP
- Resistors

MOS transitor as capacitor

Non-linear but **very good density** – lower area required



Normally used with $v_{GS}>V_{TH}$

If linearity is not important
(capacitance can vary with voltage)

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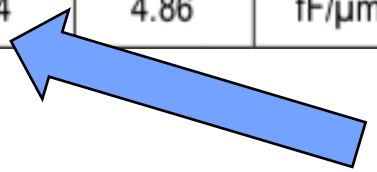
MOS transitor as capacitor

Example from a tech process parameters:

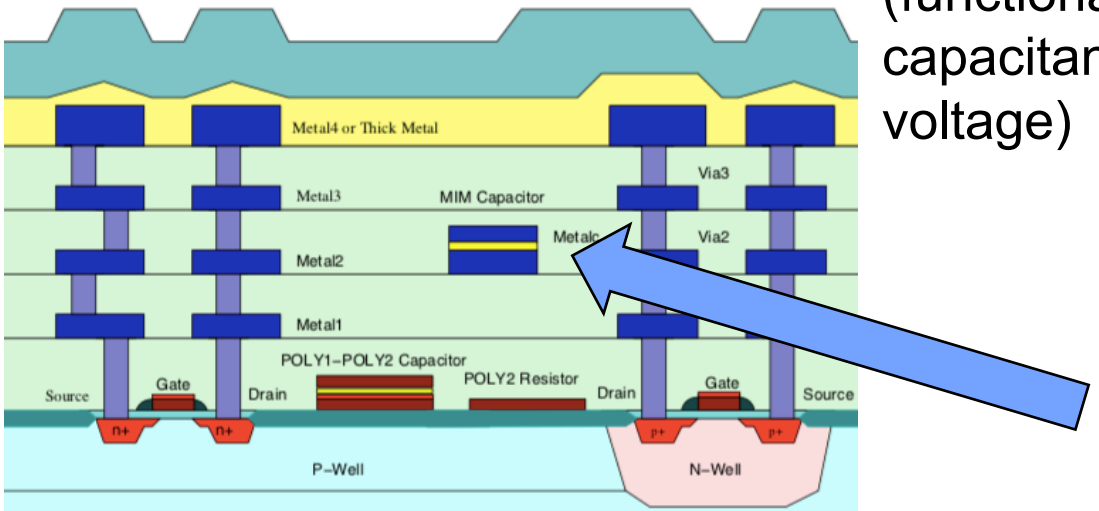
PASS/FAIL PARAMETERS					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
POLY1 - DIFF (gate oxide)					
POLY1 - DIFF area	CGOX	4.26	4.54	4.86	fF/μm²



MIM (Metal-Isolator-Metal) capacitors

Linear but **only available in some processes** – additional processing steps required

Normally used if process allows and if linearity is important (functionality does not allow capacitance to vary with voltage)



MIM capacitor

Parameter	Symbol	Min	Typ	Max	Unit
CMIM area capacitance	CMIM	1.00	1.25	1.50	fF/μm²

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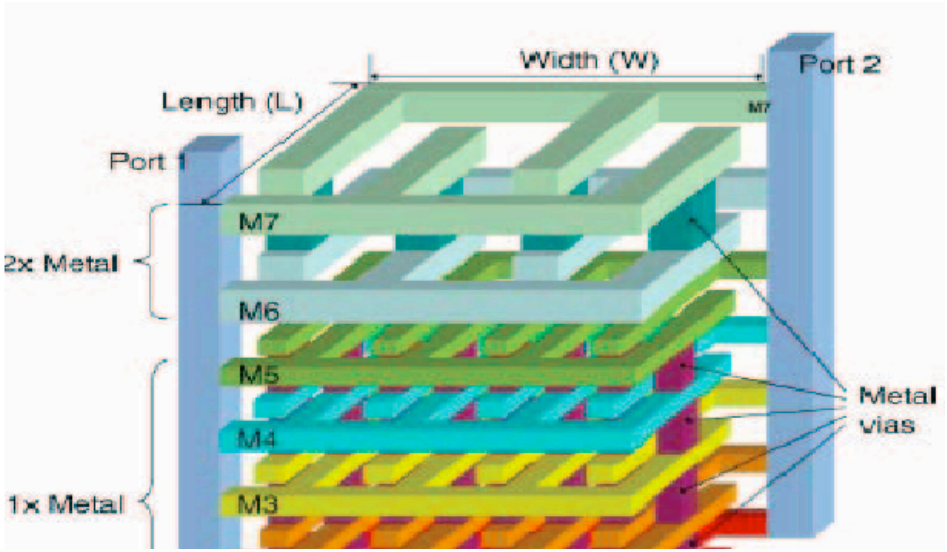
MOM (Metal-Oxide-Metal) capacitors

Linear but **require higher area** – no additional processing steps required

Used if process does not allows MIM and if linearity is important (functionality does not allow capacitance to vary with voltage)



- MOM capacitors as a stack of *fringe capacitors* (based on side capacitance)

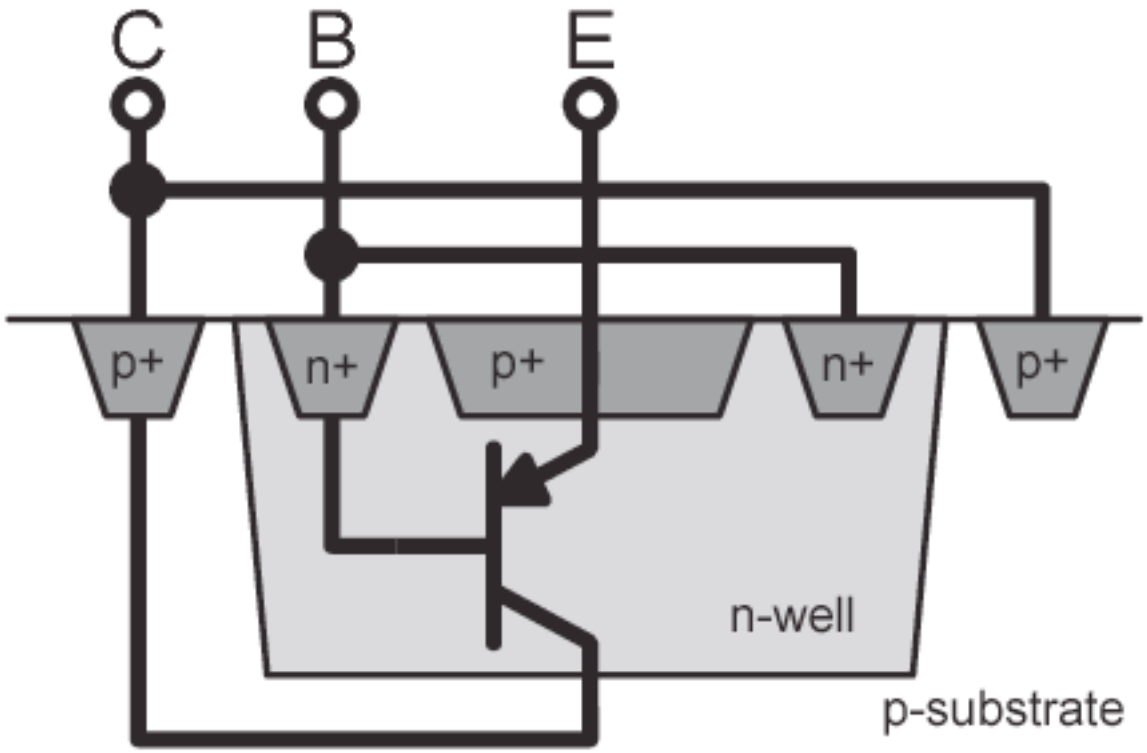
MET2 - MET1					
MET2 - MET1 area	CM2M	0.026	0.036	0.059	fF/µm²

Chapter II

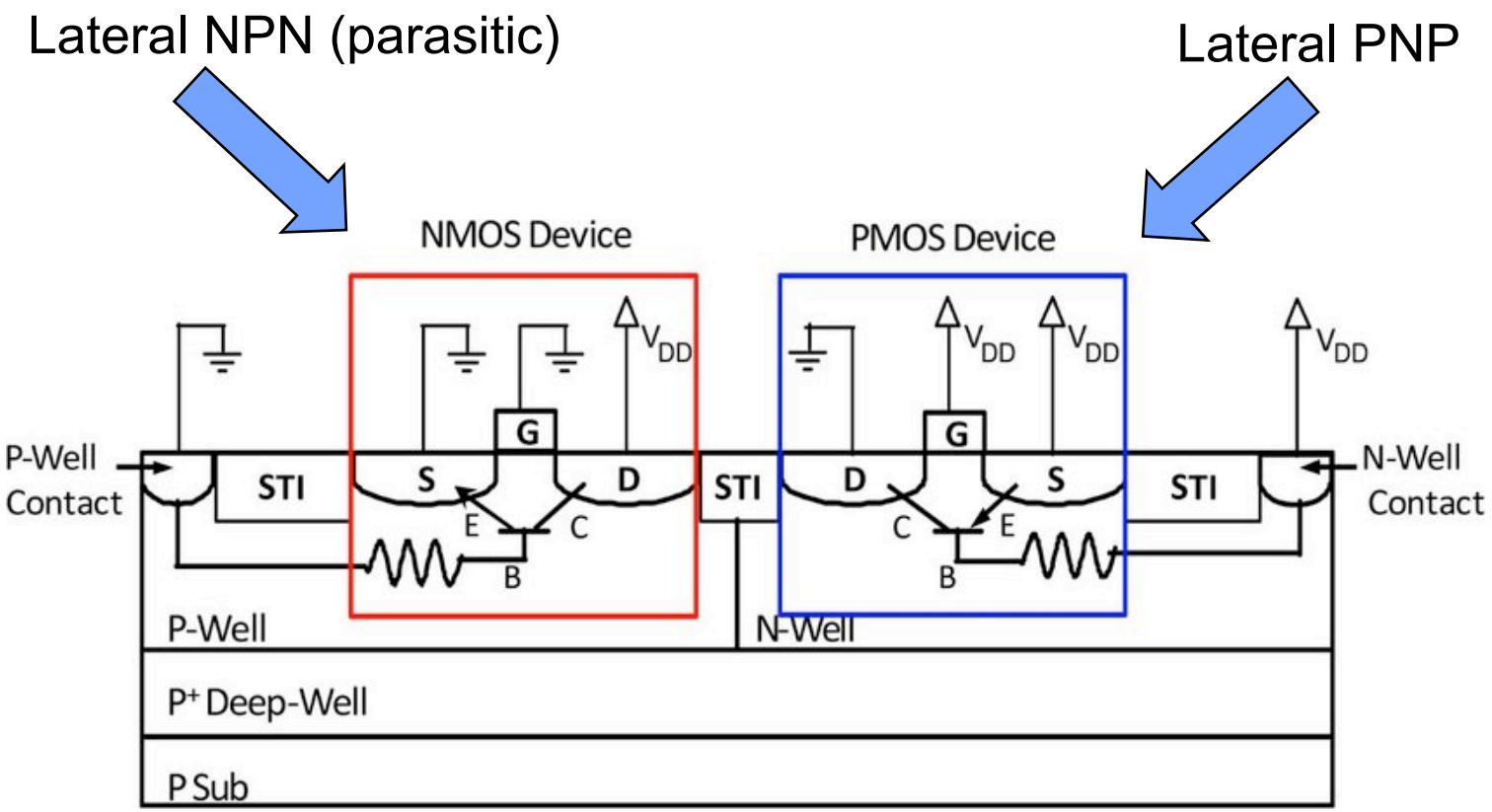
Devices in CMOS Technology

- MOS analytical models
- Capacitors
- **Bipolar PNP**
- Resistors

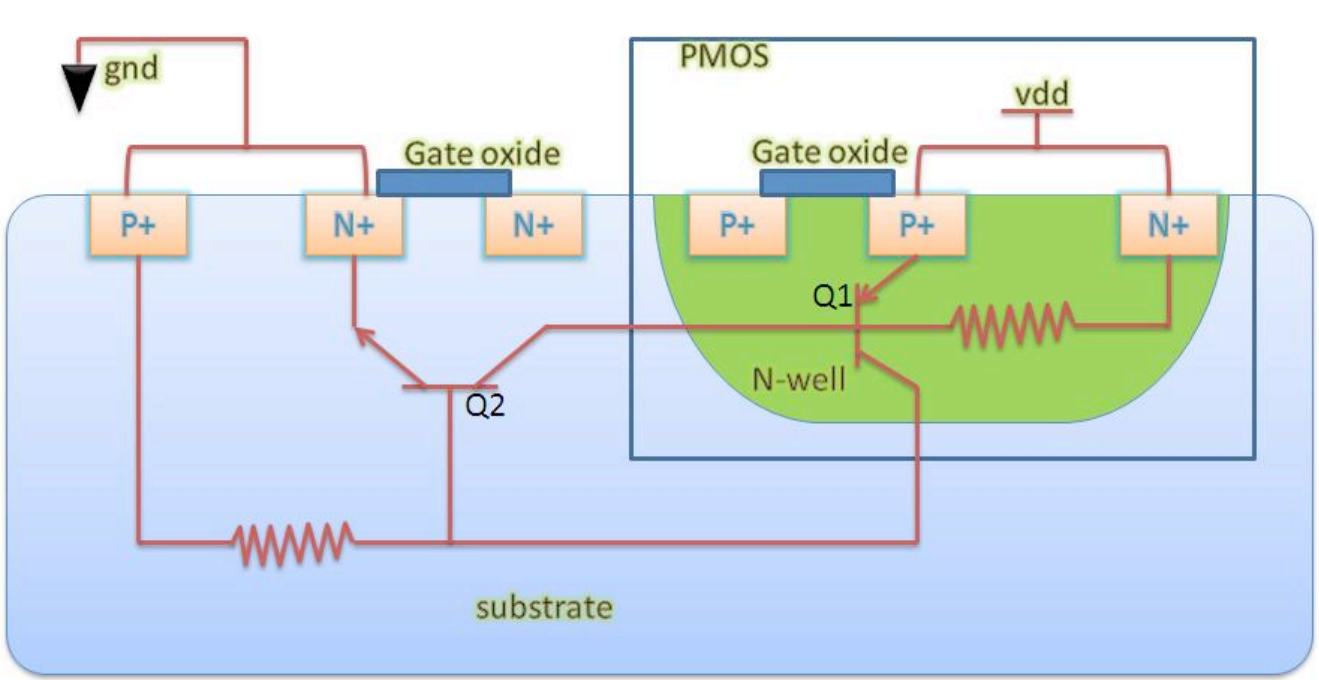
Bipolar PNP - Vertical

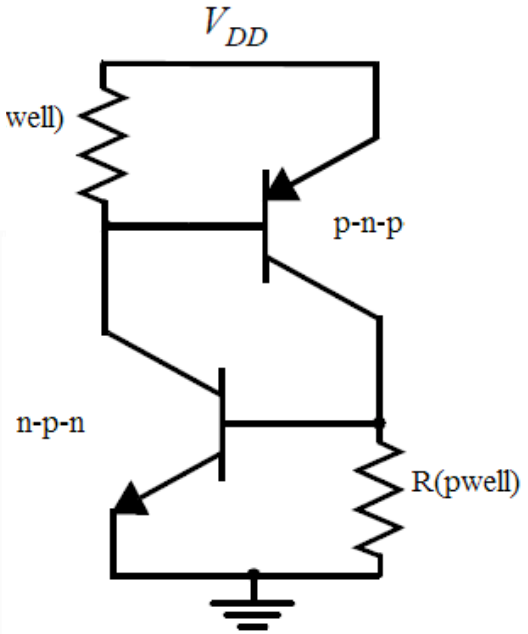


Bipolar PNP – Lateral



Bipolar parasitics and latchup





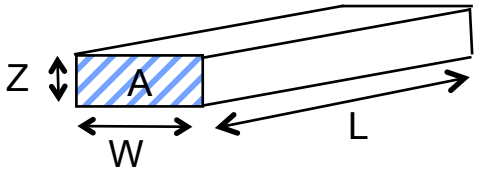
Chapter II

Devices in CMOS Technology

- MOS analytical models
- Capacitors
- Bipolar PNP
- **Resistors**

Resistors

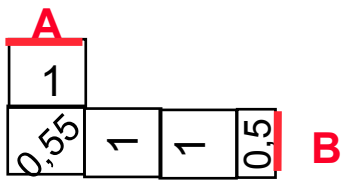
Resistivity - if a trace of metal or semiconductor with length L, cross-section with area A, and presents a resistance of value R, the corresponding material has a resistivity defined as: **$\rho = (A\,R) / L$**



Sheet *resistance* – if the thickness of the conducting material is constant, Z = cte, a square (L = W) has a resistance only dependent of Z and ρ : $R_{\square} = \rho\, L / A = \rho\, L / (W\, Z) = \rho / Z$

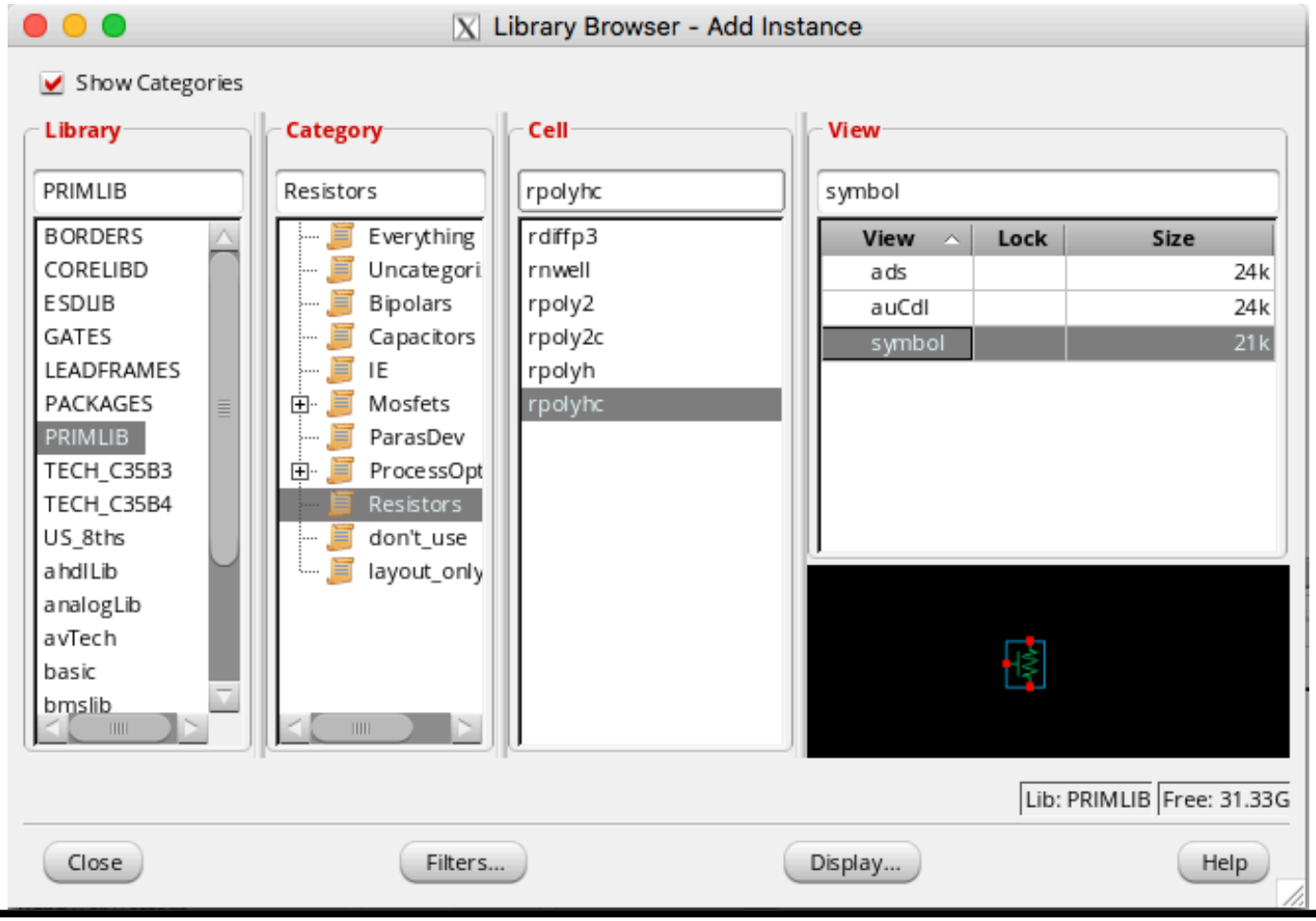
Any rectangle has a resistance that can be estimated multiplying the sheet resistance by the number of squares (L/W): $R = \rho\, L / (W\, Z) = R_{\square}\, L / W$

Ex:



$R_{AB} = (3 + 0{,}5 + 0{,}55)\, R_{\square}$

Resistors



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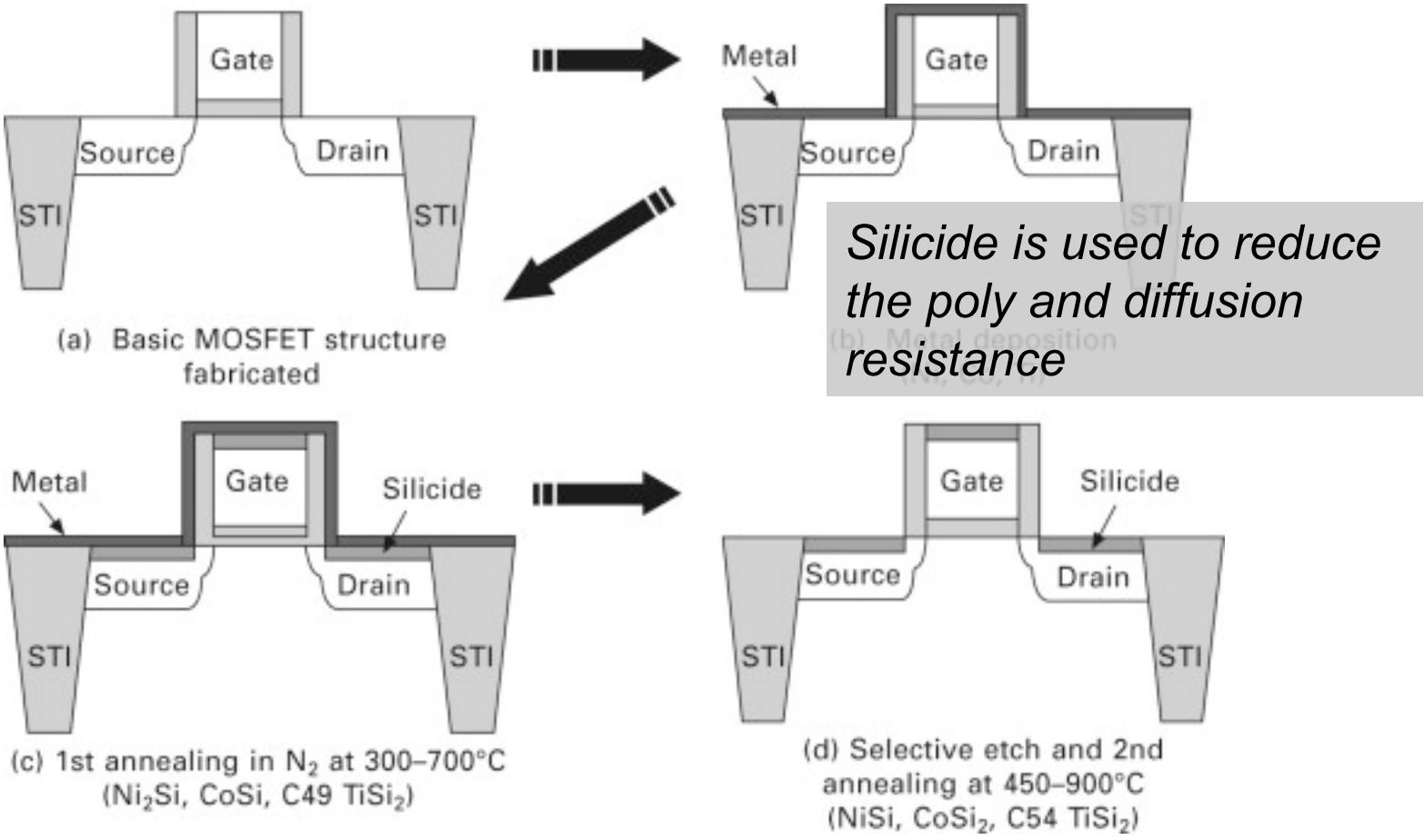
Resistors

Small sheet resistance and very large variance

MET1 sheet resistance	RMET		80	150	mΩ/□
POLY1 gate sheet resistance	RGATE		8		Ω/□
NDIFF sheet resistance	RDIFFN	55	70	85	Ω/□
PDIFF sheet resistance	RDIFFP	100	130	160	Ω/□

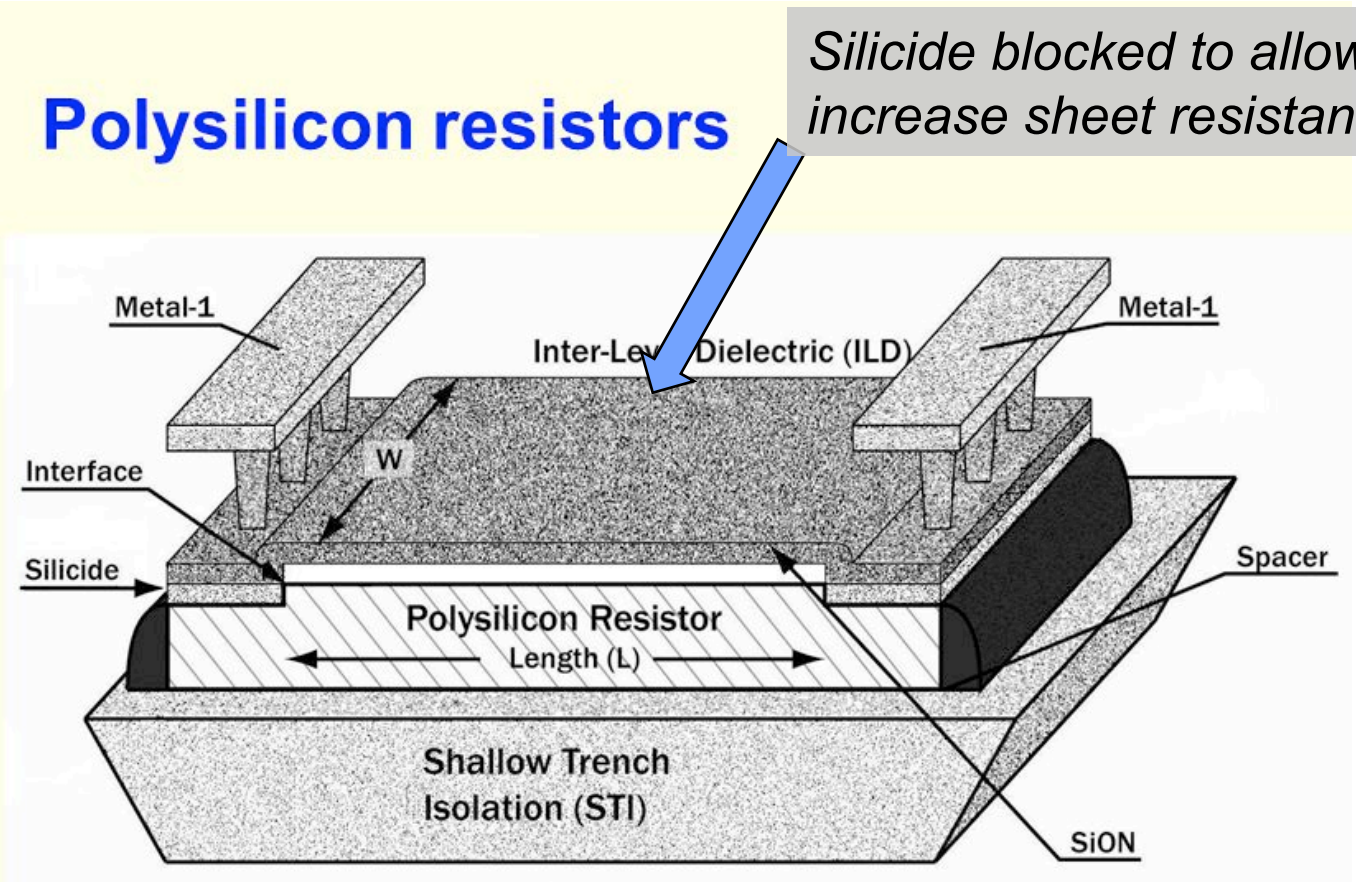
CMOS processes are optimized by adding a metal layer (silicide) to reduce the sheet resistance of diffusions and poly

Resistors – silicide reduces resistance



Silicide is used to reduce the poly and diffusion resistance

Resistors- silicide blocking to save area



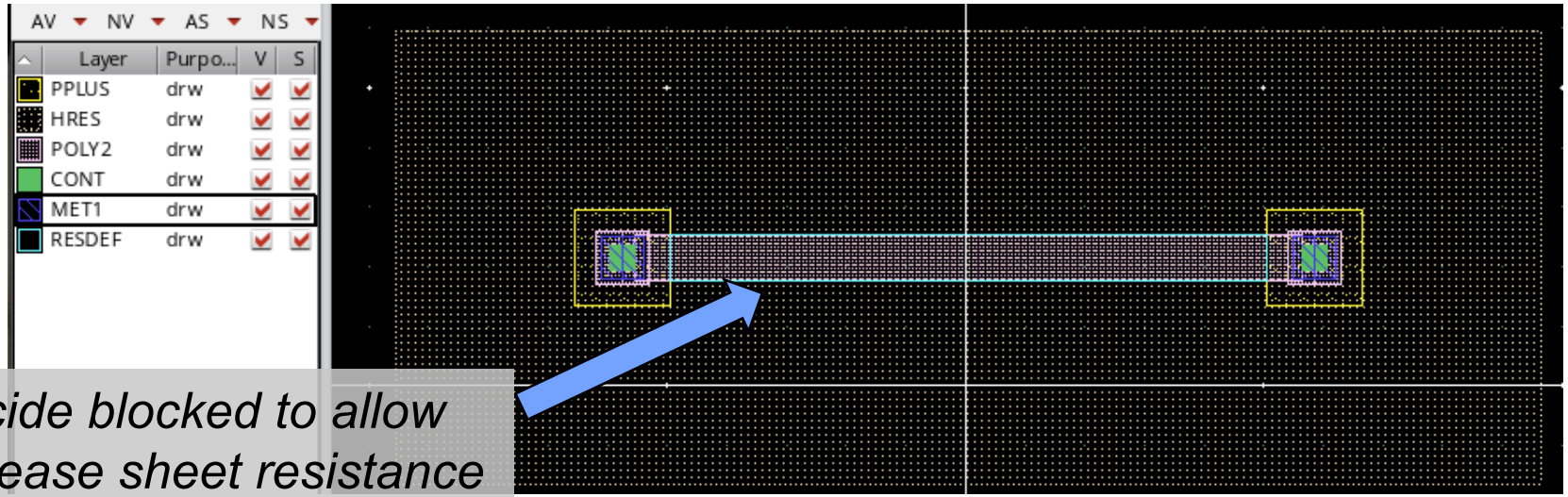
Resistors

higher sheet resistance due to silicide blocking

Parameter	Symbol	Min	Typ	Max	Unit
RPOLYH sheet resistance	RPOLYH	0.9	1.2	1.5	kΩ/□
RPOLYH effective width 0.8 µm	WPOLYH	0.45	0.60	0.75	µm
MET1-RPOLYH contact resistance 0.4x0.4µm²	RCNTMPH		70	150	Ω/cnt
RPOLYH temperature coefficient	TCPOLYH		-0.4		10^{-3}/K
RPOLYH voltage coefficient	VCRPOLYH		-0.8		10^{-3}/V

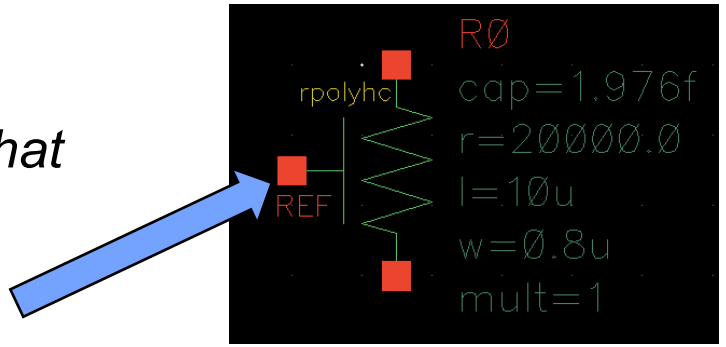
all resistances have temperature dependence (+/-) and nonlinearity (dependence on voltage)

Resistors



Silicide blocked to allow increase sheet resistance

Pin required to identify the node that is the substrate of the resistor, allowing to model the parasitic capacitance to that node



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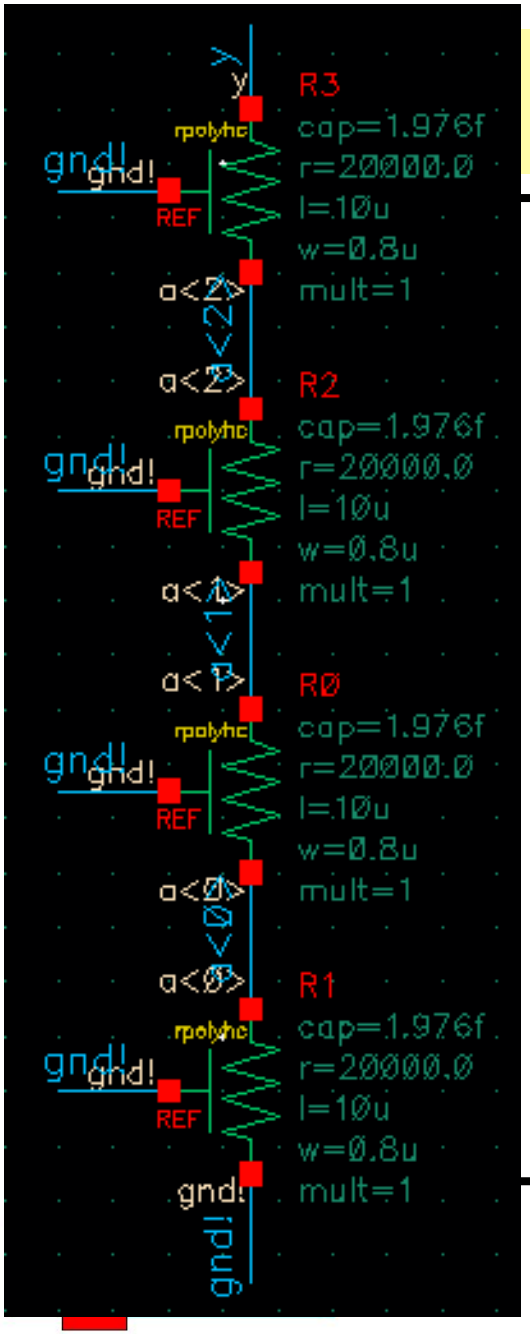
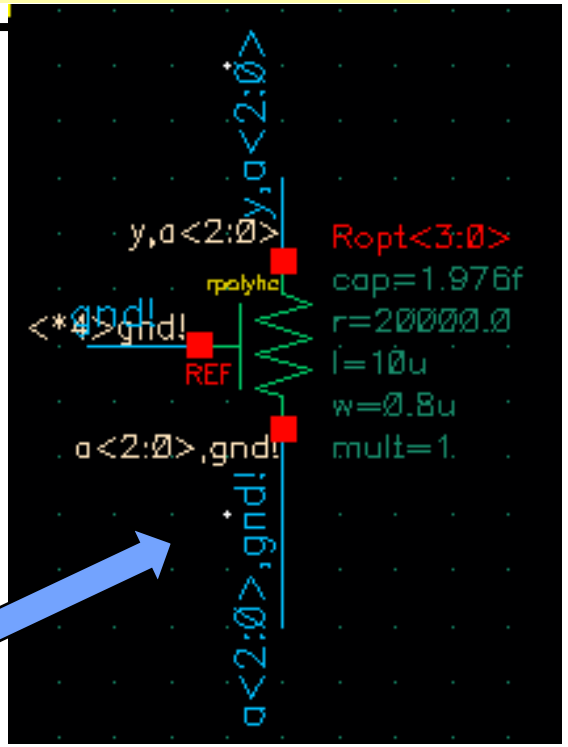
Resistors

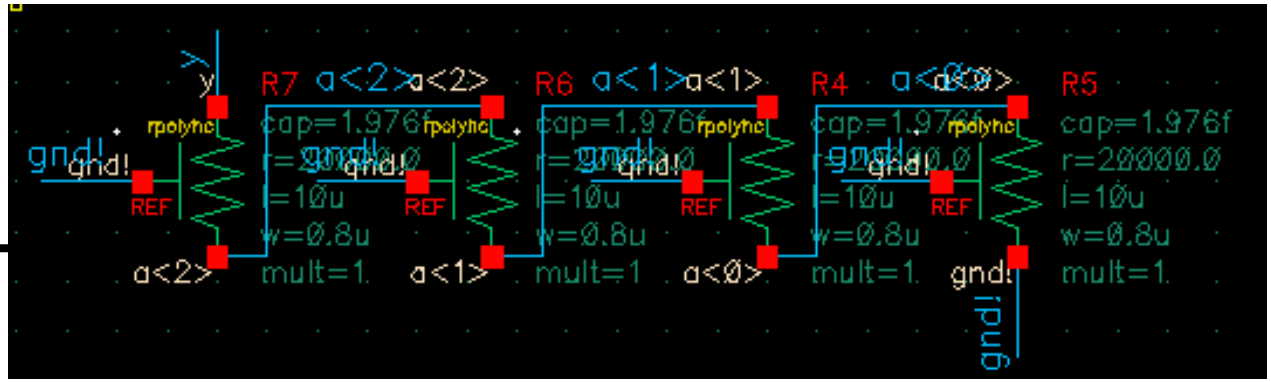
- **Limited max length**
  and
- **Matching**

force the division of one resistance in the sum of several units

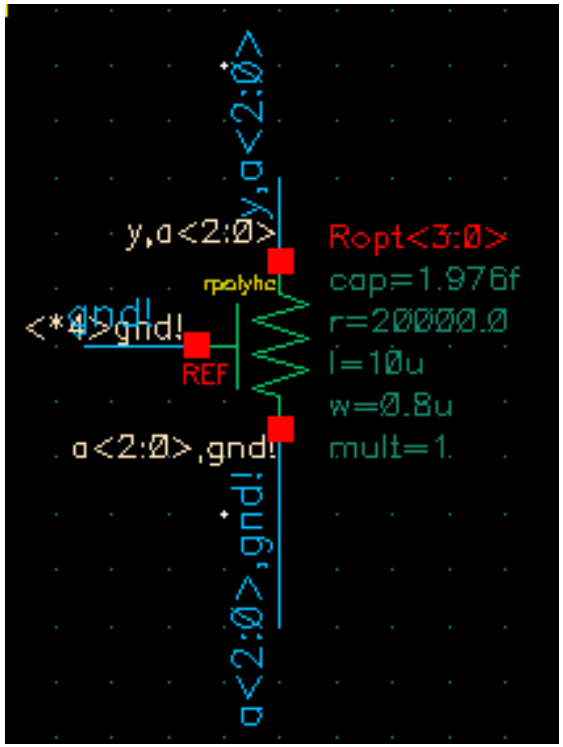
compact representation







Resistors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w=0.8u
a<2:0>,gnd!
mult=1
a<2:0>,gnd!