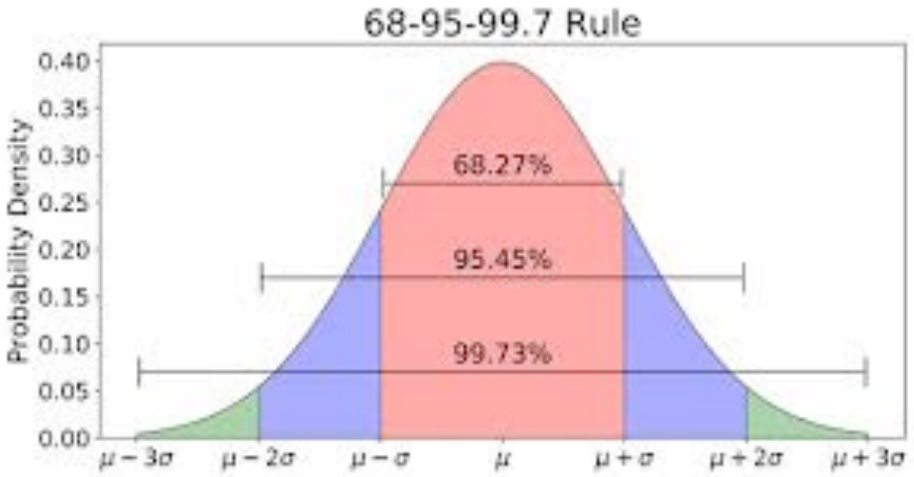
Chapter IV

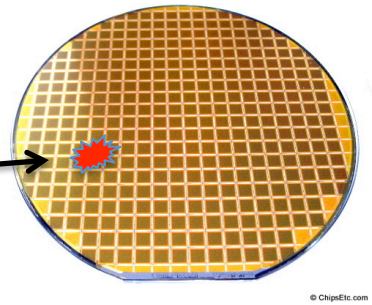
Layout design techniques

- **Design for yield**
- Matching and Vos
- Area optimization
- Routing, current density and noise

Chapter IV – Design for yield

- MOS process is not perfect:
  - All **technology parameters** are characterized **statistically**
  - Manufacturing **defects** are inevitable

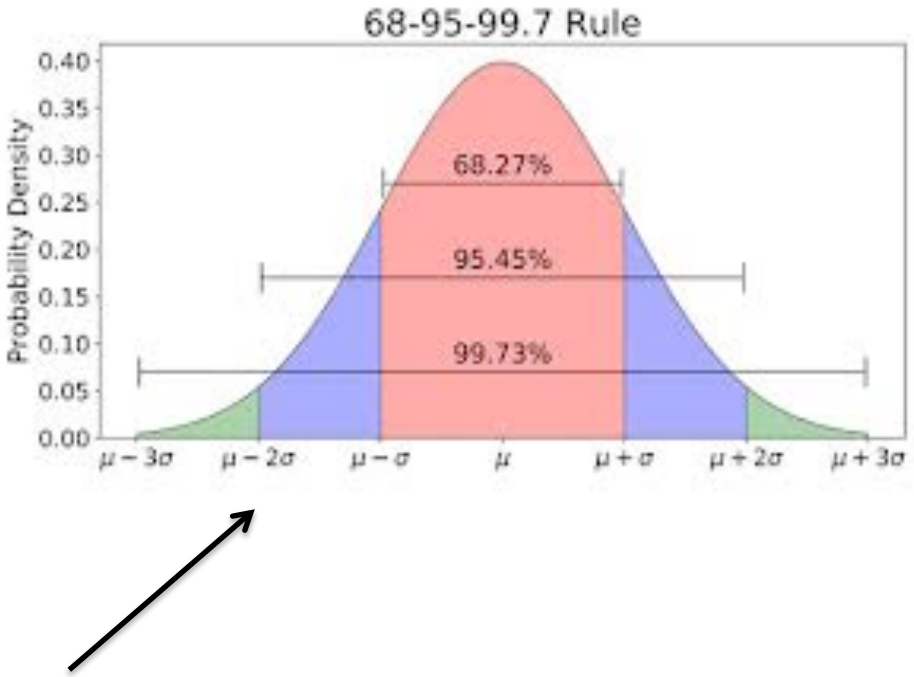




yield < 1 !!!

Chapter IV – Design for yield

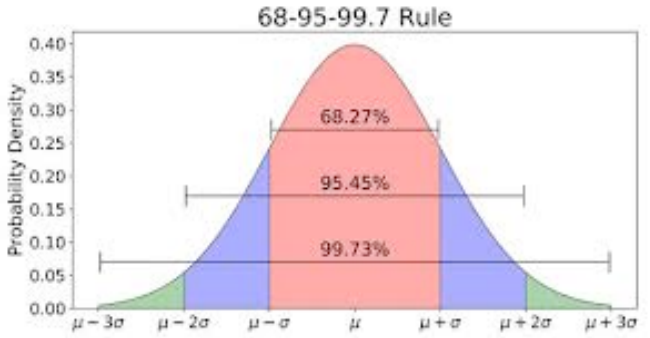
- MOS process is not perfect:
  - All **technology parameters** are characterized **statistically**



Mobility and density of carriers, tox, V_{TH}, sheet resistance, capacity density, all simulation parameters,… are characterized statistically

Chapter IV – Design for yield

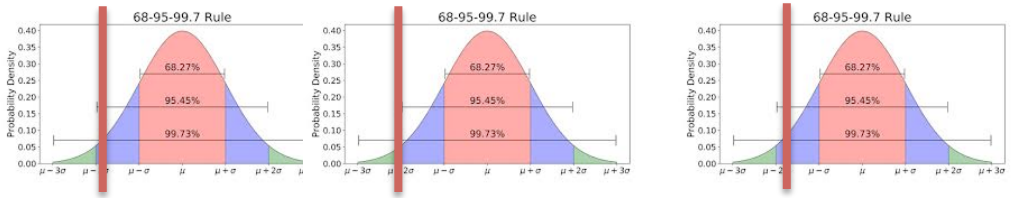
Mobility and density of carriers, tox, V_{TH}, sheet resistance, capacity density, all simulation parameters,… are characterized statistically

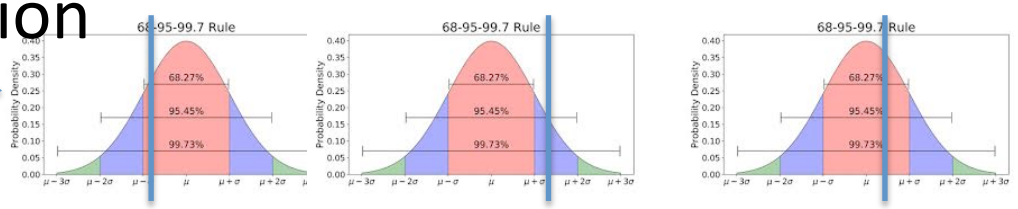


Design must be robust to process parameters variation

Validation through:

- Corner simulation
- Monte Carlo Simulation

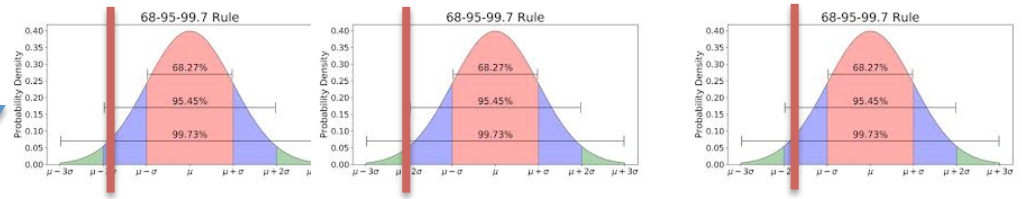




Chapter IV – Design for yield

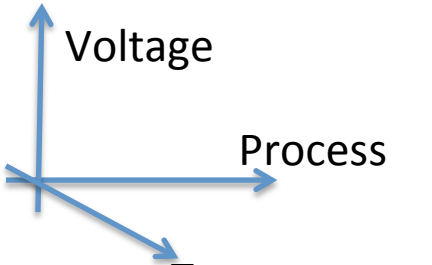
Design must be robust to process parameters variation

Validation through:



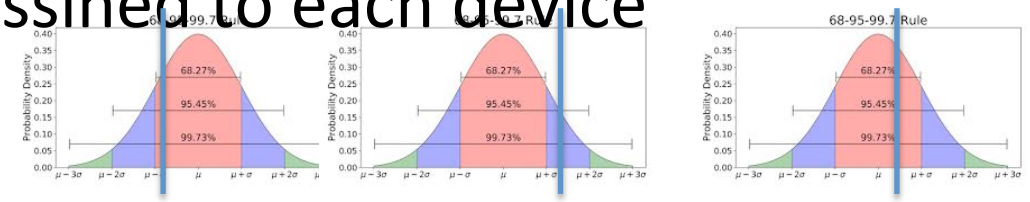
- Corner simulation

  - Simulate with **all combinations of extreme** process, voltage, temperature,…
  (all devices have the same conditions)



- Monte Carlo Simulation

Individual values are assined to each device

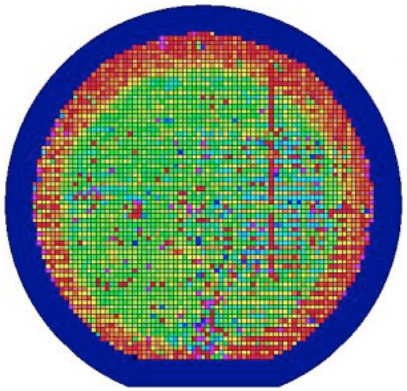


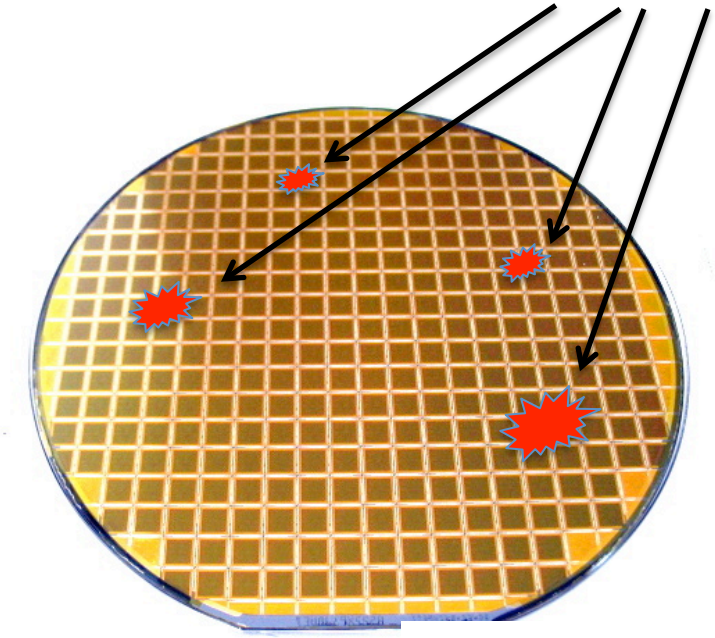
Chapter IV – Design for yield

- MOS process is not perfect:
  - It is characterized by a density of **defects**

(ex: # defects / cm^2)

- Defects can cause:
  - Hard faults
  - Parametric faults



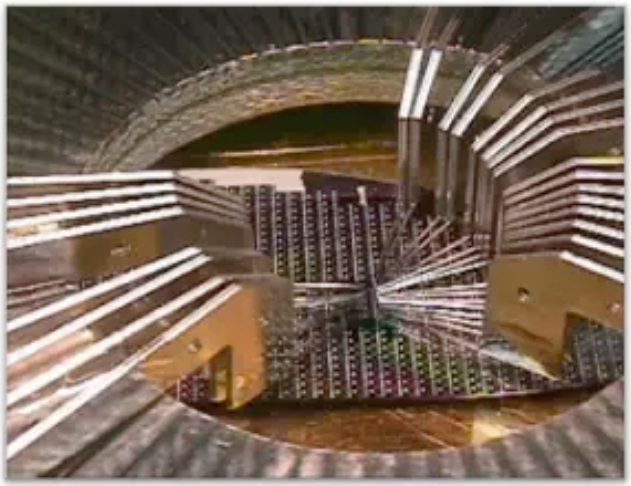


yield < 1 !!!

Chapter IV – Design for yield

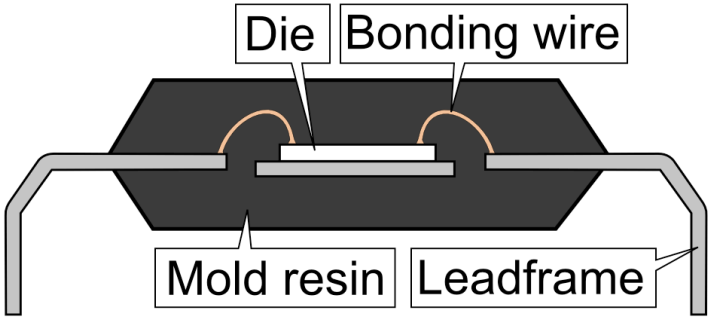
- **Production test** is mandatory to identify defective chips

Wafer-level testing



Package testing

DIP



- Different from characterization test

Chapter IV – Design for yield

- **Fault coverage (FC)** is a metric to quantify the quality of the test

FC = #detected faults / #faults

- FC metric is based on a *fault model* – electrical model of possible impact of defects

Ex: Line-Stuck-At fault model (LSA0, LSA1) assumes that each defect impacts a circuit net like a short to ground or to the supply

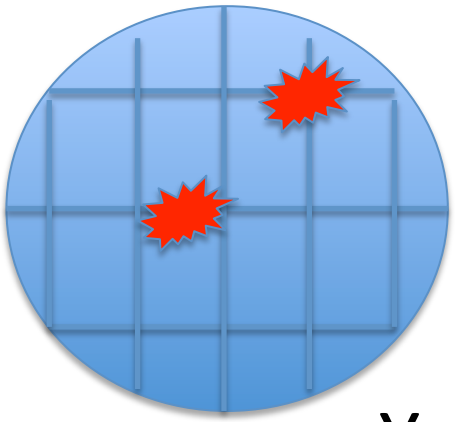
Chapter IV – Design for yield

- Summary of main concepts in IC testing:
  - Defects occur in CMOS process: (yield < 1)
  - Production test is mandatory
  - Fault coverage evaluates test quality

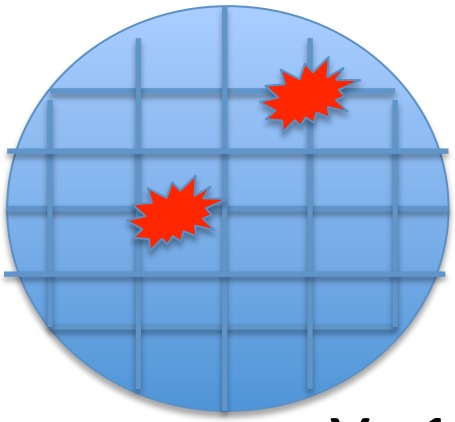
    +
  - Defect Level = number of defective parts that pass production test (unit is ppm)

Chapter IV – Design for yield

- Minimization of Defect Level through:
  - **Design for high yield**
  - Test preparation for high fault coverage
- Yield increases with **die area reduction**:



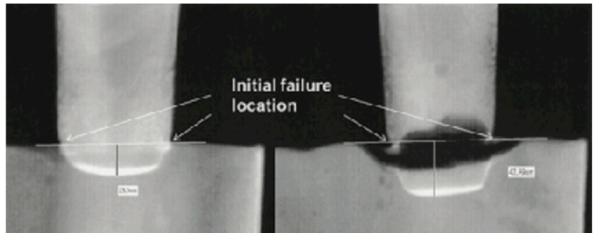
Y=4/8=0.5

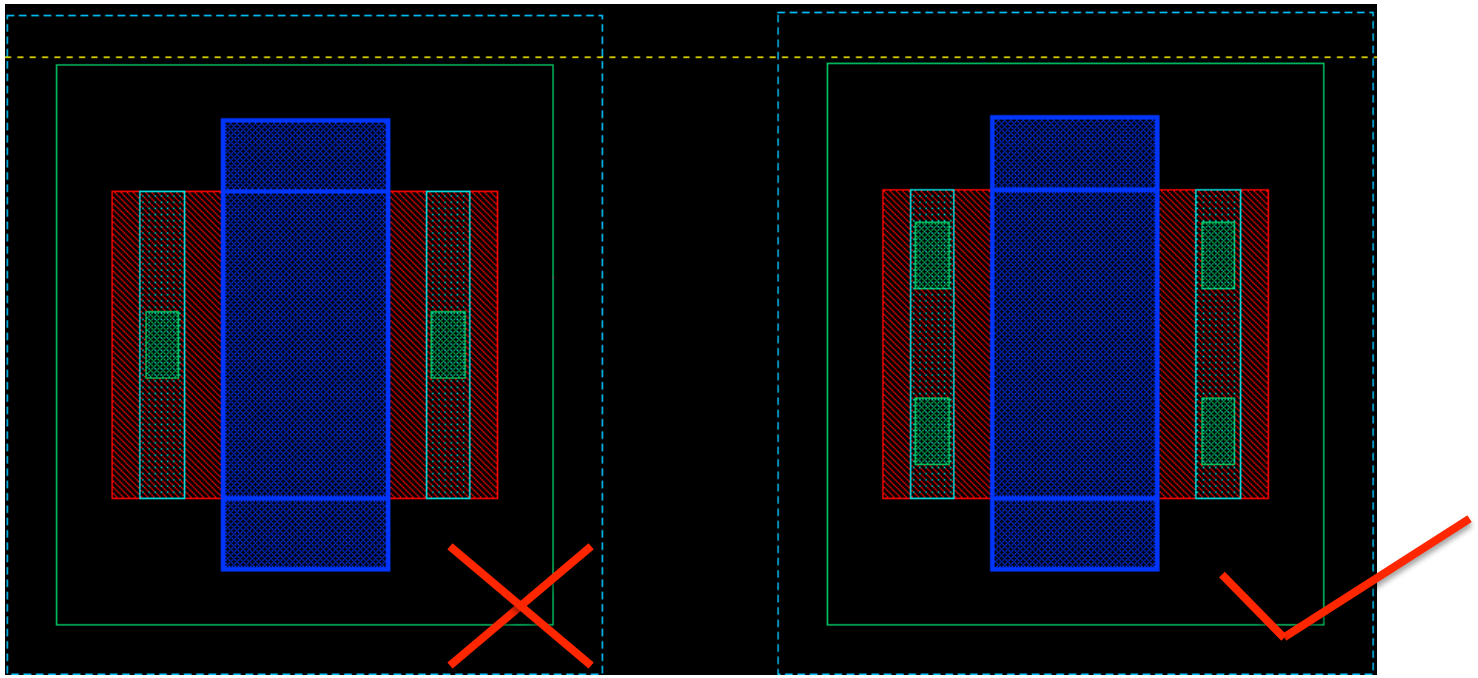


Y=12/16=0.75

Chapter IV – Design for yield

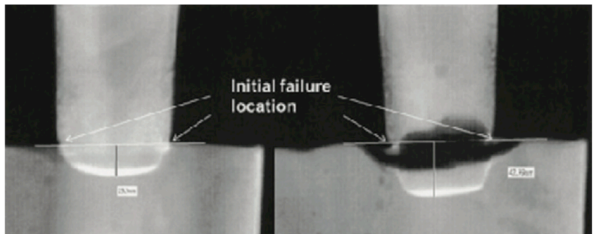
- Die area reduction
- **Add redundancy**

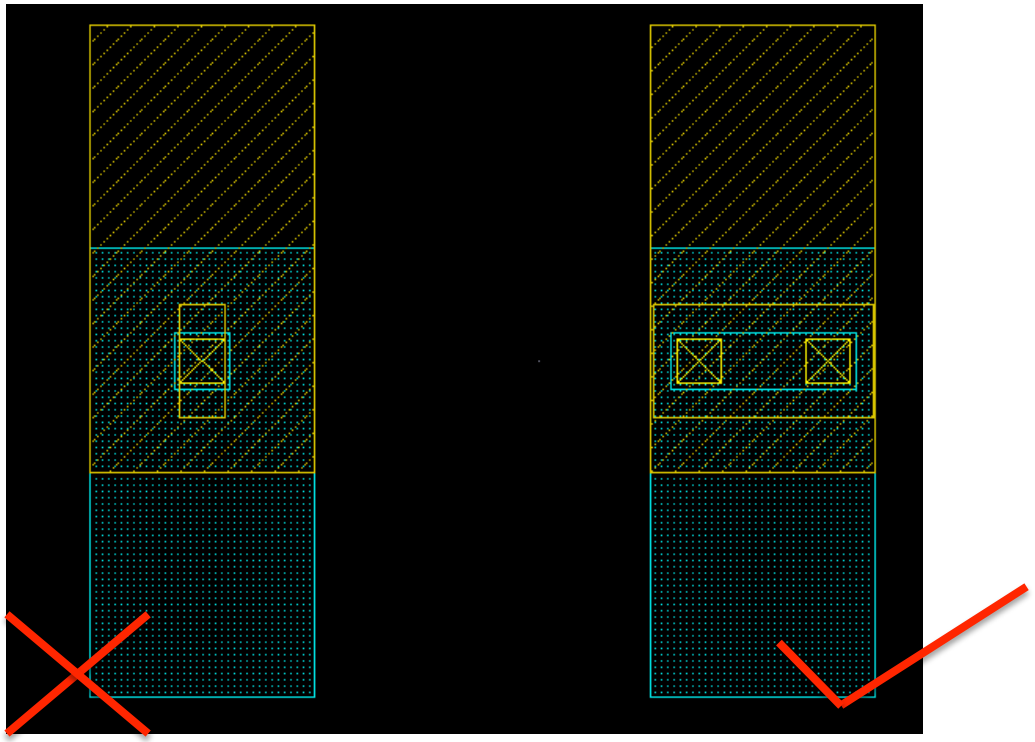




Chapter IV – Design for yield

- Die area reduction
- **Add redundancy**

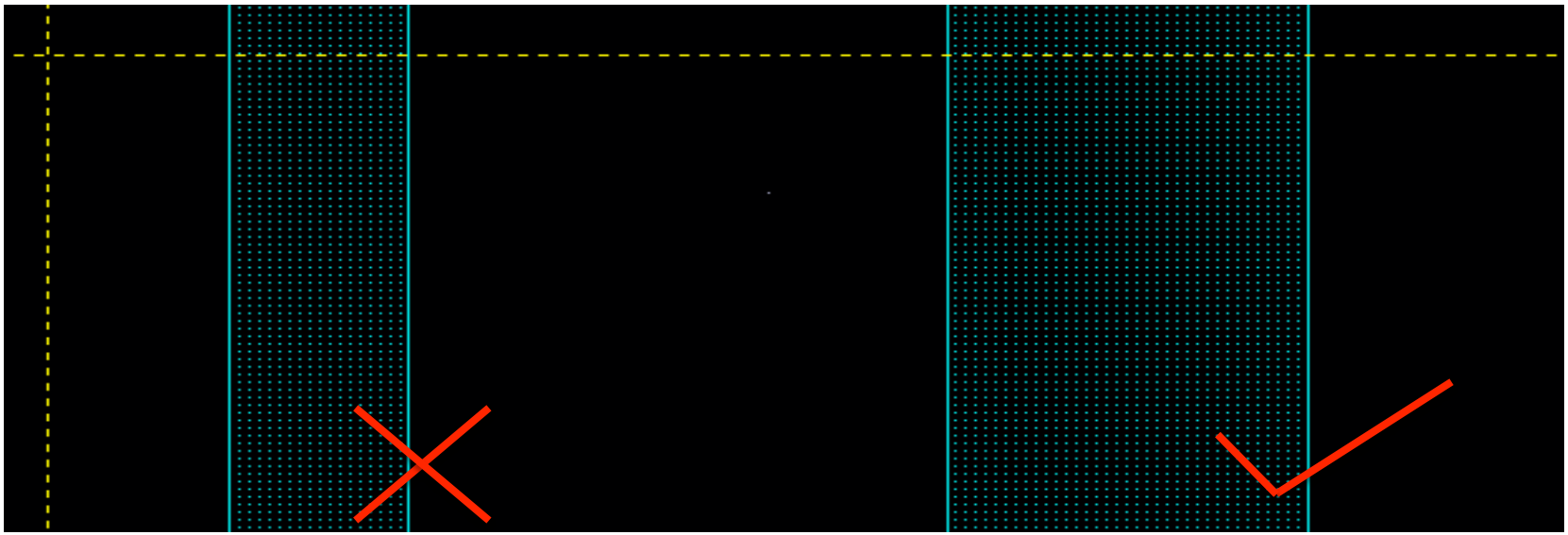




Chapter IV – Design for yield

- Die area reduction
- Add redundancy
- **Use DFY / DFM design rules**

(design for yield / design for manufacturability)



Chapter IV

Layout design techniques

- Design for yield
- **Matching and Vos**
- Area optimization
- Routing, current density and noise

Chapter IV – Matching

Matching is required when the circuit performance depends on the **correlation between parameters of different devices**

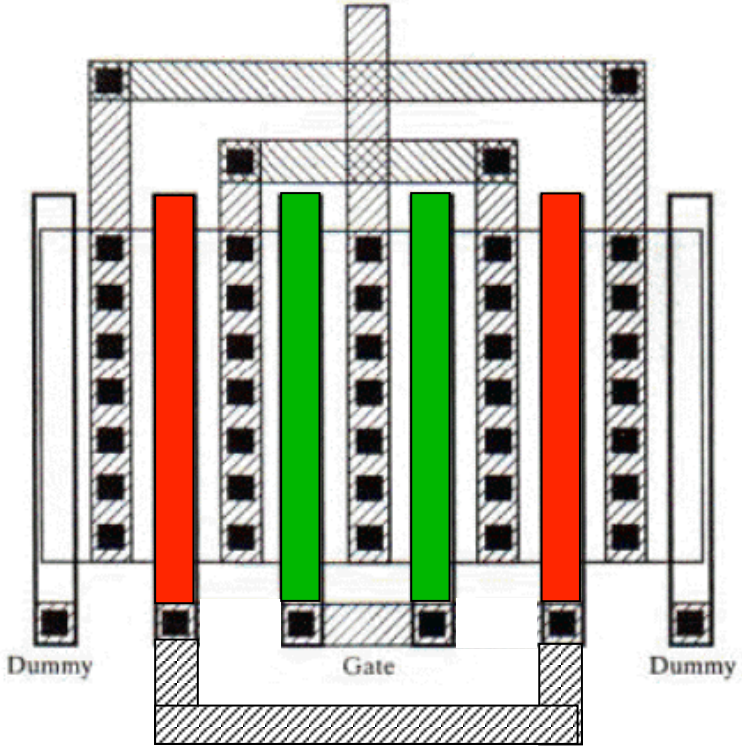
Examples of circuits where matching is mandatory:

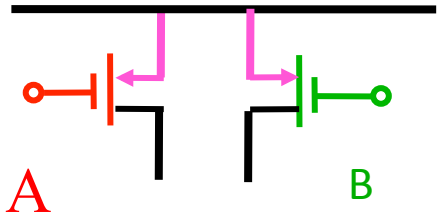
- Differential pairs – in order to limit the offset voltage (Vos)
- Current mirrors – in order to limit the current mirror error
- Resistive divider – in order to limit the division error and to minimize area
- Switching capacitors – in order to limit function error

Chapter IV – Matching

Common-Centroid Layout:

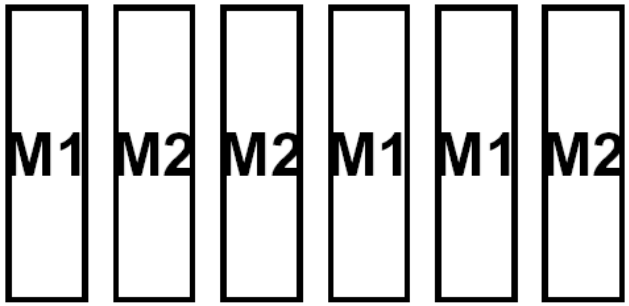
Matching obtained by dividing the gates in two



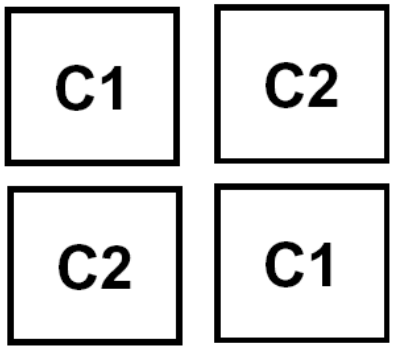


Topology: $_{D}A_{S}B_{D}B_{S}A_{D}$

Chapter IV – Matching



Interdigitized



Common centroid

Chapter IV – Matching

Examples of interdigitized MOS topologies:

1. $({}_{D}A_{S}B_{D}B_{S}A)_{D}$ — *A:B = 1:1*

2. $({}_{S}A_{D}A)({}_{S}B_{D}B_{S}B_{D}B)({}_{S}A_{D}A_{S})$

3. $({}_{S}A_{D}A_{S}B_{D}B)_{S}(B_{D}B_{S}A_{D}A_{S})$

4. $({}_{S}A_{D}A_{S}B_{D}B_{S}A_{D}A)_{S}$ — *A:B = 2:1*

5. $({}_{S}A_{D}A_{S}B_{D}B_{S}C_{D}C)_{S}(C_{D}C_{S}B_{D}B_{S}A_{D}A_{S})$ — *A:B:C = 1:1:1*

Chapter IV – Matching

Common-Centroid layout design guidelines:

1. **Placement**: The geometric center of the devices to match must be very near

2. **Symmetry**: The layout of the devices must be evenly distributed in both directions: x and y

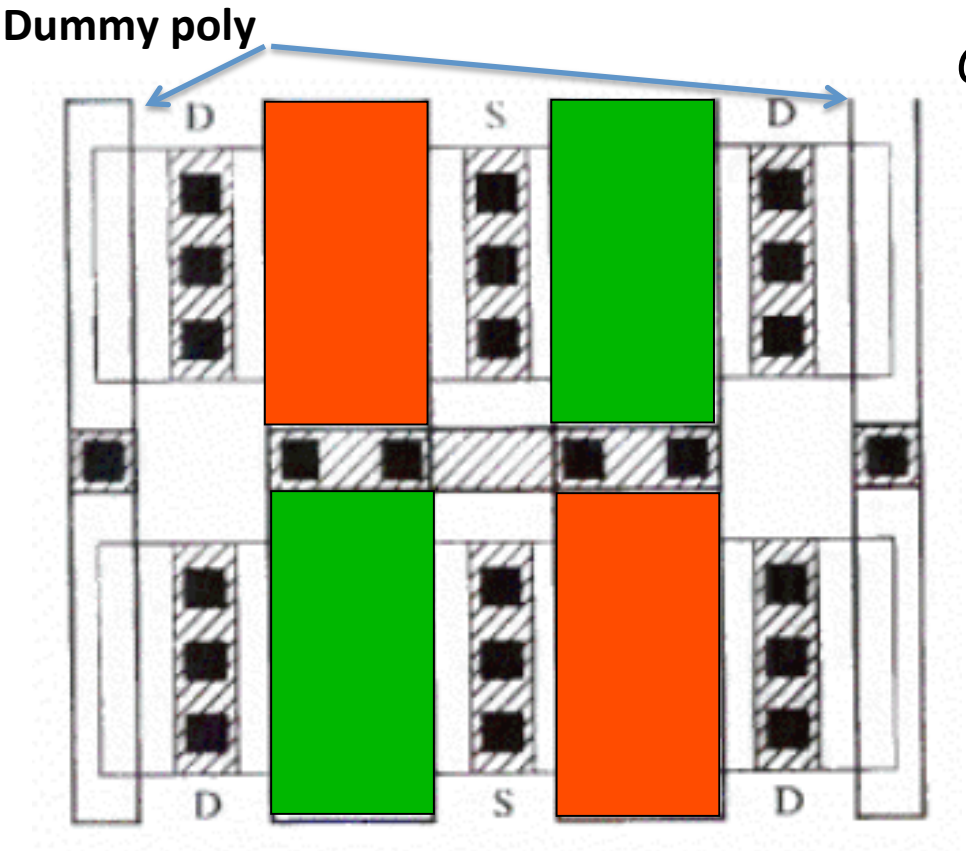
3. **Regularity**: Partial devices must be distributes uniformly

4. **Dispersion**: The layout must be as compact and square as possible

5. **Orientation**: The number of partial devices oriented in each direction must be the same for each device to be match

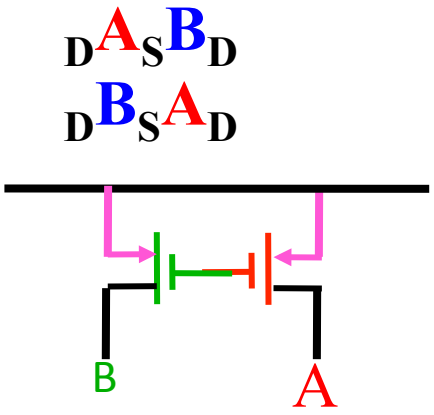
6. **Dummys**: ensure that devices at the perimeter of the structure are produced in the same conditions as devices internal to the structure

Chapter IV – Matching



Common-Centroid

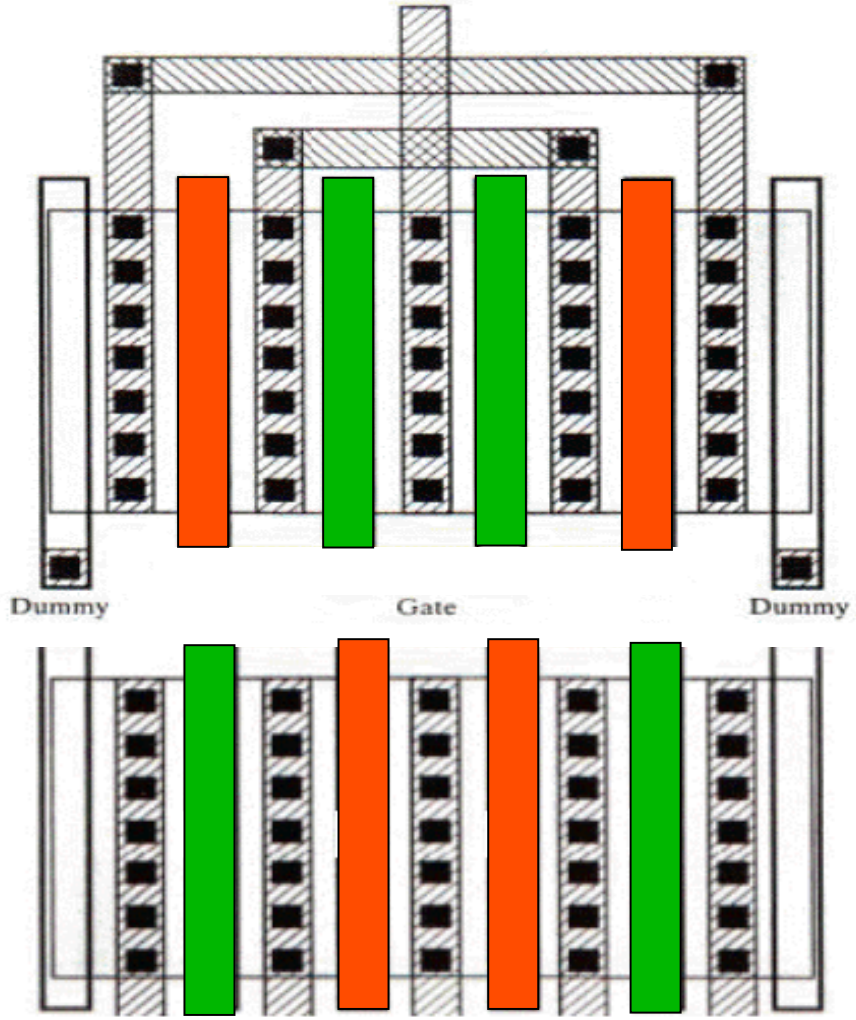
Dividing each transistor in two transistors



- A B / B A compliant with the orientation guideline

Dummy transistors are also placed (and connected accordingly) in the schematic in order to ensure a clean LVS

Chapter IV – Matching

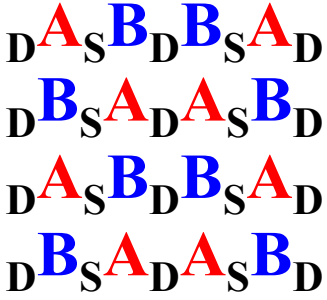


Common-Centroid

Dividing each transistor in 4 transistors

$_{D}A_{S}B_{D}B_{S}A_{D}$
$_{D}B_{S}A_{D}A_{S}B_{D}$

Chapter IV – Matching



Common-Centroid

Vos in the differential the pair

$$V_{OS} = V_O / A_d \qquad A_d = g_{m\_diff} r_{o4} // r_{o2}$$

$$\sigma(\Delta V_T) = \frac{A_{VT}}{\sqrt{W \cdot L}} \qquad V_{O\_diff} = g_{m\_diff} r_{o4} // r_{o2} \times \Delta V_{T\_diff}$$

$$V_{OS\_diff\_\max} = \Delta V_{T\_diff} = \frac{3 A_{VT}}{\sqrt{W_{diff} L_{diff}}} \qquad (A_{VT} \approx 0.1\ t_{ox})$$

99,7%

- Transistors of the diff pair need to be large in order to limit V_{OS}
- Rule of thumb: $W*L > 25um^2$

Chapter IV – Differential pairs

Vos in the differential the pair (c. mirror)

$V_{OS} = V_O / A_d$

$$V_{O\_mirr} = g_{m\_mirr} r_{o4} // r_{o2} \times \Delta V_{T\_mirr}$$

$$A_d = g_{m\_diff} r_{o4} // r_{o2}$$

$$\sigma(\Delta V_T) = \frac{A_{VT}}{\sqrt{W \cdot L}}$$

$$V_{OS\_mirr\_\max} = \frac{3A_{VT}}{\sqrt{W_{mirr} L_{mirr}}} \frac{g_{m\_mirr}}{g_{m\_diff}}$$

$$V_{OS} = \sqrt{\left(V_{OS\_diff}\right)^2 + \left(V_{OS\_mirr}\right)^2}$$

Chapter IV

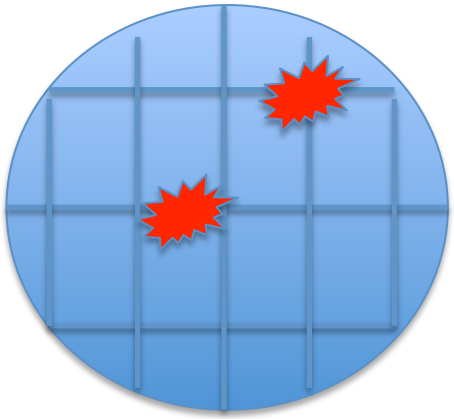
Layout design techniques

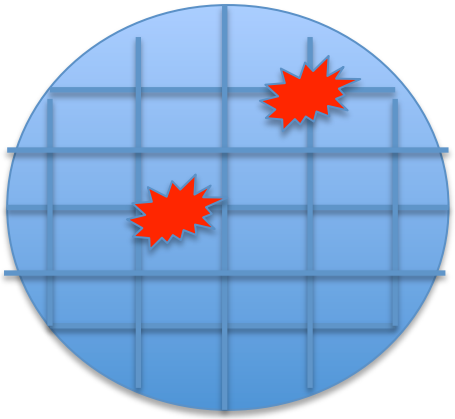
- Design for yield
- Matching and Vos
- **Area optimization**
- Routing, current density and noise

Chapter IV – Area optimization

- Area needs to be minimized since yield increases with **die area reduction**

Ex:





Y=4/8=0.5

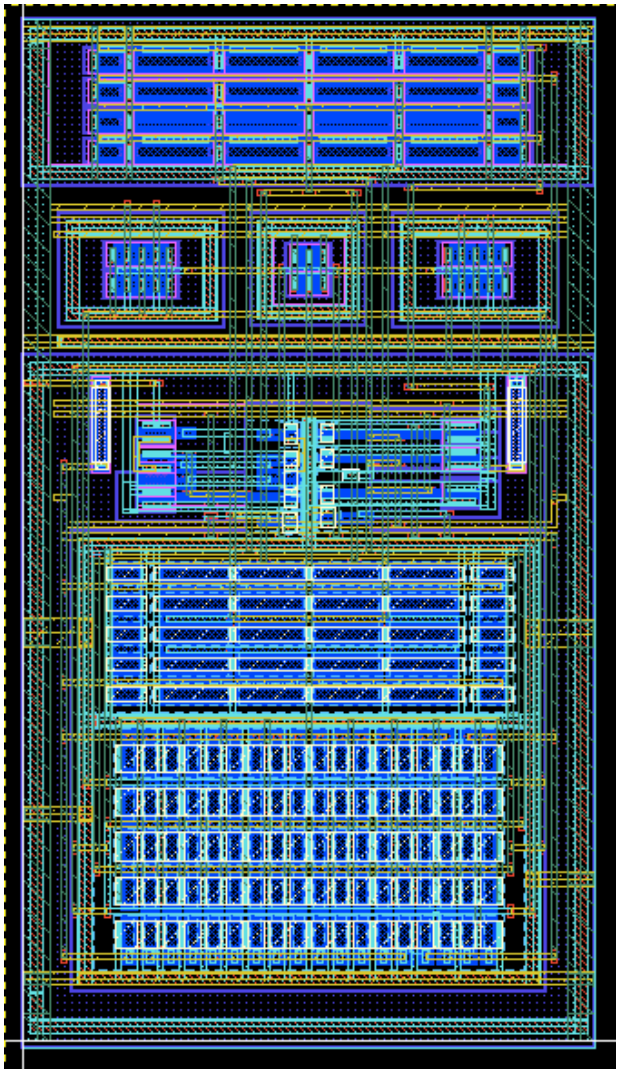
Y=12/16=0.75

Chapter IV – Area optimization

Example of layout of analog circuit (comparator)

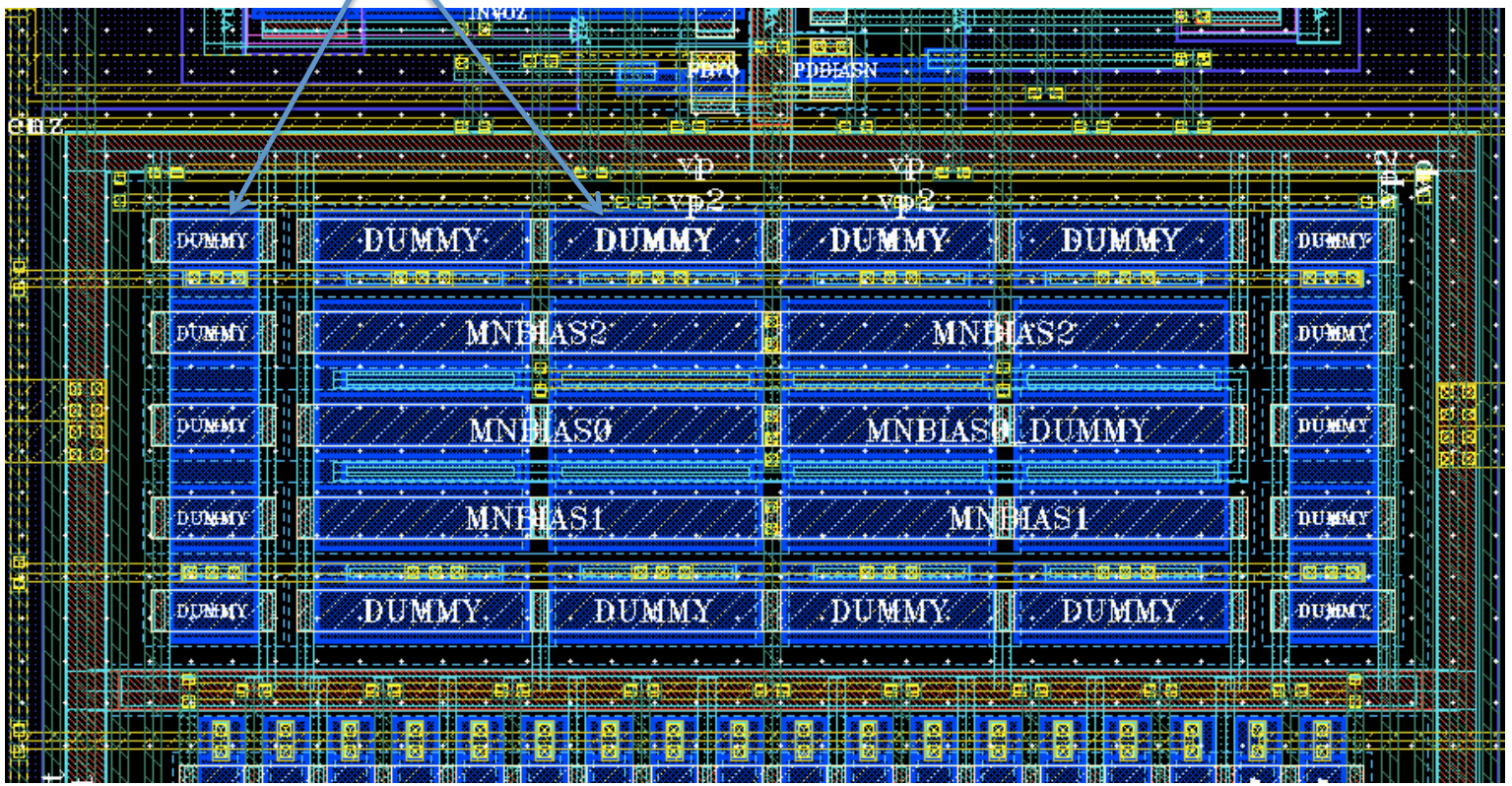
Notice:

- Common centroid design
- Guard rings for bulk biasing and noise shielding
- Compact design (area optimized)

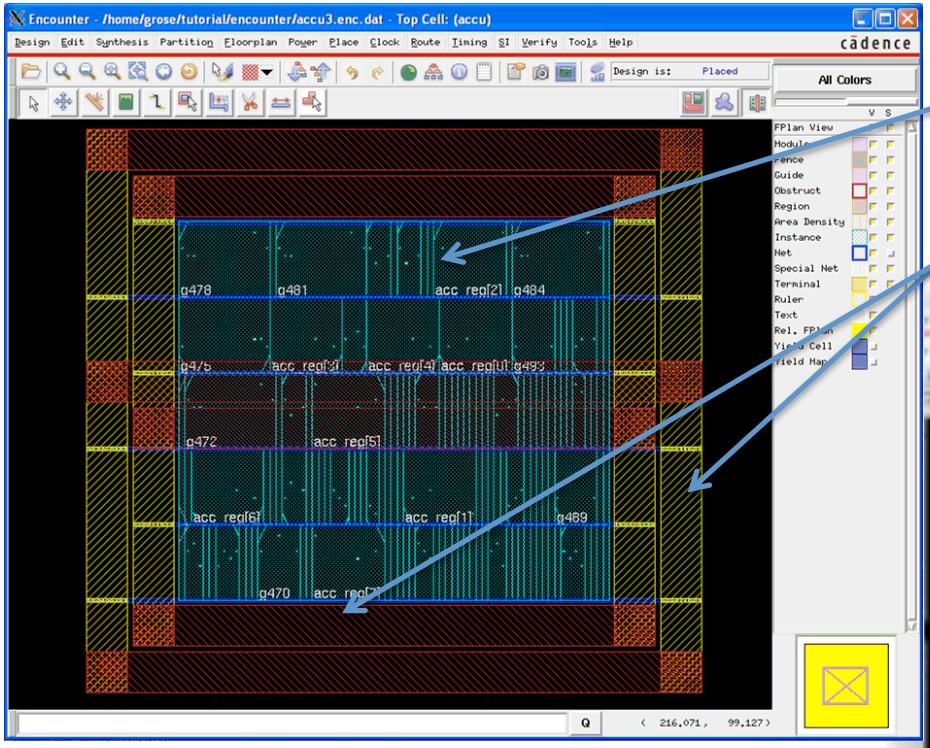


Chapter IV – Area optimization

zoom of previous layout
- Notice dummys around relevant transistors

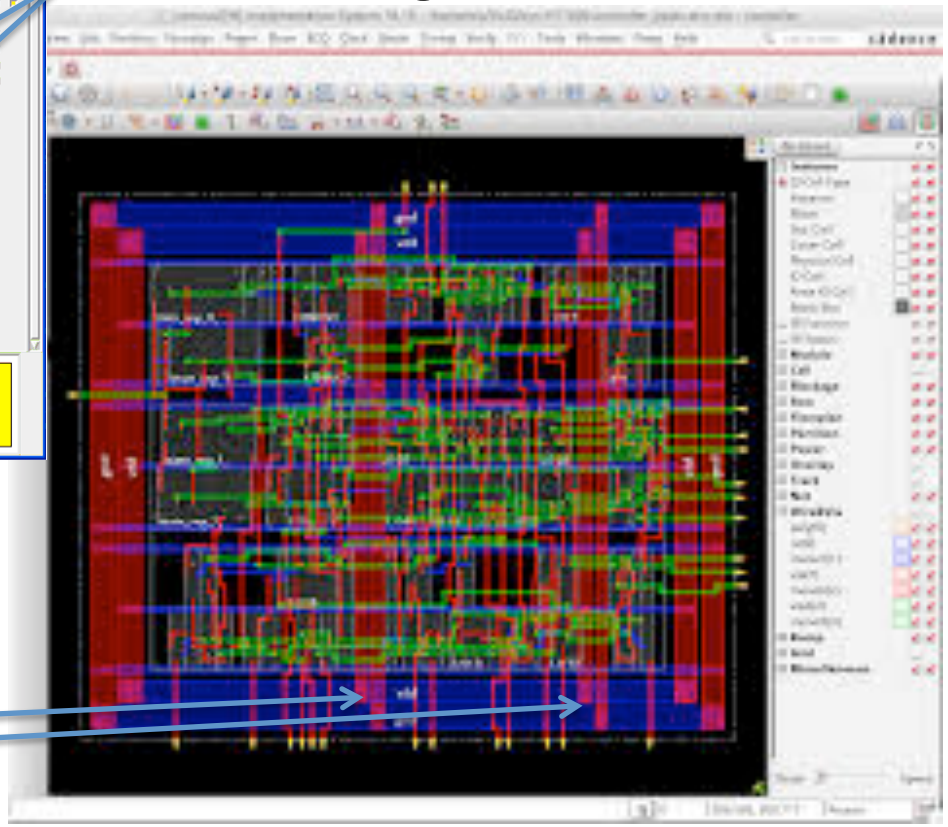


Chapter IV – Area optimization



Digital layout:

- Notice standard cell compact placement and
- Power rings

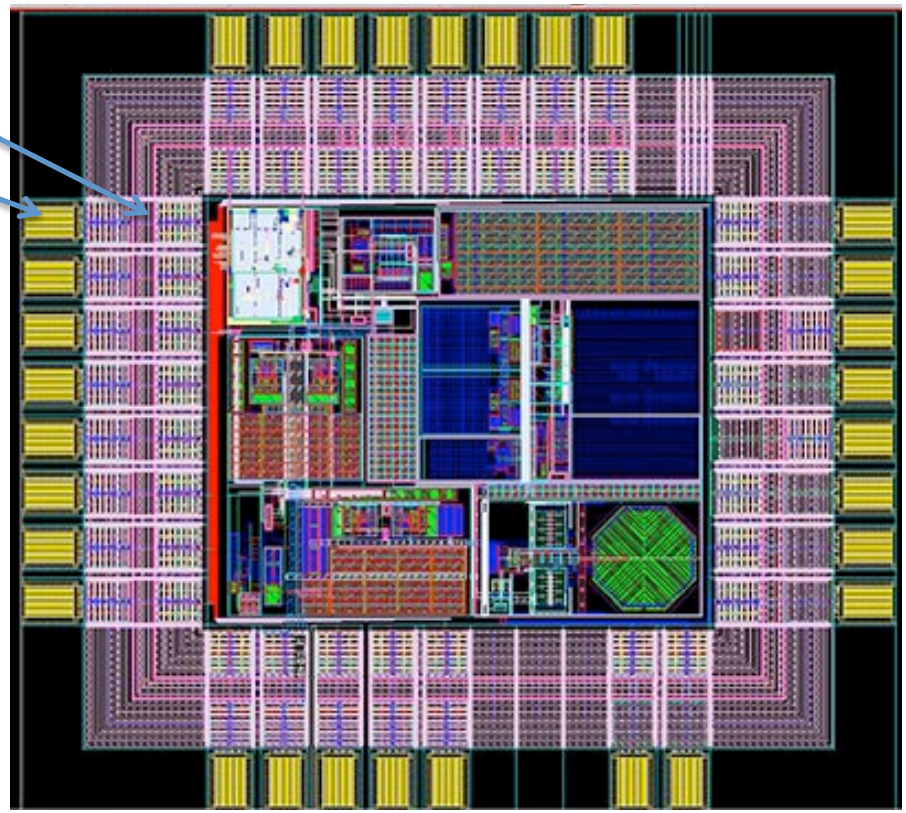


- Routing with higher level metals on the top of cells
- Stripes connected to power rings

Chapter IV – Area optimization

Full chip layout:

- Pads and IO cells with closed IO supply ring
- Hierarchy with different cores
- Near perfect “tetris”
- Digital shape is decided based on available area
- Placement of cores (floorplanning) optimizes:
  - distance between noisy and sensitive signals
  - length of large current connections



Chapter IV

Layout design techniques

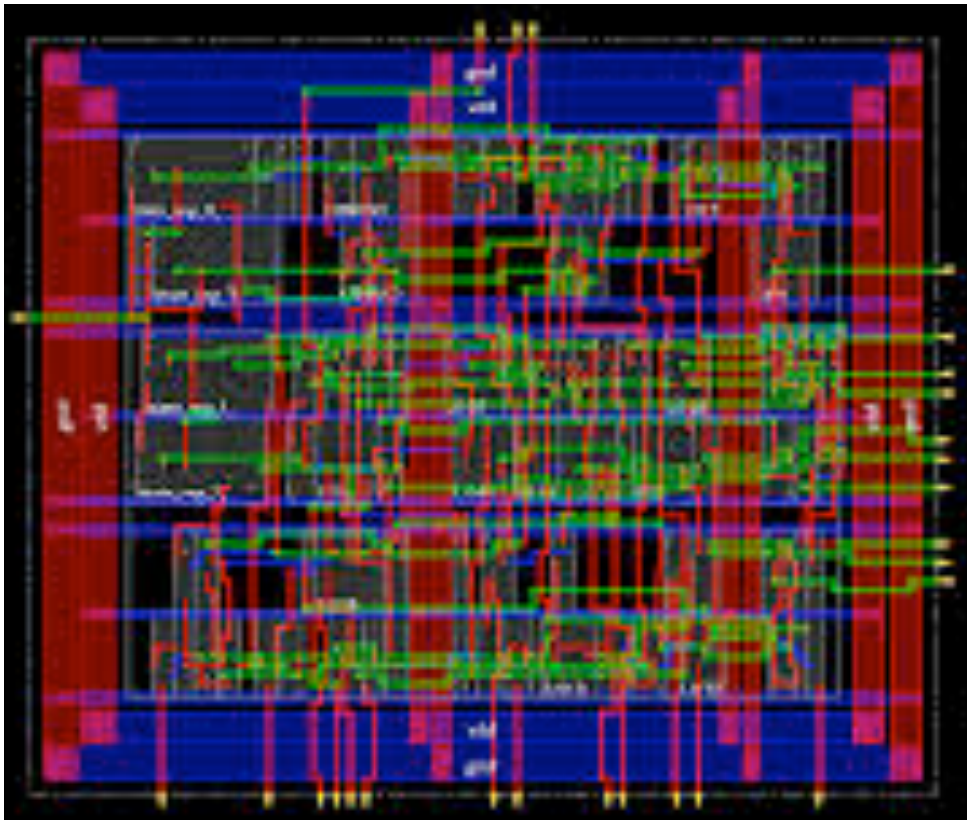
- Design for yield
- Matching and Vos
- Area optimization
- **Routing, current density and noise**

Chapter IV – Routing, current density and noise

- Routing uses odd/even metals for connections with direction

vertical/horizontal or horizontal/vertical

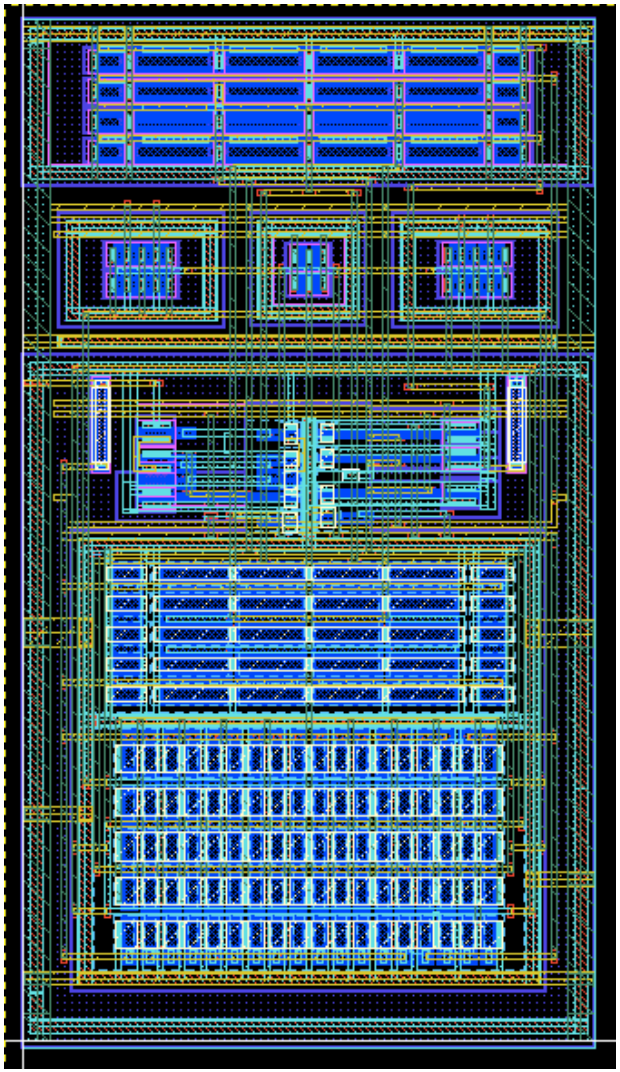
In the digital example:
M1, M3 horizontal;
M2, M4 vertical



Chapter IV – Routing, current density and noise

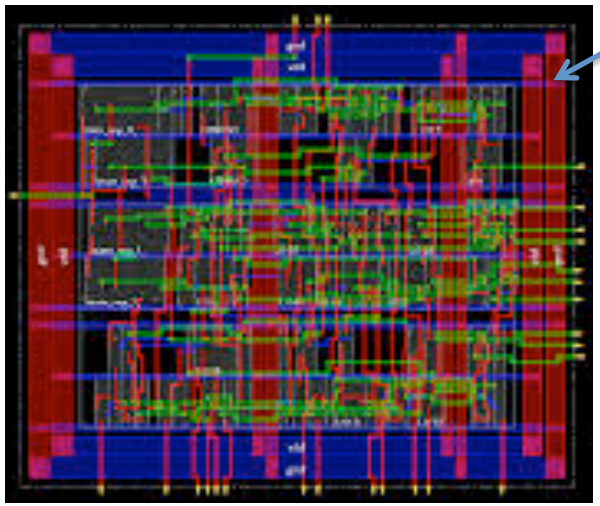
- Routing uses odd/even metals for connections with direction vertical/horizontal or horizontal/vertical

In the analog example:
M1, M3 horizontal;
M2, M4 vertical

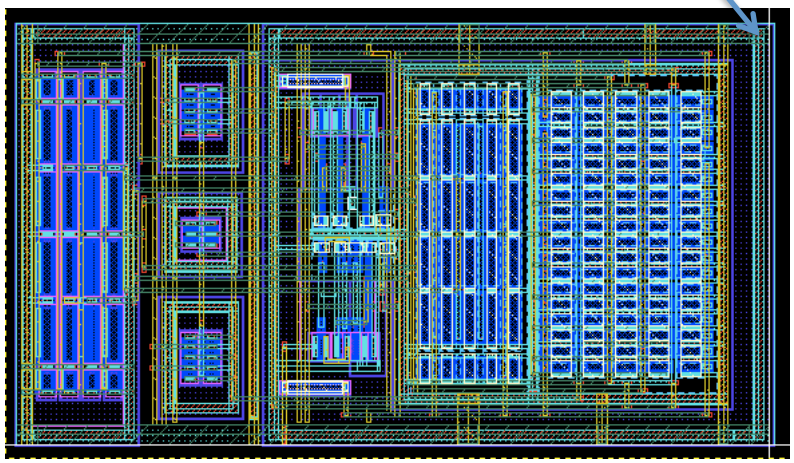


Chapter IV – Routing, current density and noise

- Interconnections require a minimum metal width constrained by:
  - Design for yield − special attention to long lines
  - Resistance − special attention to long lines
  - current density − special attention to nets with large currents



Supply rails are always wider



Chapter IV – Routing, current density and noise

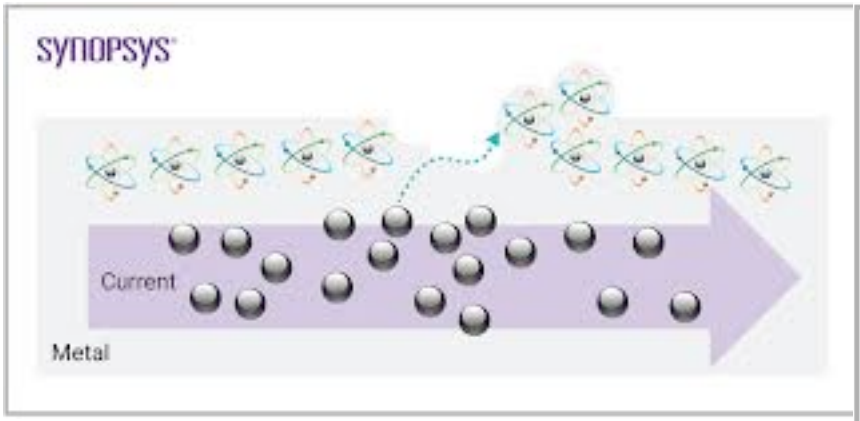
- current density – special attention to nets with large current

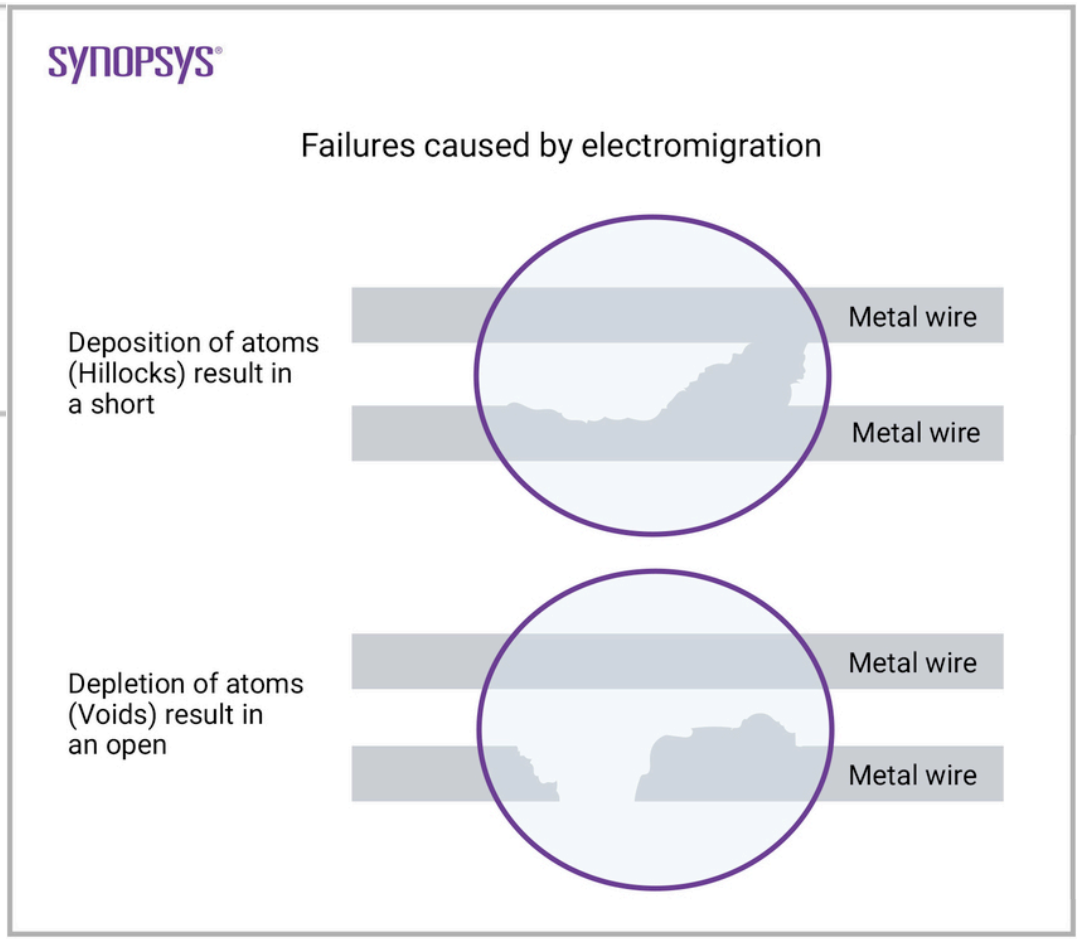
Parameter	Symbol	Min	Typ	Max	Unit
POLY1 current density	JPOLY			0.5	mA/µm
POLY2 current density	JPOLY2			0.3	mA/µm
MET1 current density	JMET			1.0	mA/µm
MET2 current density	JMET2			1.0	mA/µm
MET3 current density valid for triple metal process	JMET3T			1.6	mA/µm
MET3 current density valid for quadruple metal process	JMET3			1.0	mA/µm
MET4 current density	JMET4			1.6	mA/µm

- If current density is exceeded, electromigration will start

Chapter IV – Routing, current density and noise

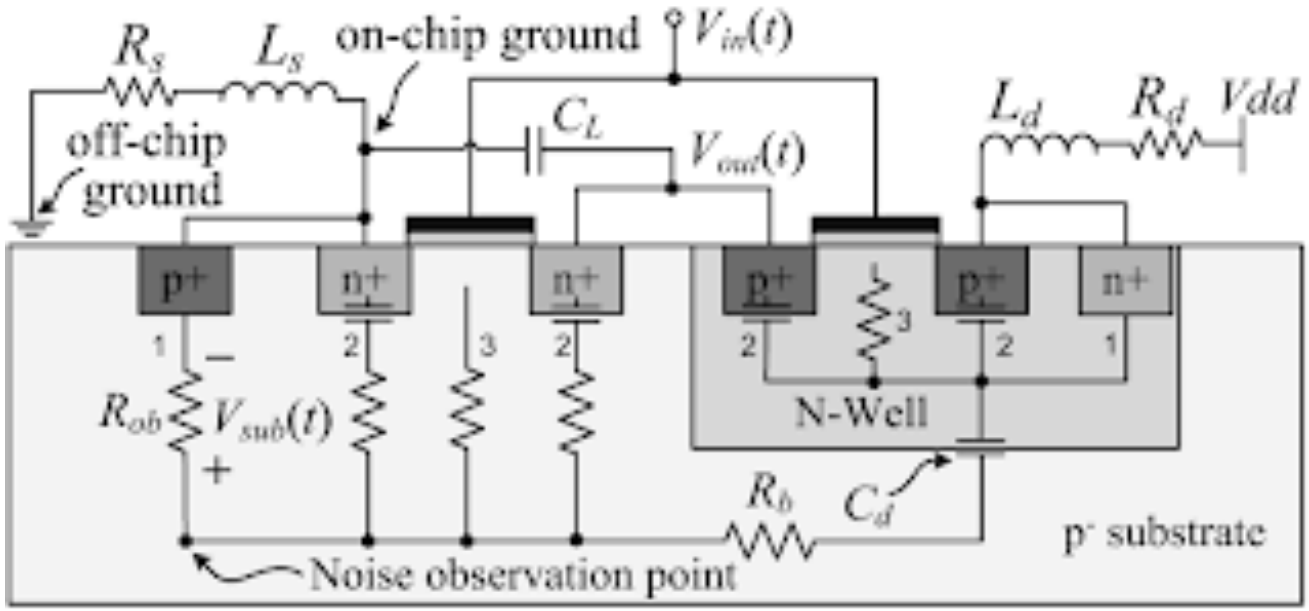
- current density – special attention to nets with large current
  - If current density is exceeded, **electromigration** will start…





Chapter IV – Routing, current density and noise

- Three types of noise:
  - Capacitive and/or resistive coupled switching activity
    - ex: substrate propagated noise, clock signals, etc
  - Noise inherent to electrical current
  - Noise in the power supply



Chapter IV – Routing, current density and noise

- Three types of noise:
  - Capacitive and/or resistive coupled switching activity
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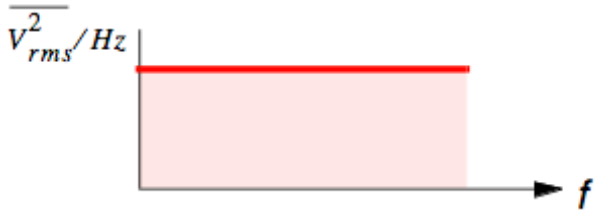
- Mitigation of capacitive or resistive coupled noise:
  - Floorplanning − distance between noisy circuits and sensitive circuits is the best approach
  - Guard rings create a shorter path to supply/ground and reduce substrate noise − use at noise source and at sensitive areas
  - Sensitive signal shielding (can be done vertically and/or horizontally)

Chapter IV – Routing, current density and noise

- Capacitive and/or resistive coupled switching activity
- Noise inherent to electrical current

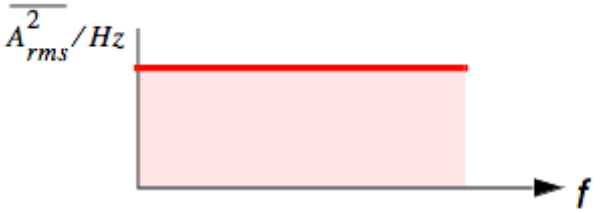
THERMAL • thermal excitation of charge carriers



$$\frac{\overline{V_{rms}^2}}{\Delta f} = 4kTR \text{ , } V^2/Hz$$

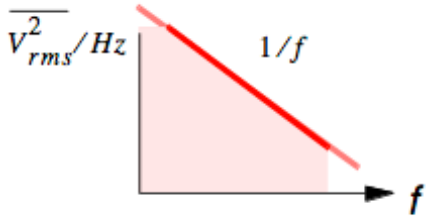
Common trade-off: noise vs power…

SHOT • fluctuations in dc current flow through junctions



$$\frac{\overline{I_{rms}^2}}{\Delta f} = 2qI_{DC} \text{ , } A^2/Hz$$

FLICKER • traps in semiconductors



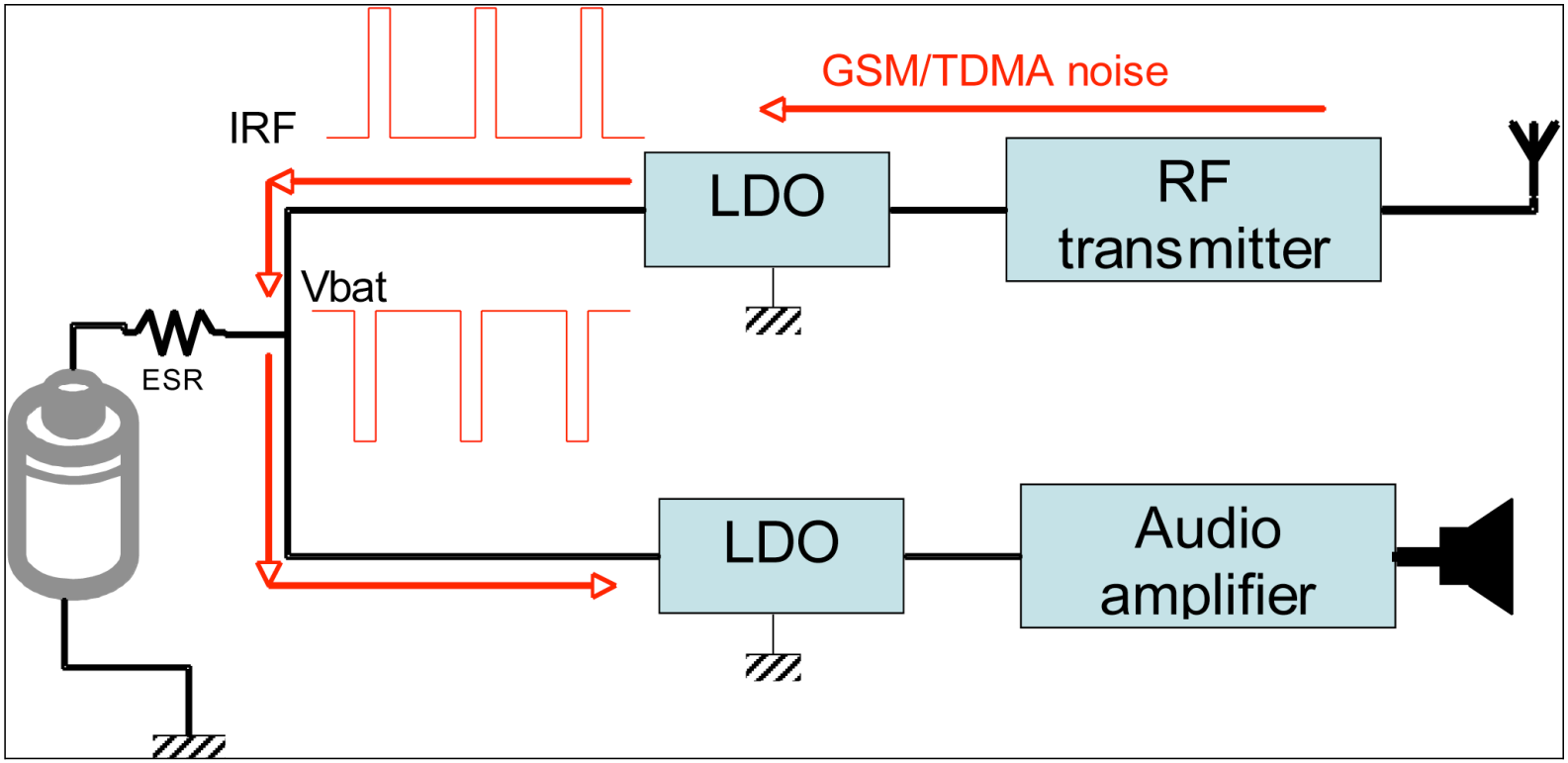
$$\frac{\overline{V_{rms}^2}}{\Delta f} = \frac{K_f \cdot V_{DC}^2}{f} \text{ , } V^2/Hz$$

T = Temperature, K
k = 1.38 x 10^{-23} J/K
q = 1.6 x 10^{-19} C
K_f = Flicker coefficient

Chapter IV – Routing, current density and noise

…Noise inherent to electrical current

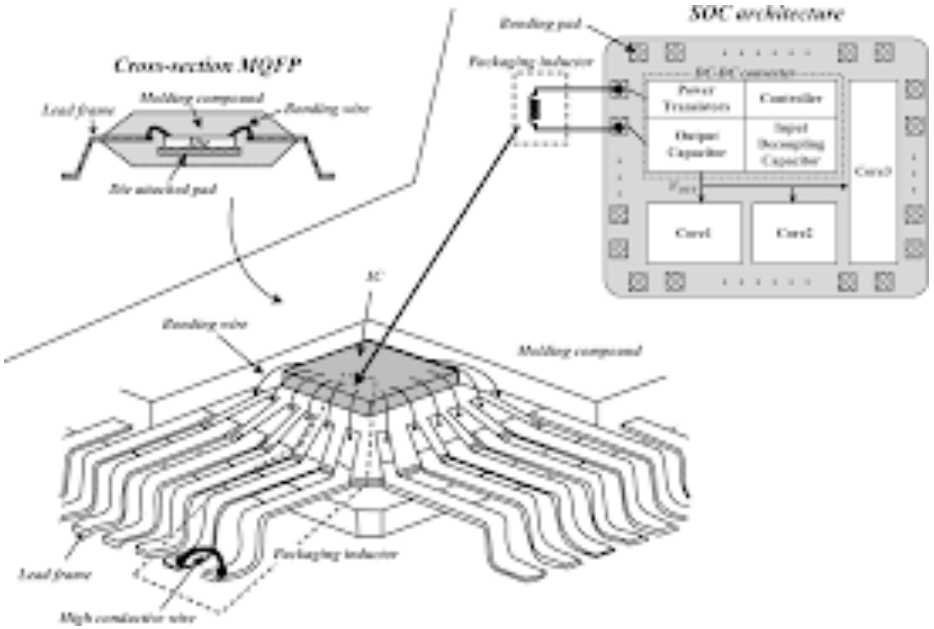
- Noise in the power supply

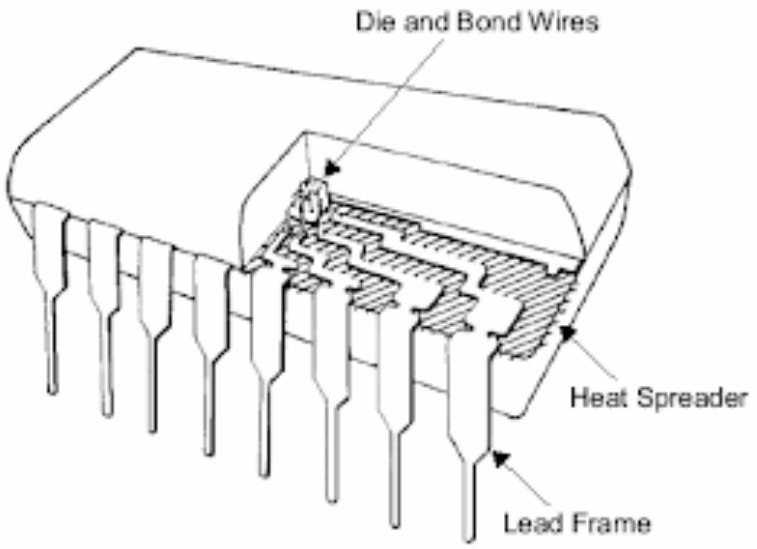


Chapter IV – Routing, current density and noise

…Noise inherent to electrical current

- Noise in the power supply



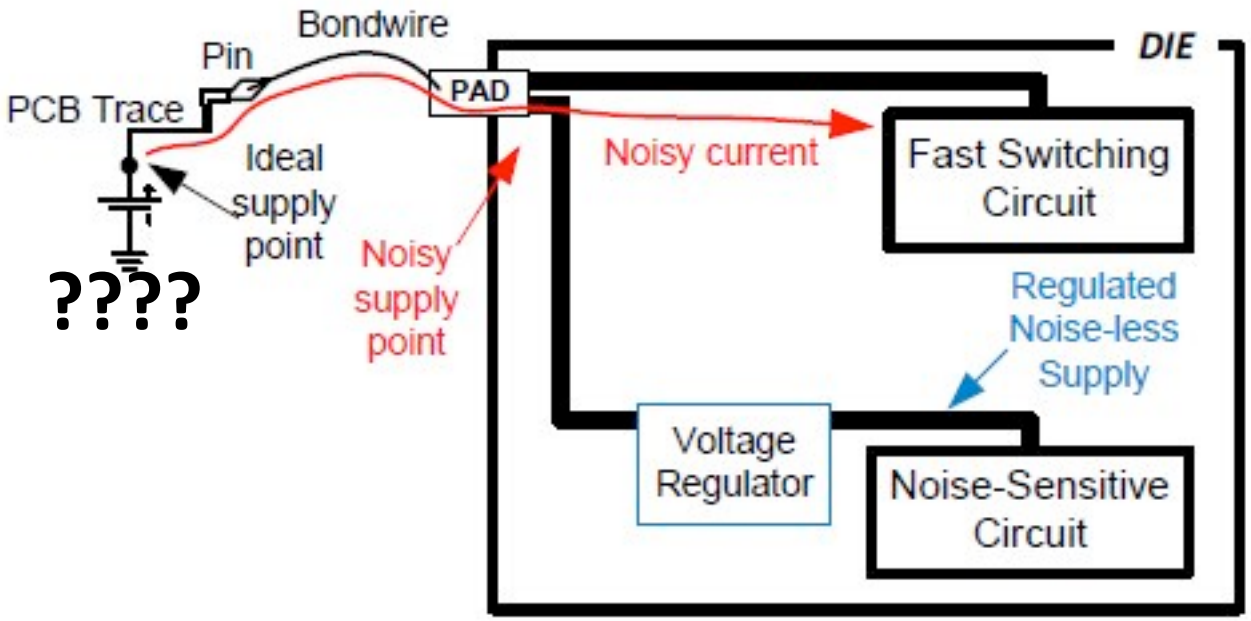


Chapter IV – Routing, current density and noise

…Noise inherent to electrical current

- Noise in the power supply (VCC and GND!!!!)

!!! It is a frequent error to consider only VCC noise and ignore GND noise. Both paths include PCB traces, bonding wires, etc => current transients cause noise on both



Noise on regulated supply depends on PSRR

Chapter IV – Routing, current density and noise

Mitigation:

- Use star connected supply and ground
- Use reference ground signals analog circuits (without current, they wor have noise)
- Use / design high PSRR circuits (saturated transistors help increasing PSRR)