week	Lab	Deliverable date*	Weight	Lectures
09/mai	1st Lab - Simulation in virtuoso ID(VGS), ID(VDS)	18/mai	0.1	Cap 1- Mixed signal design flow / Cap 3 - MOS transistor functions (current source)
16/mai	2nd Lab - Design of a standard cell	25/mai	0.1	Cap 1 - CMOS process steps and sequence, packaging and test
23/mai	3rd Lab - Current mirror study	03/jun	0.2	Cap 2 - CMOS technology devices
30/mai				Cap 3 - MOS transistor functions (switch, voltage limiter and transconductance)
06/jun	4th Lab - Cascode topology study	10/jun	0.3	Cap 3 - Examples of circuits with MOS, OPAMPs and comparators
13/jun	5th Lab - Current reference design	24/jun	0.3	Cap 4 - Layout design techniques
20/jun				Cap 5 - Digital cell design
	Exam		0.5	

* Each day of delay in the deliverable has a penaly of -1 (0-20)