Chapter I

CMOS Technology

- **Mixed-signal design flow**
- Processing steps
- Processing sequence
- Package and test

Chapter I

Mixed-signal design flow

- Cadence virtuoso: CDBOA and technology

- Design flow (tutorial):
  - Schematic entry
  - Simulation
  - Layout design and validation

Mixed signal design flow

Cadence virtuoso: CDBOA and technology

Devices available
Simulation models
Layout design & validation

} technology dependent
- part of Physical Design Kit

Interface
Ideal devices
Design tools

} technology independent
- part of Cadence virtuoso

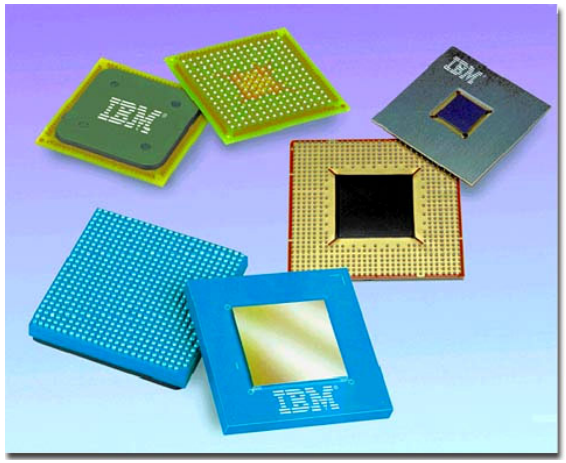
The presentation moves to Cadence virtuoso as support

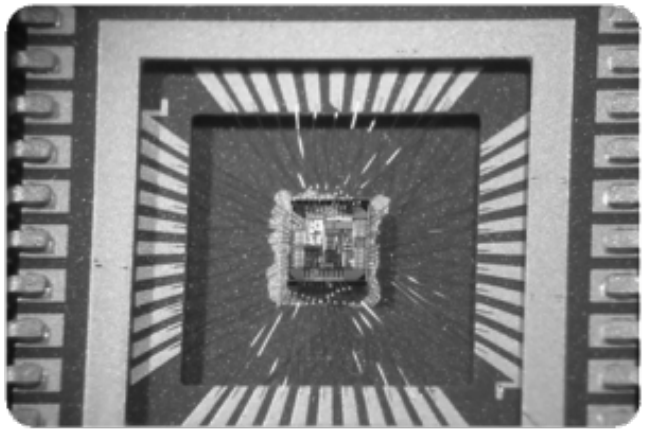
Chapter I

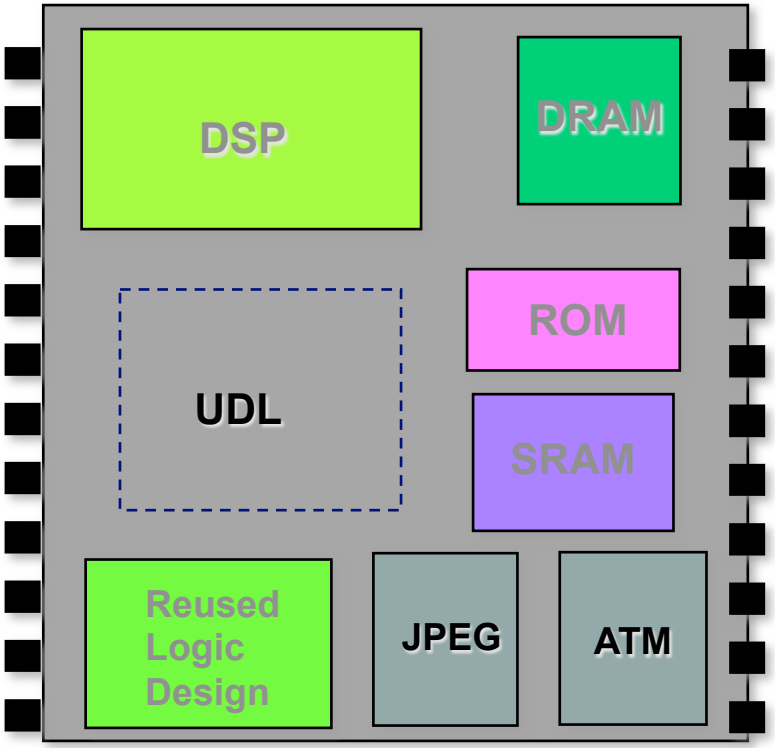
CMOS Technology

- Mixed-signal design flow
- **Processing steps**
- Processing sequence
- Package and test

The *System* on *Chip*

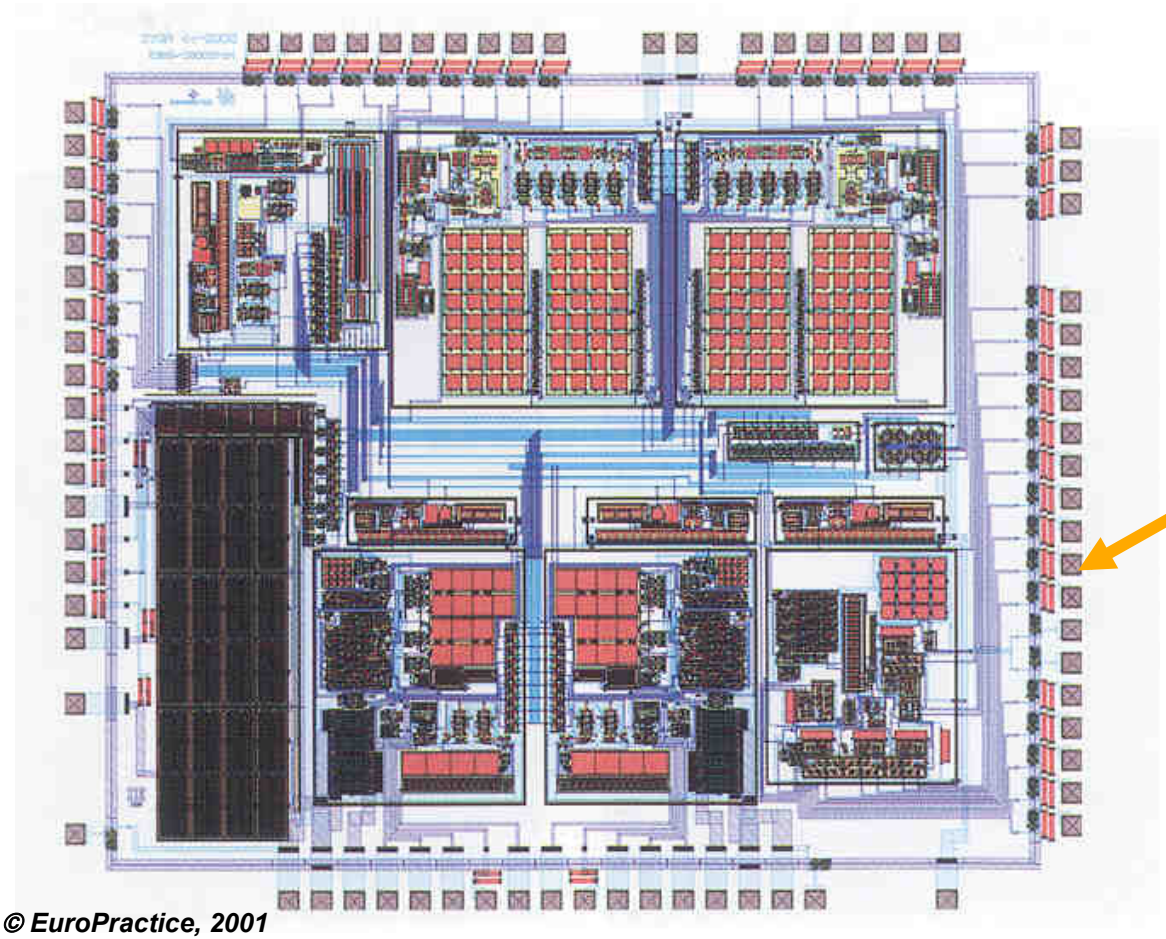






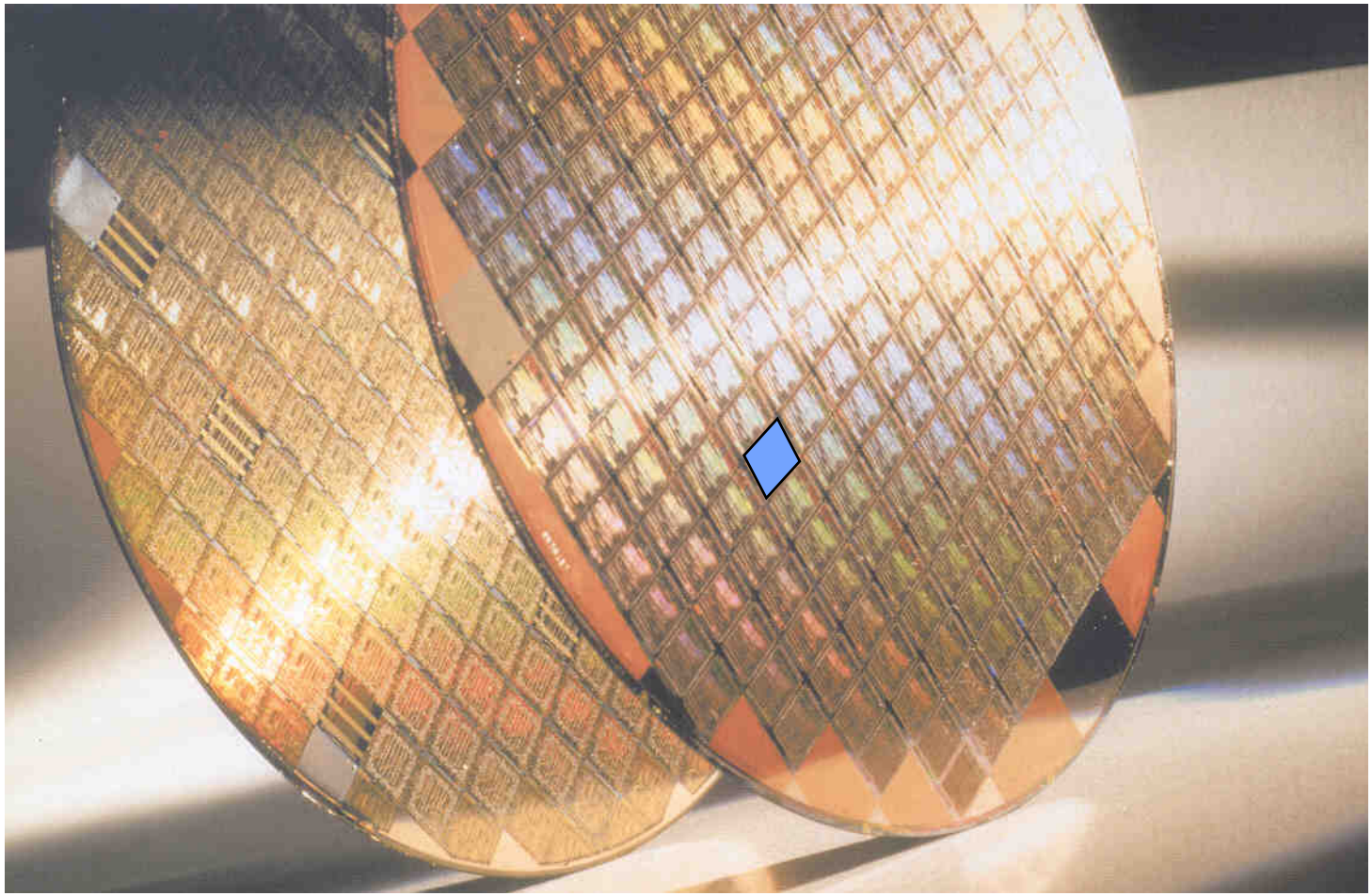
Core-Based SOC

Pacemaker – Alcatel 2μ A/D CMOS technology



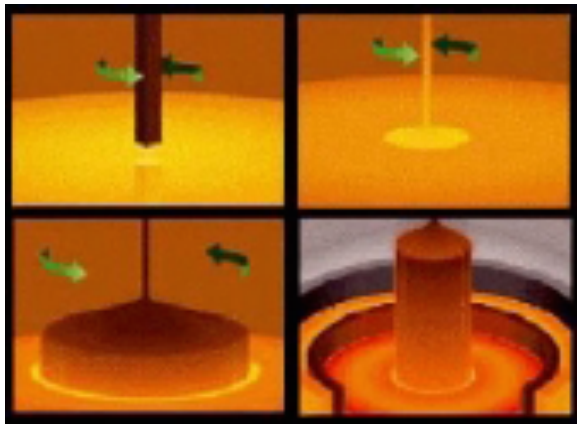
ICROELECTRÓNICA

From the *Wafer* to the *Die*

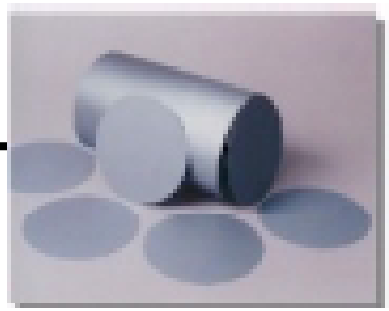


Silicon Wafer Processing

Crystal Growth and Wafer Slicing Process



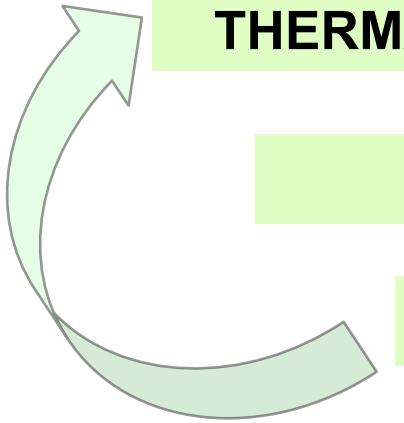
- The sand used to grow the wafers has to be a very clean
- The sand is heated to about 1600 degrees C – just above its melting point
- A pure silicon *seed* crystal is placed into the molten sand bath
- The seed is pulled out slowly as it is rotated
- The result is a pure silicon cylinder: an ingot
- The ingot is sliced into very thin wafers
- Wafers are polished until they are very smooth and just the right thickness



ICROELECTRÓNICA

Silicon Wafer Processing

CRYSTAL GROWTH



THERMAL OXIDATION, IMPLANT, DEPOSITION

PHOTOLITHOGRAPHY

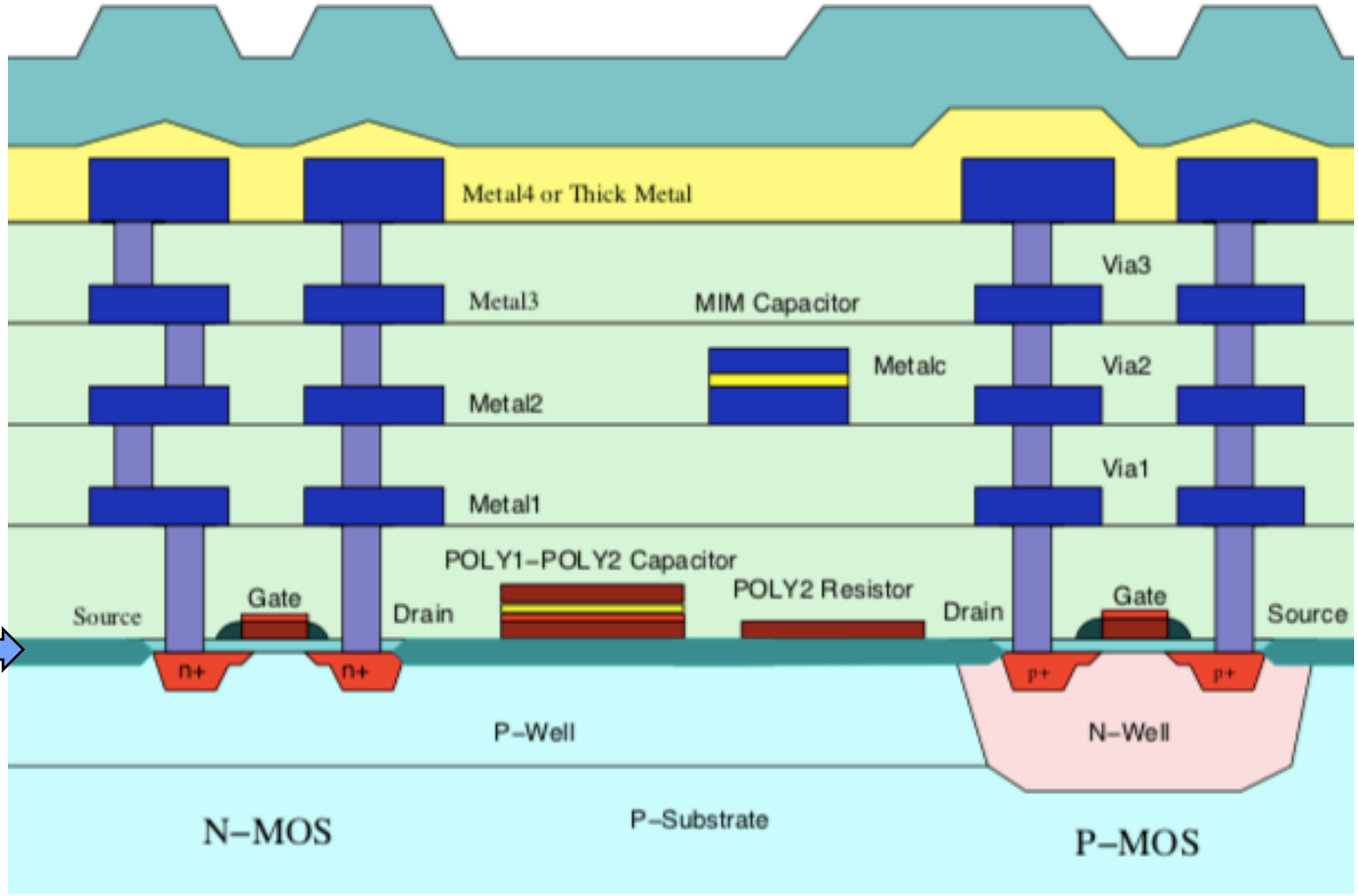
CORROSÃO (ETCHING)

PAKAGING AND TEST

ICROELECTRÓNICA

Silicon Wafer Processing

THERMAL OXIDATION



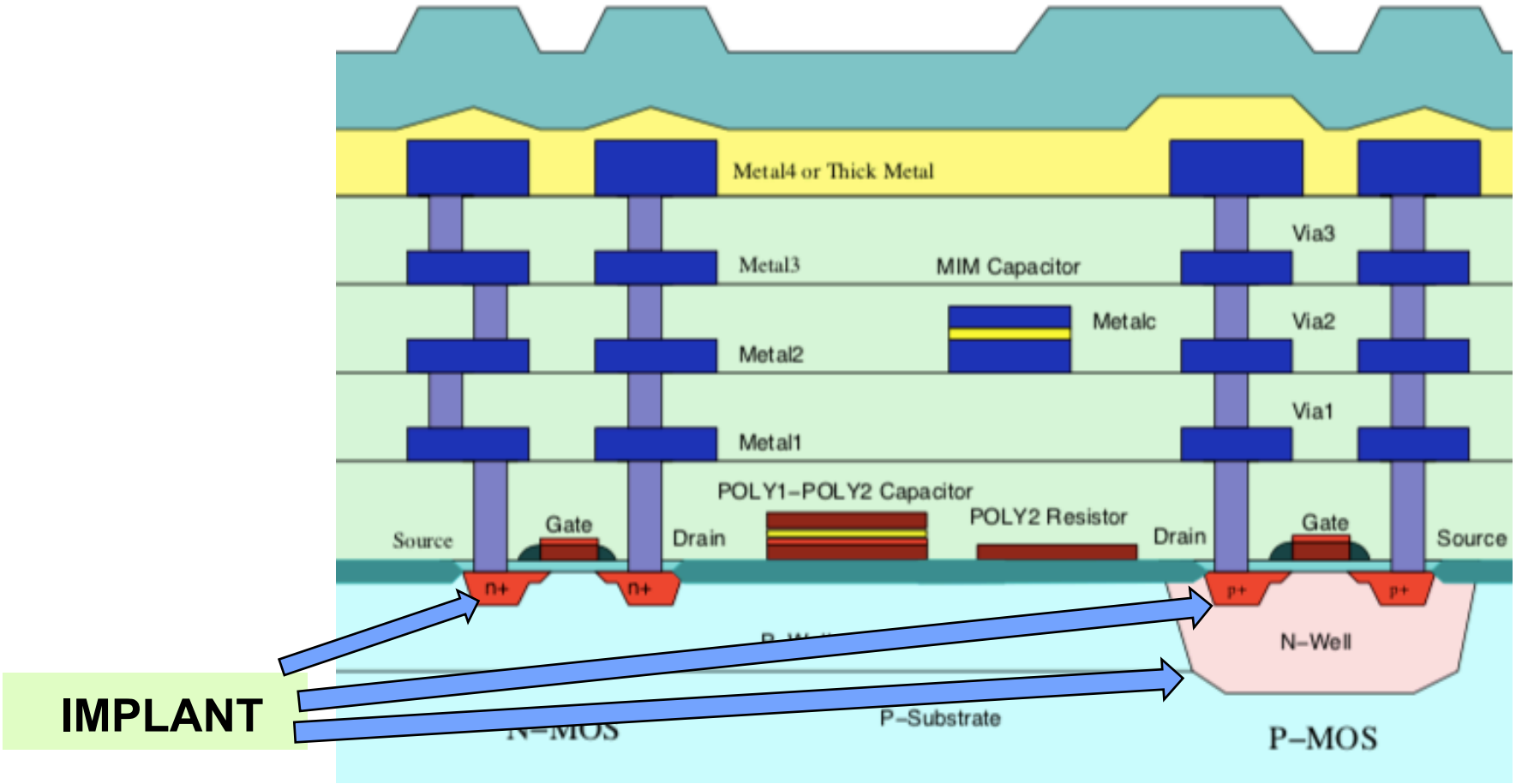
MICROELECTRÓNICA

Silicon Wafer Processing

THERMAL OXIDATION

- SiO_2 (silicon dioxide) is formed in the silicon material by exposing it to oxygen at temperatures of 900 degrees C or higher
- SiO_2 protects the *wafer* and acts as an isolator
- The growing of *x* µm of SiO_2 requires 0,47*x* µm of silicon

Silicon Wafer Processing



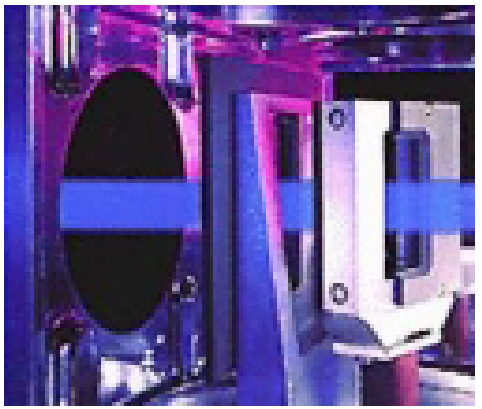
Silicon Wafer Processing

IMPLANT

Diffusion - Diffusion is done in a furnace with a flow of gas running over the wafers (very similar to oxidation except using a different gas other than oxygen)

- **Ion Implant -** shoots the desired dopant ions into the wafer (uses an electric field) - can only process a single wafer at a time

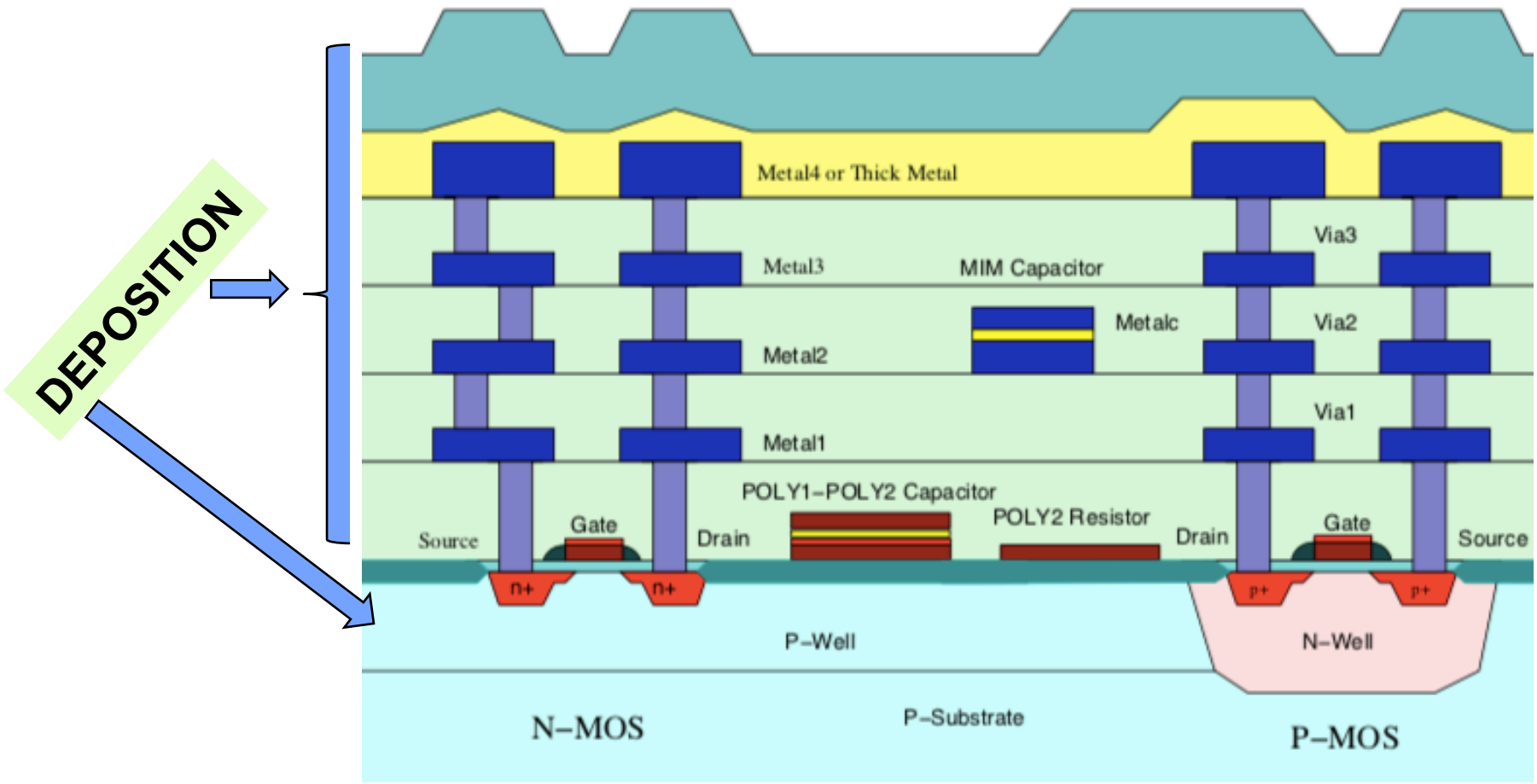
Typical dopants include:
- Boron +
- Phosphorous -



Magnets controlling the ion beam

These processes can be damaging to the wafer, so a heating process known as annealing is used to reduce any damage to the wafers.

Silicon Wafer Processing

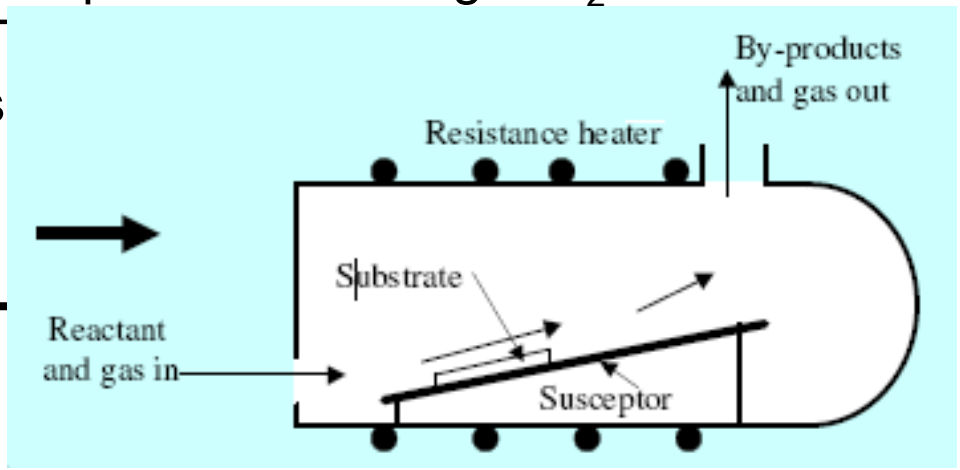


Silicon Wafer Processing

DEPOSITION - Chemical Vapor Deposition

Chemical Vapor Deposition *(CVD)* – A selected reactant material is diffused in a carrier gas that flows over the hot substrate surface. The heat from the hot substrate surface prompt chemical reactions between the reactant and the carrier gas to form the desired thin film on the substrate surface.

Thin films made of silicon compounds including SiO_2 and metals such as Al, Ag, Au, T
deposited on substrates us



Silicon Wafer Processing

DEPOSITION - Physical Vapor Deposition

Physical Vapor Deposition *(PVD)* - a thin film of material is deposited on a substrate:

1) the material to be deposited is converted into vapour by physical means
2) the vapour is transported across a region of low pressure from its source to the substrate
3) the vapour undergoes condensation on the substrate to form the thin film

Unlike CVD, which operates at elevated temperature, the PVD (physical vapor deposition) operates at room temperature.

Silicon Wafer Processing

DEPOSITION - Physical Vapor Deposition

Physical Vapor Deposition *(PVD)* **methods:**

- **PVD by Sputtering** - physical vapor deposition (PVD) technique wherein atoms or molecules are ejected from a target material by high-energy particle bombardment so that the ejected atoms or molecules can condense on a substrate as a thin film.

- **PVD by Evaporation** – evaporation/condensation by controlling the pressure and temperature

Silicon Wafer Processing

DEPOSITION - Epitaxy

- Epitaxy is quite similar to what happens in CVD processes
- In **V**apor **P**hase **E**pitaxy (VPE) a number of gases are introduced in an induction heated reactor where only the substrate is heated
- The temperature of the substrate typically must be at least 50% of the melting point of the material to be deposited
- If the substrate is an ordered semiconductor crystal, it is possible with this process to continue building on the substrate with the same crystallographic orientation with the substrate
- If an amorphous/polycrystalline substrate surface is used, the film will also be amorphous or polycrystalline
- An advantage of epitaxy is the high growth rate of material (>100μm)

Silicon Wafer Processing

Photolithography

• When the design is ready glass photomasks are made - one mask for each layer of the circuit.

•These glass photomasks are used in a process called photolithography.

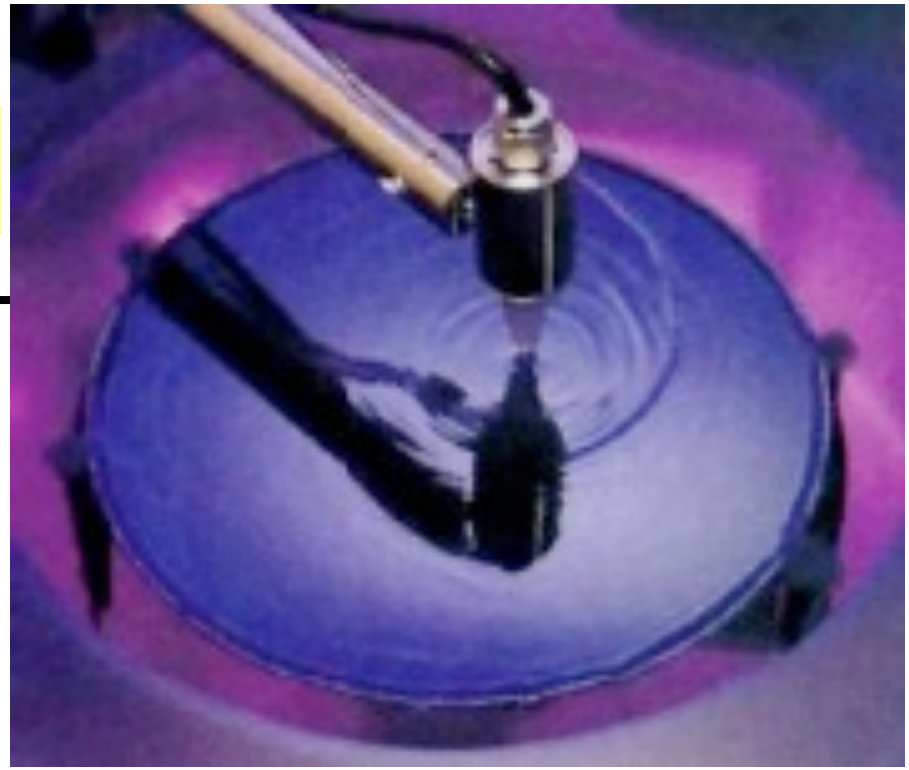
• The wafers are exposed to a multiple-step photolithography process that is repeated once for each mask

Silicon Wafer Processing

Photolithography

- Coating of photoresist
- Exposure to UV
- Development

Silicon Wafer Processing



Photolithography – Coating of photoresist

- The wafer is uniformly coated with a thick light-sensitive liquid called photoresist. The coating is applied while the wafer is spinning (1500-8000 rpm)
- The photoresist thickness is in the range: 0.5 - 2μm. Thickness uniformity of ~5nm is required.
- The wafer is heated in order to cure the photoresist (*soft baking*).

Silicon Wafer Processing

Photolithography - Coating of photoresist

After spin coating, resist contains up to 15% organic solvent. This is removed by soft-baking at 75-100ºC for approximately 10 mins. This step also

- Releases stress
- Improves adhesion of resist to wafer

Silicon Wafer Processing

Photolithography - Exposure to UV

- Parts of the wafer are selected for exposure by carefully aligning a mask between an ultraviolet light source and the wafer.

- In the transparent areas of the mask, light passes through and exposes the photoresist.

Silicon Wafer Processing

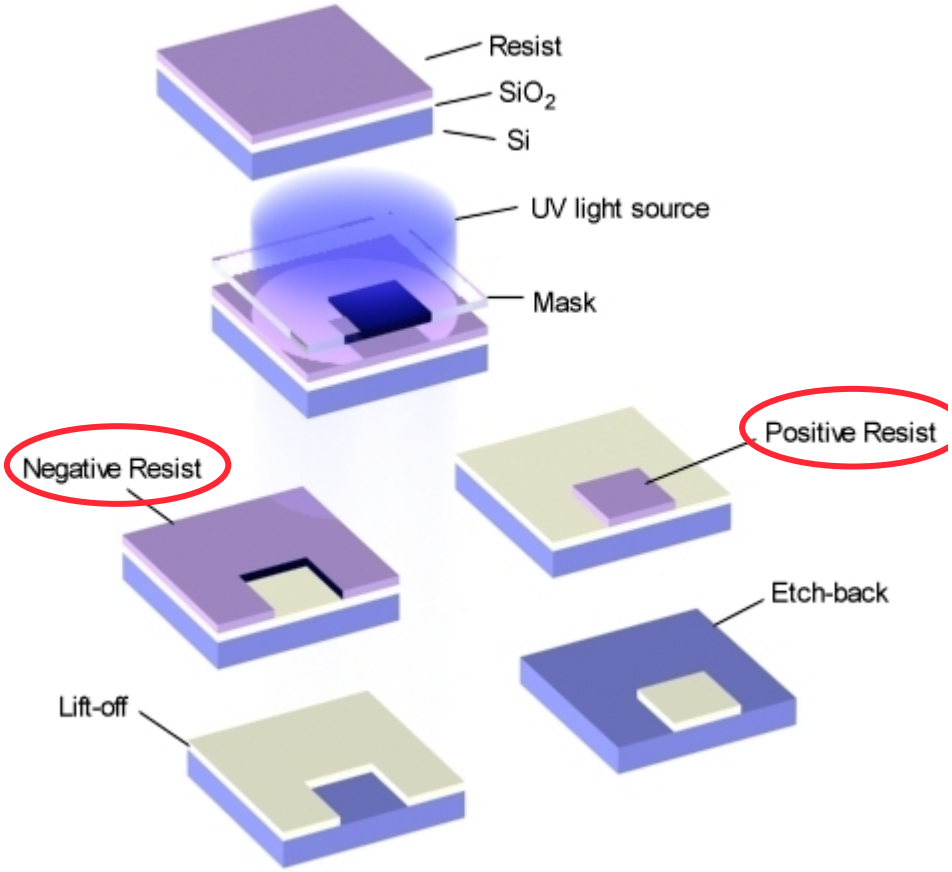
Photolithography - Exposure to UV

There are two types of photoresist:

- **negative** - UV light causes the negative resist to become polymerized, and more difficult to dissolve

- **positive** - UV light changes the chemical structure of the resist so that it becomes more soluble in the developer

Positive resists are now the dominant type in use



ICROELECTRÓNICA

Silicon Wafer Processing

Photolithography - Exposure to UV

•A *mask* is a square glass plate with a patterned emulsion of metal film on one side

•The mask is aligned with the wafer, so that the pattern can be transferred onto the wafer surface

•Each mask must be aligned to the previous one

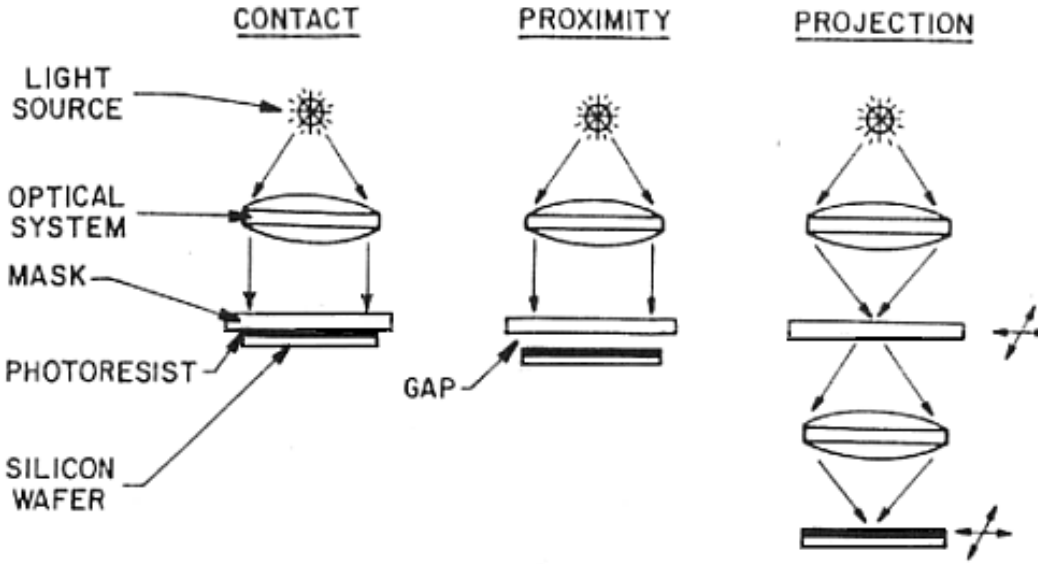
•The photoresist is exposed through the pattern on the mask with a high intensity ultraviolet light

Silicon Wafer Processing

Photolithography - Exposure to UV

•There are three primary exposure methods: *contact*, *proximity*, and *projection.*

•The main advantage of *projection* is that the mask can be quite a bit larger then the final pattern and through optical and mechanical manipulations a better resolution can be exposed onto the photoresist - *Direct Wafer Stepping (DWS)*



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Silicon Wafer Processing

Photolithography - Exposure to UV

Factors affecting resolution:

• Diffraction of light at the edge of an opaque feature in the mask as the light passes through alignment of wafer to mask,

• non-uniformities in wafer flatness,

Theoretical limits of photo lithography: ***smallest feature size by projection lithography is the same as the λ of the UV source.***

Means of Exposure:

Extreme UV (EUV) 10-14nm

Deep UV (DUV) 150-300nm

Near UV (UV) 350-500nm

For λ =400 nm, resolution is approximately 1 μm

ICROELECTRÓNICA

Silicon Wafer Processing

Photolithography - Exposure to UV

New generation lithography techniques:

- **Extreme ultraviolet lithography**

- **X-ray lithography (**shorter λ and immunity to particle contamination, but only 1:1 scale and complex mask production)

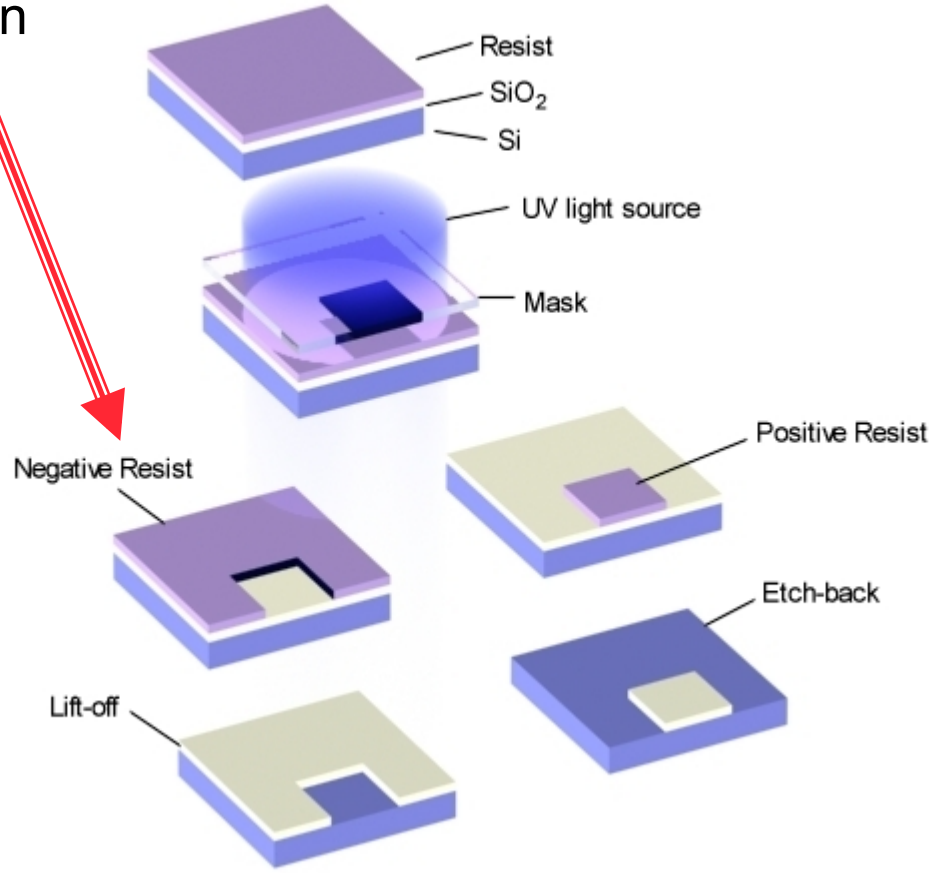
- ***Direct Write to Wafer methods*** (DWW): Electron beam or Ion-beam lithography – more expensive

Silicon Wafer Processing

Photolithography - Development

Negative photoresist hardens and becomes impervious to etchants when exposed to ultraviolet light.

This chemical change allows the subsequent developer solution to remove the unexposed photoresist while
leaving the hardened, exposed photoresist on the wafer.



Silicon Wafer Processing

Etching

The etching process is used immediately after photolithography to etch the unwanted material from the wafer.

- Wet etching - A batch of wafers is dipped into a higly concentrated pool of acid

- Dry etching - uses gas instead of chemical etchants. Dry etching is capable of producing critical geometries that are very small.

Acid being poured onto a wafer

Silicon Wafer Processing

Process Steps Outline

• **Diffusion** - A layer of material such as oxide is grown or deposited onto the wafer.
• **Coat / Bake** - The resist, a light sensitive protective layer, is applied and cured in place (*soft baking*).
• **Align** - A reticule is positioned over the wafer. Ultraviolet light shines through the clear portions of the reticule exposing the pattern onto the photosensitive resist.
• **Develop** - The resist is developed and unwanted resist is washed away.
• **Dry Etch** - Dry etch removes oxide not protected by resist.
• **Wet Etch and Clean** - The remaining resist is removed in wet etch to reveal the patterned oxide layer (*stripping*).

Chapter I

CMOS Technology

- Mixed-signal design flow
- Processing steps
- **Processing sequence**
- Package and test

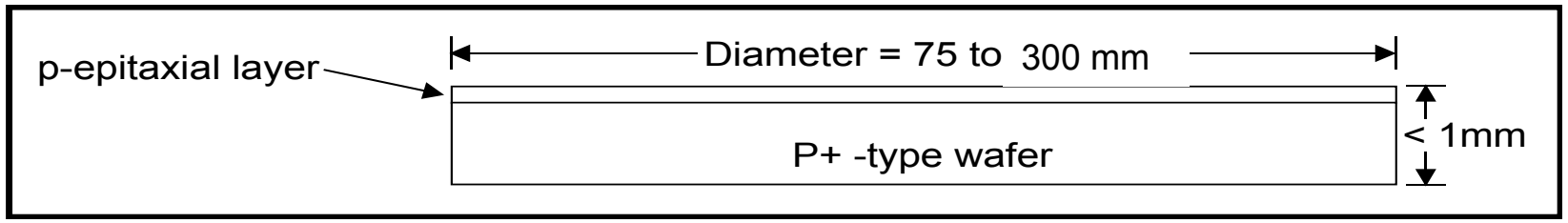
Silicon Wafer Processing – Details

1 –*wafer* preparation

•In a N well process the wafer must have P type impurities

•The *wafer* typical diameter is between 75 mm and 300 mm, with a thickness <1 mm (typically between 500 µm and 800 µm)

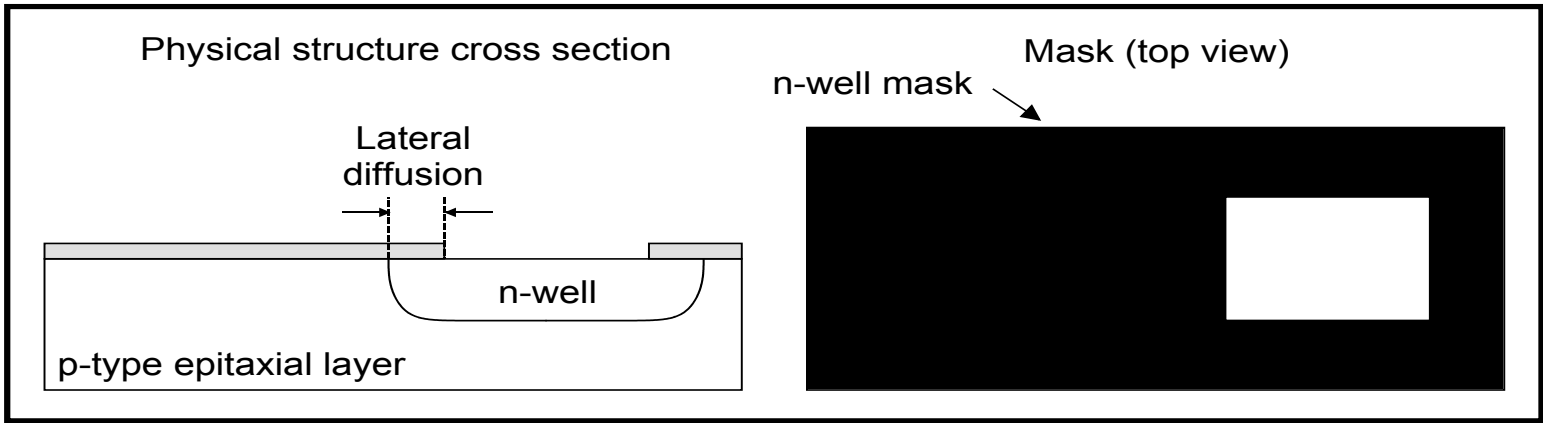
•Can be obtain building an epitaxial layer P- (about 2 µm, smaller concentration, more pure, smaller *latch-up risk*)



Silicon Wafer Processing – Details

2 – N Well

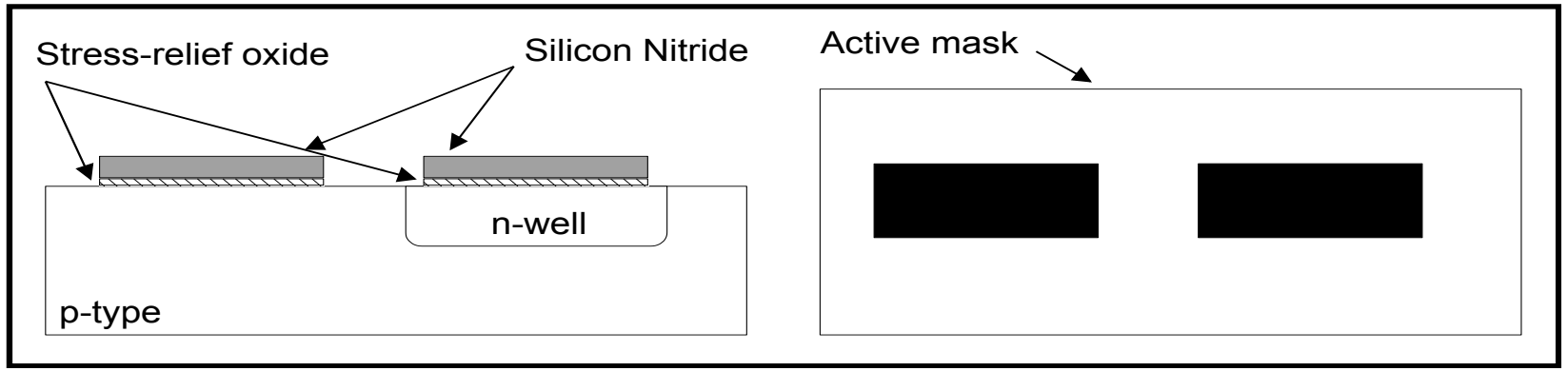
- The first mask used defines the N wells position
- The N wells can be obtained by diffusion or ion implant (better since it has smaller lateral diffusion)
- The N well is very deep: 30000 Å



Silicon Wafer Processing – Details

3 – Active area definition

- Areas for the implementation of transistors (gate, source and drain) and other diffusions (biasing the substrate and well, guard rings).
- This area will receive the thin oxide
- Is protected with SiO_2 (≈ 200 Å) and Si_3N_4 (≈ 2500 Å)

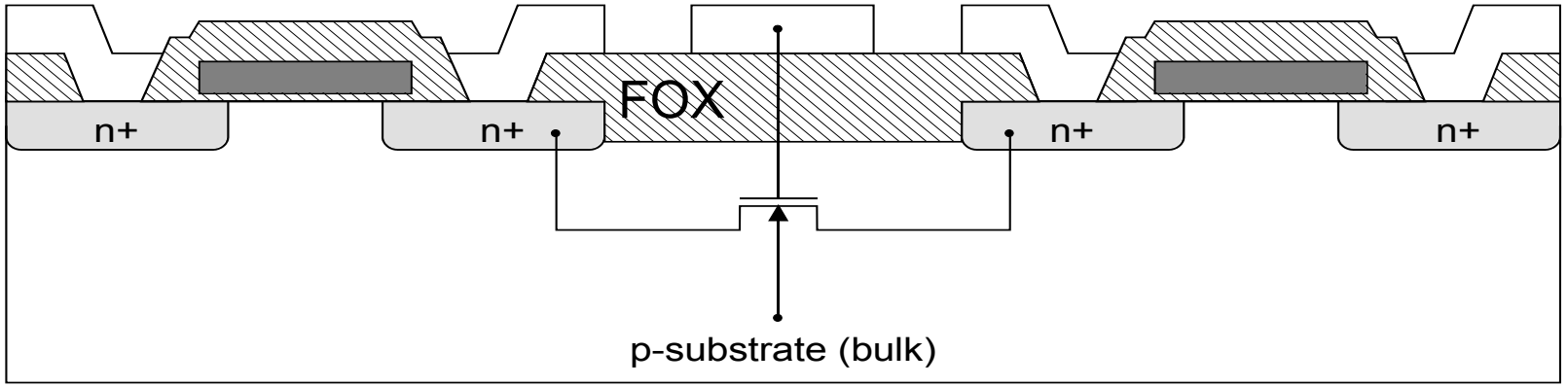


Silicon Wafer Processing – Details

4 – Devices isolation

- There are parasitic MOS transistors besides the ones designed:
  - The implemented diffusions form drains and sources
  - The gates are the metal and poly interconnections
  - It is mandatory to force the Vth of these parasitic MOS to be higher then the supply voltage:
    - Increasing the bulk concentration between diffusions of different transistors (*channel-stop*)
    - Increasing the thickness of the FOX.

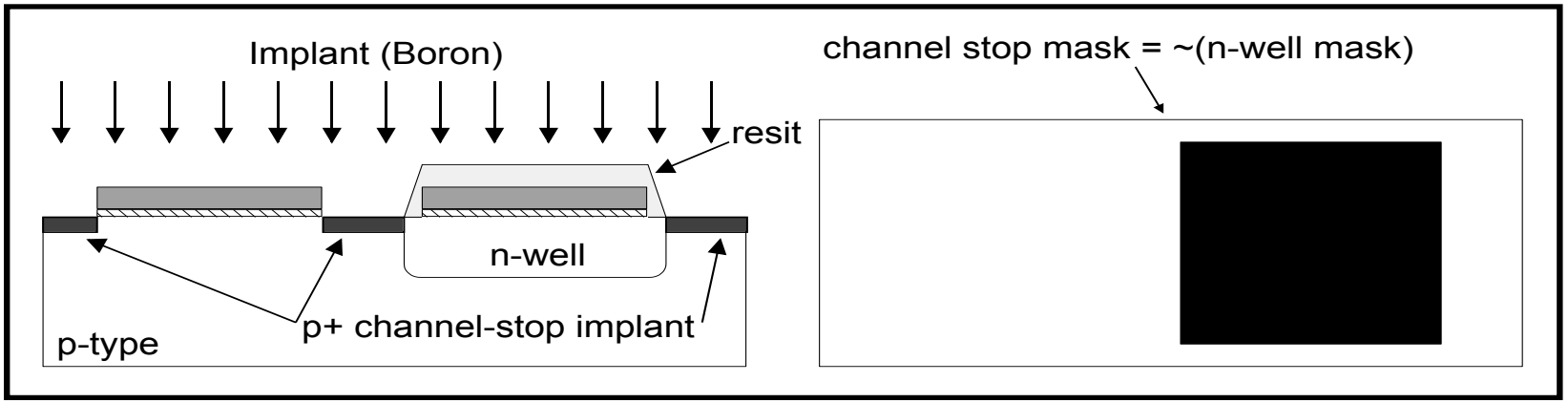
Parasitic FOX device



Silicon Wafer Processing – Details

4 – Devices isolation (*channel-stop*)

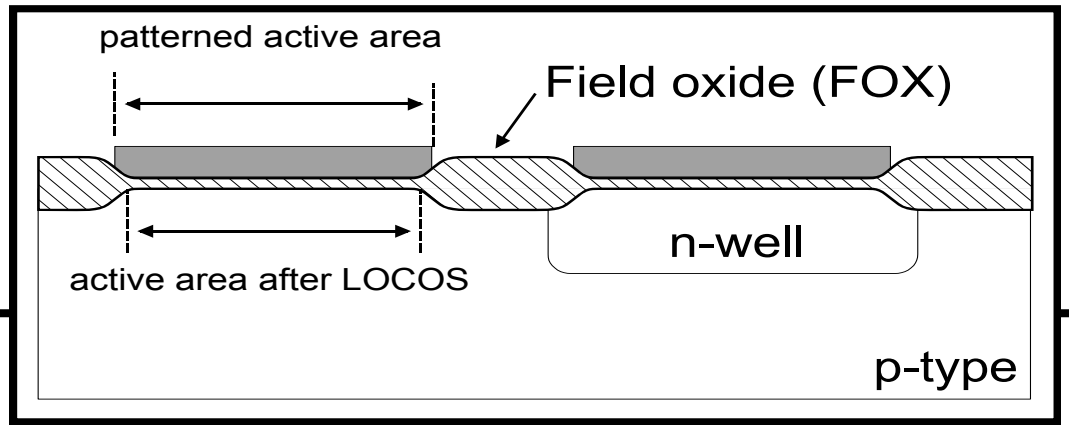
- The channel-stop is obtain by ion implant, customized using Si_3N_4 (in the P substrate) and *photoresist* (in the N well)



Silicon Wafer Processing – Details

4 – Devices isolation (*LOCOS*)

- Growing of the thick oxide - *Local oxidation of silicon (LOCOS):*
  - *photoresist* is removed
  - Si_3N_4 and SiO_2 are the masks
  - SiO_2 grows: 1000 ºC + H_2O ou 1200 ºC + O
  - The oxide grows in all directions reducing the original masked active area



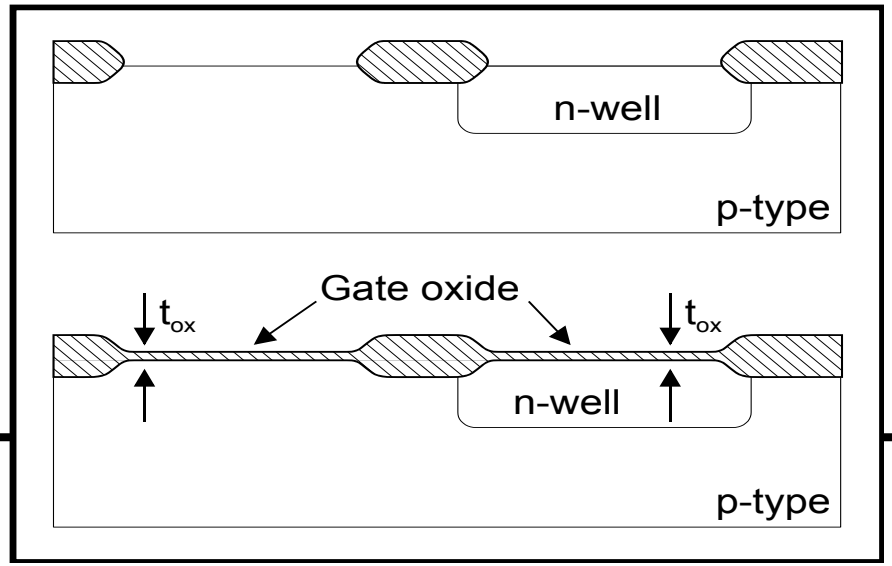
Silicon Wafer Processing – Details

5 – Thin oxide

- The active area masks (Si_3N_4 over SiO_2) are removed
- The concentration at the surface is adjusted in order to obtain the desired V_{th}
- The thin oxide grows with a thickness that varies from t_{ox} = 20 Å to 100 Å

4 atoms

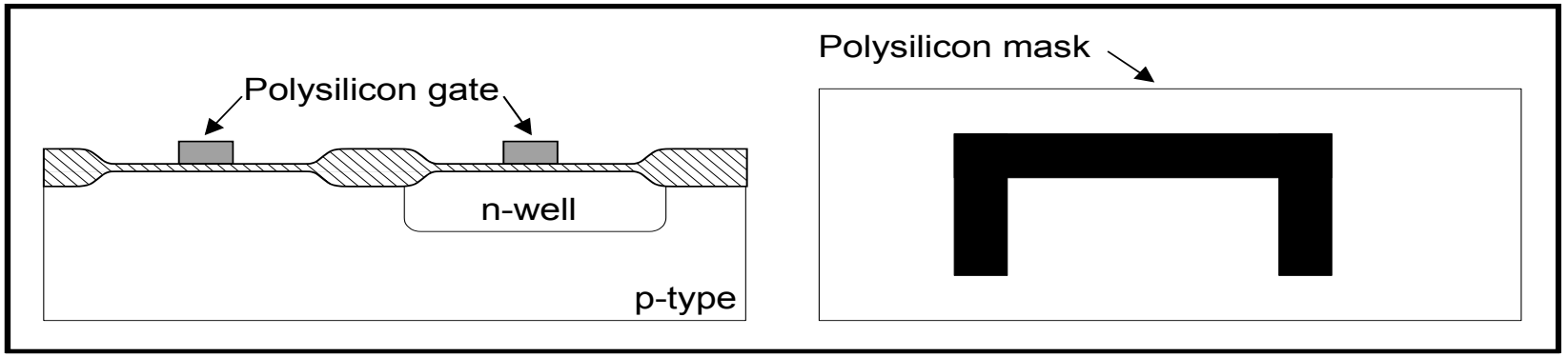
Is one of the most critical steps in the process !



Silicon Wafer Processing – Details

6 – POLY

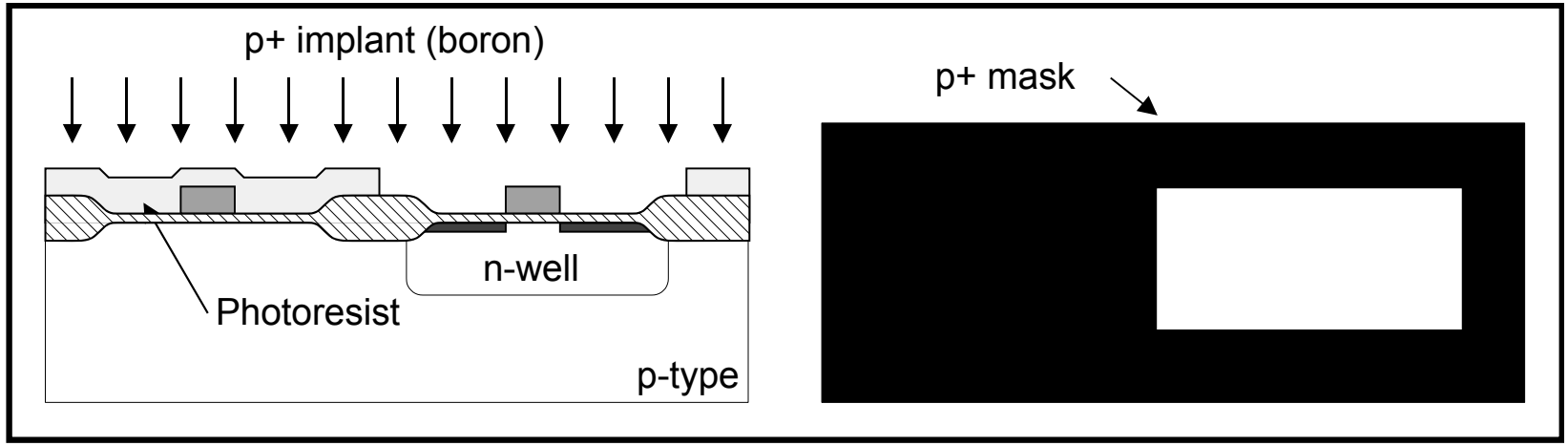
- The wafer is covered with a layer of polysilicon (*poly thickness*: 1500-3000 Å)
- Polysilicon is lithographically customised (in the most critical lithographical step of the process)
- The polysilicon is usually doped (N+) while deposited in order to reduce its resistivity



Silicon Wafer Processing – Details

7 – P type diffusion

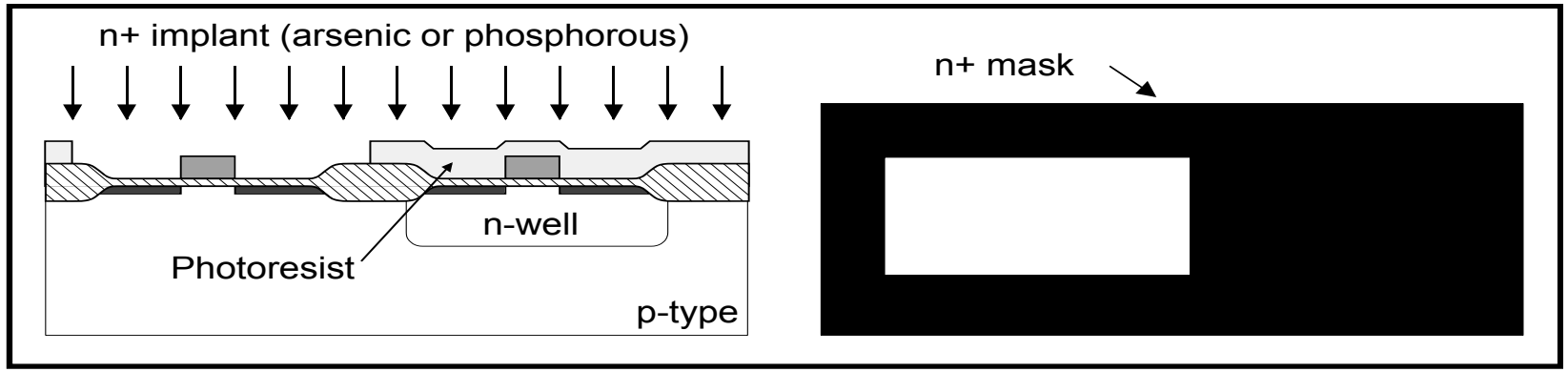
- Lithographic selection of the target areas
- Ion implant is carried out with a beam of boron ions
- The transistors are formed using *poly* as a mask that creates a gap between the implant of the drain and source areas:
  - *Called self-aligned process*
  - The *poly* of the P type transistors gets P type impurities over the N type received during deposition. The final type depends on the dominant doping.



Silicon Wafer Processing – Details

8 – N type diffusion

- Lithographic selection of the target areas
- Ion implant is carried out with a beam of phosphorous ions
- The transistors are formed using *poly* as a mask that creates a gap between the implant of the drain and source areas:
  - *Called self-aligned process*
  - The *poly* of the N type transistors gets more N type impurities.

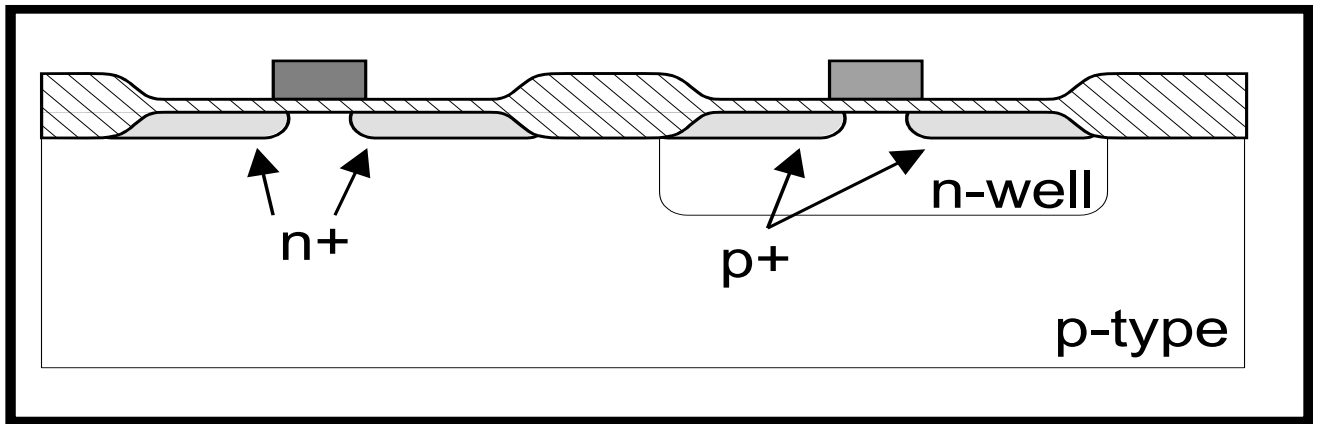


Silicon Wafer Processing – Details

9 – Annealing

- After ion implant a cycle of *thermal annealing* is required
  - The crystalline structure is reorganized (after the damages caused by ion implant) and additional diffusion of implanted impurities takes place

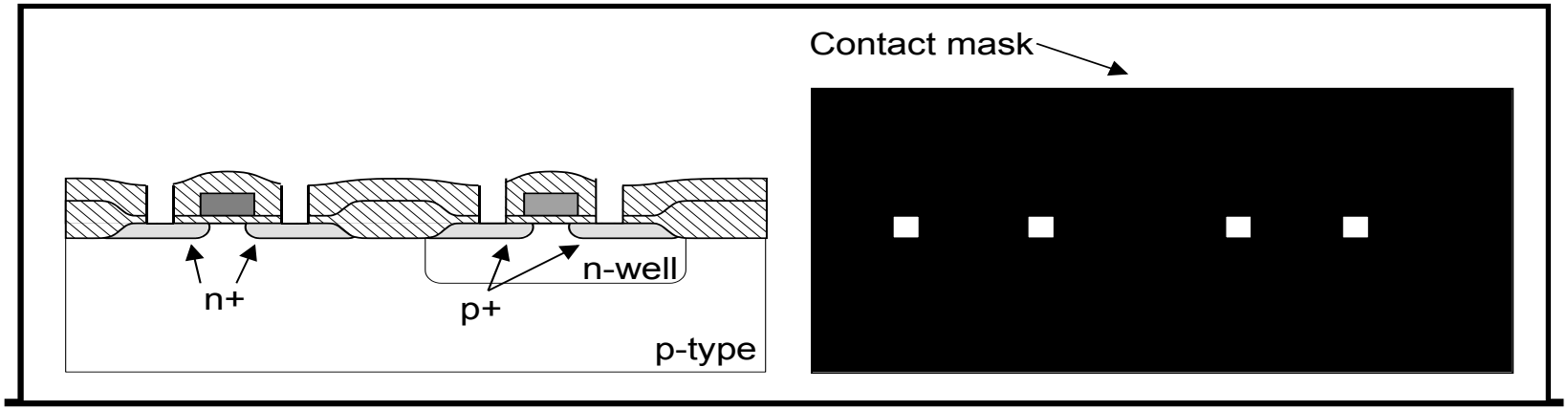
- After this step the temperature must stay low in order to preserve the distribution of impurities



Silicon Wafer Processing – Details

10 – Contacts

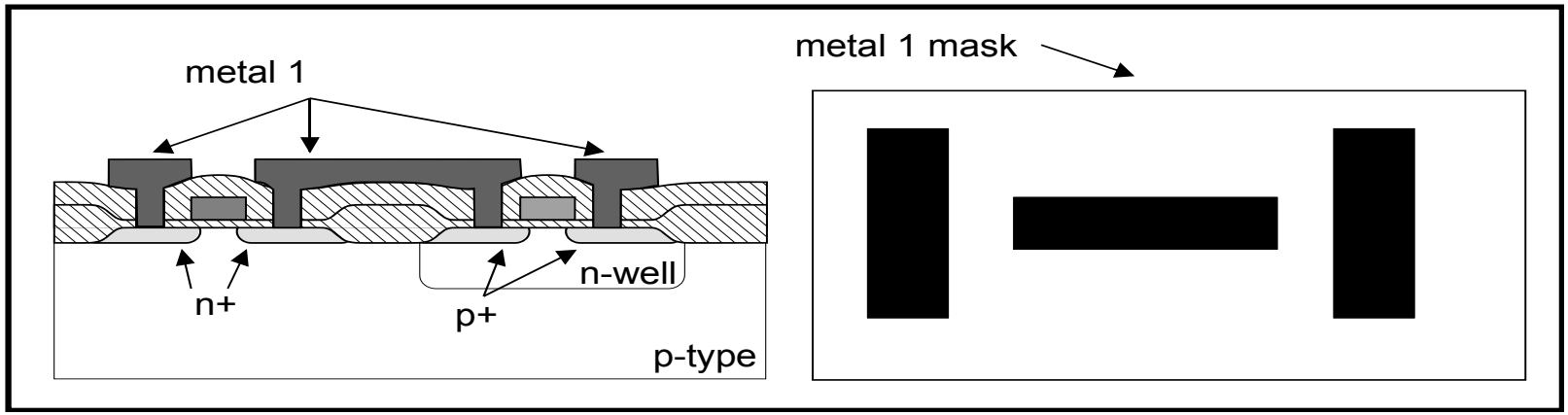
- The wafer surface is covered with SiO_2 using CVD (≈ 1µm, at low temperature)
- A lithographical process is used to open slots in the previously deposited SiO_2 allowing access to the lower level electrical nodes (*poly* or diffusion)



Silicon Wafer Processing – Details

11 – Metal 1

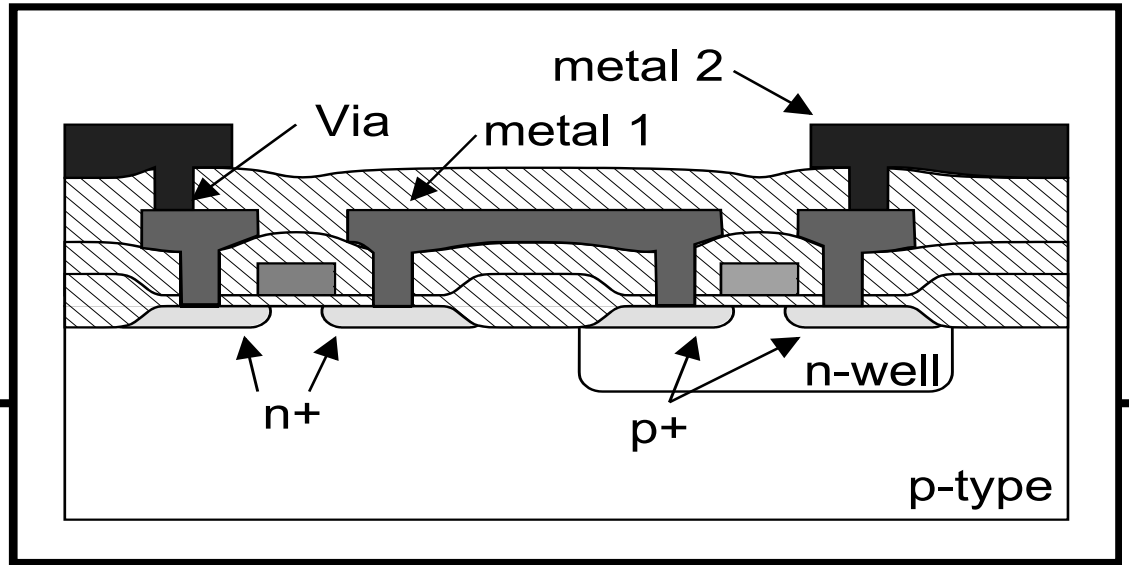
- The wafer surface is covered with metal (≈ 5000 Å)
- A lithographical process is used to selectively remove the metal



Silicon Wafer Processing – Details

12 – Metal 2

- The wafer surface is covered again with SiO_2 using CVD (at low temperature, thickness ≈ 1μm)
- A lithographical process is used to open slots in the SiO_2 in order to allow access to the metal 1 nodes (vias)
- The wafer surface is covered with metal (2)
- A lithographical process is used to selectively remove the metal



Silicon Wafer Processing – Details

13 – Passivation

- The top protection of the circuit consists of:
  - SiO_2 and
  - Si_3N_4
- A lithographical process is used to open large slots in the passivation in order to allow access to the top metal nodes (pads)

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CMOS Technology

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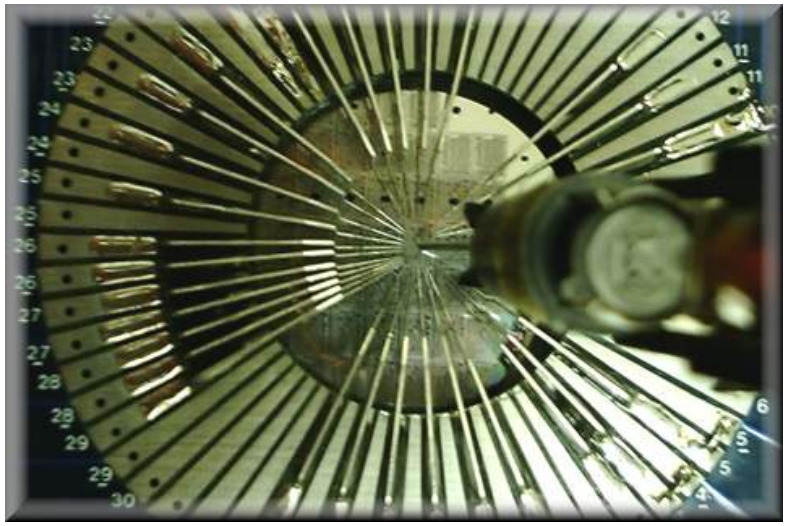
Silicon Wafer Processing

PAKAGING AND TEST



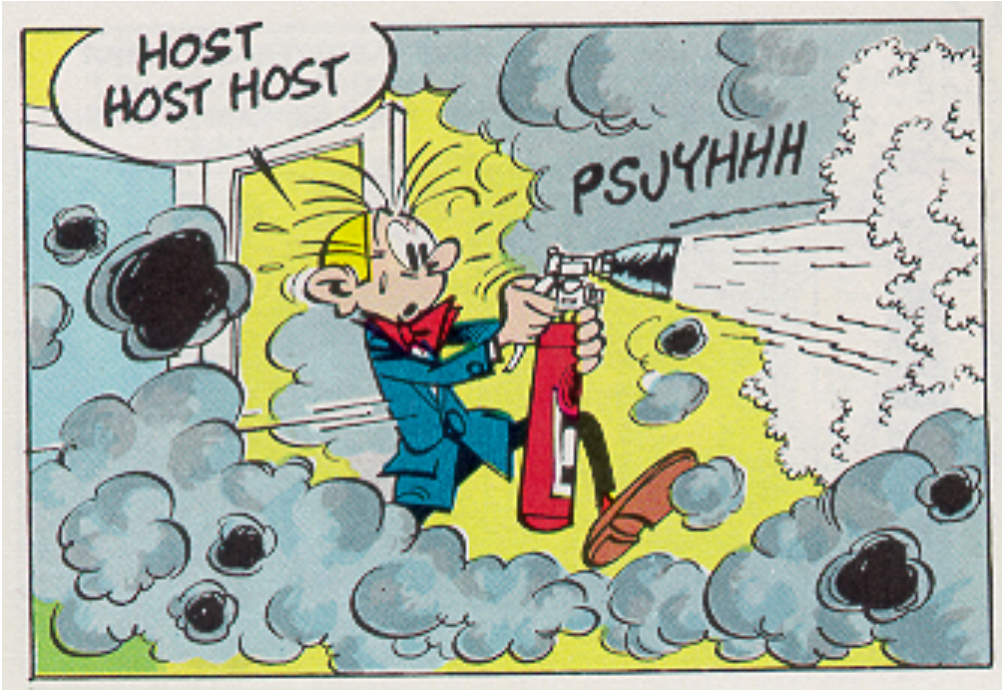
- Parametrical test using test structures regularly distributed in the *wafer*
- Wafer *die* test marking defective dies
- *dies* separation
- *die* fixing (not marked as defective) and connection to package by:
  - *Wire bonding* **or**
  - *Flip-chip*
- Final test

Silicon Wafer Processing

PAKAGING AND TEST

Packaging purposes:

- Heat transfer from the die to the exterior
- Protect the die from the exterior environment
- Allow interface for production test
- Implement an interface with PCB
  - Mechanical
  - Electrical



Goals:

- Minimum dimensions
- Lowest price possible

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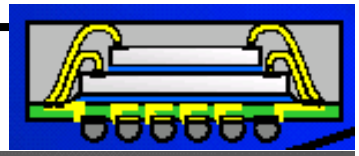
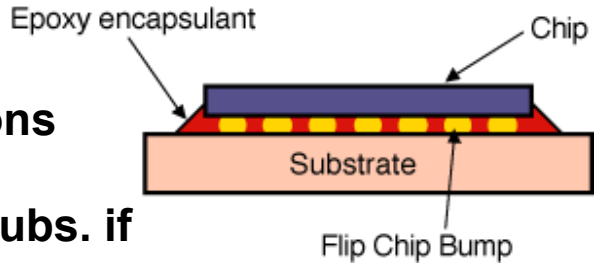
Silicon Wafer Processing

PAKAGING AND TEST

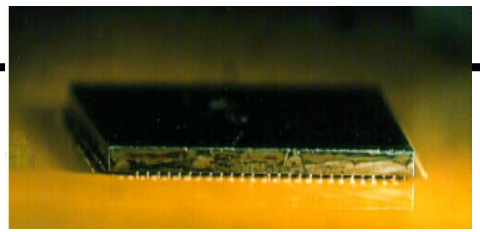


Connection between die and packaging:

- *Wire bonding*
  - Only the *die* boundary is available for connectio
  - Sequencial pin connection
  - Heat transfer through the substrate
  - *L ≈ 1 nH*



- *Flip-chip*
  - All the die area is available for interconnections
  - All pins are connected simultaneously
  - Heat transfer through the connections (and subs. if required)
  - Even thermal physical properties required
  - *L ≈ 0,1 nH*



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Silicon Wafer Processing

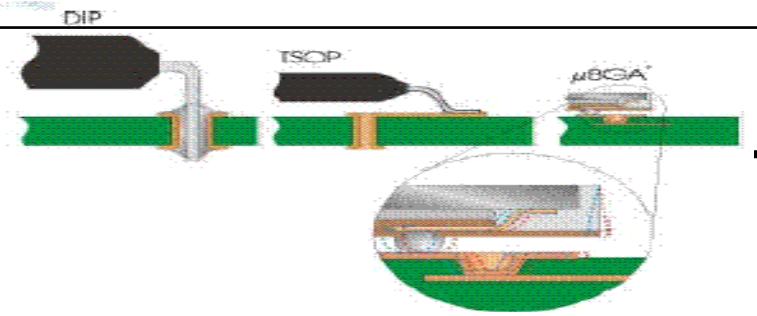
PAKAGING AND TEST

Types of packaging:

- Ceramic
  - **Good thermal properties**
  - **Expensive**
- Plastic
  - **Bad thermal properties (can be improved with metallic heat dissipation)**
  - **Cheap**

Interface with PCB:

- ***Pin through hole***
  - **Easy manual assembly**
  - **Each pin is available in all PCB levels**
  - **Limited density**
- ***Surface Mount Devices (SMD)***
  - **Requires dedicated equipment for PCB assembly**
  - **Only the surface of the PCB is available (it doesn't interfere with bottom PCB levels)**
  - **Higher density**



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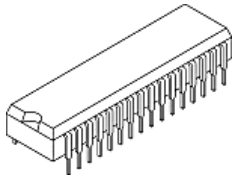
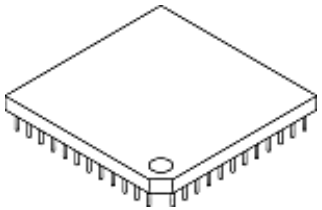
PAKAGING AND TEST

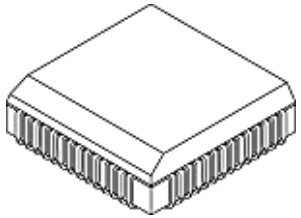
Traditional packaging:

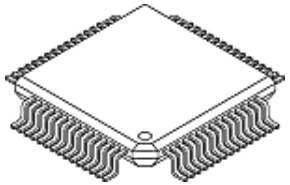
Inductances: 1 - 20 nH

- ***DIL (Dual In Line)***
  - **Small number of pins**
  - **Large space**
- ***PGA (Pin Grid Array)***
  - **until 400 pins**
  - **frequently used in old CPUs**
- ***PLCC (Plastic Leaded Chip Carrier)***
  - **until 84 pins**
  - **Requires large space**
  - **SMD**
- ***QFP (Quarter Flat pack)***
  - **until 300 pins**
  - **Requires large space**
  - **SMD**









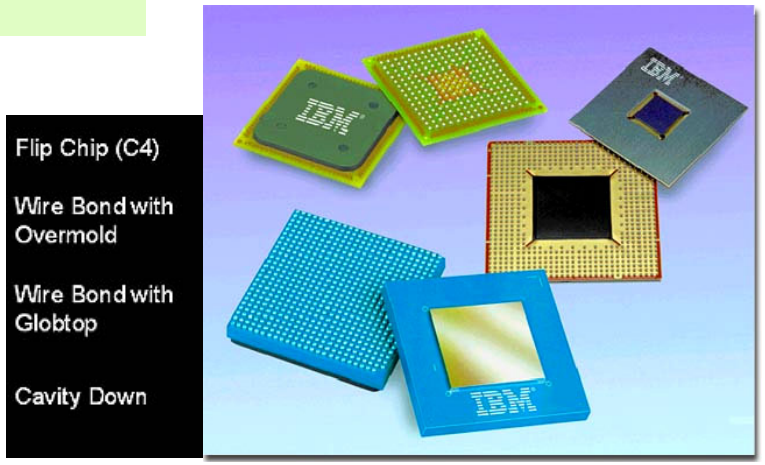
Silicon Wafer Processing

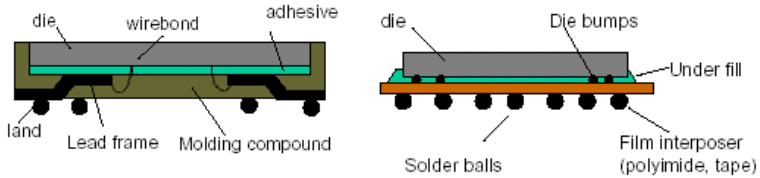
PAKAGING AND TEST

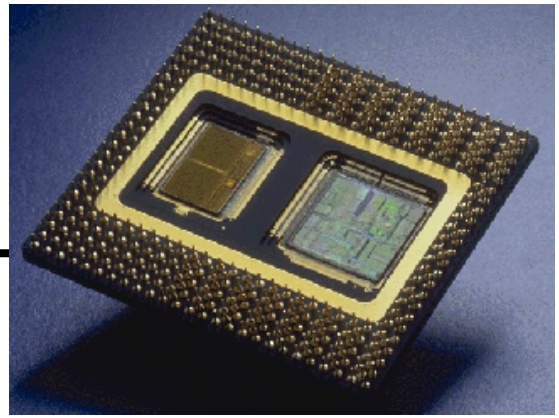
More recent packages:

Inductances: 1 - 5 nH

- *BGA (Ball Grid Array)*
  - Small balls for PCB connection
  - Large number of pins
  - Small space required
  - Lower inductance
- *CSP (Chip scale Packaging)*
  - Like BGA but smaller
- *MCP (Multi Chip Package)*
  - Allows different technologies in the same device
  - Increases yield since each chip is tested before packaging







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