DF
DEPARTAMENTO
DE FÍSICA
TÉCNICO LISBOA

Nanotechnologies and Nanoelectronics

2021-semestre 1-P2

Homework #2

The work should be sent to: susana.freitas@tecnico.ulisboa.pt

10 January 2022

Deadline: ~~31 December 2021~~ @ 23:59[1].

Please send the work in one single file[2] (e.g., pdf, jpeg, word) identified as: **NN2021_YourName_HW2**

[1] The documents received up to 5 days after the deadline will have a penalty of 1 point (out of 20) per day. No documents will be accepted after the 6th day.

[2] In case you need to have pictures of hand-written work, or multiple format digital formats for your solutions, please merge them into one single document.

Nanotechnologies and Nanoelectronics
2021-S1-P2

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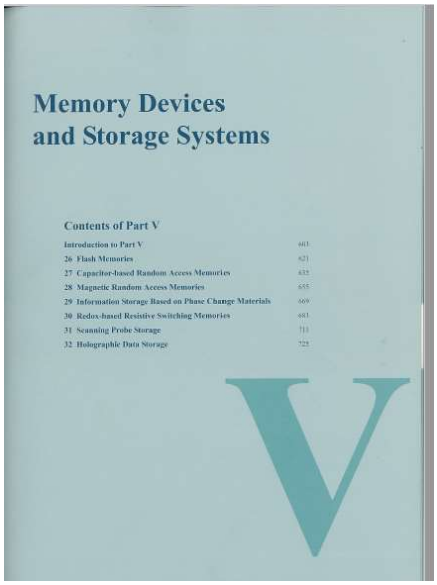
Support bibliography:

Book "Nanoelectronics and Information Technology"

Chapters 26, 27, 28 and 29

from SECTION V- Memory devices and Storage Systems (3rd edition 2012)



For each memory architecture

1) Flash memories [chapter 26]

2) Capacitive memories DRAM [chapter 27]

3) Magnetic memories MRAM [chapter 28]

4) Phase change memories PCM [chapter 29]

Write a summary table (maximum 2 pages each) with the key information:

Memory type: _____	
Design of a typical architecture of the storage element	[insert figure here, including dimensions and materials]
Physical operation principle and basic equations	
Physical limits of scaling (i.e, what are the limitations to reduce the size towards a ultrahigh density memory)	
Indicate how the retention time can be calculated, and what are the key physical parameters that affect the retention of a bit state	
Reliability issues (i.e, what are the causes of failure during operation (read/write) and data storage)	
Example of manufacture companies for such a memory device	