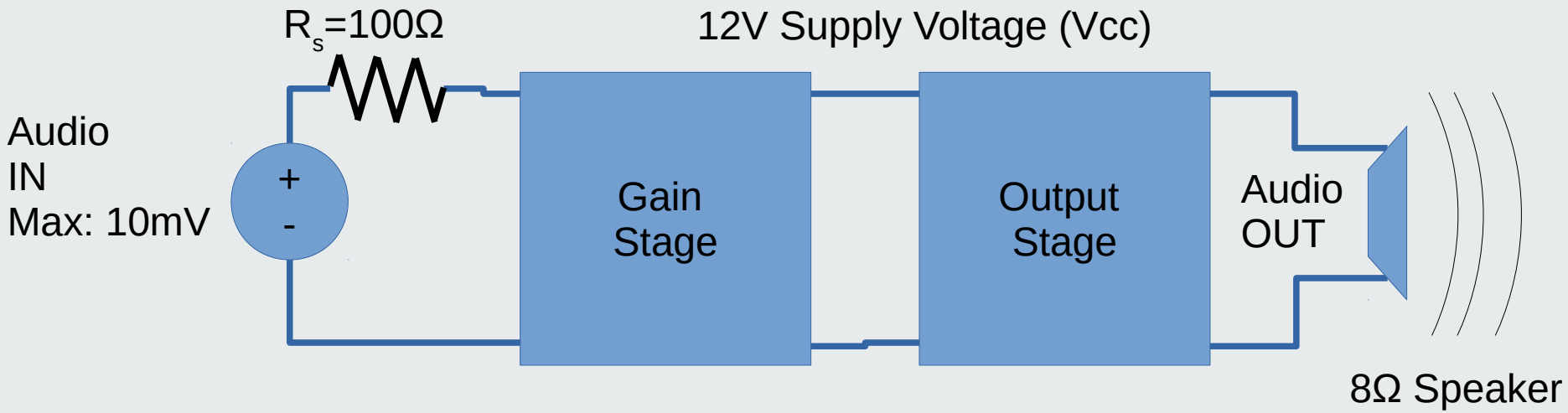
TÉCNICO LISBOA

Circuit Theory and Electronics Fundamentals

Lecture 17: Presenting the Audio Amplifier Lab Assignment

- Audio amplifier lab assignment presentation
- Bias circuit
- Coupling capacitors
- Bypass capacitor
- Incremental circuit and gain
- Output stage
- Incremental circuit, input and output impedances

Audio Amplifier Circuit



Based on Lectures 16 and 17, choose the architecture of the Gain and Output amplifier stages. Provided the output has no visible distortion in the output sine waves, the merit M of your work is given by

$$M = \frac{voltageGain * bandwidth}{cost * lowerCutoffFreq}$$

cost = cost of resistors + cost of capacitors + cost of transistors
cost of resistors = 1 monetary unit (MU) per kOhm
cost of capacitors = 1 MU/μF
cost of transistors = 0.1 MU per transistor

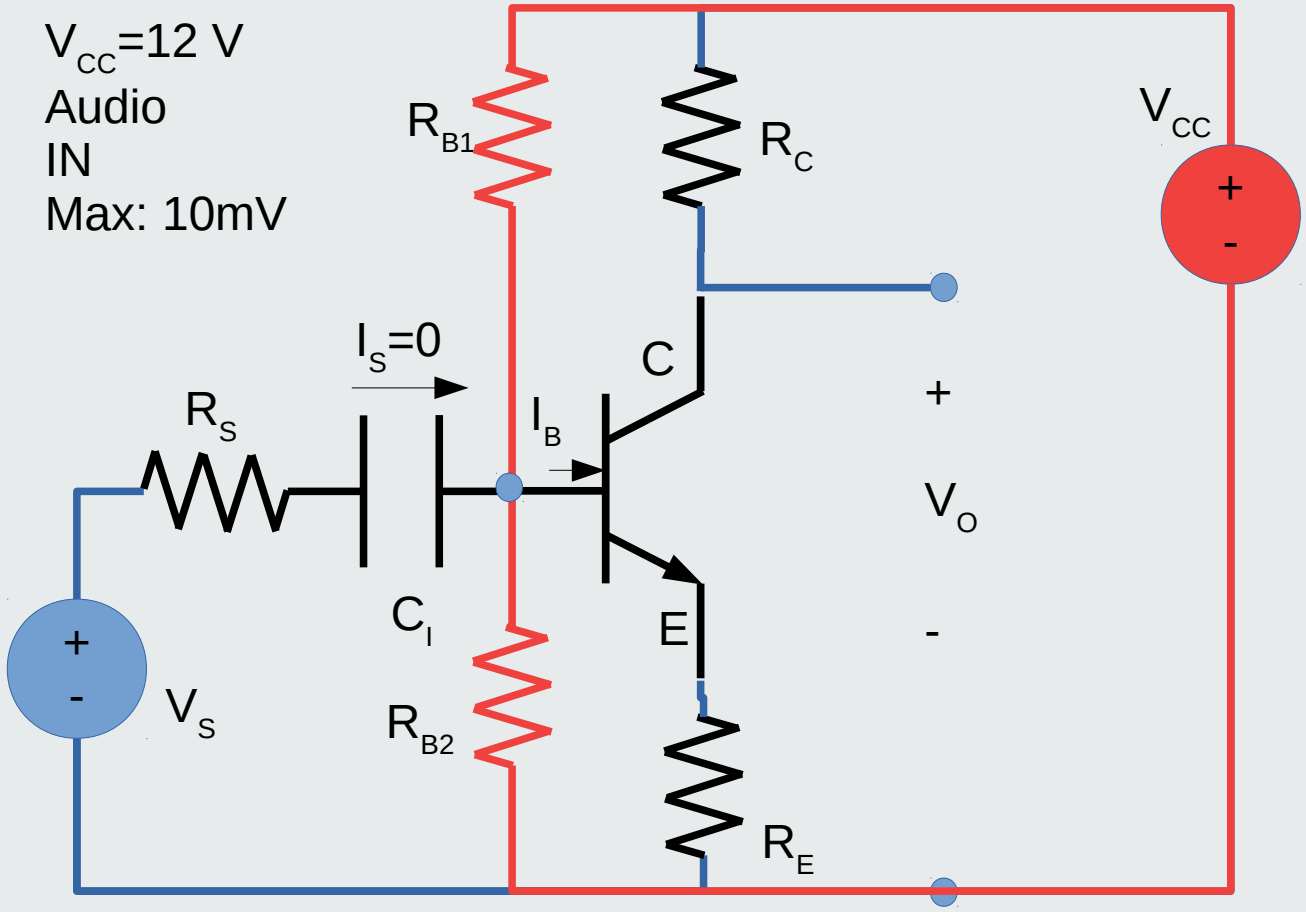
Simulation Analysis

- Write an Ngspice script to simulate the audio amplifier. Start with the provided script
- Use the provided transistor models: the gain stage must use the NPN transistor and the output stage must use the PNP transistor
- Measure the output voltage gain in the passband, the lower and upper 3dB cut off frequencies (the difference between them is the bandwidth), the input and output impedances
- Perform incremental modifications to improve the merit figure
  - Make sure the BJTs operate in the F.A.R. ($V_{CE} > V_{BE}$) by means of a suitable O.P. (For the PNP, $V_{EC} > V_{EB}$)
  - Understand the purpose of the coupling capacitors and their effect on the bandwidth
  - Understand the purpose of the bypass capacitor and its effect on the gain
  - Understand the effect of resistor R_C on the gain

Theoretical Analysis

1) Compute the OP using the theoretical DC model studied. Compare it to Ngspice's OP and explain.
2) Compute the gain, input and output impedances separately for the 2 stages, and explain why they can be connected without significant signal loss.
3) Compute the frequency response $V_o(f)/V_i(f)$, using the incremental circuit, solving the circuit for a frequency vector in log scale with 10 points per decade, from 10Hz to 100MHz.

Gain stage: degenerated common emitter amp; OP(1)



Can't connect source to base directly:

Source has 0V DC value an base needs a different DC value

Source can't bias the BEJ forwardly

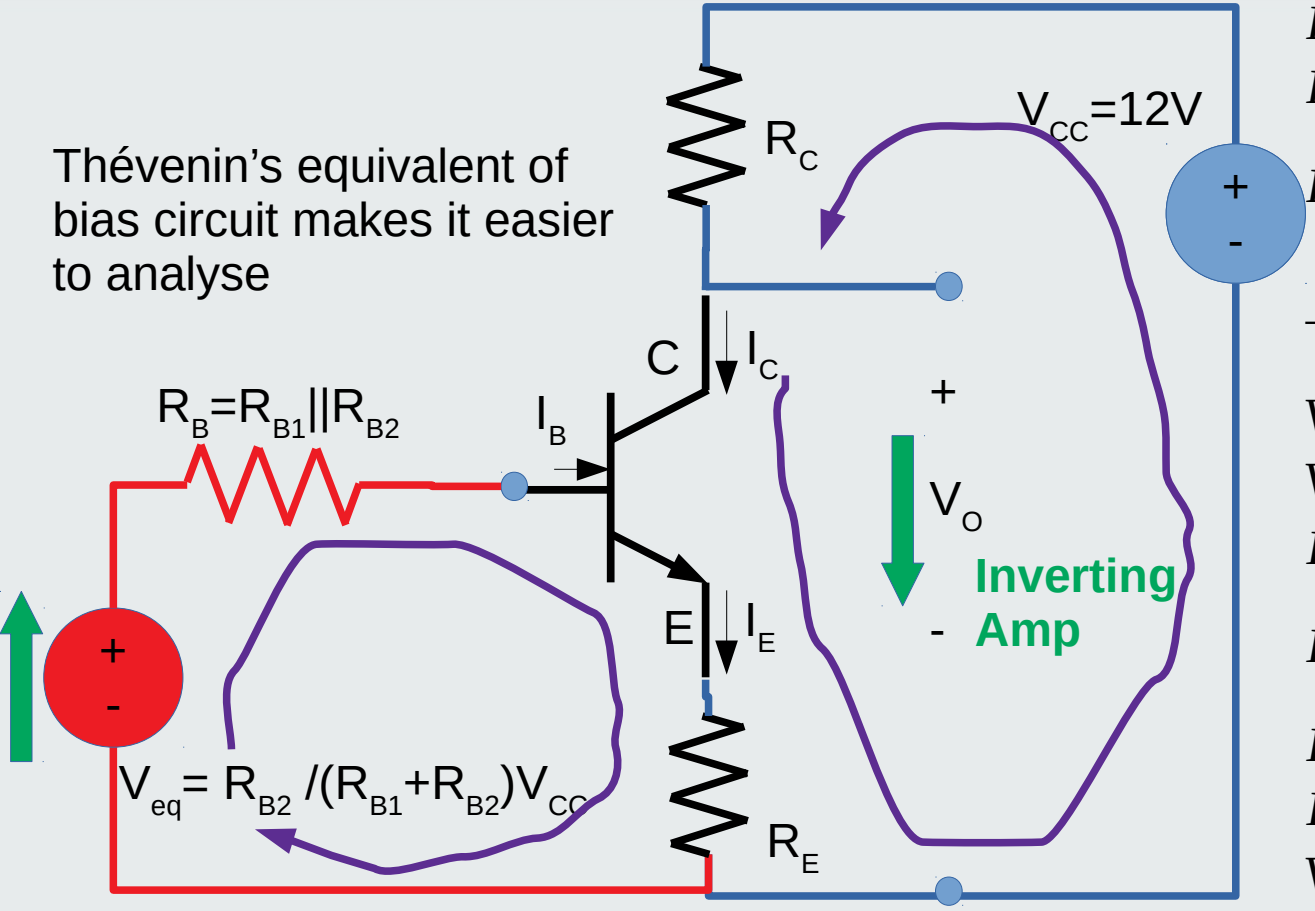
We need a coupling capacitor and a bias circuit

C_I blocks the 0V DC component of V_s (open- circuit at low freq.)

The bias circuit V_{CC},R_{B1},R_{B2} will determine the base voltage V_B and ensure the BEJ is ON!

Gain stage: degenerated common emitter amp; OP(2)

Thévenin's equivalent of bias circuit makes it easier to analyse

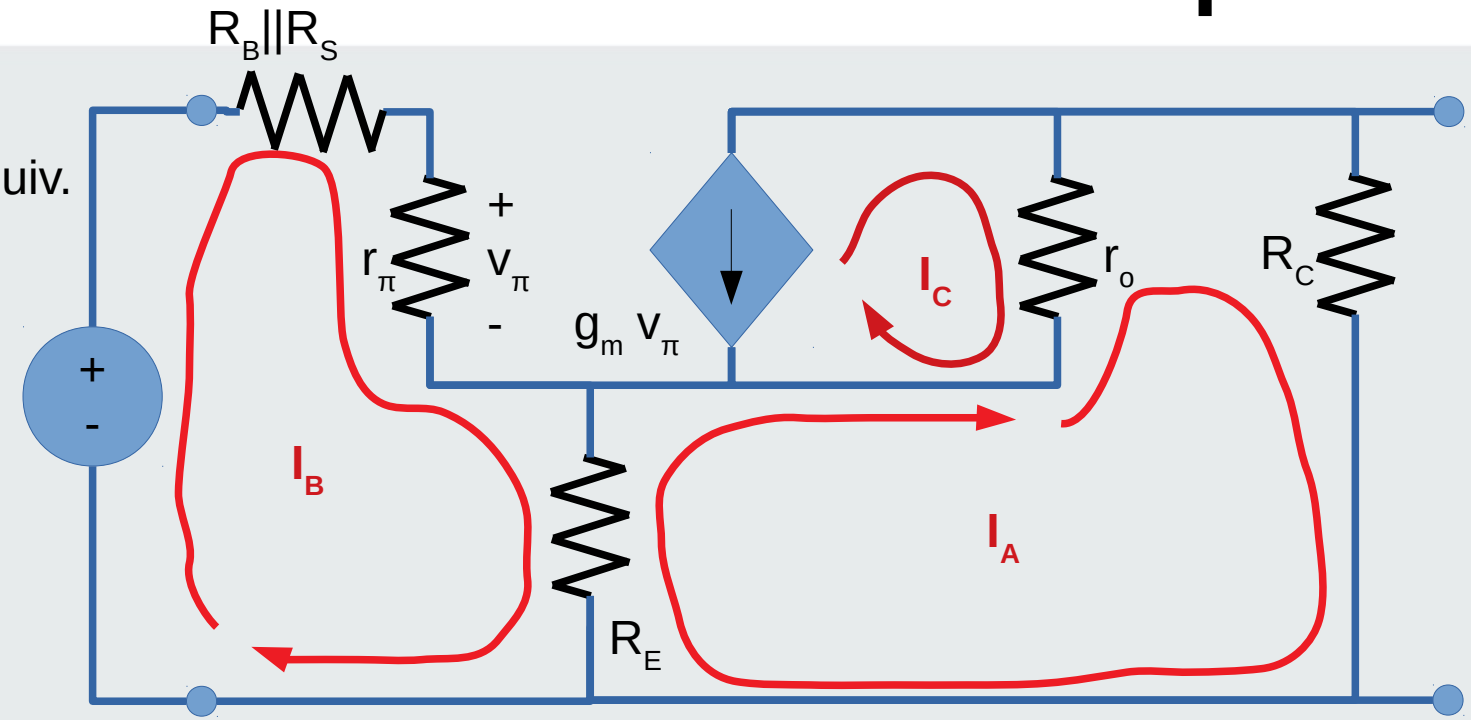


$$R_{B1}=80\,k\Omega$$
$$R_{B2}=20\,k\Omega$$
$$R_B=\frac{R_{B1}R_{B2}}{R_{B1}+R_{B2}}=16\,k\Omega$$
$$-V_{eq}=\frac{R_{B2}}{R_{B1}+R_{B2}}V_{CC}=2.4\,V$$
$$V_{eq}+R_B I_B+V_{BEON}+R_E I_E=0$$
$$V_{BEON}\approx 0.7\,V\ ,\beta_F=178.7$$
$$I_E=(1+\beta_F)I_B$$
$$I_B=\frac{V_{eq}-V_{ON}}{R_B+(1+\beta_F)R_E}=50.04\,\mu A$$
$$I_C=\beta_F I_B=8.24\,mA$$
$$I_E=8.99\,mA$$
$$V_O=V_{CC}-R_C I_C=3.06\,V$$
$$V_E=R_E I_E=0.90\,V$$
$$V_{CE}=V_O-V_E=2.16\,V>V_{BEON}$$

OP complete: all static voltages and currents computed!

Confirms FAR:

Gain stage: incremental circuit for medium frequencies



From BC547A model

$V_A = 69.7\,V$

$\beta_F = 178.7$

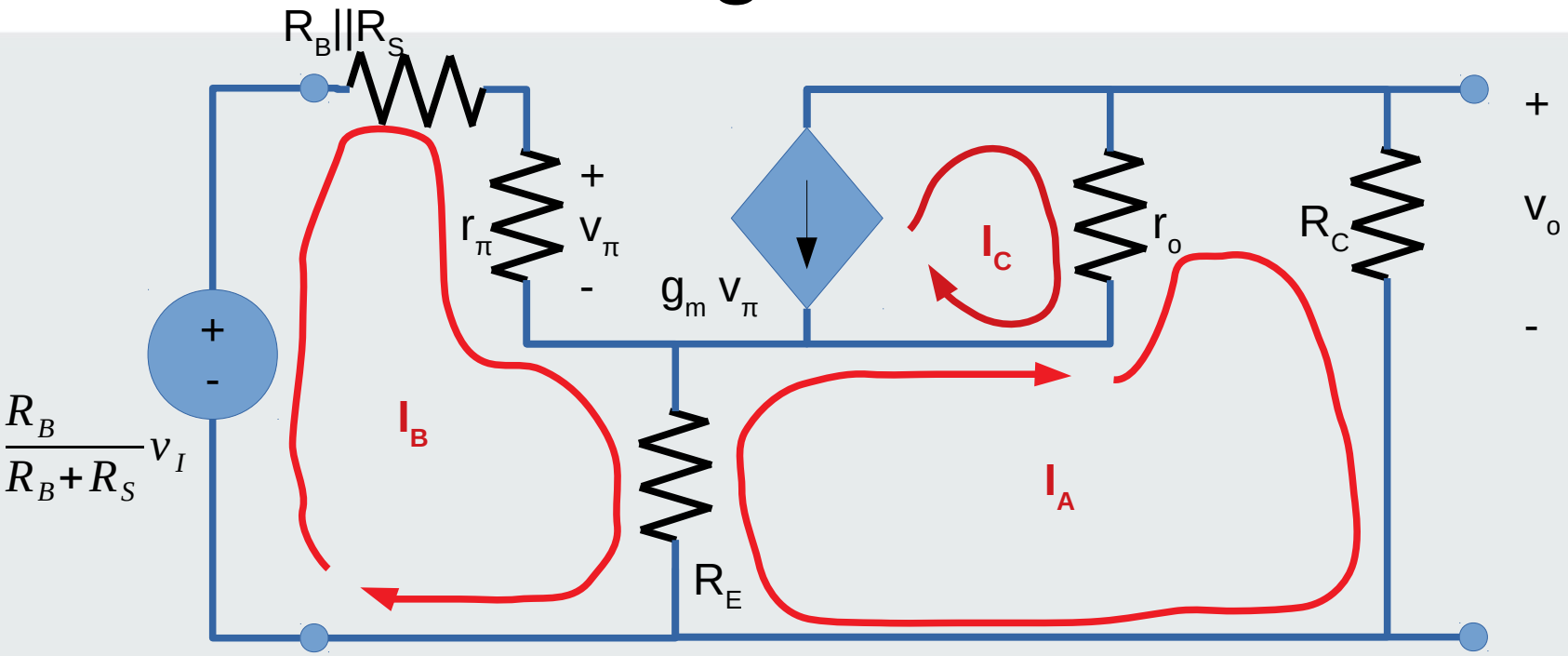
Incremental parameters:

$$g_m = \frac{I_C}{V_T} = 358\,mS$$

$$r_\pi = \frac{\beta_F}{g_m} = 500.0\,\Omega$$

$$r_o \approx \frac{V_A}{I_C} = 7.79\,k\,\Omega$$

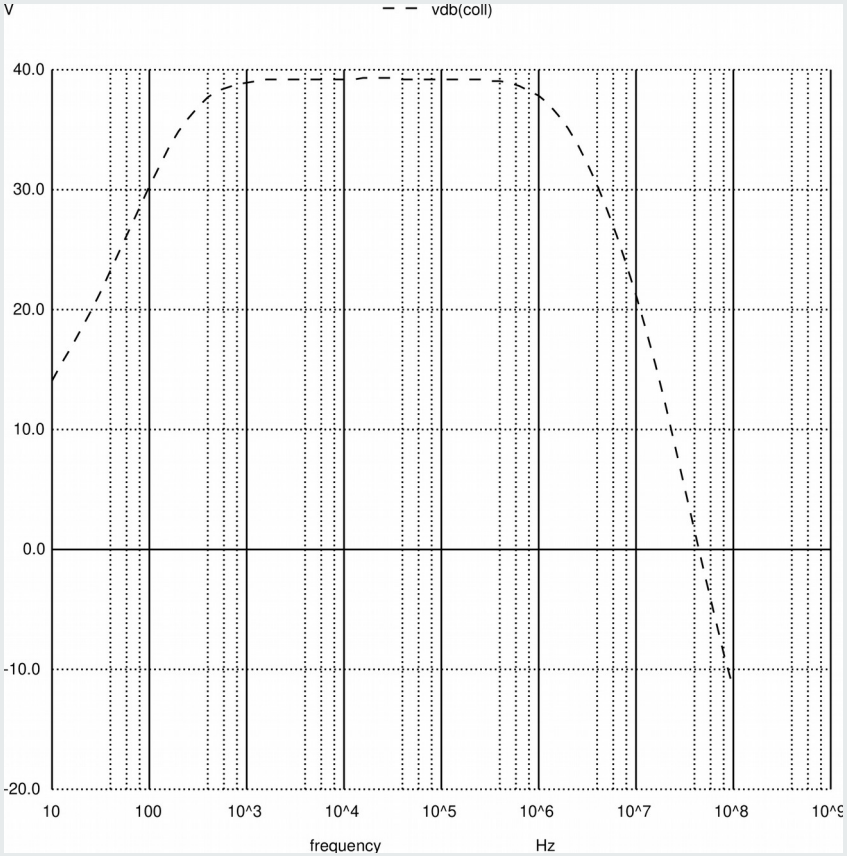
Gain stage: incremental circuit gain



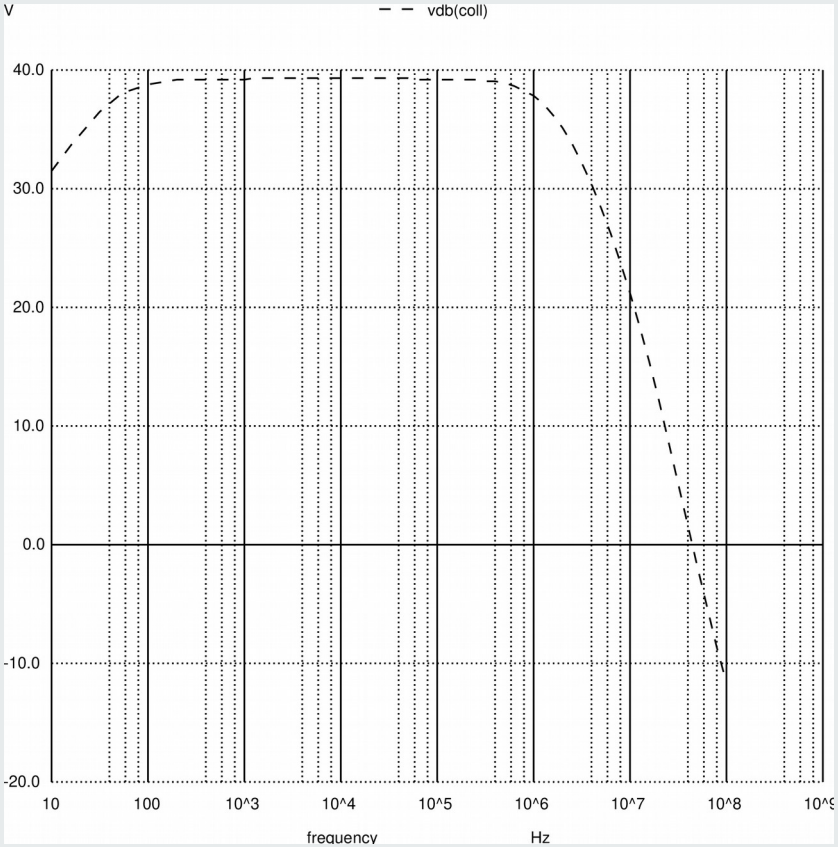
From previous lecture

$$\frac{v_o}{v_i} = \frac{R_B}{R_S+R_B} R_C \frac{R_E - g_m r_\pi r_o}{(r_o+R_C+R_E)(R_B||R_S+r_\pi+R_E)+g_m R_E r_o r_\pi - R_E^2} = -9.51$$

Gain stage: effect of the input coupling capacity



Input capacitance too low!
Lower cutoff frequency too high!

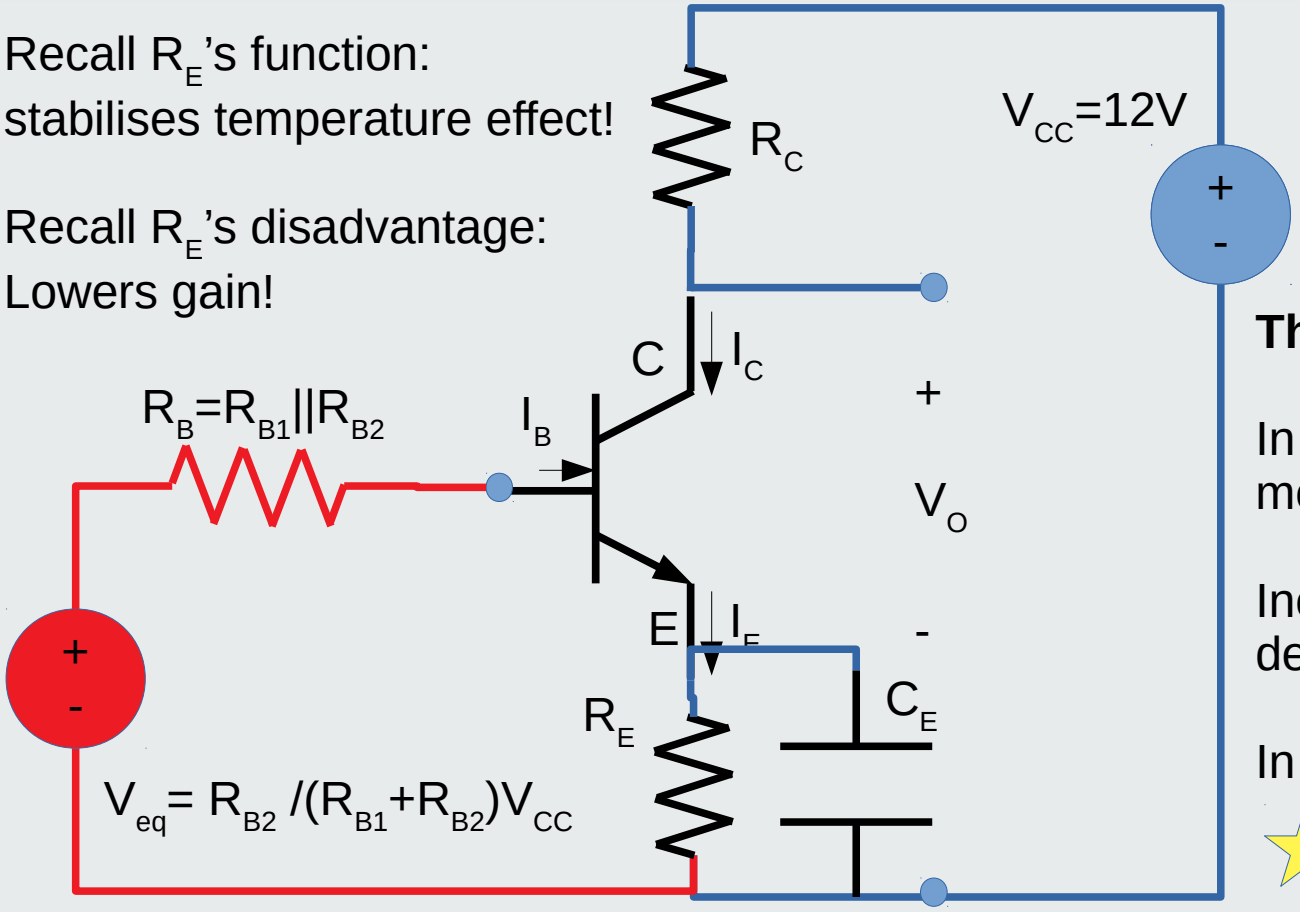


Input capacitance good enough!
Lower cutoff frequency close to 20Hz.

Gain stage: bypass capacitor

Recall R_E's function:
stabilises temperature effect!

Recall R_E's disadvantage:
Lowers gain!



The best of both worlds:

In DC temperature stability is most important

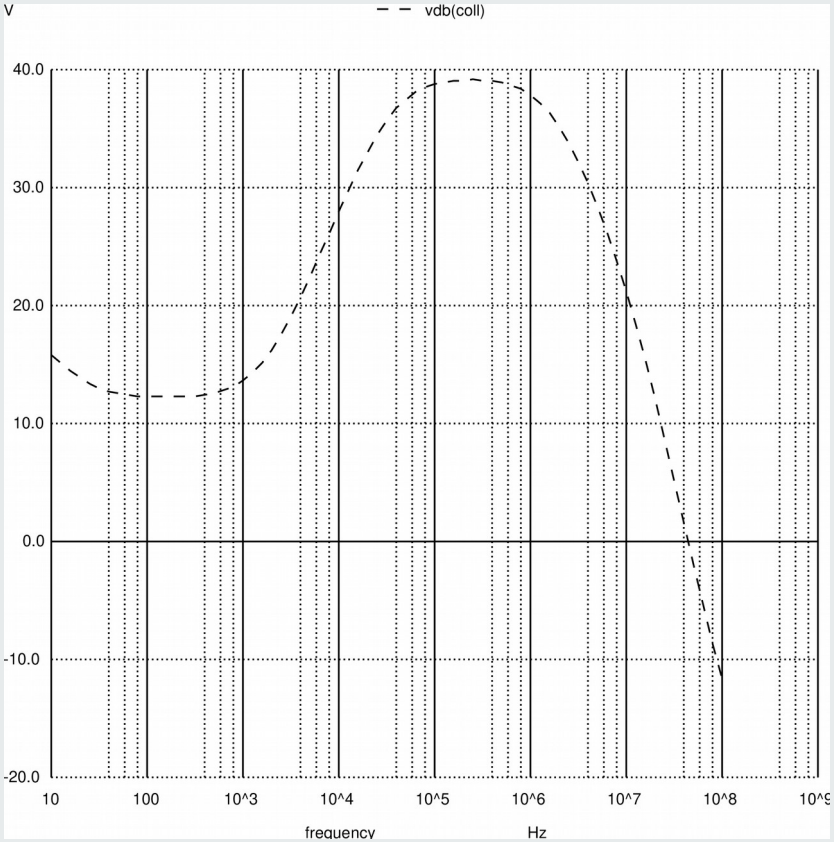
Incremental parameters depend on DC values

In AC gain is most important

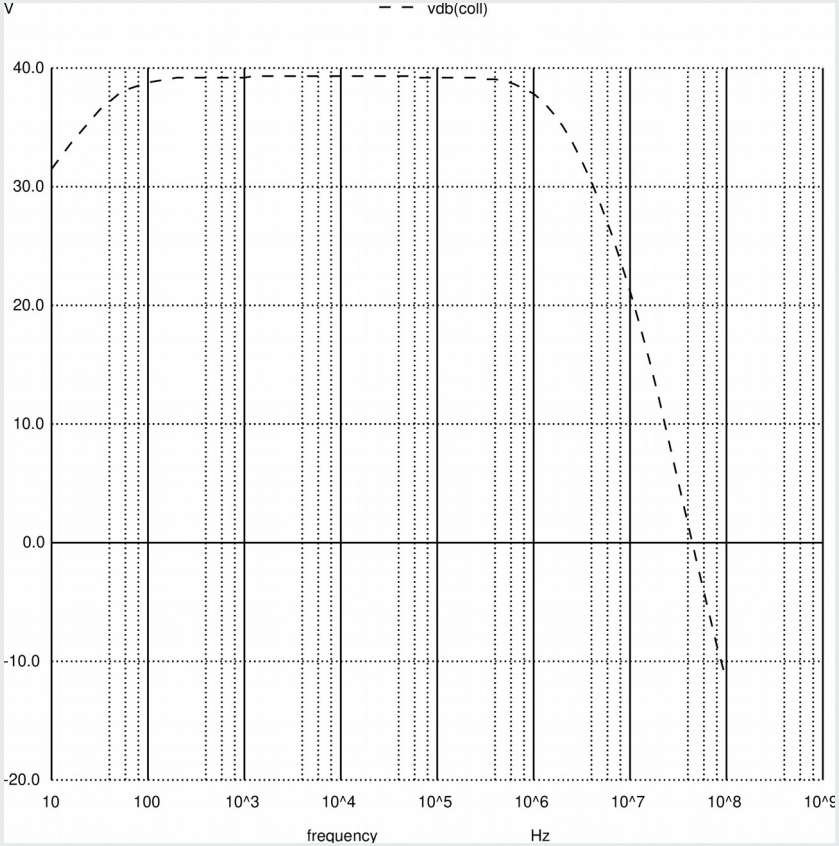
Use a capacitor C_E to bypass R_E!!!!!

CE is an open-circuit for low frequency (DC) and a short-circuit for higher frequencies (AC)

Gain stage: effect of the bypass capacitor

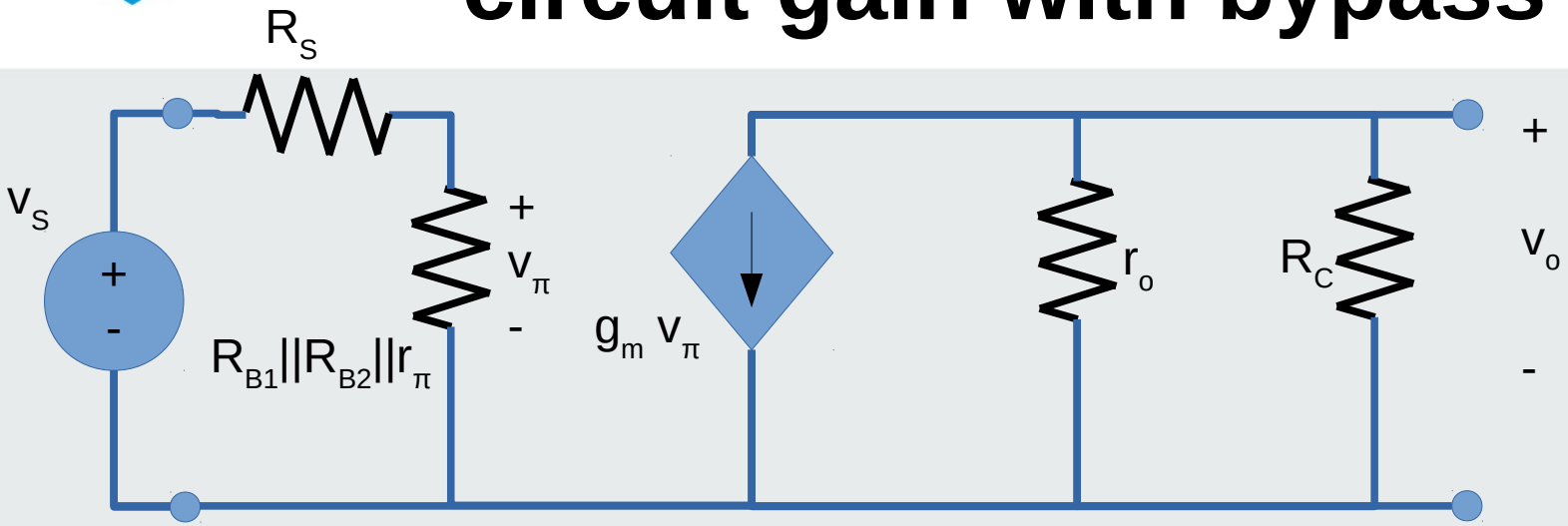


Bypass capacitance too low!
Gain is low in part of the bandwidth!



Bypass capacitance good enough!
Gain is stable in desired passband.

Gain stage: incremental circuit gain with bypass C



With $R_E = 0$:

$$\frac{v_o}{v_i} = -g_m (R_C || r_o) v_\pi$$

$$v_\pi = \frac{r_\pi || R_{B1} || R_{B2}}{R_S + r_\pi || R_{B1} || R_{B2}} v_S$$

$$\frac{v_o}{v_i} = -g_m (R_C || r_o) \frac{r_\pi || R_{B1} || R_{B2}}{R_S + r_\pi || R_{B1} || R_{B2}} v_S$$

Gain stage: input and output impedances

$$Z_I = R_{B1} || R_{B2} || r_\pi = 484.43\,\Omega$$

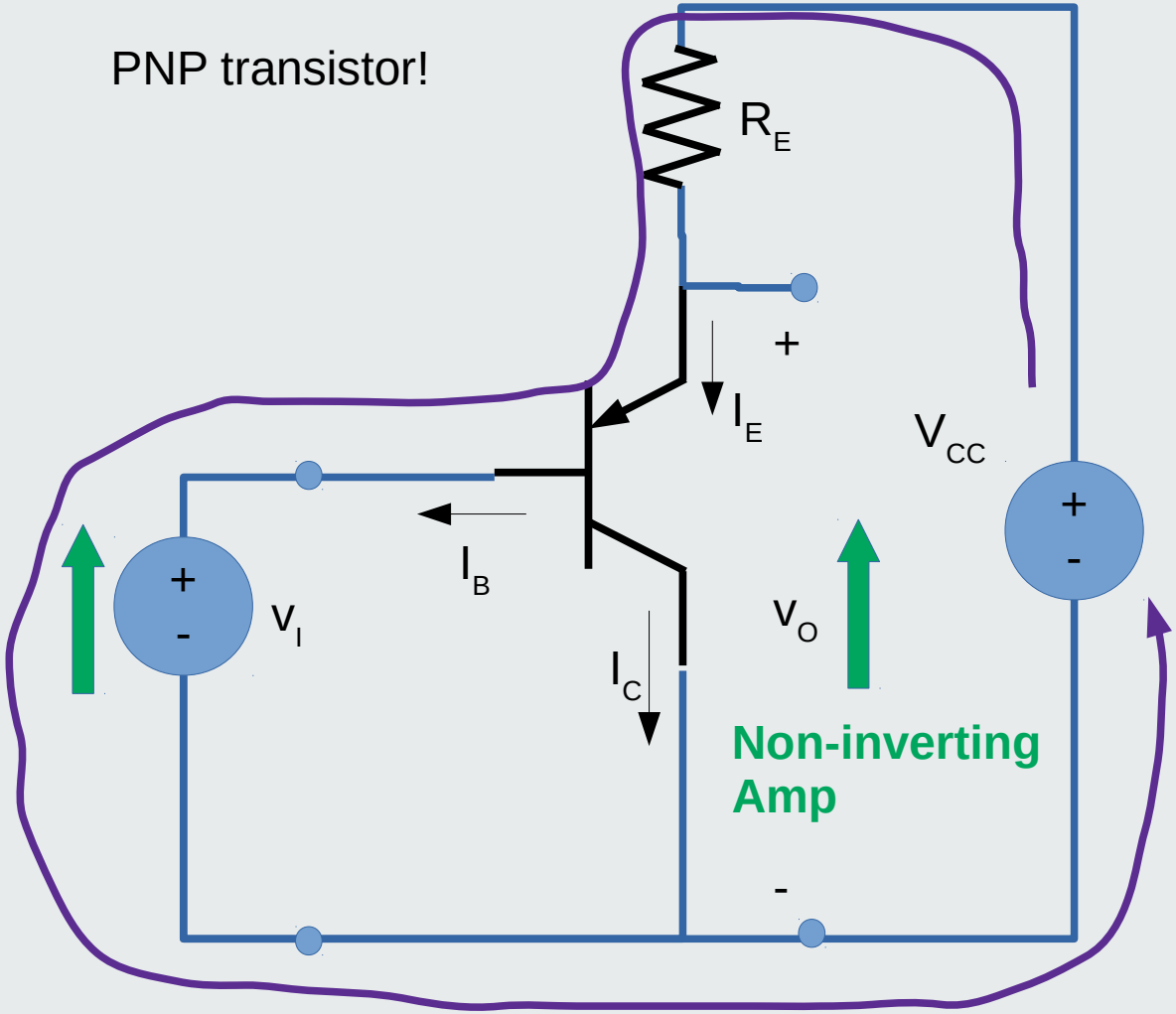
Not very compatible with R_S = 100 Ω

$$Z_O = R_C || r_o = 886.28\,\Omega$$

Certainly cannot be connected to an 8Ω load!!

An output stage is in demand!!

Output stage: common collector amplifier OP

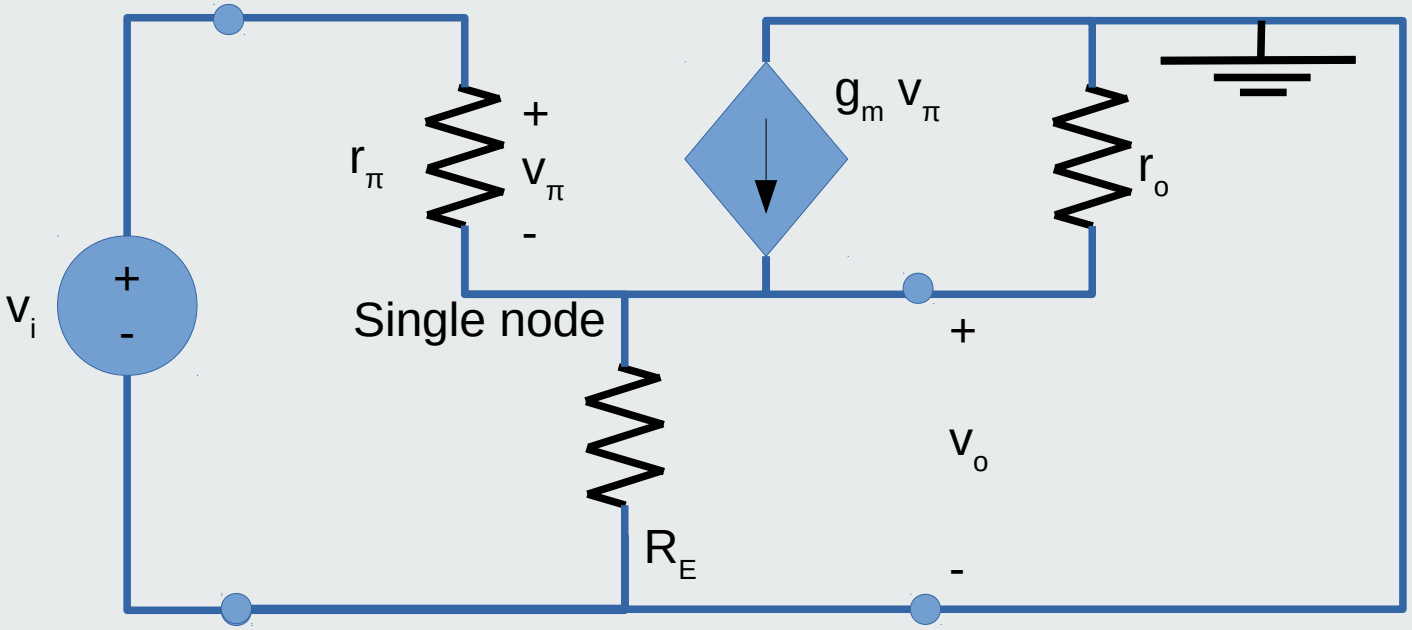


$$V_{CC} = 12\,V$$
$$V_{EBON} \approx 0.7\,V$$
$$R_E = 100\,\Omega$$
$$R_E I_E + V_{EBON} + V_I - V_{CC} = 0$$
$$I_E = \frac{V_{CC} - V_{EBON} - V_I}{R_E} = 82.24\,mA$$
$$V_O = V_{CC} - R_E I_E = 3.76\,V$$
$$V_O = V_I + V_{EBON}$$

Output current I_E much stronger than in Gain Stage!

Part of this current will feed the Load!

The common collector amplifier: voltage gain



Convenient to work with admittances

$$g_\pi = \frac{1}{r_\pi}$$

$$g_E = \frac{1}{R_E}$$

$$g_o = \frac{1}{r_o}$$

KCL: $$\left(\frac{1}{R_E}+\frac{1}{r_o}\right)v_o + \frac{v_o - v_i}{r_\pi} - g_m v_\pi = 0$$

$$v_\pi = v_i - v_o$$

$$\frac{v_o}{v_i} = \frac{g_m}{g_\pi + g_E + g_o + g_m} = 0.99$$

Almost unitary gain as predicted!

From BC557A model $V_A = 37.2\,V$, $\beta_F = 227.3$

Output stage: input and output impedances

From previous lecture:

$$Z_I = \frac{g_\pi + g_E + g_o + g_m}{g_\pi (g_\pi + g_E + g_o)} = 8.6\,k\Omega$$

Quite compatible with gain stage Z_O = 886.28 Ω

$$Z_O = \frac{1}{g_\pi + g_E + g_o + g_m} = 0.3\,\Omega$$

Amazingly low output impedance!

Very good to connect to an 8Ω load!

The output stage is doing its job!!

Another coupling capacitor between the Output stage and the load is also needed.

Lab report

1) Produce all tables and plots required in the simulation and analysis sections
2) Compare Octave and Ngspice results side by side looking for accuracy or discrepancy, and explaining both. Read the repository's README file.
3) The results of interest are, obviously,

   - the gain's frequency response

   - input /output impedances to support the driver (input audio source) and load (speaker), respectively, adequately

   - the cost of the components used

Evaluation criteria

1) The instructor should *git pull* your repo, and run *make flawlessly*
2) The report should not have obvious mistakes in figures, tables, formulae, section titles or main sentences
3) 1 bonus point (mark can be 5 offsetting previous grade losses) for the 5% best merit figures

    - if your work is in the top 5%, expect a more thorough review