TÉCNICO LISBOA

Master Degree (M.Sc.) in Electrical and Computer Engineering

5th year, 1st Quarter

2021-2022

Ultra Low Power Circuits

(*Circuitos de Ultra-Baixo Consumo*)

Cadence Laboratory Guidelines

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Ver. 1.0

(prepared for Cadence 6.1.7 and AMS HitKit 4.10)

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Introduction

The goal of this document is to guide the students throughout the laboratory and project part of this course.

This is an "under construction" document and will be changed throughout the course.

Setting and running Cadence 6.1.7 and the AMS (4.10) Design Kit

To set, in the lab, the Cadence environment and the AMS 0.35µm CMOS design kit (AMS Hitkit) do the following

1. **First time only**

   (ALL STUDENTS SHOULD HAVE THE FENIX AFS SYSTEM ACTIVATED)
   (https://ciist.ist.utl.pt/ciistadmin/user/)

   (One of the group elements logs in with fenix user/passwd)

   >ssh -X ist<ist_number>@fatima2.vps.tecnico.ulisboa.pt (login in the user area)

   (In a WINDOWS environment it is necessary to have an Xserver installed (i.e., exceed, win32, Xming, cygwin, etc) and putty configured to import X)

   >mkdir CADENCE

   (create shared folder in one of the group elements directory)

   > fs sa -dir "CADENCE" -acl ist<number> rlidwk

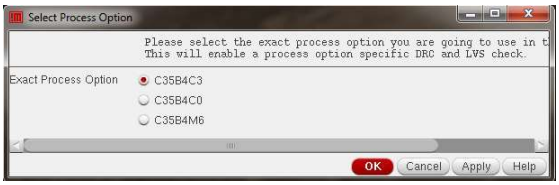
   >cd CADENCE

   >mkdir C35

   > cd C35

   >source **/opt/ic_tools/init/init-amsC35-410**

   >ams_cds –tech c35b4 &



2. **Regular login**

   >ssh -X ist<ist_number>@fatima2.vps.tecnico.ulisboa.pt

   >cd CADENCE/C35

   >source /opt/ic_tools/init/init-amsC35-410

   > ams_cds &

Getting Started

The Cadence main window (Fig. 1, Common Interface Window, CIW) is opened. From the CIW menus, all Cadence main commands, tools, and options are available. This main window also reports all the output information whatever Cadence tools you are working in. Here you can at first see the **NEW** and **OPEN** commands that allow the user to open a new, or an existing, library and then a cell inside a library. It also has the EXIT command which ends the Cadence session.

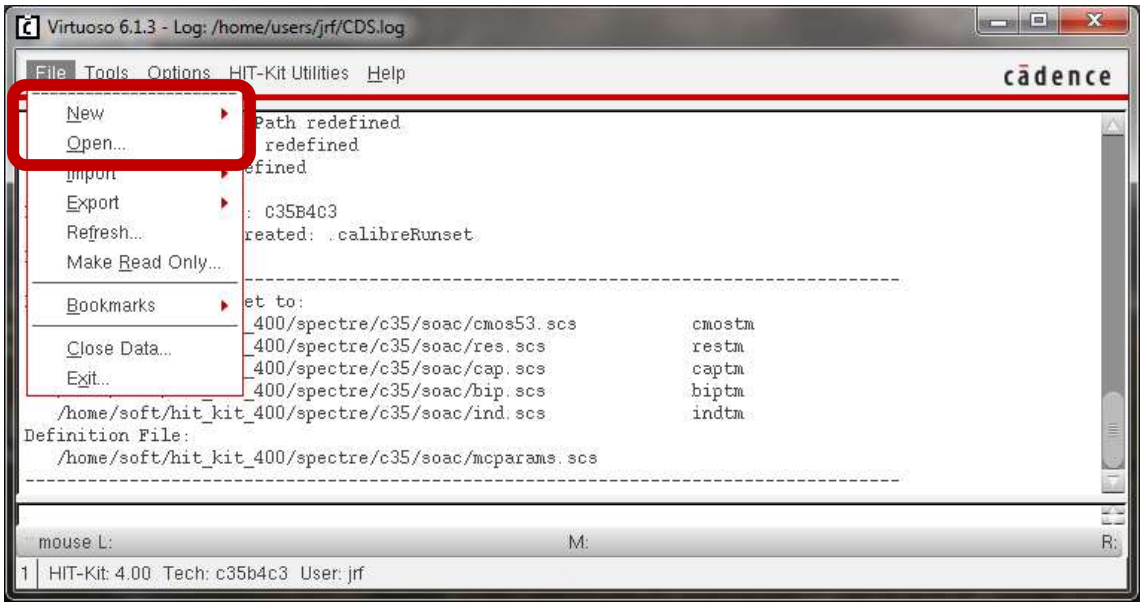


Fig. 1. CIW window

The Library Manager Window also opens when starting Cadence (Fig.2). In this library you have access to all basic "SPICE" circuit elements in the "**analogLib**", the AMS elements are in the "**PRIMLIB**", and more complex functional elements as ADCs and DACs are in the "**ahdlLib**". Then you can add your own libraries that will appear in the Library column as you name them (i.e., I have included **SIA2012**). A library contains cells, and a cell can contain several views. Most used views for the designer in this course are the **symbol**, the **veriloga**, the **schematic**, the **layout**, and the **extracted**. The other views are used by the software with little action from the designer.

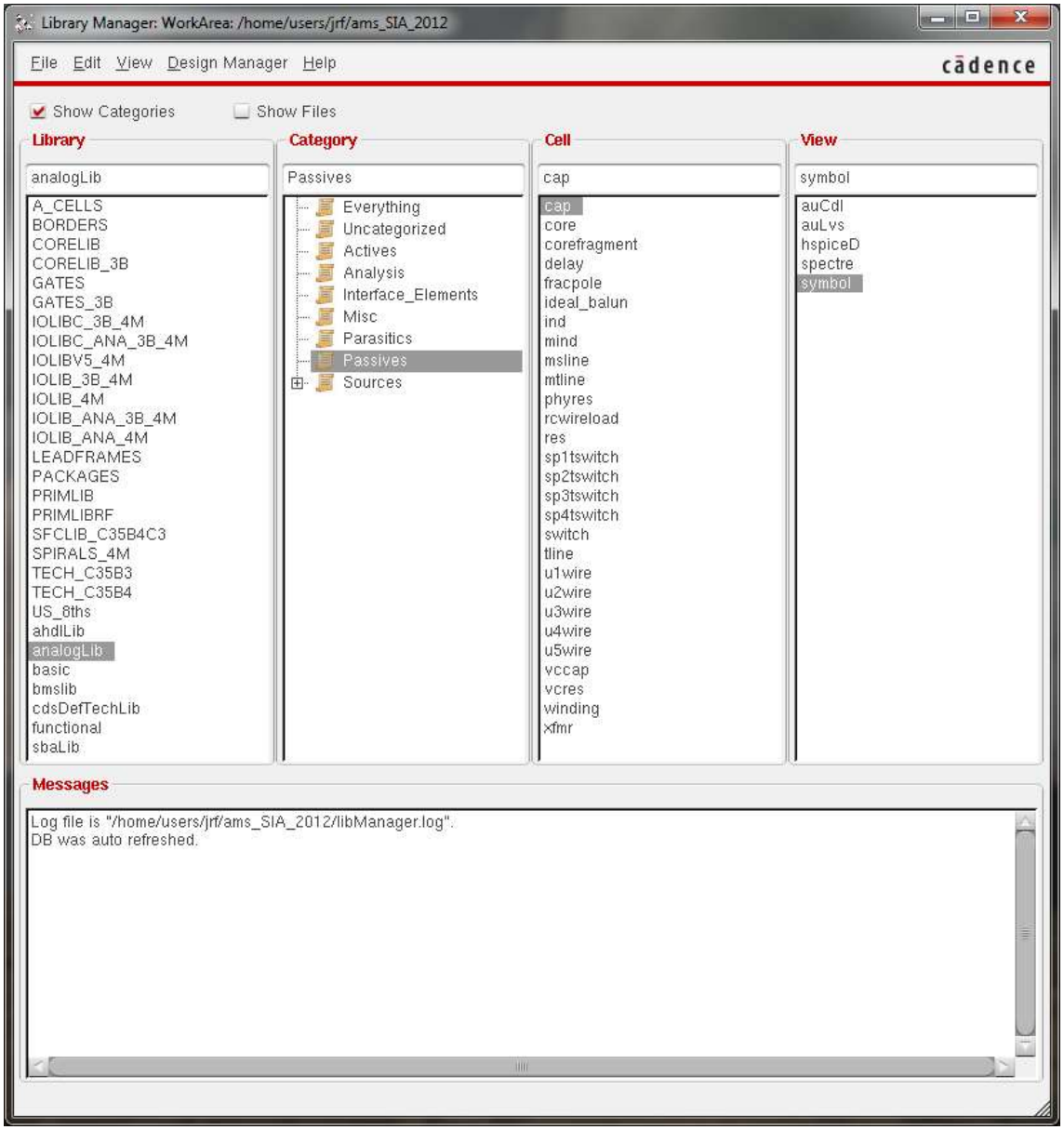


Fig. 2. Library Manager window

Analog Design Environment XL (ADE XL)

Open a new file with a test cell name and an “adexl”view; then open a “schematic” as shown in Fig. 3. The window view is represented in Fig. 4 where you can see the window and the ADE interface for simulation together. This simulator has more options than the basic ADE L, it will allow, for instance, to do Monte Carlo analysis and other types of simulations useful for analog design. You can now start populating it with circuit elements.

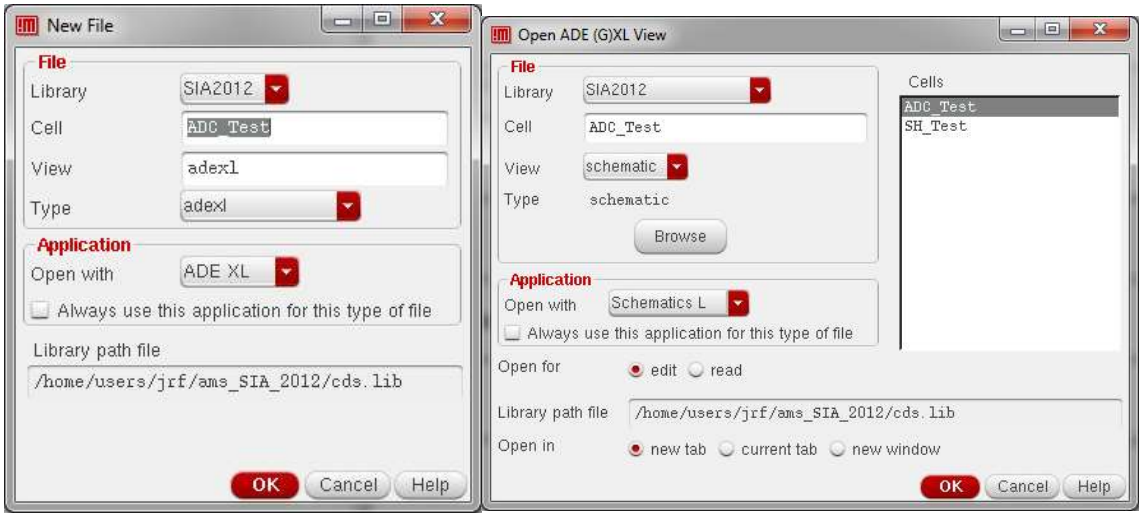


Fig. 3. Create ADE XL view of the circuit

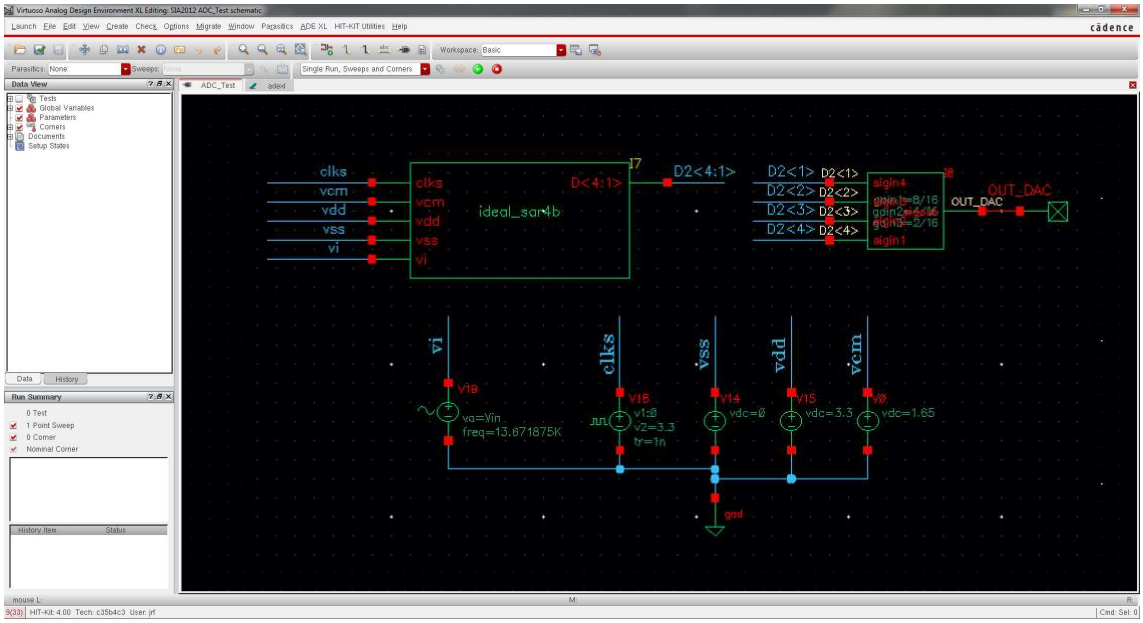


Fig. 4. ADE XL interface of the circuit

Hands on tutorial: Cadence Design Environment (1weeks)

Goals:

1. Introduction to CADENCE DF II (version 6) with ADE L and XL
2. Introduction to analog design flow at transistor level.
3. Execute the flow:
    a. Input schematic.
    b. Creating symbols, work hierarchically.
    c. Simulation
    d. Layout Design and verifications (DRC, LVS)
    e. Netlist Extraction, verification and simulations
    f. GDS2 file generation for tapeout

Note1: This is not a standalone document; it does not provide information on the technology and it does not provide information on all options of the software tools.

Note2: The layout do not require to be optimized

To Do:

1. Open a new Library (example "SIA2020") and open a new Cell (example "Amplifier"), schematic view for a two stage amplifier circuit.
2. Import components from the analogLib and PRIMLIB and do the schematic represented in Fig. 4 with all the specifications. Add names to the wires to make it easier to identify the curves after simulating.

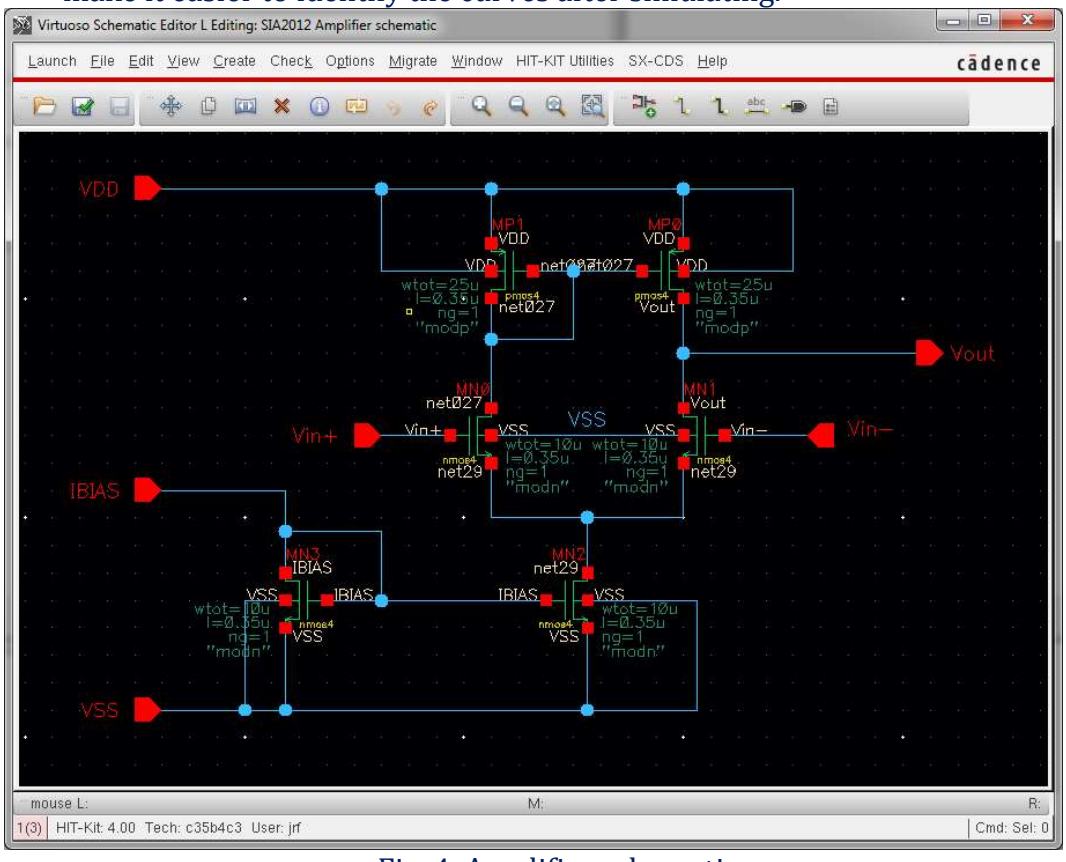


Fig. 4. Amplifier schematic

3. Design hierarchical
    a. Create a symbol select: Create > Cellview > From cellview.
    b. A window appears by default, click OK.
    c. A window with the created symbol opens (Fig. 5); it can be edited if one wants to have it more meaningful (Example: design an OPAMP symbol).
    d. The amplifier may now be used in a higher hierarchical schematic.

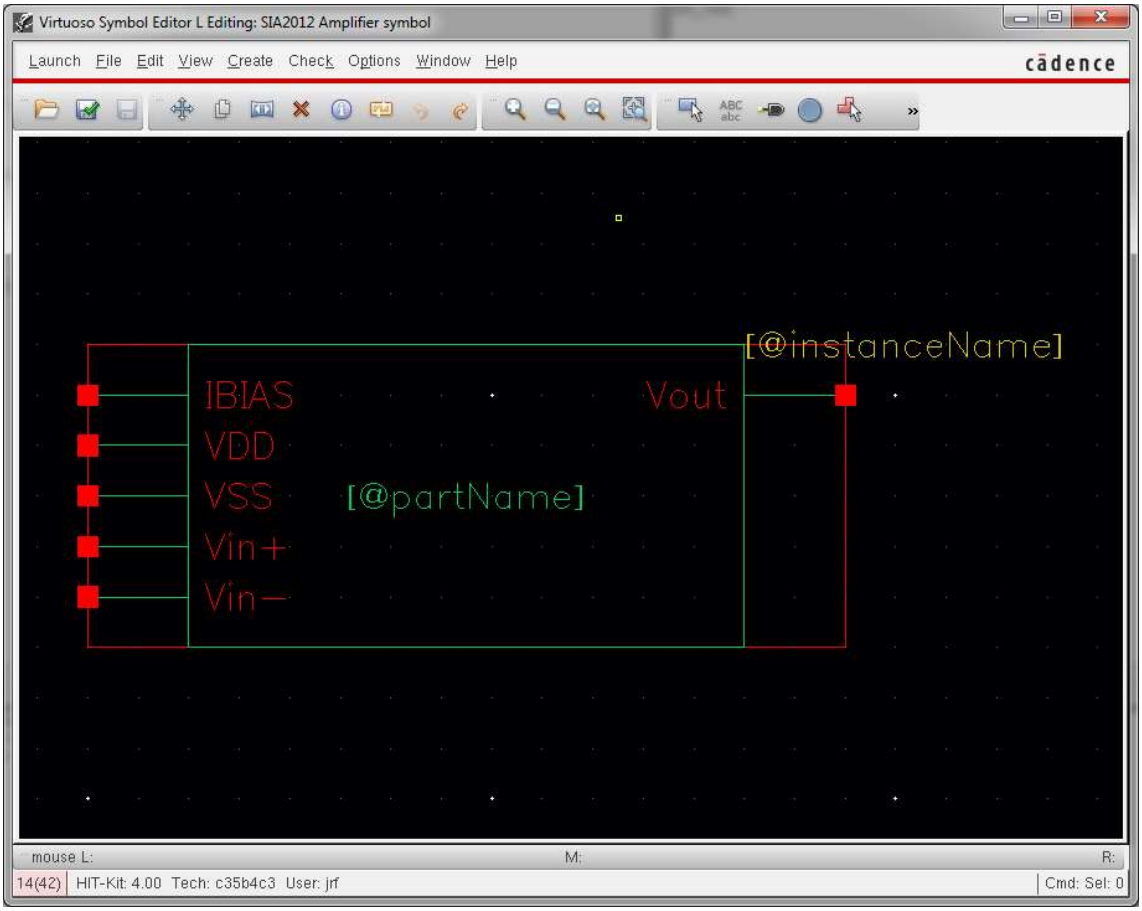


Fig. 5. Amplifier symbol

4. Create a new schematic with the testbench:
    a. Create a new Library named “(same name) _Sim” (example “SIA2020_Sim”)
    b. Create a new cell with the same name (example: “Amplifier”) and a view related with the respective simulations.
    Only one simulation should exist per view, however in this report for simplicity we will have a single setup for dc, ac and transient analysis.
    c. Design the schematic in Fig. 6 (See the source properties in Fig. 7).

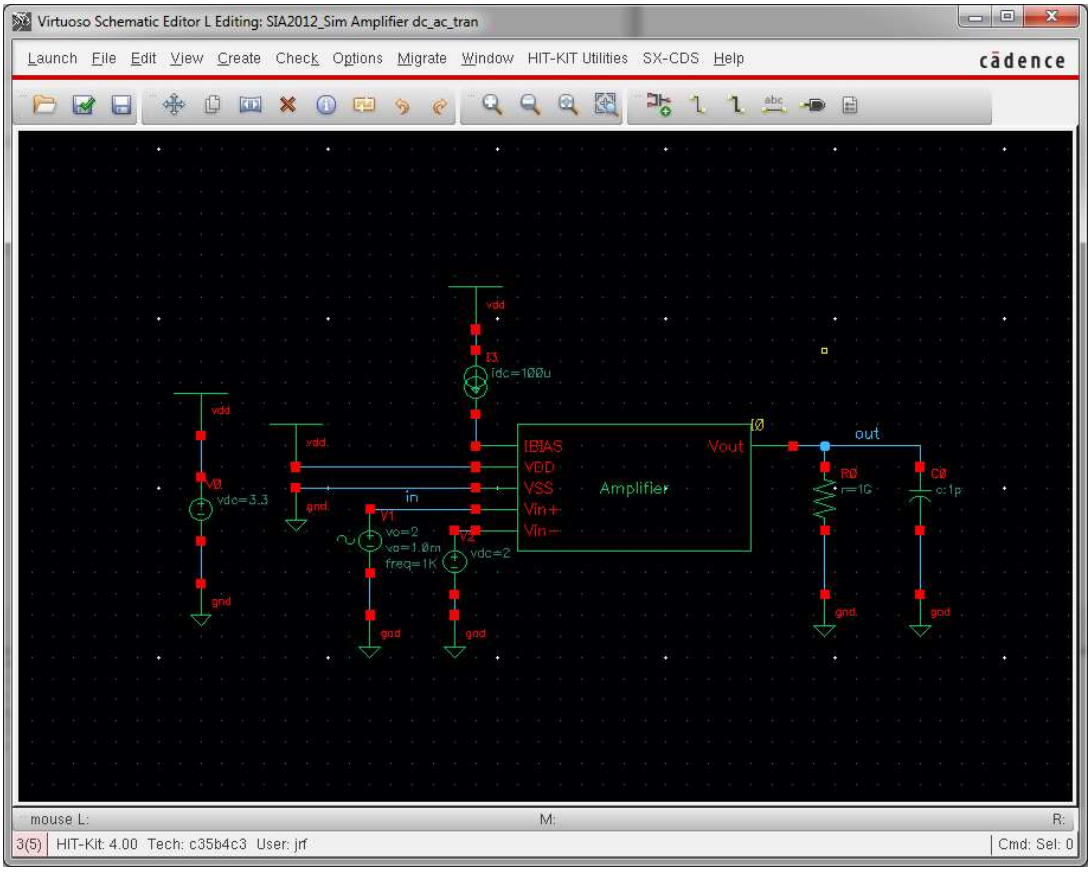


Fig. 6. Simulation Testbench

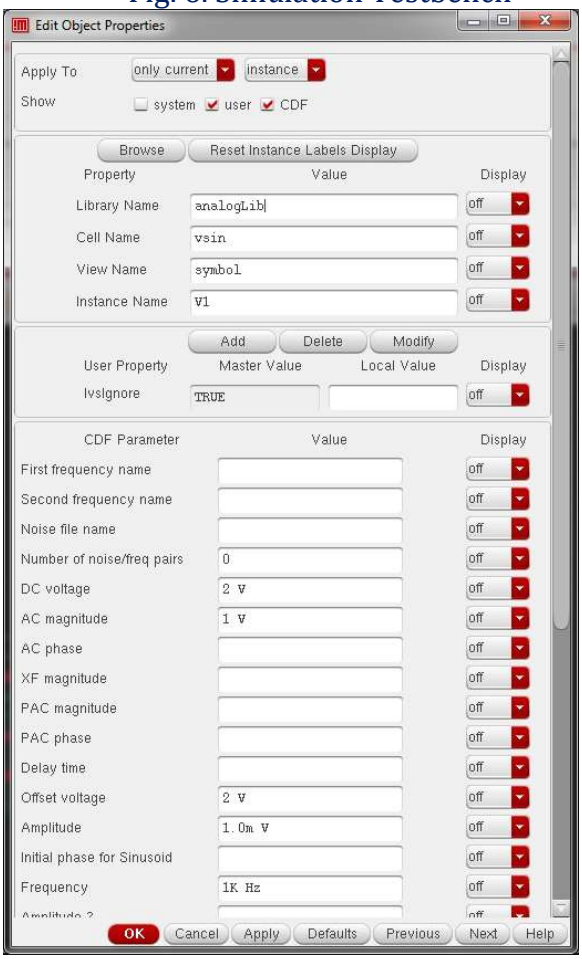


Fig. 7. Source description

5. Simulate the circuit using the “Analog Environment” dialog window for DC, AC, transient and noise analysis in Fig. 8, according to the information in Fig. 9.

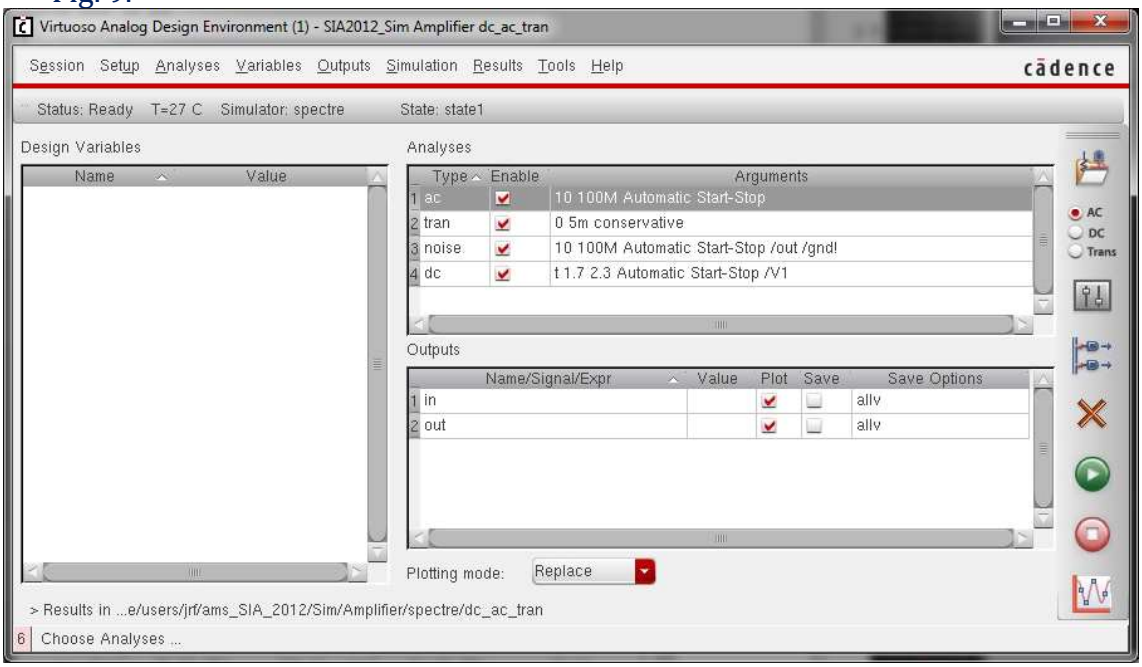
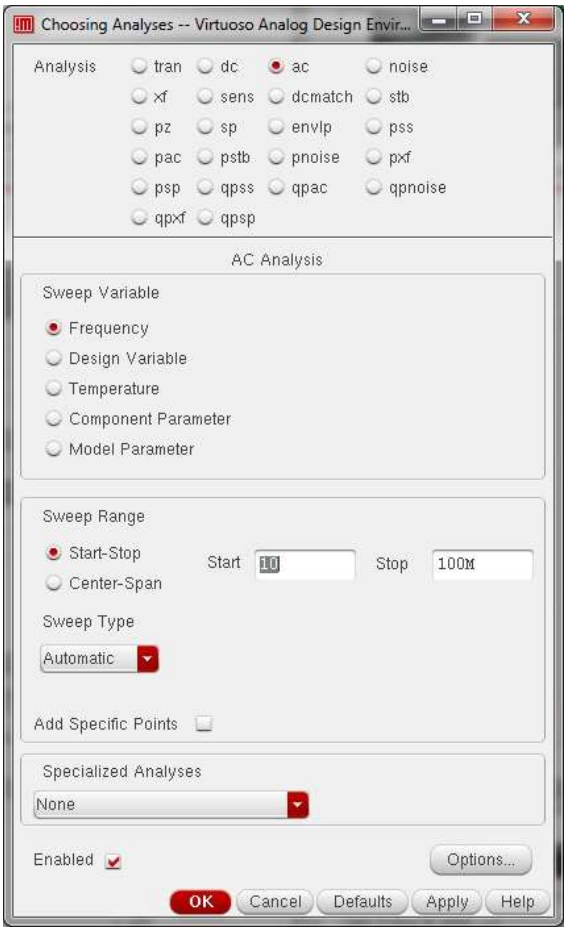


Fig. 8. Simulation Window



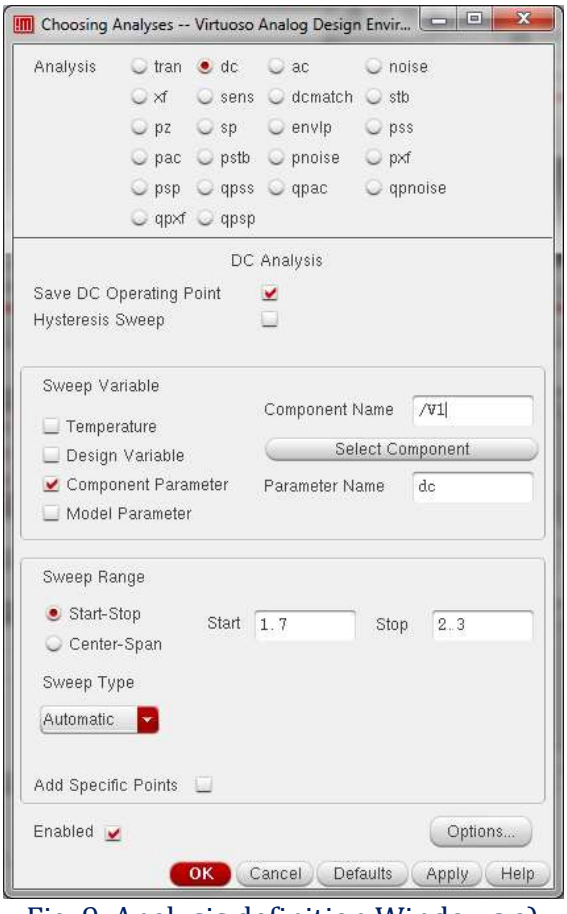
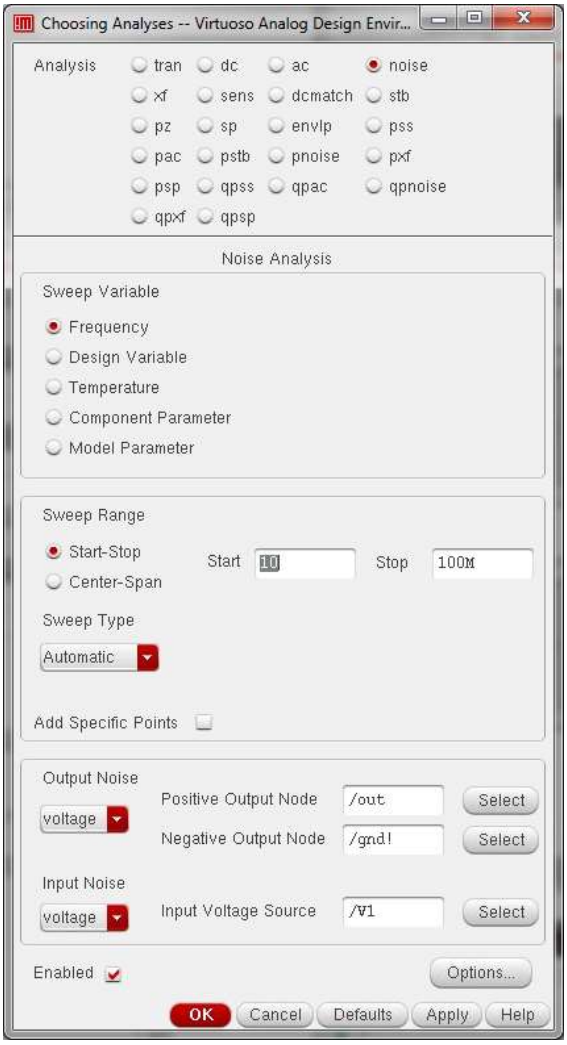


Fig. 9. Analysis definition Windows a)



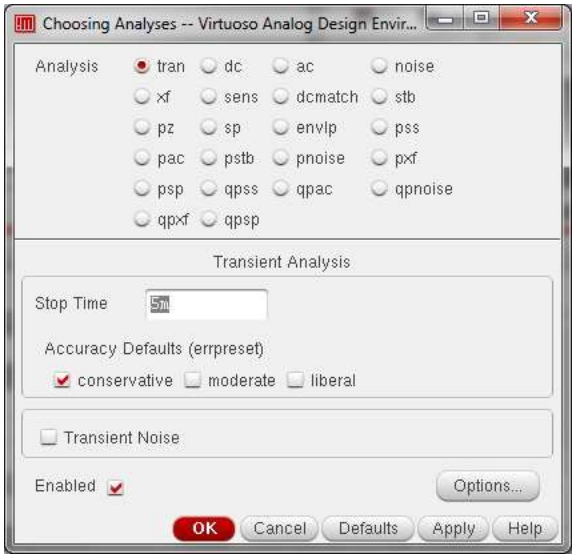


Fig. 9. Analysis definition Windows b)

6. The waveform window should look like the one represented in Fig.10.

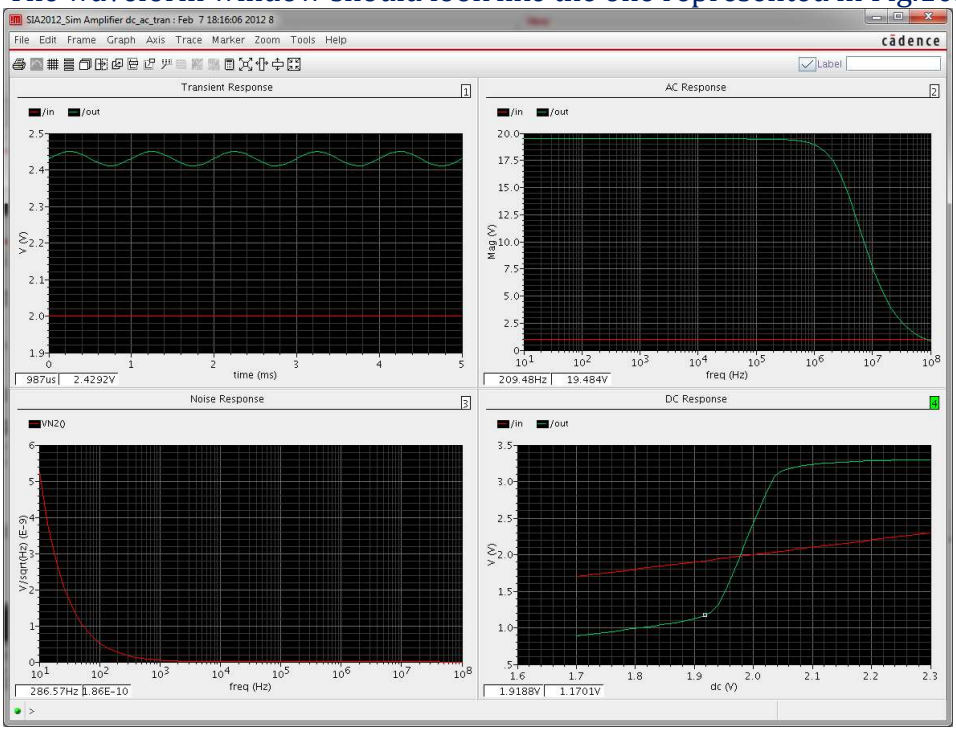


Fig. 10: Waveform Window

7. Perform a 3 run Monte Carlo simulation on the circuit.
    a. In the "Analog Design Environment" window do: Setup→Model Libraries
    b. Observe Fig. 11, select the line corresponding to the CMOS transistor models, change section to "cmosmc", click "Change" click "OK"

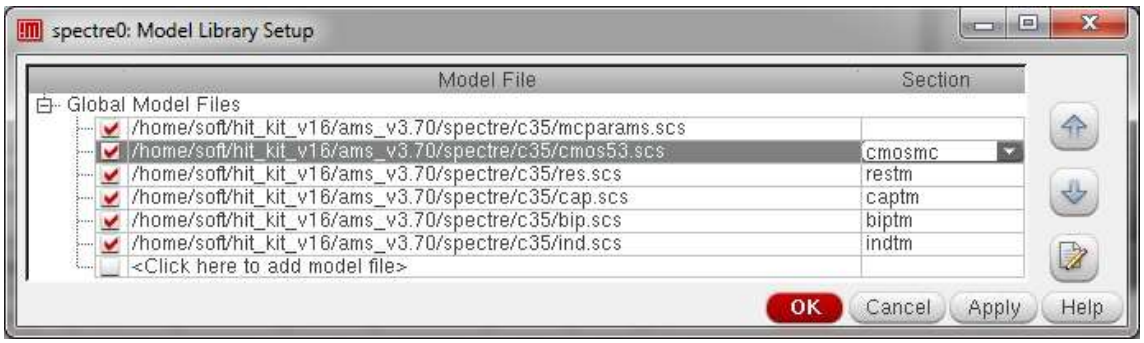


Fig. 11: Model Library Setup window

    c. In the "Analog Design Environment" window do: Tools→Monte Carlo
    d. Parameterize the window as represented in Fig. 12.

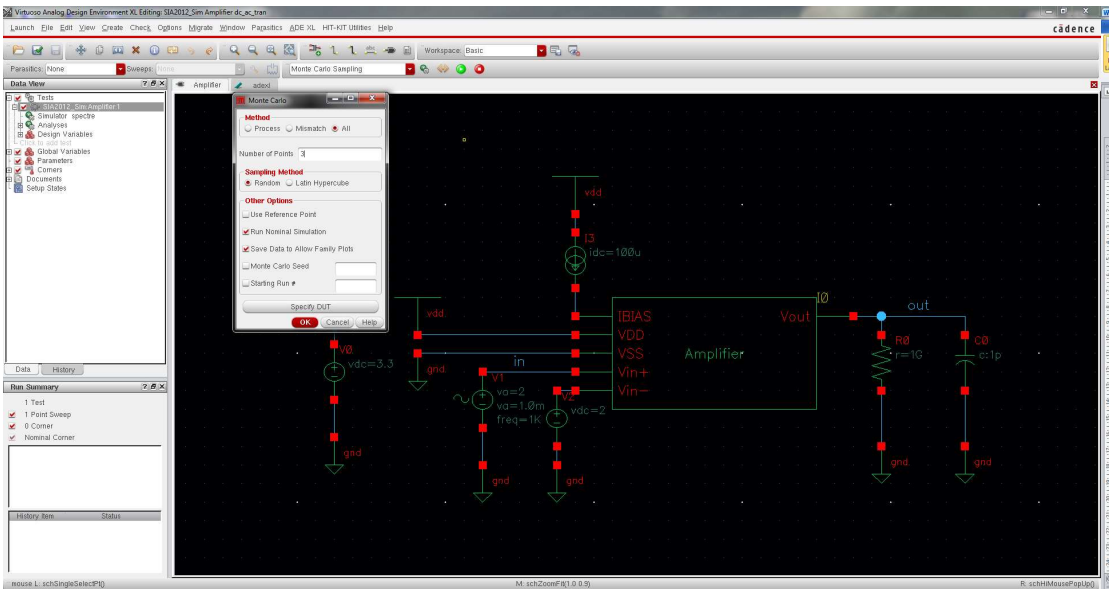


Fig. 12: Monte Carlo analysis window

    e. Do: Simulation→Run and observe the waveform window (Fig. 29).

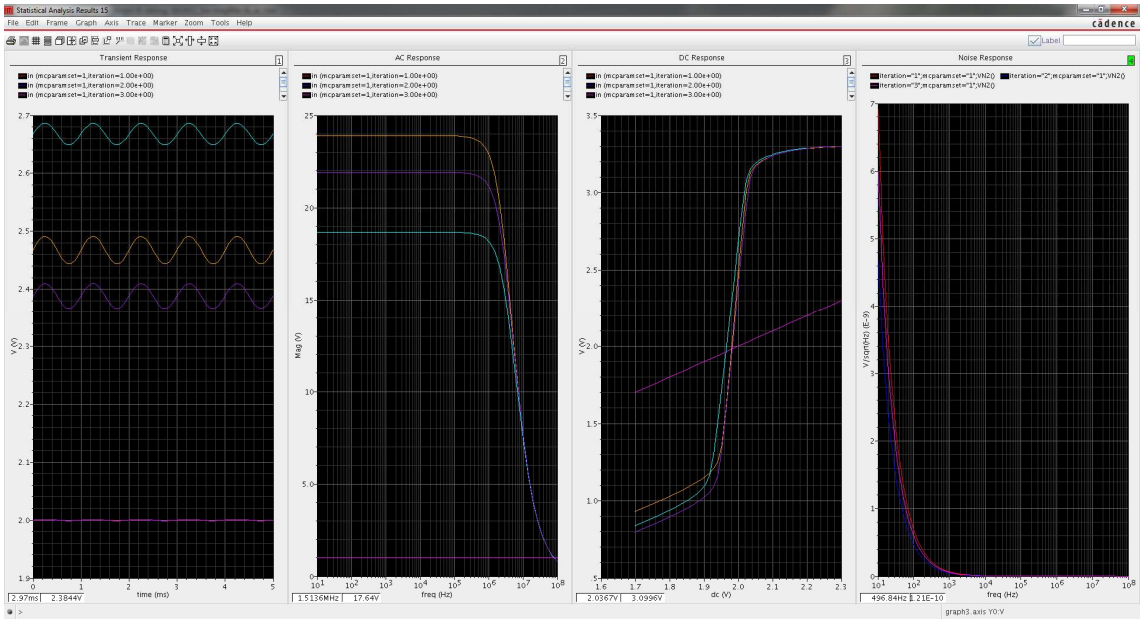


Fig. 13: Monte Carlo waveform window