

Ultra Low Power Circuits

Master Degree (M.Sc.) in Electrical and Computer Engineering

5th year, 1st Quarter 2022-2023

#1 Circuits Report (1 week -October 7, with report)

Goals: Get the feeling for Currents and Voltages values in sub-threshold and in strong inversion.

To Do:

- 1) NMOS transistor simulation: $W = \text{Group_number} \times 1\mu\text{m}$ / $L = 0.35\mu\text{m}$
 - a. $V_{DS} = 1.2\text{V}$, $0\text{V} < V_{GS} < 1.2\text{V}$
Plot I_D vs V_{GS} , with key points and comments
 - b. $V_{GS1} = 0.5\text{V}$; $V_{GS2} = 0.4\text{V}$; $V_{GS3} = 0.3\text{V}$; $0 < V_{DS} < 0.5\text{V}$
Plot I_D vs V_{DS} for 3 V_{GS} curves, with key points and comments.
- 2) Design a CMOS Inverter with $V_{th} = V_{DD}/2 \sim 0.6\text{V}$
 - a. $V_{DD} = 1.2\text{V}$, $0\text{V} < V_{GS} < 1.2\text{V}$
 - i. Plot V_o vs V_i
 - ii. Plot I_D vs V_{GS} , with comments
 - b. $0\text{V} < V_{DD} < 1\text{V}$, $0\text{V} < V_i < V_{DD}$
 - i. Plot V_o vs V_i , with comments

Report:

1 page with Identification and plots; 1 page with relevant comments

#2/#3 Analog Report (2 weeks -October 21, with report)

Goals: Design of a Low-gm Amplifier.

To Do:

Consider $V_{DD}=1V$ and a current source of $2\mu A$.

- 1) Design a transconductance amplifier (Fig.1) with $i_o/v_d < 10\mu S$. Consider schematic changes in the current mirrors with the circuit in Fig.2. Consider using the transistors in the differential pair in weak inversion.
- 2) Estimate the operation zone of the transistors.
- 3) Obtain the gain and output resistance of the amplifier.

Report:

4 pages with Identification, dimensioning, plots; and relevant comments.

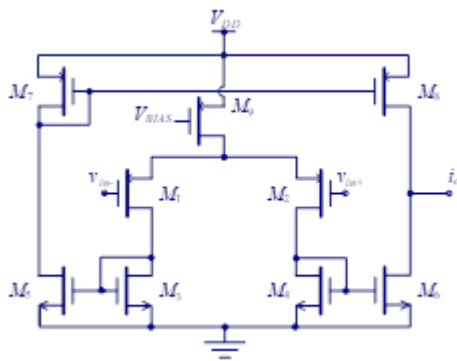


Fig. 1 Amplifier schematic

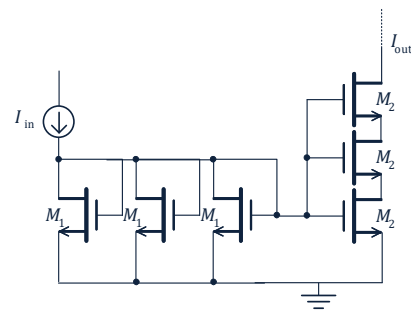
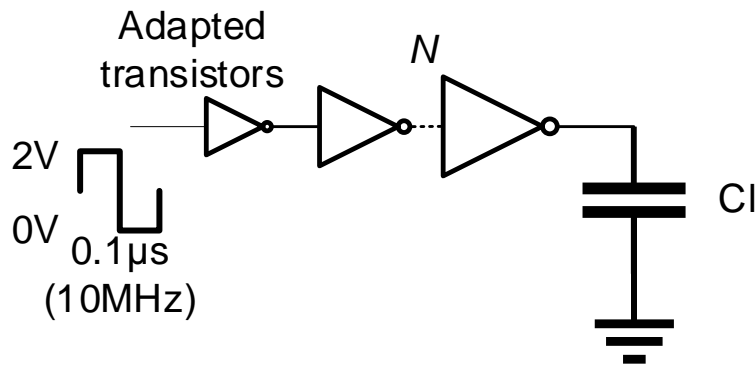


Fig.2 Current mirror scaling

#4 Digital Report (2 weeks -November 4, with report)

Goals: Design of a digital output driver.

To Do: Design an output driver employing CMOS inverters.



Constraints:

Output capacitance $C_l=10\text{pF}$

Supply voltage 2V

Frequency 10MHz

Design space:

Number of stages N

Inverter structure First inverter: NMOS minimum dimensions; PMOS adapted.

All other inverters free.

Transistor dimensioning

Goals:

Minimize power consumption

Minimize Area

Report (5 pages):

2 pages with Identification, figures and plots; 3 pages with relevant comments.