Ultra Low Power Circuits

Lab #1 - Circuits Report

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Bologna Master Degree in Electrical and Computer Engineering (MEEC)

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1) nMOS transistor

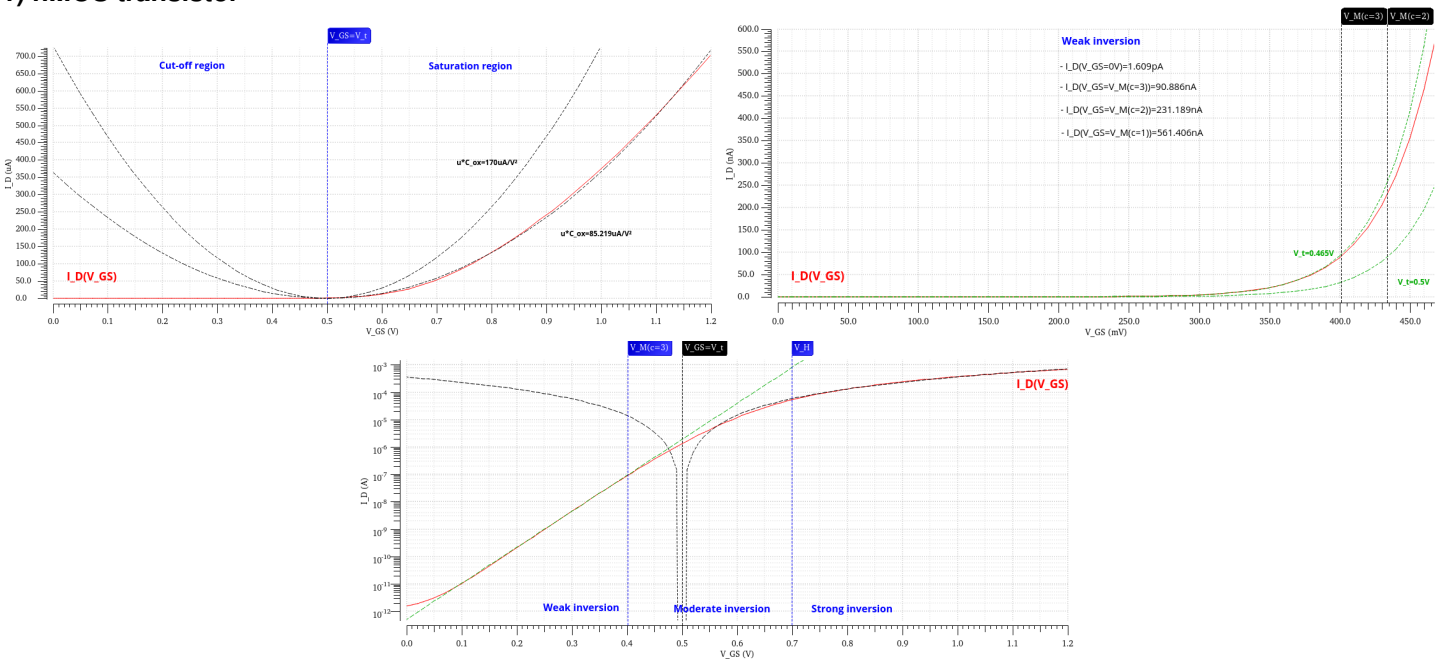

Figure 1: Curves $I_D(V_{GS})$ obtained for an nMOS transistor with $W = 12\mu m$ and $L = 0.35\mu m$, using voltage values $V_{DS} = 1.2V$ and $0V < V_{GS} < 1.2V$. On the left, the two regions of the simpler MOS transistor model are indicated - the separation occurs at $V_{GS} = V_t = 0.5V$. The dashed lines correspond to curves given by equation 1, for two different values of $\mu_n C_{ox}$. On the right, the weak inversion region is shown for voltage values $V_{GS} \leq V_M(c = 1) = 0.467V$. The dashed lines correspond to curves given by equation 2, for two different values of V_t (having $\mu_n C_{ox} = 85.219\mu A/V^2$ been considered). On the bottom, the plot is shown for all values of V_{GS} and using a logarithmic scale for the vertical axis, thus the three regions of the advanced MOS transistor model are distinguishable. The black and green dashed lines are the same as before, having only the values $\mu_n C_{ox} = 85.219\mu A/V^2$ and $V_t = 0.465V$ been (respectively) considered in this case.

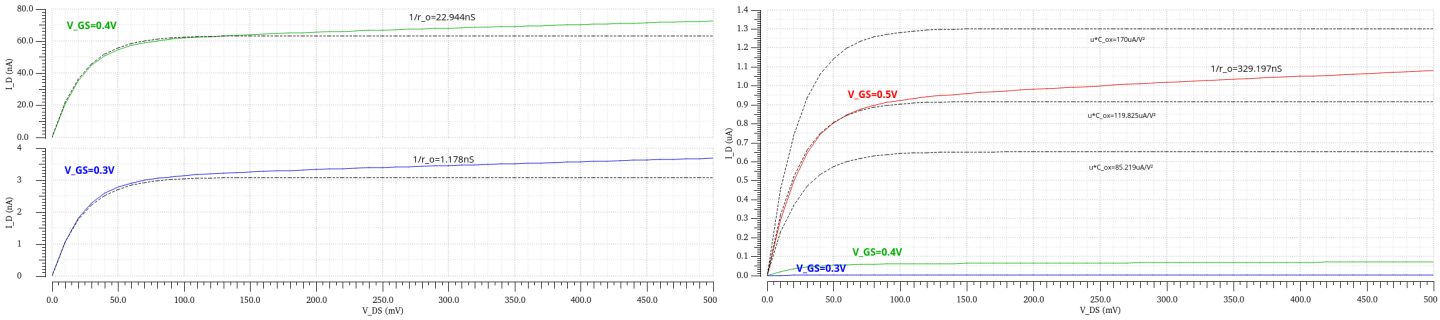

Figure 2: Curves $I_D(V_{DS})$ obtained for an nMOS transistor with $W = 12\mu m$ and $L = 0.35\mu m$, using voltage values $V_{GS} = 0.3, 0.4, 0.5\ (V)$ and $0V < V_{DS} < 0.5V$. The dashed lines correspond to curves given by equation 2, having $\mu_n C_{ox} = 170\mu A/V^2$ (value indicated in the datasheet) been used, except with $V_{GS} = 0.5V$ - in this case, three values of $\mu_n C_{ox}$ were considered. For each $I_D(V_{DS})$ curve, the slope $1/r_o$ (for $V_{GS} \in [200, 500]mV$) was calculated.

2) CMOS inverter

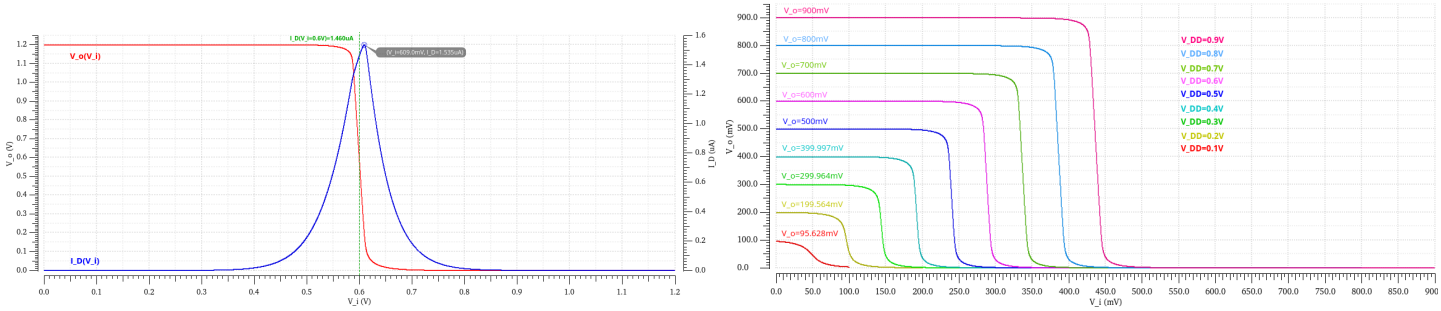

Figure 3: On the left, $V_o(V_i)$ and $I_D(V_i)$ curves (with $V_i = V_{GS}$) obtained for a CMOS inverter with $V_{th} = V_{DD}/2 = 0.6V$, having an nMOS transistor with $W = 1\mu m$ and $L = 0.35\mu m$ and a pMOS transistor with $W = k \times 1\mu m$ ($k = 106$) and $L = 0.35\mu m$ been used. The dashed line was made at $V_i = 0.6V$ and the coordinates (V_i, I_D) shown for the blue curve were obtained for the maximum I_D value. On the right, curves $V_o(V_i)$ obtained for the same CMOS inverter, but using different values of $0V < V_{DD} < 1V$ and with $0V < V_i < V_{DD}$ for each case. The voltage values V_o indicated above each curve were measured at $V_i = 0V$.

1) nMOS transistor

a. In order to obtain the desired curves, an instance `nmos4` from the library PRIMLIB was used. By connecting voltage sources `vdc` (from analogLib) to the drain and gate of the nMOS transistor, the voltages V_{GS} and V_{DS} (V_G and V_D, respectively, since the source is connected to ground) could be controlled. Initially, by using a fixed V_{DS}, a parabolic behaviour is apparent in the $I_D(V_{GS})$ curve starting at $V_{GS} \approx V_t = 0.5V$ (threshold voltage value given in the datasheet for a short channel nMOS transistor) - this corresponds to the **saturation region** (in which I_D increases up until $\approx 700\mu A$). Since $V_{GS} < V_{DS} + V_t = 1.7V$, the triode region is not reached. On the other hand, for $V_{GS} < V_t$, the current seems to remain approximately at $0V$ - this corresponds to the **cut-off region** in the simpler MOS transistor model. In order to test this model, the equation $\boldsymbol{I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_t)^2}$ (1) for the drain current in the saturation region was initially plotted with $\mu_n C_{ox} \equiv KPN = 170\mu A/V^2$ (value given in the datasheet). However, in Figure 1 it is clear that there was a considerable misalignment with the experimental data. Therefore, with some values of the curve in the saturation region, a fit was performed with equation 1, using Fitteia - a web-based fitting platform and trademark of Instituto Superior Técnico-, from which $\mu_n C_{ox} = 85.219\mu A/V^2$ was obtained - this new curve had a much better correspondence with the experimental values. The process parameter KPN (in the datasheet) was determined for "large transistors" and, in particular, in the linear region; this value could have a very large variability, depending on the dimensions of the transistor and the values of V_{DS} being considered, thus the considerable disparity observed. By using a more advanced MOS transistor model, the curve can be divided into three different regions (**weak**, **moderate** and **strong** inversion). Since $V_S = 0V$, the drain current in the weak inversion region can be given by $\boldsymbol{I_D = \mu_n C_{ox} (n-1) V_T^2 \frac{W}{L} e^{(V_G - V_t)/(nV_T)} \left(1 - e^{-V_D/V_T}\right)}$ (2), where $V_T = \frac{kT}{q} \approx 23.633mV$ (at $T = 27^oC$) is the thermal voltage. By plotting this equation in the graph shown in Figure 1 (on the right), a considerable similarity was observed up until $V_{GS} = V_M = V_t - c \cdot nV_T$ (with $c = 1, 2, 3$ and considering $n = 1.4$) - particularly until $V_M(c = 3)$; from $V_M(c = 3)$ to $V_M(c = 1)$, the value of I_D increases by one order of magnitude. However, a small correction had to be done to the value of the threshold voltage V_t to obtain a better correspondence with the experimental data; all technology parameters are characterized statistically, by normal distributions, thus, in practical applications, small variations from the average values are to be expected. In fact, according to the datasheet, the threshold voltage should vary between $V_t = 0.4V$ and $V_t = 0.6V$; the value $V_t = 0.465V$ is therefore acceptable to use for this transistor model. The bottom graph in Figure 1 includes both of the previously mentioned fits and the boundaries between the three regions (at $V_M(c = 3) = 0.401V$ and $V_H = V_t + 6nV_T = 0.699V$) are clear.

b. Using the same nMOS transistor, the $I_D(V_{DS})$ curves were obtained for different values of V_{GS}; in all cases, $V_{GS} \leq V_t = 0.5V$, thus equation 2 (for the weak inversion region) should be used instead of equation 1; the relation $V_{DS} > V_{GS} - V_t$ is always verified, but $V_{GS} > V_t$ is not, thus the saturation region is not reached. With the voltage values $V_{GS} = 0.3, 0.4\ (V)$, there is a very satisfactory correspondence between the dashed lines and the curves (as shown in Figure 2), especially for **smaller values** of $\boldsymbol{V_{DS}}$; in fact, $\mu_n C_{ox} = 170\mu A/V^2$ had to be used to obtain this similarity (as mentioned before, KPN shown in the datasheet was calculated using a linear regime and small values of V_{DS}). However, as V_{DS} increases, the disparity becomes more significant - this could be due to channel-length modulation. For the red curve, none of the previously mentioned $\mu_n C_{ox}$ values was appropriate - by using Fitteia, the best fit for $V_{DS} \in [0, 100]nA$ led to a new parameter "$\mu_n C_{ox}$" $= 119.825\mu A/V^2$. However, since $V_{GS} = 0.5V > V_M(c = 1) = 0.467V$, it was to be expected that the model described by equation 2 would not fit the experimental data as effectively for this curve - as seen before, in Figure 1, $V_{GS} = 0.5V$ corresponds to the moderate inversion region, in which equation 2 differs more from the experimental data. This might also be a consequence of the high variability of $\mu_n C_{ox}$ and of the (noticeable) effect of channel-length modulation (leading to a seemingly linear increase in I_D for higher values of V_{DS}). In fact, using Fitteia, linear fits were performed for $V_{DS} \in [200, 500]mV$, having the slopes $1/r_o$ been obtained for each case. As shown in Figure 2, this slope increases as V_{GS} increases (as do the current I_D values), specifically by one order of magnitude from one curve to another - whereas the respective current values increase by two orders of magnitude.

2) CMOS inverter

a. In order to simulate the CMOS inverter, the instances `pmos4` and `nmos4` (from PRIMLIB) were used, having both drains been connected. Since the mobility of electrons is higher than the mobility of holes ($\mu_n > \mu_p$, usually by a factor between 2 and 4), the pMOS transistor must have a higher W/L ratio. Taking equation 1 into account, in order for both transistors to have the same current in saturation, while using the same $L = 0.35\mu m$, we must have $\frac{W_p}{W_n} = \frac{KPN}{KPP} \approx 2.931$ - where $KPN = \mu_n C_{ox} = 170\mu A/V^2$ and $KPP = \mu_p C_{ox} = 58\mu A/V^2$ are the values present in the datasheet, whereas W_n and W_p are the widths of the respective transistors (in this case, $W_n = 1\mu m$). **However**, the fact that the respective threshold voltages are $V_{t_n} = 0.50V$ and $V_{t_p} = 0.65V$ (respectively) leads to $V_{th} < 0.6V$ - since $V_{t_n} < V_{t_p}$, the input voltage $V_i = V_{GS}$ would not need to increase as much for the pMOS transistor to enter the cut-off region and for the nMOS transistor to leave it. Therefore, the ratio W_p/W_n needs to much higher than expected in order to have $V_{th} = 0.6V$; by simulating with different values of this ratio, it was concluded that $\boldsymbol{W_p/W_n = 106}$ led to $V_o(V_i = 0.6V) = 0.6V$, as desired. Taking this into account, the curves $V_o(V_i)$ and $I_D(V_i)$ shown in Figure 3 indicate that, for most $V_i < 0.6V$, $V_{SG} > V_t$ for the pMOS transistor (thus, it is ON), while the opposite happens for the nMOS (which is OFF), so the input signal '0' is turned into an output of '1' ($V_o = V_{DD}$). For higher $V_i (> 0.6V)$, the pMOS eventually turns OFF and the nMOS turns ON, thus the output signal is '0'. When V_i is very low or very high, only one of the transistors is ON, while the other can be considered an open circuit, thus I_D tends to zero. However, for values around $0.6V$, some current still flows through both transistors, thus I_D is larger and reaches its maximum value. It can be noticed that the peak current value occurs at $V_i = 0.609V > 0.6V$. This might simply be due to the fact that a certain step size must be selected in the simulation; therefore, in reality, the curve $I_D(V_i)$ should have a sharper peak which would occur at $V_i = 0.6V$ (as seen in Figure 3, there is a certain distortion around the maximum value).

b. Using the same configuration mentioned above, the circuit was simulated for different values of V_{DD}, with $0V < V_i < V_{DD}$. Once again, the voltage value $V_o = V_{DD}/2$ is reached at around $V_i = V_{DD}/2$, whilst $V_o(V_i = 0V) = V_{DD}$ for most cases. It is worth noting that an inverter characteristic is still obtained when the supply voltage V_{DD} is not even large enough to turn the transistors ON (that is, to have $V_{GS/SG} > V_t$) . The explanation can be found in sub-threshold operation, in which some current still flows and the output switches between low and high levels. As seen before, the current values in weak (and moderate) inversion are very small, but a small increase in V_i (which leads to even lower V_{SG} for the pMOS transistor) makes it so that the drain current in the nMOS transistor (which grows exponentially, as shown in equation 2) becomes much more significant than the current in the pMOS transistor (which decreases exponentially), thus the transition from '1' to '0' occurs - even for very low values of V_i (as seen in Figure 3). The very low value of the switching currents ensures a very slow operation but this might be acceptable for some applications (such as watches or pacemakers, for example); the low values of V_{DD} also lead to lower power consumption. At around $100mV$, however, a deterioration of the gate characteristic is more apparent, due to the very low voltages V_i involved. In fact, as seen in Figure 1, it could be seen that I_D decreases less than what is predicted by equation 2 for $V_{GS} < 0.1V$; therefore, when $0V < V_i < 100mV$, the difference between the currents of the nMOS and pMOS transistors as the transition occurs won't be as significant, thus compromising the operation of the inverter.