Ultra Low Power Circuits
(Circuitos de Ultra-Baixo Consumo)

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Masters in Electrical and Computer Engineering
5th Year, 1st Quarter
2022-2023

General Course Information.

1

Ultra Low Power Circuits

1. ULP Circuits

- 0.1 ULP Course Structure
  - General Information
- 1.1. Minimizing Energy Consumption
  - Motivation and Framework:
    - Computing; IoT; Battery operated; Medical and others.
- 1.2.& 1.3 MOS Transistor Operation
  - Revisions:
    - Working principle
    - Level 1 MOS transistor model
- 1.4 Advanced MOS Transistor Model
  - Weak inversion region
  - EKV Model
- 1.5 Bulk and SOI technologies
  - Planar (Conventional)
  - FinFET
  - GAAFET and MBCFET

2

Common Ground Assessment

- Transistors:
  - MOS ?
  - Bipolar ?
- Circuits:
  - Analog (basic stages, amplifiers, etc)?
  - Digital (CMOS inverters, ...)?
- Software:
  - Spice or equivalent?
  - Cadence or equivalent?

Course Prerequisites

Should have had at IST (or equivalents):

Circuit Analysis; Electronic Circuits; Electronic Systems.

A plus: Microelectronics and Analog and Mixed Integrated Circuits.

Basic understanding of electronics:

1) Circuit analysis techniques.
2) Active and passive devices; large and small signal models.
3) Elementary amplifier stages and electronics building blocks.
4) Integrated circuit technology.

Course Objectives

At the end students are expected to be able to:

1) Understand the context of ULP circuits operation in battery powered devices, low-power low frequency applications, and low duty-cycle applications
2) Be able to design analog and digital circuits operating with extremely low currents and voltages, with transistors operating in sub-threshold region, which involves scaling voltages below the device thresholds.

Course Program

1. ULP Circuits
   - 1.1. Minimizing Energy Consumption
   - 1.2. Weak inversion region
   - 1.3. EKV Model of the MOS transistor
   - 1.4 Bulk and SOI technologies

2. ULP Analog Circuit Design
   - 2.1. Current mirrors
   - 2.2. Amplifiers
   - 2.3. Voltage and Current references
   - 2.4 Oscillators
   - 2.5. Translinear circuits
   - 2.6. Energy harvesting

3. ULP Digital Circuit Design
   - 3.1. Power gating, isolation and level converters
   - 3.2. Clock gating
   - 3.3. Asynchronous circuits
   - 3.4. Retention memory
   - 3.5. Dynamic voltage and frequency scaling

4. ULP System Level Design
   - 4.1. Architecture level decisions
   - 4.2. Case Studies

Information

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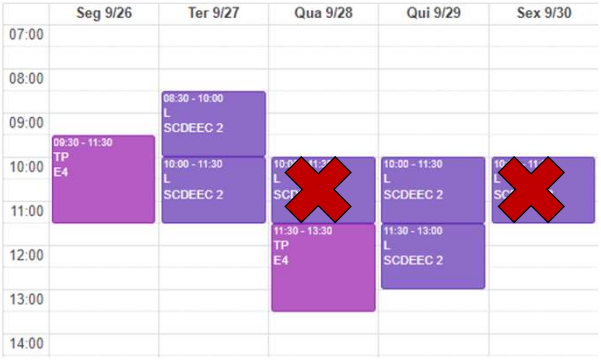
Note: Laboratory sessions are at the Microlab



(ALL STUDENTS SHOULD HAVE THE FENIX AFS SYSTEM ACTIVATED)
https://ciist.ist.utl.pt/ciistadmin/user/

Preliminary Schedule

- Course Assessment
  - 5 Weekly projects

Week		Theory	Lab	Milestones
1	19-Sep	1. ULP Circuits #3	Hands on tutorial: Cadence Design Environment	Common Ground
2	26-Sep			
3	3-Oct	2. ULP Analog Circuit Design #5 (Project: October 3rd; Holiday: October 5th)	Circuits	Circuits Report
4	10-Oct		Analog 1	Analog 1 Report
5	17-Oct		Analog 2	Analog 2 Report
6	24-Oct	3. ULP Digital Circuit Design #3	Analog/Digital	Analog/Digital Report
7	31-Oct	4. ULP System Level Design #1	Digital	Digital Report
8	7-Nov	Project Discussion		
9	14-Nov			

Bibliography

Principal Bibliography:

Sub-threshold Design for Ultra Low-Power Systems
Wang, Alice, Calhoun, Benton Highsmith, Chandrakasan, Anantha P.
Springer, ISBN: 978-0-387-33515-5
2006

Secondary Bibliography:

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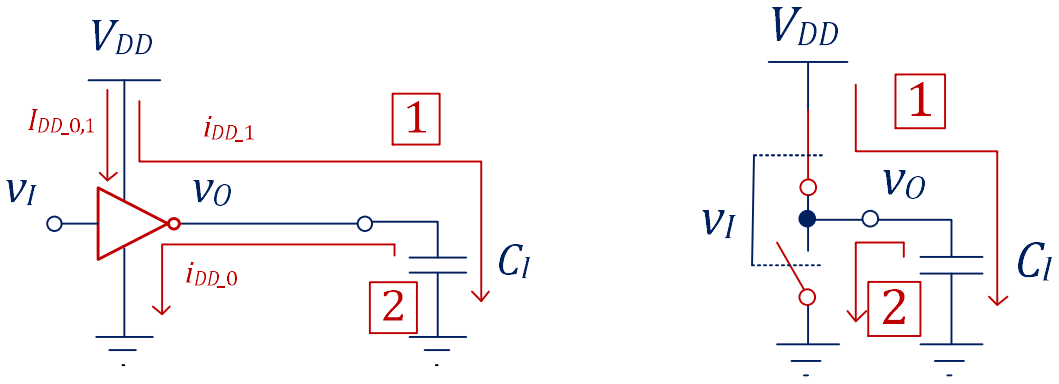
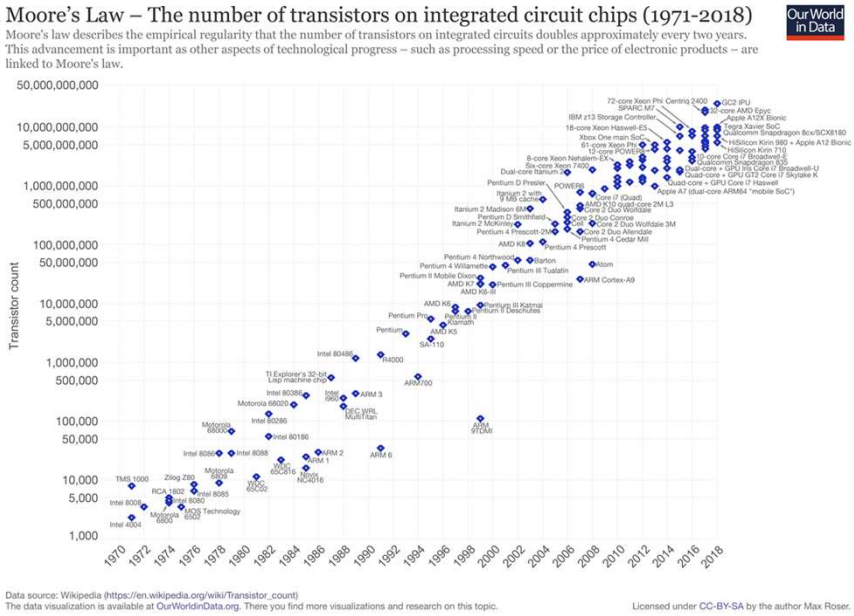
Digital Trend: CMOS Inverter Power Consumption



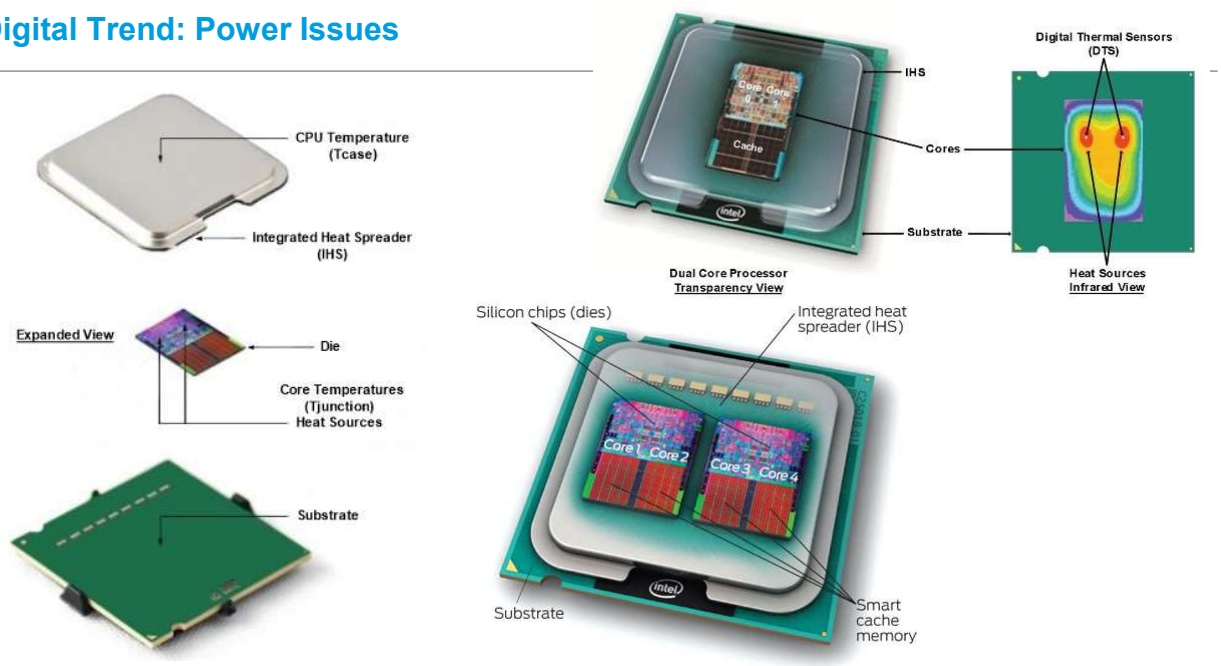
Static Power → $P_D \approx 0$

Dynamic Power → $\boxed{P = f\, C_l\, V_{DD}^2}$

Digital Trend: Processors

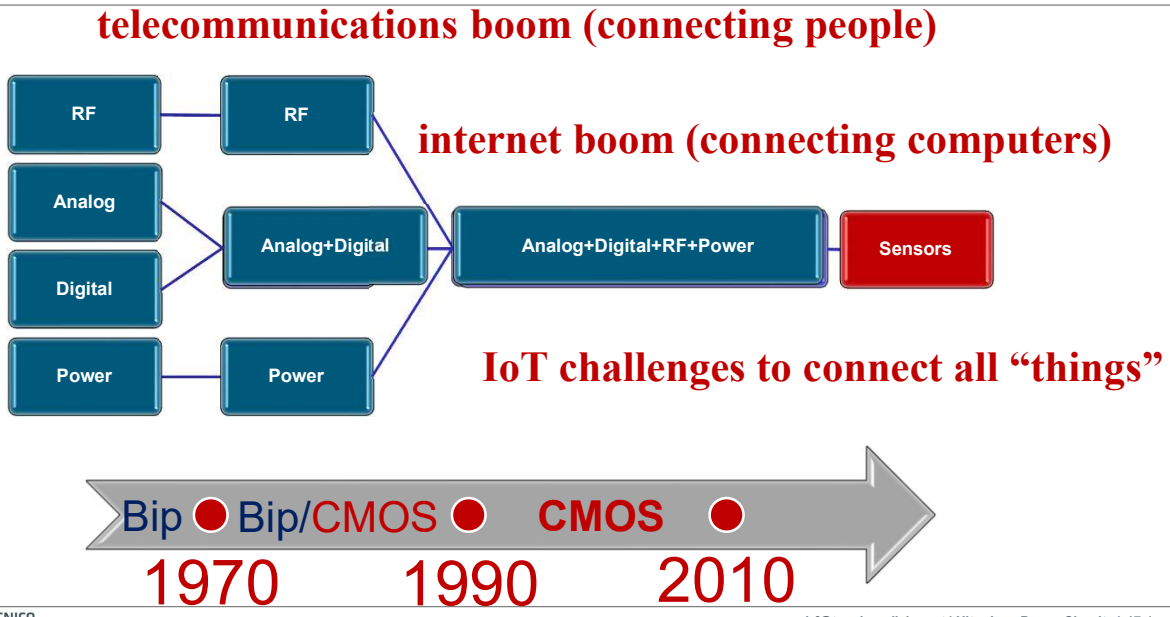


Digital Trend: Power Issues

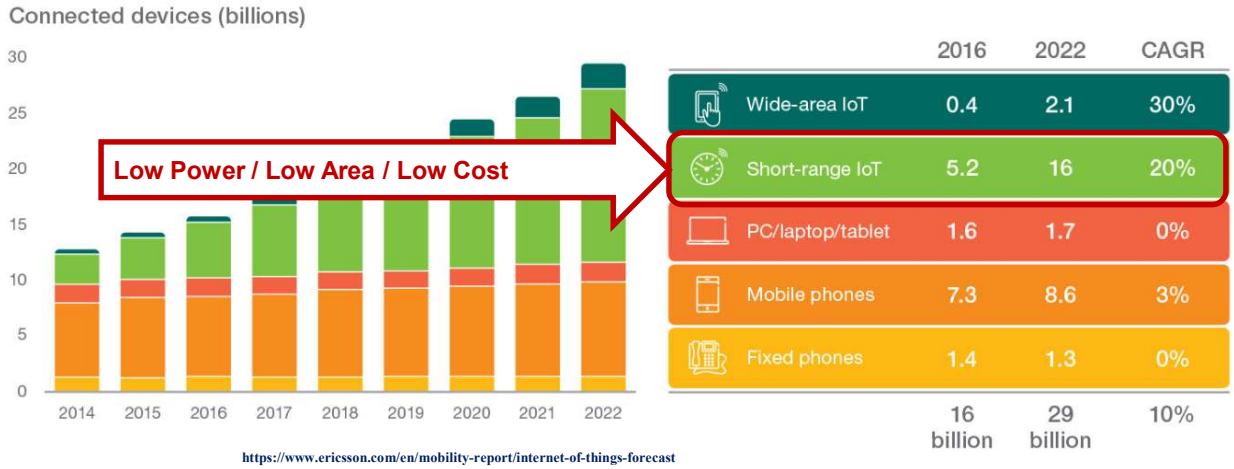


Application Trends: Data Centers

Application Trends: IoT



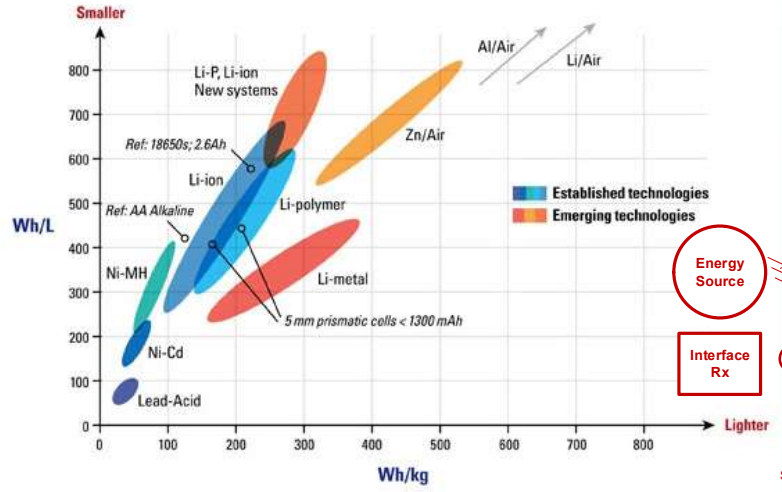
Application Trends: IoT



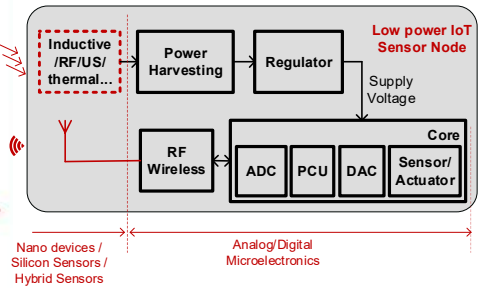
https://www.ericsson.com/en/mobility-report/internet-of-things-forecast

Application Trends: Portables

- https://www.altenergymag.com/article/2010/04/is-lithium-the-new-holy-grail-in-battery-development/662

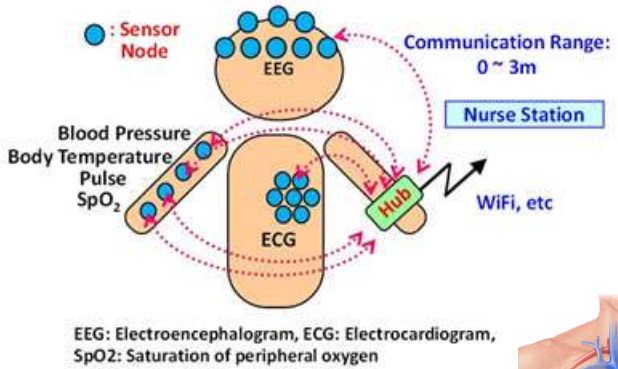


- Battery
  or/and
  Power Harvesting

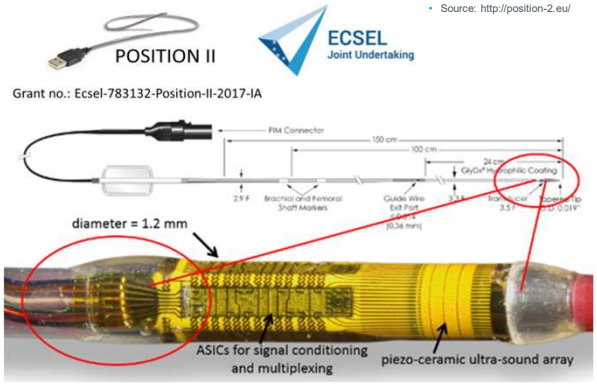


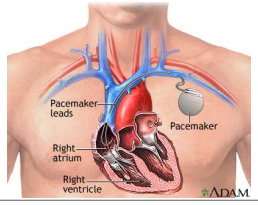
Application Fields: e.g. Medical

- Source: https://www.medicaldevice-network.com/news/newsfujitsu-laboratories-and-imec-holst-centre-develop-ultra-low-power-wireless-transceivers-4177738/



- Source: http://position-2.eu/



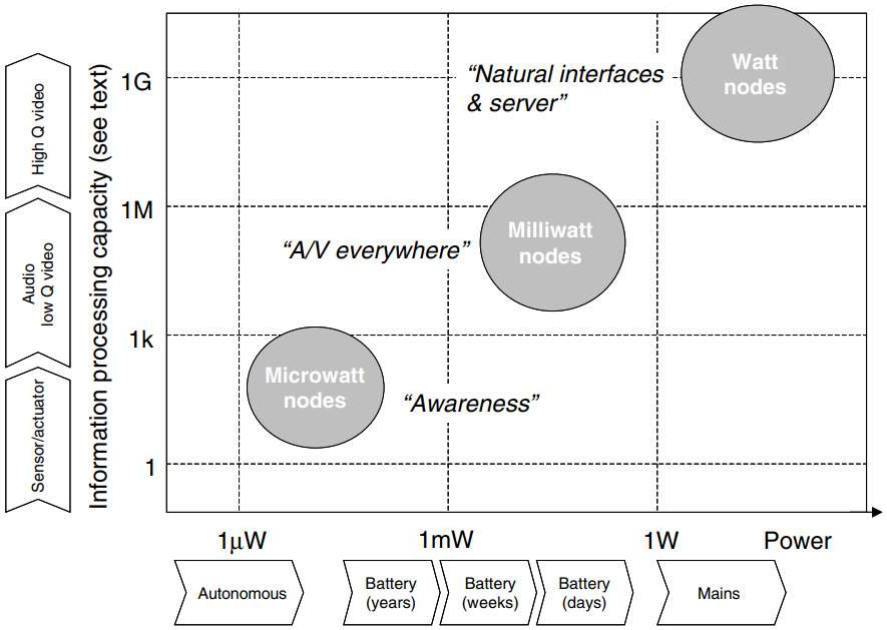


- Source: https://medlineplus.gov/ency/article/007369.htm

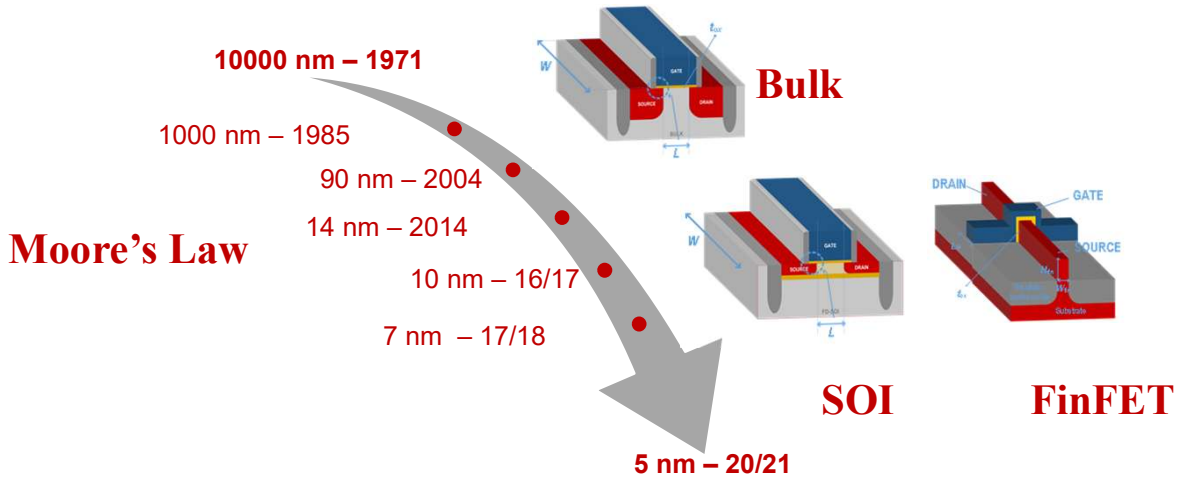
Applications

- Source: Ambient Intelligence Technology: An Overview" by F. Snijders

- All efficient applications are power concerned



Technology Evolution

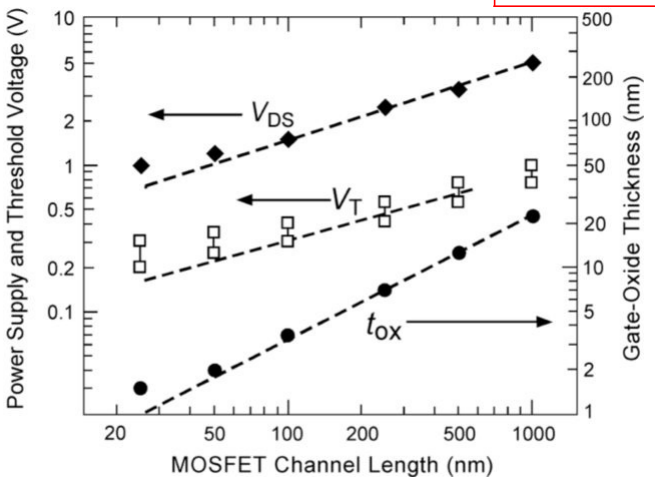


Technology Evolution

- CMOS

Static Power → $P_D \approx 0$

Dynamic Power → $P = f\, C_l\, V_{DD}^2$



$$i_D = \frac{1}{2}\mu_n \frac{\varepsilon_{ox}}{t_{ox}} \frac{W}{L}(v_{GS} - V_t)^2$$

- V_{DD} ↘↘↘↘
- V_t ↘↘
- t_{ox} ↘↘↘↘

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Terms and conventions

Large Signals: non-linear→distortion

Small Signals: ~linear

$$i_D = I_D + i_d$$
$$v_{GS} = V_{GS} + v_{gs}$$
$$v_{DS} = V_{DS} + v_{ds}$$

total or Instantaneous → $\boldsymbol{i_D = I_D + i_d}$ ← AC value or variable

DC value or constant

Linear System

If $x_1(t) \rightarrow y_1(t),\ x_2(t) \rightarrow y_2(t)$

then $a\,x_1(t) + b\,x_2(t) \rightarrow a\,y_1(t) + b\,y_2(t)$

Time Invariant System

If $x(t) \rightarrow y(t)$

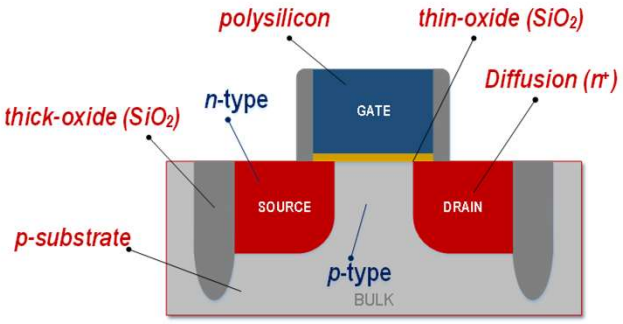
then $x(t\text{-}t_1) \rightarrow y(t - t_1)$

Memoryless System: if transient response does not depend on past values.

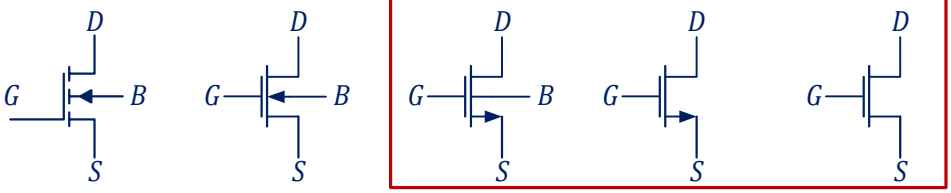
MOS Transistor

Structure:

- D-Drain
- G-Gate
- S-Source
- B-Substrate/Bulk/Body

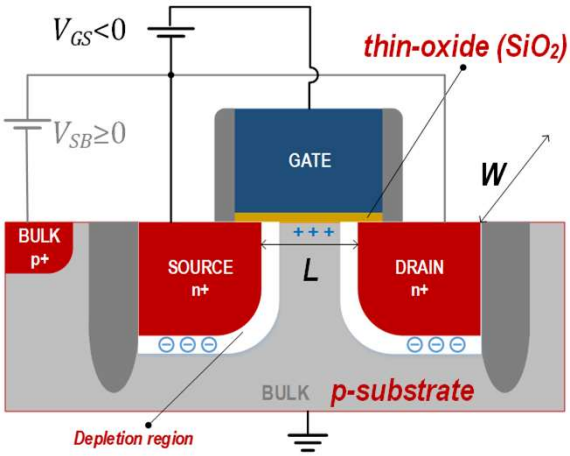


NMOS



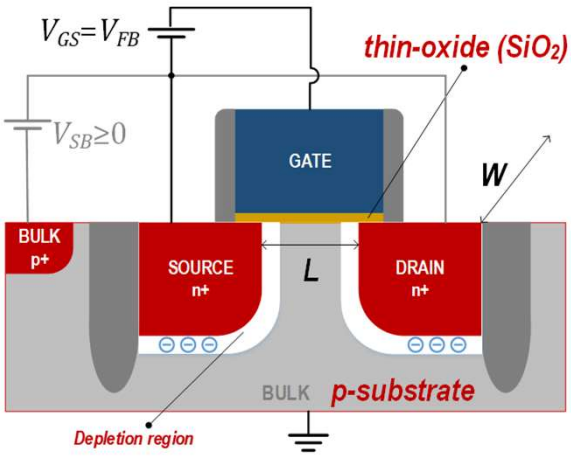
MOS Transistor DC Operation

- Accumulation



- Flat Band

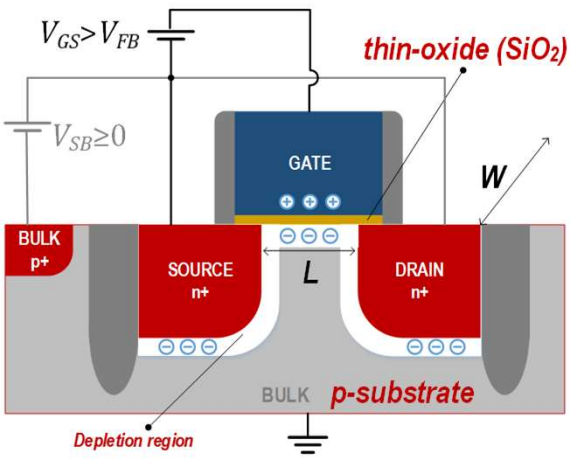
(Qualitative V_{GS} ↗↗ effect)



MOS Transistor DC Operation (V_{GS} effect)

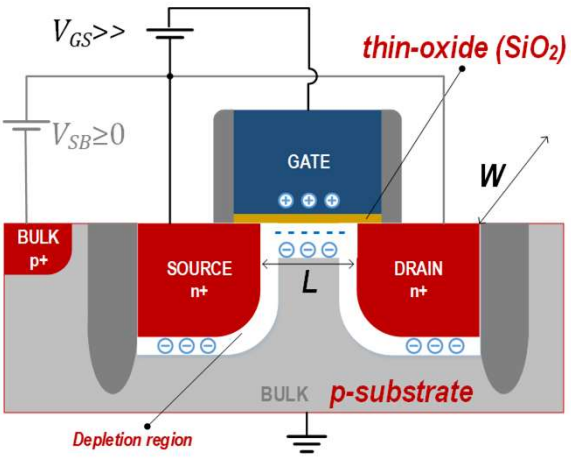
- Depletion

(Qualitative V_{GS} ↗↗ effect)



- Inversion

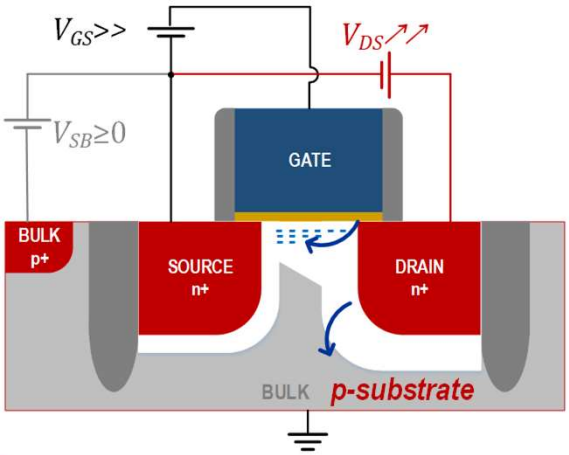
(Qualitative V_{GS} ↗↗ effect)



MOS Transistor DC Operation

- Inversion

(Qualitative V_{DS} ↗↗ effect)

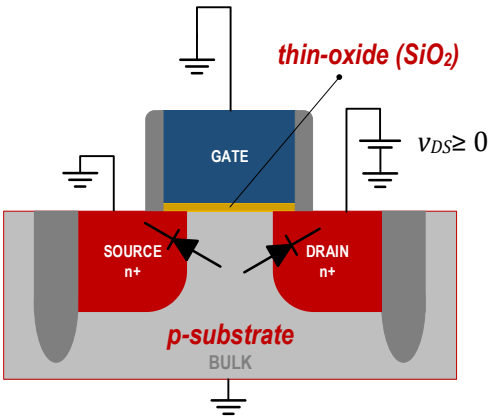


- Qualitative V_{DS} ↗↗ effect
  - Flat Band depletion: drain is more depleted
  - Weak Inversion (diffuse from S to D)
  - Moderate Inversion (more charge; diffusion+drift)
  - Strong Inversion (more charge mostly drift; pinch off)
- Qualitative V_{SB} ↗↗ effect
  - Depletion region larger
  - Higher V_t

(Level 1) MOS Transistor Model: Cut off region

- Enhancement mode NMOS:
- V_{GS}=0 ⇒ I_D=I_S =0 (two back-to-back *pn* juntions)
- I_G=0 isolated gate
- I_B=0 BD & BS
  inverted biased

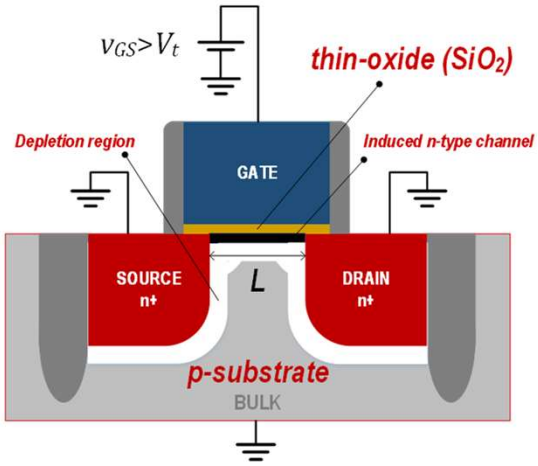
- $V_{GS} \leq V_t \Rightarrow I_D=I_S=0$



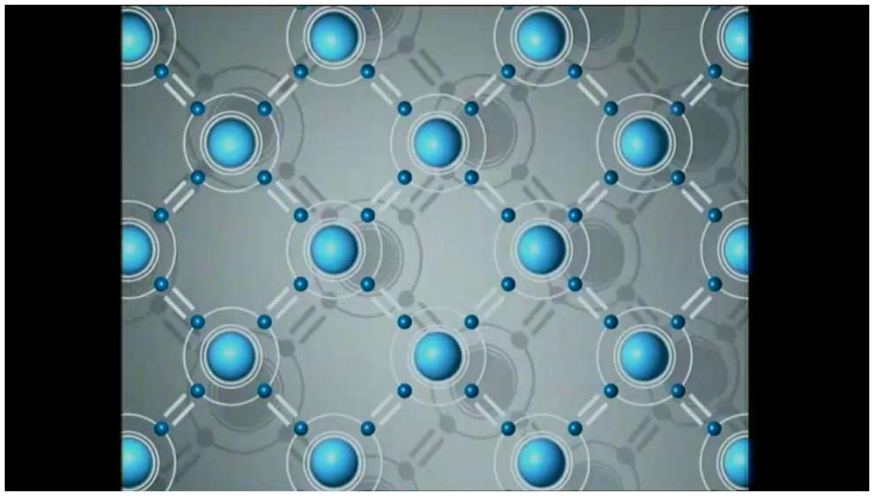
(Level 1) MOS Transistor Model: Triode and Saturation regions

- Positive Gate voltage: $V_G \nearrow$ depletion zone; $V_G \nearrow\nearrow$ induced channel
- I_G=0 isolated gate
- I_B=0 BD & BS
  inverted biased
- I_D=I_S (KCL)
  with V_{BS}=0

$$V_{GS} > V_t \Rightarrow I_D = I_S$$



Source: Infineon



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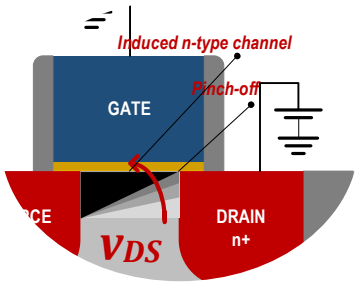


$$V_{GS} > V_t \Rightarrow I_D = I_S$$

(Level 1) MOS Transistor Model: Triode and Saturation regions

- Triode region: $0 < v_{DS} < v_{GS}\text{-}V_t$
- $i_D = k[2(v_{GS} - V_t)v_{DS} - v_{DS}^2]$

$$k = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}$$

- Small v_{DS}
  - $v_{DS} << v_{GS} - V_t$ → almost linear
  - $i_{DS} \approx k[2(v_{GS} - V_t)v_{DS}]$

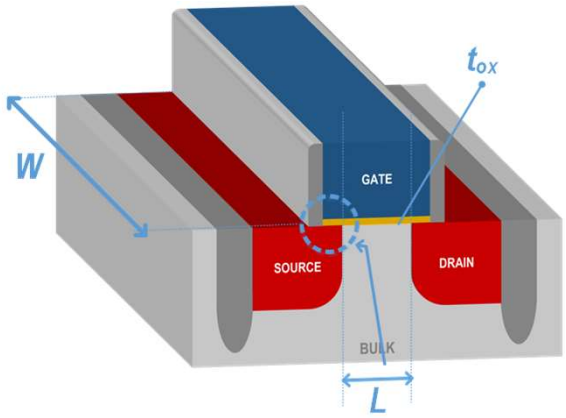
$$\rightarrow r_{ds} \approx \frac{1}{\mu_n C_{ox}\frac{W}{L}(v_{GS} - V_t)}$$

(Level 1) MOS Transistor Model: Triode and Saturation regions

$$k = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}$$

$\mu_n \rightarrow$ carrier mobility

$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \rightarrow$ unit area capacitance



$\varepsilon_{ox} = 3.97\varepsilon_0 \rightarrow SiO_2$ permitivity
$t_{ox} \rightarrow$ oxide thickness
$\varepsilon_{Si} = 11.7\varepsilon_0 \rightarrow$ Si permitivity
$\varepsilon_0 = 8.854 \times 10^{-14}[F/cm] \rightarrow$ free space permitivity

$W \rightarrow$ channel width $L \rightarrow$ channel length $\frac{W}{L} \rightarrow$ aspect ratio

(Level 1) MOS Transistor Model: Triode and Saturation regions

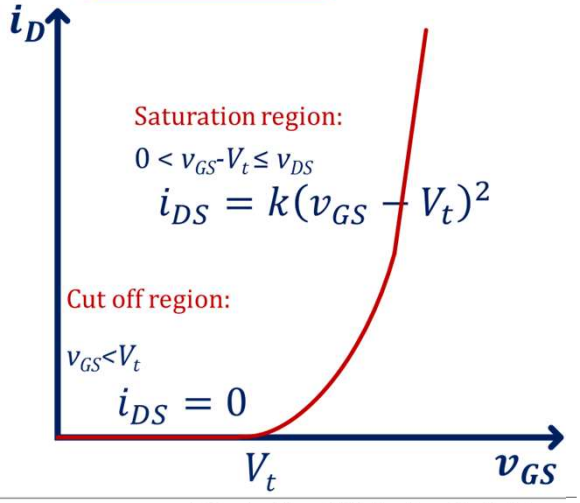
$$k = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}$$

- Triode region: $0 < v_{DS} < v_{GS}\text{-}V_t$
- $i_D = k[2(v_{GS} - V_t)v_{DS} - v_{DS}^2]$

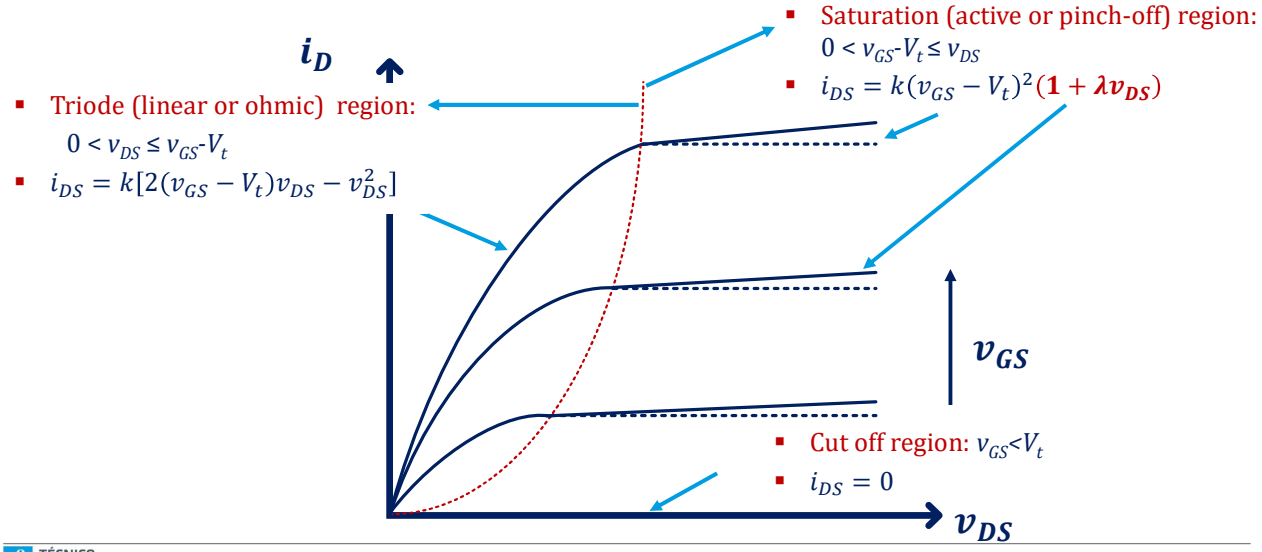
  - *Small v_{DS} → almost linear*

- Saturation region: $0 < v_{GS}\text{-}V_t < v_{DS}$
- $i_D = k(v_{GS} - V_t)^2$

  - *Current only depends on v_{GS}*



(Level 1) MOS Transistor Model: Triode and Saturation regions



(Level 1) MOS Transistor Model: Body Effect

- V_t increase with V_{SB} (NMOS) → degrades circuit performance
  - enlarges Depletion zone → smaller channel → V_t increase
- If V_{SB} =0 no body effect

- $V_t = V_{t0} + \gamma\left[\sqrt{2\phi_f + v_{SB}} - \sqrt{2\phi_f}\right]$

Digital: reduce noise margins
Analog: source of distortion

In advanced applications:
used as 2nd gate for speed;
used as a mixer terminal.

- Typical: $2\phi_f$ = 0.6V, $\gamma = 0.5V^{1/2}$

(Level 1) MOS Transistor Model NMOS Transistor equations

- Cutoff region: $v_{GS} < V_t$
- $i_{DS} = 0$

$$k = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}$$

- Triode region: $0 < v_{DS} < v_{GS}-V_t$
- $i_{DS} = k[2(v_{GS} - V_t)v_{DS} - v_{DS}^2]$

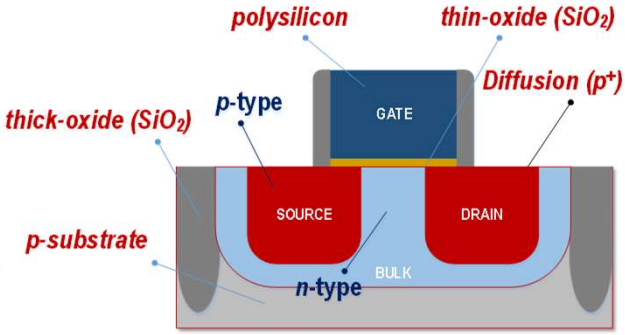
- Saturation region: $0 < v_{GS}-V_t < v_{DS}$
- $i_{DS} = k(v_{GS} - V_t)^2(1 + \lambda v_{DS})$

$$V_t = V_{t0} + \gamma\left[\sqrt{2\phi_f + v_{SB}} - \sqrt{2\phi_f}\right]$$

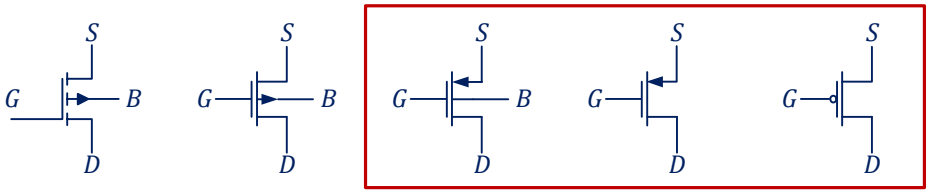
PMOS Transistor

Structure:

- D-Drain
- G-Gate
- S-Source
- B-Substrate/Bulk/Body



PMOS



PMOS Transistor equations

- Cutoff region: $v_{SG} < V_t$
- $i_D = 0$

- Triode region: $0 < v_{SD} < v_{SG} - V_t$
- $i_D = k[2(v_{SG} - V_t)v_{SD} - v_{SD}^2]$

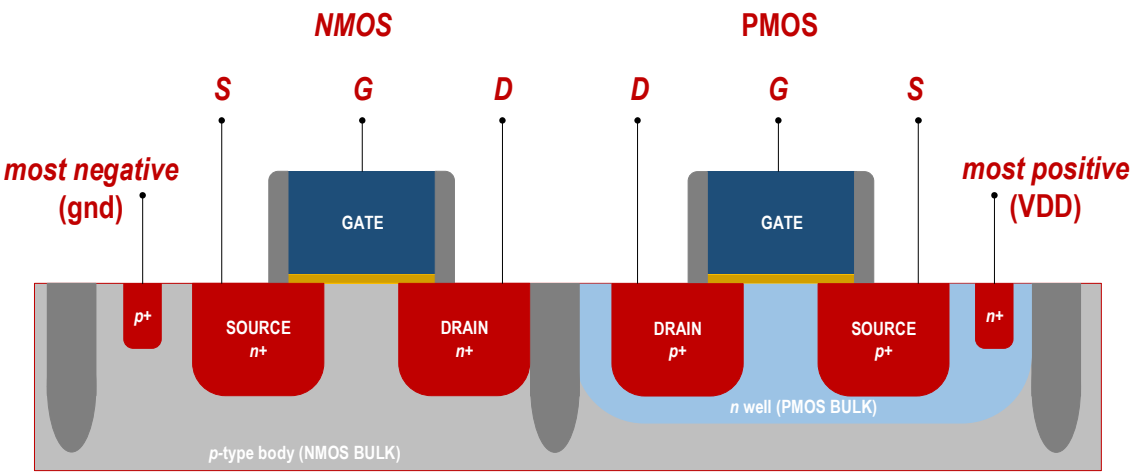
- Saturation region: $0 < v_{SG} - V_t < v_{SD}$
- $i_D = k(v_{SG} - V_t)^2(1 + \lambda v_{SD})$

Relative to NMOS:
electrons↔holes
n-well equivalent to substrate
change voltages and currents
V_{DD}↔gnd

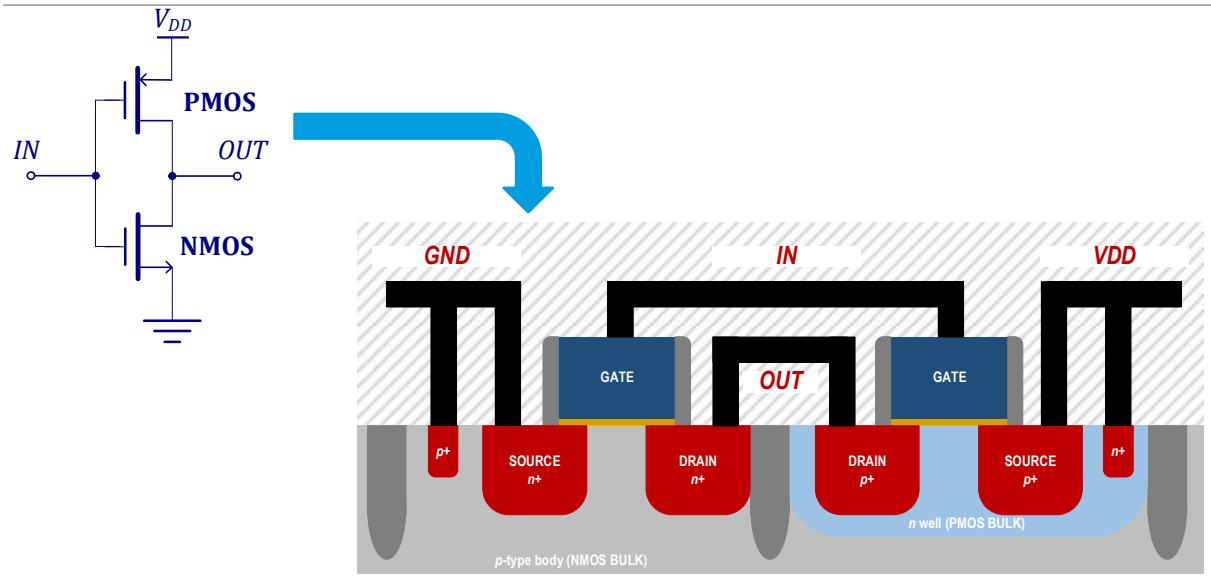
$$k = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}$$

$$V_t = V_{t0} + \gamma\left[\sqrt{2\phi_f + v_{BS}} - \sqrt{2\phi_f}\right]$$

CMOS →NMOS+PMOS



CMOS Inverter



Ultra Low Power Circuits

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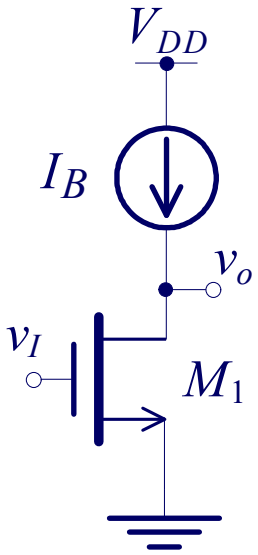
Advanced Models Single-Transistor MOS Gain



$$A_V = -g_m r_o = -\frac{2V_E L}{V_{GS} - V_t} = -\frac{2V_E L}{V_{OVD}}$$

Example:
$V_E L \approx 10V$
$V_{OVD} \approx 200mV$
$\rightarrow |A_V| \approx 100$

- High Gain: V_{OVD} ↓; L ↑
  …but this leads to low speed!

Advanced Models Large Signals: Weak-Strong Inversion

Strong inversion

$$i_D = \frac{\mu_n C_{ox}}{2n}\frac{W}{L}(v_{GS} - V_t)^2\,(1 + \lambda V_{DS}); \quad n = \frac{\gamma}{\sqrt{2\varphi_f + V_{BS}}}; \quad \lambda \approx \frac{1}{V_E L}$$

$$g_m = \frac{2I_D}{V_{GS} - V_t}$$

$V_t \rightarrow$ Threshold Voltage
$V_T = \frac{kT}{q} \rightarrow$ Thermal Voltage

Subthreshold or Weak inversion

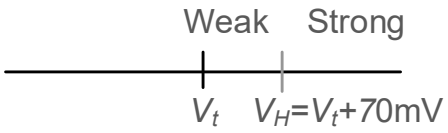
$$i_D = I_O \exp\left(\frac{v_{GS} - V_t}{n.V_T}\right); \quad n \approx 1.4\sim1.8$$

$$g_m = \frac{I_D}{n.V_T}$$

Boundary: $g_m = \frac{2I_D}{V_{GS} - V_t} = \frac{I_D}{n.V_T} \Rightarrow V_{GS} - V_t = 2n.V_T \Leftrightarrow V_{GS} \approx V_t + 70\text{mV}$

Advanced Models Large Signals: Weak-Strong Inversion

- Boundaries depend on models, technologies and authors:
- "Rules of thumb" for v_{GS}:



  - Conventional designs: near weak inversion but not in weak inversion: → V_{OVD} ≈150mV~200mV.

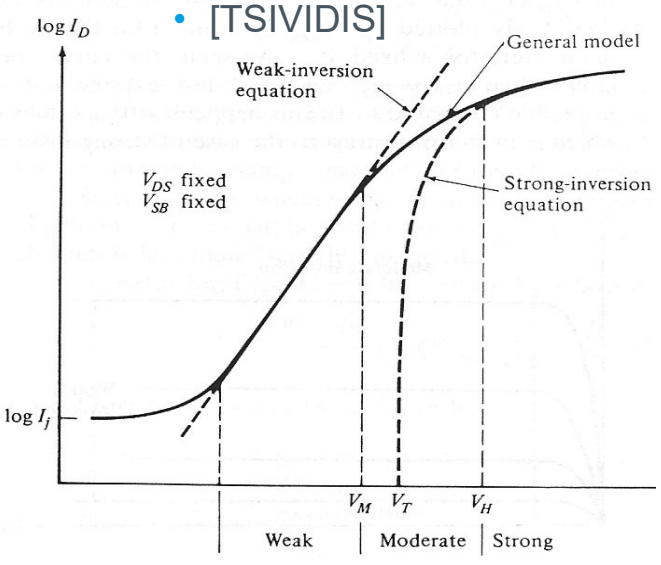
Advanced Models Large Signals: Weak-Moderate-Strong

$$i_D = I_{D0}\, e^{\frac{v_G}{n.V_T}} \left(e^{\frac{-v_S}{V_T}} - e^{\frac{-v_D}{V_T}} \right)$$

$$I_{D0} = \mu C_{OX}(n-1)V_T^2 \frac{W}{L} e^{\frac{V_t}{n.V_T}}$$

- I_{D0}: "leakage" (residual drain) current in saturation for V_G = V_S= 0; increases exponentially when V_t is reduced.

- [TSIVIDIS]



Advanced Models Large Signals: Weak Inversion

$$i_D = I_{D0}\, e^{\frac{v_G}{n.V_T}} \left(e^{\frac{-v_S}{V_T}} - e^{\frac{-v_D}{V_T}}\right)$$
$$I_{D0} = \mu C_{OX}(n-1)V_T^2 \frac{W}{L} e^{\frac{V_t}{n.V_T}}$$

$V_{GS} < V_M \qquad i_D = I_M\, e^{\frac{v_{GS}-V_M}{n.V_T}} \left(1 - e^{\frac{-v_{DS}}{V_T}}\right)$

$$g_m = \frac{I_D}{n.V_T}$$

$$\begin{cases} I_M = \mu C_{OX}(n-1)V_T^2 \dfrac{W}{L} \\ V_M = V_t - CnV_T \end{cases}$$

$$\begin{cases} V_t = V_{t0} + \gamma\left[\sqrt{|2\varphi_f + v_{SB}|} - \sqrt{|2\varphi_f|}\right] \\ n = \dfrac{\gamma}{\sqrt{|2\varphi_f + v_{SB}|}} \approx 1.4 \\ \gamma = \dfrac{\sqrt{2q\varepsilon_S N_B}}{C_{OX}} \approx \dfrac{2}{3} \approx 0.66 \\ C: 1 \to 3 \quad \Rightarrow V_M = V_t - 30mV \to V_t - 100mV \end{cases}$$

Advanced Models Large Signals: Strong Inversion

Strong inversion

$$i_D = \frac{\mu_n C_{ox}}{2n}\frac{W}{L}(v_{GS} - V_t)^2\,(1 + \lambda V_{DS}); \quad n = \frac{\gamma}{\sqrt{2\varphi_f + V_{BS}}}; \quad \lambda \approx \frac{1}{V_E L}$$

$$g_m = \frac{2I_D}{V_{GS} - V_t}$$

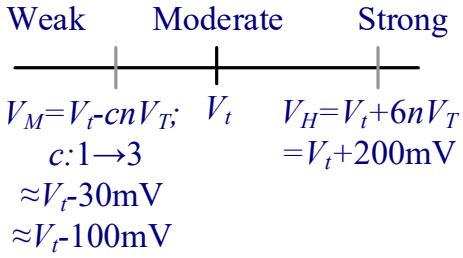
Subthreshold or Weak inversion

$$i_D = I_{DO} \exp\left(\frac{v_{GS} - V_t}{n.V_T}\right); \quad n \approx 1.4{\sim}1.8 \qquad g_m = \frac{I_D}{n.V_T}$$

Boundary: $g_m = \dfrac{2I_D}{V_{GS} - V_t} = \dfrac{I_D}{n.V_T} \Rightarrow V_{GS} - V_t = 2n.V_T \Leftrightarrow V_{GS} \approx V_t + 70\text{mV}$

Advanced Models Large Signals: Moderate Inversion

- "Rules of thumb" for v_{GS}:



- There are unified models.

  Cost in complexity which translates in computation time.
- There are non-physical based models, fitting on experimental data as BSIM3

Advanced Models Large Signals: …at the higher end

- At high v_{GS} current becomes more linear again;
  - Mainly due to velocity saturation
  - Increase in electric field does not cause electrons to travel through the channel faster due to colisions.

Velocity saturation

$$i_{DS_{VS}} = WC_{ox} \underbrace{V_{SAT}}_{\approx 10^7 \text{cm/s}} (v_{GS} - V_t)$$

$$g_{m\_SAT} = WC_{ox} \underbrace{V_{SAT}}_{\approx 10^7 \text{cm/s}} \text{ is absolute max}$$

does not depend on v_{GS}, is constant; not used for analog

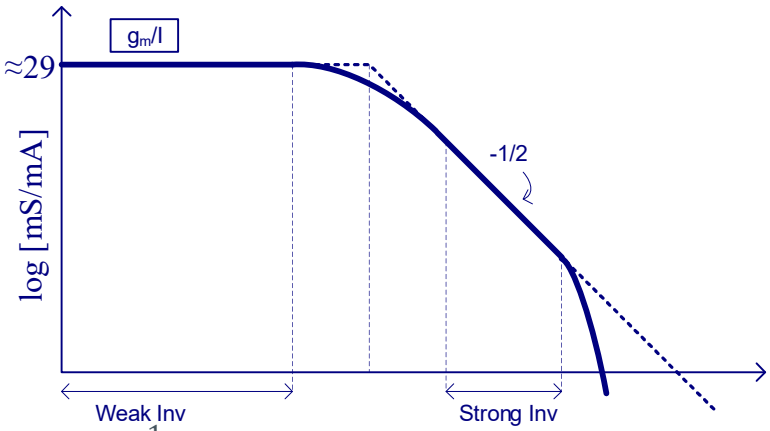
$$g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{v_{GS}=V_{GS}} \rightarrow$$

Strong Inversion: Saturation

$$g_m = \mu C_{OX}\frac{W}{L}\frac{1}{\alpha}(V_{GS}-V_t) = \frac{2I_D}{V_{GS}-V_t} = 2\sqrt{\frac{1}{2}\mu C_{OX}\frac{W}{L}\frac{1}{\alpha}I_D}$$

Strong Inversion: Triode $\quad g_m = \mu C_{OX}\frac{W}{L}V_{DS}$

Weak Inversion: $g_m = \frac{I_D}{nV_T}$



$g_m/I = \frac{1}{nV_T}$ $\quad\downarrow\quad$ $g_m/I \propto \sqrt{I_D}$

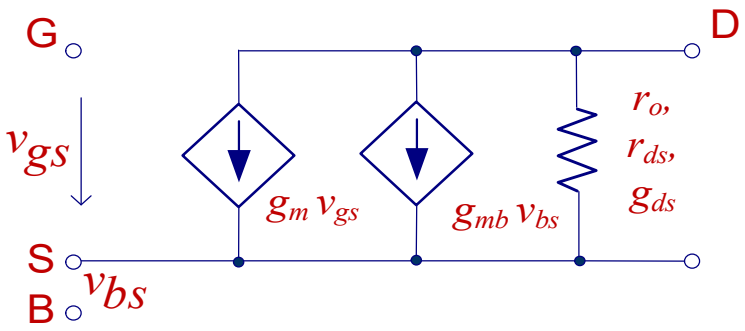
$$I_0 = \underbrace{2\mu C_{OX} n V_T^2}_{I_0'}\frac{W}{L} \rightarrow IC = \frac{I_{DS}}{I_0} \propto V_{GS}-V_t$$

Advanced models Small Signals: Bulk transconductance and D-S conductance

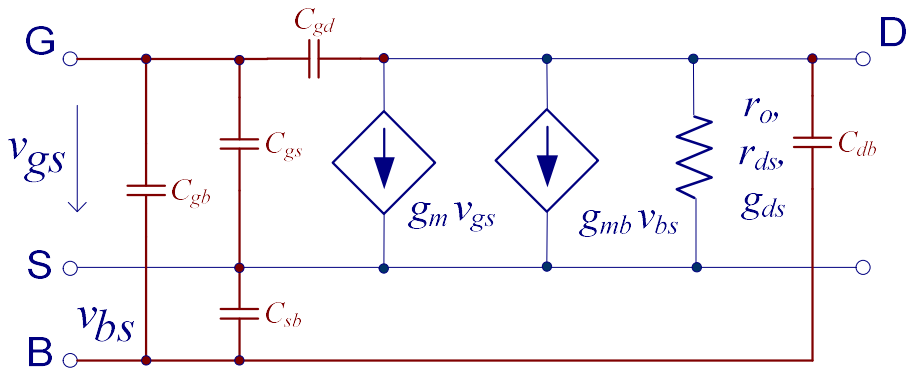
$$g_{mb} = \left.\frac{\partial i_D}{\partial v_{BS}}\right|_{V_{GS},V_{DS},V_{BS}} = \frac{\partial i_D}{\partial V_t} \cdot \frac{\partial V_t}{\partial v_{BS}} = g_m \cdot (n-1)$$

[g_{mb}= 0.1 to 0.3 g_m]

$$g_{ds} = \frac{\Delta i_D}{\Delta v_{DS}} \rightarrow \left.\frac{\partial i_D}{\partial v_{DS}}\right|_{v_{GS}=V_{GS};v_{DS}=V_i}$$



Advanced models Capacitance



Advanced models Capacitance (intrinsic)

Weak Inversion

$$C_{gb\_i} = \frac{n-1}{n} \cdot W \cdot L \cdot C_{OX}$$

Strong Inversion

triode (V_{DS}=0):

$$\begin{cases} C_{gs\_i} = C_{gd\_i} = \frac{1}{2} \cdot W \cdot L \cdot C_{OX} \\ C_{gb\_i} \approx 0 \\ C_{bs\_i} = C_{bd\_i} = \frac{\gamma}{2\sqrt{2\varphi_f - V_{SB}}} \cdot \frac{W \cdot L \cdot C_{OX}}{2} \end{cases}$$

saturation:

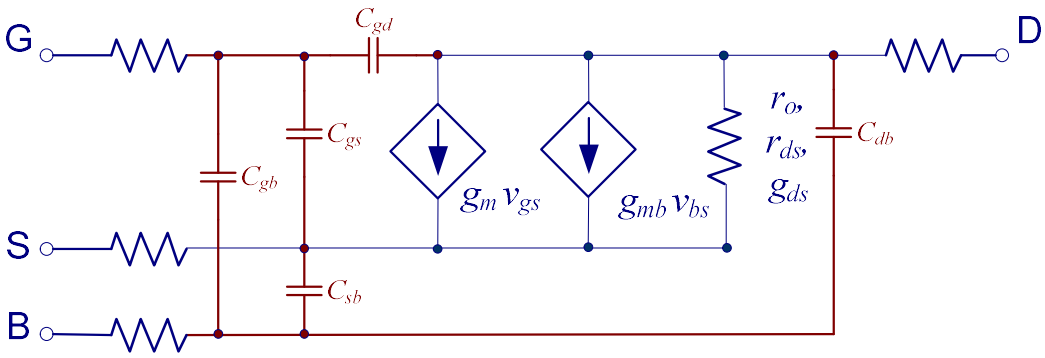
$$\begin{cases} C_{gs\_i} = \frac{2}{3} \cdot W \cdot L \cdot C_{OX} \\ C_{gd\_i} = 0 \\ C_{gb\_i} = \frac{\gamma}{2\sqrt{2\varphi_f - V_{SB} - V_{DS}}} \cdot \frac{W \cdot L \cdot C_{OX}}{3} \\ C_{bs\_i} = \frac{\gamma}{2\sqrt{2\varphi_f - V_{SB}}} \cdot \frac{W \cdot L \cdot C_{OX}}{2} \\ C_{bd\_i} = 0 \end{cases}$$

Advanced models Capacitance (extrinsic)

- Better to design finger transistors instead of a “big” transistor. Reduces the area of drain and source by two.

$$\begin{cases} C_{gs\_e} = C_{gd\_e} = W \cdot C_W \\ C_{gb\_e} = L \cdot C_L \\ C_{bs\_e} = C_{bd\_e} = \propto A_S + \propto P_S \end{cases}$$

Advanced models Capacitance



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Moore's Law

- 10 µm – 1971
- 6 µm – 1974
- 3 µm – 1977
- 1.5 µm – 1982
- 1 µm – 1985
- 800 nm – 1989
- 600 nm – 1994
- 350 nm – 1995
- 250 nm – 1997
- 180 nm – 1999

Increase process complexity

Increase leakage

- 130 nm – 2001
- 90 nm – 2004
- 65 nm – 2006
- 45 nm – 2008
- 32 nm – 2010
- 22 nm – 2012
- *14 nm – 2014*
- *10 nm – 2016-2017*
- *7 nm – 2017-2018*
- *5 nm – 2020-2021*

high-k/metal gate

SOI; FinFET

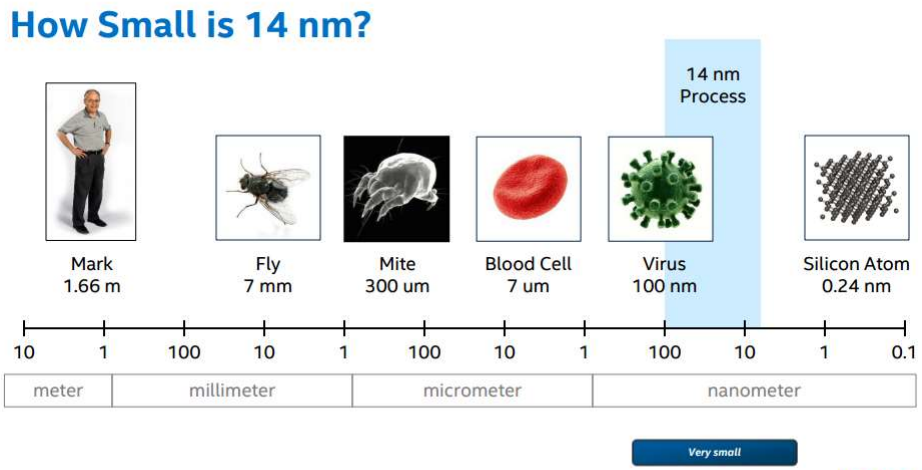
2018: 14nm
i7, 8th generation

Others…

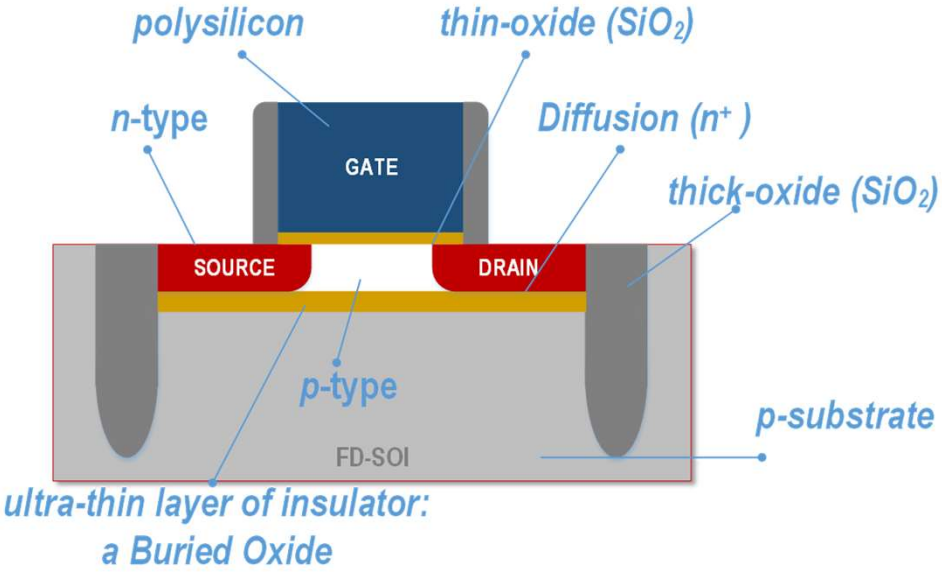
Moore's Law

- 1965: Moore's Law [Intel]

taken from http://www.intel.com/content/dam/www/public/us/en/documents/pdf/foundry/mark-bohr-2014-idf-presentation.pdf



SOI: Silicon-on-Insulator



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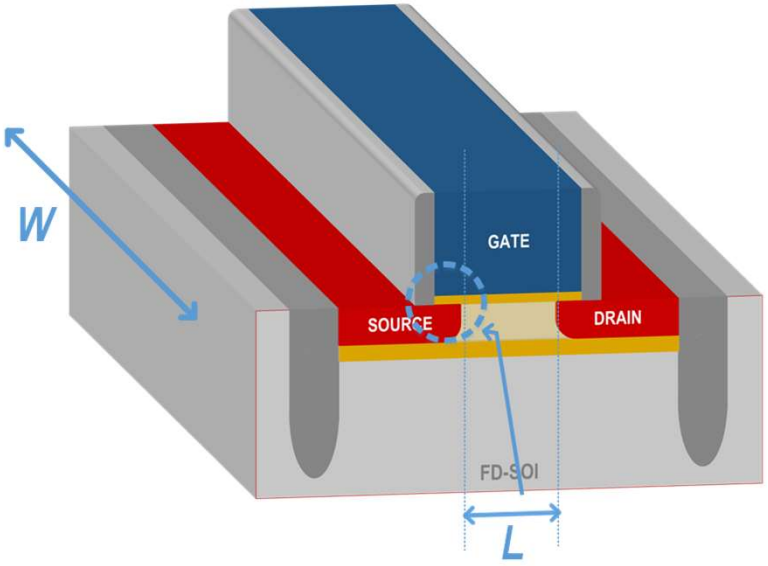
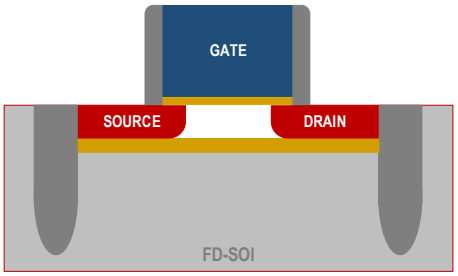


SOI: Silicon-on-Insulator

FD-SOI (Fully Depleted Silicon On Insulator)

- reduced geometries
- faster transistors
- lower power transistors
- maintains transistor geometry
- buried oxide layer
  - more gate control; better performance
  - two gate control “extreme” body biasing
  - no need for dopants: reduced mismatch
  - no leakage

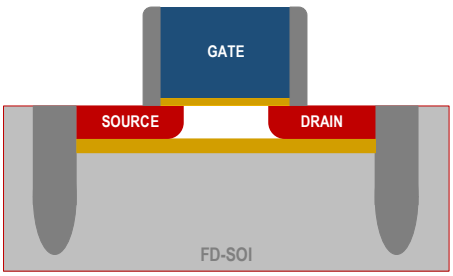


SOI: Silicon-on-Insulator

FD-SOI (Fully Depleted Silicon On Insulator)

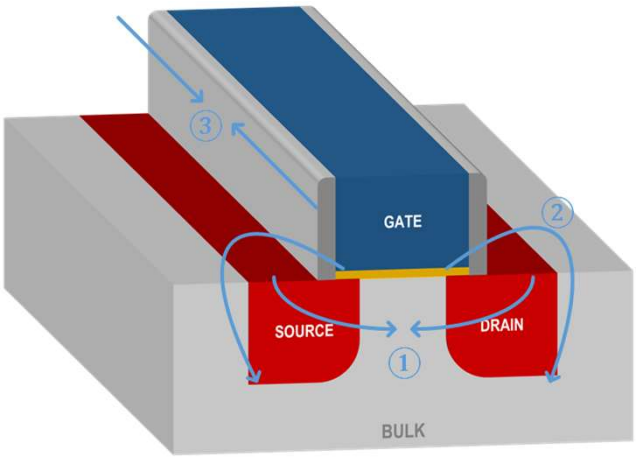
- simplified fabrication process

- Two gates: two different modes
  - gate V++ and backgate V+ → faster
  - gate V+ and backgate V++ → less power

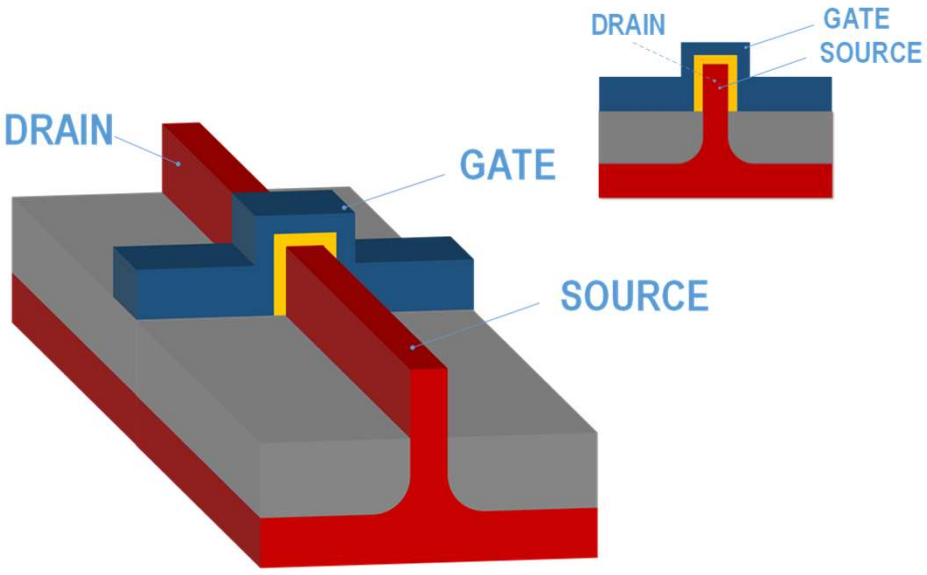


ST Microelectronics: An introduction to FD-SOI - YouTube

FinFET



FinFET



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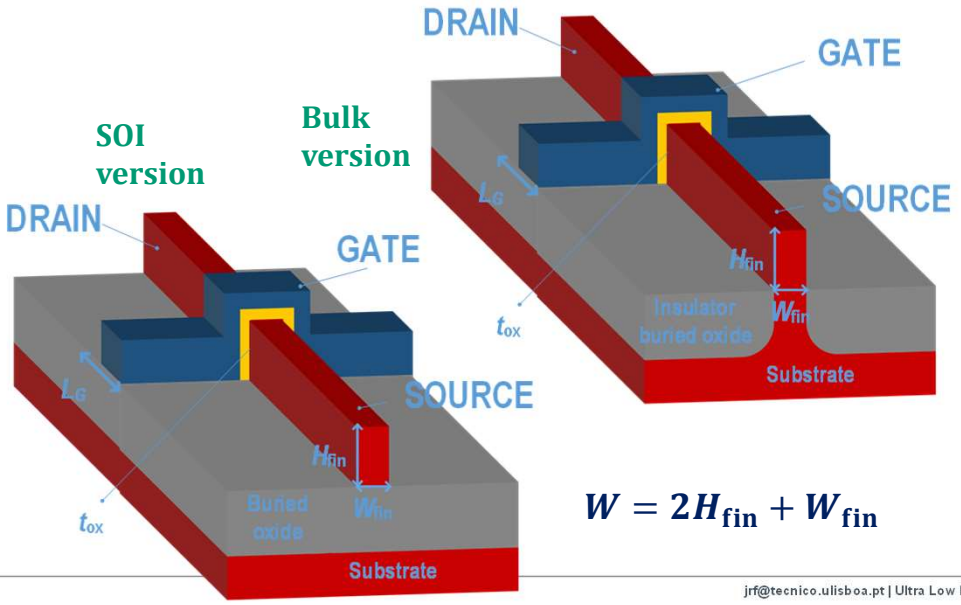
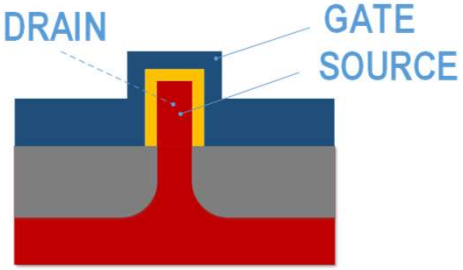


$$W = 2H_{\text{fin}} + W_{\text{fin}}$$

FinFET

- Tri-gate or double gate
- Fixed dimension steps
- One orientation
- 3D- complex parasitic capacitances
- down to 5nm (?)



Next….

- Samsung https://youtu.be/3otqUu-7WUQ