# Ultra Low Power Circuits

## Lab #2 - Analog Report

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Bologna Master Degree in Electrical and Computer Engineering (MEEC)

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### (A) Initial current mirror configuration

The **transconductance amplifier** shown in Figure 1 was initially designed. In this case, a simple current mirror configuration is included. The input pin `VDD` will be connected to the supply voltage and `VSS` to ground. From the output `OUT`, the response of this circuit will be obtained in different simulations. However, in all cases, a DC voltage component of $\mathbf{V_{out} = 401mV}$ is forced by using voltage sources. As seen in Lab 1, the separation between the weak and moderate inversion regions, in the $I_D(V_{GS})$ curves, was clearer at $V_M(c = 3) = V_t - c \cdot n \cdot V_T = 401mV$ for the nMOS transistor used in that report. Therefore, by maintaining this DC value in the output, it can be expected, with a reasonable degree of certainty, that the nMOS transistors M4 and M6 (which will have a different width $W$ from the transistor in Lab 1) should be working in the weak inversion region.

As for the pMOS transistors M1 and M2, the DC value of the input voltages $V_{in-}$ and $V_{in+}$ was also determined in order for these transistors to work in weak inversion. The dimensioning will be made in order to have $V_{net20} \lesssim V_{DD} = 1V$ in `net20` (shown in Figure 1). By using the same procedure as for the nMOS transistors, it should be defined that $V_{SG} = V_{DD} - V_{in-/in+} = V_M(c = 3) = 0.579V$ for the pMOS transistors (considering $V_T = 23.633mV$ - same as in Lab 1 - and $V_t = 0.65V$ - as shown in the datasheet). Therefore, the DC voltage in the inputs used in this report is $\mathbf{V_{in-} = V_{in+} = 421mV}$.

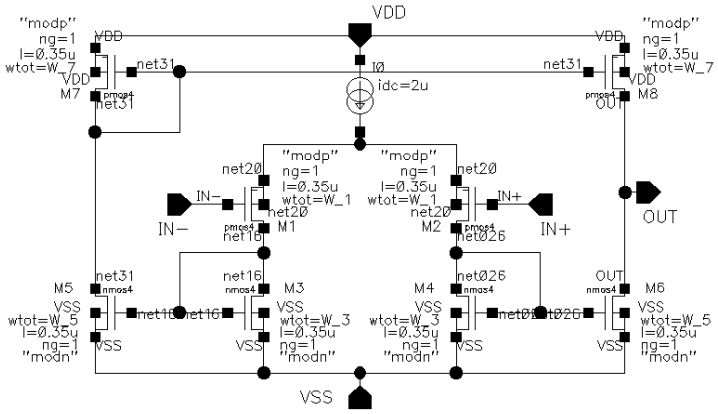


**Figure 1:** Schematic of the transconductance amplifier with a simple current mirror configuration, designed in Cadence Virtuoso. For all transistors, a width $W = 125\mu m$ was used in the simulations.

In this circuit, it is necessary to have a DC current of $\mathbf{2\mu A}$ connected to the differential pair. Firstly, the schematic shown in Figure 1 was simulated in order to obtain the voltage and current values in the DC operating point. For this purpose, the cellview shown in Figure 2 was used (in this case, `vdc` voltage sources were connected to the inputs and output).

A DC analysis was initially performed, in which the width $W$ of the transistors in the differential pair was swept. This was made in order to determine which $W$ led to $V_{net20} \lesssim V_{DD} = 1V$ and guaranteed that $I_D(M1) = I_D(M2) = 1\mu A$ in the DC operating point (current of $2\mu A$ equally divided through both branches of the differential pair). Thanks to this procedure, the width $\mathbf{W = 125\mu m}$ was selected and will be used for all analyses shown in this report. Moreover, all the transistors have the same width, which can be beneficial in circuit fabrication (since it should be easier to fabricate many transistors when the size does not vary among them). Additionally, all transistors have a channel length of $L = 0.35\mu m$. The results of this DC analysis are shown further ahead, in Table 1.

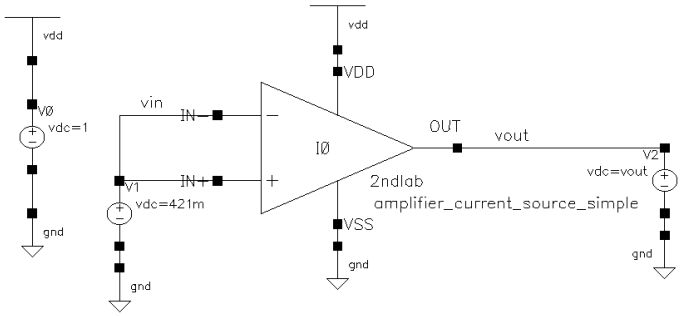


**Figure 2:** View used for DC analysis with the transconductance amplifier shown in Figure 1. In the simulations, a voltage value `vout=401mV` was selected. Very similar views were used with other amplifier configurations (indicated in Figure 5).

Having obtained the voltage and current values in the DC operating point, the cellview shown in Figure 3 was used to run an AC analysis with a frequency sweep. For this purpose, an instance `vsin` with a DC voltage of $V_{in-} = 421mV$ and an AC component of $v_{in-} = 1V$ was connected to `IN-`. By doing this and obtaining the current value in the voltage source `vout` (in the output), the value $i_{out}/v_d$ will be plotted; since $v_d = 1V$, this corresponds to the value of the **transconductance**, $\mathbf{g_m}$. Using the same cellview, a transient analysis is made and the value of the output current is plotted over time.

In the first plot, the expected change in the transconductance with frequency was obtained, except for very high frequencies. The latter occurs to the influence of second order effects, which are not usually considered in simpler models; due to this, the transconductance eventually starts to increase. For lower and medium-range frequencies - in the bandwidth, approximately up until $\mathrm{f} = 1\mathrm{MHz}$ - the value $\mathrm{iout/vd}$ has no significant variation, remaining perfectly constant for lower frequencies. This corresponds to **weak inversion** for the transistors. The numerical value of 23.4 corresponds to $\mathrm{g_m/I}$, since $\mathrm{I} = 1\mu\mathrm{A}$ in each branch of the differential pair. For higher frequencies (in between 1MHz and 10MHz), the curve is approximately linear and corresponds to the strong inversion region. As for the transient analysis, an almost sine-like curve was obtained for the output current, with plateaus of constant $\mathrm{I_{out}}$ at the minimum and maximum values of this current. To obtain this plot, the frequency $\mathrm{f} = 100\mathrm{Hz}$ was used at `vin-` (in which there is weak inversion).

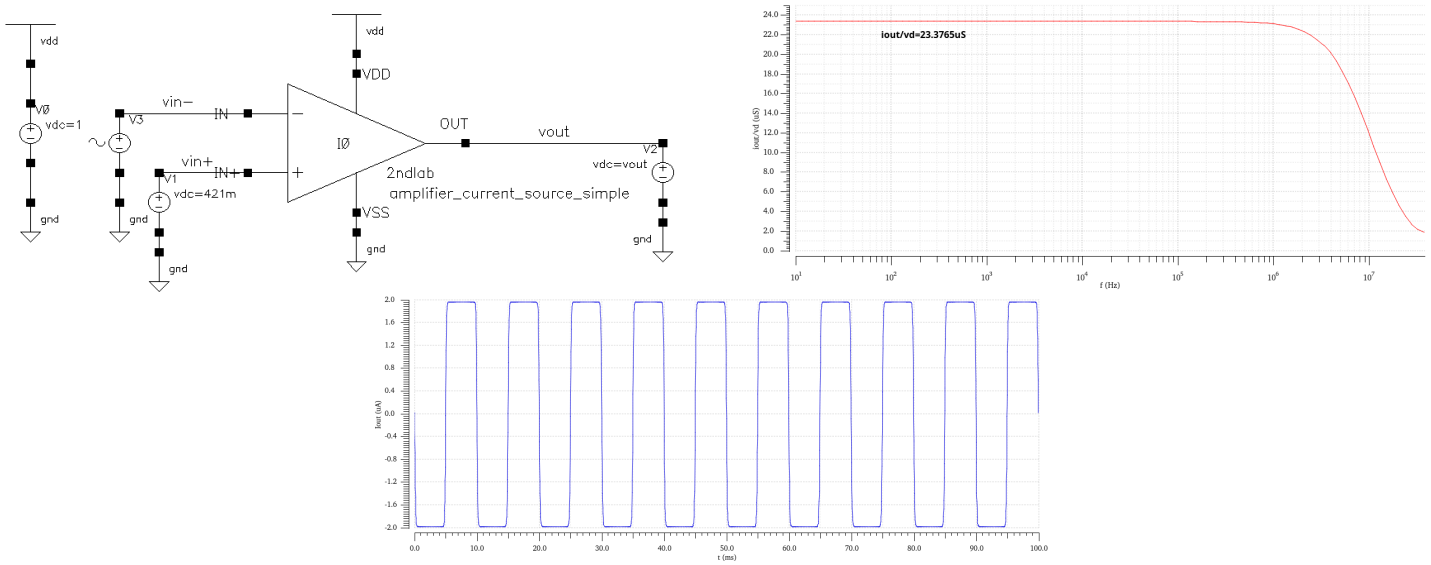


**Figure 3:** On the top left, view used for AC and transient analyses with the transconductance amplifier shown in Figure 1, with an instance `vsin` connected to the input `IN-`. In the simulations, a voltage value `vout=401mV` and an AC voltage value of 1V at `V3` (with 421mV in the DC component) were selected. Very similar views were used with other amplifier configurations (indicated in Figure 5). On the top right, plot of the transconductance, obtained from a frequency sweep (10Hz to 38MHz) in AC analysis, whose numerical values are the same as the values of the output current (at `V2`), since $\mathrm{g_m} = \mathrm{i_{out}/v_d}$ (with $\mathrm{v_d} = 1\mathrm{V}$). On the bottom, plot of the output current $\mathrm{i_{out}}$ obtained from a transient analysis (stop time of 100ms), having the frequency $\mathrm{f} = 100\mathrm{Hz}$ been selected in `V3`.

Finally, in the cellview shown in Figure 4, an AC voltage was now connected to the output (using DC voltage sources in the inputs), in which a DC component $\mathrm{V_{out}} = 401\mathrm{mV}$ and an AC value of $\mathrm{v_{out}} = 1\mathrm{V}$ were selected. Due to the latter, in an AC analysis with a frequency sweep, the plot of the output current will offer the value of $\mathrm{r_o^{-1}}$, where $\mathrm{r_o}$ is the output resistance of the amplifier. Similarly to the graph shown in Figure 3, a constant value was obtained for lower frequencies - this corresponds to $\mathrm{r_o^{-1}}$, where $\mathbf{r_o}$ is the **output resistance** of the amplifier.

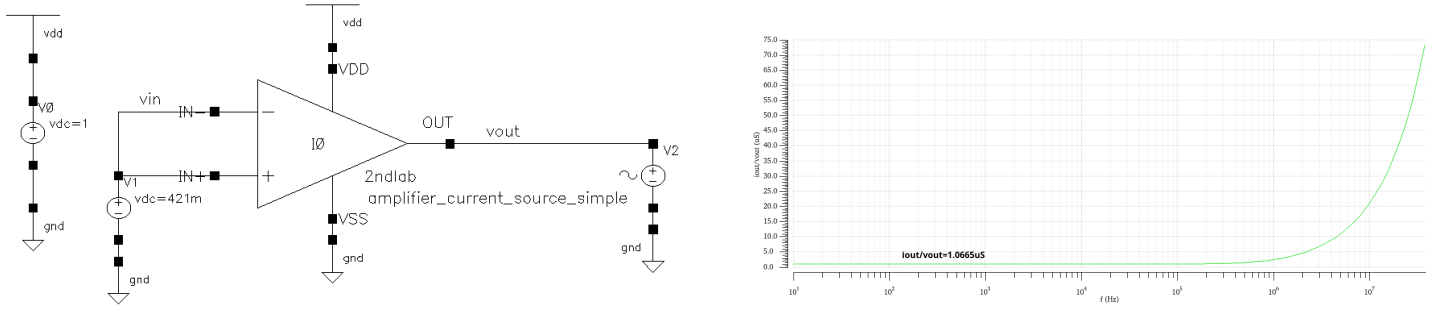


**Figure 4:** On the left, view used for AC analysis with the transconductance amplifier shown in Figure 1, with an instance `vsin` connected to the output. In the simulations, an AC voltage value of 1V at `V2` was selected (with a DC component of 401mV). Very similar views were used with other amplifier configurations (indicated in Figure 5). On the right, plot of the inverse of the output resistance, obtained from a frequency sweep (10Hz to 38MHz) in AC analysis, whose numerical values are the same as the values of the output current (at `V2`), since $\mathrm{r_o} = \mathrm{i_{out}/v_{out}}$ (with $\mathrm{v_{out}} = 1\mathrm{V}$).

The exact same analyses were made for three different circuit configurations. As indicated in Figure 5, asides from using a current source connected to the differential pair (as shown in Figure 1), a pMOS transistor (of width $\mathrm{W} = 125\mu\mathrm{m}$) with an externally applied gate voltage ($\mathrm{V_{bias}}$) was included in a different schematic (which is in all other aspects the same as in Figure 1). The value of this voltage was determined in order to have $\mathrm{I_D(M9)} = 2\mu\mathrm{A}$ above the differential pair. In addition, another schematic, with a current mirror, was used in the design of the amplifier. In this case, a bias current $\mathrm{I_{bias}}$ was connected to the drain of the pMOS transistor and a sweep of its value was made in order to have $\mathrm{I_D(M9)} = 2\mu\mathrm{A}$ once again - using width $\mathrm{W} = 125\mu\mathrm{m}$ for both transistors. In a typical current mirror application, the drain currents in M9 and M10 could be the same; however, in this case, due to the low value of $\mathrm{V_{DD}} = 1\mathrm{V}$, it is not possible for both these pMOS transistors to have $\mathrm{V_{SD}} > \mathrm{V_{SG}} - \mathrm{V_t}$ and $\mathrm{V_{SG}} > \mathrm{V_t}$, thus the saturation region is not reached and the drain current in M9 will naturally be lower than the externally applied drain current in M10. Since the plots obtained with configurations (b) and (c) are very similar to the plots obtained for configuration (a), they will not be included in this report - only the respective numerical results.

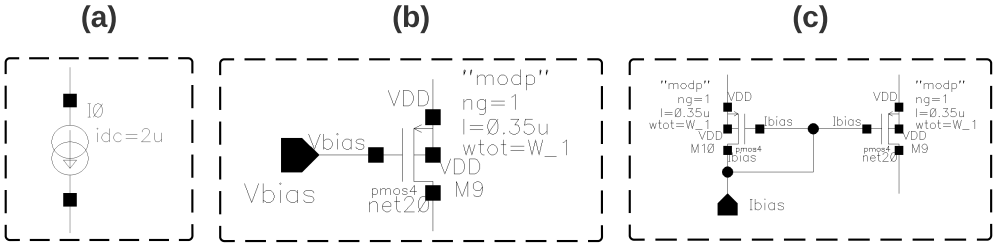


**Figure 5:** Configurations used to provide a current of $2\mu A$ above the differential pair: **(a)** current source; **(b)** single pMOS transistor; **(c)** current mirror. In all transistors, a width of $\mathrm{W} = 125\mu\mathrm{m}$ was used in the simulations. For the results in this section, the values $\mathrm{V_{bias}} = 132.114\mathrm{mV}$ and $\mathrm{I_{bias}} = 243.399\mu\mathrm{A}$ were selected; on the other hand, $\mathrm{V_{bias}} = 214.36\mathrm{mV}$ and $\mathrm{I_{bias}} = 83.955\mu\mathrm{A}$ were used to obtain the results shown in the next section.

Having performed every necessary simulation, with each of the three amplifier configurations, the respective numerical results are now shown in Table 1. Firstly, it indicates that $\mathrm{V_{SG}(M1/M2)}, \mathrm{V_{SG}(M7/M8)} < \mathrm{V_M(c=3)_{pMOS}} = 0.579\mathrm{V}$, thus it can be estimated that all the pMOS transistors (M1, M2, M7 and M8) are operating in **weak inversion**. On the other hand, the exact same cannot be said for the nMOS transistors, since $\mathrm{V_{GS}(M3/M5)}, \mathrm{V_{GS}(M4/M6)} \gtrsim \mathrm{V_M(c=3)_{nMOS}} = 0.401\mathrm{V}$; however, it can also be predicted that all nMOS transistors in the circuit are working in **weak inversion**, since $\mathrm{V_{GS}(M3/M5)}, \mathrm{V_{SG}(M4/M6)} < \mathrm{V_M(c=2)_{nMOS}} = 0.434\mathrm{V}$.

Regarding the transconductance, $\mathrm{g_m} = \mathrm{i_{out}/v_d} > 10\mathrm{uS}$, thus the desired transconductance values were not obtained with these current amplifier configurations. Even though $\mathrm{r_o}$ was the same for all cases, $\mathrm{g_m}$ was slightly larger for (a), which led to a slightly larger gain $\mathrm{A_o} = \mathrm{g_m r_o}$.

| | Values | | |
|---|---|---|---|
| **Designation** | **(a)** | **(b)** | **(c)** |
| $\mathrm{V_{net20}}$ | 999.0mV | | |
| $\mathrm{V_{net31}}$ | 421.6mV | | |
| $\mathrm{V_{SG}(M1/M2)}$ | 578.0mV | | |
| $\mathrm{V_{GS}(M3/M5)}$ | 411.0mV | | |
| $\mathrm{V_{GS}(M4/M6)}$ | 411.0mV | | |
| $\mathrm{V_{SG}(M7/M8)}$ | 578.4mV | | |
| $\mathrm{V_{SG}(M9/M10)}$ | - | 867.9mV | 868.0mV |
| $\mathrm{I_D(M1)}$ | 1.0$\mu$A | | |
| $\mathrm{I_D(M2)}$ | 1.0$\mu$A | | |
| $\mathrm{I_D(M7)}$ | 1.0$\mu$A | | |
| $\mathrm{I_D(M8)}$ | 1.0$\mu$A | | |
| $\mathrm{I_D(M9)}$ | - | 2.0$\mu$A | 2.0$\mu$A |
| $\mathbf{g_m}$ | 23.4$\mu$S | 23.1$\mu$S | 23.1$\mu$S |
| $\mathbf{r_o}$ | 937.6k$\Omega$ | 937.6k$\Omega$ | 937.6k$\Omega$ |
| $\mathbf{A_o}$ | 21.9 | 21.7 | 21.7 |

**Table 1:** Numerical results obtained from the DC and AC simulations done with the transconductance amplifier shown in Figure 1, as well as by replacing the current source with the other configurations shown in Figure 5. The transconductance is designated as $\mathrm{g_m(=i_{out}/v_d)}$, $\mathrm{r_o}$ is the output resistance and $\mathrm{A_o} = \mathrm{g_m r_o}$ is the gain of the amplifier.

## (B) New current mirror configuration

As mentioned in the previous section, the desired relation $\mathrm{g_m} = \mathrm{i_{out}/v_d} < 10\mu\mathrm{S}$ was not obtained. Therefore, the proposed alterations to the current mirrors were made, having the schematic shown in Figure 6 been designed. In this case, the output current of each new current mirror configuration will be divided by $3^2 = 9$ (due to the number of transistors used in the new current mirrors), which should lead to a transconductance of $\mathrm{g_m}/9$, when compared to the results in the previous section. Once again, all transistors have widths of $\mathrm{W} = 125\mu\mathrm{m}$ and the DC voltage values $\mathrm{V_{in-/in+}} = 421\mathrm{mV}$ and $\mathrm{V_{out}} = 401\mathrm{mV}$ were used once again.

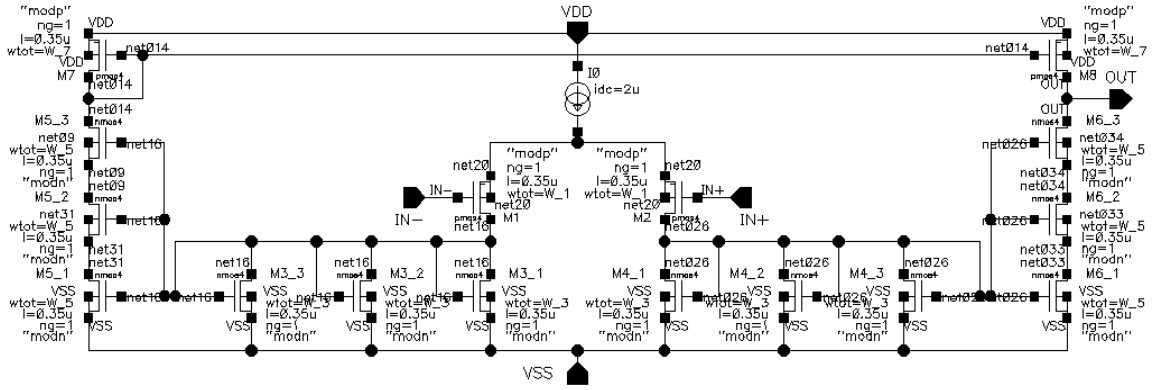


**Figure 6:** Schematic of the transconductance amplifier with a new current mirror configuration, designed in Cadence Virtuoso. For all transistors, a width $\mathrm{W} = 125\mu\mathrm{m}$ was used in the simulations.

Regarding the schematic shown in Figure 6 (with configuration (a) from Figure 5), the same DC, AC and transient simulations were performed, having the plots shown in Figure 7 been obtained. For this purpose, similar cellviews from the ones shown in Figures 3 and 4 were used, having the amplifier been replaced with the new design. A similar behaviour can be seen for $\mathrm{g_m} = \mathrm{i_{out}/v_d}$ in the different frequencies, with an initial plateau followed by an approximately linear decrease and a final increase due to second order effects. However, as predicted, much lower $\mathrm{g_m}$ values have been obtained. On the other hand, there is also a lower bandwidth, i.e., the weak inversion

occurs for a smaller interval of frequencies - the decrease in $g_m$ becomes more significant starting at frequencies close to 0.1MHz, 1 order of magnitude smaller than in the previous section. As for the transient analysis plot, a similar wave shape has been obtained, even though the respective current values are much smaller (in 1 order of magnitude) - as expected. Finally, a lower output resistance $r_o$ has been obtained.

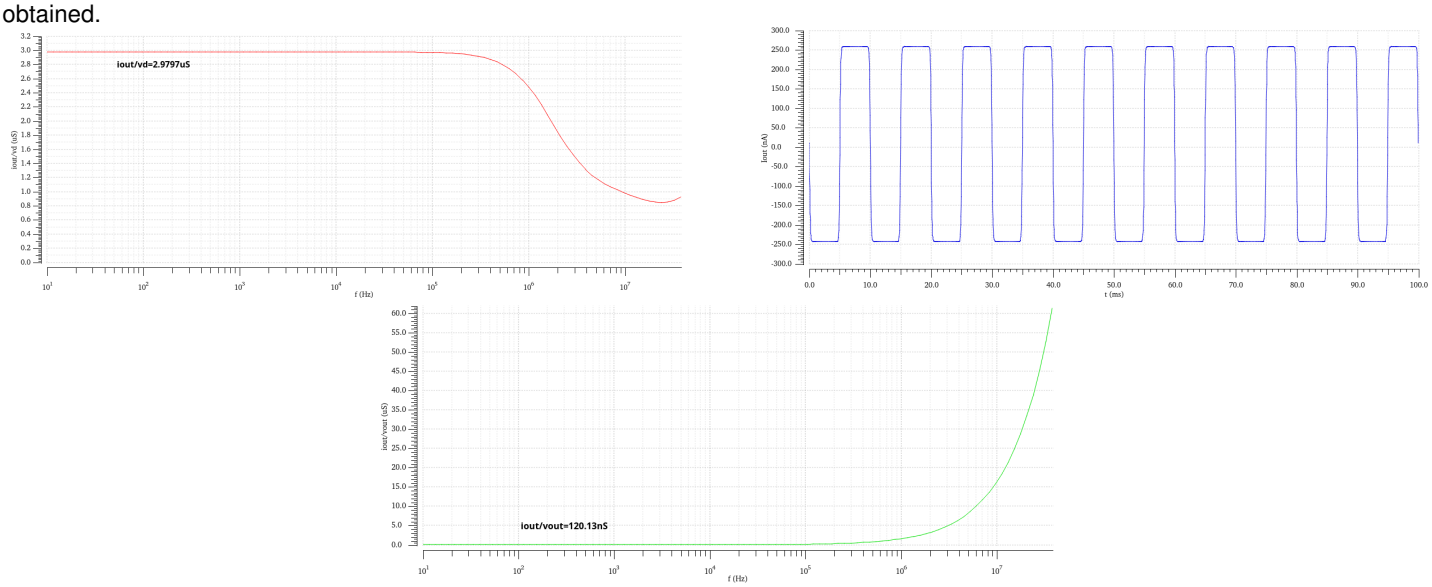


**Figure 7:** On the top left, plot of the transconductance, obtained from a frequency sweep (10Hz to 38MHz) in AC analysis, whose numerical values are the same as the values of the output current (at V2, shown in Figure 3), since $g_m = i_{out}/v_d$ (with $v_d = 1V$). On the top right, plot of the output current $i_{out}$ obtained from a transient analysis (stop time of 100ms), having the frequency $f = 100Hz$ been selected in V3 (shown in Figure 3). On the bottom, plot of the inverse of the output resistance, obtained from a frequency sweep (10Hz to 38MHz) in AC analysis, whose numerical values are the same as the values of the output current (at V2, shown in Figure 4), since $r_o = i_{out}/v_{out}$ (with $v_{out} = 1V$).

Having performed the simulations with the new current mirrors and with all configurations from Figure 5, the results shown in Table 2 were obtained. In this case, $V_{SG}(M1/M2), V_{SG}(M7/M8) < V_M(c = 3)_{pMOS} = 579mV$, thus transistors M1, M2, M7 and M8 should be working in **weak inversion**. However, the newly added M9 and M10 (the latter only in configuration (c)) are not; in fact, M7 and M8 should be working in moderate inversion, since $V_M(c = 1)_{pMOS} = 626mV < V_{SG}(M7/M8) < V_{H,pMOS} = 849mV$. On the other hand, $V_{GS} < V_M(c = 3)_{nMOS} = 401mV$ - which did not occur in the simulations in the previous section -, thus all nMOS transistors in the transconductance amplifier should clearly be working in **weak inversion**.

Regarding the values of the transconductance, the desired relation $g_m = i_{out}/v_d < 10\mu S$ has been achieved, with the difference being in 1 order of magnitude when compared to the previous results. Contrarily to what was expected (final transconductance values given by $g_m/9$, when compared to the previous simulations), ratios of 7.8 (for configuration (a)) and 7.5 (for configurations (b) and (c)) have been obtained. Finally, all output resistances $r_o$ were the same among each other and higher in 1 order of magnitude when compared to the previous section. Since $g_m$ was slightly lower for configuration (a), a slightly lower gain $A_o = g_m r_o$ was obtained, even though $A_o$ for these new circuits are higher than $A_o$ obtained with the previous current mirror configurations.

| | Values | | |
|---|---|---|---|
| **Designation** | **(a)** | **(b)** | **(c)** |
| $V_{net20}$ | 997.9mV | | |
| $V_{net31}$ | 12.8mV | | |
| $V_{net9}$ | 34.6mV | | |
| $V_{net14}$ | 501.5mV | | |
| $V_{net33}$ | 12.7mV | | |
| $V_{net34}$ | 33.9mV | | |
| $V_{SG}(M1/M2)$ | 576.9mV | | |
| $V_{GS}(M3/M5\_1)$ | 373.5mV | | |
| $V_{GS}(M4/M6\_1)$ | 373.5mV | | |
| $V_{GS}(M5\_2)$ | 360.7mV | | |
| $V_{GS}(M5\_3)$ | 338.8mV | | |
| $V_{GS}(M6\_2)$ | 360.8mV | | |
| $V_{GS}(M5\_3)$ | 339.5mV | | |
| $V_{SG}(M7/M8)$ | 498.5mV | | |
| $V_{SG}(M9/M10)$ | - | 785.6mV | 785.1mV |
| $I_D(M1)$ | 1.0$\mu$A | | |
| $I_D(M2)$ | 1.0$\mu$A | | |
| $I_D(M3)$ | 333.3nA | 333.5nA | 333.3nA |
| $I_D(M4)$ | 333.3nA | 333.5nA | 333.3nA |
| $I_D(M5)$ | 122.3nA | 122.4nA | 122.4nA |
| $I_D(M6)$ | 121.1nA | | |
| $I_D(M9)$ | - | 2.0$\mu$A | 2.0$\mu$A |
| $\mathbf{g_m}$ | 3.0$\mu$S | 3.1$\mu$S | 3.1$\mu$S |
| $\mathbf{r_o}$ | 8.3M$\Omega$ | | |
| $\mathbf{A_o}$ | 24.8 | 25.5 | 25.5 |

**Table 2:** Numerical results obtained from the DC and AC simulations done with the transconductance amplifier shown in Figure 6, as well as by replacing the current source with the other configurations shown in Figure 5. The transconductance is designated as $g_m(= i_{out}/v_d)$, $r_o$ is the output resistance and $A_o = g_m r_o$ is the gain of the amplifier.