Digital Signal Processing Systems
Problems about Phase Locked Loops (PLLs)

I — Check only one answer. The penalty for a wrong answer is ¼ point. The minimum score in this group is zero.

1) An analog multiplier used as a phase detector:
☐ can have positive or negative gain.
☐ allows a phase excursion of 2π radians.
☐ only works with square wave signals.
☐ does not generate undesirable signal components at the output.

2) In an analog PLL in which the loop filter has a pole at the origin, the hold range:
☐ is always limited by the VCO.
☐ does not depend on the saturation limits of the VCO.
☐ is not limited by the phase detector.
☐ does not depend on the characteristics of the loop filter.

3) An analog PLL (with positive return gain):
☐ has a lock range which may be higher than the hold range.
☐ is always stable if its order is less or equal to 2.
☐ is always unstable it its order is greater or equal to 3.
☐ has a lock range which is always less than the hold range.

4) A XOR phase detector:
☐ has a linear characteristic when operation is with sinewaves.
☐ allow operation with a $3\pi/2$ rad phase excursion.
☐ can not operate with rectangular waves.
☐ does not generate undesirable signal components at the output.

5) An analog phase locked loop (PLL) in which the loop filter has a pole at a finite frequency:
☐ responds with a nonzero but finite phase error to a phase step.
☐ responds with a finite nonzero phase error to a frequency step.
☐ responds with a finite nonzero phase error to a frequency ramp.
☐ responds with an infinite phase error to a phase ramp.

6) An analog PLL with return gain $\lambda > 0$:
☐ is stable only if it is of first order.
☐ is stable regardless of the order.
☐ if it is of third order it cannot be made stable.
☐ can be designed to be stable no matter the order.

7) A type D *flip-flop* phase detector:
☐ has a linear, periodic, phase characteristic.
☐ allows a maximum phase excursion of π radians.
☐ only works with square waves.
☐ has a phase characteristic with dead-zones which depend on the waveforms duty-cycle.

II — Consider an analog PLL in which the phase detector characteristic is shown in the box at right. The loop has a lowpass filter with $-6V$ and $+8V$ saturation voltages, DC gain $F(0)$ and a pole at f_p. The voltage-controlled oscillator (VCO) generates a wave with the characteristics in the box at right.
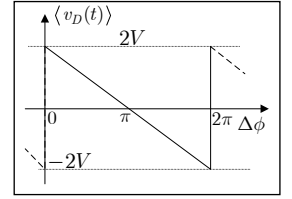
a) Determine the maximum filter gain $F(0)$ such that 1) the loop is stable and 2) the hold range is as large as possible.

$$\omega_o = \begin{cases} \omega_{o1} = 10\pi \times 10^6 \text{ rad/s}, & v_E \leq -8V \\ \omega_{ol} + k_o v_E & -8V \leq v_E \leq 8V \\ \omega_{o2} = 2\pi \times 10^6 \text{ rad/s}, & v_E \geq 8V \end{cases}$$

b) Determine the static characteristics of all PLL components and sketch them interconnected. Determine k_o, ω_{ol} and the phase detector gain k_D. If you did not answer a) consider $F(0) = 2$ from now on.

c) Determine the PLL hold range $\Delta\omega_L$ stating which components are responsible for its limitation. Determine the filter pole frequency f_p such that the lock range is approximately $\Delta\omega_C \approx 0.8\Delta\omega_L$. Justify.

d) Determine the input frequency for which the phase shift between the input and VCO signals is $\Delta\phi = 3\pi/2$.

e) Explain how could the PLL be modified such that the phase shift between the input and VCO signals is always $\Delta\phi = 3\pi/2$, independently of the input frequency. With this modification would the hold range be different? If yes recompute it.

f) Determine the detection characteristic of a logic AND gate when operation is with rectangular waves both with duty-cycle $\delta = 0.25$ and amplitude levels 0V e 1V. Comment on its usefulness and shortcomings as a phase detector.

$$\Delta\omega_C = \sqrt{2\omega_p{}^2\left(\sqrt{1 + \left(\frac{\Delta\omega_L}{\omega_p}\right)^2} - 1\right)} \overset{\Delta\omega_L \gg \omega_p}{\approx} \sqrt{2\omega_p \cdot \Delta\omega_L}$$

Grades: **I -** 7 **II -** a) 2 b) 3 c) 3 d) 1 e) 2 f) 2