TÉCNICO LISBOA

Digital Signal Processing Systems

Problems about Multirate Signal Processing

I — Check only one answer. The penalty for a wrong answer is ¼ point. The minimum score in this group is zero.

1) In a polyphase interpolation structure with a factor L which uses a FIR anti-aliasing filter with N coefficients, with respect to direct form I:

☐ the filter is processed at the lower, pre-interpolation rate.

☐ the number of required multiplications lowers from N to L/N.

☐ the number of memory locations required is the same.

☐ is only useful for high values of L.

2) In a decimator which uses a CIC anti-aliasing filter:

☐ the most efficient computation sequence is: integrator, ($\downarrow M$), *comb*.

☐ the input signal does not have to be oversampled.

☐ with two's complement arithmetic overflows never occur in the filter computation.

☐ the filter's phase characteristic is not linear.

3) In a multirate signal processing system with rational factor L/M:

☐ if $L>M$ there is never loss of information even if the interpolation is done after the decimation.

☐ if the interpolation is done after the decimation loss of information may occur even if $L>M$.

☐ if $L<M$ there is always loss of information.

☐ if the decimation is done after the interpolation there is never loss of information even if $L<M$.

4) In a multirate signal processing system with rational factor L/M:

☐ if $L > M$ there is never loss of information.

☐ if $L < M$ the operation is an interpolation.

☐ if $L > M$ and the interpolation is performed before the decimation, loss of information may occur.

☐ if $L > M$ and the decimation is performed before the interpolation, loss of information may occur.

5) In a polyphase decimation structure with factor M which uses a FIR anti-aliasing filter with N coefficients, with respect to the direct form I implementation:

☐ the filter is processed at the highest (pre-decimation) sampling frequency, f_s.

☐ the number of required multiplications is reduced from N to N/M.

☐ the memory requirement is reduced from N to N/M.

☐ is advantageous only for small values of M.

II – A digital signal processing system operates with a sampling frequency of $f_s = 4$ kHz.

a) The sampling frequency is to be increased to 256 kHz using 3 identical interpolation stages. State what is the value of the maximum input signal bandwidth and if loss of information occurs in this operation. Sketch the interpolation stages block diagram stating the filter cutoff frequency and quality factor as well as the sampling frequency of each stage.

b) Explain the differences of this multistage interpolator with respect to a one-stage interpolator.

c) Sketch the structure of a polyphase decimator with $M = 4$ in which the anti-aliasing filter is a FIR filter with $N = 12$ coefficients. What is the computational and memory economy with respect to the direct I form implementation?

d) Sketch the most efficient signal flow diagram of a one-stage CIC filter to be used as an anti-image filter in an interpolator with interpolation factor L. Justify your answer with detaill.

III — Consider a digital radio system in which it is necessary to decrease the sampling frequency from f_s to $\frac{f_s}{6}$ using a decimator with a CIC *anti-aliasing* filter. The input signal has unilateral bandwidth $B = \frac{f_s}{24}$.

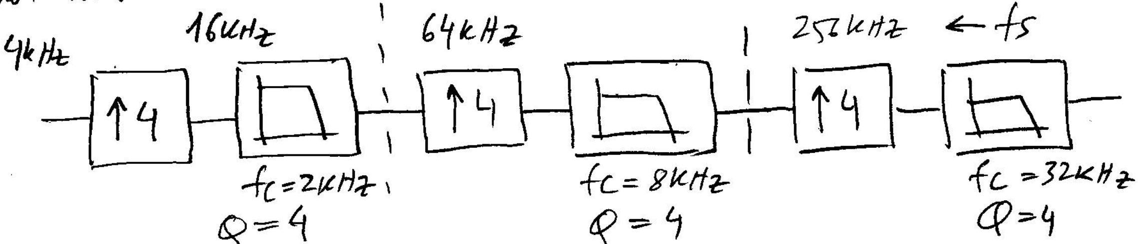
a) Sketch the most efficient signal flow diagram of the decimation CIC filter with two stages ($N = 2$) stating the sampling frequencies along the diagram. Explain the advantages and disadvantages of this type of filter.

b) Sketch the amplitude of the CIC filter frequency response for $0 \le f \le f_s$. Determine the number of CIC stages N that should be used to have at least 50 dB attenuation on the first aliasing band.

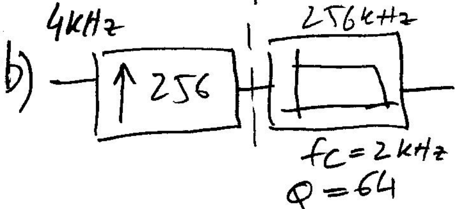
SPDS – Multirate signal processing I-) 1/1/2/4/2

II – $f_s = 4kHz \to 256kHz$, $L = \frac{256}{4} = 64 = 4^3 \Rightarrow$ 3 stages with $L=4$

Since the input sampling frequency is $f_s = 4kHz$, the maximum signal bandwidth is $B = \frac{f_s}{2} = 2kHz$. There is no loss of information because decimation is not involved.

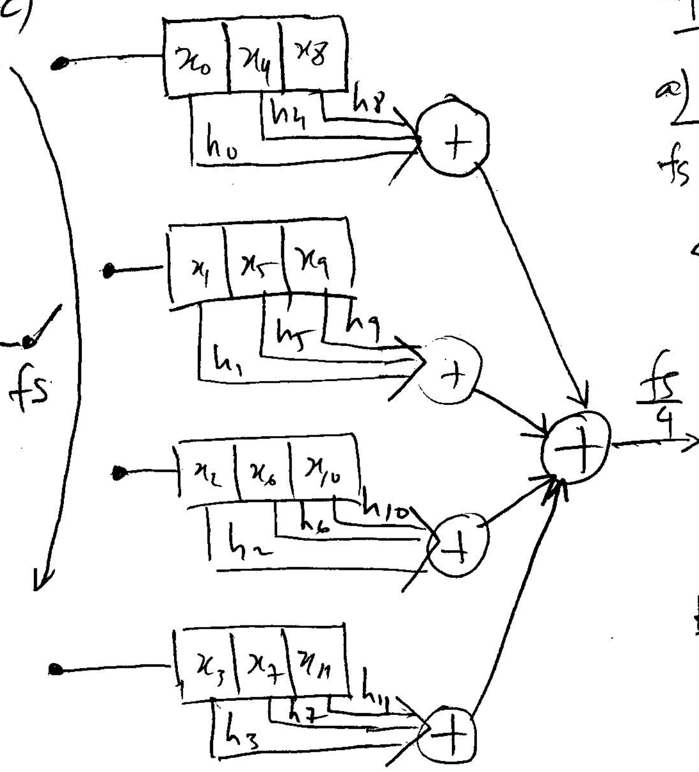


b)



Complexity is proportional to the filter quality factor. With one stage $C = Q = 64$. With 3 stages $C = 3 \times 4 = 12$, $\approx \frac{64}{12} = 5.333$ more economical

c)

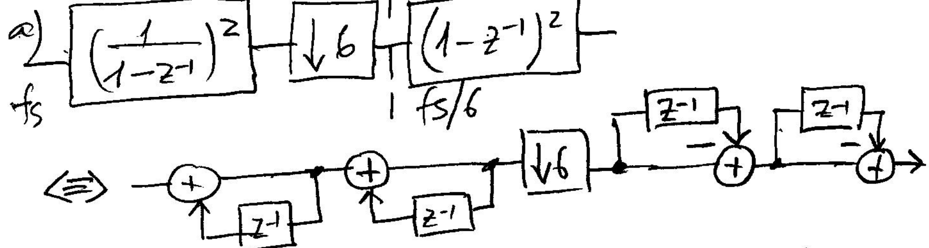


No memory economy.

$\frac{N}{M} = \frac{12}{4} = 3\times$ computational economy

III – $f_s \to \frac{f_s}{6}$, $M = 6$ using A.A. CIC filter $N = 2$ stages

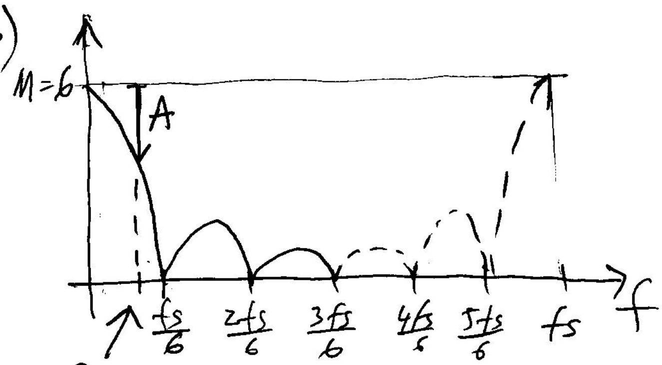
a)



⊕ Simple, easy to replicate, no multiplications, no coefficient memory, linear phase

⊖ lack of flexibility of the filtering function, input signal needs to be oversampled (at least 2X)

b)



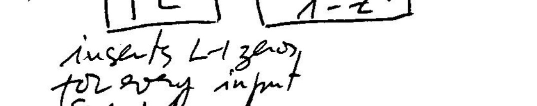
$\frac{f_s}{M} - B = \frac{f_s}{6} - \frac{f_s}{24} = \frac{3f_s}{24} = \frac{f_s}{8}$,

$|H(\omega)| = \left|\frac{\sin \frac{M\omega T_S}{2}}{\sin \frac{\omega T_S}{2}}\right|$, $A = \frac{|H(0)|}{|H(\omega)|_{\omega = 2\pi\left(\frac{f_S}{M} - B\right)}} =$

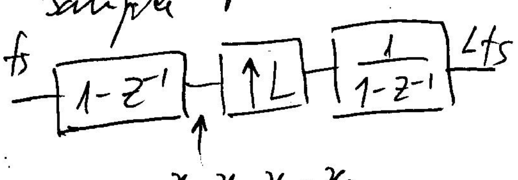
$= 6\left|\frac{\sin \pi/8}{\sin 6\pi/8}\right| = 3.2472 = 10.23$ dB/stage

To achieve 50dB, $N = 5$ stages are required the actual attenuation is 51.15 dB

d)



inserts L-1 zeros for every input sample



$x_0 - x_1, x_1 - x_2, \ldots$

reduces memory locations from L to 1, and the comb filter is processed at the lower rate.