

Sistemas de Processamento de Sinal (SPDSina)

Analog phase locked loop (PLL) analysis

Consider an analog PLL with a multiplier-type phase detector, a first order lowpass filter and a sinusoidal VCO with the following characteristics:

- a) Sketch the PLL clock diagram and propose a circuit to implement the loop filter using an operational amplifier with $\pm 5 \text{V}$ supply and saturation voltages.
- b) Consider $v_i(t) = V_i \sin(\omega_i t + \phi_i)$ and $v_o(t) = V_o \cos(\omega_o t + \phi_o)$ with $V_i = V_o = 2V$. Determine and sketch the static characteristics of all loop components and the hold range. Determine an approximation for the lock range.
- c) Consider that the loop is locked with a sinusoidal input signal with frequency $\omega_i = 4\pi$ Mrad/s. Determine the phase difference between the VCO signal and the input signal.
- d) Consider the linearization of the loop around the previous frequency $\omega_i=4\pi$ Mrad/s. Sketch the loop signal flow diagram and determine the system transfer function. Compute the frequency and quality factor of the poles.
- e) Redesign the loop in order to operate as a phase modulator with a Butterworth characteristic for lowpass signals with bandwidth $10~\mathrm{kHz}$ @ -3dB.

Loop feter $V_{0}(s)$ P_{1} $V_{E}(s)$ $V_{E}(s)$ Va) vito VCO

(Ku/s) VCO < 4b(t)= < Vi Vo sinux t + di) (os (ustoda)) F(0) = - R =-2 = ViV Sin(withou) t+ dit do] + + Sin[(wi-wo) t + di-do] > clinine to do by F(s) Wp = 1 = 211 × 1000 red/13 When locked, wi awo = Vivo (Sin [(wi-w)t+ AQ]) $\langle v_p(t) \rangle = \frac{\sqrt{i} v_0}{2} \sin \Delta \phi = 2 \sin \Delta \phi$ justantaneous, total Lockpoint Stability

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|-2=Kpf(0)Ko>0 New (Mad/s) W(t) = WUE + KU VE/t) 10TT = Wel + 5KO -> SKO = TT Macd/S/V 2TT = Wel - 3KO -> [Wel = STT Macd/S Stace = free running VCO frequery 21 Ku- WE -3 Hold range: Upper limit = WI = 9T Mrcd/s limited by the lower saturation" of the phase detector. Lower limit = WI = 27T Mrcf/s limited by the lower saturation of the DWL = WL+-WL = 7TMred/s (3.5MH2) Approximation for the lock range: So DWC = 2#X83.67 Kmed/s because DWL = 7.TM ned/s and wp = 27 Kred/s. c) Loop locked with wi=4TTMncd/s so VE=-IV, VD = =1=0.5V. KHZ the other hand VD = 2 sin Ad so Ad= a sin(\frac{1}{2}) = a sin \frac{1}{4} = 0.92TT. December 1 why? d) Gain Kp = \frac{\partial (\sigma \text{ (Ad = 0.92)}}{\partial \text{ (Ad = 0.92)}} = 2005 0.92) = 1.935 V/mod. this is our operating point

System fransfer function: KD F/s). Ku di (F(s) - F(s) - F(s) -Tols) 1+ KOF(S) Kg $\frac{\omega_{p}\lambda}{s^{2}+\omega_{p}s+\omega_{p}\lambda} \quad \begin{cases} Q_{c} = \frac{\omega_{c}}{\omega_{p}} = \sqrt{\frac{\lambda}{\omega_{p}}} \\ \omega_{c} = \sqrt{\frac{\lambda}{\omega_{p}}\lambda} \end{cases}$ KD F(0) Ko 5 1 + Kn F(u) Ko $= \frac{\omega_{pK_0K_0F(0)}}{3^2 + \omega_pS + \omega_pK_0K_0F(0)}$ Qc = 43.9 WC = 211 x 43.9 Kred/s e) Redesign to have a phase modulator with we = 27 x10 Kred/s and Qc = 1/2 439 f - - - - N=Qc (Butleworth) reference obdillator (Stable)

Fi [+] + F(S) | Ko/S | Øo $T_{PM}(s) = \frac{\varphi_1(s)}{V_p(s)} = \frac{T/s}{K_D} \rightarrow lowpan$ = up N/KD 32 + ax + ax² Qc + ax² wc = up = 211 x 10 Kred/s = 211 x 14.1 Kred/s
PC 1/12 KHz e) (continuation) So, must increase filter bandwidth from 1KHz to 14.1KHz LWL = Ko(Vewer-Venin) because wol is the same. $44^{2} = (2\pi \times 10^{4})^{2} = 44 \times 10^{4} = \frac{(2\pi \times 10^{4})^{2}}{2\pi \times 14.1 \times 10^{3}}$ $= K_0(4-(-3)=7K_0)$ 1 1 = 21TX1278/x2//3 $= 2\pi \times \frac{10^7}{12}$ 1600 = \ 2wp2 (\1+(\frac{\DM}{ap})^2-1) Must change it: choose either Flo) or Ko, Ko is difficult to change. = 211 × 11.79 Kred/s Keep $F(0) \Rightarrow K_0 = \frac{2\pi x_{10}^4}{\sqrt{2}F(0)K_0} = \frac{2\pi x_{10}^4}{\sqrt{2}(-2)(-1.935)}$ Smaller than DWL but much closer = T. 3654.2 rells/ (much lower) Note: NOW, DWL=ZITX12.78 Kred/s and Up= ZTT X14.1 kneds so up) DWL and the approximation used in b) for DWL is not valid because DWL > Wor is not fue.