TÉCNICO LISBOA

Analog and Mixed Integrated Systems

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Middle Target: Project of a Folded Cascode Amplifier with NMOS Input Differential Pair

Bologna Master Degree in Electrical and Computer Engineering (MEEC)

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1) Introduction

The objective of this assignment is to implement a **Folded Cascode Amplifier with an NMOS input differential pair** according to the specifications shown in Table 1. This report includes an explanation on the circuit dimensioning and respective simulations performed in Cadence Virtuoso.

Parameter	Value
Supply voltage, V_{DD} [V]	3.3
Small signal gain, A_v [dB]	66
Bandwidth, Bw [kHz]	10
Phase margin, PM [°]	60
Load capacitance, C_L [pF]	5
Slew-rate, SR [V/μs]	10
Current budget, I_{DD} [μA]	400
Die area budget [mm^2]	0.01

Table 1: Specifications imposed for the folded cascode OTA.

For this purpose, the amplifier architecture shown in the schematic of Figure 1 was used, for reasons which will be discussed throughout this report - these include using low biasing voltages, working with (most) transistors in saturation and minimizing power consumption. To obtain the preliminary circuit dimensioning, some initial restrictions were imposed for simplification purposes - it is considered that all transistors have the same resistance r_o and the same transconductance g_m. Considering this, a theoretical analysis is then performed to obtain the required characteristics of the transistors for simulation purposes. Once these values have been tested, some modifications are made in order to obtain the desired experimental results. After that, current mirrors and an `sp1tswitch` (from `analogLib`) are added to improve the performance of the OTA.

2) Theoretical analysis

The small signal voltage gain of the amplifier (A_v), transconductance of the the transistors in the differential pair (g_m) and output resistance of the amplifier (R_o) are related by equation 1. Moreover, the dominant pole ω_1 is given by equation 2, where C_L is the load capacitance. By multiplying both equations, the relation shown in (3) is obtained. In this equation, all values on the right-hand side are specifications imposed in Table 1, thus the required transconductance value $\mathbf{g_m \approx (6.27 \times 10^{-4})S}$ can be obtained. Using this value, equation 1 leads to an output resistance of $\mathbf{R_o \approx 3.182M\Omega}$. It is worth noting that the values considered for A_v and ω_1 are the lower bounds for gain and bandwidth, respectively. Small changes in g_m and R_o will lead to different values of these parameters. The experimental results should not lead to a lower gain nor bandwidth from the ones indicated in Table 1, thus a decrease in R_o (to increase ω_1) should also be made with an increase in g_m, in order not to reduce A_v.

$$\begin{cases} A_v = g_m R_o \quad (1) \\ \omega_1 = 2\pi f_1 = \frac{1}{R_o C_L} \quad (2) \end{cases} \Rightarrow \quad g_m = A_v \times 2\pi f_1 \times C_L \quad (3)$$

The following step is to use the determined output resistance value to obtain the required resistance r_o for each transistor. For this purpose, equation 4 should be taken into account. In this expression, which also applies to a folded cascode OTA with a PMOS input differential pair [1], the transconductances and resistances correspond to the transistors M_2, M_4, M_6, M_8 and M_{10} indicated in Figure 1. Considering the same resistance r_o and transconductance g_m for all transistors, this equation can be simplified and the value $\mathbf{r_0 \approx 123.4k\Omega}$ can be obtained from it, since the values of R_o and g_m have already been determined.

$$R_o = [g_{m4} r_{o4} (r_{o2} || r_{o10})] \; || \; (g_{m6} r_{o6} r_{o8}) \approx \frac{g_m r_0^2}{3} \quad (4)$$

Now, it is possible to perform the proper circuit dimensioning. For this purpose, the channel length of all transistors was fixed at $L = 1\mu m$. This value - which is not the lowest channel length for this technology (i.e., $L = 0.35\mu m$) - was selected in order to avoid short-channel problems (such as the high impact of channel length modulation) and maintain some margin to eventually reduce L if needed. In order to obtain the necessary widths for the NMOS and PMOS transistors in the circuit, DC simulations were performed with `nmos4` and `pmos4` instances from `analogLib`, for fixed $V_{GS/SG}$ values. By sweeping the value of $V_{DS/SD}$, the inverse of the slopes of the drain current curves in saturation were determined for different values of the channel widths. It was concluded that $\mathbf{W_n = 40\mu m}$ (for the NMOS transistor) and $\mathbf{W_p = 100\mu m}$ (for the pMOS transistor) led to resistance values significantly close to the desired $r_o = 123.4k\Omega$ ($r_{o_n} \approx 118k\Omega$ and $r_{o_p} \approx 120k\Omega$, respectively). It can be seen that $W_p/W_n = 2.5$, which makes sense due to the fact that the mobility of electrons is between 2 to 4 times higher than the mobility of holes [2], thus the channel width of the PMOS transistors must be higher to compensate this and obtain the same current values. It is worth noting that these resistance values are lower than the previously determined r_o. There is no longer an ideal mathematical model and some of the parameters are obtained experimentally, thus discrepancies between the theoretical and experimental results are sure to occur. In this case, it is to be expected that these lower r_o experimental values lead to a smaller output resistance R_o, thus leading to a lower small signal gain A_v and a higher bandwidth, taking into account equations 1 and 2 (respectively).

Having obtained the dimensions of the transistors, it is worth estimating the proper biasing voltages to apply in the transistors. To make sure that the NMOS transistors in the differential pair (M_1 and M_2, shown in Figure 1) work in the saturation region, the overdrive voltage of $V_{OD_{1,2}} = 0.2V$ is assumed. The value of the current in saturation increases with V_{GS}, but this higher voltage also means that the transistor works as a current source for a smaller range of V_{DS} (saturation range). On the other hand, a smaller value increases the sensitivity to V_t - thus the usual design criteria of defining $V_{OD} = V_{GS} - V_t = 200mV$. Using equation 5 and the previously obtained value for g_m, the drain current in these two NMOS transistors can be obtained. This corresponds to the value of $I_N/2$, where I_N is the drain current in M_{11}.

$$I = g_m V_{OD} \quad (5)$$

Based on information extracted from [3], in order to ensure maximized gain and low power dissipation, it can be established that $I_N = (2/3) \times I_{DD}$, where I_{DD} is the total current fed to the circuit. With this in mind, the drain currents in all other transistors can be determined and, therefore, the respective overdrive voltages (using equation 5). Finally, using equations 6 and 7, as well as approximate threshold voltage values $V_{t_n} = 0.5V$ (for the NMOS transistors) and $V_{t_p} = 0.7V$ (for the PMOS transistors) from the parameters in the datasheet [4], estimates for the gate, drain and source voltages in each transistor can be obtained - these values are shown in Table 2. It is important to note, however, that these values do not represent the actual node voltages to be obtained in the circuit, since the overdrive voltages presented here would not lead to a decrease from $V_{DD} = 3.3V$ (on the top of the schematic) to $0V$ (in GND). They are rather limitations for all transistors to work in saturation - which will not happen in experimental results.

$$\text{NMOS}: \begin{cases} V_G = V_S + V_{OD} + V_{t_n} \\ V_D = V_S + V_{OD} \end{cases} \quad (6), \quad \text{PMOS}: \begin{cases} V_G = V_S - V_{OD} - V_{t_p} \\ V_D = V_S - V_{OD} \end{cases} \quad (7)$$

Transistor	Type	V_t[V]	g_m[μS]	r_o[KΩ]	L[μm]	W[μm]	I_D[μA]	V_{OD}[V]	V_G[V]	V_S[V]	V_D[V]
M_1	NMOS	0.5	627	118.3	1	40	125.6	0.2	1.1	0.4	0.6
M_2	NMOS	0.5	627	118.3	1	40	125.6	0.2	1.1	0.4	0.6
M_3	NMOS	0.5	627	118.3	1	40	62.8	0.1	0.7	0.1	0.2
M_4	NMOS	0.5	627	118.3	1	40	62.8	0.1	0.7	0.1	0.2
M_5	PMOS	0.7	627	119.7	1	100	62.8	0.1	2.2	3.0	2.9
M_6	PMOS	0.7	627	119.7	1	100	62.8	0.1	2.2	3.0	2.9
M_7	PMOS	0.7	627	119.7	1	100	188.4	0.3	2.3	3.3	3.0
M_8	PMOS	0.7	627	119.7	1	100	188.4	0.3	2.3	3.3	3.0
M_9	NMOS	0.5	627	118.3	1	40	62.8	0.1	0.6	0	0.1
M_{10}	NMOS	0.5	627	118.3	1	40	62.8	0.1	0.6	0	0.1
M_{11}	NMOS	0.5	627	118.3	1	40	251.2	0.4	0.9	0	0.4

Table 2: Circuit dimensioning and transistor parameters obtained from theoretical analysis, to be tested in initial simulations.

3) Simulation results using the initial circuit configuration

Initially, simulations were run using the schematic and testbench shown in Figure 2, along with the theoretical values shown in Table 2. However, the AC simulation led to a small signal gain of $A_v = 73.24\text{dB}$ and a bandwidth of $BW = 6.0\text{kHz}$. In order to obtain the desired gain and bandwidth values, adjustments were made to the biasing voltage in M_{11} and the input voltage in $M_{1/2}$. By reducing the biasing voltage V_{bias_n}, the current in transistor M_{11} decreases, limiting the current in the differential pair, thus decreasing A_v and increasing the bandwidth - an increase in V_{bias_2} would have an opposite effect, since it would increase the percentage of I_{DD} flowing on the right side of the circuit. Because of this, the new value $\mathbf{V_{bias_N} = 875mV}$ was used. Moreover, since a very small change in this variable had too large of an impact on the results, the voltages `vin+` and `vin-` were slightly increased to 1.3V to help moderate these variations.

By using the testbench shown in Figure 1 once again - with the new values of V_{bias_n}, `vin+` and `vin-` - the very satisfactory values $A_v = 66.68\text{dB}$ and $BW = 12.45\text{kHz}$ were obtained. However, by performing corner analysis in this circuit, incredibly inadequate results were obtained. For this reason, the plots obtained in this first step are not included here and it is therefore necessary to use a different circuit configuration to obtain the desired results.

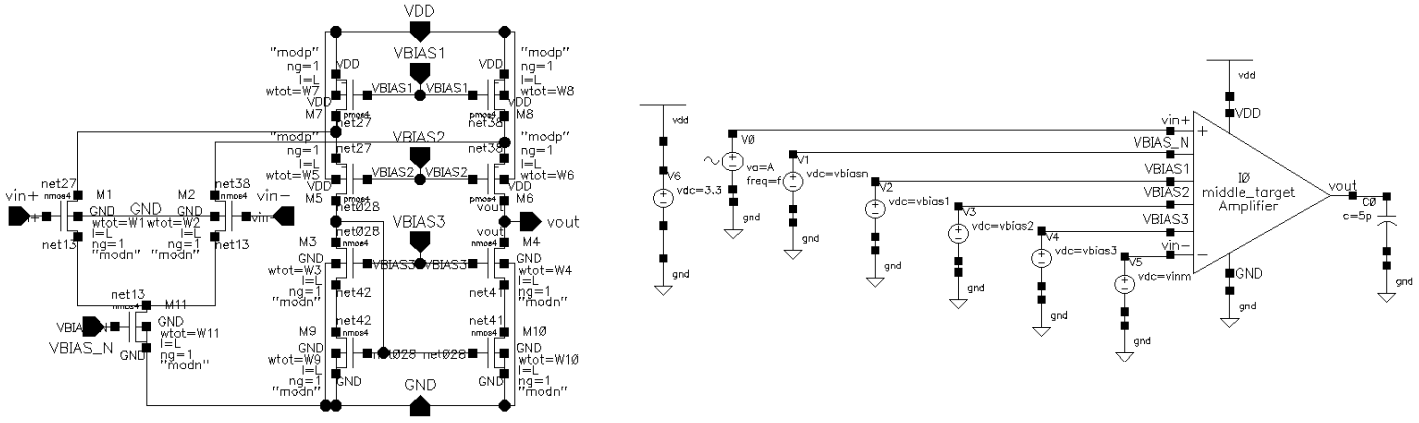

Figure 1: On the left, initial schematic for the folded cascode amplifier. On the right, testbench used for DC, AC and transient simulations, having an AC source been connected to `vin+`.

3.1) Adding current mirrors for better performance

The circuit configuration and dimensioning mentioned previously led to the desired gain and bandwidth values, but a very poor performance in corner analysis was obtained. This occurs because the change in mobility and threshold voltage values performed in this type of analysis significantly impacts the current values in the different branches of the circuit, which drastically changes the gain and bandwidth. This problem can be mitigated by adding **current mirrors** forcing the current values $\mathbf{I_N}$ and $\mathbf{I_{DD}/2}$. By doing so, any of the referred changes will be countered by a changed in the voltages in order to keep the same current values. Since the simulations performed previously led to the desired gain and bandwidth, the DC operating point current values obtained then (i.e., with the testbench shown in Figure 1) will now be forced with the current mirrors - these are $I_N = 304\mu\text{A}$ and $I_{DD}/2 = 173\mu\text{A}$. To do this, the schematic and testbench shown in Figure 2 were used. A DC analysis was performed to determine the channel widths in the newly added transistors, M_{12} and M_{13}, that would lead to these current values, having the parameters $\mathbf{W_{12} = 39\mu m}$ and $\mathbf{W_{13} = 90\mu m}$ been obtained. The other parameters in the circuit (channel widths, channel length and biasing voltages V_{bias_2} and V_{bias3}) were maintained.

The results obtained using the schematic and testbench from Figure 2 are shown in Figure 3. As seen here, adequate values for the small signal gain ($A_v = 66.48\text{dB}$), bandwidth ($BW = 12.72\text{kHz}$) and phase margin ($PM = 76.49° > 60°$) were obtained, with the differences regarding the previous results being explained by the rounded values of W_{12} and W_{13}. This amplification (≈ 2109, in linear units) can be seen in the transient analysis results. For this plot, an input voltage with amplitude of 1mV was selected. It can be seen that distortion occurs for lower voltage values, as transistors can no longer be in saturation, thus the signal at the output is not a sinusoidal wave. This highlights one of the main problems in this circuit configuration - the **DC node voltage** in the output is set at 610.28mV, value in which output sinusoidal waves are centered. Because of this, the values allowed for the amplitude of the input waves are significantly limited.

In this case, the corner analysis and Monte Carlo simulations led to much more acceptable results than before. Even though the current values forced by the current mirrors still change due to changes in μ and V_t, they are not as significant as before. In corner analysis, the

mobilities and threshold voltages of NMOS and PMOS transistors change according to Table 4. In WP (worst power), both mobilities (μ_n and μ_p) increase, while both threshold voltages decrease, which leads to higher current values both in NMOS and PMOS transistors (for instance, I_N and I_{DD}). In this case, the sizes of the transistors help the total current division between branches to favor the NMOS differential pair, increasing the g_m and decreasing the output resistance R_{OUT}. In WO (worst one), only μ_n increases, thus, even though the total current I_{DD} (provided by PMOS transistors) decreases, a larger ratio of this current is fed to the differential pair and A_v increases. In WS (worst speed) it is expected that the opposite of the worst power case occurs, since both mobilities decrease. Less current will be fed into the circuit and for the relation of transistors sizes used, a favoritism of current though the folded branch will be apparent, reducing gain. With WZ (worst zero) the opposite of the worst one case is expected. The PMOS mobility increase will bring the total current to higher values with the NMOS mobility decrease not favoring it's division to the differential pair. This will have a large negative effect on the g_m, lowering the gain.

These results appear in Figure 3 and show that there is still a considerably large discrepancy amongst the gain and bandwidth values, in particular for the WZ **corner** and two of the **Monte Carlo** cases. This fact, along with the low value of the **DC node voltage in the output**, make it clear that additional modifications need to be made to the circuit architecture in order to obtain a proper performance for the folded cascode amplifier.

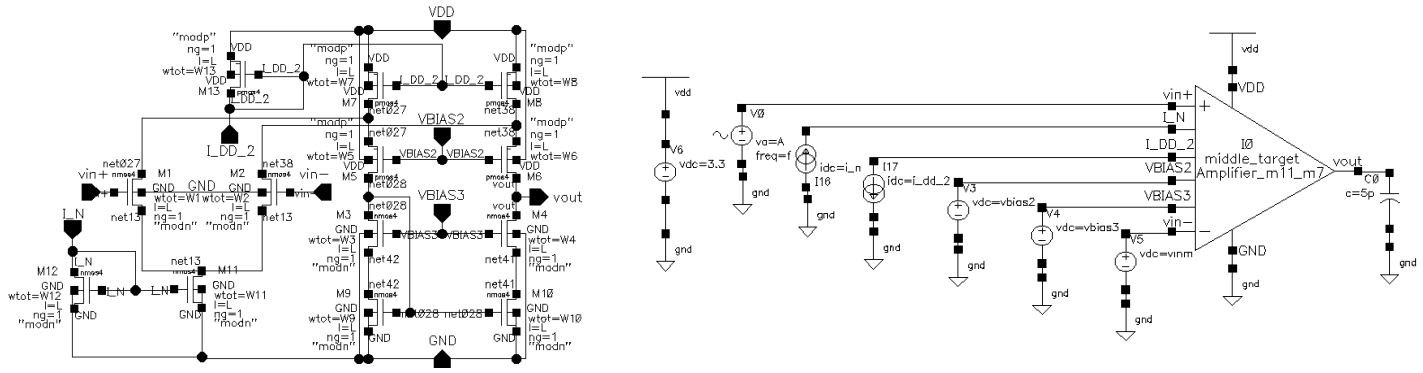

Figure 2: On the left, schematic of the folded cascode amplifier with current mirrors to force the currents in all branches; for this purpose, the transistors `M12` and `M13` were added. On the right, testbench used for this schematic, in which current sources `idc` are connected to the newly added pins.

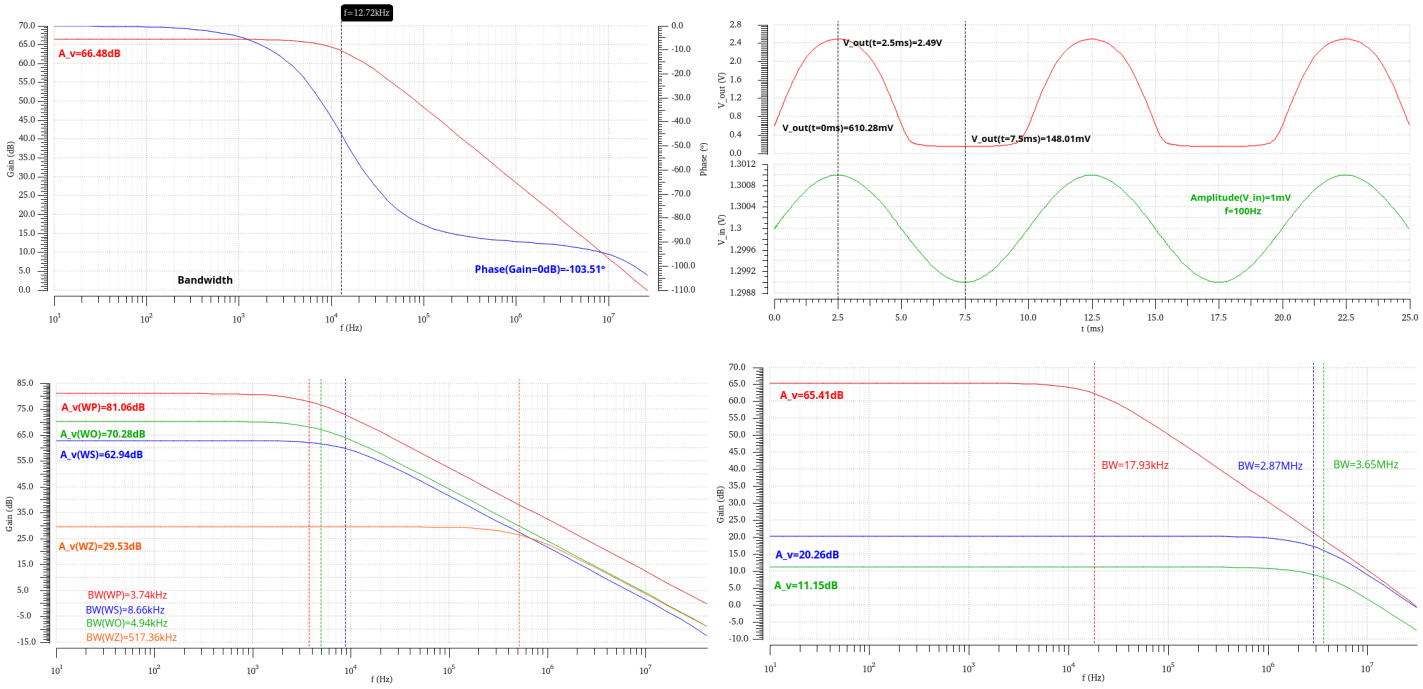

Figure 3: Curves obtained with the testbench shown in Figure 2. On the top left, it can be seen that the desired gain and bandwidth have been obtained; on the top right, saturation of the OPAMP for lower output voltage values; on the bottom, poor performance of this circuit in corner analysis and Monte Carlo simulations (respectively).

4) Adding `sp1tswitch` to fix DC output node voltage at $1.65\mathrm{V}$

Something that can be done to control the output voltage is to use a simulation switch. This switch will remain open (i.e., at '0') in AC simulations, whilst remaining closed (i.e., at '1') in DC and transient simulations. This virtual device allows the circuit to have a feedback from the output voltage to one of the inputs. This will not only copy the DC point that we use as an input voltage, but also help with any small variations on the output by compensating them with a negative feedback on the input, reaching a more stable operational point. We are not changing the circuit, we are just externally controlling the working point of operation.

The equation which describe the differential input amplifier is given by $V_{out} = A \cdot (V^+ - V^-) \Rightarrow V^+ = \frac{1+A}{A} \cdot V^-$ when $V_{out} = V^-$ (A is the gain of the amplifier). Since $A >> 1$, the relation $V_+ \approx V_- = V_{out}$ is obtained. Therefore, in order to center the output sinusoidal waves around $1.65\mathrm{V}$ and fix the issue mentioned in section 3.1, the DC voltage at `vin+` must be fixed at $\mathbf{V^+ = 1.65V}$.

By running an initial AC analysis to obtain the gain and phase curves, using the same parameters (channel widths, channel lengths and biasing voltages) from section 3.1, the desired A_v and bandwidth were not obtained. Moreover, by changing the values of the biasing

voltages, it was not possible to simultaneously obtain the two desired specifications, as the product of bandwidth and gain would not be enough. Therefore, the **channel widths** of the differential pair transistors ($\mathbf{M_1}$ and $\mathbf{M_2}$) were increased to a value of $\mathrm{W} = 175\mu\mathrm{m}$, since an increase in this parameter leads to a simultaneous higher gain and bandwidth. Taking away the current mirrors to experiment with all the possible biasing voltages, small adjustments were made in $\mathrm{V_{bias_N}}$ (changing it to $900\mathrm{mV}$) and $\mathrm{V_{bias_2}}$ (which changed to $1.95\mathrm{V}$). This variables were chosen because of what was mentioned in section 3. These modifications led to the desired gain and bandwidth. Re-implementing the current mirrors, the new achieved currents can now be forced, keeping the benefits seen in section 3.1. In order to determine the channel widths of $\mathrm{M_{12}}$ and $\mathrm{M_{13}}$, a similar procedure as before was performed, having $\mathrm{W_{12}} = 40\mu\mathrm{m}$ and $\mathrm{W_{13}} = 97\mu\mathrm{m}$ been selected (to mirror the current values of $353\mu\mathrm{A}$ and $186\mu\mathrm{A}$ into the transistors $\mathrm{M_{11}}$ and $\mathrm{M_{7/8}}$, respectively). The circuit dimensioning and values obtained for the DC operating point are shown in Table 3.

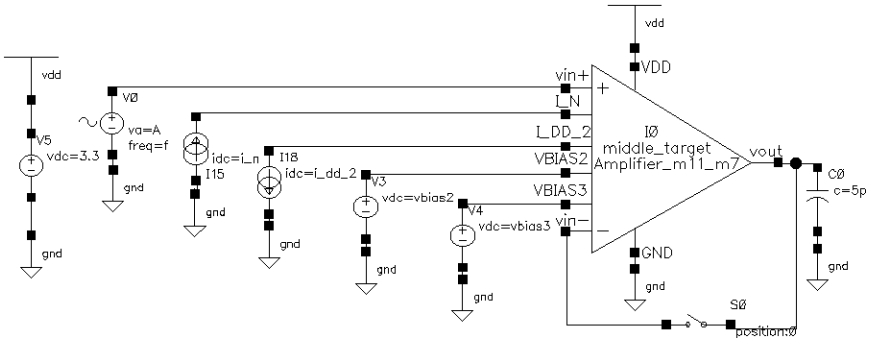

Figure 4: Testbench with an `sp1tswitch` closed for DC and transient, open for AC. The schematic shown in Figure 2 (for the amplifier with current mirrors) was used in these simulations.

Transistor	$\mathbf{W}[\mu\mathrm{m}]$	$\mathbf{I_D}[\mu\mathrm{A}]$	$\mathbf{V_G}[\mathrm{V}]$	$\mathbf{V_S}[\mathrm{V}]$	$\mathbf{V_D}[\mathrm{V}]$
$\mathrm{M_1}$	175	175.8	1.65	0.81	2.80
$\mathrm{M_2}$	175	175.8	1.65	0.81	2.81
$\mathrm{M_3}$	40	9.46	0.70	0.11	0.56
$\mathrm{M_4}$	40	9.48	0.70	0.11	1.65
$\mathrm{M_5}$	100	9.46	1.95	2.80	0.56
$\mathrm{M_6}$	100	9.48	1.95	2.81	1.65
$\mathrm{M_7}$	100	185.3	2.3	3.3	2.80
$\mathrm{M_8}$	100	185.3	2.3	3.3	2.81
$\mathrm{M_9}$	40	9.46	0.56	0	0.11
$\mathrm{M_{10}}$	40	9.48	0.56	0	0.11
$\mathrm{M_{11}}$	40	351.5	0.90	0	0.81
$\mathrm{M_{12}}$	40	353	0.90	0	0.90
$\mathrm{M_{13}}$	97	186	2.3	3.3	2.3

Table 3: Channel widths, DC operating point drain currents and DC node voltages for the simulations performed with an `sp1tswitch` (channel length $\mathrm{L} = 1\mu\mathrm{m}$ for all transistors).

Designation	nMOS	pMOS
WO	$\mu\nearrow$ $V_t\searrow$	$\mu\searrow$ $V_t\nearrow$
WZ	$\mu\searrow$ $V_t\nearrow$	$\mu\nearrow$ $V_t\searrow$
WP	$\mu\nearrow$ $V_t\searrow$	$\mu\nearrow$ $V_t\searrow$
WS	$\mu\searrow$ $V_t\nearrow$	$\mu\searrow$ $V_t\nearrow$

Table 4: CMOS corners: worst case one (WO), worst case zero (WZ), worst case power (WP) and worst case speed (WS) - including the respective variations in carrier mobility μ and threshold voltage $\mathrm{V_t}$.

Using the final circuit configuration (with current mirrors and the switch), the results can be seen in Figure 5 and Table 5. Firstly, it can be confirmed that the desired $\mathrm{A_v} = 66.47\mathrm{dB}$, $\mathrm{BW} = 10.22\mathrm{kHz}$ and $\mathrm{PM} = 76.26^\circ > 60^\circ$ were obtained. In the transient analysis, the output sinusoidal wave has the same amplitude as the input, due to the `sp1tswitch` implementation, having the output been centered around $\approx 1.65\mathrm{V}$, as desired. In terms of corner analysis and Monte Carlo runs, the **success of this circuit implementation** is clear, since the differences between gain and bandwidth values are much smaller than before. The relative positions between the curves of the different corners is the same as before apart from the WP curve, which now goes below WS. This must happen because, in this section, a much larger channel width is used in the differential pair; therefore, the increase in μ_n is no longer as significant and does not change the drain current in $\mathrm{M_1}$ and $\mathrm{M_2}$ significantly. In fact, it can be seen that the curves for WO and WS are very close (in both cases, μ_p decreases), as well as the curves WP and WZ (in which μ_p increases). As for Monte Carlo, a more significant discrepancy is once again seen in the green curve. In Monte Carlo runs (Process and Mismatch), the mobilities and threshold voltages of the transistors also change, according to normal distributions. In future work, the variations which occur in this third curve could be analysed in detail, in order to eventually upgrade the circuit performance even more.

In order to obtain the common-mode gain shown below, a new testbench (similar to the one in Figure 4) was used, in which the input sine wave was connected to both `vin+` and `vin-`. With this, the common-mode small signal $\mathbf{A_{cm}} = \mathbf{-8.45dB}$ was obtained. Using this and the differential gain $\mathrm{A_d} = 66.47\mathrm{dB}$, the **Common-mode rejection ratio (CMRR)** can be calculated by $\mathrm{CMRR} = \mathrm{A_d} - \mathrm{A_{cm}}$ (in dB) - these values are shown in Table 5. Secondly, another testbench was used in which an input square wave (with an amplitude of $0.65\mathrm{V}$ and frequency $100\mathrm{Hz}$ was connected (only) to `vin+`; using the square wave in the output, the **slew-rate** was calculated (with an average of the High→Low and Low→High values) and is also shown below. Finally, using the testbench shown in Figure 4, a noise and harmonic distortion analysis was performed, similarly to what was performed in the previous laboratory assignment. To obtain the **DFT**, as well as the values of the **Signal-to-noise and Distortion (SINAD)**, **Signal-to-noise ratio (SNR)**, **Spurious Free Dynamic Range (SFDR)** and **Total Harmonic Distortion (THD)**, the simulation parameters shown on the bottom right of Figure 5 were used. In this way (and using an input frequency of $\mathrm{f_i} = 1.328125\mathrm{kHz} = 17 \times \Delta\mathrm{f}$), **coherent sampling** occurs - the frequency and final time were changed from the previous laboratory assignment in order to obtain a higher frequency resolution (i.e., lower $\Delta\mathrm{f}$).

Considering only the channel widths and lengths of the transistors, a **preliminary area estimate** of $\mathbf{1.087 \times 10^{-3} mm^2}$ - much lower than the imposed die area budget of $0.01\mathrm{mm}^2$, to be respected after having done the layout. By running transient analysis with different amplitudes in the input sine wave, an **output dynamic range** of $\mathbf{13.35dB}$ (corresponding to $\mathrm{V_{out_{max}}} = 3.08\mathrm{V}$ and $\mathrm{V_{out_{min}}} = 662\mathrm{mV}$, in which saturation is reached) was obtained, along with an **input dynamic range** of $\mathbf{9.40dB}$ (corresponding to $\mathrm{V_{in_{max}}} = 2.48\mathrm{V}$ and $\mathrm{V_{in_{min}}} = 0.84\mathrm{V}$, in which 90% of $\mathrm{A_v} = 66.47\mathrm{dB}$ is reached).

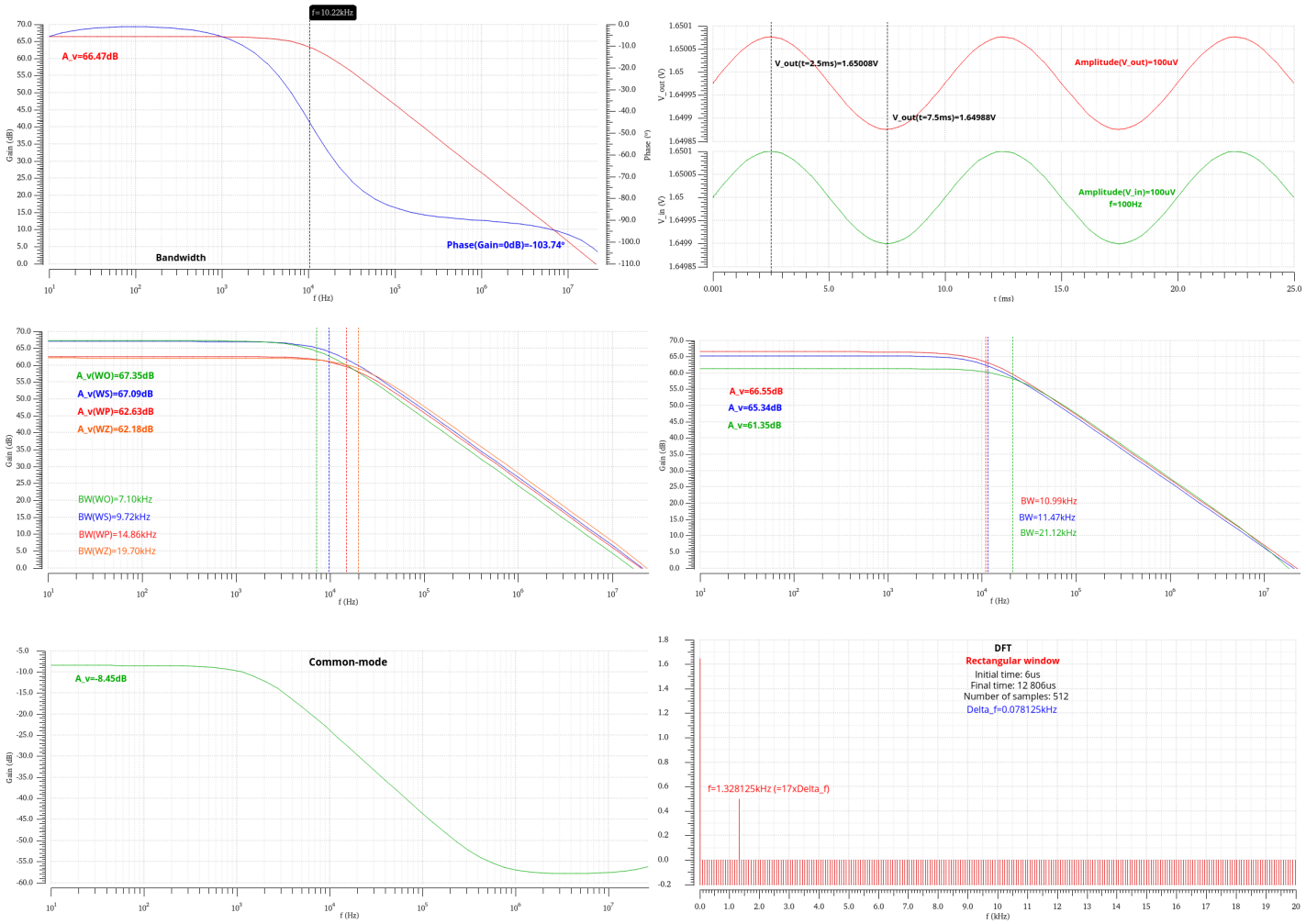

Figure 5: Curves obtained by including an `sp1tswitch`. On the top left, desired gain and bandwidth curves; on the top right, transient simulation results; in the middle, performance of the circuit in corner analysis and Monte Carlo simulations (respectively); on the bottom left, common-mode gain curve; on the bottom right, Discrete Fourier Transform with a rectangular window.

Simulations	$\mathbf{A_v}$**[dB]**	**BW[kHz]**	**PM[°]**	**SR[V/**μ**s]**	$\mathbf{I_{DD}}$**[**μ**A]**	**CMRR[dB]**	**SINAD, SNR[dB]**	**SFDR[dB]**	**THD[%]**
Typical	66.47	10.22	76.26	10.41	370.6	74.92	59.35	67.52	0.11
WP	62.63	14.86	80.12	10.96	376.5	83.14	57.41	63.50	0.13
WS	67.00	9.72	69.76	7.32	368.3	67.98	60.06	66.58	0.10
WO	67.35	7.10	78.64	8.84	366.9	78.94	58.11	63.92	0.12
WZ	62.18	19.70	68.30	8.90	377.4	67.35	59.69	66.82	0.10
MC 1	66.55	10.99	74.72	11.88	377.0	66.70	58.68	67.34	0.12
MC 2	65.34	11.47	77.00	10.99	372.9	71.01	58.57	67.48	0.12
MC 3	61.35	21.12	62.34	8.23	378.1	95.27	56.51	63.40	0.15
Interval	[61.35,67.35]	[7.10,21.12]	[68.30,80.12]	[7.32,11.88]	[368.3,378.1]	[66.70,95.27]	[56.51,60.06]	[63.50,67.52]	[0.10,0.15]

Table 5: Final results obtained for the folded cascode amplifier, using an `sp1tswitch` in the testbench.

5) Conclusion

Initially, a theoretical analysis was made in order to obtain preliminary parameters for the folded-cascode amplifier, which led to undesired gain and bandwidth values in simulation. By changing two biasing voltages, the desired values were obtained, although with very poor performance in corner analysis and Monte Carlo simulations. For this reason, two current mirrors were added, which allowed to obtain better results, but not significantly satisfactory - moreover, the DC output voltage stood around $0.6\mathrm{V}$. In order to obtain much more adequate results, an `sp1tswitch` was added to the testbench, in order to equal the DC voltages of `vin-` and `vout`. By considerably increasing the channel widths of the NMOS transistors in the differential pair (to $175\mu\mathrm{m}$) and slightly altering the biasing voltages, all the proposed objectives for this laboratory assignment were achieved - in terms of small signal gain, bandwidth, phase margin, slew rate, current budget and area. Additionally, the input and output dynamic ranges, noise and total harmonic distortion were characterized and also provided incredibly satisfactory results.

References

[1] Guides and slides available in the subject's Fenix webpage.

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