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Digital Signal Processing Systems

Problems about Phase Locked Loops (PLLs)

I — Check only one answer. The penalty for a wrong answer is ¼ point. The minimum score in this group is zero.

1) An analog multiplier used as a phase detector:
☐ can have positive or negative gain.
☐ allows a phase excursion of 2π radians.
☐ only works with square wave signals.
☐ does not generate undesirable signal components at the output.

2) In an analog PLL in which the loop filter has a pole at the origin, the hold range:
☐ is always limited by the VCO.
☐ does not depend on the saturation limits of the VCO.
☐ is not limited by the phase detector.
☐ does not depend on the characteristics of the loop filter.

3) An analog PLL (with positive return gain):
☐ has a lock range which may be higher than the hold range.
☐ is always stable if its order is less or equal to 2.
☐ is always unstable it its order is greater or equal to 3.
☐ has a lock range which is always less than the hold range.

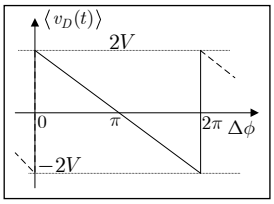
4) A XOR phase detector:
☐ has a linear characteristic when operation is with sinewaves.
☐ allow operation with a $3\pi/2$ rad phase excursion.
☐ can not operate with rectangular waves.
☐ does not generate undesirable signal components at the output.

5) An analog phase locked loop (PLL) in which the loop filter has a pole at a finite frequency:
☐ responds with a nonzero but finite phase error to a phase step.
☐ responds with a finite nonzero phase error to a frequency step.
☐ responds with a finite nonzero phase error to a frequency ramp.
☐ responds with an infinite phase error to a phase ramp.

6) An analog PLL with return gain $\lambda > 0$:
☐ is stable only if it is of first order.
☐ is stable regardless of the order.
☐ if it is of third order it cannot be made stable.
☐ can be designed to be stable no matter the order.

7) A type D *flip-flop* phase detector:
☐ has a linear, periodic, phase characteristic.
☐ allows a maximum phase excursion of π radians.
☐ only works with square waves.
☐ has a phase characteristic with dead-zones which depend on the waveforms duty-cycle.

II — Consider an analog PLL in which the phase detector characteristic is shown in the box at right. The loop has a lowpass filter with $-6V$ and $+8V$ saturation voltages, DC gain $F(0)$ and a pole at f_p. The voltage-controlled oscillator (VCO) generates a wave with the characteristics in the box at right.



$$\omega_o = \begin{cases} \omega_{o1} = 10\pi \times 10^6 \text{ rad/s}, & v_E \le -8V \\ \omega_{ol} + k_o v_E & -8V \le v_E \le 8V \\ \omega_{o2} = 2\pi \times 10^6 \text{ rad/s}, & v_E \ge 8V \end{cases}$$

a) Determine the maximum filter gain $F(0)$ such that 1) the loop is stable and 2) the hold range is as large as possible.

b) Determine the static characteristics of all PLL components and sketch them interconnected. Determine k_o, ω_{ol} and the phase detector gain k_D. If you did not answer a) consider $F(0) = 2$ from now on.

c) Determine the PLL hold range $\Delta\omega_L$ stating which components are responsible for its limitation. Determine the filter pole frequency f_p such that the lock range is approximately $\Delta\omega_C \approx 0.8\Delta\omega_L$. Justify.

d) Determine the input frequency for which the phase shift between the input and VCO signals is $\Delta\phi = 3\pi/2$.

e) Explain how could the PLL be modified such that the phase shift between the input and VCO signals is always $\Delta\phi = 3\pi/2$, independently of the input frequency. With this modification would the hold range be different? If yes recompute it.

f) Determine the detection characteristic of a logic AND gate when operation is with rectangular waves both with duty-cycle $\delta = 0.25$ and amplitude levels 0V e 1V. Comment on its usefulness and shortcomings as a phase detector.

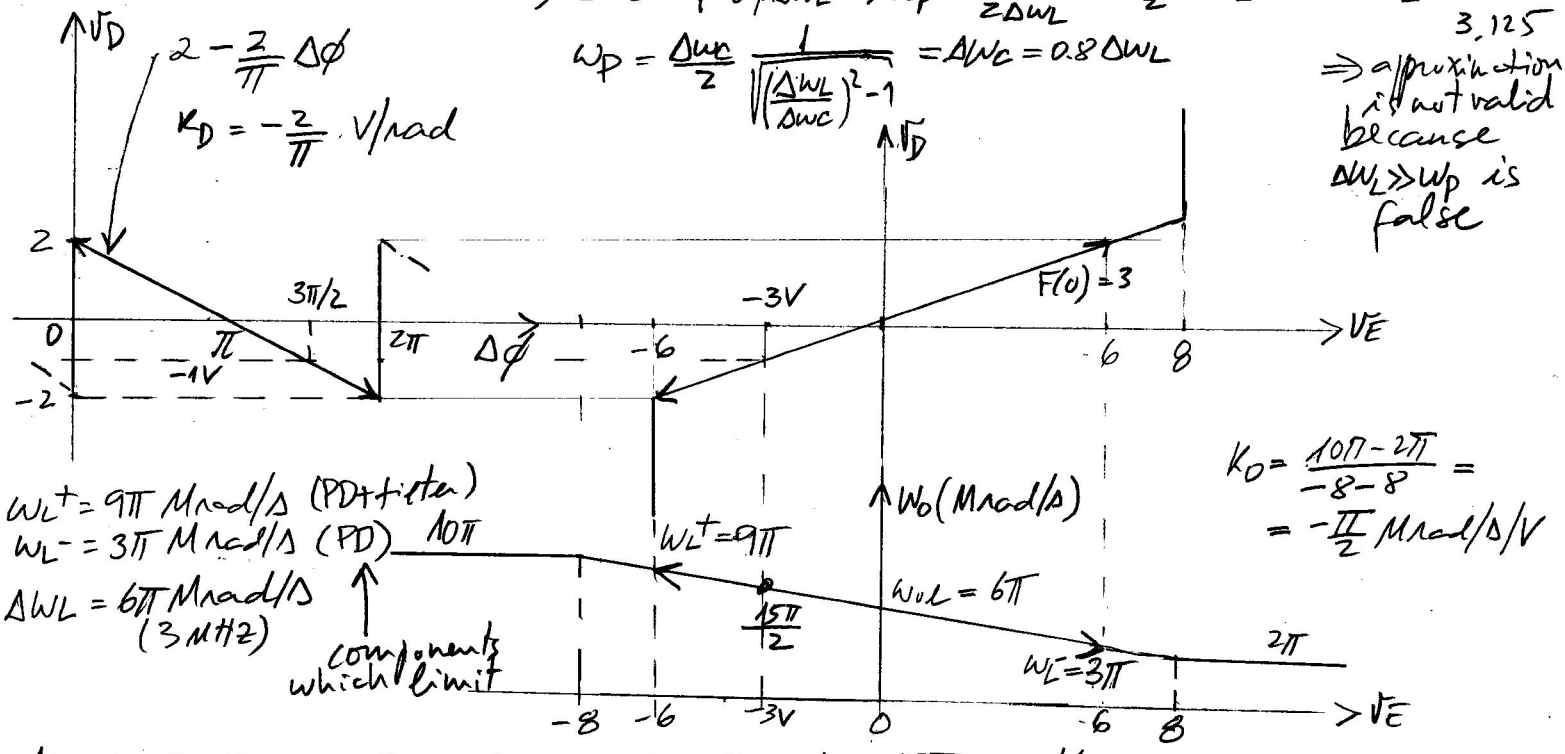
$$\Delta\omega_C = \sqrt{2{\omega_p}^2\left(\sqrt{1+\left(\frac{\Delta\omega_L}{\omega_p}\right)^2}-1\right)} \overset{\Delta\omega_L \gg \omega_p}{\approx} \sqrt{2\omega_p \cdot \Delta\omega_L}$$

Grades: **I -** 7 **II -** a) 2 b) 3 c) 3 d) 1 e) 2 f) 2

SEPS - fourth set of problems, PLLs, solution I- 1/2/3/2/4/4/4 (SEPS)
SPDS 1/3/2/1/2/4/1 (SPDS)

II- a) To have an hold range as large as possible the maximum voltage excursion at V_E should be achieved. Since $K_0<0$ and $K_D<0$, $F(0)$ must be positive. Because the filter saturates at $-6V$, the maximum value of $F(0)$ is $F(0)=3$ since $V_{D\,min}=-2V$.

b)



c) $\Delta\omega_C \simeq \sqrt{2\omega_p\Delta\omega_L} \rightarrow \omega_p = \frac{\Delta\omega_C^2}{2\Delta\omega_L} = \frac{0.8^2}{2}\Delta\omega_L = 0.32\Delta\omega_L = \frac{\Delta\omega_L}{3.125}$

$\omega_p = \frac{\Delta\omega_C}{2}\frac{1}{\sqrt{\left(\frac{\Delta\omega_L}{\Delta\omega_C}\right)^2-1}} = \Delta\omega_C = 0.8\Delta\omega_L$

$\Rightarrow$ approximation is not valid because $\Delta\omega_L \gg \omega_p$ is false

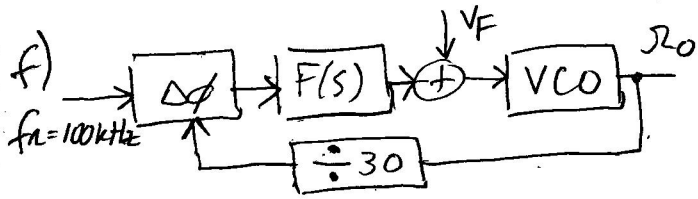
$K_D = \frac{10\pi-2\pi}{-8-8} = -\frac{\pi}{2}$ Mrad/s/V

d) $\Delta\phi=\frac{3\pi}{2}$, $V_D=-1V$, $V_E=-3V$, $\omega_0 = 6\pi - \frac{\pi}{2}(-3) = \frac{15\pi}{2}$ Mrad/s

e) To have a constant phase shift $\Delta\phi$ between the input and the VCO a perfect integrator is required as loop filter so $F(s) = K\frac{1+s/\omega_z}{s}$. The zero at $-\omega_z$ is needed for stability. In this case the loop operates with $\langle V_D\rangle = 0$ so $\Delta\phi=\pi$. To have $\Delta\phi = 3\pi/2$ it is necessary to add 1V before the filter so $\langle V_D\rangle$ becomes $-1V$ (the perfect integrator always operate with an input signal which, on average is zero.

The hold range is modified because now V_E can extend from $-6V$ to $8V$. So ω_L^+ is the same but ω_L^- is now 2π Mrad/s, $\Delta\omega_L = 7\pi$ Mrad/s (3.5 MHz) the PD is no longer responsible for the $\Delta\omega_L$ limitation, the filter is for ω_L^- and ω_L^+ and the VCO also, for ω_L^-.

f)



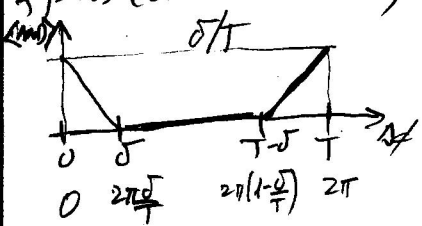
$\omega_0 = 6\pi$ Mrad/s = 3MHz.

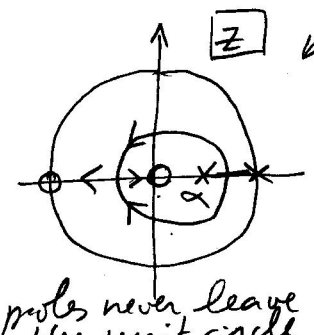
g) the loop is stable for

$0 \le \lambda \le 2\frac{1+\alpha}{1+\beta}$ (see slides)

So to have any $\lambda>0$ $\frac{1+\alpha}{1+\beta}$ must be infinite, so $\beta=-1$ i.e., place a zero at $z=-1$. Works for any $0<\alpha\le 1$.

f) SPDS (continuation)





f) SPDS, AND gate, $\delta=0.25$