Systems On-Chip

Lab 5

Backend

Bologna Master Degree in Electrical and Computer Engineering (MEEC)
Instituto Superior Técnico
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1 Introduction

In this laboratory assignment, the tool `innovus` is used to perform **place and route (P&R)** of the battery charger controller which has been worked on in the previous reports. The place and route phase is one of the flow steps necessary to transform a digital circuit RTL description into a GDSII layout representation ready for fabrication submission, which can all be performed using the Cadence Innovus Implementation System. For this purpose, the tutorial "Introduction to innovus Place & Route" was initially repeated in order to implement the place and route typical flow in the `COUNTER4BIT` directory. After that, a similar procedure was applied for the charger controller block, whose LEF file (`file.lef`) had been obtained in the previous laboratory assignment, regarding the frontend deliverable. At the end of this report, an updated LEF file obtained with this new tool is presented.

Throughout this report, multiple files are included and properly commented on. However, due to their considerable quantity, they are also included in the `zip` file delivered in the submission for this laboratory assignment, for easier access. These files are the following:

- `our_innovus` - in which the commands for the whole P&R process are implemented;
- `ccopt_clock_tree_structure.txt` and `ccopt_clock_trees.txt` - to view the results after CTS (clock tree synthesis);
- `BATCHARGERctr_prePlace.summary.gz`, `BATCHARGERctr_preCTS_setup.summary.gz` and `BATCHARGERctr_preCTS_hold.summary.gz`, `BATCHARGERctr_postCTS_setup.summary.gz` and `BATCHARGERctr_postCTS_hold.summary.gz`, `BATCHARGERctr_postRoute_setup.summary.gz` and `BATCHARGERctr_postRoute_hold.summary.gz`, `BATCHARGERctr_SignOff_setup.summary.gz` and `BATCHARGERctr_SignOff_hold.summary.gz` - all included in the `timingReports` sub-directory, relative to **timing analysis** performed in different steps of the P&R process;
- `verify_drc.txt` and `verify_connectivity.txt` - obtained after the nano route implementation;
- `verifyGeometry.txt` - obtained after the filler cells inclusion, to check for possible DRC errors;
- `check_timing.txt` - obtained on sign-off to check if there are timing problems with the constraints and design;
- `checkDesign.txt` - obtained on sign-off to check for any error in the design;
- `BATCHARGERctr.lef` - the updated LEF file automatically generated once all the procedures have been performed.

Additionally, some other significant files obtained in the P&R process are also included in the `zip` file, but not in this report (for different reasons):

- `BATCHARGERctr_synth.v` and `captable.cap` - provided beforehand;
- `BATCHARGERctr.save.io` - file with the pins arrangement;
- `BATCHARGERctr_PG_rings.fp` - in which the design floorplan (FP) was saved (not included in the report due to its considerable size);
- `BATCHARGERctr_pr.v` - which includes the final gate netlist (also a considerably large file);
- `checknetlist.rpt` and `checkPlacement.rpt` - additional files obtained from the `checkDesign -all` command;
- `innovus.log` - the log file originated after running the script `our_innovus`.

2 Place and Route (P&R)

In the third laboratory assignment, scan was added to the charger controller and logic synthesis was performed, from which the gate level controller described in `BATCHARGERctr_synth.v` was obtained. However, while using this file, there were issues in `innovus` regarding the scan chains; because of this, another gate level controller was obtained with the command '`cp /afs/ist.utl.pt/users/6/1/ist13261/public/BATCHARGERctr_synth.v .`'. Additionally, the sub-directory `lef_libs` was included in the previously created `P_and_R` directory - this contains LEF files selected in the menu `file/import design` of `innovus`. Once inside the sub-directory `BATCHARGER`, a proper script is run with the command `source /opt/ic_tools/init/init-innovus20-11-hf000`, after which the tool is initiated with the command `innovus`. By replicating the procedure in the tutorial for the battery charger controller, the actions performed in the graphic interface and the commands given by the command line were copied from the successively generated log files `innovus.cmd`, `innovus.cmd1`, etc. By doing this, the necessary commands can be all executed at once with the developed TCL script `our_innovus` (in which the termination `.tcl` is not necessary), included in Figure 1. Using the command `source our_innovus`, all the results shown throughout this report were obtained. The information contained in this file will therefore be explained alongside the respective process steps.

The first process step is relative to the **floorplan (FP)**, in which Core to IO margins of $3.6\mu\mathrm{m}$ (multiples of $0.4\mu\mathrm{m}$) were selected. The core height (which should be a $3.2\mu\mathrm{m}$ multiple) and the core width (a $0.4\mu\mathrm{m}$ multiple) were defined according to the estimated area obtained in the synthesis of the third laboratory assignment - this will be specified further below, alongside the new LEF file. After this, **global net connections** were performed with `dgnd` and `dvdd`. These two nets had to be added in the newly acquired `BATCHARGERctr_synth.v`, as `inout` parameters, in order to obtain the respective pins in the layout. Having done this, **PG rings** were then added to the design, using `metal1` (odd number metal) for the horizontal direction and `metal2` (even number metal) for the vertical direction. Once **special route** had been performed, all of the pins defined in the gate level controller were properly placed in the layout, according to specific rules which will be discussed alongside the new LEF file (shown in Figure 14). The pins arrangement is saved in `BATCHARGERctr.save.io` (included in the `zip` file), using the command `saveIoFile -locations BATCHARGERctr.save.io`. In this file, it can be confirmed that all the pins were correctly placed in the design in the proper locations defined in the TCL script.

After this, **vertical stripes** connecting the PR rings to inner points of horizontal PG rows were added. For this purpose, the layer `metal4` was used (even number due to the vertical direction). The proper MMMC configuration is performed using the initial commands in `our_innovus`, for which the `BATCHARGERctr.view` file is necessary. The design FP was saved in `BATCHARGERctr_PG_rings.fp`, a lengthy file (not included in the report) which describes aspects such as the placement of pins and global net connections. The following file presented in this report - included in Figure 2 - corresponds to **timing analysis** performed in the pre-Place design phase, in which the gatelist can be almost equal to the synthesis gatelist; therefore, usually there are no timing problems, except if they were inherited from synthesis. This file seems to indicate some violating paths, which cannot be corrected since the gate level controller used in this laboratory assignment was not the one obtained in Lab 3, as mentioned previously. This file also includes values for WNS (worst negative slack) - the difference between the clock period and the delay between a pair of registers; a positive worst case setup time slack means the constraint is met and a negative slack means that the longest path has a path delay longer than the clock period of the circuit. Moreover, values for TNS (total negative slack) - the sum of all negative slacks - are also given. It can be seen that undesired negative values for WNS and TNS - inherited from synthesis - are obtained.

After placing the **standard cell**, the pre-CTS stage was reached, thus a new **timing analysis** (with Setup and Hold) was performed, from which the files included in Figure 3 were obtained. As desired, the WNS values are all positive, design rules violations (DRV) are absent and TNS values are null. For this purpose, **optimization** was required - thus the command `optDesign -preCTS` (in `our_innovus`, shown in Figure 1) implemented before the respective timing analysis.

```
#####################################################
#
#  Innovus Command Logging File
#  Created on Wed Jan  4 11:13:26 2023
#
#####################################################

#@(#)CDS: Innovus v20.11-s130_1 (64bit) 08/05/2020 15:53 (Linux 2.6.32-431.11.2.el6.x86_64)
#@(#)CDS: NanoRoute 20.11-s130_1 NR200802-2257/20_11-UB (database version 18.20.512) {superthreading v2.9}
#@(#)CDS: AAE 20.11-s008 (64bit) 08/05/2020 (Linux 2.6.32-431.11.2.el6.x86_64)
#@(#)CDS: CTE 20.11-s059_1 () Aug  2 2020 05:46:30 ( )
#@(#)CDS: SYNTECH 20.11-s028_1 () Aug  1 2020 06:14:27 ( )
#@(#)CDS: CPE v20.11-s013
#@(#)CDS: IQuantus/TQuantus 19.1.3-s260 (64bit) Thu May 28 10:57:28 PDT 2020 (Linux 2.6.32-431.11.2.el6.x86_64)

set_global _enable_mmmc_by_default_flow      $CTE::mmmc_default
suppressMessage ENCEXT-2799
win
set_global _enable_mmmc_by_default_flow      $CTE::mmmc_default
suppressMessage ENCEXT-2799
win
set_global _enable_mmmc_by_default_flow      $CTE::mmmc_default
suppressMessage ENCEXT-2799
win
set ::TimeLib::tsgMarkCellLatchConstructFlag 1
set conf_qxconf_file NULL
set conf_qxlib_file NULL
set defHierChar /
set delaycal_input_transition_delay 0.1ps
set distributed_client_message_echo 1
set fpIsMaxIoHeight 0
set gpsPrivate::dpgNewAddBufsDBUpdate 1
set gpsPrivate::lsgEnableNewDbApiInRestruct 1
set init_gnd_net dgnd
set init_lef_file {../lef_libs/header8m2t_V55.lef ../lef_libs/fsc0h_d_generic_core.lef ../lef_libs/FSC0H_D_GENERIC_CORE_ANT_V55.lef}
set init_mmmc_file BATCHARGERctr.view
set init_oa_search_lib {}
set init_pwr_net dvdd
set init_verilog BATCHARGERctr_synth.v
set pegDefaultResScaleFactor 1.000000
set pegDetailResScaleFactor 1.000000
set timing_library_float_precision_tol 0.000010
set timing_library_load_pin_cap_indices {}
set tso_post_client_restore_command {update_timing ; write_eco_opt_db ;}
init_design
getIoFlowFlag
setIoFlowFlag 0
floorPlan -site core -s 40 60.8 3.6 3.6 3.6 3.6
uiSetTool select
getIoFlowFlag
fit
clearGlobalNets
globalNetConnect dvdd -type pgpin -pin VCC -instanceBasename *
globalNetConnect dgnd -type pgpin -pin GND -instanceBasename *
set sprCreateIeRingOffset 1.0
set sprCreateIeRingThreshold 1.0
set sprCreateIeRingJogDistance 1.0
set sprCreateIeRingLayers {}
set sprCreateIeRingOffset 1.0
set sprCreateIeRingThreshold 1.0
set sprCreateIeRingJogDistance 1.0
set sprCreateIeRingLayers {}
set sprCreateIeStripeWidth 10.0
set sprCreateIeStripeThreshold 1.0
set sprCreateIeStripeWidth 10.0
set sprCreateIeStripeThreshold 1.0
set sprCreateIeRingOffset 1.0
set sprCreateIeRingThreshold 1.0
set sprCreateIeRingJogDistance 1.0
set sprCreateIeRingLayers {}
set sprCreateIeStripeWidth 10.0
set sprCreateIeStripeThreshold 1.0
setAddRingMode -ring_target default -extend_over_row 0 -ignore_rows 0 -avoid_short 0 -skip_crossing_trunks none -stacked_via_top_layer metal8 -stacked_via_bottom_layer metal1 -
via_using_exact_crossover_size 1 -orthogonal_only true -skip_via_on_pin {  standardcell } -skip_via_on_wire_shape {  noshape }
addRing -nets {dgnd dvdd} -type core_rings -follow core -layer {top metal1 bottom metal1 left metal2 right metal2} -width {top 0.4 bottom 0.4 left 0.4 right 0.4} -spacing {top 0.4 bottom
0.4 left 0.4 right 0.4} -offset {top 1.8 bottom 1.8 left 1.8 right 1.8} -center 1 -threshold 0 -jog_distance 0 -snap_wire_center_to_grid None
setSrouteMode -viaConnectToShape { noshape }
sroute -connect { blockPin padPin padRing corePin floatingStripe } -layerChangeRange { metal1(1) metal8(8) } -blockPinTarget { nearestTarget } -padPinPortConnect { allPort oneGeom } -
padPinTarget { nearestTarget } -corePinTarget { firstAfterRowEnd } -floatingStripeTarget { blockring padring ring stripe ringpin blockpin followpin } -allowJogging 1 -
crossoverViaLayerRange { metal1(1) metal8(8) } -nets { dgnd dvdd } -allowLayerChange 1 -blockPin useLef -targetViaLayerRange { metal1(1) metal8(8) }
getPinAssignMode -pinEditInBatch -quiet
setPinAssignMode -pinEditInBatch true
editPin -pinWidth 0.2 -pinDepth 0.52 -fixOverlap 1 -global_location -unit MICRON -spreadDirection clockwise -side Right -layer 3 -spreadType start -spacing 0.8 -start 47.2 6.0 -pin
{{vbat[7]} {vbat[6]} {vbat[5]} {vbat[4]} {vbat[3]} {vbat[2]} {vbat[1]} {vbat[0]}}
setPinAssignMode -pinEditInBatch false
getPinAssignMode -pinEditInBatch -quiet
setPinAssignMode -pinEditInBatch true
editPin -pinWidth 0.2 -pinDepth 0.52 -fixOverlap 1 -global_location -unit MICRON -spreadDirection clockwise -side Right -layer 3 -spreadType start -spacing 0.8 -start 47.2 12.8 -pin
{{ibat[7]} {ibat[6]} {ibat[5]} {ibat[4]} {ibat[3]} {ibat[2]} {ibat[1]} {ibat[0]}}
setPinAssignMode -pinEditInBatch false
getPinAssignMode -pinEditInBatch -quiet
setPinAssignMode -pinEditInBatch true
editPin -pinWidth 0.2 -pinDepth 0.52 -fixOverlap 1 -global_location -unit MICRON -spreadDirection clockwise -side Right -layer 3 -spreadType start -spacing 0.8 -start 47.2 19.6 -pin
{{tbat[7]} {tbat[6]} {tbat[5]} {tbat[4]} {tbat[3]} {tbat[2]} {tbat[1]} {tbat[0]}}
setPinAssignMode -pinEditInBatch false
getPinAssignMode -pinEditInBatch -quiet
setPinAssignMode -pinEditInBatch true
editPin -pinWidth 0.2 -pinDepth 0.52 -fixOverlap 1 -global_location -unit MICRON -spreadDirection clockwise -side Right -layer 3 -spreadType start -spacing 0.8 -start 47.2 26.4 -pin
{{vcutoff[7]} {vcutoff[6]} {vcutoff[5]} {vcutoff[4]} {vcutoff[3]} {vcutoff[2]} {vcutoff[1]} {vcutoff[0]}}
setPinAssignMode -pinEditInBatch false
getPinAssignMode -pinEditInBatch -quiet
setPinAssignMode -pinEditInBatch true
editPin -pinWidth 0.2 -pinDepth 0.52 -fixOverlap 1 -global_location -unit MICRON -spreadDirection clockwise -side Right -layer 3 -spreadType start -spacing 0.8 -start 47.2 33.2 -pin
{{vpreset[7]} {vpreset[6]} {vpreset[5]} {vpreset[4]} {vpreset[3]} {vpreset[2]} {vpreset[1]} {vpreset[0]}}
setPinAssignMode -pinEditInBatch false
getPinAssignMode -pinEditInBatch -quiet
setPinAssignMode -pinEditInBatch true
editPin -pinWidth 0.2 -pinDepth 0.52 -fixOverlap 1 -global_location -unit MICRON -spreadDirection clockwise -side Right -layer 3 -spreadType start -spacing 0.8 -start 47.2 40.0 -pin
{{tempmin[7]} {tempmin[6]} {tempmin[5]} {tempmin[4]} {tempmin[3]} {tempmin[2]} {tempmin[1]} {tempmin[0]}}
setPinAssignMode -pinEditInBatch false
getPinAssignMode -pinEditInBatch -quiet
setPinAssignMode -pinEditInBatch true
editPin -pinWidth 0.2 -pinDepth 0.52 -fixOverlap 1 -global_location -unit MICRON -spreadDirection clockwise -side Right -layer 3 -spreadType start -spacing 0.8 -start 47.2 46.8 -pin
{{tempmax[7]} {tempmax[6]} {tempmax[5]} {tempmax[4]} {tempmax[3]} {tempmax[2]} {tempmax[1]} {tempmax[0]}}
setPinAssignMode -pinEditInBatch false
getPinAssignMode -pinEditInBatch -quiet
setPinAssignMode -pinEditInBatch true
editPin -pinWidth 0.2 -pinDepth 0.52 -fixOverlap 1 -global_location -unit MICRON -spreadDirection clockwise -side Right -layer 3 -spreadType start -spacing 0.8 -start 47.2 53.6 -pin
{{tmax[7]} {tmax[6]} {tmax[5]} {tmax[4]} {tmax[3]} {tmax[2]} {tmax[1]} {tmax[0]}}
setPinAssignMode -pinEditInBatch false
getPinAssignMode -pinEditInBatch -quiet
setPinAssignMode -pinEditInBatch true
editPin -pinWidth 0.2 -pinDepth 0.52 -fixOverlap 1 -global_location -unit MICRON -spreadDirection clockwise -side Right -layer 3 -spreadType start -spacing 0.8 -start 47.2 60.4 -pin
{{iend[7]} {iend[6]} {iend[5]} {iend[4]} {iend[3]} {iend[2]} {iend[1]} {iend[0]}}
setPinAssignMode -pinEditInBatch false
getPinAssignMode -pinEditInBatch -quiet
setPinAssignMode -pinEditInBatch true
editPin -pinWidth 0.2 -pinDepth 0.52 -fixOverlap 1 -unit MICRON -spreadDirection clockwise -side Bottom -layer 4 -spreadType center -spacing 0.8 -pin clk
editPin -use CLOCK -pinWidth 0.2 -pinDepth 0.52 -fixOverlap 1 -layer 4 -pin clk
setPinAssignMode -pinEditInBatch false
getPinAssignMode -pinEditInBatch -quiet
setPinAssignMode -pinEditInBatch true
editPin -pinWidth 0.2 -pinDepth 0.52 -fixOverlap 1 -global_location -unit MICRON -spreadDirection clockwise -side Left -layer 3 -spreadType start -spacing 0.8 -start 0 20 -pin vtok
setPinAssignMode -pinEditInBatch false
getPinAssignMode -pinEditInBatch -quiet
setPinAssignMode -pinEditInBatch true
editPin -pinWidth 0.2 -pinDepth 0.52 -fixOverlap 1 -global_location -unit MICRON -spreadDirection clockwise -side Left -layer 3 -spreadType start -spacing 0.8 -start 0 22 -pin en
setPinAssignMode -pinEditInBatch false
getPinAssignMode -pinEditInBatch -quiet
setPinAssignMode -pinEditInBatch true
editPin -pinWidth 0.2 -pinDepth 0.52 -fixOverlap 1 -global_location -unit MICRON -spreadDirection clockwise -side Left -layer 3 -spreadType start -spacing 0.8 -start 0 24 -pin rstz
setPinAssignMode -pinEditInBatch false
getPinAssignMode -pinEditInBatch -quiet
setPinAssignMode -pinEditInBatch true
editPin -pinWidth 0.2 -pinDepth 0.52 -fixOverlap 1 -global_location -unit MICRON -spreadDirection clockwise -side Left -layer 3 -spreadType start -spacing 0.8 -start 0 26 -pin cc
setPinAssignMode -pinEditInBatch false
getPinAssignMode -pinEditInBatch -quiet
setPinAssignMode -pinEditInBatch true
editPin -pinWidth 0.2 -pinDepth 0.52 -fixOverlap 1 -global_location -unit MICRON -spreadDirection clockwise -side Left -layer 3 -spreadType start -spacing 0.8 -start 0 28 -pin tc
setPinAssignMode -pinEditInBatch false
getPinAssignMode -pinEditInBatch -quiet
setPinAssignMode -pinEditInBatch true
editPin -pinWidth 0.2 -pinDepth 0.52 -fixOverlap 1 -global_location -unit MICRON -spreadDirection clockwise -side Left -layer 3 -spreadType start -spacing 0.8 -start 0 30 -pin cv
setPinAssignMode -pinEditInBatch false
getPinAssignMode -pinEditInBatch -quiet
setPinAssignMode -pinEditInBatch true
```

```
editPin -pinWidth 0.2 -pinDepth 0.52 -fixOverlap 1 -global_location -unit MICRON -spreadDirection clockwise -side Left -layer 3 -spreadType start -spacing 0.8 -start 0 32 -pin imonen
setPinAssignMode -pinEditInBatch false
getPinAssignMode -pinEditInBatch -quiet
setPinAssignMode -pinEditInBatch true
editPin -pinWidth 0.2 -pinDepth 0.52 -fixOverlap 1 -global_location -unit MICRON -spreadDirection clockwise -side Left -layer 3 -spreadType start -spacing 0.8 -start 0 34 -pin vmonen
setPinAssignMode -pinEditInBatch false
getPinAssignMode -pinEditInBatch -quiet
setPinAssignMode -pinEditInBatch true
editPin -pinWidth 0.2 -pinDepth 0.52 -fixOverlap 1 -global_location -unit MICRON -spreadDirection clockwise -side Left -layer 3 -spreadType start -spacing 0.8 -start 0 36 -pin tmonen
setPinAssignMode -pinEditInBatch false
getPinAssignMode -pinEditInBatch -quiet
setPinAssignMode -pinEditInBatch true
editPin -pinWidth 0.2 -pinDepth 0.52 -fixOverlap 1 -global_location -unit MICRON -spreadDirection clockwise -side Top -layer 4 -spreadType start -spacing 0.8 -start 24 60.8 -pin dvdd
setPinAssignMode -pinEditInBatch false
getPinAssignMode -pinEditInBatch -quiet
setPinAssignMode -pinEditInBatch true
editPin -pinWidth 0.2 -pinDepth 0.52 -fixOverlap 1 -global_location -unit MICRON -spreadDirection clockwise -side Top -layer 4 -spreadType start -spacing 0.8 -start 20 60.8 -pin dgnd
setPinAssignMode -pinEditInBatch false
set sprCreateIeRingOffset 1.0
set sprCreateIeRingThreshold 1.0
set sprCreateIeRingJogDistance 1.0
set sprCreateIeRingLayers {}
set sprCreateIeRingOffset 1.0
set sprCreateIeRingThreshold 1.0
set sprCreateIeRingJogDistance 1.0
set sprCreateIeRingLayers {}
set sprCreateIeStripeWidth 10.0
set sprCreateIeStripeThreshold 1.0
set sprCreateIeStripeWidth 10.0
set sprCreateIeStripeThreshold 1.0
set sprCreateIeRingOffset 1.0
set sprCreateIeRingThreshold 1.0
set sprCreateIeRingJogDistance 1.0
set sprCreateIeRingLayers {}
set sprCreateIeStripeWidth 10.0
set sprCreateIeStripeThreshold 1.0
setAddStripeMode -ignore_block_check false -break_at none -route_over_rows_only false -rows_without_stripes_only false -extend_to_closest_target none -stop_at_last_wire_for_area false -
partial_set_thru_domain false -ignore_nondefault_domains false -trim_antenna_back_to_shape none -spacing_type edge_to_edge -spacing_from_block 0 -stripe_min_length stripe_width -
stacked_via_top_layer metal8 -stacked_via_bottom_layer metal1 -via_using_exact_crossover_size false -split_vias false -orthogonal_only true -allow_jog { padcore_ring  block_ring } -
skip_via_on_pin {  standardcell } -skip_via_on_wire_shape {  noshape  }
addStripe -nets {dgnd dvdd} -layer metal4 -direction vertical -width 1 -spacing 0.4 -set_to_set_distance 100 -start_from right -start_offset 5 -stop_offset 5 -switch_layer_over_obs false -
max_same_layer_jog_length 2 -padcore_ring_top_layer_limit metal8 -padcore_ring_bottom_layer_limit metal1 -block_ring_top_layer_limit metal8 -block_ring_bottom_layer_limit metal1 -
use_wire_group 0 -snap_wire_center_to_grid None
setAddStripeMode -ignore_block_check false -break_at none -route_over_rows_only false -rows_without_stripes_only false -extend_to_closest_target none -stop_at_last_wire_for_area false -
partial_set_thru_domain false -ignore_nondefault_domains false -trim_antenna_back_to_shape none -spacing_type edge_to_edge -spacing_from_block 0 -stripe_min_length stripe_width -
stacked_via_top_layer metal8 -stacked_via_bottom_layer metal1 -via_using_exact_crossover_size false -split_vias false -orthogonal_only true -allow_jog { padcore_ring  block_ring } -
skip_via_on_pin {  standardcell } -skip_via_on_wire_shape {  noshape  }
addStripe -nets {dgnd dvdd} -layer metal4 -direction vertical -width 1 -spacing 0.4 -set_to_set_distance 100 -start_from left -start_offset 5 -stop_offset 5 -switch_layer_over_obs false -
max_same_layer_jog_length 2 -padcore_ring_top_layer_limit metal8 -padcore_ring_bottom_layer_limit metal1 -block_ring_top_layer_limit metal8 -block_ring_bottom_layer_limit metal1 -
use_wire_group 0 -snap_wire_center_to_grid None
set_analysis_view -setup {WC_AN} -hold {BC_AN}
redirect -quiet {set honorDomain [getAnalysisMode -honorClockDomains]} > /dev/null
setPlaceMode -fp false
timeDesign -prePlace -pathReports -drvReports -slackReports -numPaths 50 -prefix BATCHARGERctr_prePlace -outDir timingReports
place_design
optDesign -preCTS
redirect -quiet {set honorDomain [getAnalysisMode -honorClockDomains]} > /dev/null
timeDesign -preCTS -pathReports -drvReports -slackReports -numPaths 50 -prefix BATCHARGERctr_preCTS_setup -outDir timingReports
redirect -quiet {set honorDomain [getAnalysisMode -honorClockDomains]} > /dev/null
timeDesign -preCTS -hold -pathReports -slackReports -numPaths 50 -prefix BATCHARGERctr_preCTS -outDir timingReports
setOptMode -fixCap true -fixTran true -fixFanoutLoad false
ccopt_design
report_ccopt_clock_trees > ccopt_clock_trees.txt
report_ccopt_clock_tree_structure > ccopt_clock_tree_structure.txt
redirect -quiet {set honorDomain [getAnalysisMode -honorClockDomains]} > /dev/null
timeDesign -postCTS -pathReports -drvReports -slackReports -numPaths 50 -prefix BATCHARGERctr_postCTS_setup -outDir timingReports
redirect -quiet {set honorDomain [getAnalysisMode -honorClockDomains]} > /dev/null
timeDesign -postCTS -hold -pathReports -slackReports -numPaths 50 -prefix BATCHARGERctr_postCTS -outDir timingReports
setOptMode -fixCap true -fixTran true -fixFanoutLoad false
optDesign -postCTS
setNanoRouteMode -quiet -timingEngine {}
setNanoRouteMode -quiet -routeTopRoutingLayer default
setNanoRouteMode -quiet -routeBottomRoutingLayer default
setNanoRouteMode -quiet -drouteEndIteration default
setNanoRouteMode -quiet -routeWithTimingDriven false
setNanoRouteMode -quiet -routeWithSiDriven false
routeDesign -globalDetail
redirect -quiet {set honorDomain [getAnalysisMode -honorClockDomains]} > /dev/null
timeDesign -postRoute -pathReports -drvReports -slackReports -numPaths 50 -prefix BATCHARGERctr_postRoute_setup -outDir timingReports
redirect -quiet {set honorDomain [getAnalysisMode -honorClockDomains]} > /dev/null
timeDesign -postRoute -hold -pathReports -slackReports -numPaths 50 -prefix BATCHARGERctr_postRoute -outDir timingReports
setDelayCalMode -engine aae -SIAware true
setAnalysisMode -analysisType onChipVariation -cppr both
setOptMode -fixCap true -fixTran true -fixFanoutLoad false
optDesign -postRoute
getFillerMode -quiet
addFiller -cell FILLER32EHD FILLER2HD FILLER1HD FILLER16EHD -prefix FILLER
redirect -quiet {set honorDomain [getAnalysisMode -honorClockDomains]} > /dev/null
timeDesign -signoff -pathReports -drvReports -slackReports -numPaths 50 -prefix BATCHARGERctr_signOff_setup -outDir timingReports
redirect -quiet {set honorDomain [getAnalysisMode -honorClockDomains]} > /dev/null
timeDesign -signoff -hold -pathReports -slackReports -numPaths 50 -prefix BATCHARGERctr_signOff -outDir timingReports
check_timing -verbose > check_timing.txt
checkDesign -all > checkDesign.txt
saveIoFile -locations BATCHARGERctr.save.io
saveFPlan BATCHARGERctr_PG_rings.fp
verify_drc > verify_drc.txt
verifyGeometry > verifyGeometry.txt
verify_connectivity > verify_connectivity.txt
saveNetlist BATCHARGERctr_pr.v
write_lef_abstract BATCHARGERctr.lef
```

Figure 1: TCL script `our_innovus` that automatically performs the executed P&R of the controller (with the command `source our_innovus`).

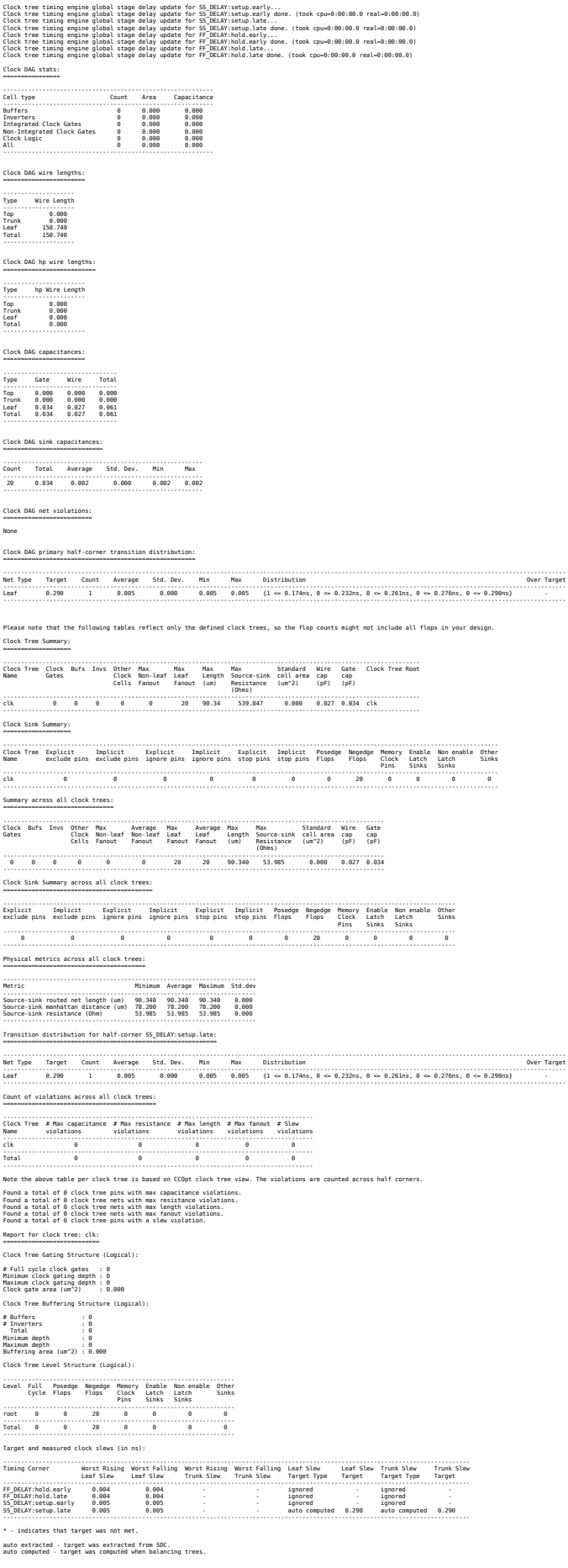
```
#############################################################
#  Generated by:      Cadence Innovus 20.11-s130_1
#  OS:                Linux x86_64(Host ID fatima.novalocal)
#  Generated on:      Sun Jan  8 15:17:47 2023
#  Design:            BATCHARGERctr
#  Command:           timeDesign -prePlace -pathReports -drvReports -slackReports -numPaths 50 -prefix BATCHARGERctr_prePlace -outDir timingReports
#############################################################

------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):| -4.566  | -4.566  |  3.038  |
|           TNS (ns):| -77.617 | -77.617 |  0.000  |
|    Violating Paths:|   17    |   17    |    0    |
|          All Paths:|   40    |   37    |   24    |
+--------------------+---------+---------+---------+

Density: 83.053%
------------------------------------------------------------
```

Figure 2: Pre-Place timing analysis file obtained in `BATCHARGERctr_prePlace.summary.gz`, included in the sub-directory `timingReports`.

```
#############################################################
#  Generated by:      Cadence Innovus 20.11-s130_1
#  OS:                Linux x86_64(Host ID fatima.novalocal)
#  Generated on:      Mon Jan  9 17:51:52 2023
#  Design:            BATCHARGERctr
#  Command:           timeDesign -preCTS -pathReports -drvReports -slackReports -numPaths 50 -prefix BATCHARGERctr_preCTS_setup -outDir timingReports
#############################################################

------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  2.780  |  7.514  |  2.780  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|   40    |   37    |   24    |
+--------------------+---------+---------+---------+

+---------------+-----------------------------+-----------+-----------------+
|               |             Real            |       Total       |
|    DRVs       +-----------------+-----------+-----------------+
|               |  Nr nets(terms) | Worst Vio |  Nr nets(terms) |
+---------------+-----------------+-----------+-----------------+
|   max_cap     |      0 (0)      |   0.000   |      0 (0)      |
|   max_tran    |      0 (0)      |   0.000   |      0 (0)      |
|   max_fanout  |      0 (0)      |     0     |      0 (0)      |
|   max_length  |      0 (0)      |     0     |      0 (0)      |
+---------------+-----------------+-----------+-----------------+

Density: 85.263%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------



#############################################################
#  Generated by:      Cadence Innovus 20.11-s130_1
#  OS:                Linux x86_64(Host ID fatima.novalocal)
#  Generated on:      Mon Jan  9 17:51:54 2023
#  Design:            BATCHARGERctr
#  Command:           timeDesign -preCTS -hold -pathReports -slackReports -numPaths 50 -prefix BATCHARGERctr_preCTS -outDir timingReports
#############################################################

------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

+--------------------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.110  |  0.110  |  4.989  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|   40    |   37    |   24    |
+--------------------+---------+---------+---------+

Density: 85.263%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
```

Figure 3: Pre-CTS timing analysis files obtained in `BATCHARGERctr_preCTS_setup.summary.gz` and `BATCHARGERctr_preCTS_hold.summary.gz` (respectively), included in the sub-directory `timingReports`.

After the previous steps, the **clock tree synthesis (CTS)** phase was reached. To perform it, the command `ccopt_design` was included in `our_innovus` and the results were written in text files using the commands `report_ccopt_clock_trees > ccopt_clock_trees.txt` and `report_ccopt_clock_tree_structure > ccopt_clock_tree_structure.txt`. These files, included in Figures 4 and 5, make it clear that no violations were found and that the clock tree synthesis was correctly performed. In post-CTS, another **timing analysis** was performed, from which (among others) the files `BATCHARGERctr_postCTS_setup.summary` and `BATCHARGERctr_postCTS_hold.summary` (shown in Figure 6) were obtained. It can be seen that no negative setup or hold WNS values were obtained and no DRVs were found - thus, no optimization is needed.



```
Clock tree timing engine global stage delay update for SS_DELAY:setup.early...
Clock tree timing engine global stage delay update for SS_DELAY:setup.early done. (took cpu=0:00:00.0 real=0:00:00.0)
Clock tree timing engine global stage delay update for SS_DELAY:setup.late...
Clock tree timing engine global stage delay update for SS_DELAY:setup.late done. (took cpu=0:00:00.0 real=0:00:00.0)
Clock tree timing engine global stage delay update for FF_DELAY:hold.early...
Clock tree timing engine global stage delay update for FF_DELAY:hold.early done. (took cpu=0:00:00.0 real=0:00:00.0)
Clock tree timing engine global stage delay update for FF_DELAY:hold.late...
Clock tree timing engine global stage delay update for FF_DELAY:hold.late done. (took cpu=0:00:00.0 real=0:00:00.0)

Clock DAG stats:
================

-------------------------------------------------------
Cell type                    Count    Area     Capacitance
-------------------------------------------------------
Buffers                        0      0.000       0.000
Inverters                      0      0.000       0.000
Integrated Clock Gates         0      0.000       0.000
Non-Integrated Clock Gates     0      0.000       0.000
Clock Logic                    0      0.000       0.000
All                            0      0.000       0.000
-------------------------------------------------------


Clock DAG wire lengths:
=======================

--------------------
Type     Wire Length
--------------------
Top         0.000
Trunk       0.000
Leaf      150.740
Total     150.740
--------------------


Clock DAG hp wire lengths:
==========================

------------------------
Type     hp Wire Length
------------------------
Top             0.000
Trunk           0.000
Leaf            0.000
Total           0.000
------------------------


Clock DAG capacitances:
=======================

--------------------------------
Type     Gate     Wire     Total
--------------------------------
Top     0.000    0.000    0.000
Trunk   0.000    0.000    0.000
Leaf    0.034    0.027    0.061
Total   0.034    0.027    0.061
--------------------------------


Clock DAG sink capacitances:
============================

-----------------------------------------------------
Count    Total    Average    Std. Dev.    Min      Max
-----------------------------------------------------
 20      0.034    0.002       0.000       0.002    0.002
-----------------------------------------------------


Clock DAG net violations:
=========================

None


Clock DAG primary half-corner transition distribution:
======================================================

-------------------------------------------------------------------------------------------------------------------------------------------------------
Net Type    Target    Count    Average    Std. Dev.    Min      Max      Distribution                                                                 Over Target
-------------------------------------------------------------------------------------------------------------------------------------------------------
Leaf        0.290       1       0.005       0.000      0.005    0.005    {1 <= 0.174ns, 0 <= 0.232ns, 0 <= 0.261ns, 0 <= 0.276ns, 0 <= 0.290ns}          -
-------------------------------------------------------------------------------------------------------------------------------------------------------


Please note that the following tables reflect only the defined clock trees, so the flop counts might not include all flops in your design.

Clock Tree Summary:
===================

-----------------------------------------------------------------------------------------------------------------------------------------
Clock Tree  Clock  Bufs  Invs  Other  Max        Max     Average  Max     Max          Standard   Wire   Gate   Clock Tree Root
Name        Gates                 Clock  Non-leaf  Leaf    Length  Source-sink  cell area  cap    cap
                                  Cells  Fanout    Fanout  (um)    Resistance   (um^2)     (pF)   (pF)
                                                                   (Ohms)
-----------------------------------------------------------------------------------------------------------------------------------------
clk         0     0     0      0       0         20      90.34    539.847      0.000      0.027  0.034  clk
-----------------------------------------------------------------------------------------------------------------------------------------

Clock Sink Summary:
===================

-----------------------------------------------------------------------------------------------------------------------------------------------
Clock Tree  Explicit     Implicit     Explicit     Implicit     Explicit   Implicit   Posedge  Negedge  Memory  Enable  Non enable  Other
Name        exclude pins  exclude pins  ignore pins  ignore pins  stop pins  stop pins  Flops    Flops    Clock   Latch   Latch       Sinks
                                                                                                      Pins    Sinks   Sinks
-----------------------------------------------------------------------------------------------------------------------------------------------
clk             0            0            0            0          0          0        0       20       0       0         0          0
-----------------------------------------------------------------------------------------------------------------------------------------------

Summary across all clock trees:
===============================

-----------------------------------------------------------------------------------------------------------
Clock  Bufs  Invs  Other  Max        Average  Max     Average  Max     Max          Standard   Wire   Gate
Gates             Clock  Non-leaf   Non-leaf  Leaf    Leaf     Length  Source-sink  cell area  cap    cap
                  Cells  Fanout     Fanout    Fanout  Fanout   (um)    Resistance   (um^2)     (pF)   (pF)
                                                                      (Ohms)
-----------------------------------------------------------------------------------------------------------
 0     0     0      0        0         0        20      20      90.340   53.985       0.000      0.027  0.034
-----------------------------------------------------------------------------------------------------------

Clock Sink Summary across all clock trees:
==========================================

-----------------------------------------------------------------------------------------------------------------------------------------------
Explicit     Implicit     Explicit     Implicit     Explicit   Implicit   Posedge  Negedge  Memory  Enable  Non enable  Other
exclude pins  exclude pins  ignore pins  ignore pins  stop pins  stop pins  Flops    Flops    Clock   Latch   Latch       Sinks
                                                                                          Pins    Sinks   Sinks
-----------------------------------------------------------------------------------------------------------------------------------------------
    0            0            0            0          0          0        0       20       0       0         0          0
-----------------------------------------------------------------------------------------------------------------------------------------------

Physical metrics across all clock trees:
========================================

-----------------------------------------------------------
Metric                                Minimum  Average  Maximum  Std.dev
-----------------------------------------------------------
Source-sink routed net length (um)    90.340   90.340   90.340   0.000
Source-sink manhattan distance (um)   78.200   78.200   78.200   0.000
Source-sink resistance (Ohm)          53.985   53.985   53.985   0.000
-----------------------------------------------------------

Transition distribution for half-corner SS_DELAY:setup.late:
===========================================================

-------------------------------------------------------------------------------------------------------------------------------------------------------
Net Type    Target    Count    Average    Std. Dev.    Min      Max      Distribution                                                                 Over Target
-------------------------------------------------------------------------------------------------------------------------------------------------------
Leaf        0.290       1       0.005       0.000      0.005    0.005    {1 <= 0.174ns, 0 <= 0.232ns, 0 <= 0.261ns, 0 <= 0.276ns, 0 <= 0.290ns}          -
-------------------------------------------------------------------------------------------------------------------------------------------------------

Count of violations across all clock trees:
===========================================

-----------------------------------------------------------------------------------------
Clock Tree  # Max capacitance  # Max resistance  # Max length  # Max fanout  # Slew
Name        violations         violations       violations    violations   violations
-----------------------------------------------------------------------------------------
clk                0                  0               0             0            0
-----------------------------------------------------------------------------------------
Total              0                  0               0             0            0
-----------------------------------------------------------------------------------------

Note the above table per clock tree is based on CCOpt clock tree view. The violations are counted across half corners.

Found a total of 0 clock tree pins with max capacitance violations.
Found a total of 0 clock tree nets with max resistance violations.
Found a total of 0 clock tree nets with max length violations.
Found a total of 0 clock tree nets with max fanout violations.
Found a total of 0 clock tree pins with a slew violation.

Report for clock tree: clk:
===========================

Clock Tree Gating Structure (Logical):

# Full cycle clock gates  : 0
Minimum clock gating depth : 0
Maximum clock gating depth : 0
Clock gate area (um^2)     : 0.000

Clock Tree Buffering Structure (Logical):

# Buffers            : 0
# Inverters          : 0
  Total              : 0
Minimum depth        : 0
Maximum depth        : 0
Buffering area (um^2) : 0.000

Clock Tree Level Structure (Logical):

-----------------------------------------------------------------
Level  Full  Posedge  Negedge  Memory  Enable  Non enable  Other
       Cycle  Flops    Flops    Clock   Latch   Latch       Sinks
                               Pins    Sinks   Sinks
-----------------------------------------------------------------
root     0      0        20       0       0         0          0
-----------------------------------------------------------------
Total    0      0        20       0       0         0          0
-----------------------------------------------------------------

Target and measured clock slews (in ns):

-----------------------------------------------------------------------------------------------------------------------------------------------------------
Timing Corner         Worst Rising  Worst Falling  Worst Rising  Worst Falling  Leaf Slew      Leaf Slew  Trunk Slew     Trunk Slew
                      Leaf Slew     Leaf Slew      Trunk Slew    Trunk Slew     Target Type    Target     Target Type    Target
-----------------------------------------------------------------------------------------------------------------------------------------------------------
FF_DELAY:hold.early     0.004         0.004          -             -          ignored          -        ignored          -
FF_DELAY:hold.late      0.004         0.004          -             -          ignored          -        ignored          -
SS_DELAY:setup.early    0.005         0.005          -             -          ignored          -        ignored          -
SS_DELAY:setup.late     0.005         0.005          -             -          auto computed  0.290      auto computed  0.290
-----------------------------------------------------------------------------------------------------------------------------------------------------------

* - indicates that target was not met.

auto extracted - target was extracted from SDC.
auto computed - target was computed when balancing trees.
```

Figure 4: CTS results obtained with the command `report_ccopt_clock_trees`.

```
Clock tree clk:
 Total FF: 20
 Max Level: 2
  (L1) output port clk
   \_ ... (20 sinks omitted)
```

Figure 5: CTS results obtained with the command `report_ccopt_clock_tree_structure`.

```
#############################################################
#  Generated by:      Cadence Innovus 20.11-s130_1
#  OS:                Linux x86_64(Host ID fatima.novalocal)
#  Generated on:      Mon Jan  9 17:52:50 2023
#  Design:            BATCHARGERctr
#  Command:           timeDesign -postCTS -pathReports -drvReports -slackReports -numPaths 50 -prefix BATCHARGERctr_postCTS_setup -outDir timingReports
#############################################################

------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

+--------------------+--------+--------+---------+
|     Setup mode     |   all  | reg2reg | default |
+--------------------+--------+--------+---------+
|           WNS (ns):|  2.775 |  7.519 |  2.775  |
|           TNS (ns):|  0.000 |  0.000 |  0.000  |
|    Violating Paths:|    0   |    0   |    0    |
|          All Paths:|   40   |   37   |   24    |
+--------------------+--------+--------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +---------------+---------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+---------------+---------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+---------------+---------------+------------------+

Density: 85.263%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
```

```
#############################################################
#  Generated by:      Cadence Innovus 20.11-s130_1
#  OS:                Linux x86_64(Host ID fatima.novalocal)
#  Generated on:      Mon Jan  9 17:52:52 2023
#  Design:            BATCHARGERctr
#  Command:           timeDesign -postCTS -hold -pathReports -slackReports -numPaths 50 -prefix BATCHARGERctr_postCTS -outDir timingReports
#############################################################

------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

+--------------------+--------+--------+---------+
|     Hold mode      |   all  | reg2reg | default |
+--------------------+--------+--------+---------+
|           WNS (ns):|  0.109 |  0.109 |  4.988  |
|           TNS (ns):|  0.000 |  0.000 |  0.000  |
|    Violating Paths:|    0   |    0   |    0    |
|          All Paths:|   40   |   37   |   24    |
+--------------------+--------+--------+---------+

Density: 85.263%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
```

Figure 6: Post-CTS timing analysis files obtained in `BATCHARGERctr_postCTS_setup.summary.gz` and `BATCHARGERctr_postCTS_hold.summary.gz` (respectively), included in the sub-directory `timingReports`.

Regarding **nano route**, the post-Route **timing analysis** files shown in Figure 7 once again indicate no negative WNS values and no DRVs, thus no optimization is required. Having added the filler cells (which will fill the core empty space and help biasing n-well and p-well on empty space), the **sign-off** stage - in which the design is almost ready for fabrication - was reached and a new timing analysis was performed. Once again, no negative WNS values and no DRVs were found. The final gate netlist was then obtained with `saveNetlist BATCHAGERctr_pr.v` - the resulting file is included in the submitted `zip`.

Having completed all P&R so far, several other analyses were performed. The commands `verify_drc > verify_drc.txt`, `verify_connectivity > verify_connectivity.txt`, `verifyGeometry > verifyGeometry.txt`, `check_timing -verbose > check_timing.txt` and `checkDesign -all > checkDesign.txt` led to the files shown in Figures 9 to 13, which indicate that the place and route of the charger controller was successfully executed.

```
#############################################################
#  Generated by:      Cadence Innovus 20.11-s130_1
#  OS:                Linux x86_64(Host ID fatima.novalocal)
#  Generated on:      Mon Jan  9 17:53:50 2023
#  Design:            BATCHARGERctr
#  Command:           timeDesign -postRoute -pathReports -drvReports -slackReports -numPaths 50 -prefix BATCHARGERctr_postRoute_setup -outDir timingReports
#############################################################

------------------------------------------------------------
         timeDesign Summary
------------------------------------------------------------

+--------------------+--------+---------+---------+
|     Setup mode     |   all  | reg2reg | default |
+--------------------+--------+---------+---------+
|           WNS (ns):|  2.745 |  7.413  |  2.745  |
|           TNS (ns):|  0.000 |  0.000  |  0.000  |
|    Violating Paths:|    0   |    0    |    0    |
|          All Paths:|   40   |   37    |   24    |
+--------------------+--------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +---------------+---------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+---------------+---------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+---------------+---------------+------------------+

Density: 85.263%
Total number of glitch violations: 0
------------------------------------------------------------



#############################################################
#  Generated by:      Cadence Innovus 20.11-s130_1
#  OS:                Linux x86_64(Host ID fatima.novalocal)
#  Generated on:      Mon Jan  9 17:53:54 2023
#  Design:            BATCHARGERctr
#  Command:           timeDesign -postRoute -hold -pathReports -slackReports -numPaths 50 -prefix BATCHARGERctr_postRoute -outDir timingReports
#############################################################

------------------------------------------------------------
         timeDesign Summary
------------------------------------------------------------

+--------------------+--------+---------+---------+
|     Hold mode      |   all  | reg2reg | default |
+--------------------+--------+---------+---------+
|           WNS (ns):|  0.108 |  0.108  |  4.988  |
|           TNS (ns):|  0.000 |  0.000  |  0.000  |
|    Violating Paths:|    0   |    0    |    0    |
|          All Paths:|   40   |   37    |   24    |
+--------------------+--------+---------+---------+

Density: 85.263%
------------------------------------------------------------
```

Figure 7: Post-route timing analysis files obtained in `BATCHARGERctr_postroute_setup.summary.gz` and `BATCHARGERctr_postroute_hold.summary.gz` (respectively), included in the sub-directory `timingReports`.

```
#############################################################
#  Generated by:      Cadence Innovus 20.11-s130_1
#  OS:                Linux x86_64(Host ID fatima.novalocal)
#  Generated on:      Mon Jan  9 17:54:26 2023
#  Design:            BATCHARGERctr
#  Command:           timeDesign -signoff -pathReports -drvReports -slackReports -numPaths 50 -prefix BATCHARGERctr_signOff_setup -outDir timingReports
#############################################################

------------------------------------------------------------
         timeDesign Summary
------------------------------------------------------------

+--------------------+--------+---------+---------+
|     Setup mode     |   all  | reg2reg | default |
+--------------------+--------+---------+---------+
|           WNS (ns):|  2.771 |  7.534  |  2.771  |
|           TNS (ns):|  0.000 |  0.000  |  0.000  |
|    Violating Paths:|    0   |    0    |    0    |
|          All Paths:|   40   |   37    |   24    |
+--------------------+--------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +---------------+---------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+---------------+---------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+---------------+---------------+------------------+

Density: 85.263%
       (100.000% with Fillers)
Total number of glitch violations: 0
------------------------------------------------------------



#############################################################
#  Generated by:      Cadence Innovus 20.11-s130_1
#  OS:                Linux x86_64(Host ID fatima.novalocal)
#  Generated on:      Mon Jan  9 17:54:35 2023
#  Design:            BATCHARGERctr
#  Command:           timeDesign -signoff -hold -pathReports -slackReports -numPaths 50 -prefix BATCHARGERctr_signOff -outDir timingReports
#############################################################

------------------------------------------------------------
         timeDesign Summary
------------------------------------------------------------

+--------------------+--------+---------+---------+
|     Hold mode      |   all  | reg2reg | default |
+--------------------+--------+---------+---------+
|           WNS (ns):|  0.108 |  0.108  |  4.988  |
|           TNS (ns):|  0.000 |  0.000  |  0.000  |
|    Violating Paths:|    0   |    0    |    0    |
|          All Paths:|   40   |   37    |   24    |
+--------------------+--------+---------+---------+

Density: 85.263%
       (100.000% with Fillers)
------------------------------------------------------------
```

Figure 8: Sign-off timing analysis files obtained in `BATCHARGERctr_SignOff_setup.summary.gz` and `BATCHARGERctr_SignOff_hold.summary.gz` (respectively), included in the sub-directory `timingReports`.

```
*** Starting Verify DRC (MEM: 2037.6) ***

 VERIFY DRC ..... Starting Verification
 VERIFY DRC ..... Initializing
 VERIFY DRC ..... Deleting Existing Violations
 VERIFY DRC ..... Creating Sub-Areas
 VERIFY DRC ..... Using new threading
 VERIFY DRC ..... Sub-Area: {0.000 0.000 47.200 68.000} 1 of 1
 VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.

 Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.1  ELAPSED TIME: 0.00  MEM: 0.0M) ***
```

Figure 9: Analysis results obtained with the command `verify_drc`.

```
VERIFY_CONNECTIVITY use new engine.

******** Start: VERIFY CONNECTIVITY ********
Start Time: Sun Jan  8 15:21:40 2023

Design Name: BATCHARGERctr
Database Units: 1000
Design Boundary: (0.0000, 0.0000) (47.2000, 68.0000)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Sun Jan  8 15:21:40 2023
Time Elapsed: 0:00:00.0

******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:00.0  MEM: 0.000M)
```

Figure 10: Analysis results obtained with the command `verify_connectivity`.

```
 *** Starting Verify Geometry (MEM: 2049.0) ***

**WARN: (IMPVFG-257):   setVerifyGeometryMode/verifyGeometry command is obsolete and should not be used any more. It still works in this release but will be removed in future release. You
should change to use set_verify_drc_mode/verify_drc which is the replacement tool for verifyGeometry.
  VERIFY GEOMETRY ..... Starting Verification
  VERIFY GEOMETRY ..... Initializing
  VERIFY GEOMETRY ..... Deleting Existing Violations
  VERIFY GEOMETRY ..... Creating Sub-Areas
                  ..... bin size: 3600
  VERIFY GEOMETRY ..... SubArea : 1 of 1
  VERIFY GEOMETRY ..... Cells          :  0 Viols.
  VERIFY GEOMETRY ..... SameNet        :  0 Viols.
  VERIFY GEOMETRY ..... Wiring         :  0 Viols.
  VERIFY GEOMETRY ..... Antenna        :  0 Viols.
VG: elapsed time: 1.00
Begin Summary ...
  Cells       : 0
  SameNet     : 0
  Wiring      : 0
  Antenna     : 0
  Short       : 0
  Overlap     : 0
End Summary

  Verification Complete : 0 Viols.  0 Wrngs.

**********End: VERIFY GEOMETRY**********
 *** verify geometry (CPU: 0:00:00.6  MEM: 78.9M)
```

Figure 11: Analysis results obtained with the command `verifyGeometry`.

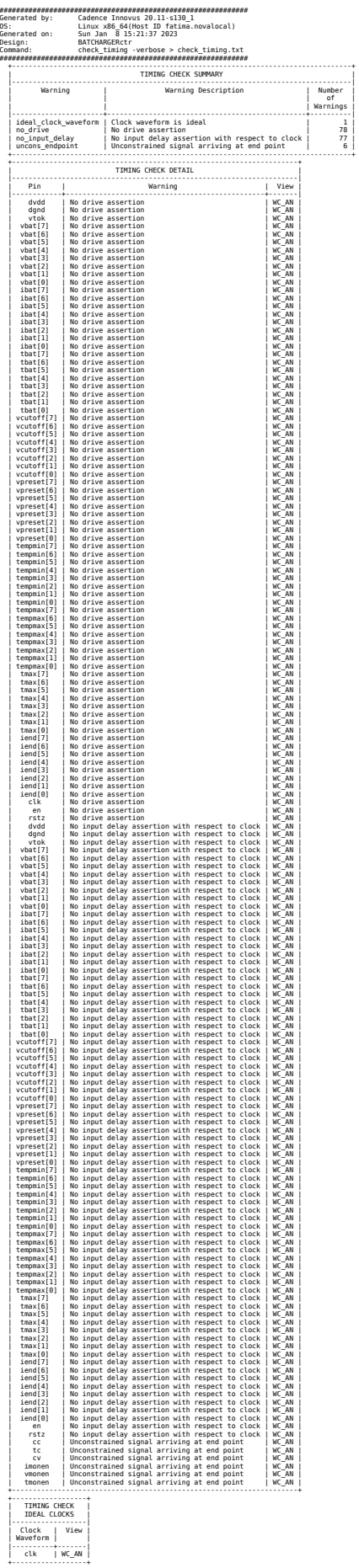


Figure 12: Analysis results obtained with the command `check_timing -verbose`.

```
Begin checking placement ... (start mem=2005.6M, init mem=2037.6M)
*info: Recommended don't use cell = 0
*info: Placed = 369
*info: Unplaced = 0
Placement Density:100.00%(2432/2432)
Placement Density (including fixed std cells):100.00%(2432/2432)
Finished checkPlace (total: cpu=0:00:00.1, real=0:00:00.0; vio checks: cpu=0:00:00.0, real=0:00:00.0; mem=2037.6M)
############################################################################
# Innovus Netlist Design Rule Check
# Sun Jan  8 15:21:40 2023

############################################################################
Design: BATCHARGERctr

------ Design Summary:
Total Standard Cell Number   (cells) : 369
Total Block Cell Number      (cells) : 0
Total I/O Pad Cell Number    (cells) : 0
Total Standard Cell Area     ( um^2) : 2432.00
Total Block Cell Area        ( um^2) : 0.00
Total I/O Pad Cell Area      ( um^2) : 0.00

------ Design Statistics:

Number of Instances            : 369
Number of Non-uniquified Insts : 351
Number of Nets                 : 305
Average number of Pins per Net : 2.77
Maximum number of Pins in Net  : 21

------ I/O Port summary

Number of Primary I/O Ports    : 84
Number of Input Ports          : 76
Number of Output Ports         : 6
Number of Bidirectional Ports  : 2
Number of Power/Ground Ports   : 0
Number of Floating Ports                    *: 2
Number of Ports Connected to Multiple Pads   *: 0
Number of Ports Connected to Core Instances   : 82
**WARN: (IMPREPO-200):  There are 2 Floating Ports in the top design.
**WARN: (IMPREPO-202):  There are 82 Ports connected to core instances.

------ Design Rule Checking:

Number of Output Pins connect to Power/Ground *: 0
Number of Insts with Input Pins tied together ?: 10
Number of TieHi/Lo term nets not connected to instance's PG terms ?: 0
Number of Input/InOut Floating Pins            : 0
Number of Output Floating Pins                 : 0
Number of Output Term Marked TieHi/Lo         *: 0

**WARN: (IMPREPO-216):  There are 10 Instances with input pins tied together.
Number of nets with tri-state drivers          : 0
Number of nets with parallel drivers           : 0
Number of nets with multiple drivers           : 0
Number of nets with no driver (No FanIn)       : 0
Number of Output Floating nets (No FanOut)     : 20
Number of High Fanout nets (>50)               : 0
**WARN: (IMPREPO-212):  There are 2 Floating I/O Pins.
**WARN: (IMPREPO-213):  There are 82 I/O Pins connected to Non-IO Insts.
Checking for any assigns in the netlist...
  No assigns found.
Checking routing tracks.....
Checking other grids.....
Checking FINFET Grid is on Manufacture Grid.....

Checking core/die box is on Grid.....

Checking snap rule ......

Checking Row is on grid......

Checking AreaIO row.....
Checking routing blockage.....
Checking components.....
Checking constraints (guide/region/fence).....
Checking groups.....
Checking Ptn Core Box.....

Checking Preroutes.....
No. of regular pre-routes not on tracks : 0
 Design check done.
Report saved in file checkDesign/BATCHARGERctr.main.htm.ascii

*** Summary of all messages that are not suppressed in this session:
Severity  ID               Count  Summary
WARNING   IMPREPO-200          1  There are %d Floating Ports in the top d...
WARNING   IMPREPO-202          1  There are %d Ports connected to core ins...
WARNING   IMPREPO-212          1  There are %d Floating I/O Pins.
WARNING   IMPREPO-213          1  There are %d I/O Pins connected to Non-I...
WARNING   IMPREPO-216          1  There are %d Instances with input pins t...
*** Message Summary: 5 warning(s), 0 error(s)
```

Figure 13: Analysis results obtained with the command `checkDesign -all`.

2.1 Updated LEF file and layout

In the script `our_innovus`, the final command line `write_lef_abstract BATCHARGERctr.lef` leads to the creation of the **LEF file** shown in Figure 14. By running this script, the **layout** shown in Figure 15 is obtained. Some relevant comments regarding these files - such as changes from the LEF file obtained in the previous laboratory assignment - are worth pointing out. Firstly, it is worth noting that the names designated for the metal layers changed from the previous laboratory assignment (i.e., ME1, ME2, etc.) - in which Cadence Virtuoso was used - to this one, in which Cadence Innovus is utilized - now, the respective layers are named `metal1`, `metal2`, etc. In practical applications in which working with the two softwares is necessary, these layer names could have to be changed when transposing from one tool to the other. Regarding the pins, most of them are digital, thus the lines `USE SIGNAL` included in the LEF file. The exceptions are `dvdd` (Power) and `dgnd` (Ground). They are also defined as inputs, outputs or input-outputs according to the information in `BATCHARGERctr_synth.v` - this is also clearly distinguishable in the layout. The pins `si`, `se` and `so` are not included now, since a new `BATCHARGERctr_synth.v` file was used, as mentioned before. The relative position of the pins were also mostly changed from the previous LEF file - for example, most signals are now placed on the right side of the layout, for no reason in particular.

On the top of the layout, the pins `dgnd` and `dvdd` were included on tracks. Since pins must be spaced apart in multiples of $0.4\mu\mathrm{m}$, they were placed in x-axis values of 20 and 24, respectively. Additionally, together with `clk`, which was put on the bottom of the layout, the layer `metal4` was selected for these pins, since even metals must be used for vertical pins. Contrarily, `metal3` was used for all other pins, which were placed on the left or right hand sides (horizontal pins). In particular, the pins of the left side (`vtok`, `en`, `rstz`, `cc`, `tc`, `cv`, `imonen`, `vmonen` and `tmonen`, from bottom to top) were placed $2\mu\mathrm{m}$ from each other (since $2\mu m$ is a multiple of $0.4\mu\mathrm{m}$). As for the other pins, the different bits for a specific parameter (i.e., `vbat`, `ibat`, `tbat`, `vcutoff`, `vpreset`, `tempmin`, `tempmax`, `tmax` and `iend`, from bottom to top) were distanced $0.8\mu\mathrm{m}$ from each other; however, a spacing of $1.2\mu\mathrm{m}$ was used for consecutive bits of different parameters (for instance, between `vbat[7]` and `ibat[0]`). The y-axis values of the coordinates were selected in `our_innovus` taking into account the pin widths of $0.2\mu\mathrm{m}$ used in this layout.

Regarding the size of the cell, an estimated area of $2016\mu\mathrm{m}^2$ had been obtained in Lab 3 (although, for a different synthesized controller). A 20% increase in area was then considered in Lab 4, already taking the clock tree into account, thus a width of 28.5 and a height of 85.0 had been used. In this case, however, it is important to note that the core height should be a $3.2\mu\mathrm{m}$ multiple and the core width a $0.4\mu\mathrm{m}$ multiple. Thus, a width of 40 and a height of 60.8 were now used (leading to a similar area as before). Due to the core to IO margins of $3.6\mu\mathrm{m}$, the values of 47.2 and 68.0 are indicated in the updated LEF file.

As shown in Figure 15, it can also be seen that, in terms of the PG rings, `metal1` (odd number metal layer) was used for the horizontal direction, whereas `metal2` was used for the vertical direction. Additionally, the vertical stripes were defined in `metal4`. As seen on the top of the layout, the proper connections `dvdd-VCC` and `dgnd-GND` were implemented through vias.

3 Conclusion

In this laboratory assignment, the design flow of **backend** place and route (P&R) has been successfully performed for the battery charger controller and an updated LEF file was obtained with the `innovus` tool. For this purpose, a TCL script that automatically performs the executed P&R - import design, define floorplan, place pins, power planning and interconnections, place, clock tree synthesis (CTS), nano route and add filler cells - was used. In each stage pre-Place, pre-CTS, post-CTS, post-Route and sign-off of the design flow, timing analysis is performed, having optimization been required in pre-CTS. Additional reports were performed and indicated that no errors or violations were found.

Figure 14: Updated LEF file `BATCHARGERctr.lef` obtained with `innovus`.

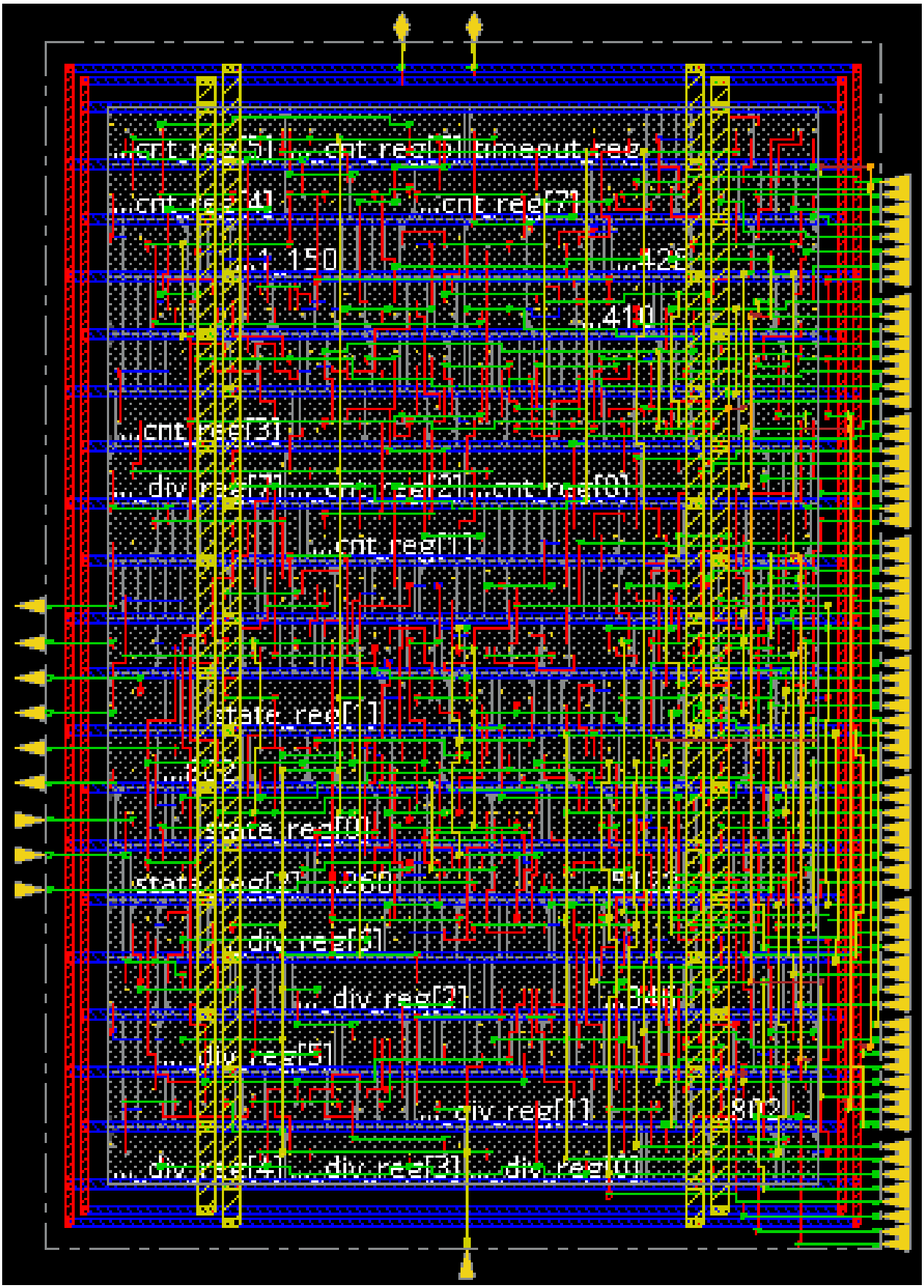


Figure 15: Screenshot of the charger controller layout implemented with `innovus`.