TÉCNICO LISBOA

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Operational Amplifier

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Contents

1 Introduction

The objective of this work is to design and simulate a one-stage **operational amplifier (OPAMP)**, in which the differential stage circuit consists of a PMOS differential pair biased by a current source. For this purpose, the technology C35B4C3 CMOS from Austria Micro Systems is used in Cadence Virtuoso. Once the schematic is built, the dimensions of the transistors in the circuit are properly selected in order to have the desired differential mode gain of 36 dB at low frequencies, along with a current of 0.7 mA in the differential pair, an output common-mode voltage of 1.5 V, a supply voltage of 3.0 V and a maximum total supply current of 5 mA. After confirming these results, the other characteristics of the OPAMP implementation are determined with DC, AC and transient simulations. Finally, once the layout of the circuit is designed and verified with DRC and LVS validations, its behaviour is simulated using an extracted view with the respective parasitic capacitors.

2 OPAMP schematic

The final pre-layout schematic of the circuit is shown in Fig. 1, in which `nmos4` and `pmos4` transistors were used, along with an `rpolyh` resistor - every component from the `PRIMLIB` library. This resistor cell was used in this schematic since it allows for higher resistance values. The current in the differential pair is fed by a current mirror (with transistors `MP4` and `MP5`) and the resistance `R0`. However, in order to determine the dimensions of the other transistors beforehand, an ideal current source `idc` was initially used to provide a current of 700 µA to the differential pair. Having obtained the desired differential gain at low frequency of 36 dB and a DC output node voltage of 1.5 V, the current source was replaced with the previously mentioned components, in order to maintain the same current in the differential pair and DC node voltage in the source of transistors `MP0` and `MP1`. The dimensions of all the components in the circuit are shown in Tab. 1. In the initial simulations, a single gate was used in each transistor. However, while designing the layout, the number of gates and the dimensions of the resistor were altered in order to minimize the occupied area. The results shown in Sec. 2 were obtained with the pre-layout characteristics.

Table 1: Dimensions of the transistors and resistor used in the OPAMP schematic.

Transistor	**Channel width, W [µm]**	**Channel length, L [µm]**	**Number of gates (post-layout)**
`MP0/MP1`	40	0.35	5
`MN0/MN1`	40	1.45	5
`MP2/MP3`	25	0.8	5
`MN2/MN3`	40	1.3	4
`MP4`	150	0.35	10
`MP5`	45	0.35	5

Resistor	**Width, W [µm]**	**Length, L [µm]**	**Resistance value [Ω]**
`R0`	10	65	7959.184
`R0` (post-layout)	5.05	32.15	7954.639

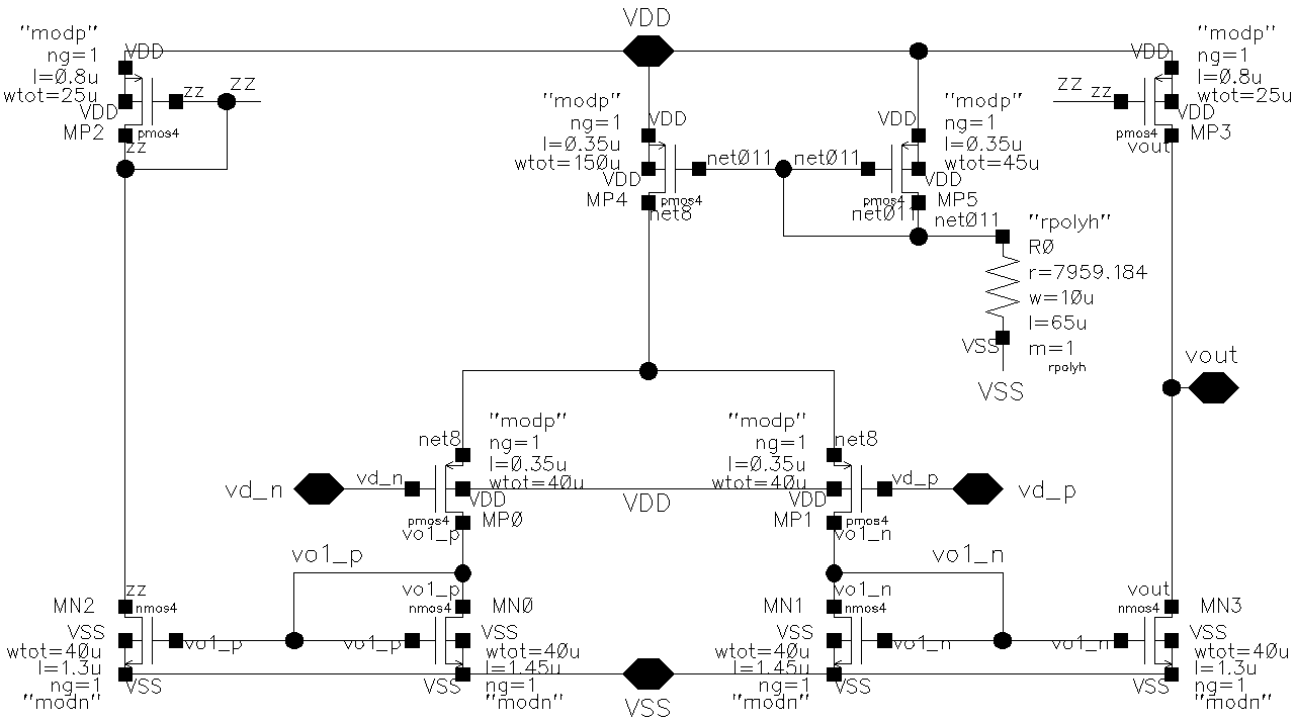

Figure 1: Schematic of the operational amplifier included in the testbench.

Having properly designed the circuit, its symbol cellview was included in the testbench shown in Fig. 2. Besides the voltage sources connected to `VDD` and `VSS`, the current source `I1` in the output corresponds to an open circuit in DC simulations, but it allows the inclusion of an AC component in the output. A similar AC component can be added to all the other sources, which also include the inputs of the differential pair. By varying the characteristics of the voltage sources and the type of analysis, the values of the different parameters indicated in Tab. 2 can be directly obtained. These include the differential mode and common-mode gains (A_d and A_s, respectively) and input impedances (Z_{id} and Z_{ic}, respectively), output impedance (Z_{out}), input offset voltage (V_{OS}), undesired differential mode gains (A^+ and A^-) and slew-rate (SR).

Table 2: Simulations to be run with the OPAMP testbench.

Results	**Simulation**	$\mathbf{v_+, v_-}$	$\mathbf{v_{CM}}$	$\mathbf{v_{DD}}$	$\mathbf{v_{SS}}$	$\mathbf{i_0}$
$\mathbf{A_d, Z_{id}}$	ac	ac	dc	dc	dc	0
$\mathbf{A_c, Z_{ic}}$	ac	0	dc+ac	dc	dc	0
$\mathbf{Z_{out}}$	ac	0	dc	dc	dc	ac
$\mathbf{V_{OS}}$	dc	dc	dc	dc	dc	0
$\mathbf{A^+}$	ac	0	dc	dc+ac	dc	0
$\mathbf{A^-}$	ac	0	dc	dc	dc+ac	0
SR	tran	pulse	dc	dc	dc	0

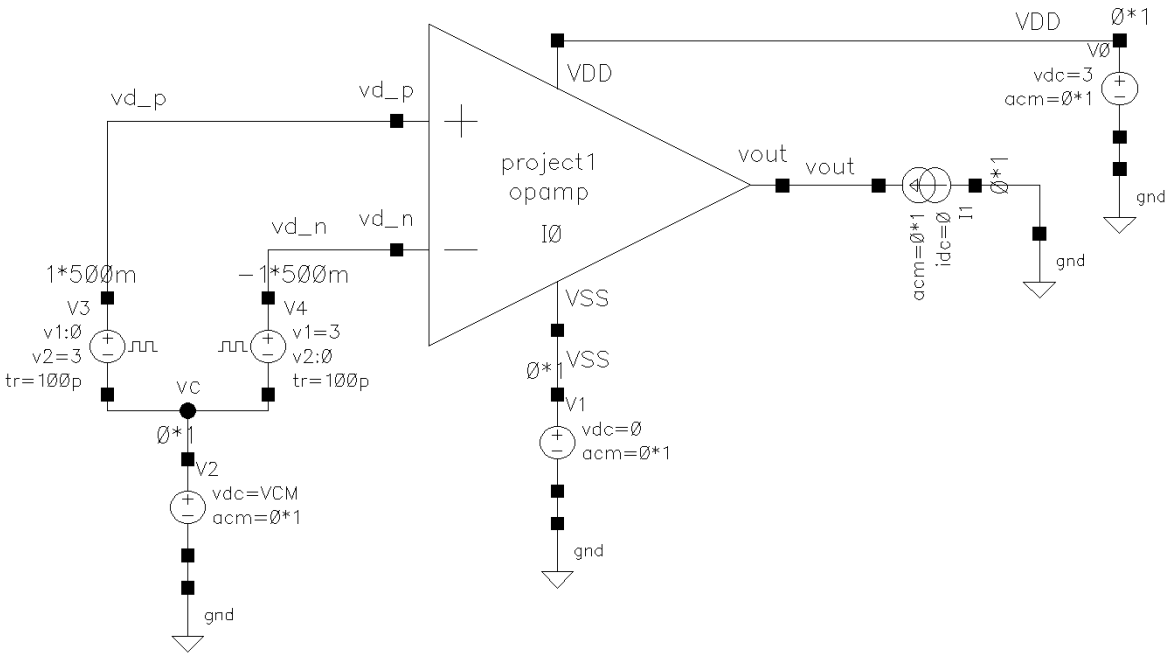

Figure 2: Testbench cellview used for simulation purposes.

2.1 Bias point simulation

Using the previously mentioned dimensions for the circuit components, the DC node voltage and DC operating point results shown in Tabs. 3 and 4 and Fig. 3 were obtained.

Firstly, it can be observed that the output voltage value is extremely close to the desired 1.5 V. For instance, in order to increase this value along the circuit design procedure, the most significant alterations occurred when the channel length and channel width of the transistors in the output (`MP2/MP3` and `MN2/MN3`) and the NMOS transistors in the differential pair (`MN0/MN1`) were changed. The current in a PMOS/NMOS transistor in the saturation region is given by

$$I_{S/D} = \frac{1}{2}\mu_{n/p}C_{ox}\frac{W}{L}(V_{SG/GS} - V_{th_{n/p}})^2(1 + \lambda_{n/p}V_{SD/DS}) \tag{1}$$

But the effect of channel length modulation (described by the parameter λ) is generally less significant, due to the sufficiently high channel length values used in most transistors. If the ratio W/L changes, the voltage drop V_{GS} (for NMOS transistors) or V_{SG} (for PMOS transistors) will therefore be altered for a certain current value. Consequently, in order to increase the DC voltage at the output node (V_{out}), the ratio W/L for transistors `MP2/MP3` can be increased - this lowers the respective V_{SG}, thus increasing V_G - the voltage at node `zz` indicated in Fig. 3. Because the circuit is symmetrical and the gate of transistor `MP2` is connected to its drain, the voltage value at `vout` is the same as this gate voltage. Similarly, decreasing W/L in these PMOS transistors leads to an decrease in V_{out}.

Similar changes in V_{out} occur when the ratio W/L for transistors `MN0/MN1` is altered - i.e., an increase in this ratio leads to an increase in the node voltage, and vice-versa. When W/L in `MN0` increases, V_{GS} decreases in order to have the same current, therefore leading to a lower gate voltage and a lower current in transistor `MN2` - because the ratio W/L did not change in the latter, I_D must

decrease, according to (1). Consequently, V_{SG} in `MP2` decreases, which increases the gate voltage of this transistor (equal to V_{out}). Finally, changing the aforementioned ratio for the NMOS transistors `MN2/MN3` leads to the opposite changes in V_{out} - that is, increasing the former leads to a decrease in the output voltage. This is because, by increasing W/L, the current also increases (while V_{GS} remains the same), which in turn decreases the gate voltage in `MP2`.

Most of these changes in the transistors lead to opposite results in the value of the differential mode gain (A_d), therefore the changes made to obtain a certain V_{out} value must be conjugated with the desired gain of 36 dB. The only exception verified experimentally occurs when the value of L for transistors `MN2/MN3` is changed, since its increase leads to similar modifications in both A_d and V_{out}.

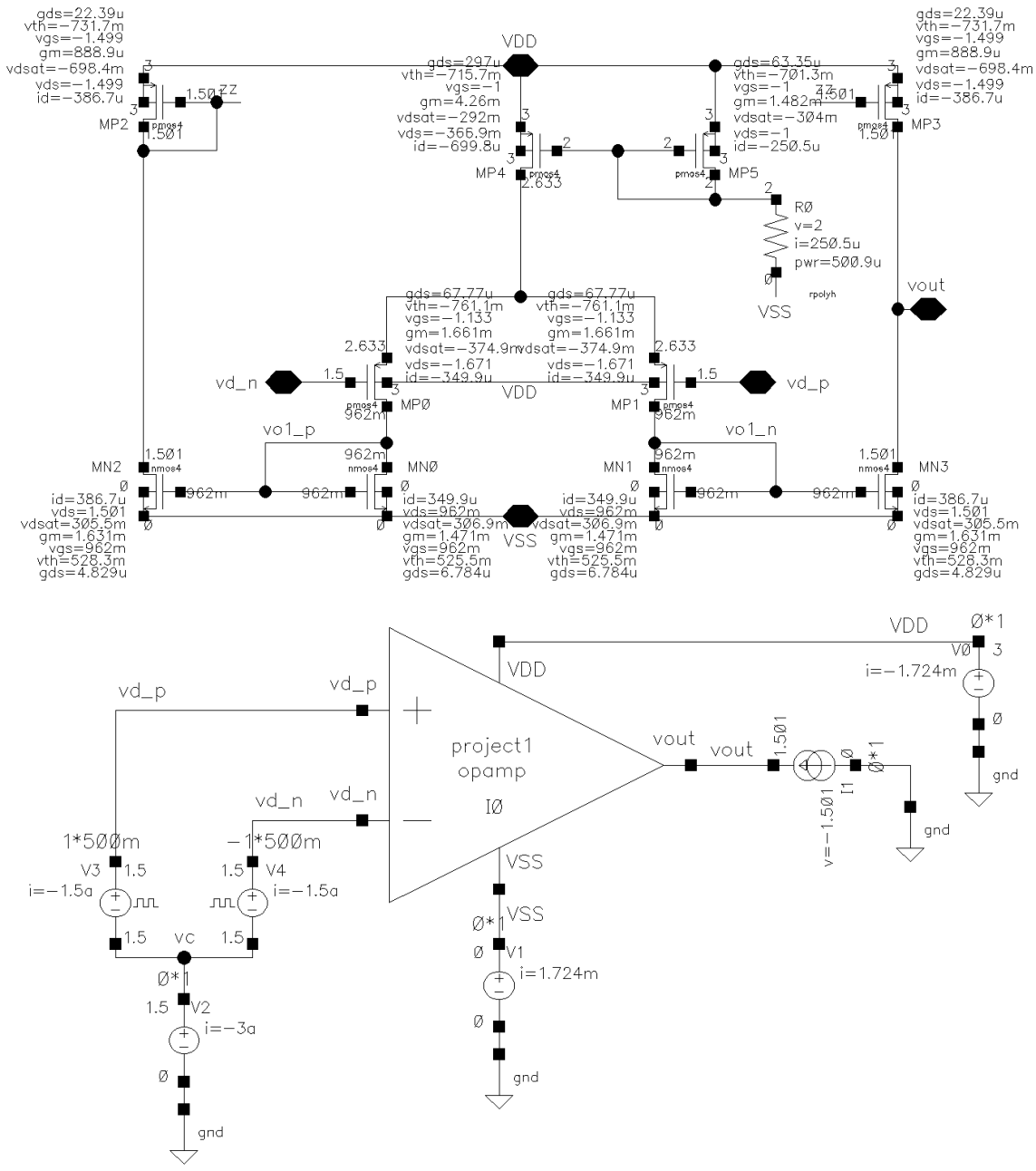

Figure 3: Schematic and testbench (respectively) with the DC node voltages and operating point results.

As seen in the results presented in Tab. 3, the dimensions of the circuit components were properly defined in order to have all transistors working in the saturation region. Initially, the channel width and channel length for the PMOS transistors in the differential pair (`MP0/MP1`) were defined in order to have the desired $A_d = 36\,\text{dB}$. However, when the ideal current source was replaced, it was necessary to make small adjustments to make sure that the current in the differential pair remained at $700\,\mu\text{A}$ and that transistor `MP4` remained in saturation. For that purpose, it was also very important to change the dimensions of transistor `MP4` - which ended up with a very large ratio W/L (since $W = 150\,\mu\text{m}$ and $L = 0.35\,\mu\text{m}$), in order to have the desired source current. On the other hand, the dimensions of `MP5` were necessary to control its gate voltage, while the resistance dimensions allowed `MP5` to have a lower source current of $250.5\,\mu\text{A}$ (as shown in Fig. 3). Additionally, the results shown in Tab. 4 indicate that the imposed specifications for the OPAMP circuit were achieved - these include I_{dp} (measured in transistor `MP4`), the total supply current (measured in the voltage sources connected to `VDD` and `VSS`) and V_{out}.

Table 3: DC node voltages and operating point results regarding the transistors in the circuit.

Transistor	$V_{SG/GS}$ [V]	V_{th} [V]	$V_{SD/DS_{sat}}$ [mV]	$V_{SD/DS}$ [V]	Operating region
`MP0/MP1`	1.133	761.1	374.9	1.671	Saturation
`MN0/MN1`	0.962	525.5	306.9	0.962	
`MP2/MP3`	1.499	731.7	698.4	1.499	
`MN2/MN3`	0.962	528.3	305.5	1.501	
`MP4`	1.000	715.7	292.0	0.367	
`MP5`	1.000	701.3	304.0	1.000	

Table 4: DC node voltages and operating point results regarding the required specifications.

Parameter	Required value	Results
Differential pair bias current, I_{dp}	$700\,\mu\text{A}$	$699.8\,\mu\text{A}$
Maximum total supply current	$\leq 5\,\text{mA}$	$1.724\,\text{mA}$
Output common node voltage, V_{out}	$1.5\,\text{V}$	$1.501\,\text{V}$

2.2 Frequency response of the differential and common-mode gains

By running AC simulations with AC components of $500\,\text{mV}$ and $-500\,\text{mV}$ in the inputs of the OPAMP (corresponding to a differential input voltage of $v_d = 1\,\text{V}$), or an AC component of $v_c = 1\,\text{V}$ in the common-mode input, the differential mode gain (A_d) and common-mode gain (A_c) can be respectively determined by

$$A_d = \frac{v_o}{v_d}\,, \quad A_c = \frac{v_o}{v_c} \tag{2}$$

Having the results shown in Figs. 4 and 5 been obtained. In order to obtain the desired $A_d = 36\,\text{dB}$, the ratio W/L of the PMOS transistors `MP0` and `MP1` in the differential pair was initially adjusted, where an increase in this ratio leads to a higher A_d (and vice-versa). It is also worth noting that the

value of the channel length of the transistors in the circuit is more impactful than the channel width on altering the gain value, since the resistance associated with each transistor varies with L, and the value of A_d directly depends on the output resistance of the OPAMP. The value of W/L in `MP0` and `MP1` was also adjusted in order to make sure transistor `MP4` worked in the saturation region (by decreasing the drain voltage of the latter). After establishing the dimensions of these PMOS transistors, more adjustments were made in the other transistors in the circuit (as described in Sec. 2.1) to obtain the results shown in Fig. 4. It can be seen that, for very high frequency values, the value of A_d decreases considerably, due to the existence of the lower frequency dominant pole - associated with the capacitances and resistances of the transistors in the circuit. With the low-frequency gain A_0 and the bandwidth specified in Fig. 4, a very high gain-bandwidth product of $B \approx 22.1Gs^{-1}$ is obtained.

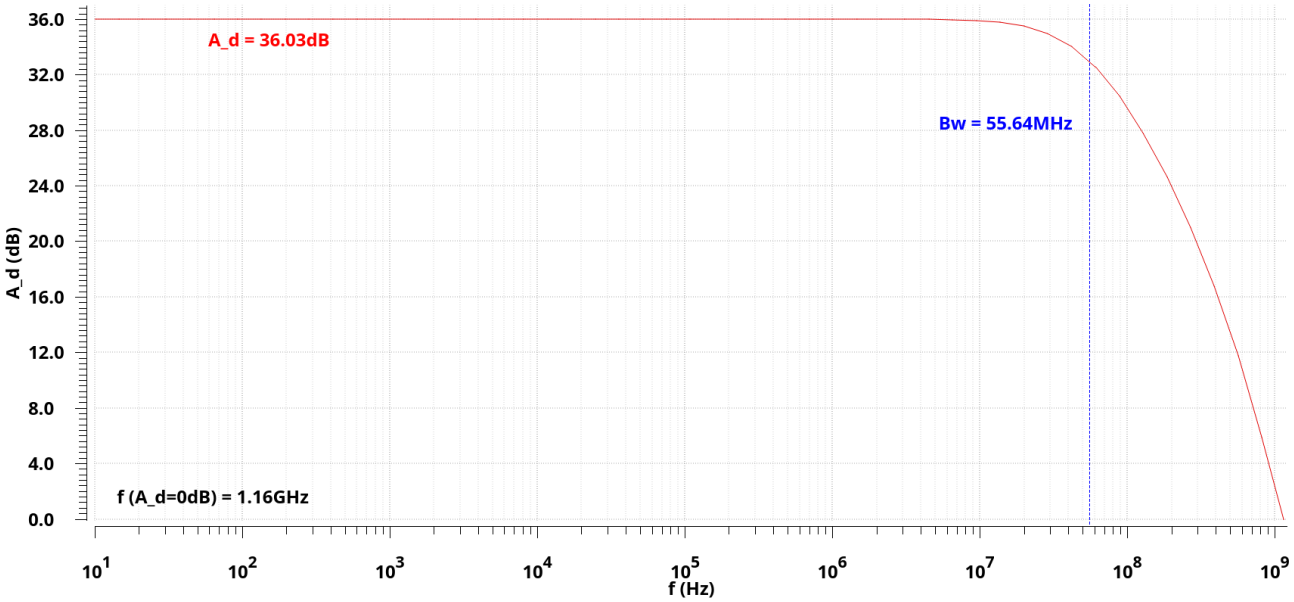

Figure 4: Frequency response of the differential mode gain (A_d).

As for the common-mode gain, which consists of an undesired gain, it can be seen in Fig. 5 that, for lower frequencies, it possesses a very low value. At a certain frequency, A_c begins to increase, which is a result of a zero that should exist in the common-mode gain expression. Although ideally the difference amplifier will amplify only the differential input signal v_D and reject completely the common-mode input signal v_C, practical circuits have an output voltage given by $v_O = A_d \cdot v_D + A_c \cdot v_C$ and the efficacy of a differential amplifier is measured by the degree of its rejection of common-mode signals in preference to differential signals. This is usually quantified by the common-mode rejection ratio (CMRR), defined as $CMRR[dB] = |A_d|[dB] - |A_c|[dB]$, which should be as high as possible. By directly using the values of the curves $A_d(f)$ and $A_s(f)$, the result shown in Fig. 6 was obtained. This curve indicates that, for low frequency, the amplification of the differential input dominates, but this characteristic degrades for higher frequencies, as A_d decreases and A_c increases. For extremely high frequencies, its value stabilizes, since both gain values decrease considerably.

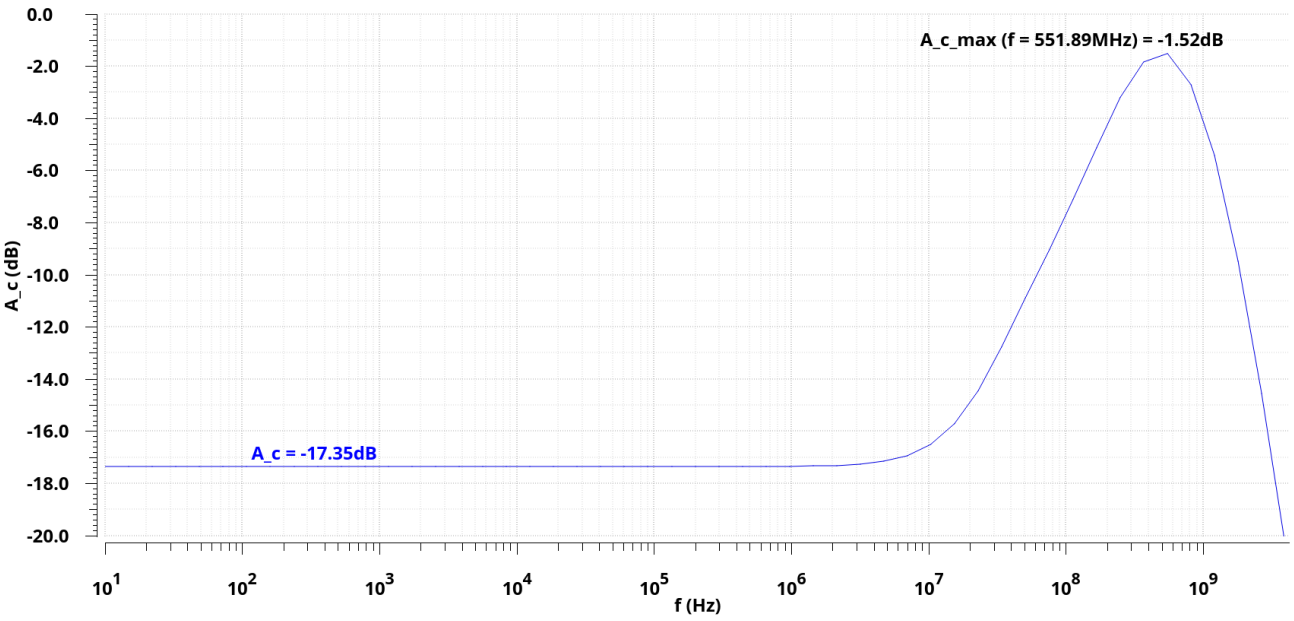

Figure 5: Frequency response of the common-mode gain (A_c).

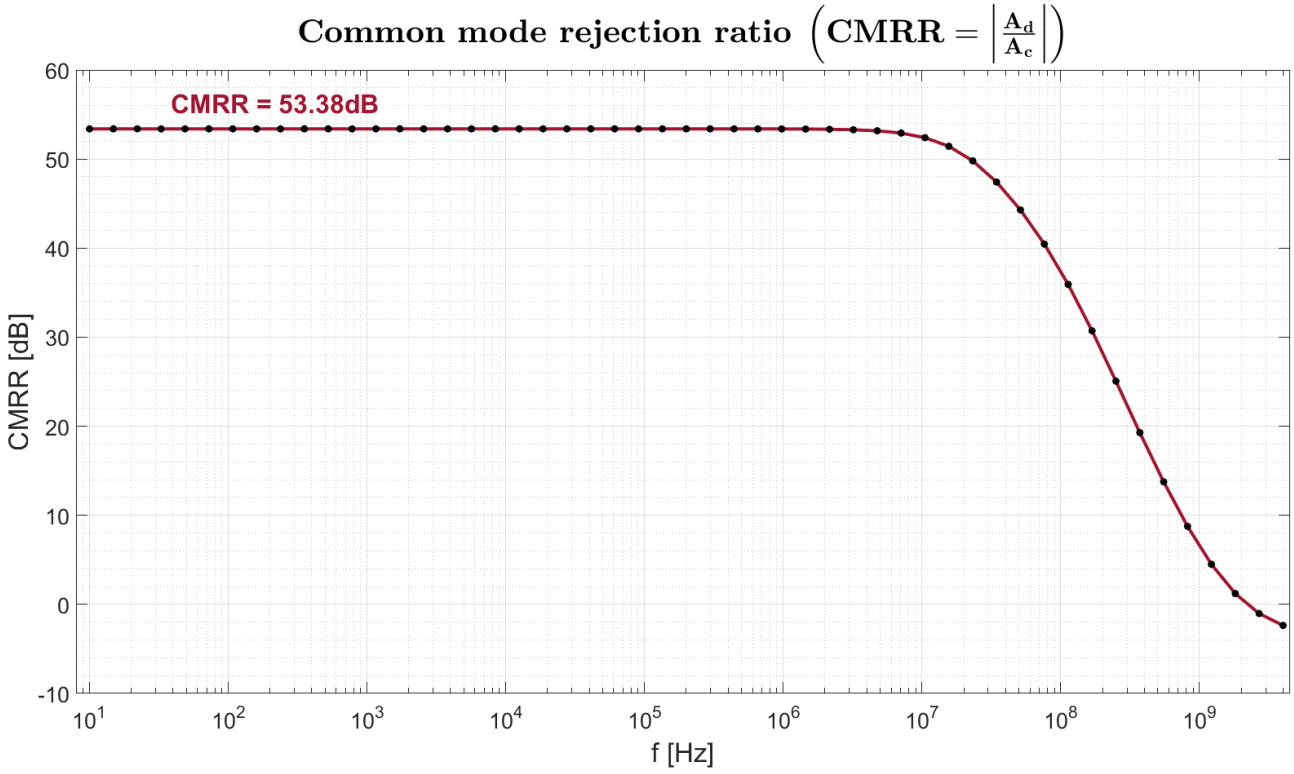

Figure 6: Frequency response of the common-mode rejection ratio (CMRR).

2.3 Frequency response of the input and output impedances

By running an AC simulation with AC components in the inputs of the OPAMP, the differential mode input impedance is obtained by $Z_{id} = v_d/i_d$, where i_d is the current entering `vd_p`. The variation of the real and imaginary parts of this impedance are depicted in Fig. 7. Regarding the imaginary part, it can be seen that the absolute value is very high for low frequencies, since the capacitances in

the circuit work almost as open circuits - this is because the impedance associated with a capacitance C is given by $Z_C = -j/(\omega \cdot C)$. As the frequency increases, the value of the imaginary part increases and the effect of these capacitors on the circuit becomes more significant. As for the real part, it has a very high value for low frequencies - in fact, the input impedances of an ideal OPAMP are infinite. However, it decreases with frequency, even though it is also apparent in Fig. 8 that, for certain low frequency values, it appears to stabilize - after which it decreases along the frequency values in which A_d also starts to deteriorate (as depicted in Fig. 4).

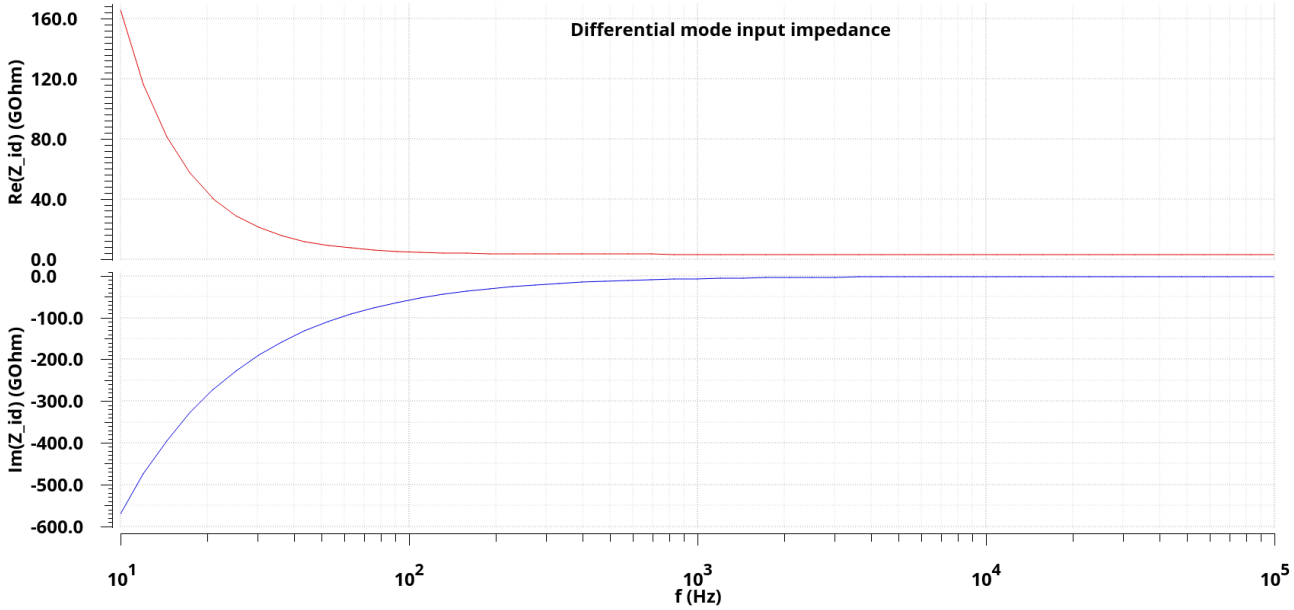

Figure 7: Frequency response of the differential mode input impedance (real and imaginary parts).

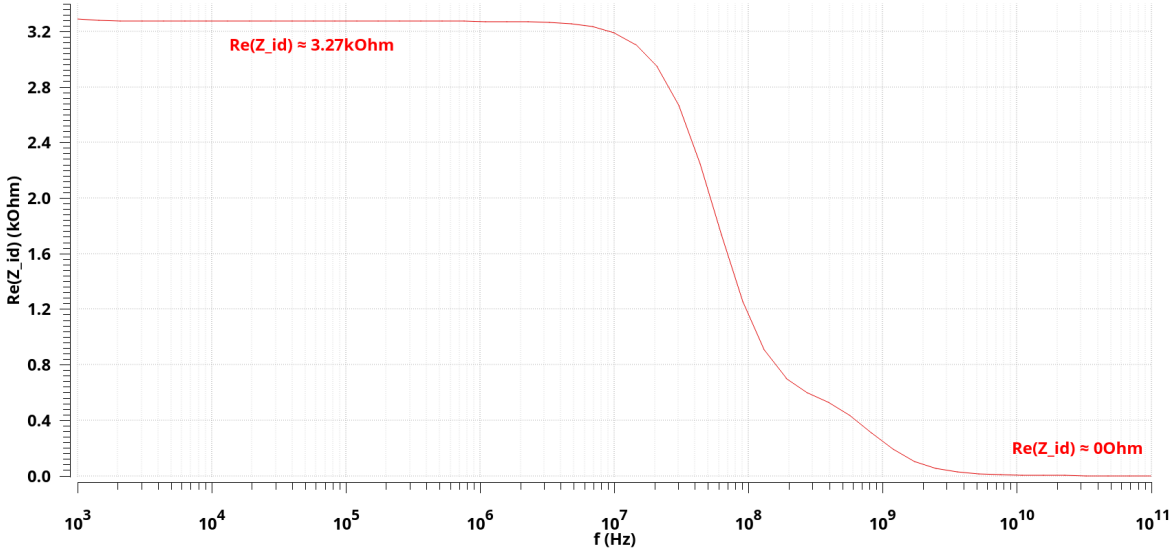

Figure 8: Frequency response of the real part of the differential mode input impedance for certain frequency values.

Regarding the common-mode input impedance, given by $Z_{ic} = v_c/i_c$, where this voltage and current are obtained from the common-mode voltage source, a similar behaviour can be observed in Fig. 9,

which once again corroborates the significant impact of the capacitances in the circuit for higher frequencies. A small detail that differs from the previous curves can be seen in Fig. 9, where it appears that the real part reaches negative values for certain frequencies - perhaps due to errors in the calculation performed by the software or the association of different components in the circuit whose reactances end up multiplying -, but then increases to zero, in the frequency values where A_c (depicted in Fig. 5) increases.

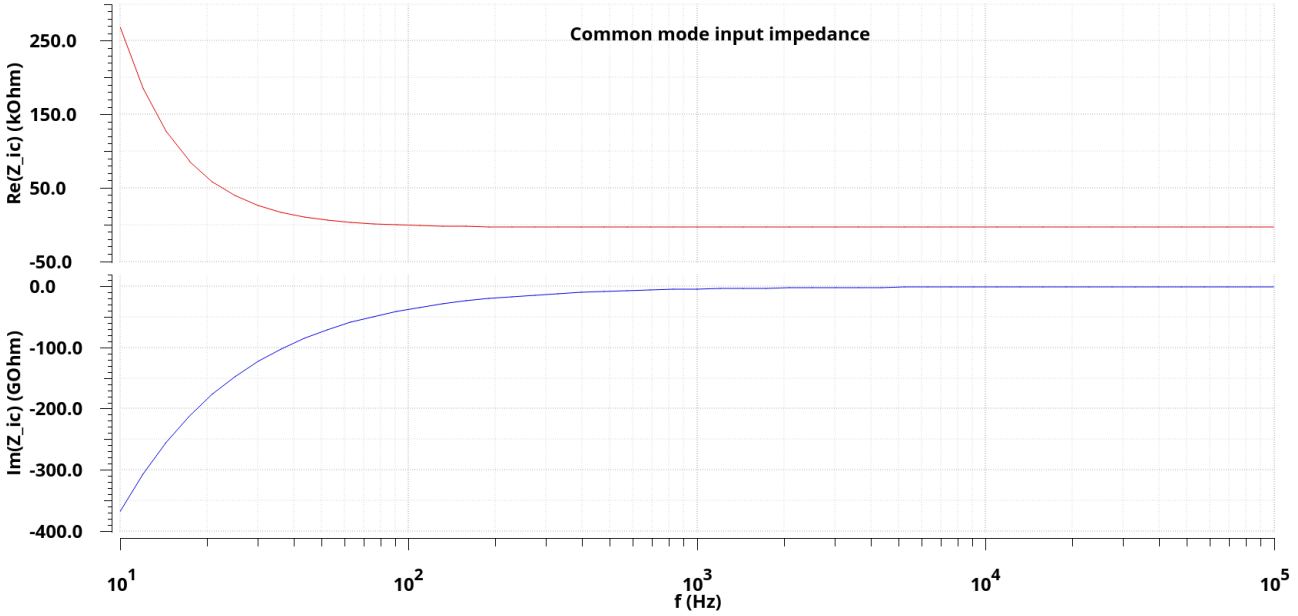

Figure 9: Frequency response of the common-mode input impedance (real and imaginary parts, respectively).

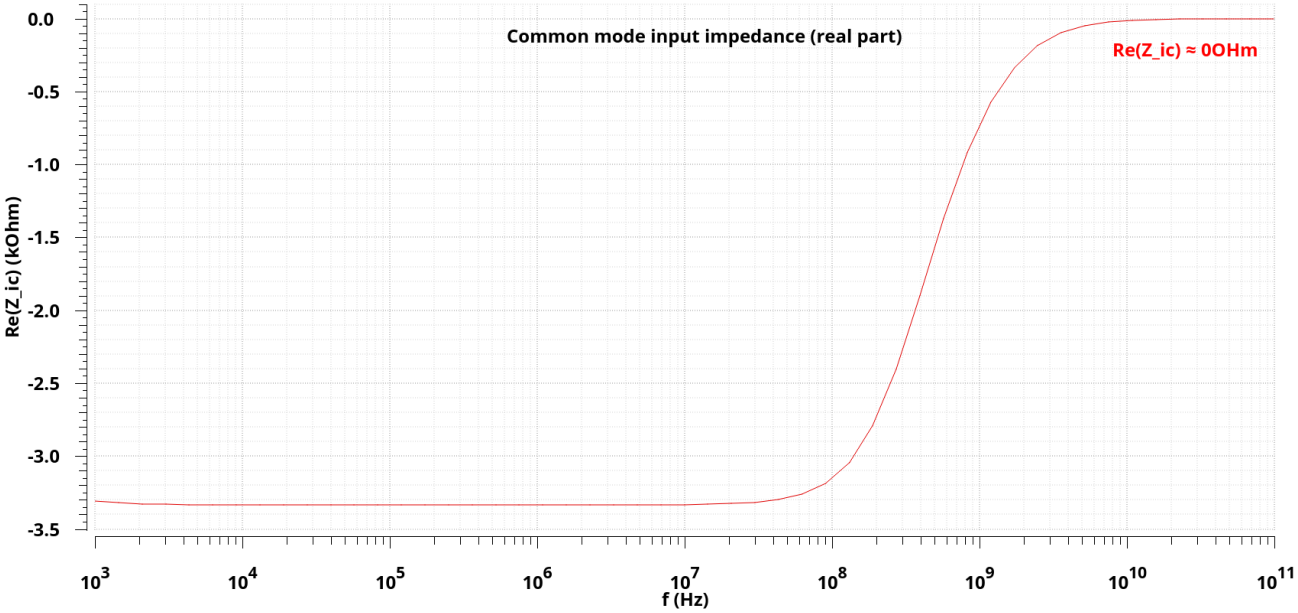

Figure 10: Frequency response of the real part of the common-mode input impedance for certain frequency values.

The output impedance of the OPAMP, whose results are shown in Fig. 11, is ideally zero. However, in real OPAMPs, that is not the case, and the real part of $Z_o = v_o/i_o$ has a value of 36.8 kΩ in this case. The value of the real part decreases around the same frequencies in which the differential mode gain decreases, since the latter is given by

$$A_d = -g_m \cdot M \cdot \frac{r_o}{2} \tag{3}$$

Where r_o is the value of the output resistance. This real component of Z_{out} corresponds to the parallel of the output resistances of both transistors in the output of the circuit. As for the imaginary part, it only moves away significant from zero around the aforementioned frequency values, not for very low frequencies - perhaps to the larger capacitance values or the existence of inductances (which might also corroborate the decrease in the imaginary part seen around medium-high frequencies). For very high frequencies, the module of the output impedance tends to zero; in fact, the differential gain tends to stabilize (at very low values) for these very high frequencies.

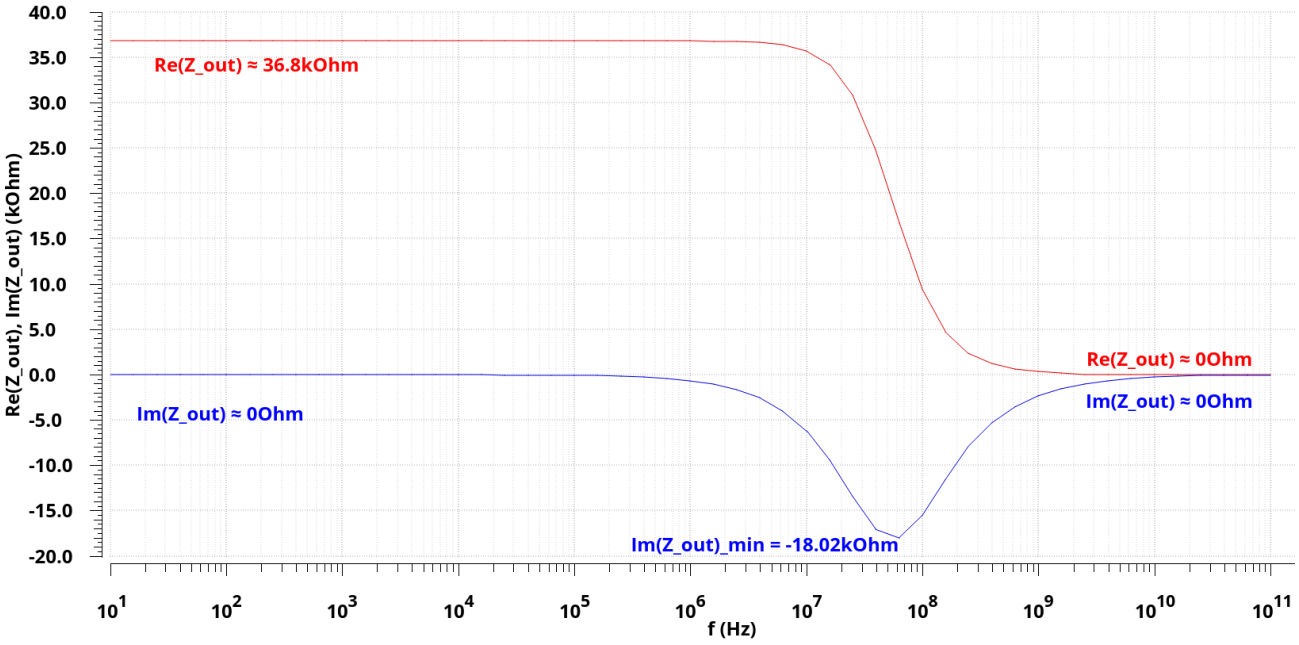

Figure 11: Frequency response of the output impedance (real and imaginary parts).

2.4 Input offset voltage

In an ideal single-ended output OPAMP which is positively biased - in this case, with $V_{DD} = 3.0\,\text{V}$ and $V_{SS} = 0\,\text{V}$ - the desired value at the output for a differential input of $v_D = 0\,\text{V}$ should be $v_O = V_{DD}/2 = 1.5\,\text{V}$. However, in a real OPAMP, that is not the case. In the results shown in Fig. 12, obtained by sweeping the parameter V_D used for the DC voltage in the inputs of the OPAMP ($V_D/2$ and $-V_D/2$), it can be seen that the output voltage does not reach 1.5 V at $v_D = 0V$. By performing a more detailed simulation around the central value, as shown in Fig. 13, an **offset voltage** of $\boldsymbol{V_{OS} = -9.71\,\mu\text{V}}$ was determined. This negative value, which is not too impactful, can be justified by the circuit design itself since, as shown in Fig. 3, regarding the bias point simulation, a DC node

voltage of $V_{out} = 1.501\,\text{V} > 1.5\,\text{V}$ was obtained in the operating point - thus, a negative v_D is necessary to have $v_O = 0\,\text{V}$.

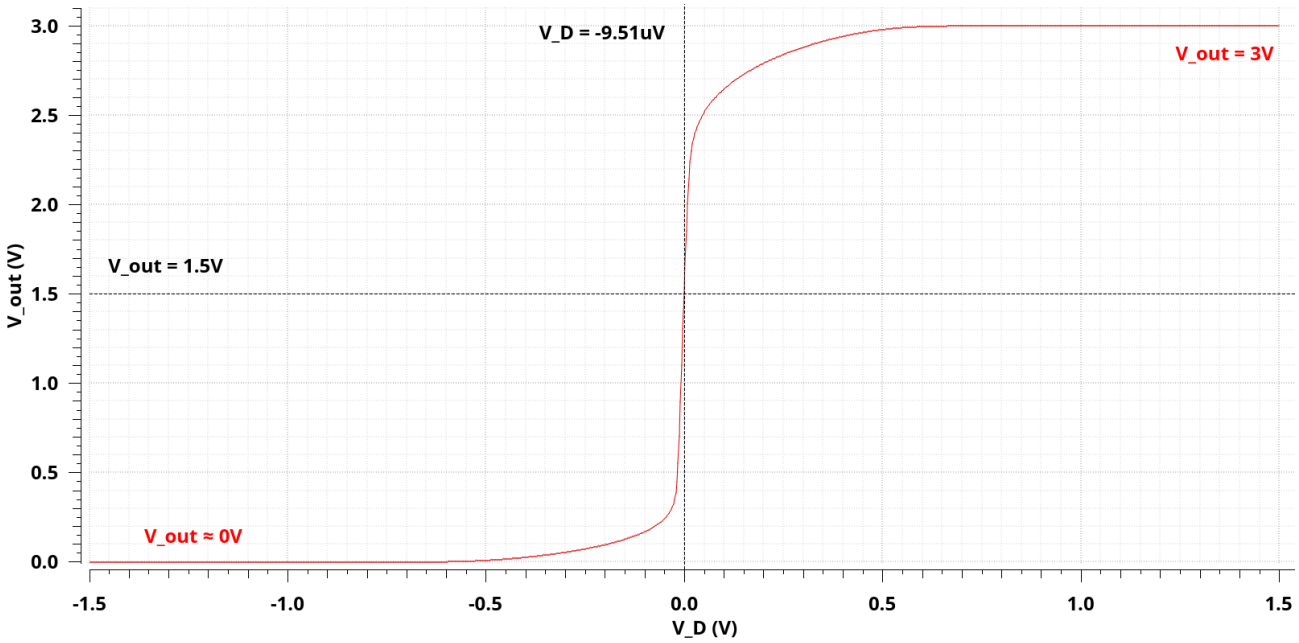

Figure 12: Output node voltage in a DC sweep of the parameter V_D, giving a preliminary input offset voltage value.

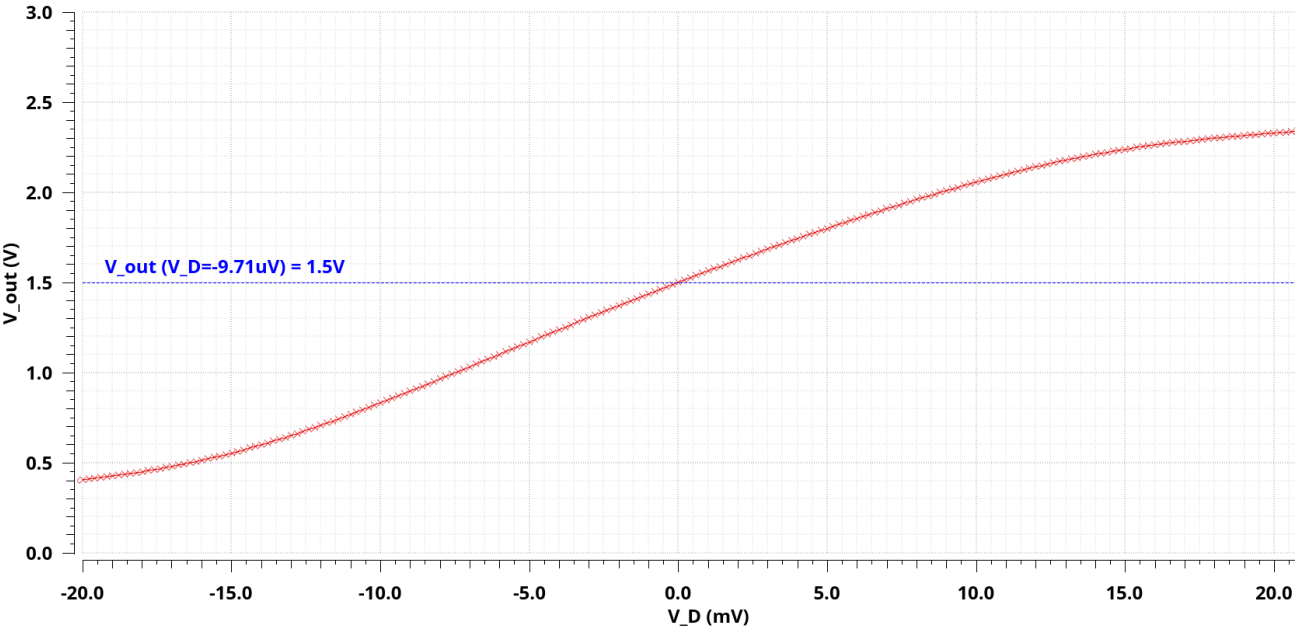

Figure 13: Detailed view of the output node voltage in a DC sweep of the parameter V_D, giving a more accurate input offset voltage value.

2.5 Power supply rejection ratios

A portion of supply ripple can make its way to the OPAMP output and corrupt the output signal. The traditional approach for reducing supply ripple by connecting large capacitances between the

supply rails and ground is usually not viable in IC design, as such capacitances would consume most of the chip area. Instead, it is essential to pay attention to the power supply rejection ratio (PSRR), used to quantify the bias nodes voltage fluctuation influence on the output node. The PSRR is defined as the ratio of the amplifier differential gain to the gain experienced by a change in the power supply voltages (an undesirable disturbance, that can be considered a small signal voltage), described by $v_{DD} = V_{DD} + v_{dd}$ and $v_{SS} = V_{SS} + v_{ss}$ for circuits using two power supplies. The PSRR is given by the ratio of the desired differential gain and the undesired gains ($A^+ = v_o/v_{dd}$ and $A^- = v_o/v_{ss}$), according to

$$PSRR^+ = \frac{A_d}{A^+}\ ,\quad PSRR^- = \frac{A_d}{A^-} \tag{4}$$

Thus, by placing an AC component in each power supply separately, the results shown in Fig. 14 were obtained; using the exported values from these curves (together with the values of $A_d(f)$), the graphs shown in Figs. 15 and 16 were posteriorly determined. As lower the value of the undesirable gains, the more the perturbation is "cancelled" out in the output. For low frequencies, A^+ is higher, which means that a perturbation in v_{DD} is reflected almost the same in the output, whereas perturbations in v_{SS} are less significant. For very high frequencies, both gains are relatively high - which is undesirable.

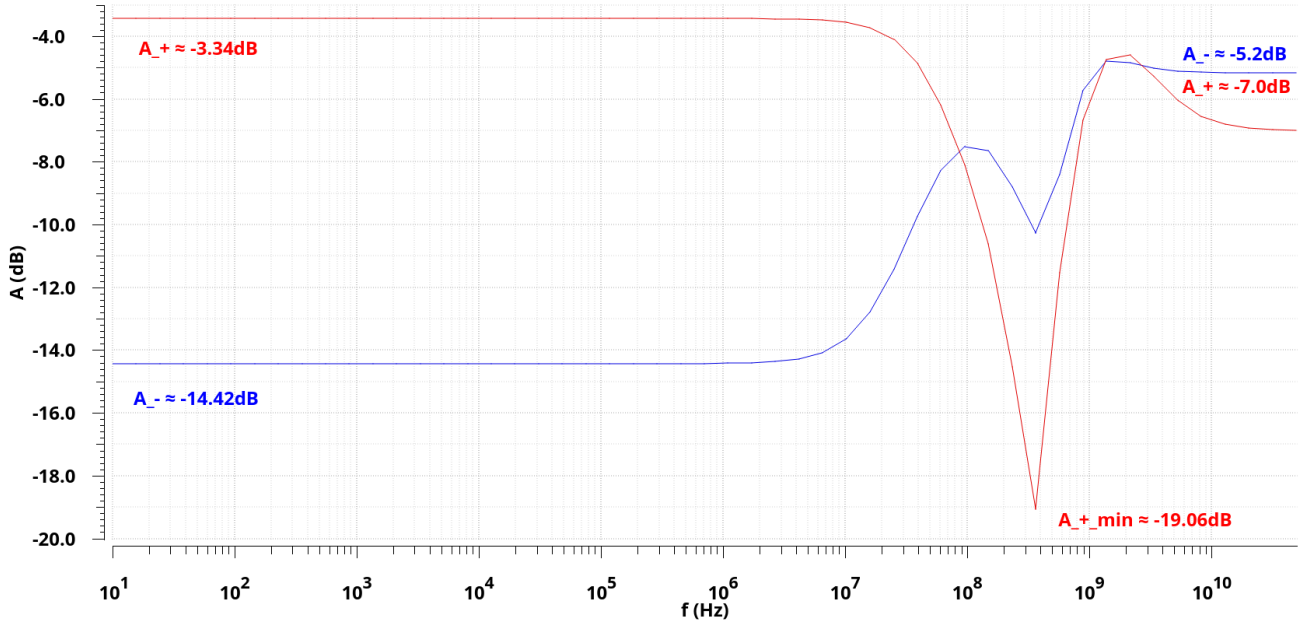

Figure 14: Frequency responses of the undesired gains A^+ and A^-.

Regarding the PSRR curves, it can be concluded that, for low frequencies, the circuit is more sensitive to small variations in v_{DD}, since $PSRR^+ < PSRR^-$ - to minimize the effect of the power supply ripple, a large PSRR is required. This could be due to the fact that perturbations in v_{DD} more directly affect the current supplied to the differential pair (controlled mostly by transistors `MP4` and `MP5`), which might significantly compromise the gain. On the other hand, perturbations in v_{SS} might be less significant due to the relatively high channel lengths used in the NMOS transistors. As the frequency increases, both perturbations become much more significant, not only because the value of

A_d decreases considerably, but also because the values of A^+ and A^- remain approximately stable. This leads to very low values for both ratios, which compromises the circuit performance at very high frequencies.

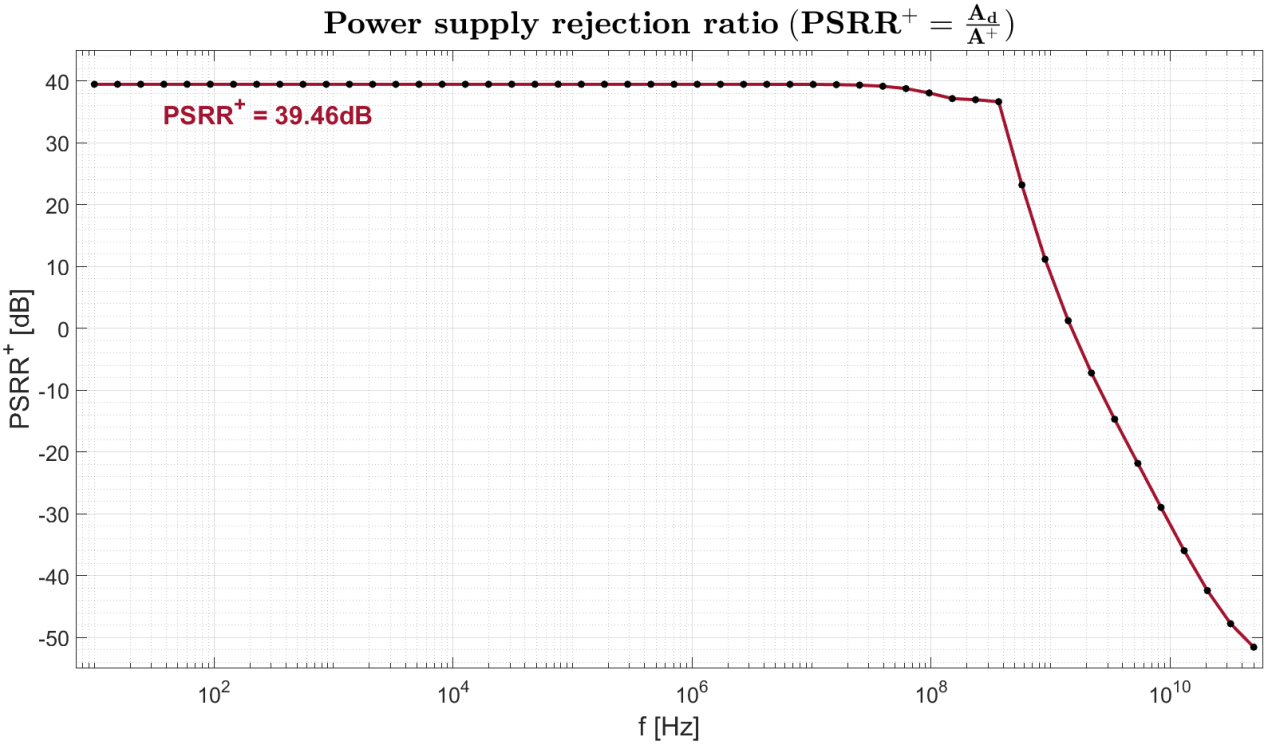

Figure 15: Frequency response of $PSRR^+$.

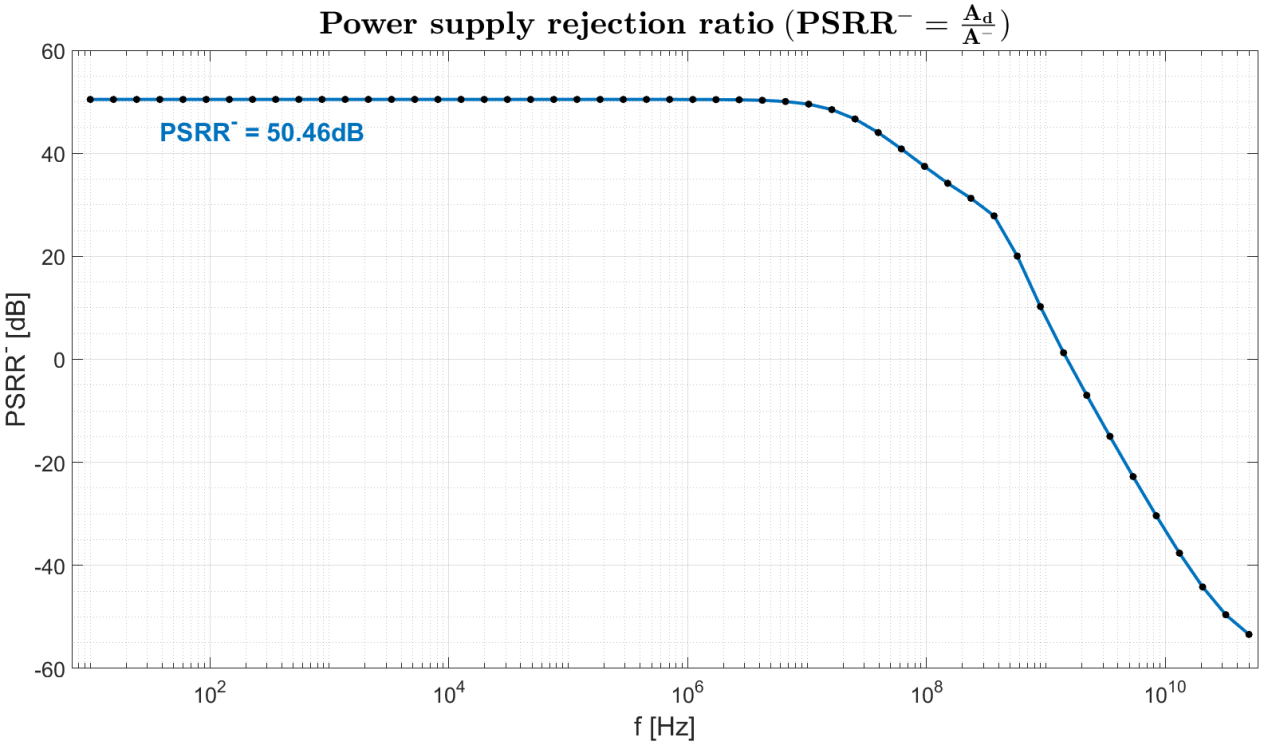

Figure 16: Frequency response of $PSRR^-$.

2.6 Input common-mode voltage range and output voltage range

Considering the DC common-mode voltage V_{CM} used in the testbench showed in Fig. 2, its value must be within a certain range in order to make sure that the input transistors work in the saturation region and that the OPAMP works properly. To define this input common-mode voltage range, the values of V_{CM} in which a significant degradation of A_d and bandwidth Bw must be taken into account. In order to determine the lower value of this range, a minimum gain of $A_d = 40\,\text{dB}$ was selected; as seen in Fig. 17, this value of the differential mode gain was reached between $V_{CM} = 0.3\,\text{V}$ and $V_{CM} = 0.4\,\text{V}$. An additional detailed simulation allowed to conclude that $V_{CM} = 0.31\,\text{V}$ corresponds to the desired minimum. Regarding the maximum value, it was decided to consider it when 10 % of the original bandwidth ($Bw = 55.64\,\text{MHz}$, as shown in Fig. 4), which corresponds to $\approx 5.56\,\text{MHz}$, was reached, since most high values of V_{CM} did not cause a decrease in A_d, but led to a degradation of the bandwidth. This analysis led to an upper limit of $V_{CM} = 2.26\,\text{V}$ in a more detailed simulation.

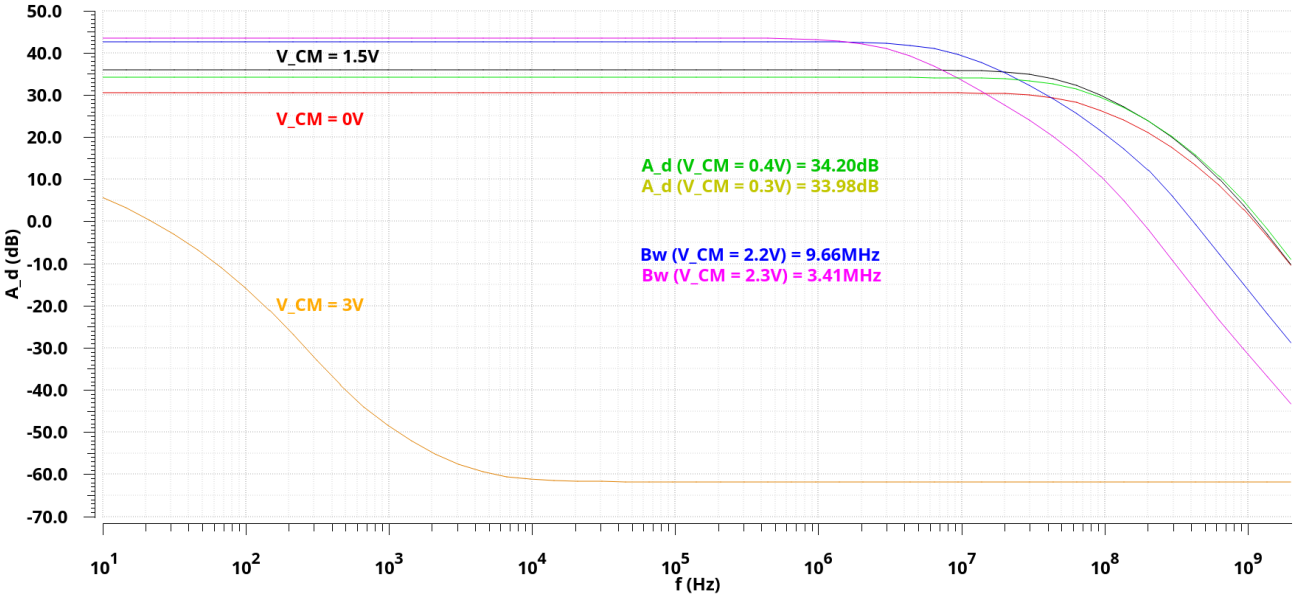

Figure 17: Differential mode gain curves used to determine the input common-mode voltage range.

The extent of the signal swing allowed at the output of the OPAMP is limited by the need to keep the output transistors in saturation - usually, within an overdrive voltage (for a PMOS or NMOS transistor) of each of the supply rails. In order to determine this output voltage maximum excursion, the upper and lower values for which the OPAMP works in a linear region were determined, using a V_D sweep similar to the one presented in Sec. 2.4. The derivative of this curve was plotted and a (relatively) arbitrary value was used to obtain the linear range, as depicted in Fig. 18. Both voltage ranges mentioned before are included in Tab. 5. As depicted in Fig. 3 (regarding the bias point), the upper transistor `MP3` had a threshold voltage of $\approx 0.73\,\text{V}$, whereas the lower transistor `MN3` had $\approx 0.53\,\text{V}$ for this parameter. The output range results depicted in Tab. 5 could therefore corroborate the prediction that its limits would be within an overdrive voltage of V_{DD} or V_{SS}. Finally, a usually important requirement in an OPAMP circuit is that it be possible for its output terminal

to be connected back to its negative input terminal so that a unity-gain amplifier is obtained. For such a connection to be possible, there must be a substantial overlap between the allowable range of the output and input common-mode voltages. This condition is verified in this particular circuit configuration according to the experimental results.

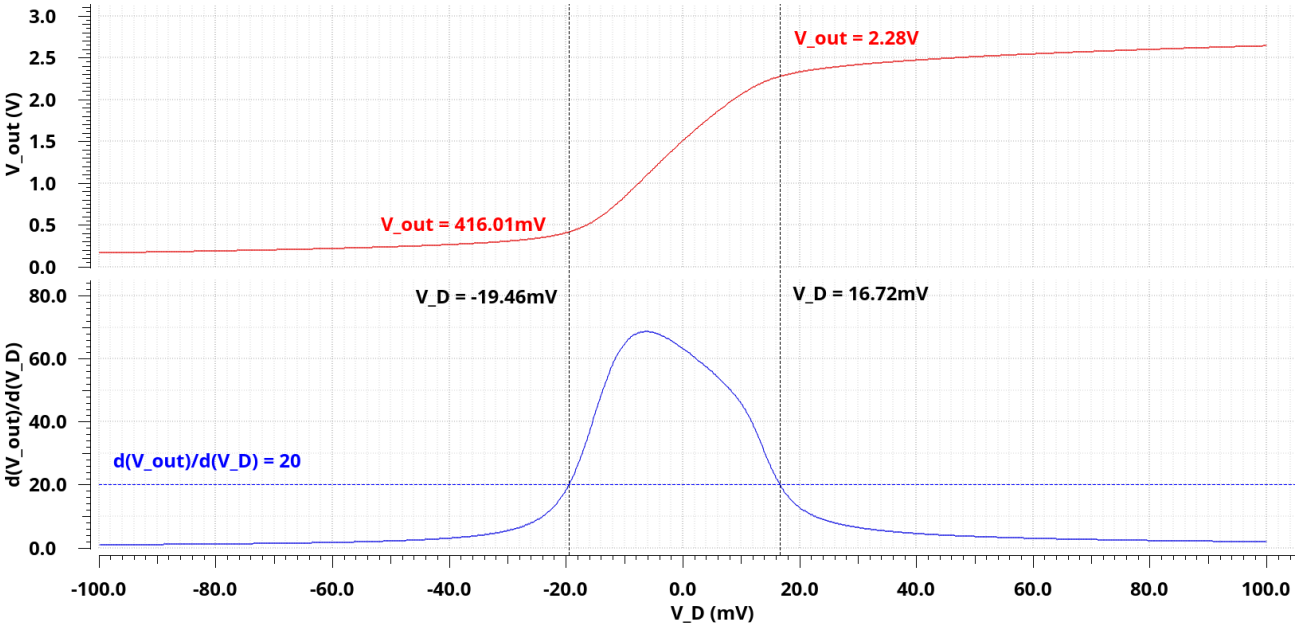

Figure 18: Curve of the output voltage variation with V_D and its derivative, used to determine the output voltage range.

Table 5: Input common-mode voltage range and output voltage range.

	Minimum voltage	**Maximum voltage**
Input common-mode voltage range	$V_{CM} = 0.31V$	$V_{CM} = 2.26V$
Output voltage range	$V_{out} = 0.42V$	$V_{out} = 2.28V$

2.7 Phase margin

Using the differential mode gain results depicted in Fig. 4, the phase margin can be easily determined by reading the phase of A_d at $f = 1.16\,\text{GHz}$, where the gain reaches 0 dB. As seen in Fig. 19, this leads to a phase margin of 8.8°. Since the phase sits above −180° at this point, there is a small safe margin that exists in the circuit regarding its stability in the "worst case" where feedback is used. With a single dominant pole, stability would always be guaranteed, since the phase would only go down to −90°. However, in the real OPAMP, other poles (at higher frequencies than the dominant pole) make it so that the phase continues to decrease for higher frequencies - much larger than the bandwidth of this circuit, however.

Table 6: Phase margin results.

Phase (A_d = 0dB)	-171.20^o
Phase margin	8.8^o

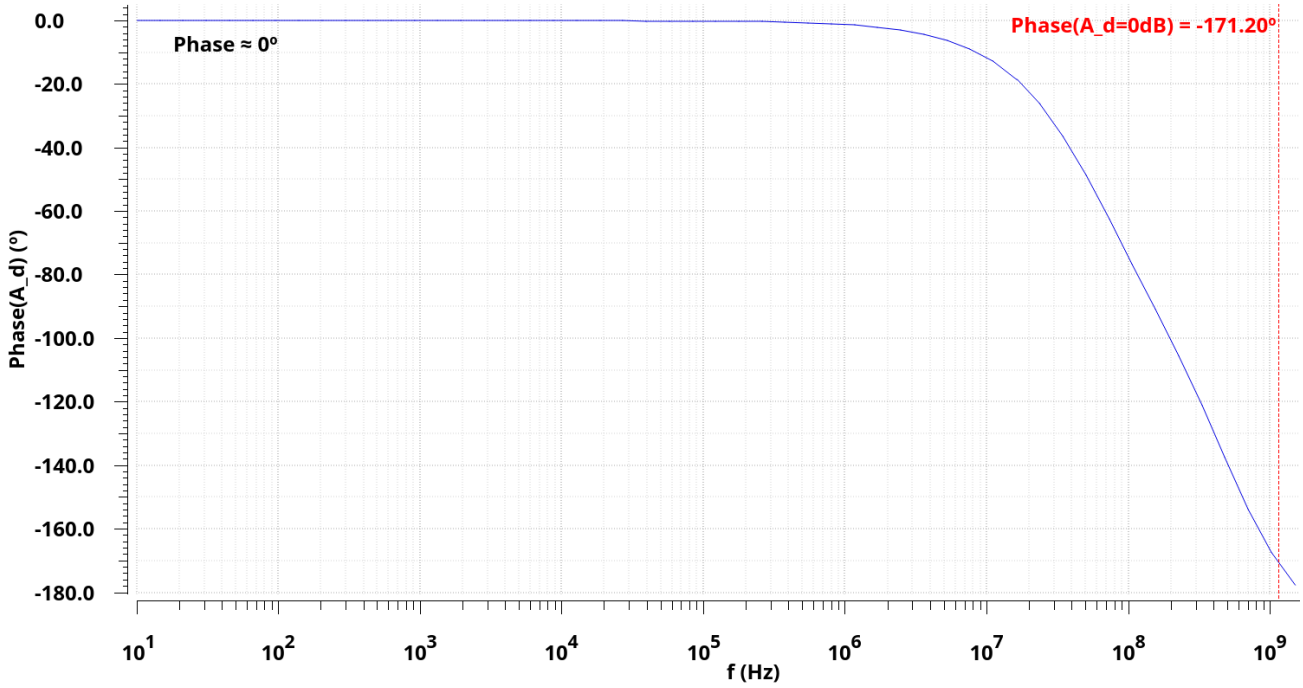

Figure 19: Frequency response of the phase of the differential mode gain.

2.8 Output rise and fall slew-rate

The slew-rate of an OPAMP, which can be determined by

$$SR = \left| \frac{dv_O(t)}{dt} \right|_{max} \tag{5}$$

Is limited by the current maximum value limitation that the OPAMP presents at the output, which needs to charge/discharge capacitors. By applying pulse signals in the inputs of the OPAMP, the value of this parameter can be determined by using the derivative of the $V_{out}(t)$ curve in a transient analysis, as depicted in Fig. 20. As shown in Tab. 7, a slightly higher value was determined for the rise slew-rate, which is due to the circuit configuration. When V_{out} changes from 0 V to 3 V, the PMOS transistors turn off and the NMOS transistors turn on, while the opposite occurs when the value of V_{out} decreases. However, the dimensions of the transistors `MP2/MP3` and `MN2/MN3` are not the same, leading to different values for the transition voltages between operating regions, added to the different mobilities associated with different types of MOS transistors. These different dimensions are associated with capacitances of different values, which naturally create a slight unbalance in the slew-rate values.

Table 7: Output rise and fall slew-rate results.

Rise slew-rate [kV/µs]	**Fall slew-rate** [kV/µs]
6.95	6.25

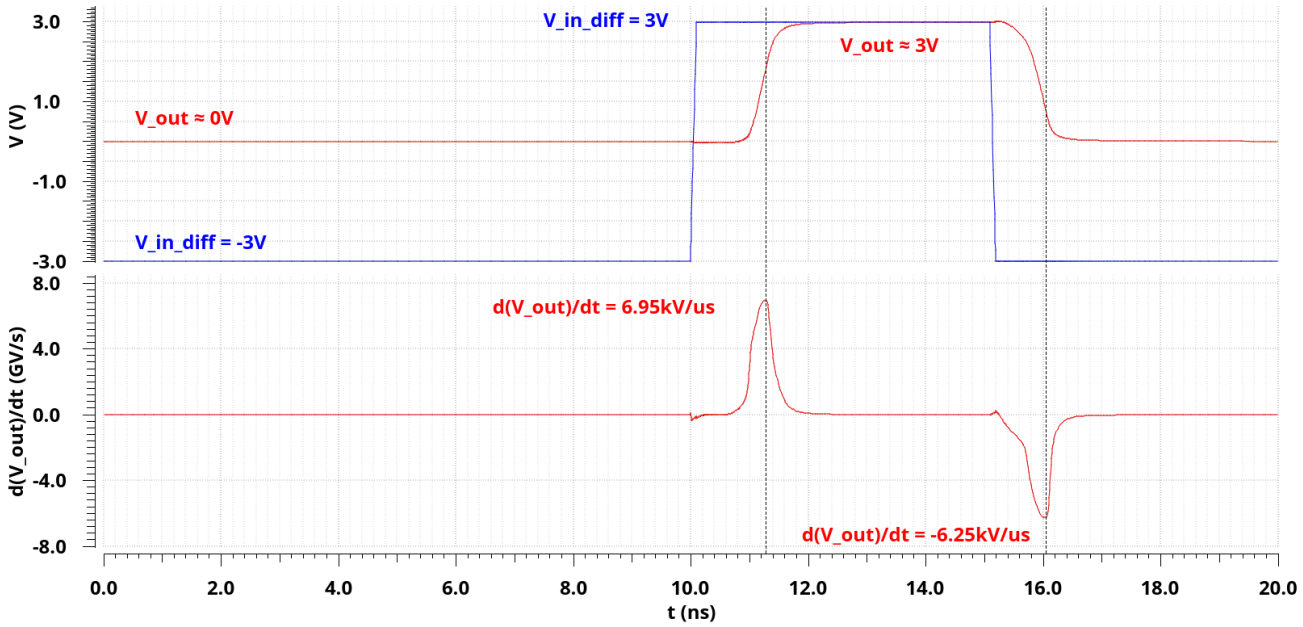

Figure 20: Output rise and fall slew-rate determination.

2.9 Total supply bias current and power consumption

Directly using the results of the DC operating point analysis shown in Fig. 3, the total supply bias current (measured in `VDD` or `VSS`) has the value shown in Tab. 8 (along with the power consumption, given by the product of this current and the supply voltage), which is lower than the upper imposed limit of 5 mA. The power consumption is quite low, which perhaps could not be achieved with other types of OPAMP circuit topologies.

Table 8: Results obtained with the DC operating points.

Total supply bias current	Supply voltage (V_{DD})	Power consumption
1.72 mA	3.0 V	5.16 mW

2.10 Corner analyses

Corner analysis is extremely useful, since the behaviour of the circuits can be tested in extreme conditions. In this case, the differential gain AC simulation was run for process dispersion in CMOS transistors and in the resistance, supply voltage variations of ±10 % and temperature dispersion (for −40°C and 125°C). In each figure shown below, the plots obtained for the varying parameters are presented alongside the nominal results, corresponding to the curves in black.

In CMOS process corners, the changes occur in the charge mobility (μ) and threshold voltage (V_{th}), as described in Tab. 9. As shown in the results of Fig. 21, the minimum gain at low frequencies occurred for WZ, whereas the maximum gain occurred for WO. The justifications for this are that a lower threshold voltage in the NMOS transistors (which occurs in the WO corner, for example) leads to an increase in $A_d \sim V_{OV}$, where V_{OV} is the overdrive voltage of the output NMOS transistor;

additionally, a lower current in PMOS transistors (which occurs when the respective mobility decreases and V_{th} increases - for instance, in the WO corner) leads to a lower current in the differential pair and, consequently, in the output transistors, which decreases the V_{SG} in `MP2`, therefore increasing the output node voltage, due to (1), therefore increasing A_d. The opposite of all these conditions corresponds to the corner WZ, which consequently leads to the lowest differential mode gain at low frequencies.

Table 9: CMOS process corners and the respective variations in μ and V_{th}.

Designation	nMOS	pMOS
WO (worst one)	$\mu \nearrow$ $V_{th} \searrow$	$\mu \searrow$ $V_{th} \nearrow$
WZ (worst zero)	$\mu \searrow$ $V_{th} \nearrow$	$\mu \nearrow$ $V_{th} \searrow$
WP (worst power)	$\mu \nearrow$ $V_{th} \searrow$	$\mu \nearrow$ $V_{th} \searrow$
WS (worst speed)	$\mu \searrow$ $V_{th} \nearrow$	$\mu \searrow$ $V_{th} \nearrow$

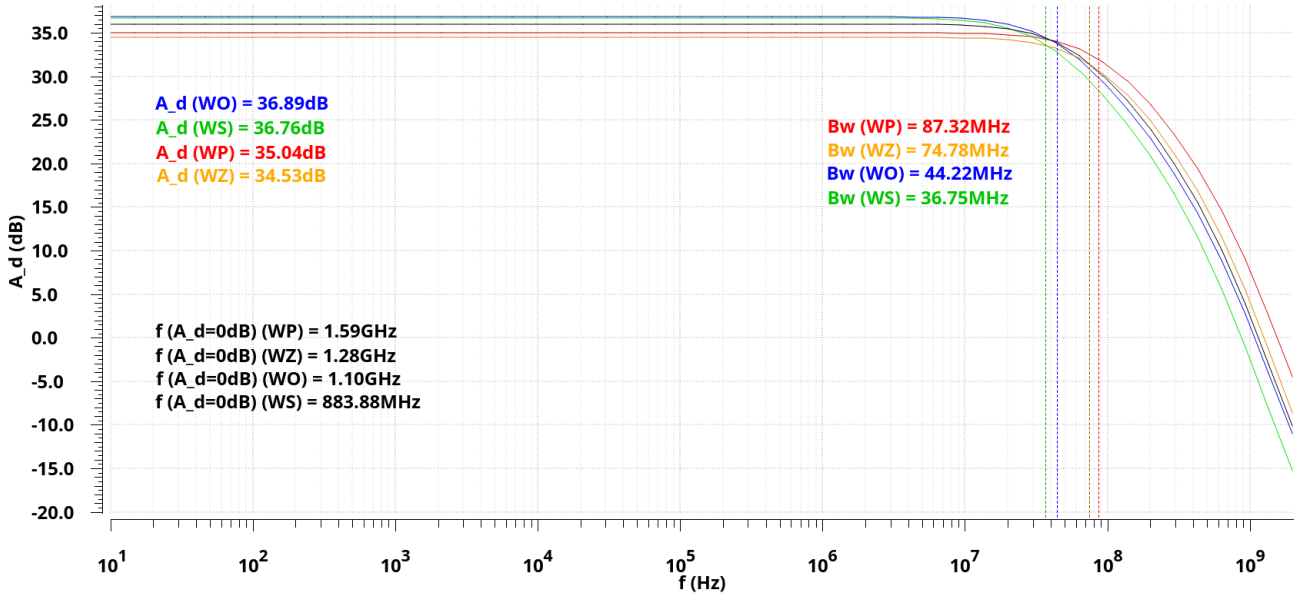

Figure 21: CMOS process corners - frequency response of the differential mode gain.

Regarding the resistance process corners, the changes in mobility should be the same as depicted in Tab. 9 since, in the worst power corner, the current in the resistor `R0` increases, whereas the opposite happens in the worst speed corner. When this current increases, the current supplied to the differential pair also increases, leading to a lower value of A_d, since the current in the output transistors rises and the output node voltage decreases due to the transistor equation in (1), while the opposite happens in `WS`. These results can be seen in Fig. 22.

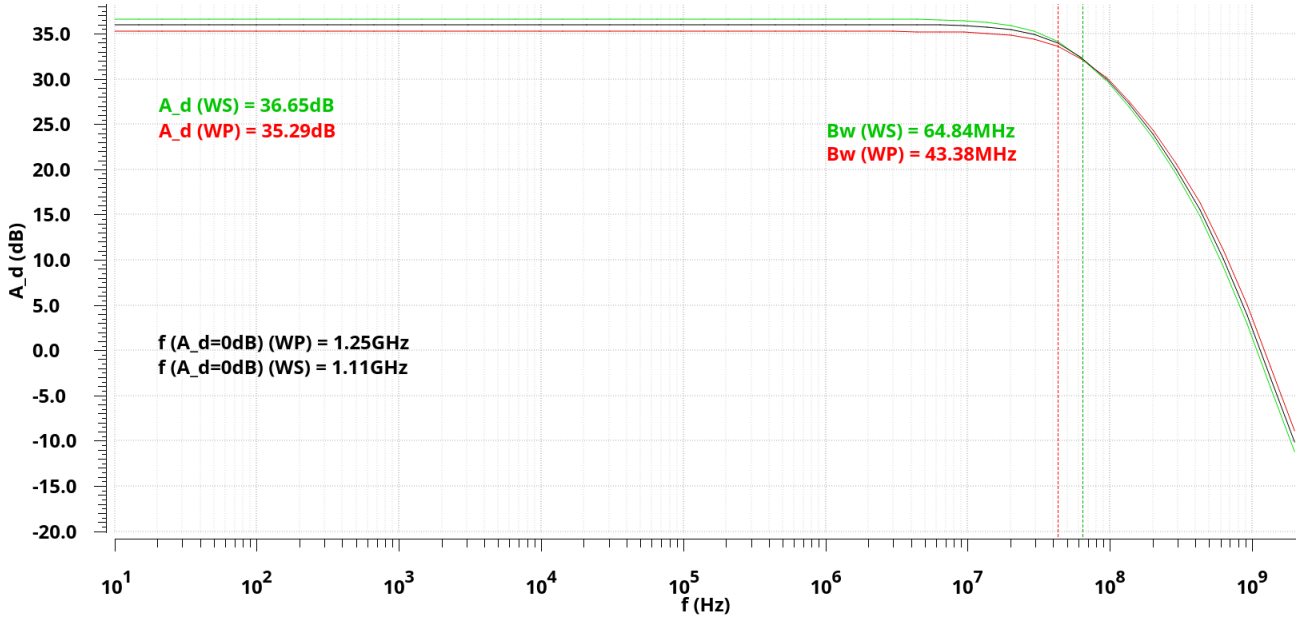

Figure 22: Resistance process corners - frequency response of the differential mode gain.

With a decrease in V_{DD}, the overall currents and voltages in the circuit decrease. However, the reduction in the output node voltage is less significant, since a lower current in the output transistors requires a lower V_{SG}, thus increasing the gate voltage in transistor `MP2`. Consequently, the value of A_d ends up increasing slightly for $V_{DD} = 2.7\,\text{V}$, as depicted in Fig. 23, while the opposite happens for a larger supply voltage.

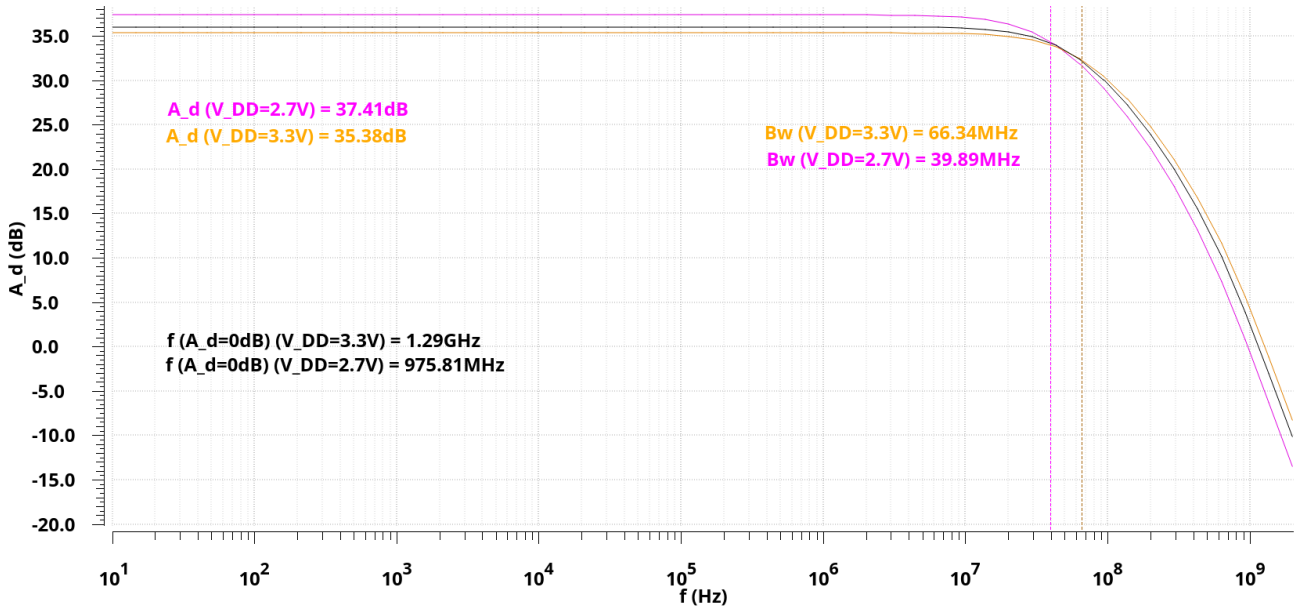

Figure 23: Supply voltage dispersion corners - frequency response of the differential mode gain.

With changes in the temperature, there is a significant modification in several parameters in the circuit, which overall lead to a lower A_d for a higher temperature, and vice-versa, as shown in Fig. 24.

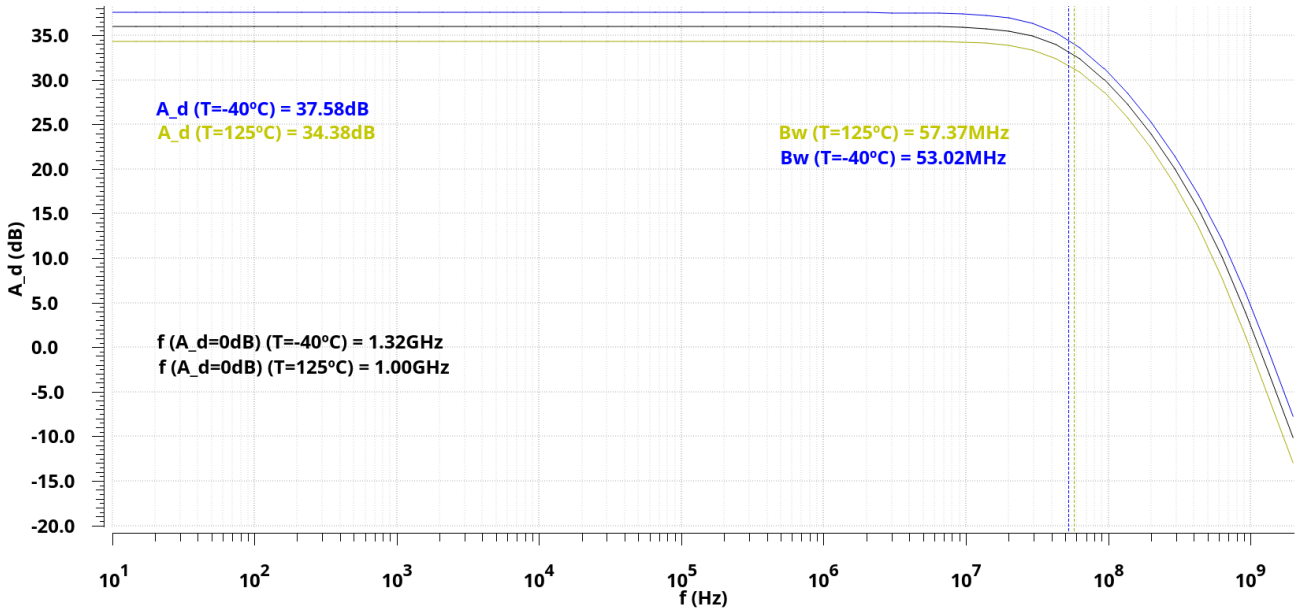

Figure 24: Temperature dispersion corners - frequency response of the differential mode gain.

By taking into account all corners variations (and the respective nominal values for temperature and supply voltage) simultaneously, the differential gain curves in Fig. 25 were obtained. As seen below, the minimum and maximum values of A_d at low frequencies occurred for the combination of conditions which, in each case described in Figs. 21-24, led to the lowest and largest values of A_d, respectively.

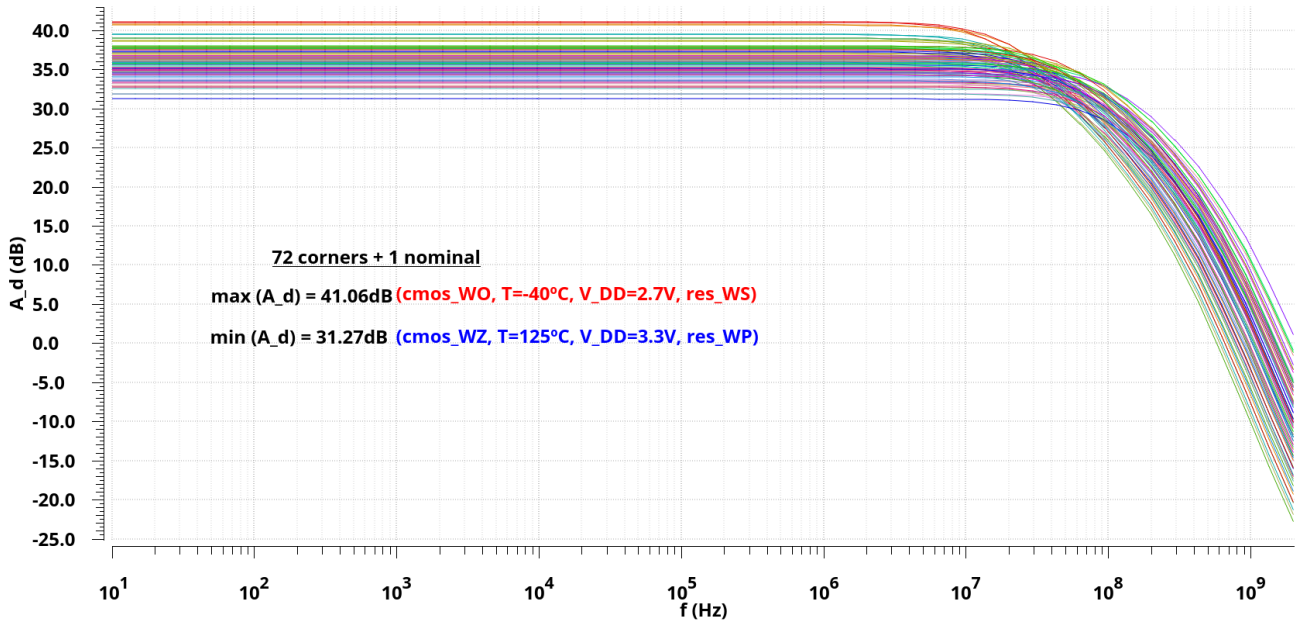

Figure 25: Simulations performed with every corner condition in consideration - frequency response of the differential mode gain.

3 OPAMP layout

A Layout XL window was launched with all the instances and I/O pins (in layer `MET4` and dimensions $10 \times 10\,\mu m^2$) generated from the schematic. Additionally, six pads (`g_padonly`, squares with 95 µm sides) from the library `IOLIB_ANA_4M` were inserted in the layout with a separation between centers equal to 120 µm in each row of three pads. These pads include layers of `MET1`, `MET2`, `MET3` and `MET4`, thus the connections between transistors and pins can be made directly with these metal layers; each pin (`vd_n`, `VDD`, `vd_p`, `VSS` and `vout`, in layer `PIN metal4`) is placed inside one of these pads (having two pads been used fo `VSS`). The vias used in this layout to perform the connections between the components consisted of `P1_C`, `VIA1_C` and `VIA2_C`, sometimes placed in stacks, having more than one column/row of contacts been placed in each case, in order to avoid compromising the circuit performance when disruption of one or more of the contacts occurs; the number of contacts may also be chosen depending on the current value in each case. The final layout design is presented in Fig. 26 and required a **total area** of $9.06 \times 10^4\,\mu m^2 = 335\,\mu m \times 270.45\,\mu m$.

Additionally, it is worth taking into account the substrate guard ring placed around the resistor, which connects to `VSS`. Moreover, a `pdiff_sub` guard ring is placed around the NMOS transistors, whose sources are connected to `VSS`. Around the PMOS transistors, a `ndiff_tub` guard ring is used and connected to `VDD`. However, in this case, since PMOS transistors should be placed in an n-well (as opposed to NMOS transistors, placed in a p-well, which exists over the entire substrate), a rectangle of `NTUB` is placed around all PMOS transistors, between the edges of the respective guard ring. These aspects are presented in more detail in Figs. 27 and 28.

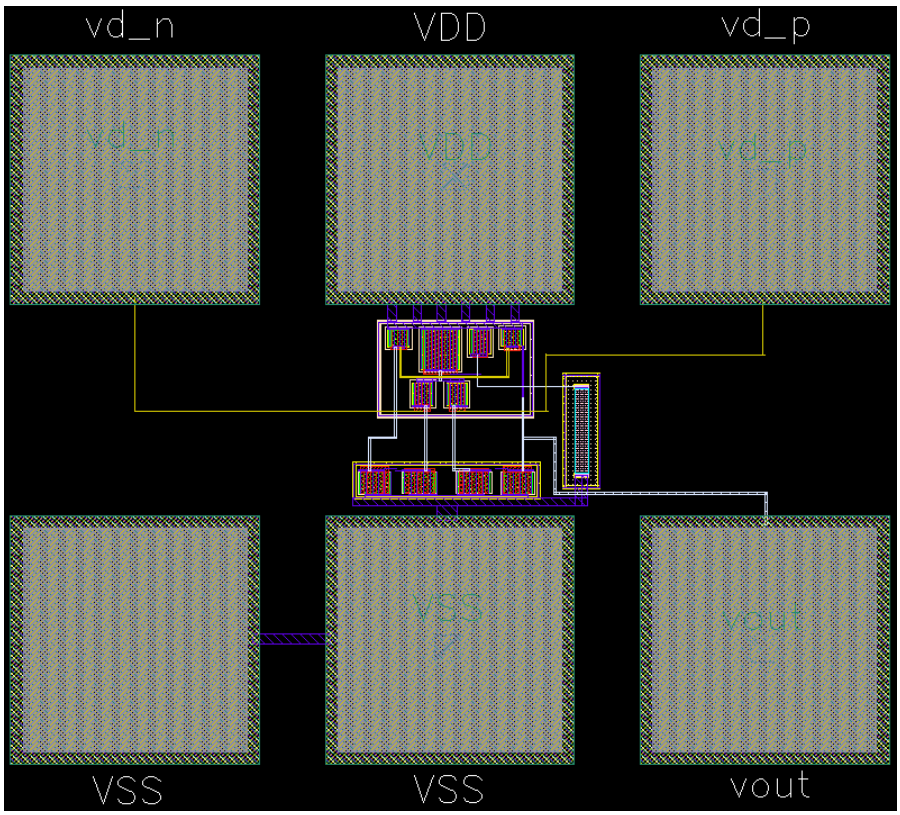

Figure 26: OPAMP layout design.

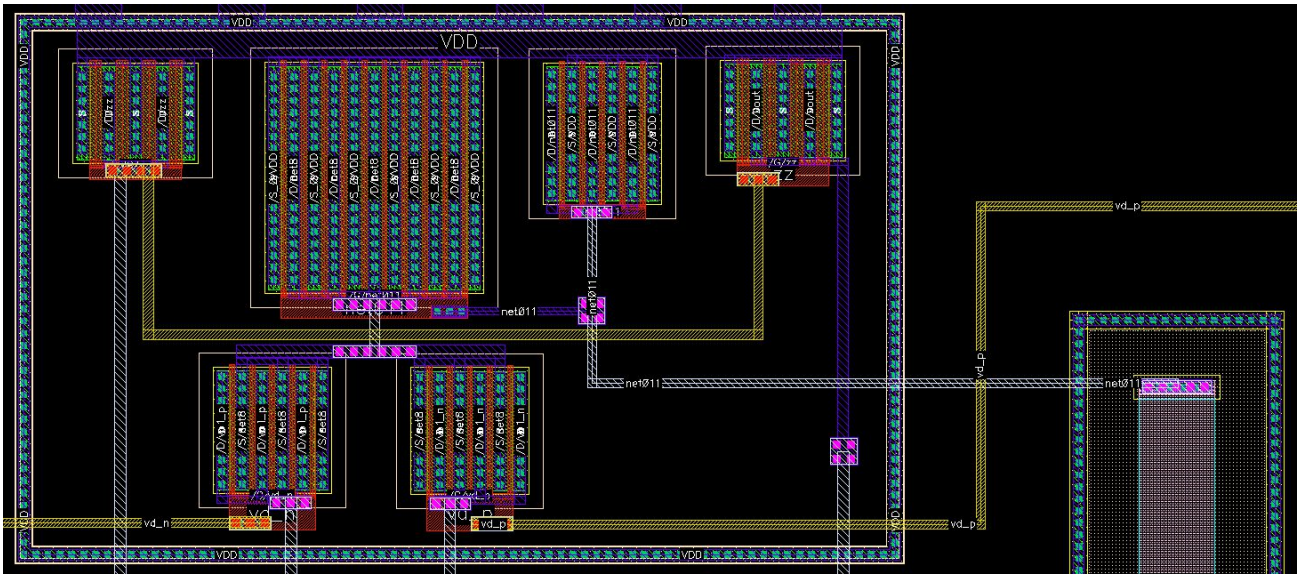

Figure 27: OPAMP layout design - detailed view of the PMOS transistors.

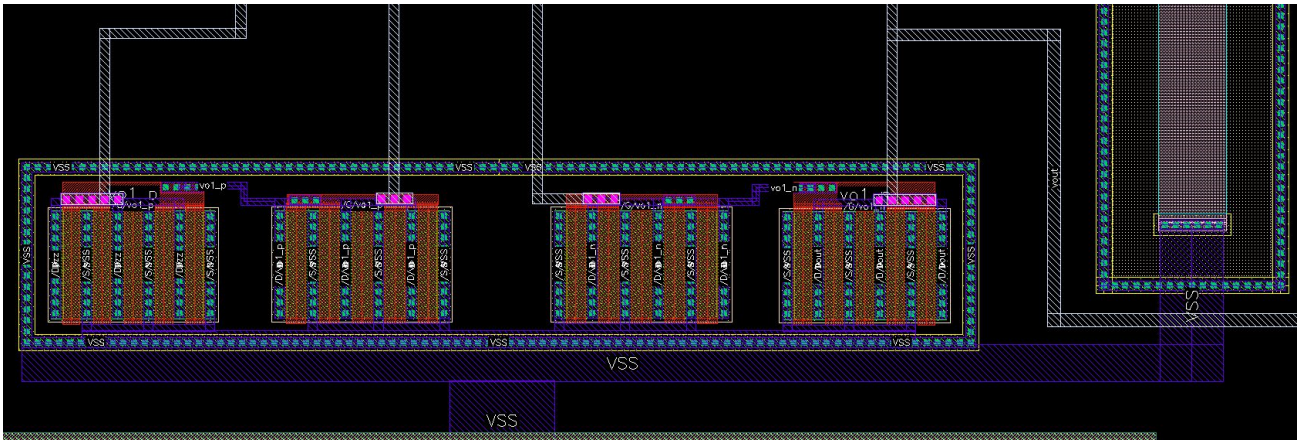

Figure 28: OPAMP layout design - detailed view of the NMOS transistors.

Finally, the Design Rule Check (DRC) program was ran (with `no_coverage`, `no_info` and `no_recommendation` switches) in order to verify if the design rules were respected and report any possible violations. The Layout Versus Schematic (LVS) verification was also performed to compare the circuit in the schematic with the one extracted from this layout. Finally, the parasitic capacitances (more significant than resistances in low frequency designs) were extracted from the layout in order to test their effect on the frequency response of the circuit. The results of these runs are showed in Fig. 29, whereas the new frequency response is depicted in Secs. 3.1 and 3.2. It is important to note that for this frequency response each transistor has the number of gates used in the layout phase to minimize the area, whereas the results shown in Sec. 2 were obtained for a single gate in each transistor. Moreover, the dimensions of the resistor were also decreased to minimize the area, while maintaining its resistance value as close as possible to the original value, as shown in Tab. 1. Despite these modifications, the results do not vary significantly and the main takeaways to be assessed from Secs. 3.1 and 3.2 are the effects of the parasitic capacitors on the circuit.

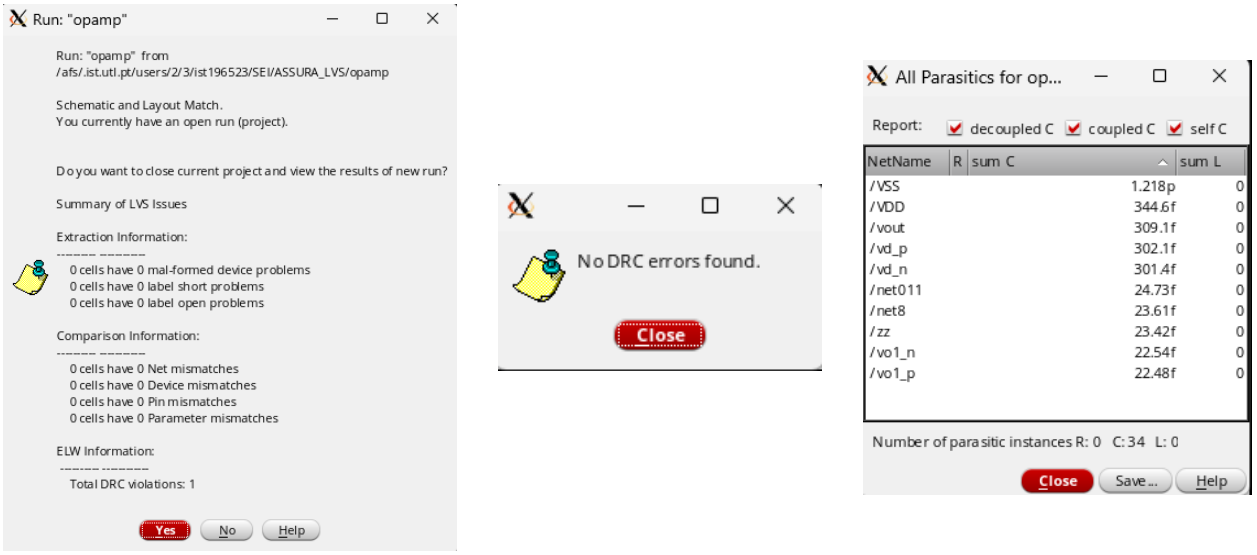

Figure 29: Results of LVS check, DRC and C parasitics extraction, respectively.

3.1 Frequency response of the differential and common-mode gains

As seen in Fig. 30, the inclusion of parasitic capacitances in the circuit does not alter the low frequency gains significantly. However, for higher frequency values, it is noticeable that both gains are lower than in the previous results. Since the values of these capacitances are very low (as shown in Fig. 29), a new dominant pole appears, leading to a lower bandwidth than before. The inclusion of new zeros and poles in the expression of the common-mode gain justifies the change in its frequency response shown below.

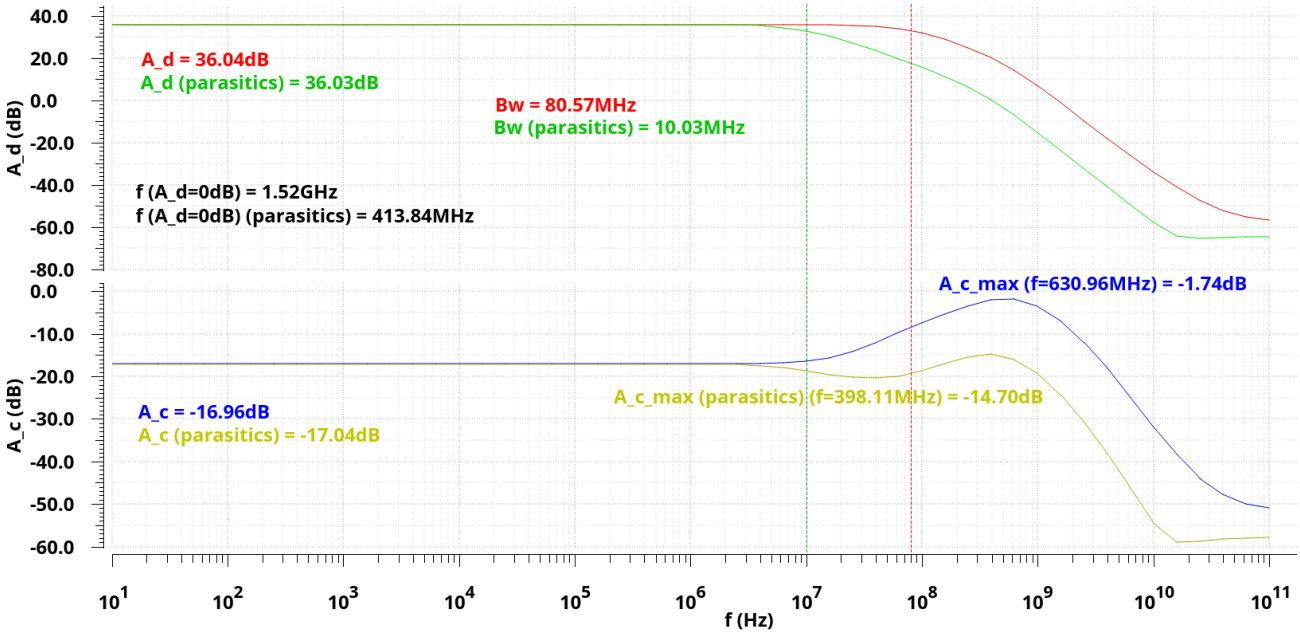

Figure 30: Frequency response of the differential and common-mode gains (A_d and A_c, respectively), before and after taking into account the parasitic capacitors.

Regarding the common-mode rejection ratio, shown in Fig. 31, its value remains similar at low frequencies, as expected. However, it is slightly lower than before for high frequencies, since A_d is now lower. Even then, since the (negative) value of A_c is also lower, the curve does not change as significantly. Due to the inclusion of new zeros and poles in the expression of the common-mode gain, the $A_c(f)$ curve presented a more irregular shape for very high frequencies; consequently, an irregular shape is also apparent in the $CMRR(f)$ curve.

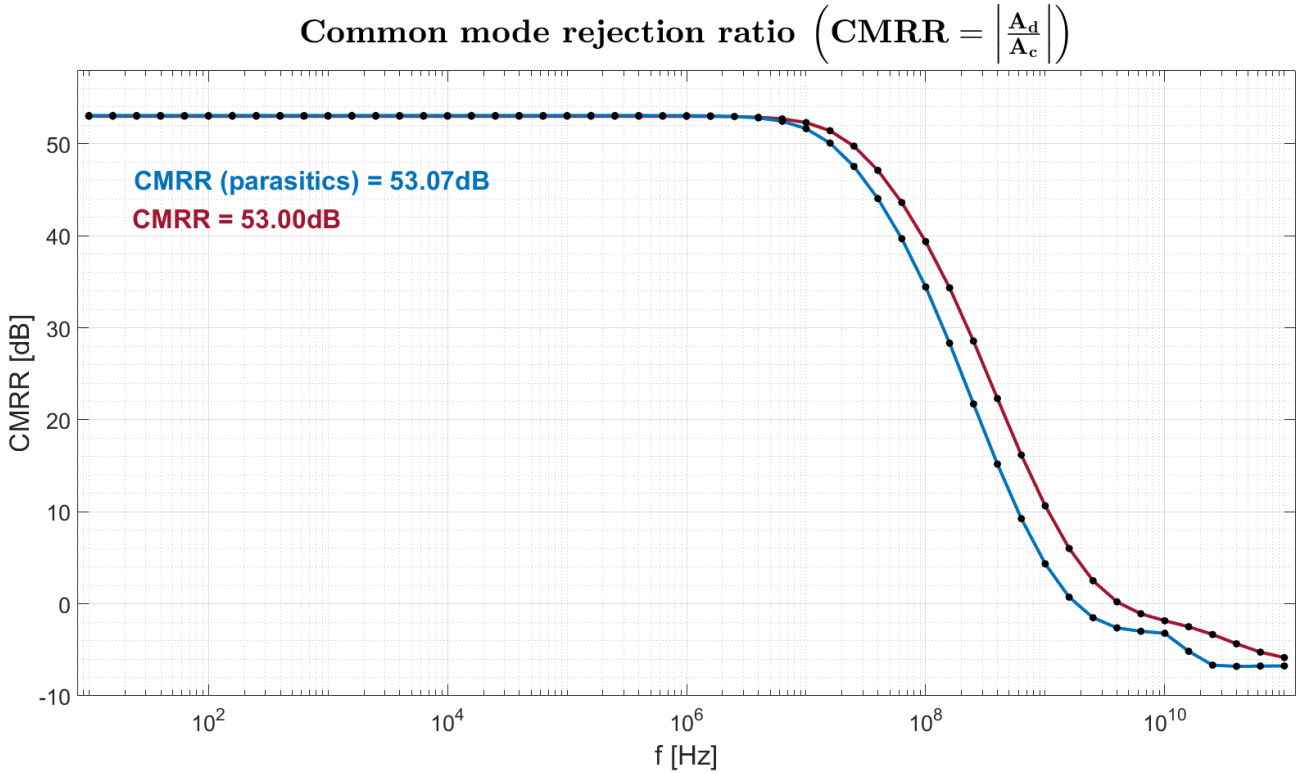

Figure 31: Frequency response of the common-mode rejection ratio (CMRR), before and after taking into account the parasitic capacitors.

3.2 Phase margin

Regarding the change in the phase margin, the results depicted in Fig. 32 make the presence of new poles apparent. In fact, the creation of a new low frequency dominant pole inside an OPAMP - for instance, by placing a capacitor - is a known strategy used to increase the phase margin, thus assuring stability in the circuit. This is exactly what happens in this case, where the inclusion of the parasitic capacitors leads to a lower dominant pole, which consequently increases the phase margin significantly, as shown in Tab. 10.

Table 10: Phase margin results, before and after taking into account the parasitic capacitors.

	Before parasitics	**After parasitics**
Phase ($\mathbf{A_d}$ = 0dB)	-172.39^o	-146.33^o
Phase margin	7.61^o	33.67^o

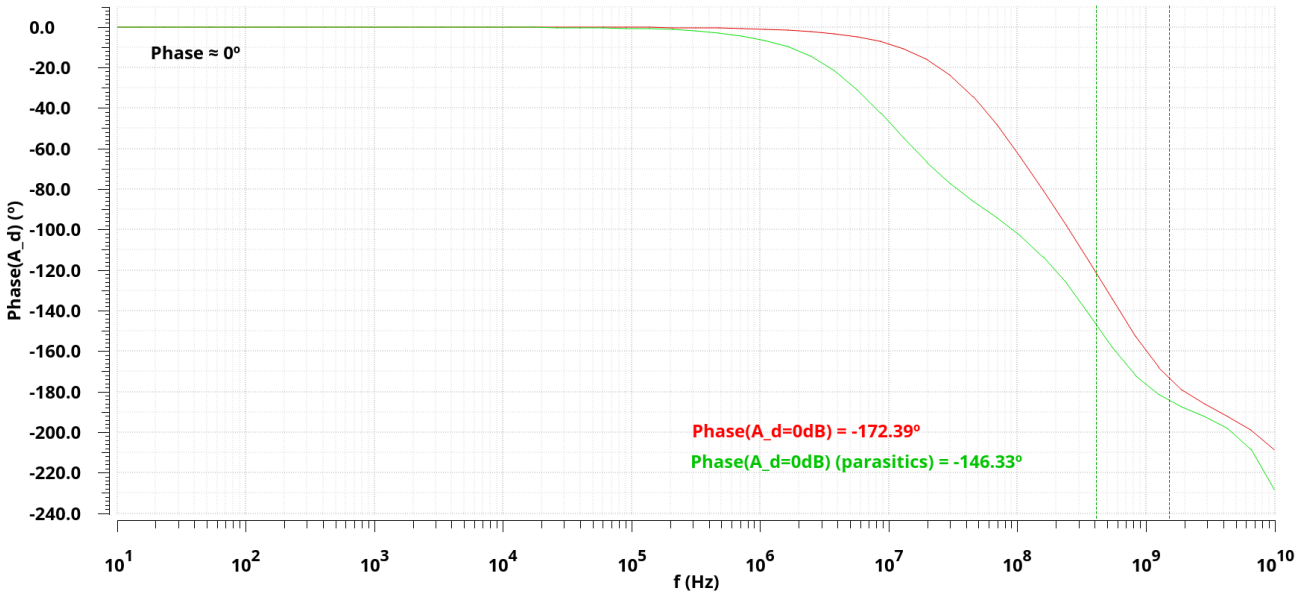

Figure 32: Frequency response of the phase of the differential mode gain, before and after taking into account the parasitic capacitors.

4 Conclusion

In summary, all of the proposed objectives for this project have been achieved. Having started by building a schematic for a one-stage operational amplifier with a PMOS differential pair biased by a current source, the dimensions of the circuit components were determined in order to comply with the circuit specifications - namely, a low frequency differential gain of $A_d = 36\,\text{dB}$, a current supply for the differential pair of 700 mA, a supply voltage of $V_{DD} = 3.0\,\text{V}$ and a maximum total supply current of 5 mA. The circuit specifications were verified using DC, AC and transient simulations, which allowed to determine other characteristics of the circuit, including: input and output impedances, input offset voltage (which stood at $V_{OS} = -9.51\,\mu\text{V}$), power supply rejection ratios ($PSRR^+$ and $PSRR^-$, which suggested that the circuit is more affected by fluctuations in v_{DD}), output and input common-mode voltage range (having the latter included 1.5 V), phase margin (with a value of 8.8°) and slew-rate. After this, the layout of this circuit was designed and verified with DRC and LVS check. The frequency response of the OPAMP containing the extracted parasitic capacitors showed a decrease in the value of the differential and common-mode gains for high frequencies, as well as a lower bandwidth, even though the phase margin increased, due to the creation of a new dominant pole in the circuit.