TÉCNICO LISBOA

DESIGN, TEST AND RELIABILITY OF ELECTRONIC SYSTEMS

1st Project

2023/2024

1. Specifications

The goal of this project is to develop a controller that fulfills the specifications presented below.

The controller must be described in **synthesizable Verilog**. The *Xilinx Vivado ML Edition* (available for download at www.xilinx.com/support/download.html) can be used to check whether the Verilog is synthesizable or not.

The controller must synthesize with the *Vivado* design suite **without any errors or warnings**. To check for these errors and warnings, choose the option *SYNTHESIS → Run Synthesis* that is available in the left pane.

To validate the behavior of the controller, the simulator included in the *Vivado* design suite can be used, the easiest to use due the integration in the design flow. To run the simulator use the option *SIMULATION → Run Simulation → Run Behavioral Simulation* that is available in the left pane.

To validate the quality of the testbench, the code coverage must be evaluated using the newest Cadence simulator (*Xcelium*) available in a remote Linux machine. The goal should be a code coverage of 100% for the *Block* and *FSM* categories. The instructions on the setup to obtain the code coverage are provided in the laboratory.

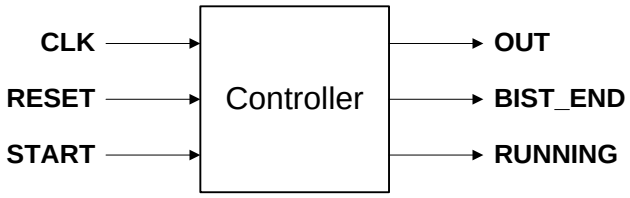

Figure 1: Controller interface

The names of the signals shown in Figure 1, as well as the sensitivity to the edges and logic levels mentioned below, **must be preserved**.

Figure 2 illustrates the behavior of the input and output signals. That information is complemented with a more detailed explanation of the controller inputs and outputs.

Controller inputs

CLK: The controller must be sensitive to the rising edges of the clock.

START: After a 0→1 transition in this signal, a new sequence must be initiated (see Figure 2). The START value is captured on the rising edge of the clock. While the full sequence is not completed (BIST_END signal set to HIGH), further transitions in the START signal must be ignored.

RESET: The RESET must be synchronous and active at the logic level '1'. This signal is used to restart the state machine and the counters, preparing the controller to start a new sequence. When the RESET signal goes LOW and the START signal is HIGH, a new sequence **must not** be restarted. The controller must wait for a 0→1 transition in the START signal to start a new sequence.

Note: When the sequence is complete, a 0→1 transition in the START signal is enough to restart a new sequence. The activation of the RESET signal is not necessary in this case.

Controller outputs

OUT: Must have the behavior illustrated in Figure 2. If the RESET signal goes HIGH, then this signal must go LOW.

BIST_END: The BIST_END signal must go HIGH when the sequence represented in Figure 2 is completed. The BIST_END signal must go LOW when the RESET signal is activated or the START signal has a 0→1 transition.

RUNNING: Must be HIGH while the controller is generating the OUT signal, as illustrated in Figure 2. If the RESET signal goes HIGH, then this signal must go LOW.

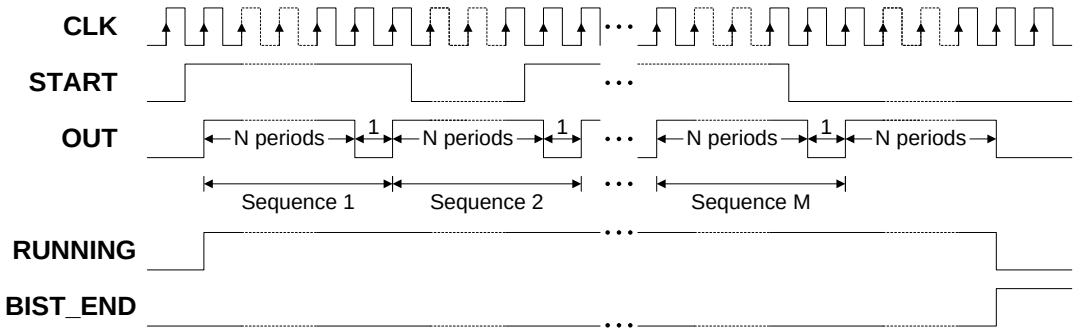

Figure 2: Waveforms

NOTES: The number of periods, **N**, and the number of sequences, **M**, is defined group by group. However, these values **must be defined as parameters** in your Verilog code, to be easily adjustable in the future.

The behavior of the START signal is just an example to indicate that all transitions of this signal during the generation of the sequence are discarded.

Figure 3 presents the simulation results for N = 3 and M = 6. This example corresponds to a basic test that starts with a reset to initialize the state machine. When the reset is disabled (1→0 transition), the **START** signal is activated to initiate the desired sequence.

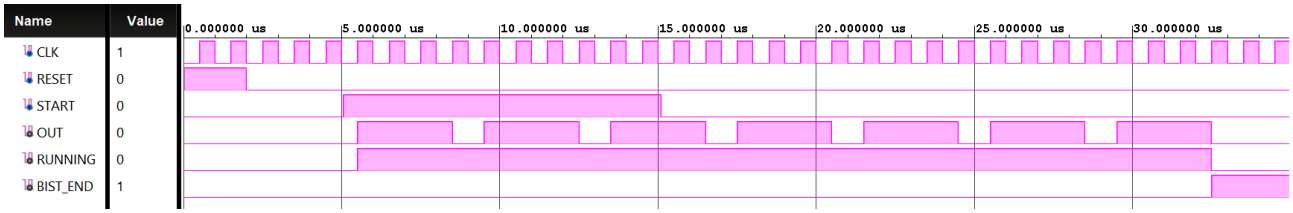

Figure 3: Basic simulation example for N = 3 and M = 6

2. Report

The short report must include, at least, the following items:

- State diagram of the state machine
- Textual description of each state of the state machine
- Description of the test scenarios that are included in your *testbench* (activation of the RESET while the sequence is running, reactivation of the START while the sequence is running, etc.).

The Verilog code and the *testbench* must be sent by email to the teacher.

3. Delivery

The delivery package must be submitted in the **Fenix** and must include, at the least, the following items:

- Report
- Verilog code
- Testbench
- Synthesis report generated by the *Vivado* design suite
- Code coverage report generated by the *Xcelium* simulator

4. Evaluation Criteria

The evaluation is based on the following criteria:

- Quality of the Verilog code: **25%** (synthesis errors and warnings have a negative impact in this criteria)
- Quality of the report: **35%**
- Code coverage results: **10%**
- Simulation results: **30%**