# Final Target: Project of a Folded Cascode Amplifier with NMOS Input Differential Pair

Bologna Master Degree in Electrical and Computer Engineering (MEEC)

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## 1) Introduction

This report regards the final stage of the project initiated in the previous laboratory assignment (middle target), in which a folded cascode amplifier with an NMOS input differential pair was projected in order to fulfill the specifications shown in Table 1. This led to the schematic shown in Figure 1, in which the respective widths of the transistors are indicated. The main objective of the current laboratory assignment is to design the respective layout, along with analysing and comparing the simulation results obtained from the schematic and the extracted view. This report intends to explain the decisions made regarding the layout design process, validate it with the results of DRC and LVS, perform the transistor level extraction and use this view to re-run all the simulations performed for the middle target report.

| Parameter | Value |
|---|---|
| Supply voltage, $\mathrm{V_{DD}}$ [V] | 3.3 |
| Small signal gain, $\mathrm{A_v}$ [dB] | 66 |
| Bandwidth, $\mathrm{Bw}$ [kHz] | 10 |
| Phase margin, $\mathrm{PM}$ [°] | 60 |
| Load capacitance, $\mathrm{C_L}$ [pF] | 5 |
| Slew-rate, $\mathrm{SR}$ [V/$\mu$s] | 10 |
| Current budget, $\mathrm{I_{DD}}$ [$\mu$A] | 400 |
| Die area budget [$\mathrm{mm^2}$] | 0.01 |

**Table 1:** Specifications imposed for the folded cascode OTA.

## 2) Layout design

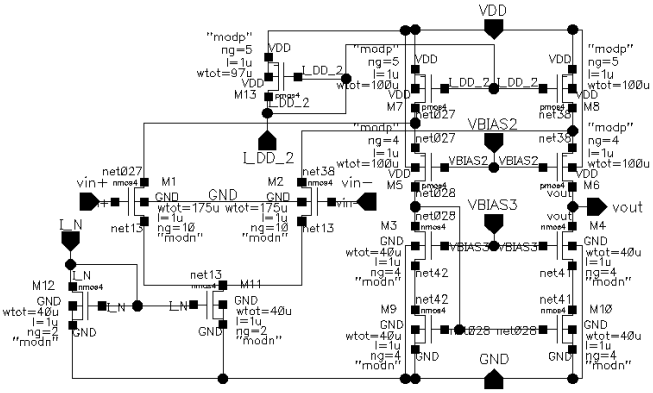


**Figure 1:** Schematic of the folded cascode amplifier with current mirrors designed in the previous laboratory assignment.

The first step of the design process was to initialize the layout by importing the transistors and required pins from the schematic; this resulted in their automatic placement without the required connections. An important aspect to take into account here is the number of gates in each transistor. When implementing the schematic, changing the number of gates led to a negligible impact on the results. However, this parameter now needs to be properly selected, since it strongly affects the size of the transistors in the layout. Having different implementations been tested, the following number of gates were eventually fixed for each transistor: 10 gates for the differential pair (transistors $\mathrm{M_1}$ and $\mathrm{M_2}$); 5 gates for the upper PMOS transistors ($\mathrm{M_7}$, $\mathrm{M_8}$ and $\mathrm{M_{13}}$); 2 gates in the NMOS current mirror ($\mathrm{M_{11}}$ and $\mathrm{M_{13}}$); 4 gates for the remaining transistors.

Moreover, the die area budget restrain shown in Table 1 needs to be considered. In the middle target, a preliminary area estimate of $1.087 \times 10^{-3}\mathrm{mm^2}$ was determined; however, this calculation leads to a substantial underestimate, since only the channel widths and channel lengths of the transistors (which are referred to the gate dimensions) were taken into account - in reality, the total width and length of the transistors in the design need to be regarded.

The main concerns regarding the placement of the components in the layout design were the following:

- **Relative placement of the transistors** in the layout - in order to simplify the connections and make the respective wires shorter. The smaller the length of the wires, the smaller the resulting resistance, implying less power dissipation. The proper planning of these placements is also made to avoid wire crossing, thus reducing the need to change between metal layers. However, it is worth noting that, even though approximating two transistors makes the respective connecting wires shorter, it also increases the capacitance between the components.
- **Grouping of PMOS and NMOS transistors**, with a clear separation between them - this avoids diffusion problems and facilitates the substrate connections, since a single n-well is created for all PMOS transistors, therefore reducing the complexity of the respective mask.
- **Orientation of contacts** (gates, drain and source fingers), allowing for easier connections, direct access to VDD and GND (when needed) and reducing of mask complexity.
- **Use of vias** to interconnect different layers, since the pins, drains and sources are in MET1 and the gates are in polysilicon (POLY1).
- **Use of MET2** - as stated previously, jumping between metal layers was avoided; however, two connections needed the use of MET2 to cross through MET1 wires.
- Respecting the **minimum distance** between components in the same layer and the **minimum width** for the different layers, along with all other design rules.

Once the proper placement of the transistors, GND and VDD rectangles (MET1), substrate connections and vias had been done - along with the adequate connections -, an initial version of the layout was obtained. As mentioned before, a layout must be drawn according to a set of strict design rules. Therefore, it needs to be validated with a DRC (Design Rule Check), during which the program checks the design against the design rules and reports any violations. This initially resulted in multiple errors, mainly regarding the distance between same layer components and minimum width of wires. In order to fix these problems, some changes in placing, sizes and wire paths had to be made, after which no violations were highlighted in the layout. The resulting layout is shown in Figure 2.

After this, a Layout-versus-Schematic (LVS) check was performed to compare the circuit given by the schematic with the one extracted from the mask layout and prove that both networks are equivalent. This LVS step provides an additional level of confidence for the integrity of the design and ensures that the mask layout is a correct realization of the intended circuit. It is worth noting that the LVS check only guarantees topological match; a successful LVS check will not guarantee that the mask layout of the cell will actually satisfy the performance requirements. Luckily, a clean report was obtained, thus another LVS was done with `resimulate_extracted` switch to get the correct connectivity for parasitic layout extraction (PEX). After this, the view `av_extracted` was obtained by running QRC. The validation results obtained with DRC, both LVS and QRC are shown in Figure 3.

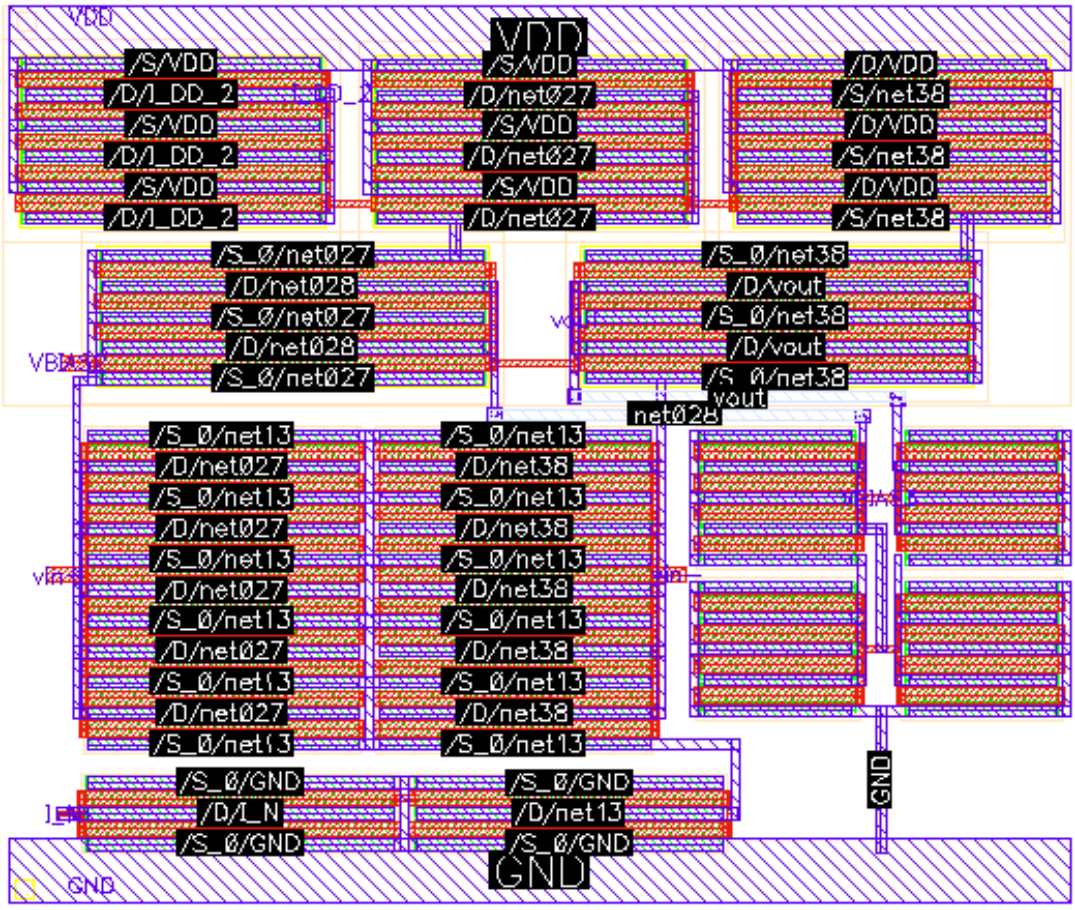


**Figure 2:** Layout of the folded-cascode amplifier.

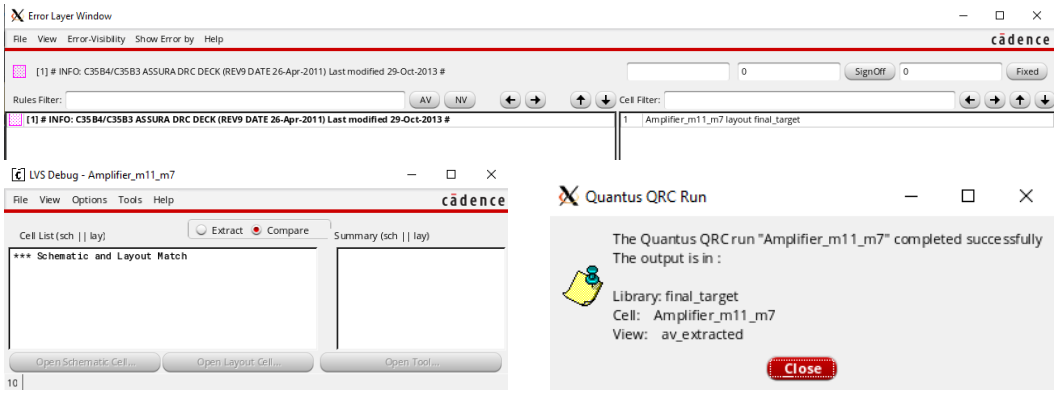


**Figure 3:** Validation of the layout by performing DRC (Design Rule Check), LVS (Layout Versus Schematic) and QRC (Quantus Extraction Solution), respectively (the same report was obtained for both LVS checks).

### 3) Pos-layout simulations

For the transistor level extraction with QRC, an RC extraction type was selected. The generated view `av_extracted` was then used in the ADE to run pos-layout simulations and compare these results with the values obtained in the middle target with the schematic. A detailed of the extracted view is shown in Figure 4, in which it is clear that several resistances, capacitances and transistors were added to the circuit model. The results obtained in these simulations (typical, corners and Monte Carlo) are shown in Figure 5 and Table 2. As seen there, a slight decrease in the small signal gain was obtained - in particular, a difference of $-1.1\text{dB}$ is seen for "typical". However, the bandwidth increased in most cases, remaining above the imposed $10\text{kHz}$. Moreover, the phase margin always remained above $60^\circ$. Referring to the slew-rate, a higher value was now obtained. A slight increase was also seen in $\text{I}_{\text{DD}}$, but it (always) remained below the imposed current budget of $400\mu\text{A}$. A lower CMRR (Common-Mode Rejection Ratio) was also obtained in most cases - due to lower differential gain and higher common mode gain. It is worth noting that, even though analogous curves were now obtained in corner analysis - when compared to the previous report -, the difference is more significant in Monte Carlo simulations, in which the curves are much closer to each other. In fact, this leads to a smaller amplitude in most intervals shown in Table 2 since, while using the schematic, more significant discrepancies were obtained in MC 3 - which led to higher overall variations in the parameter values. Regarding the DFT, very similar results were now obtained for the Signal-to-Noise Ratio (SNR), Spurious Free Dynamic Range (SFDR) and Total Harmonic Distortion (THD), even though "typical" provided slightly lower SNR and SFDR, along with a slightly higher THD. This is due to the inclusion of resistances and capacitances in the extracted view, which respectively increase the noise and crosstalk in the circuit.

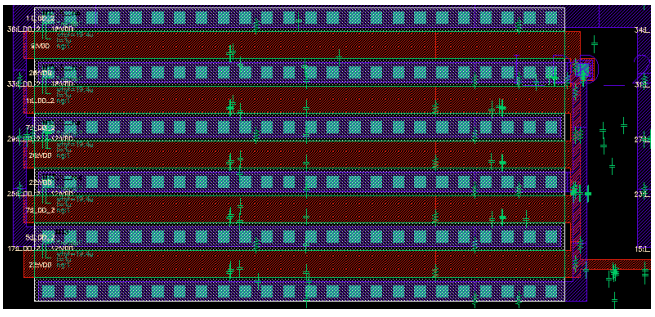

**Figure 4:** Detailed view of transistor $\text{M}_{13}$ included in `av_extracted`.

Considering the layout shown in Figure 2, a total **area** of $\mathbf{0.004mm^2}$ - lower than the imposed die area budget of $0.01\text{mm}^2$ - was measured. By running transient analyses with different amplitudes in the input sine wave, an **output dynamic range** of $\mathbf{13.33dB}$ (corresponding to $\text{V}_{\text{out}_{\text{max}}} = 3.08\text{V}$ and $\text{V}_{\text{out}_{\text{min}}} = 664\text{mV}$, in which saturation is reached) - very similar to the original value of $13.35\text{dB}$ - was obtained. Moreover, an **input dynamic range** of $\mathbf{9.40dB}$ (corresponding to $\text{V}_{\text{in}_{\text{max}}} = 2.48\text{V}$ and $\text{V}_{\text{in}_{\text{min}}} = 0.84\text{V}$, in which $90\%$ of $\text{A}_\text{v} = 65.37\text{dB}$ is reached) was determined in both cases.

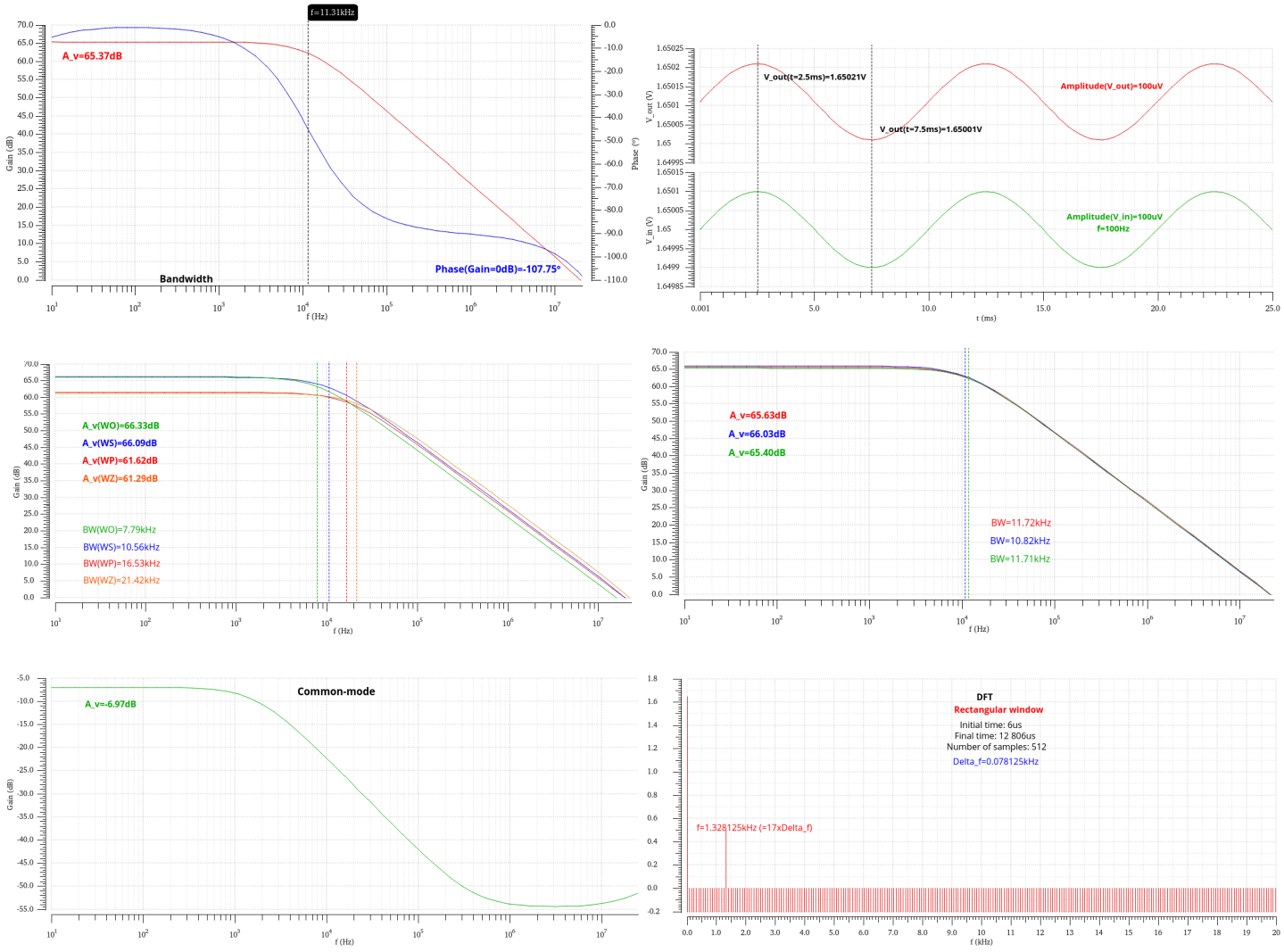


**Figure 5:** On the top left, desired gain and bandwidth curves; on the top right, transient simulation results; in the middle, performance of the circuit in corner analysis and Monte Carlo simulations (respectively); on the bottom left, common-mode gain curve; on the bottom right, Discrete Fourier Transform with a rectangular window.

| Simulations | $\text{A}_\text{v}$ [dB] | | Bw[kHz] | | PM[°] | | SR[V/$\mu$s] | | $\text{I}_{\text{DD}}$[$\mu$A] | | CMRR[dB] | | SNR[dB] | | SFDR[dB] | | THD[%] | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | S | E | S | E | S | E | S | E | S | E | S | E | S | E | S | E | S | E |
| **Typical** | 66.47 | 65.37 | 10.22 | 11.31 | 76.26 | 72.25 | 10.41 | 10.99 | 370.6 | 371.0 | 74.92 | 72.34 | 59.35 | 58.19 | 67.52 | 65.30 | 0.11 | 0.12 |
| WP | 62.63 | 61.62 | 14.86 | 16.53 | 80.12 | 77.22 | 10.96 | 10.77 | 376.5 | 377.8 | 83.14 | 77.06 | 57.41 | 57.27 | 63.50 | 63.45 | 0.13 | 0.14 |
| WS | 67.00 | 66.09 | 9.72 | 10.56 | 69.76 | 64.75 | 7.32 | 6.66 | 368.3 | 367.5 | 67.98 | 66.71 | 60.06 | 60.43 | 66.58 | 69.42 | 0.10 | 0.10 |
| WO | 67.35 | 66.33 | 7.10 | 7.79 | 78.64 | 74.99 | 8.84 | 8.98 | 366.9 | 368.9 | 78.94 | 82.70 | 58.11 | 58.21 | 63.92 | 63.92 | 0.12 | 0.12 |
| WZ | 62.18 | 61.29 | 19.70 | 21.42 | 68.30 | 64.20 | 8.90 | 8.03 | 377.4 | 376.8 | 67.35 | 65.64 | 59.69 | 60.19 | 66.82 | 68.40 | 0.10 | 0.10 |
| MC 1 | 66.55 | 65.63 | 10.99 | 11.72 | 74.72 | 71.26 | 11.88 | 10.80 | 377.0 | 377.6 | 66.70 | 75.48 | 58.68 | 56.25 | 67.34 | 64.08 | 0.12 | 0.15 |
| MC 2 | 65.34 | 66.03 | 11.47 | 10.82 | 77.00 | 72.05 | 10.99 | 10.93 | 372.9 | 374.0 | 71.01 | 69.09 | 58.57 | 56.82 | 67.48 | 63.63 | 0.12 | 0.14 |
| MC 3 | 61.35 | 65.40 | 21.12 | 11.71 | 62.34 | 72.50 | 8.23 | 10.94 | 378.1 | 370.4 | 95.27 | 57.23 | 56.51 | 58.39 | 63.40 | 65.34 | 0.15 | 0.12 |

| Interval | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | S | [61.35,67.35] | | [7.10,21.12] | | [68.30,80.12] | | [7.32,11.88] | | [368.3,378.1] | | [66.70,95.27] | | [56.51,60.06] | | [63.50,67.52] | | [0.10,0.15] | |
| | E | [61.29,66.33] | | [7.79,21.42] | | [64.20,77.22] | | [6.66,10.99] | | [367.5,377.8] | | [57.23,82.70] | | [56.25,60.43] | | [63.45,69.42] | | [0.10,0.15] | |

**Table 2:** Final results obtained for the folded cascode amplifier with the initial schematic [S] and the extracted view [E].

## 4) Conclusion

In this laboratory assignment, the project of the folded-cascode amplifier with an NMOS input differential pair has been concluded. The layout for this OTA was initially designed from the previously developed schematic, taking into account several main concerns - such as the number of gates in the transistors and design rules. Having the layout been validated with DRC and LVS checks, transistor level extraction was performed in order to obtain the view `av_extracted`, with which simulations analogous to the middle target procedure were performed. Even though the small signal gain remained $0.63\text{dB}$ below the imposed $66\text{dB}$, the bandwidth, phase margin, slew-rate and die area budget all satisfied the imposed specifications shown in Table 1. Moreover, less discrepancies were observed in the values of the parameters, mostly due to significant changes in the Monte Carlo simulations results. Regarding SNR, SFDR and THD, slightly different values were obtained due to the inclusion of capacitances and resistances in the circuit. Taking these results into consideration, it can be asserted that the proposed objective of designing an amplifier according to a set of specifications has been achieved.