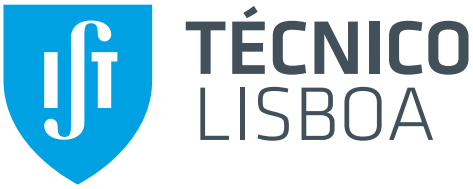

BATCHARGERctr

Datasheet

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Revision History

Version	Date	Description
1v0	December 23rd 2022	First version of charger controller block

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1. General description

The battery charger controller block coordinates the current mode of the power block - Trickle Charge (TC), Constant Current (CC) or Constant Voltage (CV) - based on the battery temperature, current and voltage provided as digital words from the ADC. The charging process of the CC/CV consists of three steps. Initially, safety and protection checks are performed by verifying if the battery initial conditions (temperature and open circuit voltage) are in the respective normal ranges. TC mode is used to charge the battery (with a small current) in case the voltage is lower than $\mathrm{V_{cutoff}}$, until it increases above it. Once $\mathrm{V} \geq \mathrm{V_{cutoff}}$, CC mode is used to further charge the battery. Finally, when the battery voltage reaches $\mathrm{V_{pre-set}}$ (preset maximum charging voltage), the process switches to CV mode, in which charging voltage is held constant at $\mathrm{V_{pre-set}}$ and the charging current decreases exponentially - the charging process stops when the charging current reaches a preset small current. When the system leaves CV mode or is not ready to enter CC nor TC modes, it goes to `start` once again, thus the charging process can be reinitiated - the charger can continue its operation after the first charging cycle ends. The monitoring of the battery temperature is carried permanently.

2. Block Diagram

The charger controller diagram is presented in Figure 1.

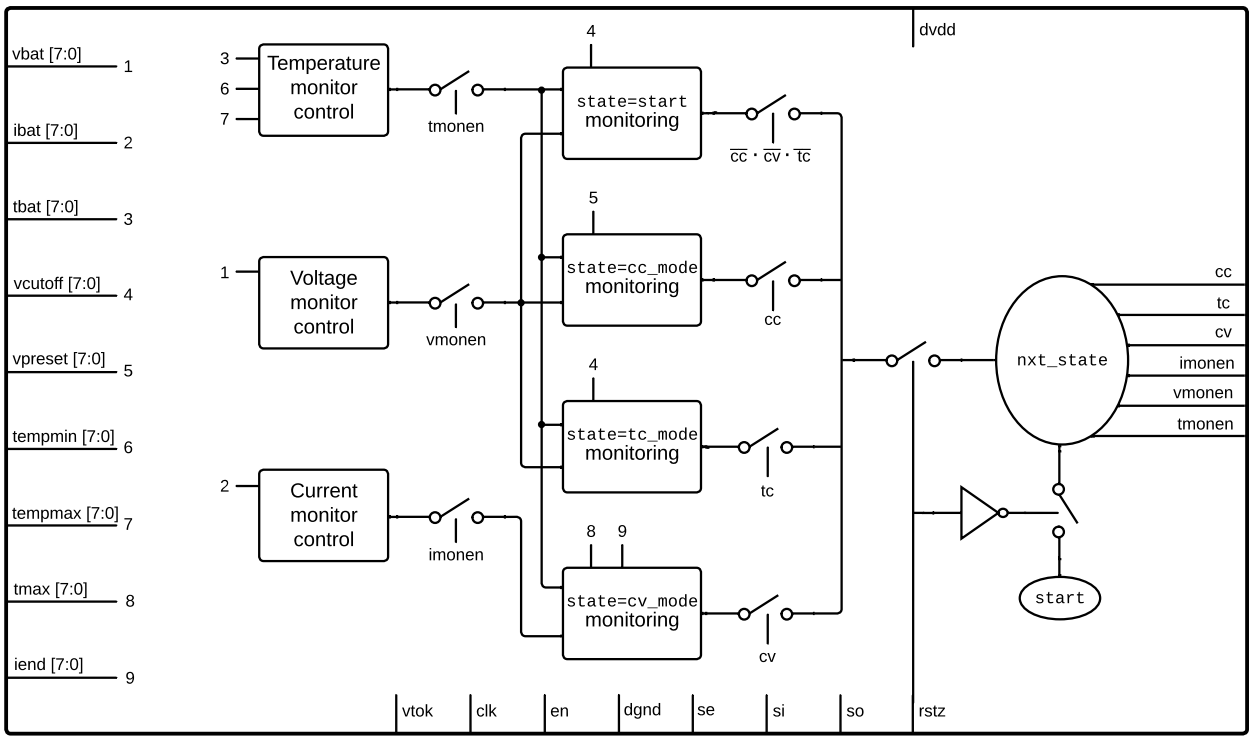

Figure 1: Charger controller diagram.

3. Pinning

Pin	Type	Dir	Supply	Description
cc	Digital	O	dvdd	Enables constant current mode
tc	Digital	O	dvdd	Enables trickle charge mode
cv	Digital	O	dvdd	Enables constant voltage mode
imonen	Digital	O	dvdd	Enables the current monitor
vmonen	Digital	O	dvdd	Enables the voltage monitor
tmonen	Digital	O	dvdd	Enables the temperature monitor
vtok	Digital	I	dvdd	Signals that voltage and temperature values are valid
vbat[7:0]	Digital	I	dvdd	8 bits data from ADC with battery voltage; vbat=adc(vref=0.5V, battery_voltage/10)
ibat[7:0]	Digital	I	dvdd	8 bits data from ADC with battery current; ibat=adc(vref=0.5V, battery_current*Rsens), Rsens=0.5*vref/(0.5C), where C is the nominal capacity of the battery, with vadc(Ibat=0.5C)=vref/2
tbat[7:0]	Digital	I	dvdd	8 bits data from ADC with battery temperature; vadc = Temp/330+20/165, tbat=adc(vref=0.5V, vadc), vadc(-40º)=0V and vadc(125º)=0.5V
vcutoff[7:0]	Digital	I	dvdd	Voltage threshold for exiting TC mode; vcutoff=Vcutoff_dec*255/5=51*Vcutoff_dec (for example, 2.9V $\rightarrow$ 1001_0011)
vpreset[7:0]	Digital	I	dvdd	Voltage for CV mode; vpreset=Vpreset_dec*255/5=51*Vpreset_dec (for example, 3.7V $\rightarrow$ 1011_1100)
tempmin[7:0]	Digital	I	dvdd	Minimum temperature, see tbat for scaling
tempmax[7:0]	Digital	I	dvdd	Maximum temperature, see tbat for scaling
tmax[7:0]	Digital	I	dvdd	Maximum charge time, unit is 2ˆtime_div_bits clock cycles
iend[7:0]	Digital	I	dvdd	Charge current to be used as end of charging criteria (for example: 0.01C=0.01*3.5=0.035$\rightarrow$0000_0010)
clk	Clock	I	dvdd	State machine clock
en	Digital	I	dvdd	Enables the module (if en=1'b0, it is disabled)
rstz	Digital	I	dvdd	System reset (if rstz=1'b0, the charger controller is reset)
dvdd	Power	I/O	-	Digital logic supply
dgnd	Power	I/O	-	Digital logic ground
se	Digital	I	dvdd	Enable for scan digital test (se=0 for normal mode, se=1 for scan mode)
si	Digital	I	dvdd	Scan-in for scan digital test
so	Digital	O	dvdd	Scan-out for scan digital test

4. Detailed description

It is the responsibility of the controller to activate only one of the input signals tc, cc or cv at each moment, in order to activate the respective mode of operation. In case the system reset parameter is set at rstz=0, the charger controller remains in `start` mode; if not, it can change to TC, CC or CV mode if certain conditions are verified. In `start`, the parameters cc, cv, tc, imonen, vmonen and tmonen remain in their "default" values - only the latter two are at '1', since the voltage and temperature should be monitored.

Trickle charge (TC) mode

This mode is used to recover the battery from a very discharged state and is enabled when tc=1'b1. This happens when, if initially in `start`, the battery voltage does not rise above 4.2V (which corresponds to the binary value 8'b1101_0110) nor vcutoff - i.e., in case the conditions vbat>8'b1101_0110 and vbat>vcutoff are not true. Additionally, the temperature must be in normal range, thus tempmin$\leq$tbat$\leq$tempmax.

In TC mode, cc and cv remain at zero, as well as imonen, since there is no need to monitor the current value. However, vmonen and tmonen remain at '1' to monitor the battery voltage and temperature, respectively.

Constant current (CC) mode

This mode is usually used in the first part of the charging process. The constant current mode is enabled when cc=1'b1. If previously in `start` mode, the controller changes to CC mode in case the temperature is in normal range (tempmin$\leq$tbat$\leq$tempmax) and both conditions vbat$\leq$8'b110_0110 and vbat>vcutoff are verified.

In this mode, the exit condition is given by the voltage, thus vmonen remains at '1', as well as tmonen (since the temperature is always monitored); on the other hand, cv, tc and imonen remain null.

Constant voltage (CV) mode

This mode is usually used in the last part of the charging process. The constant voltage mode is enabled when cv=1'b1. From CC mode, cv changes to this value when the temperature is is normal range (tempmin$\leq$tbat$\leq$tempmax) and vbat$\geq$vpreset. Once the temperature leaves its normal range (tbat<tempmin or tbat>tempmax), the battery current decreases below a certain value (ibat<iend) or tmax[7:0]$\leq$timecv[15:8] (the maxiimum time is surpassed), CV mode is exited and the next state is `start`.

In this case, both the current and temperature are monitored (thus, imonen=tmonen=1), but not the voltage (vmonen=0); the parameters cc and tc are at '0'.

The 16-bit register timecv was created in order to check when the time condition to exit CV mode is verified. The constant tmax (maximum charge time) is defined in units of 2^8 clock cycles. Thus, (only) when in CV mode, timecv is added 16'h0001 for each 2^8 clock cycles and, by comparing the 8 most significant bits of this parameter to tmax, it is therefore possible to check if the maximum charge time in CV mode is surpassed. When not in CV mode or when rstz=0 (reset is activated), timecv remains constant at 16'b0.

5. Characteristics

Note: values are provided from vin=4.5V and T=25ºC unless different information is detailed.

Parameter	Min	Typ	Max	Unit
Reference current vref	0.45	0.5	0.55	V
Supply voltage vin	3.0	-	5.0	V
Power Dissipation	-	95.6	-	μW
Area	2016.0	2419.2	-	μm^2
Clock Frequency f_{clk}	-	100.0	101.8	MHz

6. Assembly guidelines

Pin	Recommendation
cc	Digital signal. No special recommendation.
tc	Digital signal. No special recommendation.
cv	Digital signal. No special recommendation.
imonen	Digital signal. No special recommendation.
vmonen	Digital signal. No special recommendation.
tmonen	Digital signal. No special recommendation.
vtok	Digital signal. No special recommendation.
vbat[7:0]	Digital signal. No special recommendation.
ibat[7:0]	Digital signal. No special recommendation.
tbat[7:0]	Digital signal. No special recommendation.
vcutoff[7:0]	Digital signal. No special recommendation.
vpreset[7:0]	Digital signal. No special recommendation.
tempmin[7:0]	Digital signal. No special recommendation.
tempmax[7:0]	Digital signal. No special recommendation.
tmax[7:0]	Digital signal. No special recommendation.
iend[7:0]	Digital signal. No special recommendation.
clk	Noisy line, keep away from sensitive analog signals.
en	Digital signal. No special recommendation.
rstz	Digital signal. No special recommendation.
dvdd	Consider as noisy supply signal.
dgnd	Consider as noisy supply signal.
se	Digital signal. No special recommendation.
si	Digital signal. No special recommendation.
so	Digital signal. No special recommendation.

7. Test

Scan test

For testability and communication purposes, the proper pins si, se and so were added to perform scan test and simulate the charger controller at gate level. In this aspect, logic synthesis led to an estimated area of 2016.0 μm^2 (using fsc0h_d_generic_core_ss1p08v125c.lib). Automatic Test Pattern Generators (ATPG) in the software modus provided a fault coverage value of 99.53% for the gate level controller.

8. Datasheet status

Preliminary.