

Instituto Superior Técnico

Sistemas de Processamento de Sinais

Multirate signal processing

- 1) A digital signal processing system operates with a sampling frequency fs = 5 kHz but it is required to reduce this frequency to fs = 4 kHz. Sketch the block diagram of the multirate signal processing system which implements this reduction. Specify each block and sketch the spectrum of the different signals. State if there is information loss and explain why.
- 2) Consider that the interpolator anti-image filter is a FIR filter with N=12 coefficients implemented using a polyphase structure. Sketch the signal flow diagram and determine the computational economy with respect to the direct form I implementation.
- 3) Consider using a CIC (Cascade Integrator Comb) filter in the decimator of a software radio system. After shifting the spectrum of the passband signal down to DC the sampling frequency is to be reduced from fs = 30.72 MHz to fs = 80 kHz. Determine the number of stages of the CIC filter in order to have an attenuation of the first spectrum replica of at least 40 dB. Consider that the signal useful bandwidth is $f_c = 20$ kHz. Sketch the signal flow diagram of the filter.



