TÉCNICO LISBOA

Sistemas Eletrónicos Integrados

Mestrado em Engenharia Eletrónica

OPERATIONAL AMPLIFIER

Project handout

João Caldinhas Vaz

Instituto Superior Técnico

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1. Objectives

The objective of this evaluation project is to design and simulate an operational amplifier (OPAMP) integrated circuit up to the layout phase. The technology to be used is the C35B4C3 CMOS from Austria Micro Systems manufacturer. The OPAMP circuit topology will be the one-stage symmetrical type. The differential stage circuit should be a PMOS differential pair biased by current source.

2. Technology available components

- MOSFET n and p channel 3.3V (nmos4 and pmos4 cells) from PRIMLIB library.
- Capacitors poly1-poly2 (cpoly cell) from PRIMLIB library.
- Resistances poly-1, poly-2 or poly-h (rpoly1, rpoly2 and rpolyh cells), from PRIMLIB library.
- PAD component (g_padonly cell) from IOLIB_ANA_4M library.

3. Specifications

Supply voltage: 3.0V.
Differential pair bias current: see table.
Minimum low frequency gain: see table.
Maximize output voltage swing.
Minimum input referred offset voltage.
Maximum total supply current 5mA.
Input common mode range containing 1.5V.
Output common mode voltage 1.5V.
Differential input; single-ended output.
Bias and signals accesses must have pads.

4. Work plan

1 - Use annex 1 to obtain a first guess for MOSFET dimensions for a given bias point. Build the OPAMP schematic using the available devices from foundry libraries.

2 - Following are the expected simulations to obtain from the final OPAMP schematic.

2.1 – Bias point simulation.

2.2 - Frequency response of the differential mode $A_d(f)$ and common $A_c(f)$ mode gains, and CMRR(f) (in decibel) also.

2.3 - Frequency response of the differential and common mode input impedance and output impedance (real and imaginary parts).

2.4 - Input referred offset voltage.

2.5 - Frequency response of the power supplies rejection ratios (in decibel).

2.6 - Input common mode voltage range and output voltage range.

2.7 - Phase margin.

2.8 - Output rise and fall slew-rate (in V/us).

2.9 - Total supply bias current and power consumption.

2.10 - Simulate $A_d(f)$ for process, voltage ($\pm$10%) and temperature dispersion (-40 º,125º).

3 - Design the OPAMP layout and simulate its behavior including C parasitics extracted from the layout. The final layout should be placed inside a pad frame. The separation between pads centers should be equal to 120um. Following are the expected simulations for this section.

3.1 - Frequency response of the differential mode $A_d(f)$ and common $A_c(f)$ mode gains, and CMRR(f), also. Include on the same charts question 2.2 related curves.

3.2 - Phase margin.

5. Report

The final report must contain all the trade-offs made during the design and the respective justifications and comments of the achieved results.

The final OPAMP schematic and all test-benches schematics used in simulations must be presented. All requested simulations results must be included. The frequency sweeps must always be made up to a frequency where important effects are visible.

The OPAMP final layout must be presented, showing its external dimensions and PADS signals or bias names. The charts with post-layout results must also include the schematic results for an easier comparison.

The complete report number of pages should not be larger than 25. All pictures should be readable, and colors should be used. Only layout pictures can have black background. Up to the limit date the report should be submitted in course webpage exclusively in pdf format (a single pdf file).

6. Table

The specifications for each group should be chosen from the following table. The differential pair supply current is I_{dp} and the OPAMP low frequency minimum gain is a_{0_min}. VNC display number for each group is also suggested.

Group	I_{dp} [mA]	a_{0_min} [dB]	Display number
1	0.9	36	1
2	0.8	36	2
3	0.7	36	3
4	0.9	38	4
5	0.8	38	5
6	0.7	38	6
7	0.9	37	7

Annex 1

3.3V NMOS and PMOS drain current in terms of $V_{GS(SG)}$ voltage. The graphs were obtained for W/L=10. Different current values can be obtained by linearly scaling W/L.