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# Digital Signal Processing Systems

## Multirate Signal Processing

1) A digital signal processing system operates with a sampling frequency $fs = 5$ kHz but it is required to reduce this frequency to $fs = 4$ kHz. Sketch the block diagram of the multirate signal processing system that implements this reduction. Specify each block and sketch the spectrum of the different signals. State if there is information loss and explain why.

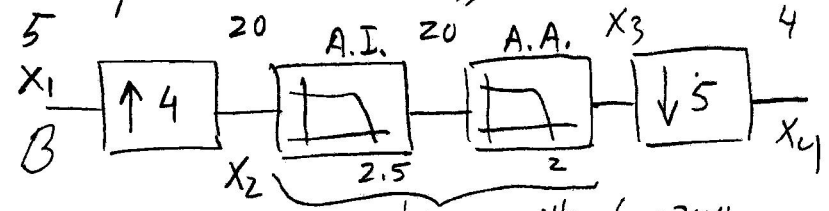
2) Consider that the interpolator anti-image filter is a FIR filter with $N = 12$ coefficients implemented using a polyphase structure. Sketch the signal flow diagram and determine the computational economy with respect to the direct form I implementation.

3) Consider using a CIC (*Cascade Integrator Comb*) filter in the decimator of a software radio system. After shifting the spectrum of the passband signal down to DC the sampling frequency is to be reduced from $fs = 30.72$ MHz to $fs = 80$ kHz. Determine the number of stages of the CIC filter in order to have an attenuation of the first spectrum replica of at least 40 dB. Consider that the signal useful bandwidth is $f_c = 20$ kHz. Sketch the signal flow diagram of the filter.

SPDS – Multirate problem

1) $f_s = 5kHz \rightarrow 4kHz$ (overall decimation)

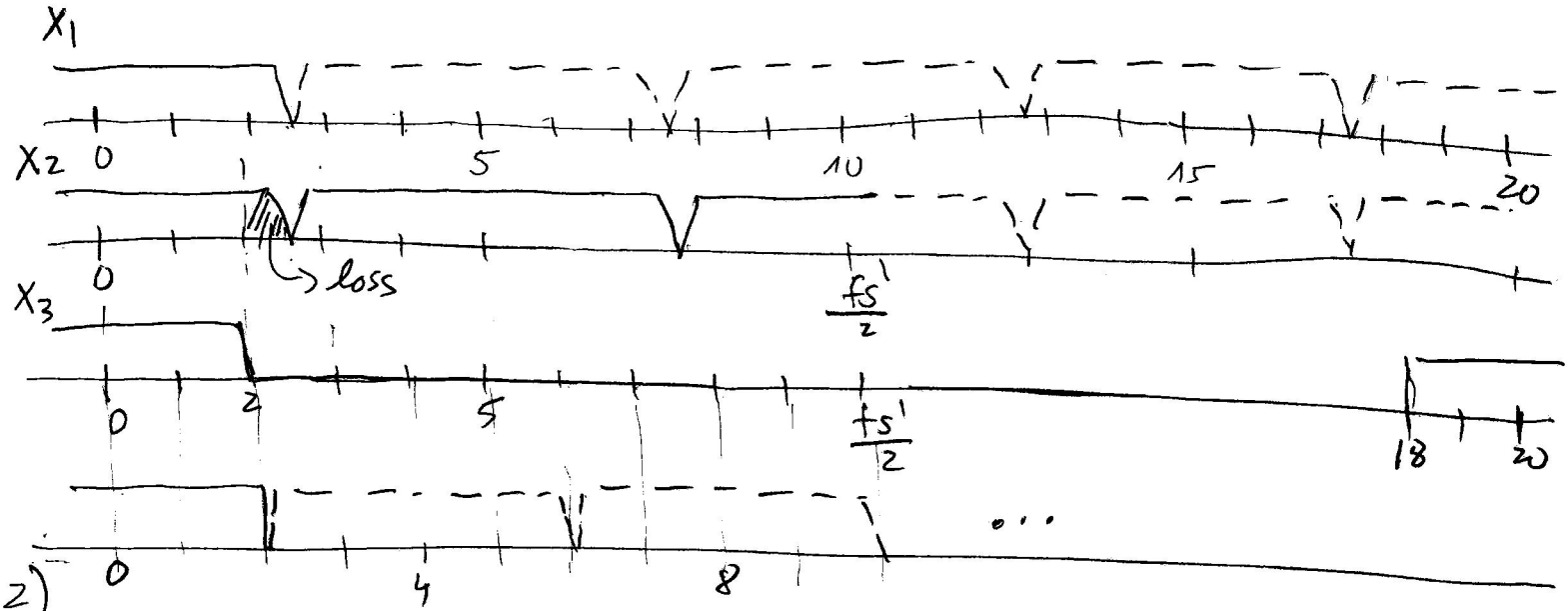
$\frac{L}{M} = \frac{4}{5}$ most simple fraction. In order to minimize loss of information interpolate first.




$B = 2.5kHz$

combine with $f_c = 2kHz$

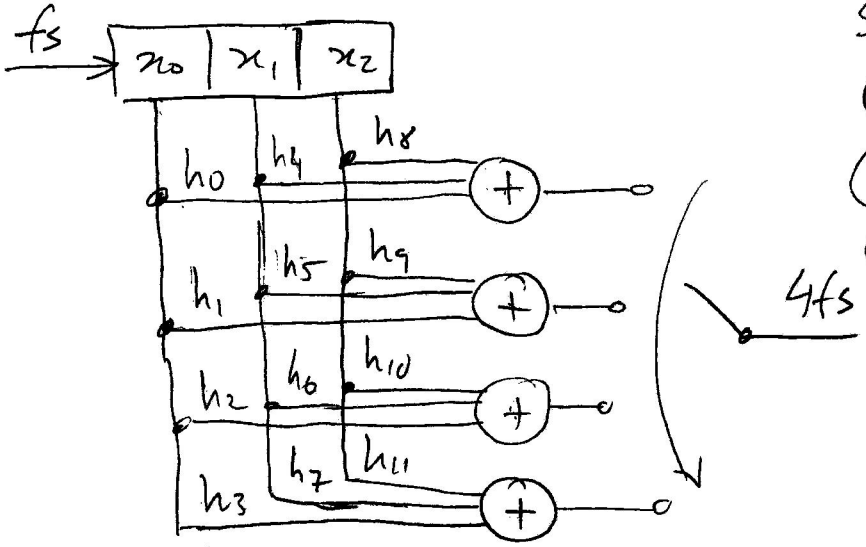
If the signal bandwidth B is less than 2kHz ⇒ no loss of information. But since $f_{s_{in}} = 5kHz$, B may be up to 2.5kHz




A.A. or (A.A + A.I) ≡ polyphase filter with N = 12 coefficients

Do not compute multiplications by zero-valued samples

| $x_0$ | 0 | 0 | 0 | $x_1$ | 0 | 0 | 0 | $x_2$ | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $h_0$ | $h_1$ | | | $h_4$ | | | | $h_8$ | | | $h_{11}$ |




Savings:

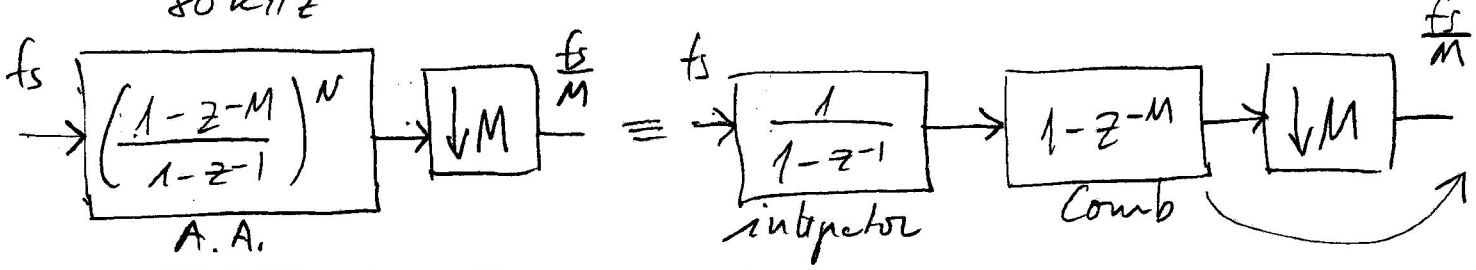
(X) $N \rightarrow \frac{N}{L}$

(+) $N \rightarrow \frac{N}{L}$

(M) $N \rightarrow \frac{N}{L}$

3) CIC decimator, N stages, $f_s = 30.72\ MHz$, $\frac{f_s}{M} = 80\ kHz$, $B = 20\ kHz$

$M = \frac{32.72\ MHz}{80\ kHz} = 384$ = decimation factor




$\equiv$ $\frac{1}{1-z^{-1}}$ → ↓M → $1-z^{-M}$ — M-1 less memory locations!

M = 3 (example)

$x_0, x_1, x_2, x_3, x_4, x_5, x_6, \ldots$ (after the integrator)

$x_0 - x_3, x_1 - x_4, x_2 - x_5, x_3 - x_6, \ldots$ $(1-z^{-3})$

$x_0 - x_3, x_3 - x_6, \ldots$ ↓3

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$x_0, x_1, x_2, x_3, x_4, x_5, x_6$ (after the integrator)

$x_0, x_3, x_6, \ldots$ ↓3

$x_0 - x_3, x_3 - x_6, \ldots$ $(1-z^{-1})$

Same

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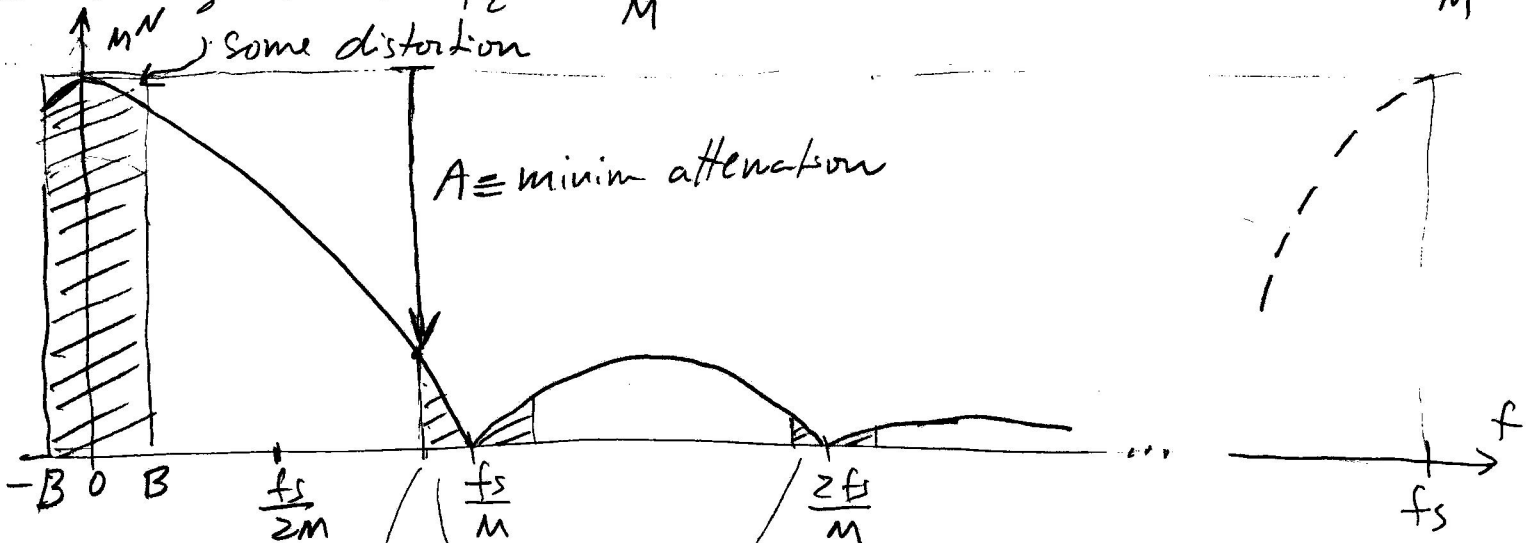
$$|H(jw)| = \left| \frac{1 - e^{jwMT_s}}{1 - e^{jwT_s}} \right|^N = \left| \frac{\sin \frac{MwT_s}{2}}{\sin \frac{wT_s}{2}} \right|^N$$

zeros:

$\frac{Mw_zT_s}{2} = k\pi$, $w_z = \frac{2\pi}{MT_s}k = k\frac{w_s}{M}$

Periodic zeros at $f_z = k\frac{f_s}{M}$




filter attenuates possible aliasing bands!

$f_1 = \frac{f_s}{M} - B$

$$\text{Attenuation} = \left| \frac{H(0)}{H(jw)|_{w=w_i}} \right| = \left| \frac{M}{\frac{\sin(MwT_s/2)}{\sin(wT_s/2)}} \right|^N = \left| \frac{M \sin\left(\frac{wT_s}{2}\right)}{\sin\left(\frac{MwT_s}{2}\right)} \right|^N = A$$

$w_i = 2\pi\left(\frac{f_s}{M} - B\right)$, $B = \frac{f_s}{4M}$ $(20kHz)$ $\quad \frac{f_s}{M} = 80kHz$

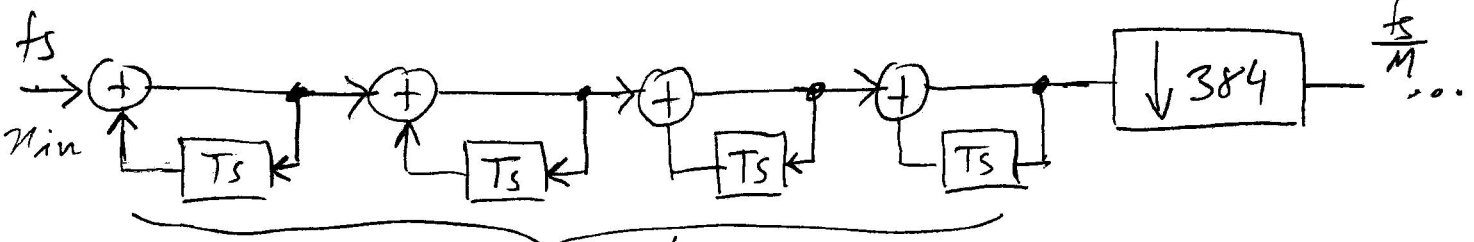
$= 2\pi\left(\frac{f_s}{M} - \frac{f_s}{4M}\right) = 2\pi\frac{3f_s}{4M} = \frac{3\pi f_s}{2M}$

$\frac{w_i T_s}{2} = \frac{3\pi f_s T_s}{4M} = \frac{3\pi}{4M}$

$$A = \left| \frac{M \sin\frac{3\pi}{4M}}{\sin\frac{3\pi}{4}} \right|^N = 3.3321^N$$

$A_{dB} = 20\log_{10} A = 20N\log_{10} 3.3321 \geq 40 \rightarrow N \geq 3.826$

So we need $\boxed{N=4}$ stages. The actual attenuation is 41.8 dB.





- Bit growth $\equiv \log_2 M^N = N \log M$

  #bits required = #bits of input + $N \log_2 M$

  $4\log_2 384 = 34.34$

  → 35 additional bits!

- Instead, use scaling algorithms which compute the dynamic range at every stage and the required number of bits.
- Linear phase, multiplier-less, no coefficient memory
- Not flexible, high DC gain, signal must be oversampled
- Need to use fixed-point, two's compliment.