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Sistemas de Processamento de Sinais (SPDSina)

Multirate signal processing

I - Consider a signal processing system operating with a sampling frequency and an input signal with bandwidth B. The sampling frequency is to be reduced to $f_s = 2$ kHz.

a) Sketch the block diagram of the signal processing circuit which realizes this operation with the less possible potential loss of information indicating the sampling frequencies, the filter's cutoff frequency and quality factor along the chain. State in which conditions loss of information does not occur. Justify.

b) Represent the signal's spectrum along the chain considering $B = 4$ kHz.

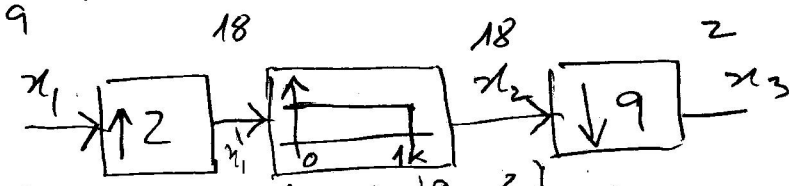
c) Sketch the block diagram of the previous decimator which uses two identical decimation stages indicating the sampling frequencies, the filter's cutoff frequency and quality factor along the chain. Compute the approximate computational economy of this solution.

d) Consider that the interpolator anti-image filter is a FIR filter with $N = 10$ coefficients. Sketch the block diagram of the polyphase implementation of the interpolator. Explain its advantages and state the economy achieved.

II - Suppose you have a signal with a bandwidth B and an A/D converter with 8 bits but you need a SNR of about 60 dB and a sampling frequency $f_s = 2B$ (minimum). Sketch the signal processing system that can achieve this SNR increase using multirate signal processing techniques.

$f_s = 9KHz \rightarrow 2KHz$ (I)

Interpolate first $\rightarrow \frac{L}{M} = \frac{2}{9}$

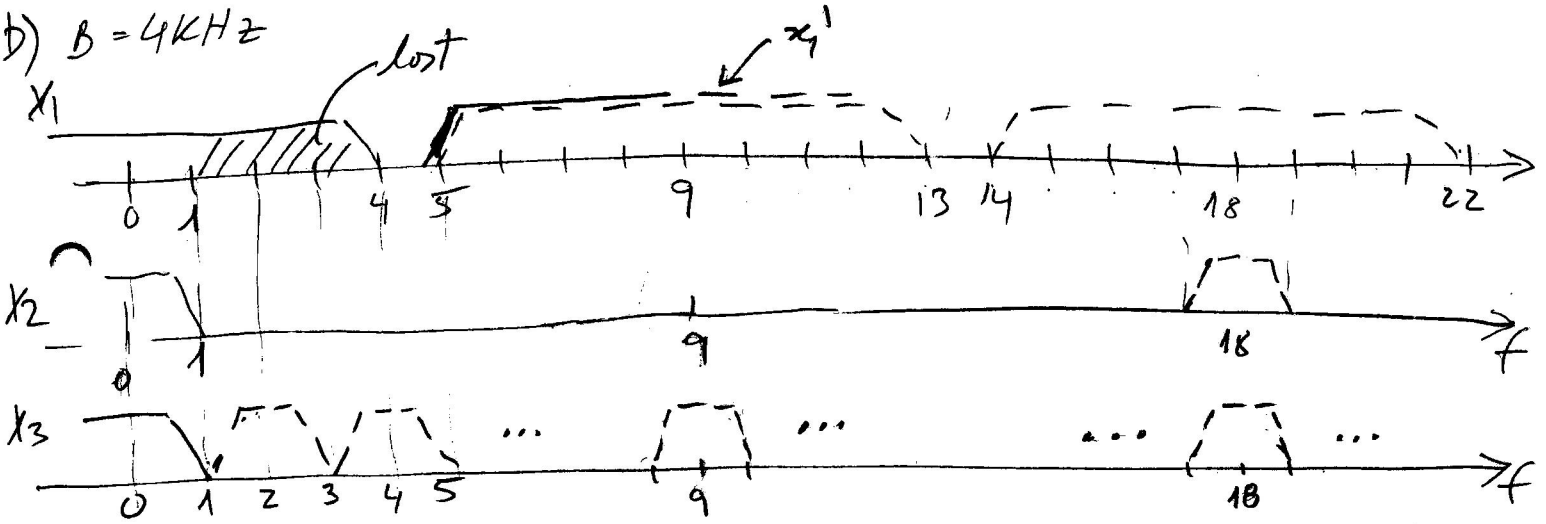


a) $f_c = \min\{\frac{9}{2}, \frac{2}{2}\} = 1K$

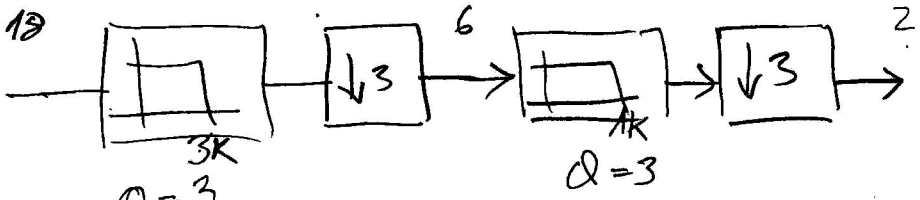
$Q \simeq \frac{18}{2} \simeq 9$

No loss of information if $B < 1KHz$ and interpolation is done first. If decimation is done first, $B < 0.5KHz$.

b) $B = 4KHz$

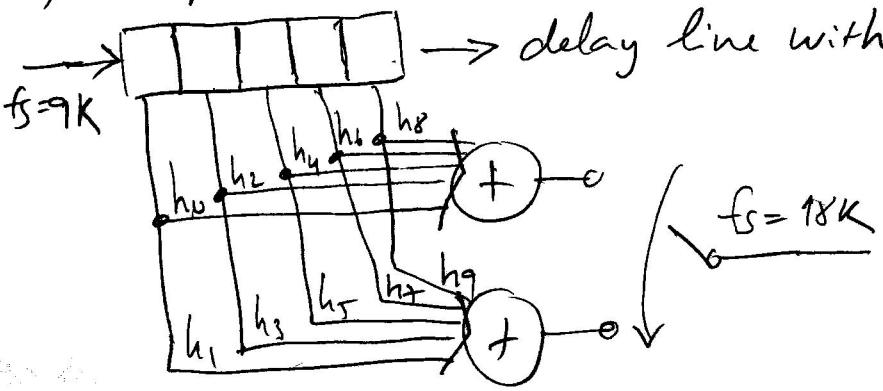


c) Two identical decimation stages $M_1 \rightarrow M_1^2 = M = 9 \rightarrow M_1 = 3$



One stage $C \simeq M = 9$, two stages, $C \simeq 2 \times 3 = 6$ (33% economy)

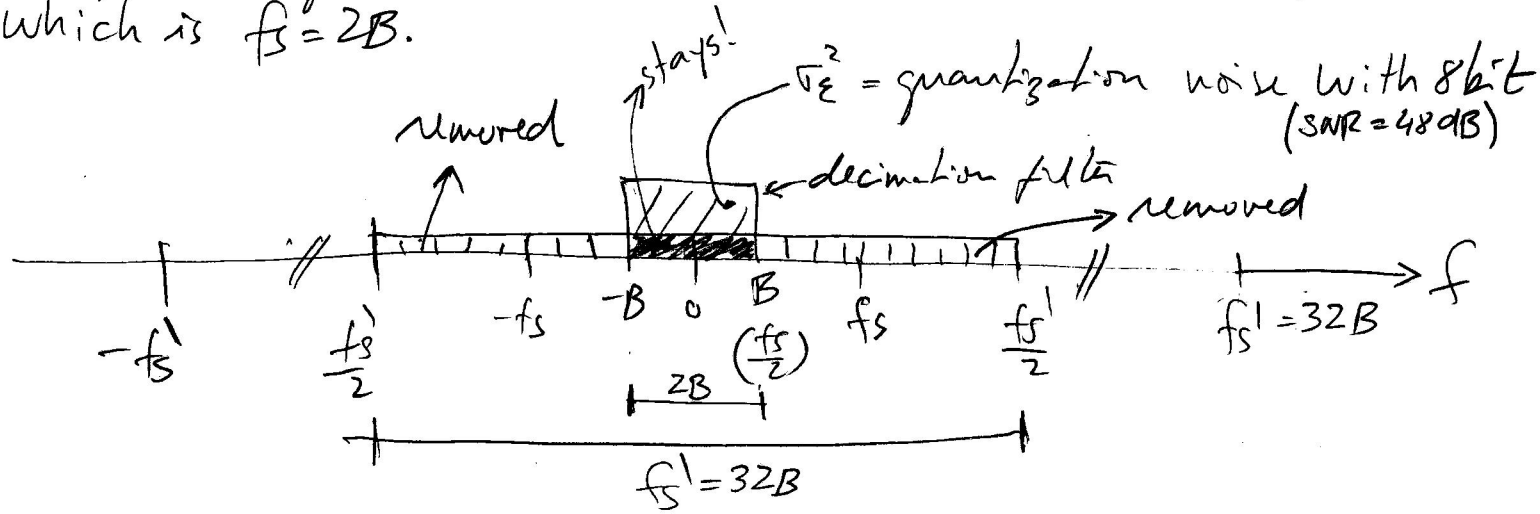
d) Interpolator is a polyphase filter with $N = 10$ ($L = 2$)



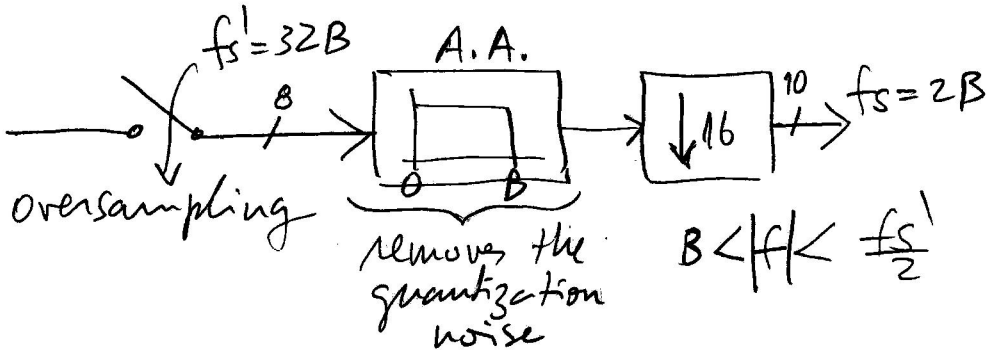
Economy (M), (+), (×) $\equiv N \rightarrow \frac{N}{L}$ (50%)

(II)

Bandwidth B, A/D = 8 bits (48 dB), need SNR = 60 dB ≈ 10 bit, so need two additional bits. This means that the actual sampling frequency must be 4×4 = 16 times the minimum f_s which is $f_s = 2B$.



new $\sigma_\varepsilon^2 \rightarrow \frac{\sigma_\varepsilon^2}{16} \rightarrow 10\log_{10}16 = 10\log_{10}2^4 = 40 \times 0.3 = 12\,dB$



the A.A. filter must use digital words with more than 10 bit for the accumulation processes. Usually about 4 guard bits are used (10+4 = 14 bit).