TÉCNICO LISBOA

Sistemas Eletrónicos Integrados

(MEE)

PULSE GENERATOR

Project handout

João Caldinhas Vaz

Instituto Superior Técnico

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1. Objectives

This project objective of this project is to design a digital integrated circuit to generate a pulse waveform. The technology in use will be CMOS 130nm available from United Microelectronics Corporation (UMC). The final result will be the pulse generator layout ready for fabrication.

2. Specifications

2.1. General

Bias voltage: 0V and 1.2V.
HDL language: Verilog.
All signals are active in high-level (H), and inactive in low-level (L).
The clock-signal (CLK) active edge is the rising one.
Faraday Technology Corporation provides the technology libraries (HS standard cells).

2.2. Pulse generator inputs / outputs

Inputs: INIT, PER and CLK. Inputs INIT and PER must be read in the CLK active edge.
Outputs: PULSE. It should be updated in the CLK active edge.

2.3. Pulse generator behavior

For the pulse generator to start (or restart) INIT must make a transition from L to H. During this transition two things can happen:
a) If PER is L one single pulse waveform is generated at the output. This waveform starts with L level during T_I, H level during T_W and back to L level during T_E.
b) If PER is H a periodic signal with period equal to single pulse waveform (including T_I, T_W and T_F) is continuous repeated.

3. Project

The workflow can be divided into three stages:

1) A functional description should be implemented in Verilog RTL code for both the pulse generator module and the testbench module. The code should be simulated.

2) The pulse generator module code should be compiled with technology libraries to produce a Verilog gate-level code with technology standard cells. The gate-level code should be simulated.

3) Finally, the gate-level code should be used to produce a physical layout of the pulse generator circuit. The final gate-level code obtained from place and route should be simulated.

4. General considerations

All time simulations should be made showing the pulse generator inputs and output signals, and module important internal signals. Simulations should present single to periodic and periodic to single pulse situations.

The report should present the important simulated waveforms. The gate-level and the place and route schematics must be presented, and final layout also. The Verilog RTL code should be annexed to the report. Important reports should be presented for synthesis and place and route final phases.

4.1. Table

The specifications for each group should be chosen according to the following table.

Group	T_I [us]	T_W [us]	T_F [us]
1	1.0	0.5	2.5
2	1.5	0.4	2.0
3	2.0	0.3	1.5
4	2.5	0.2	1.0
5	2.0	0.3	1.5
6	1.5	0.4	2.0
7	1.0	0.5	2.5