

**Micro and Nanofabrication Techniques (TMN)**

**Design project** - Step 2

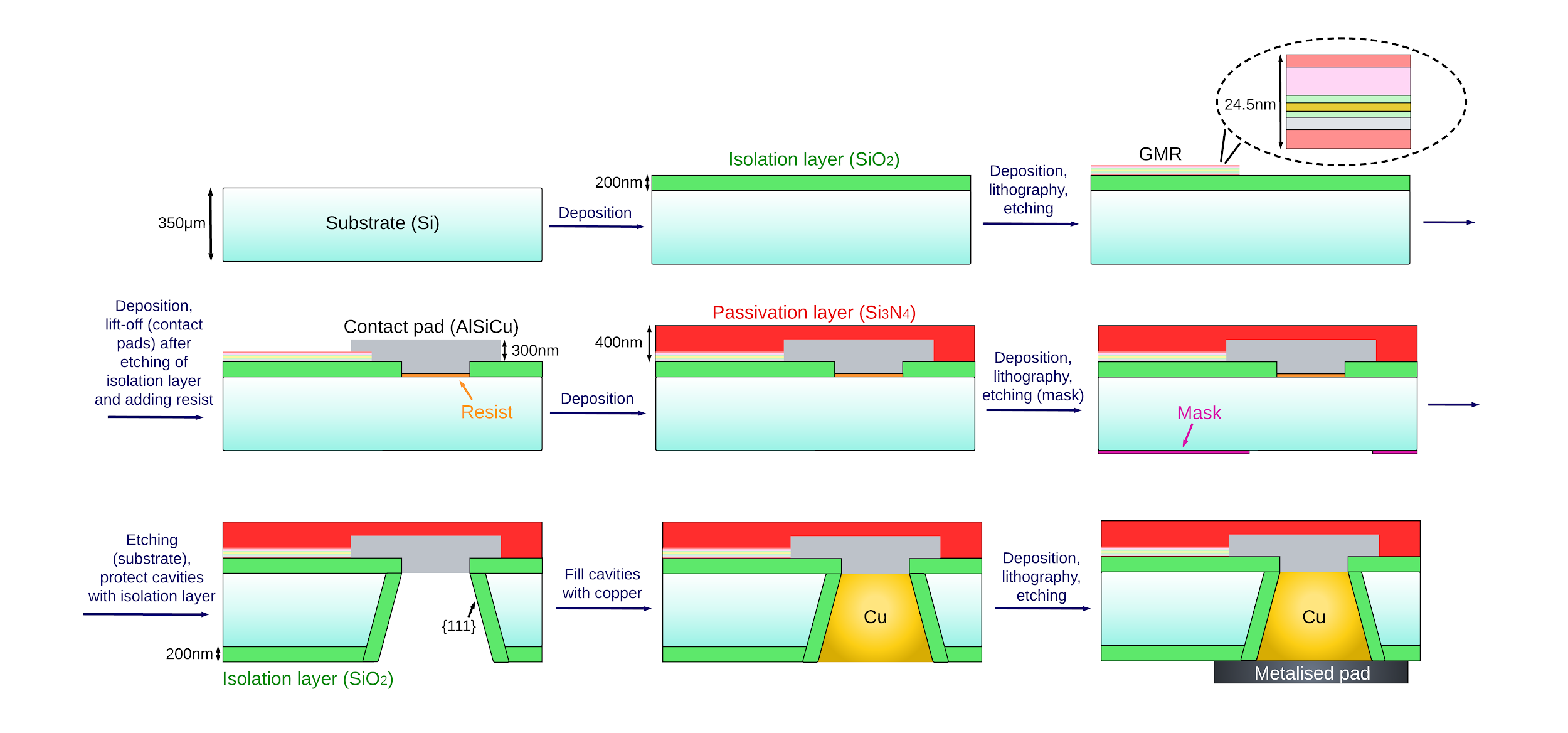
Duarte Miguel de Aguiar Pinto e Morais Marques | 96523

João Carlos Ribeiro Chaves | 96540

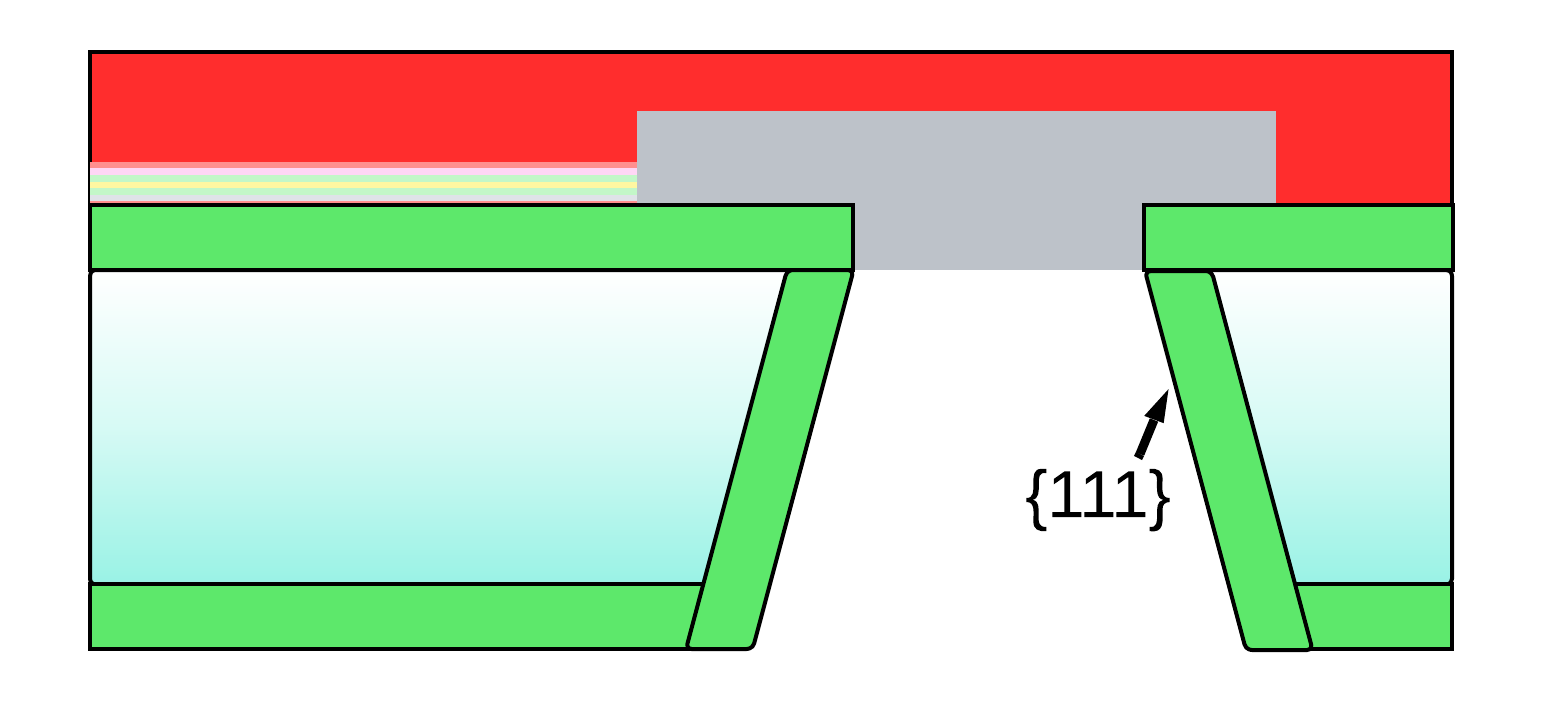
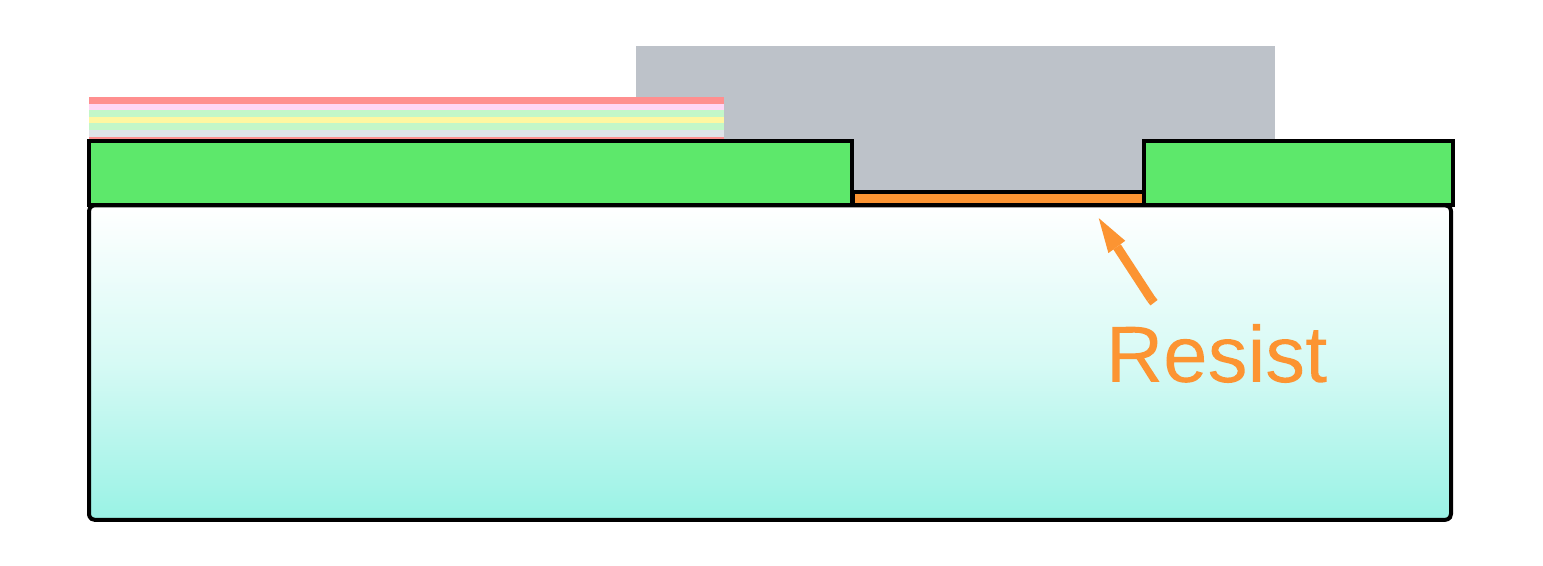
Prof. Susana Cardoso de Freitas

March 24th 2023

In the previous presentation (Step #1), we presented the global vision of the nanostructure shown below. In the next three steps (#2, #3 and #4), the following aspects will be covered: materials, dimensions, processes, specific methods, control and inspection points. For that purpose, **each line in the cross section global vision** will be analyzed in separate presentations - therefore, for now, only the isolation layer and the GMR stack (both in the frontside) will be addressed.

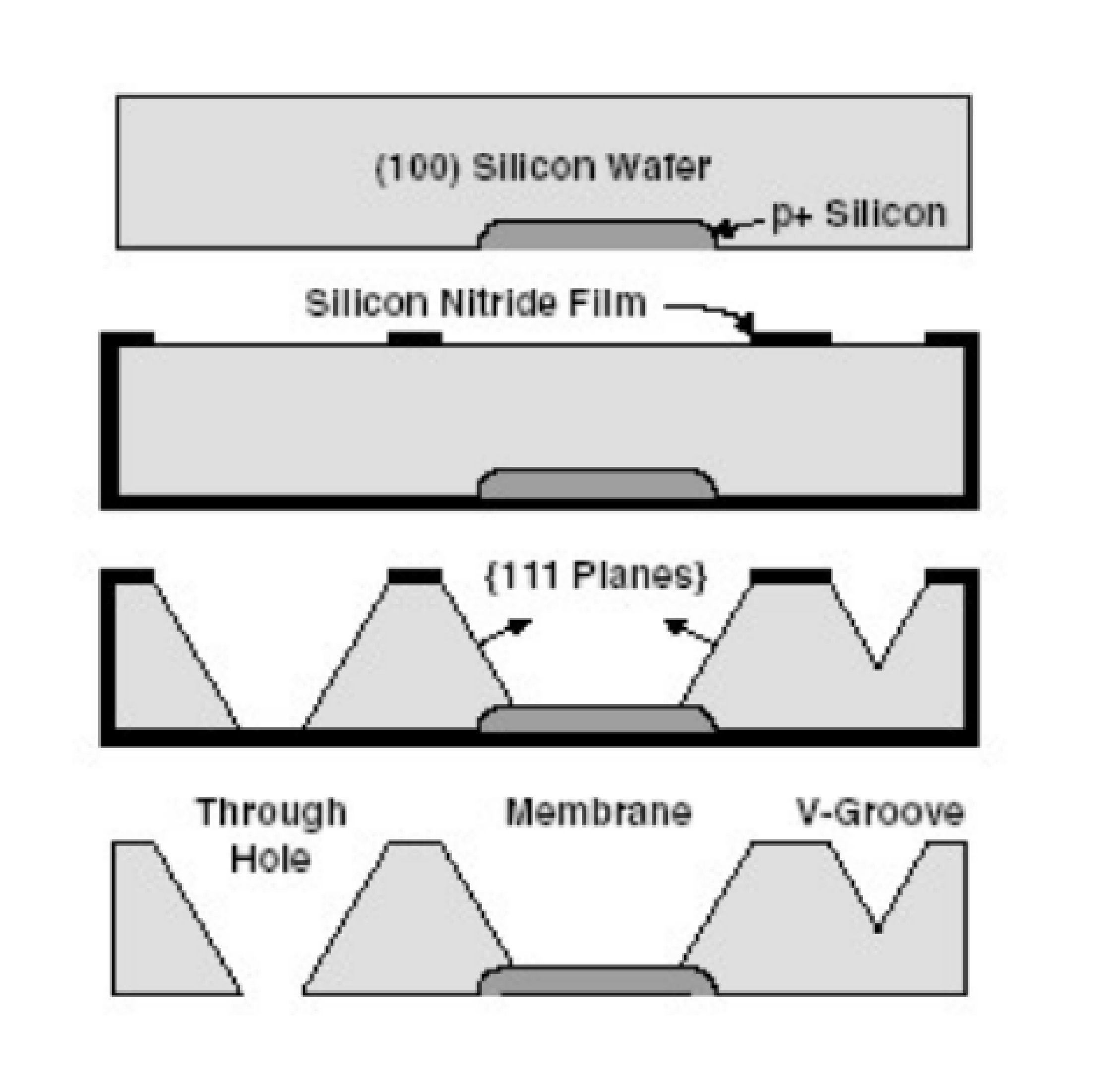
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**Some details in the process steps with questions for the professor:**

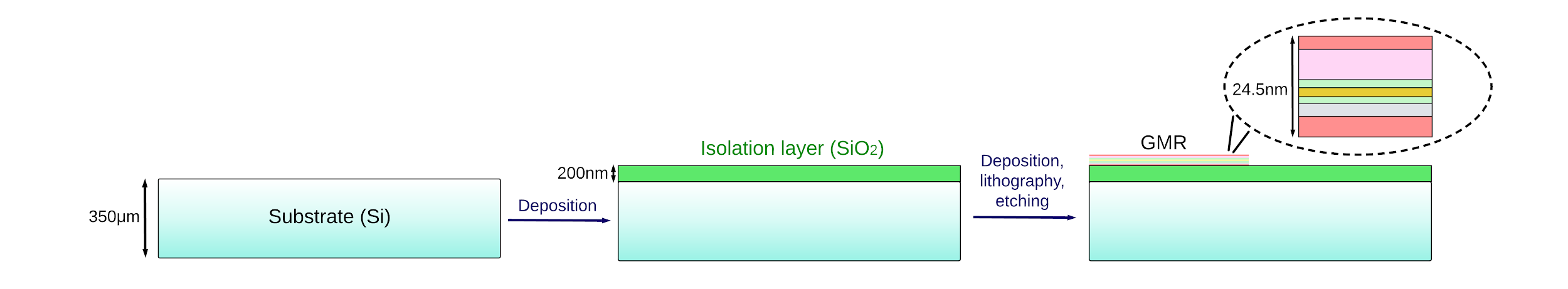
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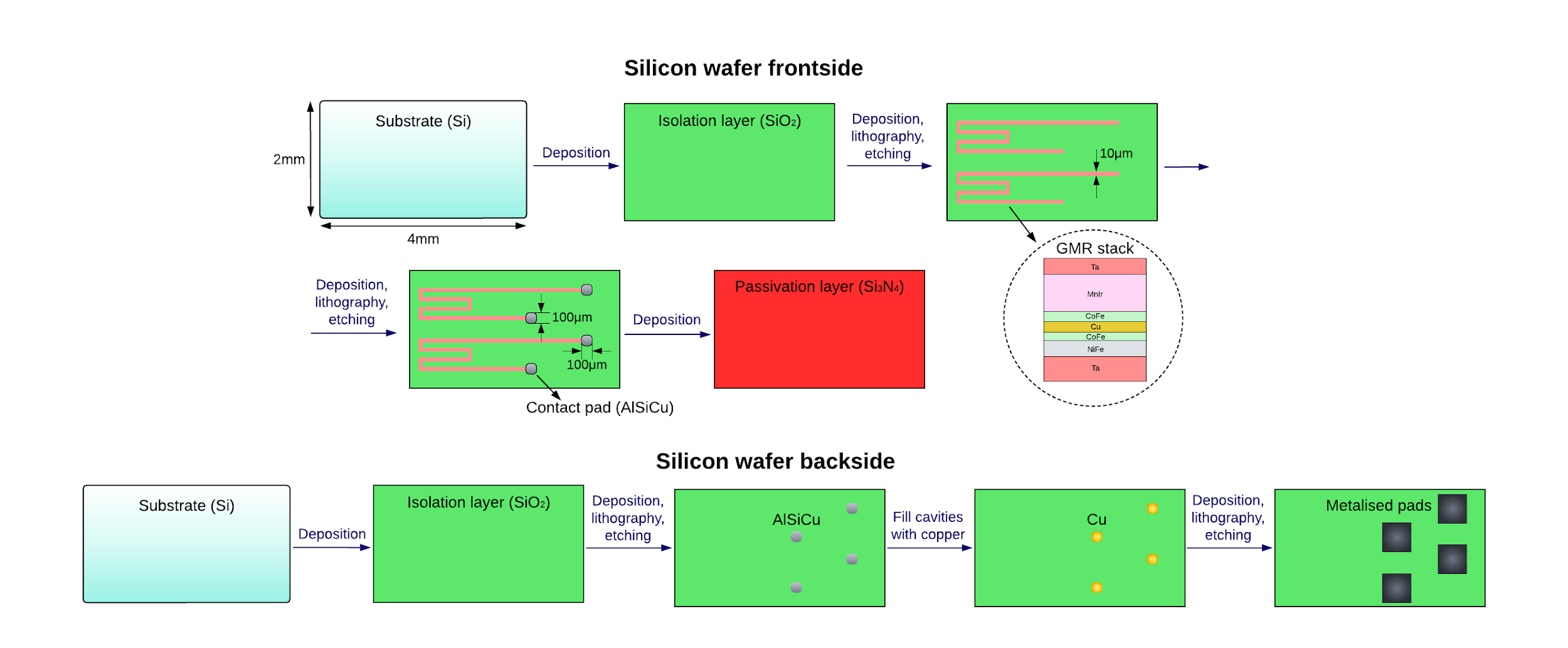
We place this resist here, not to serve as a mask for the silicon wet etching (for that purpose, we only have the mask drawn in pink, in the backside), but to be able to do **lift-off** of the isolating layer (SiO2) that we deposit in the backside + inside the cavity. This lift-off leads to the removal of the SiO2 in contact with AlSiCu and is necessary in order not to cover the metalised pad with isolating layer (so that it then enters in contact with copper).

* Our question is the following: do you think this could work? Could we do lift-off to remove part of the SiO2 (the part that is in contact with the bottom of the AlSiCu contact)?
* Another question we have is: do we need to protect the “side walls” of the Si substrate, as shown in the image below? This seems to make sense, since the wet etching performed with Si would “penetrate” the substrate through these lateral walls… However, we are not sure it is necessary, since each sensor chip will be one in dozens within a wafer (thus, the side walls could be protected already)...

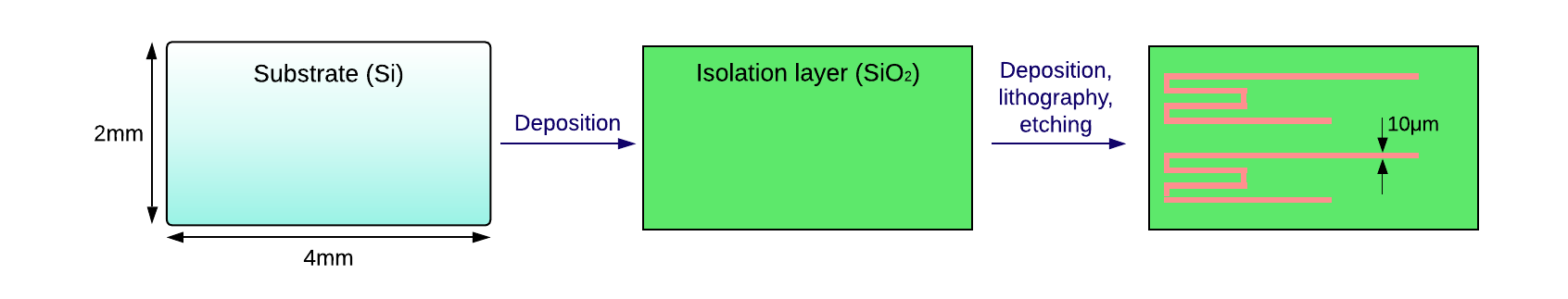


In Step #2, only the following will be addressed:

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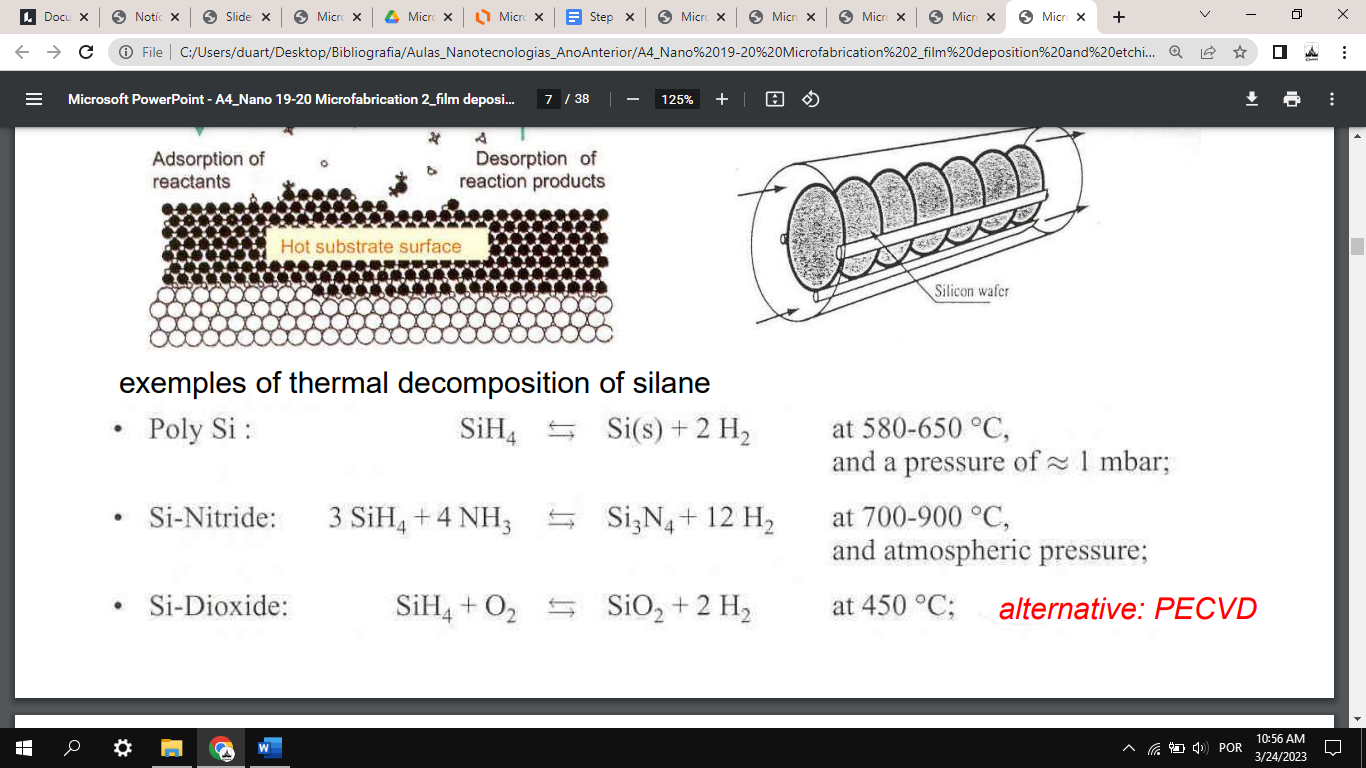
In terms of the top view:****

In Step #2:

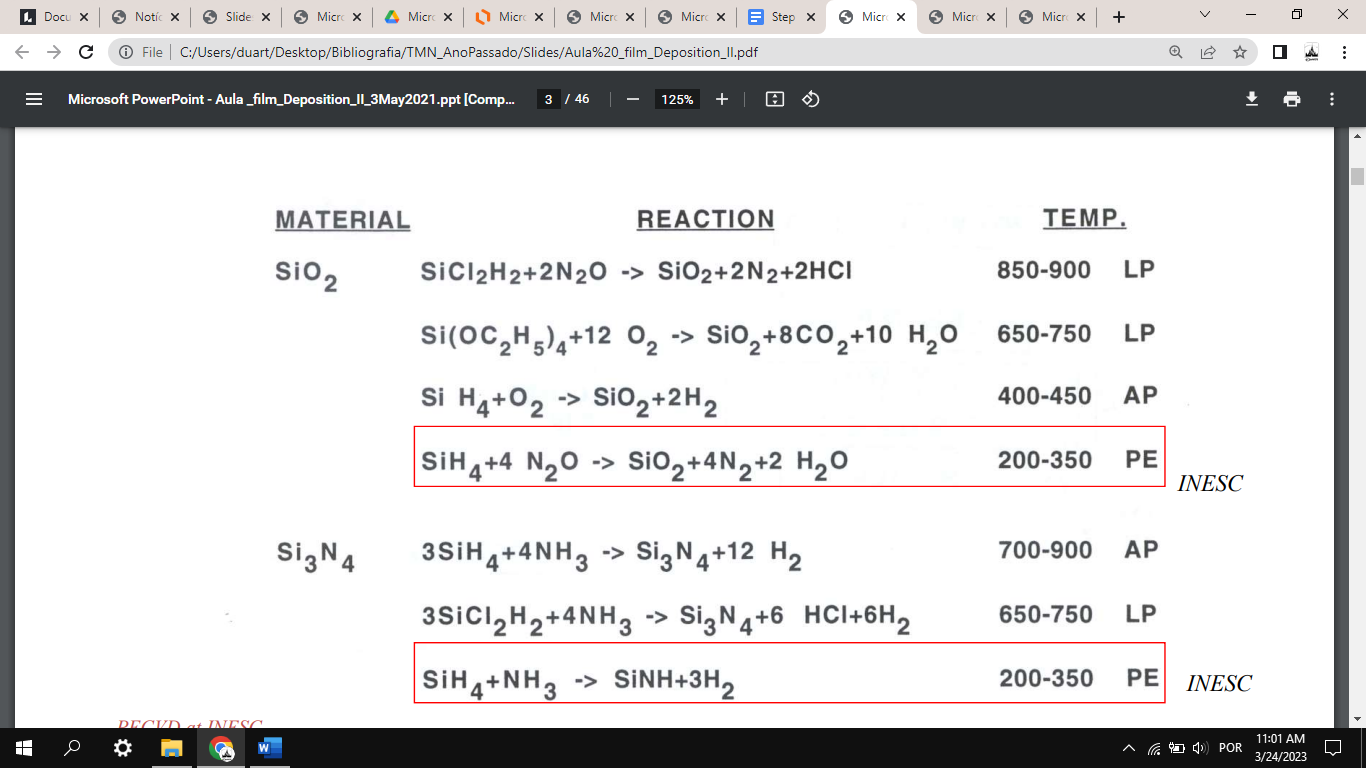
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**Deposition of SiO2**

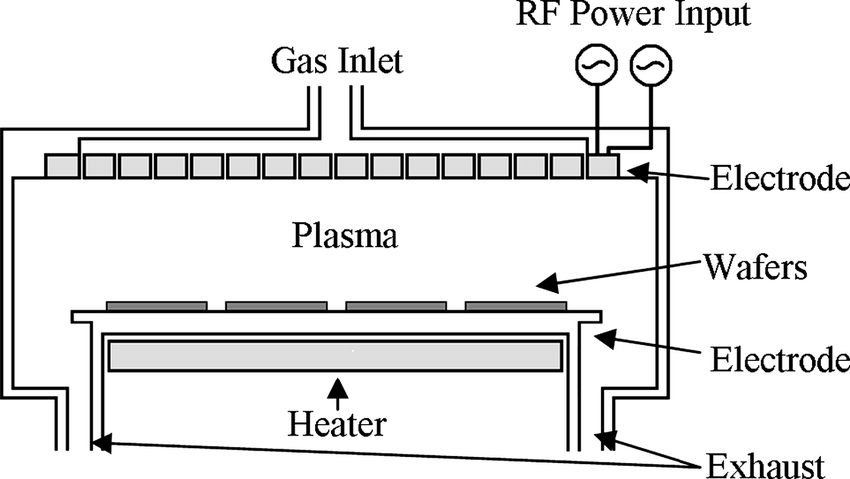
Typically, PVD is used for metals, while CVD for semiconductors and insulators. Therefore, a CVD (Chemical Vapor Deposition) method will be used here. For Si-Dioxide, the thermal decomposition of silane is given by the following equation:



Some typical characteristics of CVD include a moderate deposition rate (up to 2500 Å/min), the scalability to large wafer sizes and a low energy of deposited species. The former can be enhanced with plasma-aid. With this thinking, **PECVD (Plasma Enhanced CVD)** can be used, according to the following reaction [N2O should be replaced with NO2]:



Which occurs at a temperature of around 200-350ºC. The typical film thickness goes from 1000Å to 1 mm, thus the 200 nm thickness of our SiO2 layer is compatible with this deposition method. Typical PECVD system:



PECVD differs from LPCVD and APCVD in that it typically involves lower substrate temperatures; however, film quality can be poorer, with more defects such as pinholes and residual strain. Growth rates are usually around 60 nm/min (thus, it would take about 3min20s to deposit the 200 nm thick insulation layer).

**Control and inspection points:** visual inspection

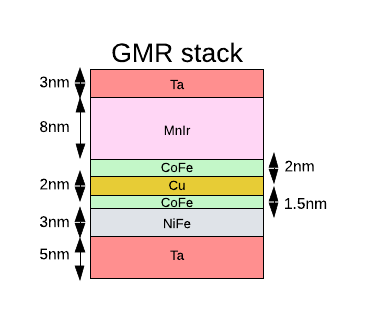
**Deposition of GMR stack**

A Physical Vapor Deposition method could be used - for example, **magnetron sputtering**. Here, the mechanism of production of depositing species is momentum transfer; the deposition rate is usually lower, except for pure metals; it is scalable up to large wafer sizes.

In a sputtering system, a plasma is struck in an inert gas such as Ar, using either DC or RF high-voltage electric fields. Ions from the plasma strike the source material to be deposited and then transported to the substrate; deposition rates of a few tens of nm/sec are possible. The sputter guns (for instance, planar magnetron or circular magnetron) can include the magnets to confine the motion of the electrons used to ionize the sputter gas.

Issues to consider: film structural quality, uniformity, conformality, deposition rate, mechanical stress, impact of deposition method on underlayers and substrate

**Control and inspection points:** (visual inspection or) **film thickness monitoring -** thickness of the deposited material can be monitored using a quartz crystal microbalance. These rely on measuring the mechanical resonance frequency of a single crystal of quartz, which moves to lower frequencies as the mass of the evaporant deposited on the crystal surface increases.



**Photoresist deposition**

To create a pattern in a thin film, specific regions on the wafer surface are protected by a mask and the material not covered by the mask is removed. Masking in ion milling can be achieved by using a material that etches more slowly than the substrate.

A **positive photoresist** will be deposited onto the chip with spin coating.

**Control and inspection points:** visual inspection

**Photoresist lithography and removal**

In order to imprint the desired pattern into our mask, the proper exposure and development need to be done.

Since the GMR stack has a width of 10 μm (as indicated in the top view), methods with lower resolution - such as e-beam lithography, X-ray lithography or ion-beam lithography - are not required. Instead, **optical lithography** (with a resolution of usually about 0.5-1 μm) will allow for a much higher throughput. Using this method, the mask can be reused in later occasions for similar processes. In order to avoid contact between the mask and the sample, proximity or projection lithography can be used (instead of contact lithography). Since the minimum feature size of proximity lithography is about 2 μm, perhaps it is not justifiable to use the more complex (but with better resolution) projection lithography method.

Once the photoresist has been patterned, the exposed area is removed with the developer.

**Control and inspection points:** visual inspection, analysis under optical microscope (to visualize 10 μm features)

**Etching of GMR stack**

This can be done with **ion milling** (that is, ion beam etching with Ar-ion, Ar+); Ar is a non-reactive species. We want to deposit some magnetic materials, so a reactive chemical process is not recommended. Since this is a physical etching process, it should be anisotropic and not selective, thus allowing to etch the entire stack at once.

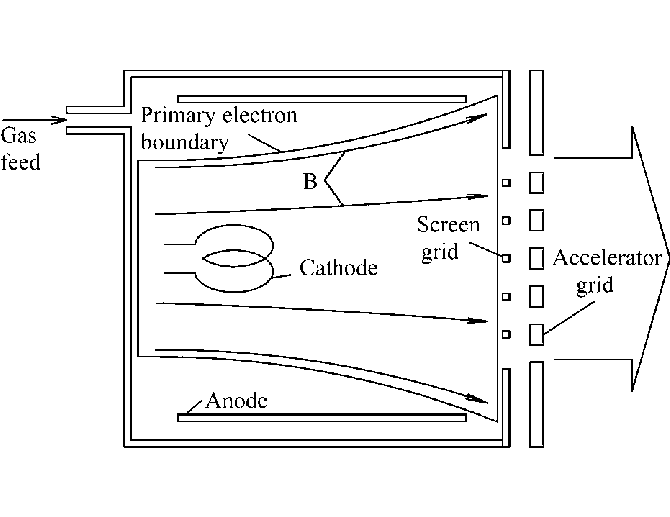
Plasma is formed in a separate ion source and ions are accelerated onto the wafer, which is held at low pressure in another chamber. Due to momentum transfer, surface atoms are knocked off. The etching products are not volatile and the process is not very selective. It is strongly directional - good for the shape of the GMR stack seen in the top view.

Since we are looking for an angle of 90º with the substrate, an angle of 70º should be used for the Ar+ beam incidence.

Ion milling yields, and therefore the etch rate, vary with the substrate material.

Potential challenges: increasing wafer size and decreasing device size make uniform feature size control over the whole wafer surface and from run to run challenging; trenches; poor selectivity can etch some SiO2.

**Control and inspection points:** mass spectroscopy (monitor the chamber atmosphere composition during the etching); higher quantities will be detected in the following order - Ta, MnIr, CoFe, Cu, CoFe, NiFe, Ta.



Kaufman ion source, used for ion beam etching

**Removal of remaining photoresist**

Photoresist strip

**Control and inspection points:** visual inspection

**Additional questions for the professor:**

* Should all the layers in the GMR stack be deposited with magnetron sputtering?
* What method should we use to remove the remaining photoresist in the end?

**Additional things that will be added in future presentation or in the report:**

* References, bibliography;
* Include drawings in scale;
* Calculations to determine necessary thickness of photoresist in order to etch entire GMR stack with ion milling; calculations regarding etch rates for different layers of GMR stack.