TÉCNICO LISBOA

Circuits Theory and Electronic Fundamentals

Integrated Master in Engineering Physics, IST, University of Lisbon

Lab 4: Audio Amplifier

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1 Introduction

The main objective of this laboratory assignment is to simulate an audio amplifier circuit with Ngspice and to compare the results with a theoretical model used to study this circuit. The architectures of the Gain and Output Stages have been chosen as shown in Figure 1, in which designations have been assigned to each node and the circuit's components. The input corresponds to an AC signal of amplitude 10 mV. On the other hand, the output, measured in the *out* node shown below, must be a sine wave with no visible distortion. It is connected to an 8 Ω audio speaker.

The Gain Stage contains the capacitors C_i and C_b and the resistances R_1, R_2, R_c and R_e, as well as a bipolar NPN transistor. The resistances R_{out} and R_L, the capacitor C_o and the bipolar PNP transistor belong to the Output Stage. In order to simulate this circuit in Ngspice, the Philips BC547A BJT model was used for the NPN transistor and the Philips BC557A BJT model was used for the PNP transistor. By studying this circuit, the gain and impedances for both stages have been computed and the frequency response has been plotted in Sections 2 and 3. The values of the circuit's components were selected in order to obtain the desired results and, at the same time, keep the monetary cost as low as possible, in order to keep the merit M (computed in Section 3) as high as possible.

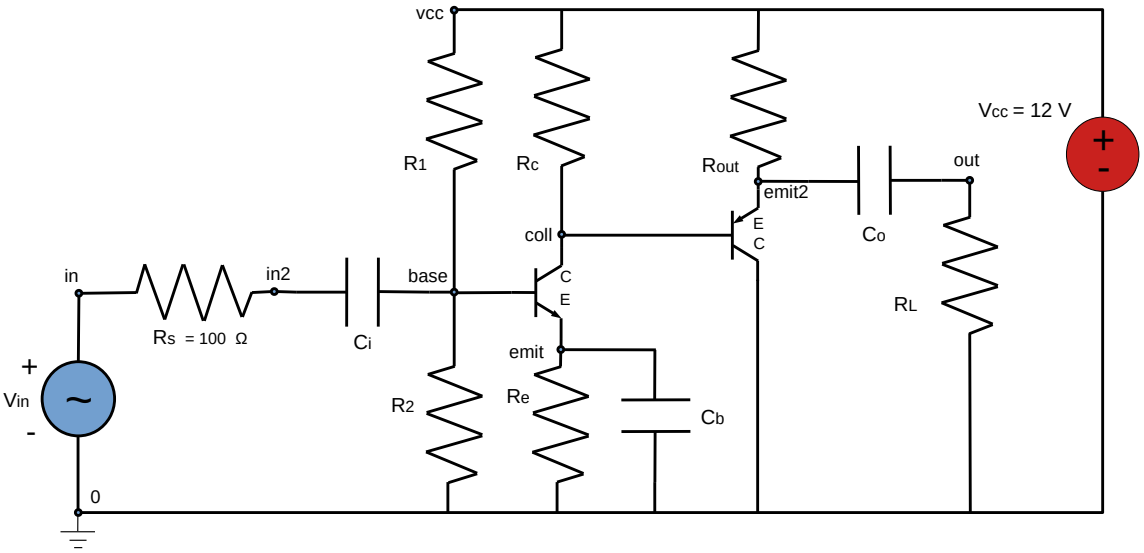


Figure 1: Circuit to be analysed in this laboratory assignment.

2 Theoretical Analysis

The values used for the circuit's resistances and capacitances were determined while doing the Simulation Analysis, in order to get the best possible results, whilst mantaining the monetary cost as low as possible and the merit as high as possible. Using these values, which will be further discussed in Section 3, the theoretical model is applied in this Section, in order to verify its validity and the disparities with the results obtained from Ngspice. The resistances and capacitances used were the following:

Name	Value
R_1	70 kΩ
R_2	10 kΩ
R_C	1 kΩ
R_E	100 Ω
R_{out}	50 Ω
C_i	1.0 mF
C_b	1.6 mF
C_o	1.2 mF

Table 1: Values used for resistances and capacitances in the circuit.

As it was learnt in class, the Gain Stage can be simplified into the circuit shown below, by using the Thévenin's equivalent of the bias circuit.

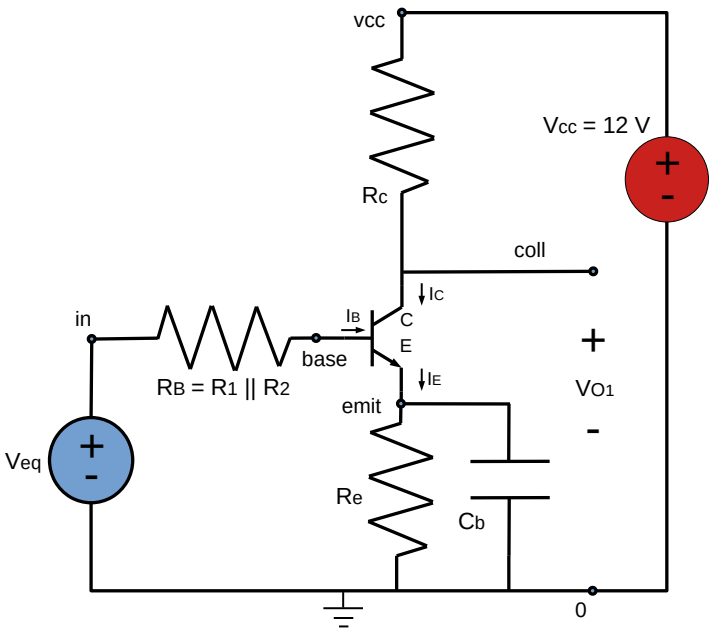


Figure 2: Gain Stage circuit.

While doing an Operating Point Analysis of the circuit shown in Figure 2, the capacitor becomes an open-circuit, thus only the resistor R_e is connected to nodes *emit* and *0*. As shown above, the equivalent resistance is given by $R_B = \frac{R_1 R_2}{R_1+R_2}$. Moreover, the equivalent voltage is given by $V_{eq} = \frac{R_2}{R_1+R_2} V_{CC}$. The current I_E that goes out of the transistor's emitter is given by

$$I_E = (1 + \beta_F) I_B \tag{1}$$

Where $\beta_F = 178.7$ for the NPN transistor model used in Ngspice and I_B is the current entering the transistor's base. Moreover, it is considered that $V_{ON} \approx 0.7$ V is the voltage for the diode model, being $V_{BE_{ON}} = V_{ON}$ for the base-emitter junction. By applying KVL, the following equation can be easily obtained: $I_B = \frac{V_{eq} - V_{ON}}{R_B + (1+\beta_F) R_E}$. Moreover, we have that $I_C = \beta_F I_B$, $V_{O_1} = V_{CC} - R_C I_C$ and $V_E = R_E I_E$. Finally, having calculated these quantities, in order to make that the theoretical model considered in this laboratory assingment is valid for the chosen values for the circuit's components, it is necessary to make sure that the following relation is satisfied:

$$V_{CE} = V_{O_1} - V_E > V_{BE_{ON}} \tag{2}$$

That is, it is necessary to make sure the transistor is working in a Forward Active Region. This relation is confirmed by the values shown in Table 2.

Name	**Value [V]**
V_{CE}	6.1117
$V_{BE_{ON}}$	0.7

Table 2: Voltages obtained in the Gain Stage.

Let us now consider the incremental analysis. The Gain Stage is, therefore, represented by the incremental circuit that learnt in class. This analysis is considered for medium frequencies, thefore the capacitor C_b can be replaced by a short-circuit. Thus, the gain in the Gain Stage is given by:

$$AV_1 = (R_B||R_S)R_C \frac{R_E - g_m r_\pi r_o}{(r_o + R_C + R_E)(R_B||R_S + r_\pi + R_E) + g_m R_E r_o r_\pi - R_E^2} \tag{3}$$

Where $g_m = \frac{I_c}{V_T}$, $r_\pi = \frac{\beta_F}{g_m}$ and $r_o \approx \frac{V_A}{I_c}$. The thermal voltage considered was $V_T = \frac{kT}{q}$ with $T = 300.15$K, $k = 1.38064852 \times 10^{-23}\ m^2 kgs^{-2}$ and $q = 1.60217662 \times 10^{-19}$. Moreover, the Early Voltage used in the NPN Ngspice model is $V_A = 69.7$ V.

This same equation can be simplified by considering $r_o = \infty$, from which $AV_1(r_o = \infty) = (R_B||R_S)R_C \frac{-g_m r_\pi}{R_B||R_S + r_\pi + R_E + g_m R_E r_\pi}$ is obtained. However, during the course of this assignment, it was verified that this approximation showed to produce worse reults, thus it wasn't considered. On ther other hand, it was considering a fairly reasonable approximation to have $R_E = 0$ in equation 3. The final results, shown in Figure 4 were, in fact, obtained by considering the average value of AV_1, obtained from equation 3 with R_E given in Table 1, and AV_1 with $R_E = 0$, because the results with the average value were much more similar to those obtained in Ngspice, rather than using only one of the two. This will be further discussed in Section 3.

Finally, the input and output impedances for the Gain Stage are given respectively by:

$$Z_{I1} = R_1||R_2||r_\pi = R_B||r_\pi = \frac{R_B r_\pi}{R_B + r_\pi} \tag{4}$$

$$Z_{O1} = R_C||r_o = \frac{R_C r_o}{R_c + r_o} \tag{5}$$

The impedances obtained are shown in Table 5 and will be discussed further beyond.

Now, let us consider the Output Stage circuit, which is shown below.

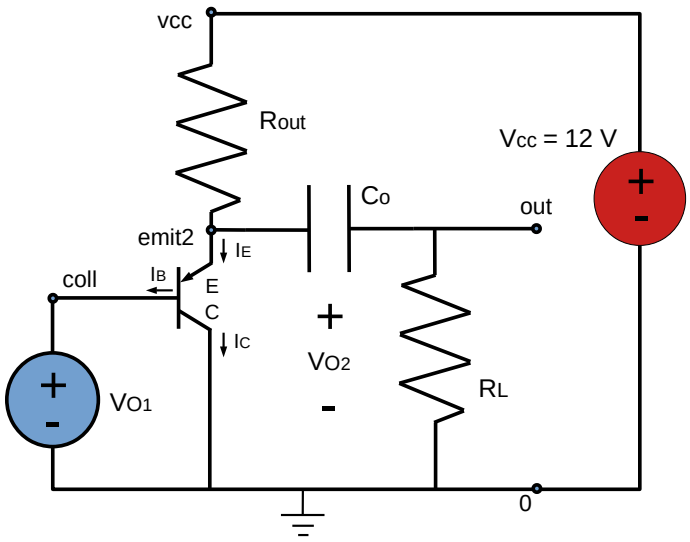


Figure 3: Output Stage circuit.

For the Operating Point analysis, however, the capacitor is considered an open-circuit. In the incremental analysis, by considering only medium frequencies, the capacitor can also be disregarded in the model. For these reasons, the output voltage V_{o_2} was drawn as the voltage drop between nodes *emit2* and *0*; however, in the Ngspice simulation, the output voltage will of course be considered in node *out*.

In the Output Stage, a PNP transistor is used. In this case, $\beta_F = 227.3$ and the Early Voltage $V_A = 37.2$ are the values used in Ngspice and therefore in the Octave script as well. Moreover, we have that $V_{EB_{ON}} = V_{ON} \approx 0.7$ V. For the OP analysis, firstly, we have that the input voltage is the output voltage from the Gain Stage, V_{O_1}. By applying KVL, the equation

$$I_E = \frac{V_{CC} - V_{EB_{ON}} - V_{O_1}}{R_{out}} \tag{6}$$

As we can see in Table 3, the current I_E is quite bigger that the one obtained in the Gain Stage. This aspect justifies the usage of the Output Stage circuit: as seen in Table 5, the output impedance from the Gain Stage, Z_{O_1}, is quite large, thus it could not be connected to the 8 Ω resistance in the load (the audio device). Now, because of the Output Stage, part of the current I_E will feed the load, which will help us at obtaining a smaller output impedance. Another thing to notice is that, as seen in Table 3, the voltage V_{CE}, which is now given by $V_{CE} = -V_{O_2} - R_E I_E$, has an absolute value of 12 V, as expected, because of V_{CC} and the fact that the capacitor isn't taken here into account. Therefore, this voltage is bigger than V_{ON} (given by this expression because of the currents defined in the PNP transistor), which guarrantees that we are still working in a Forward Active Region, as intended.

Name	**Value**
I_E (Gain Stage)	5.3802 mA
I_E (Output Stage)	93.0060 mA
$\|V_{CE}\|$	12.0 V
$V_{EB_{ON}}$	0.7 V

Table 3: Values of current I_E obtained for the Gain and Output Stages by theoretical analysis.

By incremental analysis, the gain and the input and output impedances of the Output Stage can be easily computed. They are given by the following equations:

$$AV_2 = \frac{g_m}{g_\pi + g_E + g_o + g_m} \tag{7}$$

$$Z_{I2} = \frac{g_\pi + g_E + g_o + g_m}{g_\pi(g_\pi + g_E + g_o)} \tag{8}$$

$$Z_{O2} = \frac{1}{g_\pi + g_E + g_o + g_m} \tag{9}$$

Where $g_m = \frac{I_C}{V_T}$, $g_o = \frac{I_C}{V_A}$, $g_\pi = \frac{g_m}{\beta_f}$ and $g_E = \frac{1}{R_{out}}$. For the Output Stage and the PNP transistor, the current I_C is given by $I_C = \frac{\beta_F}{1+\beta_F} I_E$ and the values of β_F and V_A are those used for the PNP model in Ngspice, as mentioned above. Taking the whole circuit (Gain Stage+Output Stage) into account, it is now necessary to obtain the gain AV and the output impedance Z_O. The input impedance of the whole circuit is given by $Z_I = Z_{I1}$. By studying the circuit in an incremental analysis, the following expressions are obtained:

$$AV = \frac{\frac{1}{r_{\pi 2}+Z_{O1}} + \frac{g_{m2} r_{\pi 2}}{r_{\pi 2}+Z_{O1}}}{\frac{1}{r_{\pi 2}+Z_{O1}} + \frac{1}{R_{E2}} + \frac{1}{r_{o2}} + \frac{g_{m2} r_{\pi 2}}{r_{\pi 2}+Z_{O1}}} AV_1 \tag{10}$$

$$Z_O = \frac{1}{g_{o2} + g_{m2}\frac{r_{\pi 2}}{r_{\pi 2}+Z_{O1}} + g_{e2} + \frac{1}{r_{\pi 2}+Z_{O1}}} \tag{11}$$

In the above expressions, the index 1 refers to values calculated for the Gain Stage and the index 2 corresponds to values determined for the Output Stage.

In Table 4, shown below, are the values, obtained through the OP analysis discussed below, which will be compared with the OP results of the Ngspice simulation. The DC (operating point) components of V_{in}, V_{in2} and V_{out} are zero because it was established, since the start, that the input voltage had no DC component.

Name	Value [V]
V_{base}	1.238024e+00
V_{coll}	6.649701e+00
V_{emit}	5.380240e-01
V_{emit2}	7.349701e+00
V_{in}	0.000000e+00
V_{in2}	0.000000e+00
V_{out}	0.000000e+00
V_{vcc}	1.200000e+01

Table 4: Operating point voltages to be compared with the simulation's results.

The values obtained for all the input and output impedances were the following:

Name	Value [Ω]
Z_{I1}	786.260649
Z_{O1}	928.710486
Z_{I2}	6007.575337
Z_{O2}	0.276371
Z_I	786.260649
Z_O	3.959082

Table 5: Values obtained for the impedances by theoretical analysis.

The values obtained for the gains were the following:

Name	Value
AV_1	-89.860235
AV_1 [dB]	39.071351
AV_2	0.989432
AV_2 [dB]	-0.092284
AV	-81.859383
AV [dB]	38.261369

Table 6: Values obtained for the gains by theoretical analysis.

As we can see by both tables above, the input impedance Z_{I2} is of the same order of magnitude and relatively similar to Z_{O1} from the Gain Stage, thus it is quite compatible. This is one of the reasons why the two stages can be connected without significant signal loss. Moreover, the final output impedance Z_O is smaller than 8Ω, the speaker's resistance. Thus, the circuit obtained in this laboratory assignment is very good to connect to the 8Ω load. This means that the output stage is an essential part of this circuit, because we were able to drastically decrease the output voltage from the Gain Stage, which could (should) not be connected to the speaker.

As for the gains, we can see that the final gain AV is quite large in absolute value. This means that the audio amplifier is doing its desired job and is increasing the input signal's amplitude. It is worth noting that the minus sign means that the output signal has a phase difference (of approximately π rad) from the input; however, that is not a problem, because the sound the listener will ear is not qualitatively affected, that is, the human ear is indifferent to this phase difference. On the other hand, the gain AV_2, from the Output Stage, is very close to 1, as expected.

Finally, a plot with the gain of the total circuit must be plotted. In order to do this, it is necessary to determine the lower cutoff frequency, from which the gain will begin to have the

value AV obtained above. For frequencies smaller than the cutoff frequency f_L, the plot of the gain in DB has a slope of +20 dB. The lower cutoff (angular) frequency for the circuit is given by

$$\omega_L \approx \sum_j \frac{1}{R_{eq_j} C_j} = \frac{1}{R_{eq_i} C_i} + \frac{1}{R_{eq_b} C_b} + \frac{1}{R_{eq_2} C_2} \tag{12}$$

Where R_{eq_j} is the resistance at the terminals of the j-th capacitor C_j with all other capacitors replaced by short-circuits. The product $R_{eq_j} C_j$ is called the short-circuit time constant associated with C_j. By analysing the circuit in this way, it was possible to conclude that these equivalent resistances are given by:

$$R_{eq_i} = R_S + Z_{I1} \tag{13}$$

$$R_{eq_b} = R_E \,||\, \frac{R_S || R_B + r_{\pi 1}}{1 + g_{m1} r_{\pi 1}} \tag{14}$$

$$R_{eq_2} = R_L + Z_O \tag{15}$$

Where the index 1 refers to values determined for the Gain Stage. Having determined ω_L, it is straightforward to obtain the cutoff frequency, which is given by $f_L = \frac{\omega_L}{2\pi}$ and is shown in Table 7. On the other hand, the higher cutoff frequency could be determined by considering the small capacitances of the transistors and not the circuit's capacitors. However, in order to plot the graph in Figure 4, the value f_H of this frequency was the one obtained from Ngspice. From this frequency beyond, it is considered that the graph is a line with slope -20 dB.

Name	Value [Hz]
f_L	30.831081

Table 7: Value obtained for the cutoff frequency by theoretical analysis.

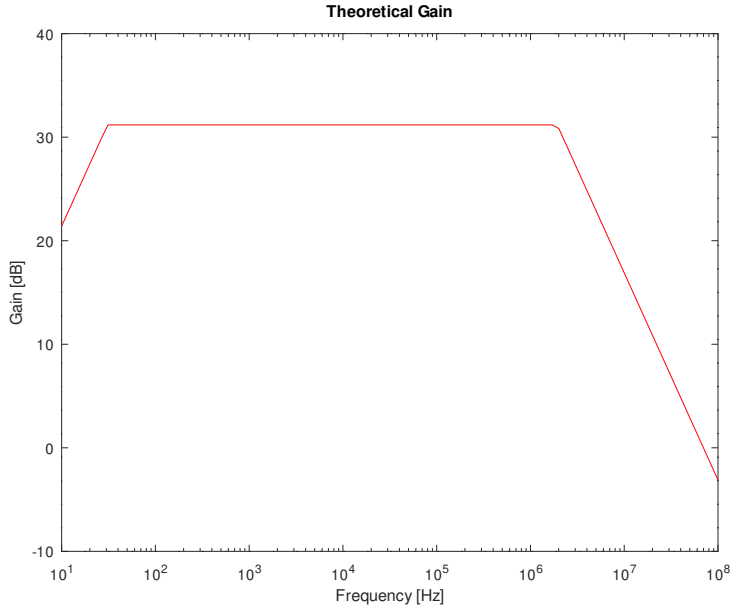


Figure 4: Plot of the gain with respect to frequency, as obtained by theoretical analysis.

The results shown in this section will be further analysed by comparing them side by side with the simulation's values and plots.

3 Simulation Analysis

In order to simulate this circuit with Ngspice, real models of NPN and PNP transistors were used, as it was discussed before. These models are very complex compared to the theoretical model used previously. Because of this, it is expected for there to be significant differences between the results from the two sections.

The simulation was done by taking the base script and tinkering with the values in order to improve the model. The bandwidth was improved as much as possible, since an audio amplifier should worrk for a wide range of frequencies, in particular those that the human ear can process (i.e., from 20 Hz to 20 kHz, approximately). Firstly, the most relevant Operating Point values from Sections 2 and 3 will be compared.

Theoretical	
Designation	**Value [V]**
V_{base}	1.238024e+00
V_{coll}	6.649701e+00
V_{emit}	5.380240e-01
V_{emit2}	7.349701e+00
V_{in}	0.000000e+00
V_{in2}	0.000000e+00
V_{out}	0.000000e+00
V_{vcc}	1.200000e+01

Simulation	
Node	**Voltage value [V]**
base	1.239489e+00
coll	7.143387e+00
emit	5.473596e-01
emit2	7.964059e+00
in	0.000000e+00
in2	0.000000e+00
out	0.000000e+00
vcc	1.200000e+01

Table 8: Comparison between theoretical and simulation OP analysis' results.

As we can see, the values confirm that the transistors are working in a forward active region, as it was seen for the theoretical analysis. This means that, for the NPN transistor, $V_{CE} > V_{BE}$, and that, for the PNP transistor, $V_{EC} > V_{EB}$. The values of the theoretical and simulation analysis are not too far off eachother. This means that the model used in the previous section is a quite good approximation. However, it does lack in some aspects. For instance, a medium frequencies incremental model was considered, which allowed us to not consider the capacitor. Moreover, an approximation was used for V_{ON}, and that is not the case in Ngspice, which, in its turn, uses very complex models for the transistors, thus very likely more accurate. The null voltages in nodes in, in2 and out were to be expected, since the input signal does not have a DC component.

As shown next, the input and output impedances of the system as a whole (Gain Stage+Output Stage) were determined. The output impedance was simulated with V_{in} turned off and a voltage source with amplitude of 1V in the output. The results obtained are shown in Table 9, together with the theoretical analysis'.

Theoretical	
Designation	**Value [Ω]**
Z_I	7.862606e+02
Z_O	3.959082e+00

Simulation	
Designation	**Value [Ω]**
in impedance	8.618356e+02
out impedance	8.556043e+00

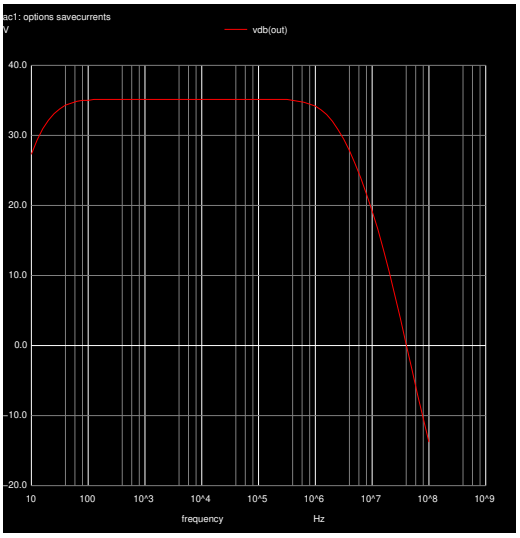
Table 9: Comparison between theoretical and simulation's input and output impedances considering the whole circuit.

As it was intended, the input impedance is high and the output impedance is small. Although improvements where made to make the output impeadance as low as possible, this value is, perhaps, still a bit high. From Table 9 the disparities between the theoretical model and the simulation's results are quite apparent, having obtained a very good output impedance with

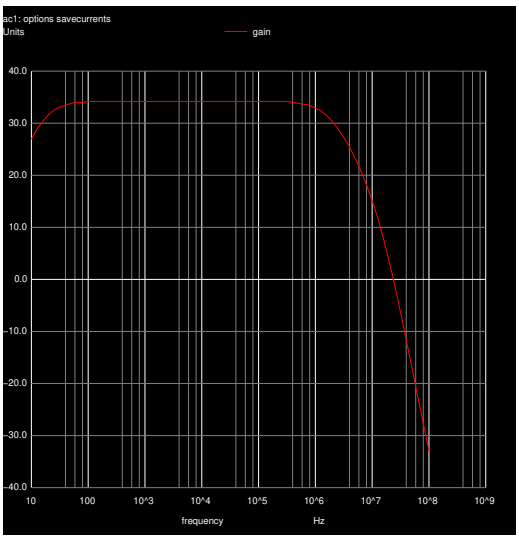
the first and a higher (and less desirable) one with the simulation. However, it is also worth noting that the values of the circuit's resistances and capacitances were chosen in order to simultaneously obtain good results and to keep the cost as low as possible.

Now, the plots of the output signal and the gain are presented. For a transient analysis of frequency f=1kHz for the input signal, the output has been plotted in Figure 6. We can notice that there are no observable losses from the original signal, that is, the wave is still sinusoidal. The plot was made after the inicial period of time in order to represent the system without transitory solutions.

Regarding the plot of the gain, it is clearly very similar to the one obtained in Section 2. Between the lower cutoff frequency and the higher cutoff frequency, the gain shows no noticible variations. Moreover, for frequencies lower than the lower cutoff frequency, we can see that the plot is approximately a line of constant positive slope, and it is very similar to a line of constant negative slope for higher frequencies.



(a) Output signal response to frequency



(b) Gain

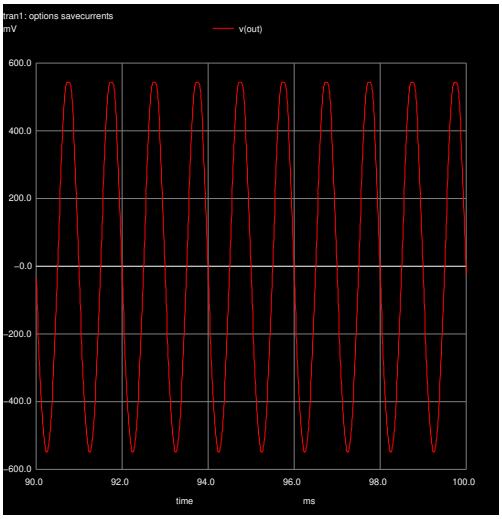


Figure 6: Output signal variance with time for f=1kHz

Having the values showed and plotted before, we are able to determine all the recquired information about the output. The lower cutoff frequency (*lowfrequence* in the table shown below) and the higher cutoff frequency (*highfrequence*) are determined by taking the maximum output signal and computing where it drops by 3dB. By subtracting these two values, the bandwidth is obtained. Finally, the maximum value of the gain plotted in Figure 5b is obtained. All these results are presented in Table 10. The highcutoff frequency and the bandwidth for the theoretical analysis are not shown because, in order to plot the gain in Section 2, the value *highfrequence* obtained in Ngspice was used. As seen in Table 10, there is a clear difference between the values obtained in Sections 2 and 3. Firstly, it is worth noting that equation 12 corresponds to an approximate value of the actual cutoff frequency, which might help explain the difference observed. For the Ngspice simulation, the values of the resistances and capacitances were chosen in order to obtain a good *lowfrequence* (amongst other quantities, like the gain). Thus, this discrepancy shows once again the limitations of the theoretical model used. Not only does equation 12 give an approximate value, it also depends on values of impedances which are themselves approximate values that come from the theoretical analysis. Once again, it is clear that Ngspice uses a quite different model for the transistors. On the other hand, we can see that the gain of the circuit (AV and *gainfinal* shown below) are quite similar, which shows that the theoretical model, even though relatively far from ideal, still produces good approximations.

Theoretical	
Designation	**Value**
f_L [Hz]	3.083108e+01
AV [dB]	3.826137e+01

Simulation	
Designation	**Value [Hz or dB]**
lowfrequence	1.991176e+01
highfrequence	1.928995e+06
bandwidth	1.928975e+06
gainfinal	3.425236e+01

Table 10: Values obtained for the lower and higher cutoff frequencies (in Hz) and the final gain (in dB), for both the simulation and the theoretical analysis; bandwidth (in Hz) for the simulation.

Finally, the total monetary cost and the merit M of the circuit have been calculated and are shown below in Table 11. These were determined by using the results obtained from Ngspice. The cost is given by $cost = cost\ of\ resistors\ +\ cost\ of\ capacitor\ +\ cost\ of\ transistores$, in which each $1k\Omega$ in the resistances costs 1 monetary unit (MU), as well as each $1\mu F$ in the capacitance; the cost of each transistor is 0.1 MU. On the other hand, the merit M is given by

$$M = \frac{voltageGain \times bandwidth}{cost \times lowerCutoffFreq} \tag{16}$$

Designation	Value
cost	3.881450e+03
merit	8.548964e+02

Table 11: Cost and merit obtained for this circuit.

4 Conclusion

In this laboratory assignment, the intended objective has been achieved. The AC/DC converter has been simulated accordingly by using Ngspice and a rather precise output voltage as close to 12V as possible has been obtained. Moreover, a suitable theoretical model was utilized in order to predict the output of the simulated circuit, having obtained a voltage quite close to the one obtained in Ngspice. However, the value obtained in this analysis was slightly further away from the desired 12V DC output voltage. The differences between the results obtained in both analysis may be due to several factors. The theoretical diode model considered is different from the much more complex diode model used by Ngspice. Moreover, the theoretical analysis is subjected to certain approximations and a nonlinear equation must be solved.

A ripple of approximately 10^{-4}V was obtained for both cases. A smaller value could have been obtained by using bigger values for R_1 and C, for example. However, that would also lead to a larger monetary cost. By taking into account the different aspects at hand, rather precise results and an acceptable merit M have been obtained.