TÉCNICO LISBOA

Circuits Theory and Electronic Fundamentals

Integrated Master in Engineering Physics, IST, University of Lisbon

Lab 3: AC/DC Converter

Alexandre Sequeira (96503), Duarte Marques (96523), João Chaves (96540)

May 8th 2021

Contents

1 Introduction

The objective of this laboratory assignment is to use an AC/DC converter to obtain an output DC signal of value 12 V from an input AC signal of amplitude 230 V and frequency 50 Hz. The envelope detector and voltage regulator circuits were chosen as shown in Figure 1, in which designations have been assigned to each node.

The envelope detector is formed by a full-wave bridge rectifier circuit, with 4 diodes connected to the resistor R_1, in parallel with the capacitor. On the other hand, the voltage regulator corresponds to the resistance R_2 in series with a positive voltage limiter (17 diodes in series). The values of the resistances and the capacitance and the number of diodes were chosen in order to decrease the monetary cost of the circuit and approximate the output signal to a constant 12 V as much as possible.

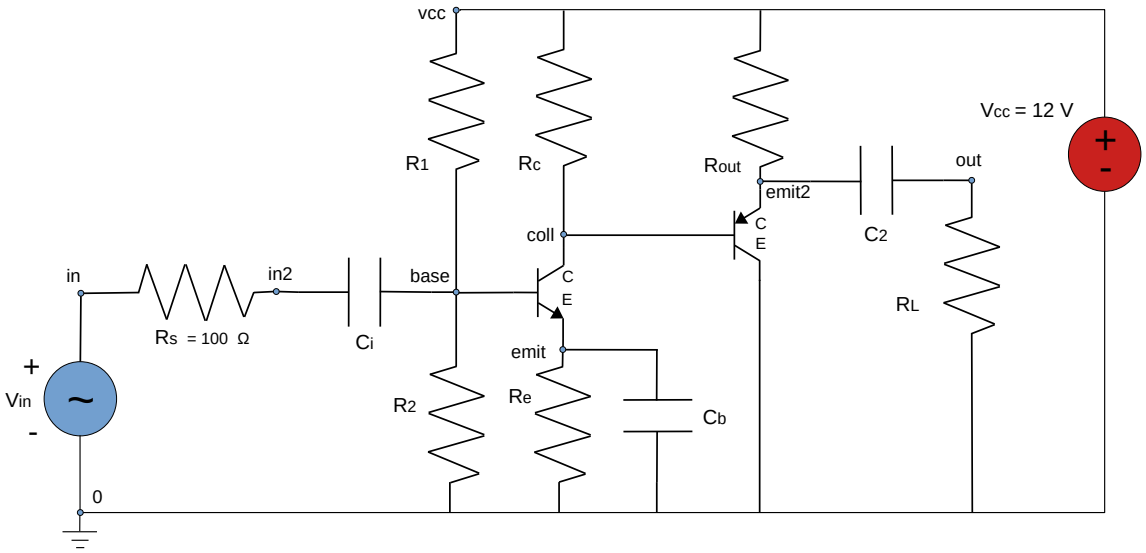


Figure 1: Circuit to be analysed in this laboratory assignment.

2 Theoretical Analysis

The full-wave bridge rectifier circuit, assuming ideal diodes, computes the absolute value of the sinusoidal AC voltage of the second transformer. Therefore, the voltage in resistor R_1's terminals is given by

$$v_{O_{rectified}}(t) = |v_{t2}| \tag{1}$$

Where v_{t2} is the AC voltage in the secondary, given by $v_{t2} = \frac{v_{t1}}{n}$, assuming that the transformers' wires are coiled according to the conventional way, that is, in order to have a downwards current through the primary and an upwards current through the secondary. The value of n corresponds to the proportion of turns between the primary and the secondary, as shown in Figure 1. Moreover, the capacitor, connected to the rectifier, transforms the rectified wave by attenuating the oscillations. Again, assuming the ideal diode model, after a time t_{OFF}, when the rectified signal's voltage value starts to decrease more abruptly, the current in the capacitor, given by $i_C = C\frac{dv_c}{dt}$, becomes very large, the diode eventually goes off and the capacitor starts discharging. This value can be computed by:

$$t_{OFF} = \frac{1}{\omega} atan\left(\frac{1}{\omega R_1 C}\right) \tag{2}$$

Where $\omega = 2\pi f$ is the angular frequency and $f = 50$ Hz is given. The diode starts conducting again after t_{ON}, in which the rectified signal's voltage equals the discharging capacitor's. While the capacitor is charging and the diodes are conducting, the voltage out of the envelope detector is given by $v_{O_{env}}(t) = v_{O_{rectified}}(t)$ (3). On the other hand, while the capacitor is discharging, it is given by:

$$v_{O_{env}}(t) = V_{t2} cos(\omega t_{OFF}) e^{-\frac{t - t_{OFF}}{R_1 C}} \tag{4}$$

The value V_{t2} is the amplitude of the voltage v_{t2} in the secondary. It is worth noting that t_{OFF} in the exponential above must be summed half a period, $\frac{T}{2} = \frac{1}{2f}$, every time equation 4 is used again (i.e., every "cycle" of charging-discharging in the capacitor).

Finally, the voltage regulator is used to attenuate the oscillations in the Envelope Detector's output voltage. In this case, the ideal diode model is not used; instead, the diode model with a

voltage source and a resistor is taken into account; a DC analysis and an incremental analysis are made. The diode equation, given by

$$i_D = I_S \left(e^{\frac{v_D}{\eta V_T}} - 1 \right) = I_S \left(e^{\frac{v_{OUT}}{N \eta V_T}} - 1 \right) \tag{5}$$

Returns the value of the current that passes in each diode. The saturation current's value used in this laboratory assignment is $I_S = 1.0 \times 10^{-14}$ A, which is the value used by Ngspice in its default diode model. This model was utilized in Section 3. On the other hand, the thermal voltage is given by $V_T = \frac{kT}{q} \approx 26$ mV at room temperature (considering $k = 1.38064852 \times 10^{-23}$ $m^2\ kg\ s^{-2}\ K$, $q = 1.60217662 \times 10^{-19}$ C and $T = 300.15$ K, which is the temperature considered by Ngspice). It was also considered that $\eta = 1$, because that is the value used by Ngspice. Because there are $N = 17$ equal diodes in series, the voltage drop through each of them is given by $v_D = \frac{v_{OUT}}{N}$, where $v_{OUT} = v_{out2}$, thus the relation given in 5.

By applying the Kirchhoff Voltage Law to the rightmost mesh, the following non-linear equation is obtained:

$$v_{OUT} + R_2 I_S \left(e^{\frac{v_{OUT}}{N \eta V_T}} - 1 \right) - v_{O_{env}} = 0 \tag{6}$$

The equation shown above was solved by using Octave and Newton Raphson's iterative method, in which the iterations are given by $x_{n+1} = x_n - \frac{f(x_n)}{f'(x_n)}$, with $f(x_n) \equiv f(v_{OUT}) = 0$ given by equation 6. It was decided to solve this system not for every instant, but only for the DC components of the voltages. Therefore, $V_{O_{env}}$ was given by the average of the voltage $v_{O_{env}}$, obtained previously. In this way, the DC component V_{OUT} was obtained. Next, the incremental analysis was taken into account. The incremental resistance of each diode is given by

$$r_d = \frac{\eta V_T}{I_S e^{\frac{V_{OUT}}{N \eta V_T}}} \tag{7}$$

Additionally, the incremental component of the output voltage is given by

$$v_{out}(t) = \frac{N r_d + R_2}{N r_d} v_{o_{env}}(t) \tag{8}$$

Where $v_{o_{env}}(t) = v_{O_{env}}(t) - V_{O_{env}}$ was calculated for every instant. The final output voltage, between nodes out2 and 0 of Figure 1, is given by:

$$v_{OUT}(t) = V_{OUT} + v_{out}(t) \tag{9}$$

Having presented the theoretical aspects at hand, it is worth mentioning the values used for the resistances and the capacitance, as well as the value of n, i.e., the quotient between the voltages in the primary and secondary, respectively. These are presented in Table 1, shown below.

Name	Value

Table 1: Values used for the resistances R_1 and R_2, the capacitance C, the amplitude V_{T2} of the secondary's AC voltage and the quotient n.

These were the same values used in the Ngspice simulation, presented in Section 3, in order to properly compare the results obtain by both methods. They were chosen in order to minimize the ripple and to obtain a final average output voltage as close to 12 V as possible, through the Ngspice simulation (these results will be shown in Tables **??** and 3). At the same time, the values of R_1, R_2 and C were kept as low as possible, in order to reduce the cost and increase the merit of the work as much as possible (these values are calculated at the end of Section 3). Moreover, we also chose the number of diodes and the voltage in the transfomer's

secondary in a way that kept this voltage sufficiently smaller than the primary's (so that the transformer decreases the voltage, not increase it). Conjugating all these different factors, the values presented in Table 1 were chosen.

By using equations 3 and 4, the output voltage of the Envelope Detector circuit is plotted below, for 10 periods (with each period given by $T = \frac{1}{2f}$, because the rectified signal has double the frequency of the original sinusoidal voltage). In the same figure, the voltage at the output of the Voltage Regulator circuit is shown. Even though it wasn't requested, the rectified signal is also shown.

Because the oscillations in the output voltages are very small, it was decided to plot them separately, but for only 6 periods, in order to visualize the signals in more detail. These plots are shown in Figures **??** and **??**. In Figure **??**, the value of $v_{OUT} - 12$V over the 10 initial periods has been plotted.

3 Simulation Analysis

In order to simulate this circuit with Ngspice, real models of npn and pnp transistors where used. We realised that this models are very complex in reagards to the thheoretical models used previously. Because of this we expect there to be significant difference between the results.

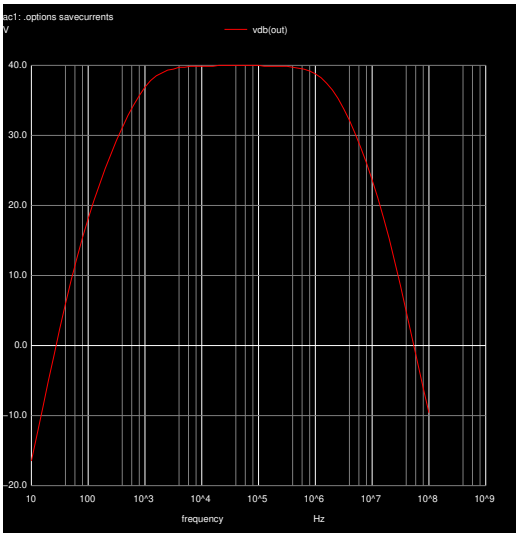
The simulation was done by taking the base script and tinkering with the values in order to improve the model. We strived to improve the bandwidth mainly since this was, observing the output graphs and value, the component that was lacking the most given that this was a audio amplifier and should worrk for a wide range of frequencies. Initially we started by determining the input and output impeadances os the system as a hole (gain stage + output stage). The output impeadance was simulated with V_{in} turned off and a voltage source with amplitude of 1 V in the output. The results obtained are the following in table 2.

Designation	**Value [Ω]**
in impeadance	5.562600e+02
out impeadance	7.802860e+00

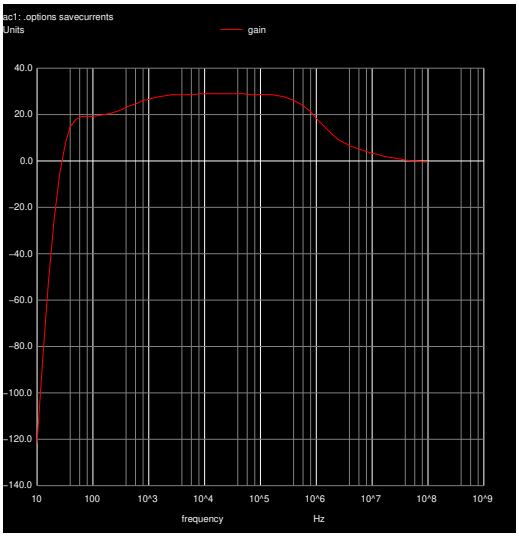
Table 2: Output and Input impeadances

As we wanted the input impeadance is high and the output is small. Although improvements where made to take the out impeadance as low as we could this value is, perhaps, still a bit high and if it was better maybe it would make a better amplifier.

We can now analise the graphics of the output signal and the gain.



(a) Output signal



(b) Gain

Analysing now the graphs obtained we are able to determine all the important information about the output. Looking initially at figure 2a, we start by obtaining the lower(lowfrequence) and higher(highfrequence) cutoff frequencies which are determined by taking the maximum output signal and seeing where this drops 3 dB. With this two values we subtract them and obtained bandwidth. Finaly looking now at figure 2b we obtain the maximum value of the gain. All the results are presented in table 3

Designation	**Value [Hz and dB]**
lowfrequence	1.020132e+03
highfrequence	1.810105e+06
bandwidth	1.809085e+06
gainfinal	2.883218e+01

Table 3: Lower frequency(Hz), high frequency(Hz), bandwidth(Hz) and gain(dB)

Finally, the total monetary cost and the merit M of the circuit used have been calculated and are shown below in Table 4. These were determined by using the results obtained from Ngspice. The cost is given by $cost = cost\ of\ resistors + cost\ of\ capacitor + cost\ of\ transistores$, in which each $1k\Omega$ in the resistances costs 1 monetary unit (MU), as well as each $1\mu F$ in the capacitance; the cost of each transistor is 0.1 MU. On the other hand, the merit M is given by

$$M = \frac{voltageGain \times bandwidth}{cost \times lowerCutoffFreq} \tag{10}$$

Designation	Value
cost	1.611800e+03
merit	3.172261e+01

Table 4: Cost and merit obtained for this circuit.

4 Conclusion

In this laboratory assignment, the intended objective has been achieved. The AC/DC converter has been simulated accordingly by using Ngspice and a rather precise output voltage as close to 12V as possible has been obtained. Moreover, a suitable theoretical model was utilized in order to predict the output of the simulated circuit, having obtained a voltage quite close to the one obtained in Ngspice. However, the value obtained in this analysis was slightly further away from the desired 12V DC output voltage. The differences between the results obtained in both analysis may be due to several factors. The theoretical diode model considered is different from the much more complex diode model used by Ngspice. Moreover, the theoretical analysis is subjected to certain approximations and a nonlinear equation must be solved.

A ripple of approximately 10^{-4}V was obtained for both cases. A smaller value could have been obtained by using bigger values for R_1 and C, for example. However, that would also lead to a larger monetary cost. By taking into account the different aspects at hand, rather precise results and an acceptable merit M have been obtained.