TÉCNICO LISBOA

Circuits Theory and Electronic Fundamentals

Integrated Master in Engineering Physics, IST, University of Lisbon

Lab 3: AC/DC Converter

Alexandre Sequeira (96503), Duarte Marques (96523), João Chaves (96540)

May 8th 2021

Contents

1 Introduction

The objective of this laboratory assignment is to use an AC/DC converter to obtain an output DC signal of value 12 V from an input AC signal of amplitude 230 V and frequency 50 Hz. The envelope detector and voltage regulator circuits were chosen as shown in Figure 1, in which designations have been assigned to each node.

The envelope detector is formed by a full-wave bridge rectifier circuit, with 4 diodes connected to the resistor R_1, in parallel with the capacitor. On the other hand, the voltage regulator corresponds to the resistance R_2 in series with a positive voltage limiter (17 diodes in series). The values of the resistances and the capacitance and the number of diodes were chosen in order to decrease the monetary cost of the circuit and approximate the output signal to a constant 12 V as much as possible.

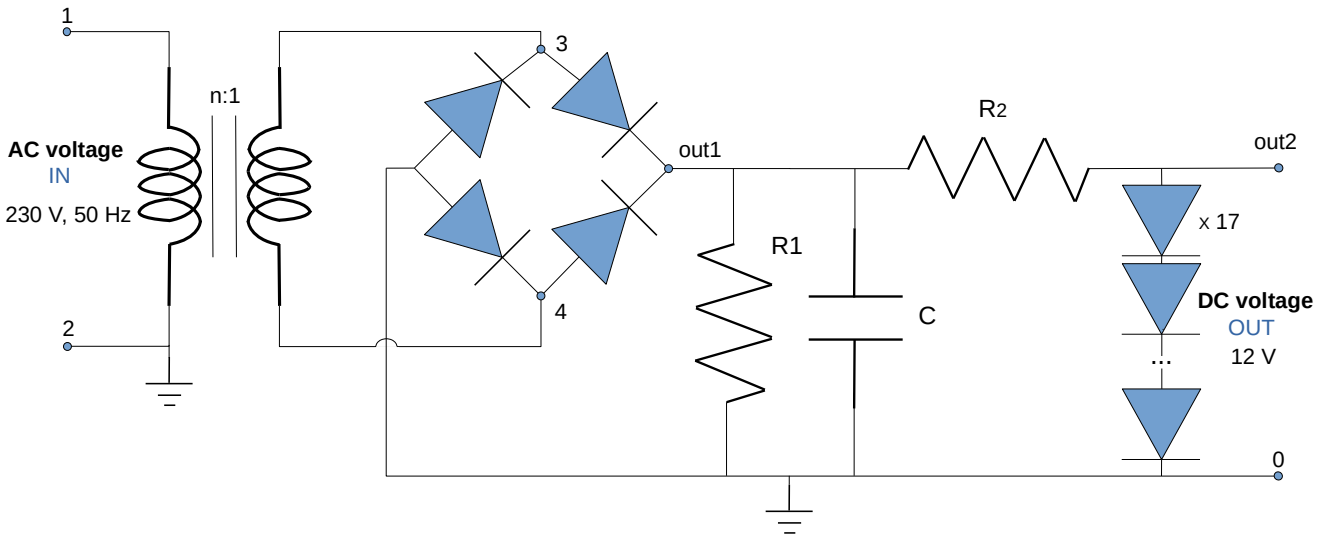


Figure 1: Circuit to be analysed in this laboratory assignment.

2 Theoretical Analysis

The full-wave bridge rectifier circuit, assuming ideal diodes, computes the absolute value of the sinusoidal AC voltage of the second transformer. Therefore, the voltage in resistor R_1's terminals is given by

$$v_{O_{rectified}}(t) = |v_{t2}| \tag{1}$$

Where v_{t2} is the AC voltage in the secondary, given by $v_{t2} = \frac{v_{t1}}{n}$, assuming that the transformers' wires are coiled according to the conventional way, that is, in order to have a downwards current through the primary and an upwards current through the secondary. The value of n corresponds to the proportion of turns between the primary and the secondary, as shown in Figure 1. Moreover, the capacitor, connected to the rectifier, transforms the rectified wave by attenuating the oscillations. Again, assuming the ideal diode model, after a time t_{OFF}, when the rectified signal's voltage value starts to decrease more abruptly, the current in the capacitor, given by $i_C = C\frac{dv_c}{dt}$, becomes very large, the diode eventually goes off and the capacitor starts discharging. This value can be computed by:

$$t_{OFF} = \frac{1}{\omega} atan\left(\frac{1}{\omega R_1 C}\right) \tag{2}$$

Where $\omega = 2\pi f$ is the angular frequency and $f = 50$ Hz is given. The diode starts conducting again after t_{ON}, in which the rectified signal's voltage equals the discharging capacitor's. While the capacitor is charging and the diodes are conducting, the voltage out of the envelope detector is given by $v_{O_{env}}(t) = v_{O_{rectified}}(t)$ (3). On the other hand, while the capacitor is discharging, it is given by:

$$v_{O_{env}}(t) = V_{t2} cos(\omega t_{OFF}) e^{-\frac{t - t_{OFF}}{R_1 C}} \tag{4}$$

The value V_{t2} is the amplitude of the voltage v_{t2} in the secondary. It is worth noting that t_{OFF} in the exponential above must be summed half a period, $\frac{T}{2} = \frac{1}{2f}$, every time equation 4 is used again (i.e., every "cycle" of charging-discharging in the capacitor).

Finally, the voltage regulator is used to attenuate the oscillations in the Envelope Detector's output voltage. In this case, the ideal diode model is not used; instead, the diode model with a

voltage source and a resistor is taken into account; a DC analysis and an incremental analysis are made. The diode equation, given by

$$i_D = I_S \left(e^{\frac{v_D}{\eta V_T}} - 1 \right) = I_S \left(e^{\frac{v_{OUT}}{N \eta V_T}} - 1 \right) \tag{5}$$

Returns the value of the current that passes in each diode. The saturation current's value used in this laboratory assignment is $I_S = 1.0 \times 10^{-14}$ A, which is the value used by Ngspice in its default diode model. This model was utilized in Section 3. On the other hand, the thermal voltage is given by $V_T = \frac{kT}{q} \approx 26$ mV at room temperature (considering $k = 1.38064852 \times 10^{-23}$ $m^2\ kg\ s^{-2}\ K$, $q = 1.60217662 \times 10^{-19}$ C and $T = 300$ K). It was also considered that $\eta = 1$, because that is the value used by Ngspice. Because there are $N = 17$ equal diodes in series, the voltage drop through each of them is given by $v_D = \frac{v_{OUT}}{N}$, where $v_{OUT} = v_{out2}$, thus the relation given in 5.

By applying the Kirchhoff Voltage Law to the rightmost mesh, the following non-linear equation is obtained:

$$v_{OUT} + R_2 I_S \left(e^{\frac{v_{OUT}}{N \eta V_T}} - 1 \right) - v_{O_{env}} = 0 \tag{6}$$

The equation shown above was solved by using Octave and Newton Raphson's iterative method, in which the iterations are given by $x_{n+1} = x_n - \frac{f(x_n)}{f'(x_n)}$, with $f(x_n) \equiv f(v_{OUT}) = 0$ given by equation 6. It was decided to solve this system not for every instant, but only for the DC components of the voltages. Therefore, $V_{O_{env}}$ was given by the average of the voltage $v_{O_{env}}$, obtained previously. In this way, the DC component V_{OUT} was obtained. Next, the incremental analysis was taken into account. The incremental resistance of each diode is given by

$$r_d = \frac{\eta V_T}{I_S e^{\frac{V_{OUT}}{N \eta V_T}}} \tag{7}$$

Additionally, the incremental component of the output voltage is given by

$$v_{out}(t) = \frac{N r_d + R_2}{N r_d} v_{o_{env}}(t) \tag{8}$$

Where $v_{o_{env}}(t) = v_{O_{env}}(t) - V_{O_{env}}$ was calculated for every instant. The final output voltage, between nodes out2 and 0 of Figure 1, is given by:

$$v_{OUT}(t) = V_{OUT} + v_{out}(t) \tag{9}$$

Having presented the theoretical aspects at hand, it is worth mentioning the values used for the resistances and the capacitance, as well as the value of n, i.e., the quotient between the voltages in the primary and secondary, respectively. These are presented in Table 1, shown below.

Name	**Value**
R_1	10.75000 $k\Omega$
R_2	5.10979 $k\Omega$
C	5000 μF
V_{T2}	50 V
n	4.6

Table 1: Values used for the resistances R_1 and R_2, the capacitance C, the amplitude V_{T2} of the secondary's AC voltage and the quotient n.

These were the same values used in the Ngspice simulation, presented in Section 3, in order to properly compare the results obtain by both methods. They were chosen in order to

minimize the ripple and to obtain a final average output voltage as close to 12 V as possible, through the Ngspice simulation (these results will be shown in Tables 3 and 4). At the same time, the values of R_1, R_2 and C were kept as low as possible, in order to reduce the cost and increase the merit of the work as much as possible (these values are calculated at the end of Section 3. Moreover, we also chose the number of diodes and the voltage in the transfomer's secondary in a way that kept this voltage sufficiently smaller than the primary's (so that the transformer decreases the voltage, not increase it). Conjugating all these different factors, the values presented in Table 1 were chosen.

By using equations 3 and 4, the output voltage of the Envelope Detector circuit is plotted below, for 10 periods (with each period given by $T = \frac{1}{2f}$, because the rectified signal has double the frequency of the original sinusoidal voltage). In the same figure, the voltage at the output of the Voltage Regulator circuit is shown. Even though it wasn't requested, the rectified signal is also shown.

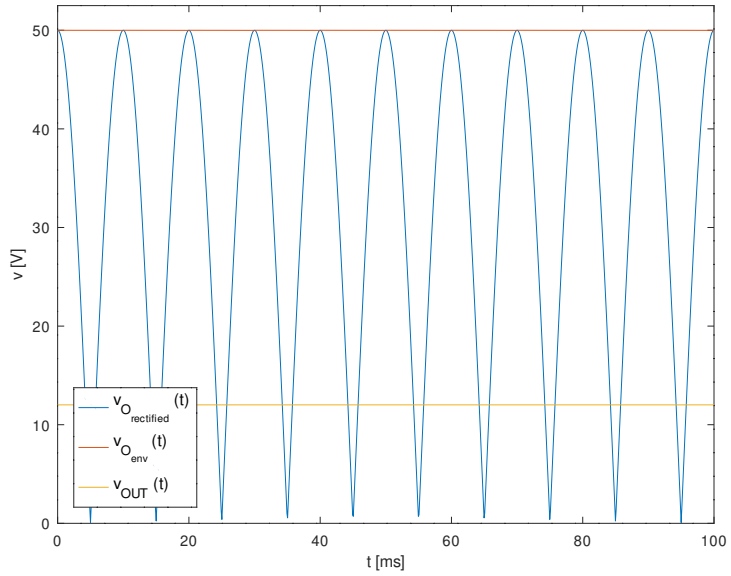
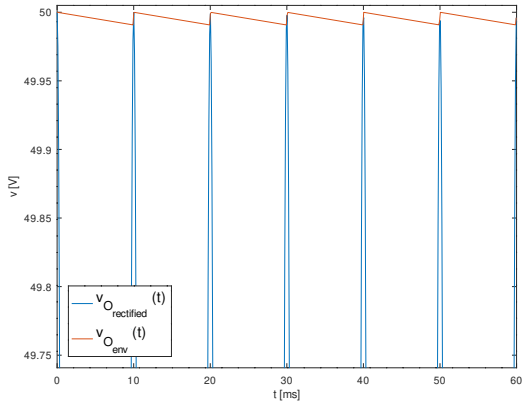
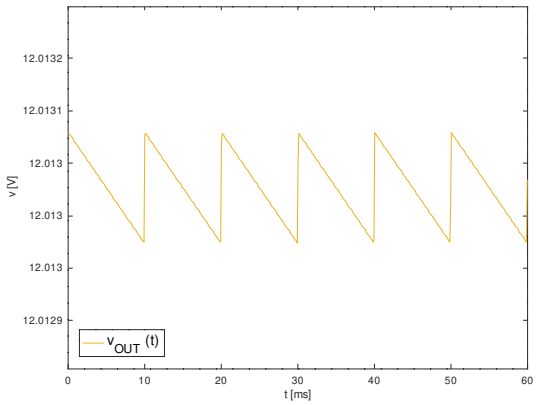


Figure 2: Rectified wave and voltages at the output of the Envelope Detector and Voltage Regulator circuits.

Because the oscillations in the output voltages are very small, it was decided to plot them separately, but for only 6 periods, in order to visualize the signals in more detail. These plots are shown in Figures 3a and 3b. In Figure 4, the value of $v_{OUT} - 12$V over the 10 initial periods has been plotted.



(a) Detailed plot of the Envelope Detector circuit's output voltage with the rectified signal for 6 periods.



(b) Detailed plot of the Voltage Regulator circuit's output voltage for 6 periods.

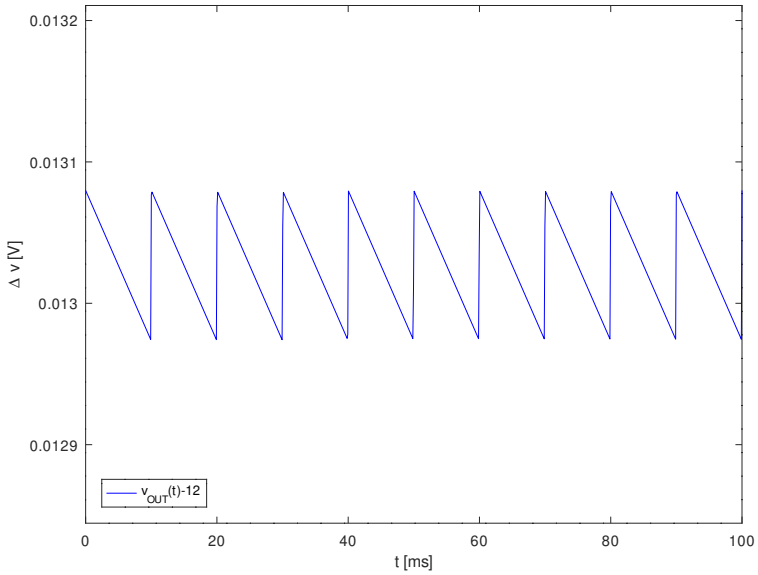


Figure 4: Difference between the final output voltage obtained and the ideal DC signal of 12 V.

Finally, the average final output voltage (output of the Voltage Regulator circuit) was determined, as well as the ripple, given by $ripple(v_{OUT}) = max(v_{OUT}) - min(v_{OUT})$. The values obtained are shown in Table 2.

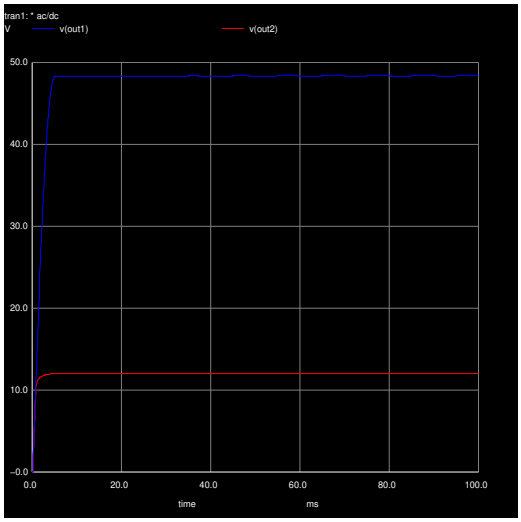
Name	Value [V]
$\overline{v}_{OUT}$	1.201303e+01
$max(v_{OUT})$	1.201308e+01
$min(v_{OUT})$	1.201297e+01
$ripple(v_{OUT})$	1.056472e-04

Table 2: Output voltage's average and ripple.

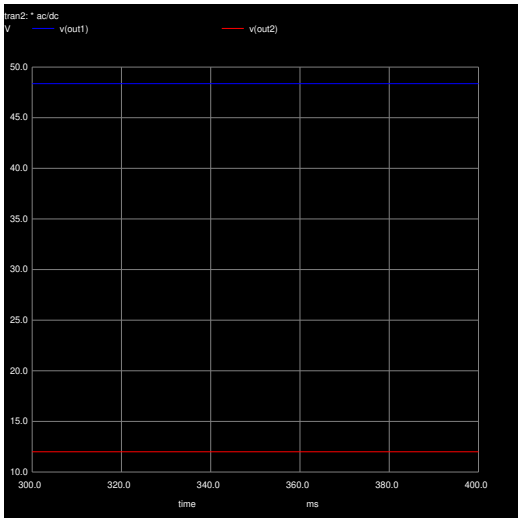
3 Simulation Analysis

In order to simulate this circuit with Ngspice, the ideal transformer model was used. Because the voltage in the primary, v_{T1}, is known, the primary was replaced by a dependant current source and the secondary by a dependant voltage source, in order to have a voltage $v_{T2} = \frac{v_{T2}}{n}$ in the secondary. The values used for R_1, R_2, C, V_{T2} and n are those shown in Table 1 of Section 2.

The plot containing the Envelope Detector's output voltage (voltage in node out1) and the Voltage Regulator's output voltage (voltage in node out2) is shown below, for 10 periods.

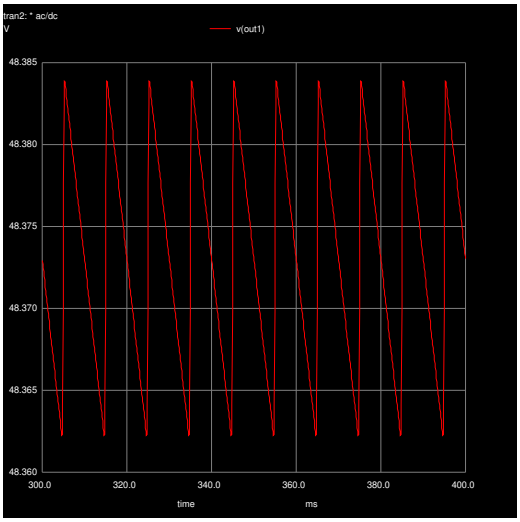


(a) Envelope Detector's output voltage (v(out1)) and Voltage Regulator's output voltage (v(out2)) for the first 10 periods.

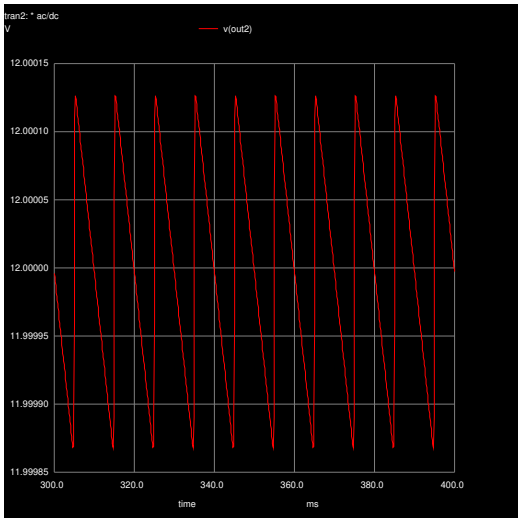


(b) Envelope Detector's output voltage (v(out1)) and Voltage Regulator's output voltage (v(out2)) for 10 later periods.

As we can see in the graphs in Figure 5a, the initial transitory behaviour of the voltages is still clearly present. Therefore, all the values measured in this section were only done in the time interval in which v(out1) and v(out2) are represented in Figure 5b (from 300 ms to 400 ms). Again, as was the case in Section 2, the behaviour of these voltages is not entirely clear from these plots, because the oscillations are very small compared to the y-axis scale. Therefore, separate plots have been made for each voltage, as shown below.



(a) Envelope Detector's output voltage (v(out1)) for the time interval [300,400]ms.



(b) Voltage Regulator's output voltage (v(out2)) for the time interval [300,400]ms.

In Figure 7, the fluctuations of the Voltage Regulator's output around 12 V (i.e., v(out2)-12) have been plotted.

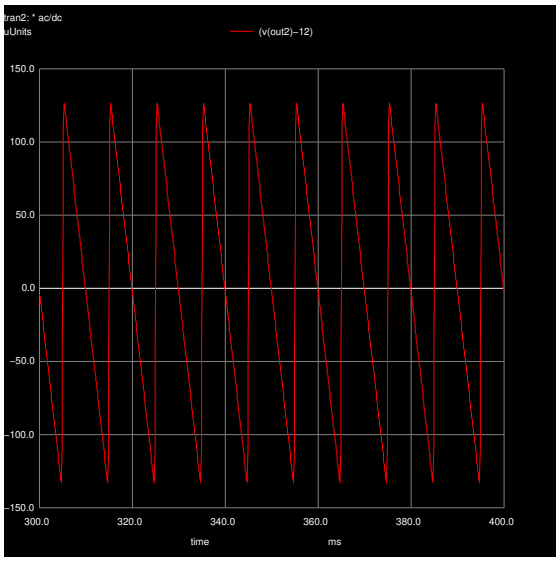


Figure 7: Deviation of output signal from the target DC voltage 12 V over the time interval [300,400]ms.

As we can see, a rather stable 12 V voltage has been obtained.

Now, as in the Theoretical Analysis, the final output's average voltage has been calculated, as well as its ripple, given by $ripple(v_{OUT}) = ripple(v(out2)) = max(v_{OUT}) - min(v_{OUT}) = max(v(out2)) - min(v(out2))$. In Table 3, the results obtained in both cases are shown side by side.

Theoretical	
Designation	**Value [V]**
$\overline{v}_{OUT}$	1.201303e+01
$max(v_{OUT})$	1.201308e+01
$min(v_{OUT})$	1.201297e+01
$ripple(v_{OUT})$	1.056472e-04

Simulation	
Designation	**Value [V]**
$\overline{v}_{OUT}$	1.200000e+01
$max(v_{OUT})$	1.200013e+01
$min(v_{OUT})$	1.199987e+01
$ripple(v_{OUT})$	2.600000e-04

Table 3: Comparison between theoretical and simulation analysis' results.

Finally, the total monetary cost and the merit M of the circuit used have been calculated and are shown below in Table 4. The cost is given by $cost = cost\ of\ resistors + cost\ of\ capacitor + cost\ of\ diodes$, in which each $1k\Omega$ in the resistances costs 1 monetary unit (MU), as well as each $1\mu F$ in the capacitance; the cost of each diode is 0.1 MU. On the other hand, the merit M is given by

$$M = \frac{1}{cost \times (ripple(v_{OUT}) + |\overline{v}_{OUT} - 12| + 10^{-6})} \tag{10}$$

Designation	**Value [V]**
Cost	5.017960e+03
Merit	7.635409e-01

Table 4: Cost and merit obtained for this circuit.

4 Conclusion

In this laboratory assignment, the objective of