TÉCNICO LISBOA

Circuits Theory and Electronic Fundamentals

Integrated Master in Engineering Physics, IST, University of Lisbon

Lab 4: Audio Amplifier

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1 Introduction

The main objective of this laboratory assignment is to simulate an audio amplifier circuit with Ngspice and to compare the results with a theoretical model used to study this circuit. The architectures of the Gain and Output Stages have been chosen as shown in Figure 1, in which designations have been assigned to each node and the circuit's components. The input corresponds to an AC signal of amplitude 10 mV. On the other hand, the output, measured in the *out* node shown below, must be a sine wave with no visible distortion. It is connected to an 8 Ω audio speaker.

The Gain Stage contains the capacitors C_i and C_b and the resistances R_1, R_2, R_c and R_e, as well as a bipolar NPN transistor. The resistances R_{out} and R_L, the capacitor C_o and the bipolar PNP transistor belong to the Output Stage. In order to simulate this circuit in Ngspice, the Philips BC547A BJT model was used for the NPN transistor and the Philips BC557A BJT model was used for the PNP transistor. By studying this circuit, the gain and impedances for both stages have been computed and the frequency response has been plotted in Sections 2 and 3. The values of the circuit's components were selected in order to obtain the desired results and, at the same time, keep the monetary cost as low as possible, in order to keep the merit M (computed in Section 3) as high as possible.

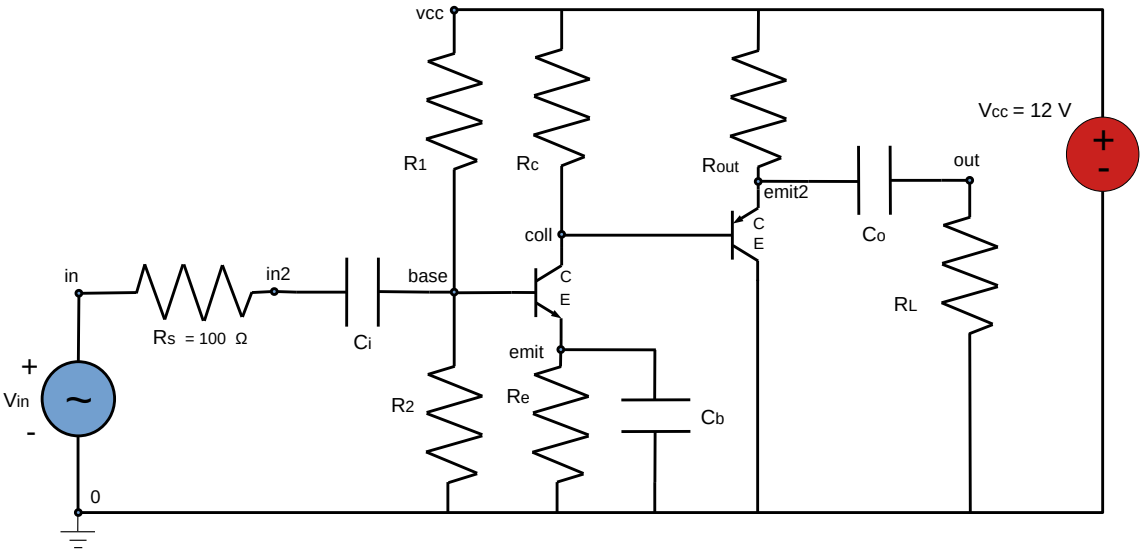


Figure 1: Circuit to be analysed in this laboratory assignment.

2 Theoretical Analysis

The values used for the circuit's resistances and capacitances were determined while doing the Simulation Analysis, in order to get the best possible results, whilst mantaining the monetary cost as low as possible and the merit as high as possible. Using these values, which will be further discussed in Section 3, the theoretical model is applied in this Section, in order to verify its validity and the disparities with the results obtained from Ngspice. The resistances and capacitances used were the following:

Name	Value
R_1	70 kΩ
R_2	10 kΩ
R_C	1 kΩ
R_E	100 Ω
R_{out}	50 Ω
C_i	1 mF
C_b	2 mF
C_o	1 mF

Table 1: Values used for resistances and capacitances in the circuit.

As it was learnt in class, the Gain Stage can be simplified into the circuit shown below, by using the Thévenin's equivalent of the bias circuit.

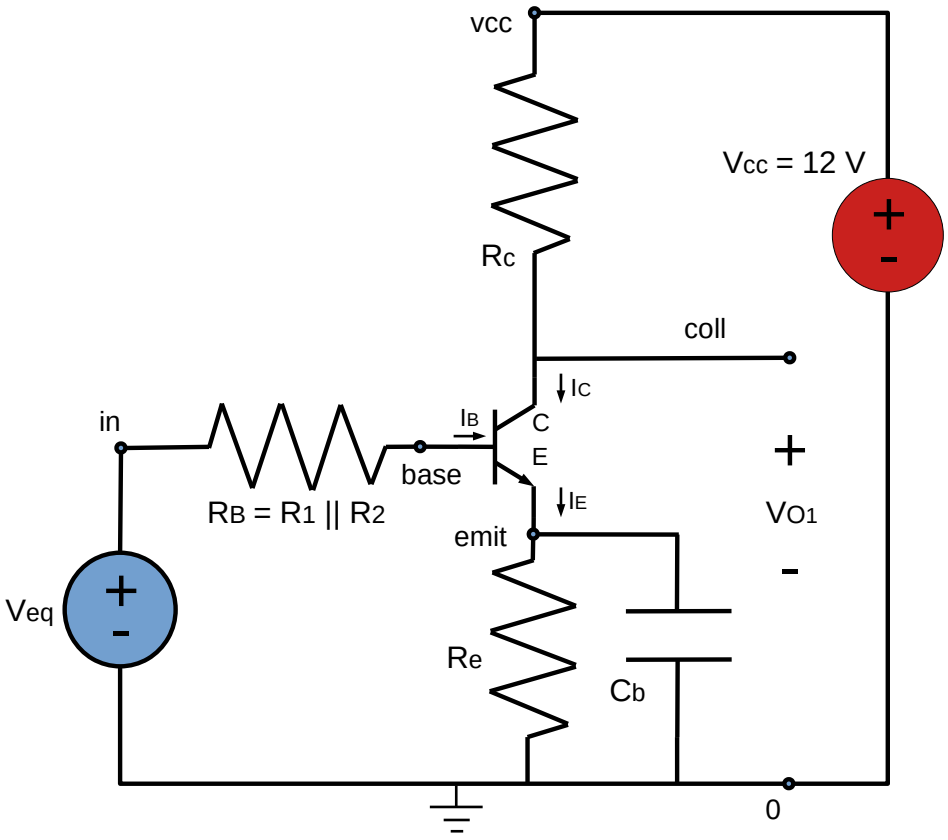


Figure 2: Gain Stage circuit.

While doing an Operating Point Analysis of the circuit shown in Figure 2, the capacitor becomes an open-circuit, thus only the resistor R_e is connected to nodes *emit* and *0*. As shown above, the equivalent resistance is given by $R_B = \frac{R_1 R_2}{R_1+R_2}$. Moreover, the equivalent voltage is given by $V_{eq} = \frac{R_2}{R_1+R_2} V_{CC}$. The current I_E that goes out of the transistor's emitter is given by

$$I_E = (1 + \beta_F) I_B \tag{1}$$

Where $\beta_F = 178.7$ for the NPN transistor model used in Ngspice and I_B is the current entering the transistor's base. Moreover, it is considered that $V_{ON} \approx 0.7$ V is the voltage for the diode model, being $V_{BE_{ON}} = V_{ON}$ for the base-emitter junction. By applying KVL, the following equation can be easily obtained: $I_B = \frac{V_{eq} - V_{ON}}{R_B + (1+\beta_F) R_E}$. Moreover, we have that $I_C = \beta_F I_B$, $V_{O_1} = V_{CC} - R_C I_C$ and $V_E = R_E I_E$. Finally, having calculated these quantities, in order to make that the theoretical model considered in this laboratory assingment is valid for the chosen values for the circuit's components, it is necessary to make sure that the following relation is satisfied:

$$V_{CE} = V_{O_1} - V_E > V_{BE_{ON}} \tag{2}$$

That is, it is necessary to make sure the transistor is working in a Forward Active Region. This relation is confirmed by the values shown in Table 2.

Name	Value [V]
V_{CE}	6.1117
$V_{BE_{ON}}$	0.7

Table 2: Voltages obtained in the Gain Stage.

Let us now consider the incremental analysis. The Gain Stage is, therefore, represented by the incremental circuit that learnt in class. This analysis is considered for medium frequencies, thefore the capacitor C_b can be replaced by a short-circuit. Thus, the gain in the Gain Stage is given by:

$$AV_1 = (R_B||R_S)R_C\frac{R_E - g_m r_\pi r_o}{(r_o + R_C + R_E)(R_B||R_S + r_\pi + R_E) + g_m R_E r_o r_\pi - R_E^2} \tag{3}$$

Where $g_m = \frac{I_c}{V_T}$, $r_\pi = \frac{\beta_F}{g_m}$ and $r_o \approx \frac{V_A}{I_c}$. The thermal voltage considered was $V_T = \frac{kT}{q}$ with $T = 300.15$K, $k = 1.38064852 \times 10^{-23}\ m^2 kgs^{-2}$ and $q = 1.60217662 \times 10^{-19}$. Moreover, the Early Voltage used in the NPN Ngspice model is $V_A = 69.7$ V.

This same equation can be simplified by considering $r_o = \infty$, from which $AV_1(r_o = \infty) = (R_B||R_S)R_C\frac{-g_m r_\pi}{R_B||R_S + r_\pi + R_E + g_m R_E r_\pi}$ is obtained. However, during the course of this assignment, it was verified that this approximation showed to produce worse reults, thus it wasn't considered. On ther other hand, it was considering a fairly reasonable approximation to have $R_E = 0$ in equation 3. The final results, shown in Figure 4 were, in fact, obtained by considering the average value of AV_1, obtained from equation 3 with R_E given in Table 1, and AV_1 with $R_E = 0$, because the results with the average value were much more similar to those obtained in Ngspice, rather than using only one of the two. This will be further discussed in Section 3.

Finally, the input and output impedances for the Gain Stage are given respectively by:

$$Z_{I1} = R_1||R_2||r_\pi = R_B||r_\pi = \frac{R_B r_\pi}{R_B + r_\pi} \tag{4}$$

$$Z_{O1} = R_C||r_o = \frac{R_C r_o}{R_c + r_o} \tag{5}$$

The impedances obtained are shown in Table 4 and will be discussed further beyond.

Now, let us consider the Output Stage circuit, which is shown below.

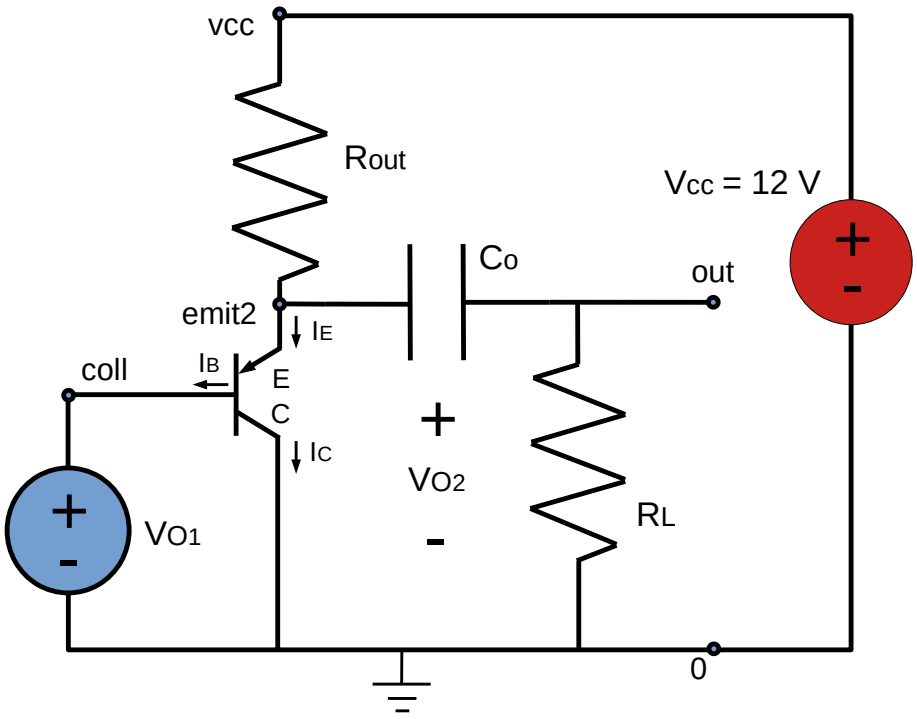


Figure 3: Output Stage circuit.

For the Operating Point analysis, however, the capacitor is considered an open-circuit. In the incremental analysis, by considering only medium frequencies, the capacitor can also be disregarded in the model. For these reasons, the output voltage V_{o_2} was drawn as the voltage drop between nodes *emit2* and *0*; however, in the Ngspice simulation, the output voltage will of course be considered in node *out*.

In the Output Stage, a PNP transistor is used. In this case, $\beta_F = 227.3$ and the Early Voltage $V_A = 37.2$ are the values used in Ngspice and therefore in the Octave script as well. Moreover, we have that $V_{EB_{ON}} = V_{ON} \approx 0.7$ V. For the OP analysis, firstly, we have that the input voltage is the output voltage from the Gain Stage, V_{O_1}. By applying KVL, the equation

$$I_E = \frac{V_{CC} - V_{EB_{ON}} - V_{O_1}}{R_{out}} \tag{6}$$

As we can see in Table 3, the current I_E is quite bigger that the one obtained in the Gain Stage. This aspect justifies the usage of the Output Stage circuit: as seen in Table 4, the output impedance from the Gain Stage, Z_{O_1}, is quite large, thus it could not be connected to the 8 Ω resistance in the load (the audio device). Now, because of the Output Stage, part of the current I_E will feed the load, which will help us at obtaining a smaller output impedance. Another thing to notice is that, as seen in Table 3, the voltage V_{CE}, which is now given by $V_{CE} = -V_{O_2} - R_E I_E$, has an absolute value of 12 V, as expected, because of V_{CC} and the fact that the capacitor isn't taken here into account. Therefore, this voltage is bigger than V_{ON} (given by this expression because of the currents defined in the PNP transistor), which guarrantees that we are still working in a Forward Active Region, as intended.

Name	Value
I_E (Gain Stage)	5.3802 mA
I_E (Output Stage)	93.0060 mA
$\|V_{CE}\|$	12.0 V
$V_{EB_{ON}}$	0.7 V

Table 3: Values of current I_E obtained for the Gain and Output Stages by theoretical analysis.

By incremental analysis, the gain and the input and output impedances of the Output Stage can be easily computed. They are given by the following equations:

$$AV_2 = \frac{g_m}{g_\pi + g_E + g_o + g_m} \tag{7}$$

$$Z_{I2} = \frac{g_\pi + g_E + g_o + g_m}{g_\pi(g_\pi + g_E + g_o)} \tag{8}$$

$$Z_{O2} = \frac{1}{g_\pi + g_E + g_o + g_m} \tag{9}$$

Where $g_m = \frac{I_C}{V_T}$, $g_o = \frac{I_C}{V_A}$, $g_\pi = \frac{g_m}{\beta_f}$ and $g_E = \frac{1}{R_{out}}$. For the Output Stage and the PNP transistor, the current I_C is given by $I_C = \frac{\beta_F}{1+\beta_F} I_E$ and the values of β_F and V_A are those used for the PNP model in Ngspice, as mentioned above. Taking the whole circuit (Gain Stage+Output Stage) into account, it is now necessary to obtain the gain AV and the output impedance Z_O. The input impedance of the whole circuit is given by $Z_I = Z_{I1}$. By studying the circuit in an incremental analysis, the following expressions are obtained:

$$AV = \frac{\frac{1}{r_{\pi 2}+Z_{O1}} + \frac{g_{m2} r_{\pi 2}}{r_{\pi 2}+Z_{O1}}}{\frac{1}{r_{\pi 2}+Z_{O1}} + \frac{1}{R_{E2}} + \frac{1}{r_{o2}} + \frac{g_{m2} r_{\pi 2}}{r_{\pi 2}+Z_{O1}}} AV_1 \tag{10}$$

$$Z_O = \frac{1}{g_{o2} + g_{m2}\frac{r_{\pi 2}}{r_{\pi 2}+Z_{O1}} + g_{e2} + \frac{1}{r_{\pi 2}+Z_{O1}}} \tag{11}$$

In the above expressions, the index 1 refers to values calculated for the Gain Stage and the index 2 corresponds to values determined for the Output Stage.

The values obtained for all the input and output impedances were the following:

Name	Value [Ω]
Z_{I1}	786.260649
Z_{O1}	928.710486
Z_{I2}	6007.575337
Z_{O2}	0.276371
Z_I	786.260649
Z_O	3.959082

Table 4: Values obtained for the impedances by theoretical analysis.

The values obtained for the gains were the following:

Name	Value
AV_1	-89.860235
AV_1 [dB]	39.071351
AV_2	0.989432
AV_2 [dB]	-0.092284
AV	-81.859383
AV [dB]	38.261369

Table 5: Values obtained for the gains by theoretical analysis.

The value obtained for the cut-off frequency was the following:

Name	Value [Hz]
Lower cut-off frequency	30.727761

Table 6: Value obtained for the cut-off frequency by theoretical analysis.

Finally, a plot with tha gain with respect to frequency is plotted below.

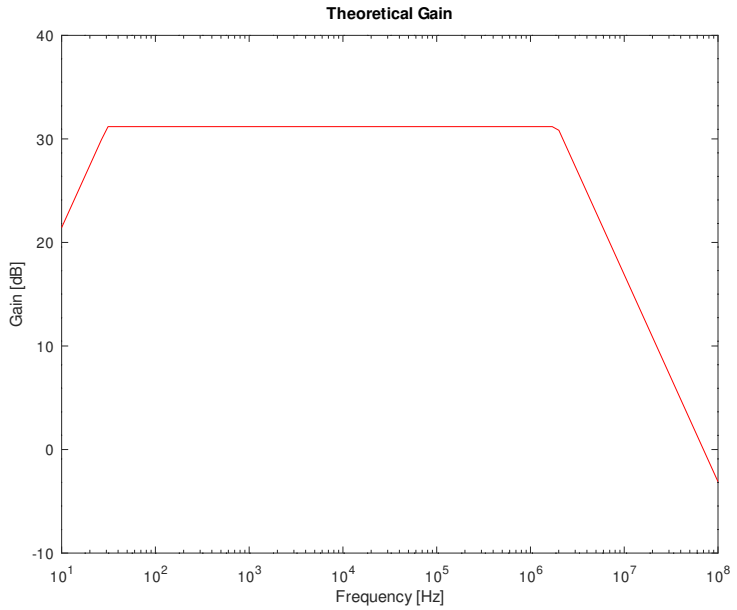


Figure 4: Plot of the gain with respect to frequency, as obtained by theoretical analysis.

3 Simulation Analysis

In order to simulate this circuit with Ngspice, real models of npn and pnp transistors where used. We realised that this models are very complex in reagards to the thheoretical models used previously. Because of this we expect there to be significant difference between the results.

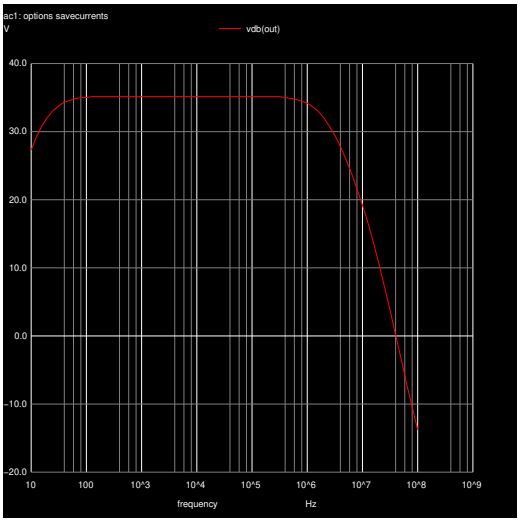
The simulation was done by taking the base script and tinkering with the values in order to improve the model. We strived to improve the bandwidth mainly since this was, observing the output graphs and value, the component that was lacking the most given that this was a audio amplifier and should worrk for a wide range of frequencies. Initially we started by determining the input and output impeadances os the system as a hole (gain stage + output stage). The output impeadance was simulated with V_{in} turned off and a voltage source with amplitude of 1 V in the output. The results obtained are the following in table 7.

Designation	Value [Ω]
in impeadance	8.618356e+02
out impeadance	8.556043e+00

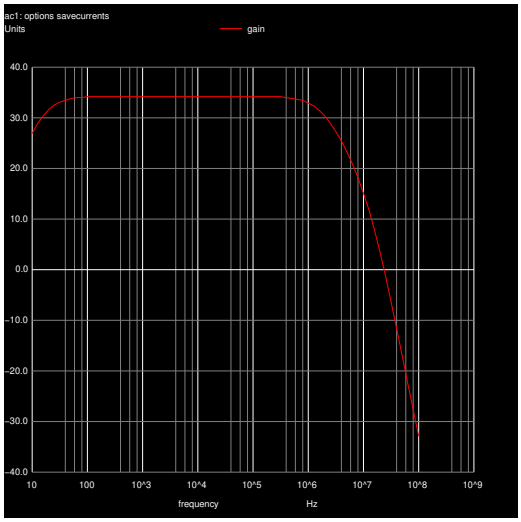
Table 7: Output and Input impeadances

As we wanted the input impeadance is high and the output is small. Although improvements where made to take the out impeadance as low as we could this value is, perhaps, still a bit high and if it was better maybe it would make a better amplifier.

We can now analise the graphics of the output signal and the gain.



(a) Output signal response to frequency



(b) Gain

We can also see in a transient analysis for f=1kHz, how is the output of the signal in regards of time, as presented in figure 6. It is observable that there are no losses of the original signal (still sinusoidal wave) The plot after the inicial seconds in order to represent the system without transitory interferences.

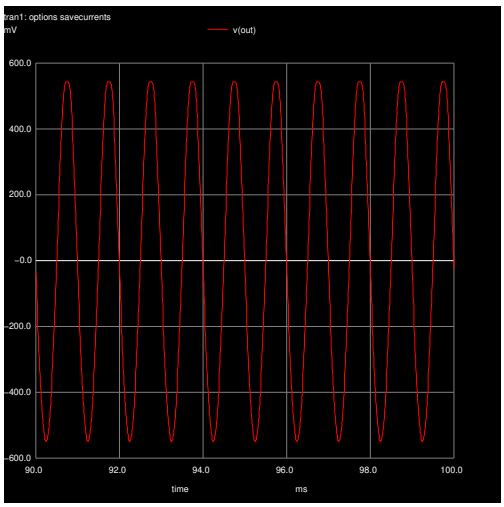


Figure 6: Output signal variance with time for f=1kHz

Analysing now the graphs obtained we are able to determine all the important information about the output. Looking initially at figure 5a, we start by obtaining the lower(lowfrequence) and higher(highfrequence) cutoff frequencies which are determined by taking the maximum output signal and seeing where this drops 3 dB. With this two values we subtract them and obtained bandwidth. Finaly looking now at figure 5b we obtain the maximum value of the gain. All the results are presented in table 8

Designation	Value [Hz and dB]
lowfrequence	1.991176e+01
highfrequence	1.928995e+06
bandwidth	1.928975e+06
gainfinal	6.394708e+01

Table 8: Lower frequency(Hz), high frequency(Hz), bandwidth(Hz) and gain(dB)

Finally, the total monetary cost and the merit M of the circuit used have been calculated and are shown below in Table 9. These were determined by using the results obtained from Ngspice. The cost is given by $cost = cost\ of\ resistors + cost\ of\ capacitor + cost\ of\ transistores$, in which each $1k\Omega$ in the resistances costs 1 monetary unit (MU), as well as each $1\mu F$ in the capacitance; the cost of each transistor is 0.1 MU. On the other hand, the merit M is given by

$$M = \frac{voltageGain \times bandwidth}{cost \times lowerCutoffFreq} \tag{12}$$

Designation	Value
cost	3.881450e+03
merit	1.596040e+03

Table 9: Cost and merit obtained for this circuit.

4 Conclusion

In this laboratory assignment, the intended objective has been achieved. The AC/DC converter has been simulated accordingly by using Ngspice and a rather precise output voltage as close to 12V as possible has been obtained. Moreover, a suitable theoretical model was utilized in order to predict the output of the simulated circuit, having obtained a voltage quite close to the one obtained in Ngspice. However, the value obtained in this analysis was slightly further away from the desired 12V DC output voltage. The differences between the results obtained in both analysis may be due to several factors. The theoretical diode model considered is different from the much more complex diode model used by Ngspice. Moreover, the theoretical analysis is subjected to certain approximations and a nonlinear equation must be solved.

A ripple of approximately 10^{-4}V was obtained for both cases. A smaller value could have been obtained by using bigger values for R_1 and C, for example. However, that would also lead to a larger monetary cost. By taking into account the different aspects at hand, rather precise results and an acceptable merit M have been obtained.