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Dublin M. Nichols for the degree of Doctor of Philosophy in Physics presented on
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Abstract

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Interactions between surface acoustic waves and charge carriers in quantum
materials

by

Dublin M. Nichols

A DISSERTATION

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Head of the Department of Physics

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TABLE OF CONTENTS

	<u>Page</u>
1 Introduction	1
1.1 Why two-dimensional materials?	2
1.2 Background and Motivation	3
1.2.1 Using surface acoustic waves to probe and control quantum phenomena	3
1.2.2 Topologically-protected charge pumps	6
2 Theory	9
2.1 The electronic properties of graphene	9
2.1.1 Graphene's unique band structure	9
2.1.2 Density of states in graphene	13
2.1.3 Thermally excited charge carriers in graphene at finite temperature .	14
2.2 Surface acoustic waves and acoustoelectric charge pumping	17
2.2.1 Elastic waves in non-piezoelectric materials	19
2.2.2 Waves in bulk piezoelectric materials	21
2.2.3 SAWs propagating in 2D materials	28
2.2.4 The 2D acoustoelectric charge pumping effect	30
2.3 Surface acoustic wave device design rules	35
3 Methods	39
3.1 Fabricating 2D devices	39
3.1.1 Exfoliation of 2D crystals	39
3.1.2 Stacking 2D materials to create heterostructure devices	43
3.2 Contacts to 2D materials	50
3.2.1 Photolithography	50
3.3 Cleaning electrodes with contact-mode AFM	54
3.3.1 Electron-beam lithography	56
3.4 Interdigitated transducers	56
4 Acoustoelectric charge pumping in ultra-clean graphene using surface acoustic waves	60
4.1 Abstract	60
4.2 Introduction	60
4.3 Background	60
4.4 Experiment design	60

TABLE OF CONTENTS (Continued)

	<u>Page</u>
4.5 Results	60
4.6 Discussion	60
4.7 Conclusion	60
4.8 Supplementary Material	60
4.9 Nonlinear acoustoelectric effect in graphene	60
 5 Flip-chip design for coupling surface acoustic waves to quantum materials	61
5.1 Introduction	61
5.2 Measuring flip-chip spacing using interference spectroscopy	62
5.3 Flip-chips with no spacers	65
5.3.1 Smallest achievable air gap	66
5.4 Flip-chip capacitor with deep RIE-etched Si spacers	67
5.5 Flip-chip air gap measurement with capacitance	73
5.6 Conclusions	74
 6 Conclusion	79
 Bibliography	80
 Appendices	88
A Limitations of quantized charge pumps based on tunneling	89
B Recipes	90
C Additional flip-chip tests	96
D Transferred contacts for high-quality contact to 2D semiconductors	98
E Gate-tunable photoluminescence in h-BN-encapsulated MoS ₂	99

LIST OF FIGURES

Figure	Page
2.1 (a) A plot of graphene's dispersion relation given by Eq. 2.1. (b) Near the Dirac points, the energy of electronic states in graphene is approximately linear with respect to momentum. (c) The momentum-space lattice of graphene, with Dirac points labelled.	10
2.2 Filling of electronic states in graphene at zero temperature for (a) $E_F > 0$, (b) $E_F = 0$, and (c) $E_F < 0$. Filled electronic states are indicated in blue. Unfilled electronic states in the valence band (holes) are indicated in red.	12
2.3 (a) Graphene band diagram with the Fermi energy indicated by E_F . (b) The $k_x - k_y$ plane at $E = E_F$. The intersection of the Dirac cone with this plane forms a circle with radius $ k_F $	13
2.4 A plot of $f(E)D(E)$ with respect to energy E for graphene at elevated temperature (left) next to graphene's dispersion relation (right). The colors represent free electrons (blue) and free holes (red). The color intensity represents the magnitude of $f(E)$ (for electrons) and $(1 - f(E))$ (for holes)..	16
2.5 A one-dimensional illustration of an element which deforms from length dx to $du + dx$	20
2.6 A surface acoustic wave travelling in a bulk piezoelectric material. The SAW amplitude $ \phi_{SAW} $ is well-known to decay approximately exponentially into the surface, with most of its energy contained within a depth $1/k$ [1].	21
2.7 Eq. 2.33 (left axis) and Eq. 2.32 (right axis) plotted as dimensionless quantities against the ratio ω_c/ω	27
2.8 (a) A SAW propagating in a bulk material with conductivity σ and permittivity ϵ . (b) A SAW propagating in a piezoelectric material with permittivity ϵ that has been capped by a conductive material of thickness d and sheet conductivity $\sigma_{2D} = \sigma d$	29
2.9 E_p (left axis) and Δn (right axis) plotted for the case of (a) $\sigma_{2D} \gg \sigma_M$ (very high sheet conductivity), (b) $\sigma_{2D} = \sigma_M$, and (c) $\sigma_{2D} \ll \sigma_M$ (very low sheet conductivity).	33
3.1	41

LIST OF FIGURES (Continued)

Figure	Page
3.2 (a) AFM scan and (b) optical image of exfoliated graphene on SiO ₂ . The AFM scan region is indicated by a gray dotted box. Scale bar = 10 μm.	42
3.3 The viscoelastic stamp fabrication process.	45
3.4 The hot-pickup process for constructing 2D heterostructures. (a) First, the polymer stamp is lowered close to a 2D flake. Inset: a ≈ 30 nm h-BN flake on SiO ₂ . (b) The z-stage is slowly lowered and/or the stage is heated by 5 °C at a time to slowly expand the polymer front over the 2D flake. Inset: a h-BN flake during the pickup process. (c) The z-stage is slowly raised, peeling the 2D flake from the substrate. Inset: A 2D flake which has been peeled from the substrate, barely visible on a polymer stamp. (d)-(e) Steps (a)-(c) are repeated, using the previous flake to pick up the next flake. (f) The completed heterostructure is placed down on the final substrate. The stage is heated to 170 °C to melt the polymer. Finally, the polymer is dissolved in a solvent.	49
3.5 h-BN flake transferred onto LiNbO ₃ before (top) and after (bottom) photolithography process to deposit metal electrodes on top of the h-BN. The h-BN lifted off with the deposited metal. Scale bar = 40 μm.	52
3.6 AFM trace (top) and schematic (bottom) for single-layer (left) and bilayer (right) liftoff processes of Cr on SiO ₂	53
3.7 Cross-sectional SEM image showing bilayer resist process with undercut length ≈ 0.4 μm. Scale bar = 3 μm	54
3.8 An optical microscope image of Pd electrodes on LiNbO ₃ after AFM cleaning at a force of 150 N and a speed of 150 μm/s. Scale bar = 40 μm.	55
3.9	57
3.10	58
3.11	59

LIST OF FIGURES (Continued)

Figure	Page
5.1 Flip-chip design from [2]. (a) The upper gate-chip is printed on quartz to allow alignment with the lower GaAs chip. The lower chip's gates are attached by micro soldering to preserve the pristine GaAs surface's ultrahigh electron mobility. (b) Side view of the stacked chips. The gate (yellow) and GaAs are separated by 100 nm using patterned Ti posts.	63
5.2 The interferometer setup used to measure the reflectance of a sample. Incident wavelength is scanned using a Labview-controlled monochromator and plotted against measured reflected power. The colors indicate incident light (red) and reflected light (blue).	63
5.3 Corrected measured reflectance of a Si-PMMA-quartz stack compared to the Filmetrics reflectance calculation with 1045 nm-thick PMMA.	64
5.4 From [3]	66
5.5 (a) A flip-chip with no spacers made from quartz and Si. The three circles indicate the spots at which I directed the laser for interference spectroscopy air gap measurement. (b) The reflectance spectrum from the central spot compared to the Filmetrics model with a $3.2\mu\text{m}$ air gap.	68
5.6 View through the microscope camera during initial alignment of the flip-chip capacitor (the top and bottom chips are still far from each other, so no Newton's rings are visible).	70
5.7 (a) Two-tier etch process for defining the center gap and post height of the flip-chip. The denoted measurements are estimated from known Cr deposition rates and known Cr and Si etch rates (see Appendix B.4). (b) The completed top and bottom sides of the flip-chip capacitor, before assembly.	71
5.8	72
5.9 (a) schematic of the capacitance measurement. (b) Dependence of central air gap modulation with respect to location of applied mounting pressure. The edge force was applied onto the quartz chip, above the etched spacers closest to the edge of the Si chip. The central force was applied directly above the capacitor pads.	75
5.10 (a) Schematic of the completed flip-chip capacitor. (b) Optical image of the completed flip-chip capacitor. Wires are seen soldered to the silver paint, making electrical contact to the top and bottom chips.	76

LIST OF FIGURES (Continued)

<u>Figure</u>		<u>Page</u>
5.11	Geometry of the bent quartz chip with a centrally-applied force that short-circuits the top and bottom capacitor pads.	77

LIST OF APPENDIX FIGURES

<u>Figure</u>	<u>Page</u>
B.1 A force curve for a dirty AFM tip. The colors indicate engaging (red) and retracting (blue) the AFM tip.	92
C.1 (a) A flip-chip with sandwiched quartz and Si surfaces separated by a grid of 50 μm -wide squares spaced by 350 μm . (b) A flip-chip where the quartz and silicon are separated by $\approx 1 \mu\text{m}$ micron of spin-coated PMMA. (c) The grid of photoresist squares under quartz during alignment. (d) A single 50 μm -wide square.	97
E.1	100
E.2	101
E.3	102
E.4	103

Chapter 1: Introduction

Interest in the transformative potential of the second quantum revolution has reached the mainstream. Not a week goes by without a hundred popular science articles promising that some new material, with some “weird quantum property”, will revolutionize your computer, car, refrigerator, and more. Central to these claims are quantum materials. In contrast to conventional materials such as silicon, which can be accurately described using semiclassical physics and basic quantum mechanics, quantum materials force us to move beyond the theories established in the early 20th century (during the first quantum revolution). These initial theories were immensely impactful — they led to the invention of transistors and formed the foundation of our computer-centric world. Quantum materials, however, boast strongly-interacting electrons, exhibit quantum interference effects, provide new quantum degrees of freedom, and manifest topological states of matter, all of which challenge our understanding of physics. But, can these materials revolutionize anything, or are they just curiosities that will never leave the lab?

When I first heard the phrase “quantum materials”, I thought it was a bit ridiculous. Aren’t all material properties essentially a result of quantum mechanics? I was convinced to the contrary by an editorial in *Nature Physics*, which writes

“Of course, on a trivial level all materials exist thanks to the laws of quantum mechanics, and there are cynics who will privately wonder if the description isn’t too broad and, well, catchy for its own good...there are good reasons to embrace quantum materials. In essence, they provide a common thread linking disparate communities

of researchers working on a variety of problems at the frontiers of physics, materials science and engineering.” [4]

The phrase “quantum materials” isn’t meant to be precise. It links together researchers who are developing quantum computers, to those exploring topological states of matter in ultracold atoms, to researchers like me who seek to harness the properties of 2D materials to explore new and exciting physics and promising applications. The development of the transistor never would have been possible without first developing a deep understanding of the basic physics of quantum mechanics. Now, as we stand on the precipice of the second quantum revolution, we must confront these challenges directly, and strive to deepen our understanding of the physics of quantum materials. Though we work on distinct challenges, we can unite under the moniker “quantum materials”.

1.1 Why two-dimensional materials?

Few quantum materials have captivated researchers’ interest as profoundly as two-dimensional (2D) materials. Two decades have passed since Novoselov et al. published their electronic measurements on atomically-thin carbon films known as graphene, which would later win them the Nobel Prize [5]. Since then, the family of 2D materials has expanded to include a plethora of 2D semiconductors and magnets. The greatest strength of 2D materials lies in their tunability. When electrons are confined to two dimensions, they are incredibly sensitive to their environment. By stacking atomically-thin 2D materials into heterostructures, we can harness their tunability for next-generation electronics. For example, 2D semiconductor heterostructures are of prime interest to overcome the fundamental limits of

silicon-based transistors, enhancing transistor density while simultaneously paving the way for more energy-efficient computing [6, 7]. 2D ferromagnets challenge established theories of magnetism, provide unprecedented electronic control over magnetism, and enable applications in sensing and data storage [8, 9]. The tunability of 2D materials allows us to tune their electronic properties and control these quantum phenomena to explore both exciting new physics and promising applications.

1.2 Background and Motivation

1.2.1 Using surface acoustic waves to probe and control quantum phenomena

A surface acoustic wave (SAW) is an elastic wave that propagates along the surface of a material, with its energy confined to a depth of around one wavelength below the surface [10]. When a SAW propagates in a piezoelectric substrate (such as LiNbO_3), it mechanically stresses the piezoelectric, generating electric fields. These travelling spatially- and temporally-periodic electric fields can interact with quantum materials, enabling novel probes into quantum phenomena which are not accessible using conventional transport techniques. For example, SAWs were recently used to demonstrate that current-induced modifications of bubble and stripe phases in 2D electron systems (2DES) are a local phenomenon [11]. In contrast to prior transport studies which indirectly probed the voltage drop on the edges of the 2DES, the authors used SAWs to probe the entire sample at once, gaining new understanding into the effects of external current on highly-ordered electron phases. Another work

used a combination of SAWs, microwave excitation, and optical detection to study quantum Hall stripes [12]. By employing SAWs with a wavelength of 60 nm, the authors were able to probe commensurability effects between the SAW superlattice and quantum Hall stripes. A plethora of earlier SAW-based studies provided new insight into the quantum Hall and fractional quantum Hall effect [13, 14, 15, 12, 16] and Wigner crystallization [17]. These works highlight the incredible strength of SAWs for probing phenomena in quantum systems. Building on these successes, researchers have begun to explore the potential of SAWs in the rapidly evolving field of 2D materials.

In 2018, interest in engineered 2D superlattices exploded with the discovery of unconventional superconductivity in twisted bilayer graphene [18]. The birth of the field of “twistronics” added a new knob to turn in the already massive parameter space available for creating bespoke 2D devices. By tuning the twist angle between two sheets of graphene (and thus the periodicity of the moiré superlattice), bilayer graphene can not only exhibit superconductivity, but also correlation-induced insulating states, magnetism, quantized anomalous Hall states, and many more [19]. In 2D semiconductors, which exhibit exciton dynamics that are of great interest for next-generation electronics, tuning the moiré superlattice provides even more control over the spin and valley degrees of freedom [20]. While graphene has a lattice periodicity on the order of 0.15 nm, the moiré superlattices in twisted devices have much longer periods (tens to hundreds of nm) which are on the order of nominal SAW wavelengths. This congruence opens up the possibility of exploring commensurability effects between moiré superlattices and SAW potentials. Contactless probing using SAWs could also circumvent the challenges of making quality electrical contacts to 2D semiconductors for transport measurements [21]. Hence, SAWs are an ideal tool for contactlessly probing

and controlling quantum phenomena in 2D materials. This potential has not gone unnoticed, as evidenced by recent works that have already employed SAWs to great effect, opening new avenues in the probing and manipulation of 2D quantum phenomena.

One phenomenon of interest is interlayer excitons in 2D semiconductor heterostructures. Interlayer excitons are composed of electrons and holes located in different layers in stacks of 2D semiconductors. Harnessing these excitons is exciting for nanophotonics and quantum information applications [22]; however, controlling them is difficult because they are charge-neutral and exhibit no net force under a uniform electric field. Prior works utilized diffusion to transport interlayer excitons, but the transport lengths achievable using diffusion are limited [23, 24]. In a recent work, the authors used SAWs to transport interlayer excitons over incredible distances in bilayer WSe₂ [25]. Given that SAWs transport both electrons and holes in the same direction (See Sec. ****), they can transport neutral excitons much further than the diffusion length. This approach also circumvents the challenges previously identified by other researchers when using local graphene gates [26]. In another work, SAWs were used as a contactless probe of measuring wave-vector dependent conductivity in ultra-clean graphene, establishing the viability of SAW resonant cavities as a probe for quantum transport phenomena in 2D materials [27]. However, these studies have only scratched the surface of what is possible by interfacing SAWs with quantum materials. Many other SAW-induced phenomena in 2D materials have been theoretically predicted, but not yet achieved experimentally [28]. Therefore, it is imperative to further develop the methods of interfacing SAWs with 2D materials, and to further our understanding of interactions between SAWs and phenomena in quantum materials. One such SAW-enabled phenomenon that has not yet been realized experimentally is topologically-protected quantized charge transport.

1.2.2 Topologically-protected charge pumps

A quantized charge pump is a device that transports electrons in precise, quantized units. Unlike conventional DC transport, where electrons flow stochastically in response to an applied voltage bias, quantized charge pumps operate at a constant frequency f , transporting a unit of charge Ne per cycle (where N is an integer), resulting in a DC current of magnitude Nef . Such devices are of great interest to metrologists, where practical sources of highly-quantized current could help define a better standard of current [29]. Many designs for quantized charge pumps have been demonstrated, with the best pumps today being based on controlling tunneling to- and from quantum dots. However, quantized charge pumps based on tunneling face fundamental limits to their accuracy, as tunneling is an inherently random process. Topologically-protected quantum charge pumps could overcome these fundamental limits.

In a topologically-protected quantum charge, the Hamiltonian of the system is adiabatically modulated by a potential periodic in space and time. During one cycle of the periodic potential, the state of the system traverses a closed path in momentum space. From the adiabatic theorem, if the system starts in an eigenstate of the Hamiltonian, and undergoes an adiabatic transformation, it must end in an eigenstate of the Hamiltonian. However, though the state begins and ends in an identical eigenstate, during the cycle it acquires a geometric phase. This geometric phase defines a *topological invariant*, or a quantity that depends only on the topology of the energy bands of the system, and is thus invariant to small perturbations from the environment [30]. Such a pump is known as the Thouless pump, named after D.J. Thouless, who was the first to propose this phenomenon theoretically.

cally [31]. Thouless found that, in a 1D electronic system under the influence of a spatially- and temporally-periodic potential, the unit of charge transported per cycle is topologically invariant. The Thouless pump is of great interest to the fields of metrology [32], where topologically protected charge pumping could enable higher-accuracy quantized charge pumps, and quantum computing [33], where a Thouless pump could generate and control the flow of spin-entangled quantum states with minimal decoherence. A charge Thouless pump has not yet been realized experimentally; however, it has been proposed that coupling carbon nanotubes to SAWs is an ideal system to realize topologically-protected charge pumping.

Talyanskii et al. proposed that a carbon nanotube coupled to a surface acoustic wave is an ideal system to create a charge Thouless pump [34]. Though charge pumping in carbon nanotubes using surface acoustic waves has been demonstrated previously [35], the Thouless pumping regime has not yet been achieved. This is likely because, to achieve the Thouless pumping state, one needs to fit many spatial periods of the SAW inside an ultraclean nanotube. This is challenging because insulating surfaces, including piezoelectric insulators (on which SAWs are generated), induce considerable electrostatic disorder within electronic systems on their surface. Therefore, surface nanotubes are too disordered to use in a Thouless pump. Thus, we must turn to two demonstrated methods of creating ultraclean nanotubes: Either encapsulate the nanotube in two-dimensional hexagonal boron nitride (h-BN) [36], or suspend the nanotube above the substrate [37]. Realizing a charge Thouless pump using a carbon nanotube was the primary motivation for the research presented in this dissertation. Therefore, I will next delve into these two approaches towards the Thouless pump and utilize them to outline this dissertation.

On its face, marrying a surface acoustic wave and suspended carbon nanotube does not

seem too challenging. It is possible to create 3 μm -long ultraclean suspended nanotubes [37], and 60 nm SAWs have been coupled to quantum materials before [12]. However, growing carbon nanotubes and generating SAWs have competing fabrication requirements. To combine the two, we would need to fabricate the two chips separately, and bring them into extremely close contact to couple the SAW to the nanotube. A technique called “flip-chip construction” has emerged in recent years, in which one chip is “flipped” onto the other. In Chapter 5, I present a method of flip-chip construction that allows the air gap between the two chips to be precisely measured, which could be used to couple SAWs to a suspended carbon nanotube. I discovered that, admittedly, this does present a significant challenge... how about encapsulating a carbon nanotube in h-BN?

In Ref. [36], they encapsulate a nanotube in h-BN using a similar dry transfer technique to the one that I outline in Sec. 3.1.2. In Ch. 4, I encapsulate graphene in h-BN and transfer it onto LiNbO_3 , then generate SAWs to pump charge through the graphene. To create the Thouless pump, a carbon nanotube could similarly be encapsulated in h-BN and transferred onto a LiNbO_3 . Then, one-dimensional contacts (as in Ref. [36]) could be made to the nanotube. One concern for this process is residues contaminating the nanotube during the transfer process. To clean the encapsulated nanotube, AFM cleaning (which I describe in Sec. 3.3) could be used to “squeegee” out any contaminants stuck between the h-BN, as in Refs. [38, 39].

Chapter 2: Theory

2.1 The electronic properties of graphene

In this section, I delve into the linear band structure of graphene and derive its density of states. Using the density of states, I calculate the thermally excited electron and hole densities in graphene. We use this calculation in Ch. 4 to compare the carrier density in our graphene samples with the lowest achievable carrier density at room temperature.

2.1.1 Graphene's unique band structure

Graphene consists of a single layer of carbon atoms in a hexagonal lattice. The band structure of graphene is well-described by a tight binding model, where only hopping energy between nearest neighbor atoms is considered [40]. From the tight binding model, the dispersion relation of graphene is

$$E(k_x, k_y) = \pm t \left(3 + 2\cos(\sqrt{3}k_x a) + 4\cos\left(\frac{3}{2}k_y a\right)\cos\left(\frac{\sqrt{3}}{2}k_x a\right) \right)^{1/2}, \quad (2.1)$$

where $k = (k_x, k_y)$ is the momentum vector of electrons in the graphene, $t = 2.8 \text{ eV}$ is the nearest-neighbor hopping energy, and $a = 1.42 \text{ \AA}$ is the distance between the two nearest neighbor atoms. Figure 2.1 (a) shows a plot of the band structure given by Eq. 2.1.

In charge-neutral graphene, the Fermi energy E_F (the energy of the highest filled state

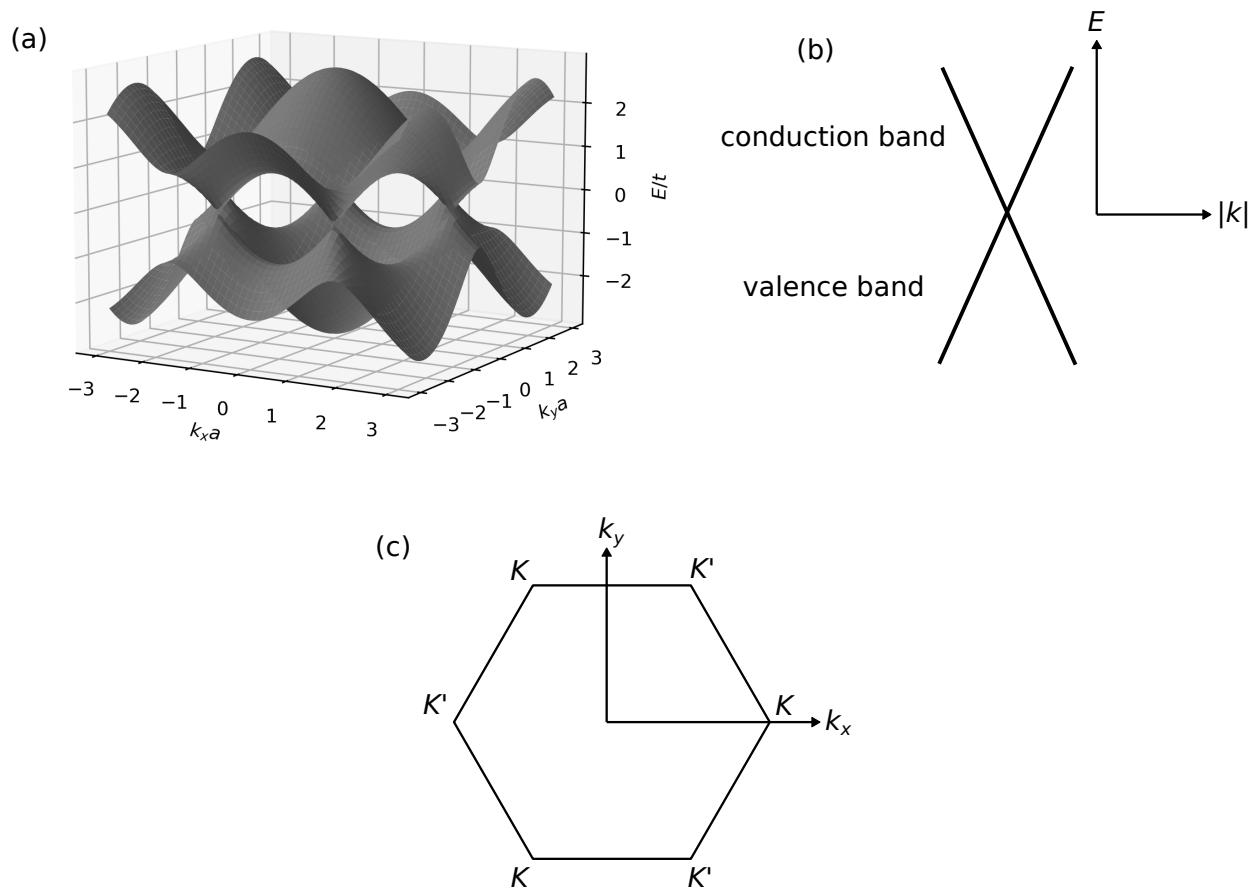


Figure 2.1: (a) A plot of graphene's dispersion relation given by Eq. 2.1. (b) Near the Dirac points, the energy of electronic states in graphene is approximately linear with respect to momentum. (c) The momentum-space lattice of graphene, with Dirac points labelled.

at zero temperature) intersects the bands at symmetry points called the K and K' points, also known as the Dirac points (Figure 2.1 (c)). Near the Dirac points, graphene's dispersion relation is linear, and can be approximated as

$$E(k) \approx \pm \hbar v_f |k|, \quad (2.2)$$

where \hbar is the reduced Planck's constant and $v_f = 3ta/2 \approx 10^6$ m/s is the Fermi velocity. Figure 2.1 (b) offers a magnified view of graphene's band structure near a Dirac point, showing its characteristic shape commonly referred to as the "Dirac cone". In conventional semiconductors and metals, we expect a parabolic energy-momentum relation of $E(k) = k^2/2m$, which gives a velocity of $v = \sqrt{2E/m}$. However, in the case of graphene, electrons near a Dirac point move at a velocity v_F which is independent of both energy and momentum, leading to many unique electronic properties [41]. For example, electrons and holes in graphene behave almost identically, in contrast to other materials [42, 41]. In the context of this dissertation, electron-hole symmetry is the most pertinent consequence of graphene's unique band structure.

In graphene, we can tune the Fermi energy using an electric field, which in turn tunes the charge carrier density.¹ Figure 2.2 illustrates graphene's band structure at zero temperature for $E_F < 0$, $E_F = 0$, and $E_F > 0$. When E_F lies above the Dirac point ($E_F > 0$), states in the conduction band are filled with electrons up to E_F (Fig. 2.2 (a)). Conversely, when $E_F < 0$, the valence band is depleted of electrons down to E_F (Fig. 2.2 (c)). These vacant electronic states, referred to as "holes", act as positively-charged quasiparticles. Similar to

¹The term "charge carrier" is commonly used to refer to both electrons and holes, and I use it in this context throughout this dissertation.

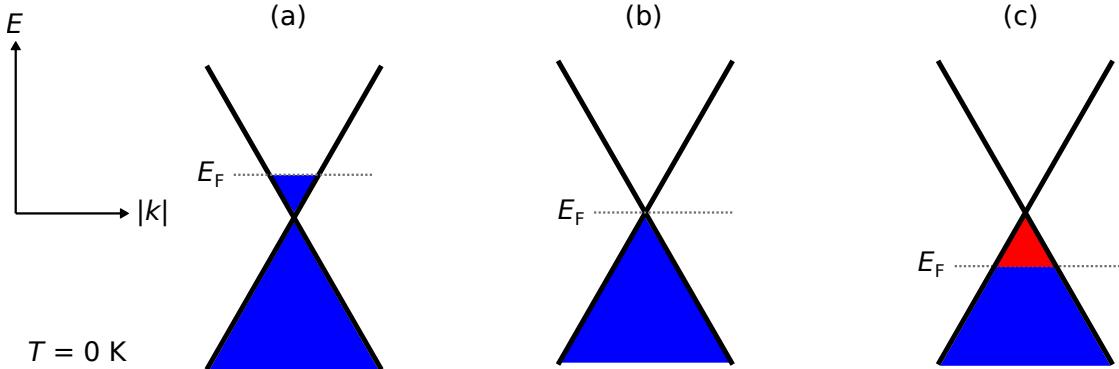


Figure 2.2: Filling of electronic states in graphene at zero temperature for (a) $E_F > 0$, (b) $E_F = 0$, and (c) $E_F < 0$. Filled electronic states are indicated in blue. Unfilled electronic states in the valence band (holes) are indicated in red.

electrons in the conduction band, holes in the valence band are free from the graphene lattice and can move in response to an electric field. In the case of charge neutral graphene ($E_F = 0$) at zero temperature, the conduction band is entirely empty, and the valence band is completely occupied, so no charge carriers should be present to conduct current (Fig. 2.2 (b)). However, in real graphene samples, charge carriers can still be present when $E_F = 0$, leading to finite conductivity when E_F is tuned to the charge neutrality point.

Extrinsic sources of charge, referred to as electrostatic disorder, can be present in real graphene samples. For instance, substrates like SiO_2 contain charge traps which induce spatially-varying charge carrier concentrations in graphene [43]. This substrate-induced disorder can be minimized by encapsulating graphene in hexagonal boron nitride (h-BN) [44]. However, even the most pristine encapsulated graphene samples exhibit some DC conductivity at the charge neutrality point [45] due to thermally-excited electrons and holes. To quantify the densities of these thermally excited electrons and holes, I will proceed to derive the density of states in graphene.

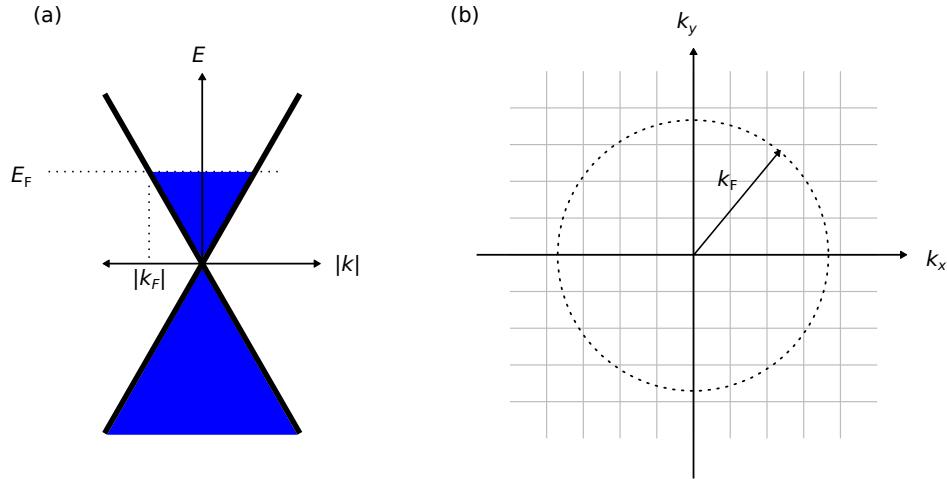


Figure 2.3: (a) Graphene band diagram with the Fermi energy indicated by E_F . (b) The k_x - k_y plane at $E = E_F$. The intersection of the Dirac cone with this plane forms a circle with radius $|k_F|$.

2.1.2 Density of states in graphene

The density of states helps us understand how many states are available for electrons to occupy at a certain energy level. Consider a sheet of graphene at zero temperature in which we have tuned the Fermi energy E_F to lie above the Dirac point, filling the states in the conduction band with electrons to an energy E_F . Figure 2.3 (b) illustrates the k -plane slice at $E = E_F$, where the momentum at which E_F intersects the Dirac cone is defined as k_F . To find the density of states, we can count the number of states that lie inside this circle (states with momentum $0 < k < k_F$), and divide this number by the area of a single state in momentum space.

The graphene lattice is periodic, so the spatial part of the electron wavefunction must also be periodic. If the graphene real space periodicity is L (or, the unit cell has area L^2 in real space), then the allowable momenta are integer multiples of $(k_x, k_y) = (2\pi/L, 2\pi/L)$.

Thus, a single occupied state takes up an area of $(2\pi/L)^2$ in momentum space. The total number of states with $k < k_F$ is given by the area of our circle of radius k_F divided by the area of a single state,

$$N = \frac{\pi k_F^2}{(2\pi/L)^2} = \frac{k_F^2 L^2}{4\pi}. \quad (2.3)$$

Then, the density of states is given by

$$D(E_F) = \frac{4}{L^2} \frac{dN}{dk_F} = 4 \frac{(2k_F)}{4\pi} = \frac{2|E_F|}{\pi \hbar^2 v_F^2}, \quad (2.4)$$

where the factor of 4 originates from graphene's four-fold degeneracy of two valleys (K and K') and two spins (spin up and spin down), and the absolute value ensures that $D(E)$ is a positive quantity. Equation 2.4 elucidates why graphene is a semimetal — though graphene has no band gap, the density of states is zero at the Fermi energy in charge-neutral graphene. However, thermal energy can excite charge carriers to occupy states that are not at the Fermi energy.

2.1.3 Thermally excited charge carriers in graphene at finite temperature

At finite temperatures, electrons will be thermally excited into the conduction band, leaving holes in the valence band. These thermally excited electrons and holes can contribute to conduction, and limit the lowest achievable carrier density (and lowest achievable conductance) in charge-neutral graphene at finite temperature. Figure 2.4 illustrates the thermally-excited electron and hole populations near the Fermi energy. The thermally excited electron and

hole densities n and p are given by

$$n = \int_0^\infty f(E)D(E)dE, \quad (2.5)$$

$$p = \int_{-\infty}^0 (1 - f(E))D(E)dE, \quad (2.6)$$

where $f(E)$ is the Fermi occupation function, which takes the form

$$f(E) = \frac{1}{1 + e^{(E/k_B T)}}, \quad (2.7)$$

where k_B is Boltzmann's constant and T is temperature. I take $E_F = 0$ to reflect charge neutral graphene.

Equations 2.5 and 2.6 can be solved analytically as follows:

$$\begin{aligned} n &= \int_0^\infty f(E)D(E)dE = \int_0^\infty \frac{1}{1 + e^{(E/k_B T)}} \frac{2E}{\pi \hbar^2 v_F^2} dE \\ &= \frac{2(k_B T)^2}{\pi \hbar^2 v_F^2} \int_0^\infty \frac{x}{1 + e^x} dx \\ &= \frac{2(k_B T)^2 \pi^2}{\pi \hbar^2 v_F^2} \frac{1}{12}, \end{aligned} \quad (2.8)$$

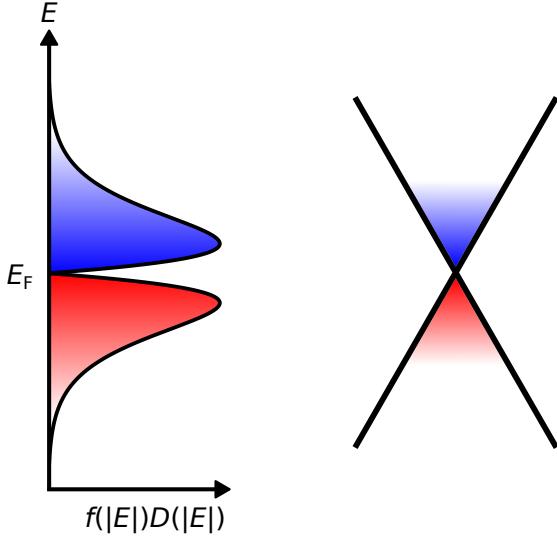


Figure 2.4: A plot of $f(|E|)D(|E|)$ with respect to energy E for graphene at elevated temperature (left) next to graphene's dispersion relation (right). The colors represent free electrons (blue) and free holes (red). The color intensity represents the magnitude of $f(E)$ (for electrons) and $(1 - f(E))$ (for holes).

$$\begin{aligned}
 p &= \int_{-\infty}^0 (1 - f(E))D(E)dE = \int_{-\infty}^0 \left(1 - \frac{1}{1 + e^{(E/k_B T)}}\right) \frac{-2E}{\pi \hbar^2 v_F^2} dE \\
 &= -\frac{2(k_B T)^2}{\pi \hbar^2 v_F^2} \int_{-\infty}^0 \left(x - \frac{x}{1 + e^x}\right) dx \\
 &= \frac{2(k_B T)^2 \pi^2}{\pi \hbar^2 v_F^2 12},
 \end{aligned} \tag{2.9}$$

where I use the substitution $x = E/(k_B T)$ to evaluate the integral. Both n and p yield identical expressions, which is consistent with the symmetry of graphene's band structure above and below $E = 0$ near the Dirac point. From Eqs. 2.8 and 2.9, I calculate the minimum achievable carrier densities at $T = 300$ K to be $n = p = 0.08 \times 10^{12} \text{ cm}^{-2}$. Therefore, the total

free carrier density in graphene at $T = 300\text{ K}$ is $0.16 \times 10^{12}\text{ cm}^{-2}$. This result is used in Ch. 4 to quantify the minimum carrier density achievable in our graphene sample, and is integral to understanding the behavior of our graphene device at the charge neutrality point.

Electrons and holes have equal and opposite charge, and thus move in opposite directions under a DC electric field (for example, when an external voltage bias is applied). Whether graphene is populated by electrons or holes, conventional current will flow in the same direction under an applied DC electric field (the sign of conventional current is the same whether an electron is moving left or a hole is moving right). Therefore, thermally excited electrons and holes cause a nonzero current to flow in a graphene device at the charge neutrality point (see *AE CHARGE PUMPING PAPER DC RESULTS*). However, the same is not true for acoustoelectric current. In an acoustoelectric device, the sign of current reverses between electron transport and hole transport (see AE CHARGE PUMPING PAPER AE RESULT).

In the following section, I introduce the theory of surface acoustic waves propagating through semiconducting piezoelectric materials and how they generate oscillating electric fields. I continue by exploring the interaction of these waves with thin films, and how the conductivity of a thin film influences its interaction with a surface acoustic wave. Lastly, I derive the expression for acoustoelectric current in a thin film, demonstrating that surface acoustic waves push both electrons and holes in the same direction.

2.2 Surface acoustic waves and acoustoelectric charge pumping

A surface acoustic wave (SAW) is an elastic wave that propagates along the surface of a material, with its energy confined to a depth of around one wavelength below the surface

[10]. When a SAW propagates in a piezoelectric substrate, it mechanically stresses the piezoelectric, generating electric fields. In turn, these electric fields generate strain in the substrate. If we coat this piezoelectric surface with a thin film, the SAW feels and responds to electronic and mechanical properties of the film (in this dissertation the thin film of interest is graphene). This interplay between a SAW and its propagation environment make SAWs interesting for both probing phenomena in quantum materials, such as *insert stuff from intro*, and using quantum materials to probe the environment, such as in gas sensors, humidity sensors.

All of these applications utilize the velocity shift and/or attenuation of the SAW as their sensing tool, which vary depending on mechanical and electronic properties of the thin film coating the piezoelectric surface. Also, in this dissertation, I use SAWs to pump charge through encapsulated graphene. Therefore, I need to develop an understanding of SAW propagation in piezoelectric substrates and the interaction of SAWs with the environment in which they are generated. As we will see, a one-dimensional model of longitudinal SAWs is sufficient to develop this understanding.

I begin this section with a discussion of elastic waves in bulk non-piezoelectric materials and derive the corresponding wave equation. Then, I discuss waves in bulk piezoelectric materials and explore how the effective stiffness of the piezoelectric substrate varies in cases of very low or very high bulk conductivity. Next, I consider the intermediate conductivity case and derive the bulk conductivity-dependent attenuation and velocity shift equations. Finally, I discuss how the velocity shift and attenuation change when the conductivity is located in a thin film on an insulating piezoelectric surface, and how the attenuation drives a DC acoustoelectric current in the thin film. This sets the stage for the later Sec. 4.6, where

I modify these equations to consider mixed-carrier transport in graphene. The discussion in this section follows that of Refs. [46, 47, 1], except where noted by additional references.

2.2.1 Elastic waves in non-piezoelectric materials

To understand the propagation of SAWs in piezoelectric materials, we must first understand the constitutive equation of waves in bulk elastic materials. The constitutive equation relates the displacement of an internal element of this elastic material, known as “strain” (a dimensionless quantity), to the internal forces which caused the strain, known as “stress” (dimensions of force per unit area). The relationship between stress and strain determines how elastic waves propagate. Consider an infinitesimal element dx which is deformed to a length $du+dx$ (Fig. 2.5). Strain, denoted by S , is defined by the local change in displacement du relative to the original length dx ,

$$S = \frac{\partial u}{\partial x}. \quad (2.10)$$

This is a one-dimensional model, so we do not consider shear strains. Stress, denoted by T (not to be confused with temperature!), is related to strain by the constitutive equation

$$T = cS, \quad (2.11)$$

where c is the stiffness coefficient, also known as Young’s modulus. This is a generalization of Hooke’s law, with a linear relationship between strain and stress. Stress T is related to du by

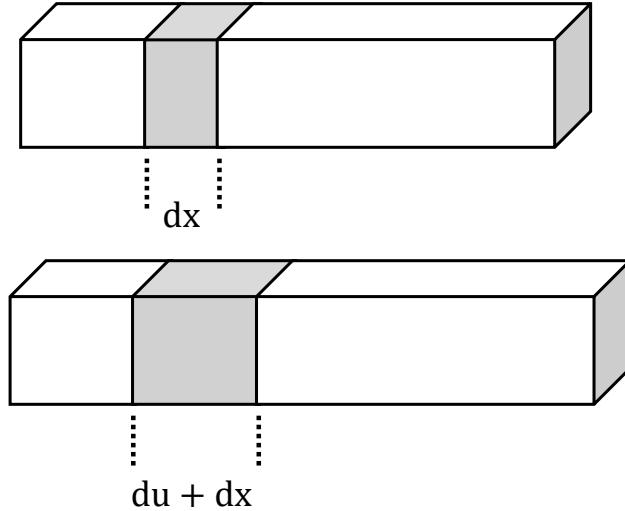


Figure 2.5: A one-dimensional illustration of an element which deforms from length dx to $du + dx$.

$$\frac{\partial T}{\partial x} = \rho \frac{\partial^2 u}{\partial t^2}, \quad (2.12)$$

where ρ is the mass density of the material. From these relations, we get an equation for waves in elastic materials

$$\frac{\partial^2 u}{\partial t^2} = \frac{c}{\rho} \frac{\partial^2 u}{\partial x^2}, \quad (2.13)$$

from which we can readily see that plane waves propagate in this elastic material with a velocity $v_0 = \sqrt{\frac{c}{\rho}}$. This is familiar from travelling acoustic waves in a string: as stiffness increases, waves propagate more quickly, and as mass density increases, waves propagate more slowly. In piezoelectric materials, this intuition holds, with one caveat: the effective stiffness of a piezoelectric material depends on more than just its mechanical properties.

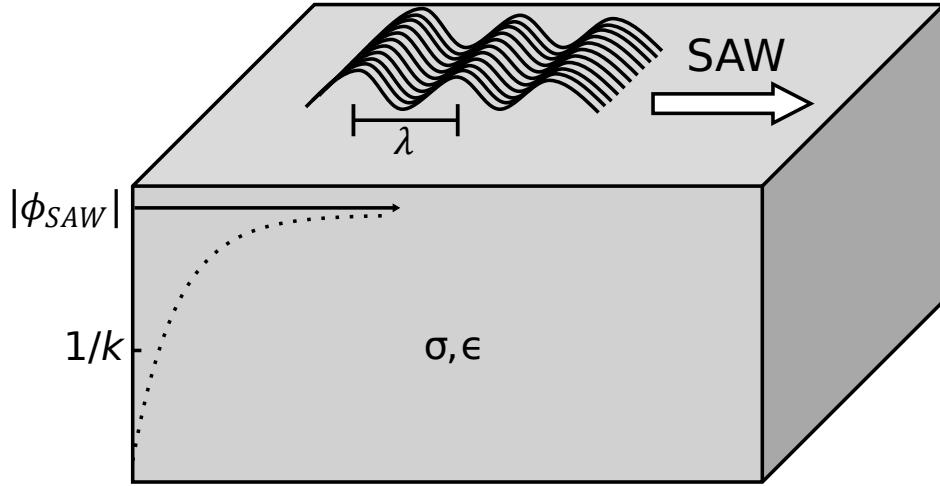


Figure 2.6: A surface acoustic wave travelling in a bulk piezoelectric material. The SAW amplitude $|\phi_{SAW}|$ is well-known to decay approximately exponentially into the surface, with most of its energy contained within a depth $1/k$ [1].

2.2.2 Waves in bulk piezoelectric materials

Consider a surface acoustic wave with wave vector k propagating in a bulk piezoelectric material with conductivity σ and dielectric permittivity ϵ , shown in Fig. 2.6. In a piezoelectric material, strain creates displacement fields (D -fields), and electric fields create stress. This translates to new constitutive equations for waves in piezoelectric materials. For small displacements u , these are

$$D = eS + \epsilon E \quad (2.14)$$

and

$$T = cS - eE, \quad (2.15)$$

where e is the piezoelectric constant (assumed here to cause electric fields only in the x -direction), c is the elastic constant at constant electric field, and ϵ is the dielectric permittivity at constant strain. Remembering the definition of displacement field $D = \epsilon E + P$, where P is polarization, we can see from Eq. 2.14 that the strength of polarization in piezoelectric materials scales with the piezoelectric constant e , and strain creates a polarization $P = eS$. Equation 2.15 can be thought of as the same generalized Hooke's law from Eq. 2.11, but with additional stress $-eE$ arising from the piezoelectric effect.

We are interested in the interaction of SAWs with conducting films, and Eqs. 2.14 and 2.15 do not include conductivity (denoted here by σ). To introduce the effect of conductivity on the constitutive equations, I first consider limiting cases of very high σ and very low σ . In a piezoelectric material with $\sigma = \infty$, $E = 0$ because the material can screen all internal electric fields. The piezoelectric equations of state reduce to

$$T = cS \quad (2.16)$$

and

$$D = eS. \quad (2.17)$$

In this case, our wave velocity is $v_0 = \sqrt{c/\rho}$ (unchanged from before), and the elastic wave propagates in tandem with D -fields. This case of a material with very high conductivity is framed by Wixforth et al. as “a material that [to the elastic wave] appears to be non-piezoelectric” [1].

The next limiting case is that of very low conductivity ($\sigma = 0$). In this perfect piezoelectric insulator, there is no free charge, so Poisson's equation requires that

$$\partial D / \partial x = 0. \quad (2.18)$$

Rearranging Eqs. 2.14 and 2.15, we find that the wave equation for our piezoelectric insulator is

$$\frac{\partial^2 u}{\partial t^2} = \frac{c}{\rho} \left(1 + \frac{e^2}{2c\epsilon}\right) \frac{\partial^2 u}{\partial x^2}. \quad (2.19)$$

Defining $c^* = c(1 + e^2/c\epsilon)$, this describes a wave travelling at a velocity $v^* = \sqrt{c^*/\rho}$. The piezoelectric interaction has caused our effective elastic constant to increase by a factor $e^2/2c\epsilon$! This quantity is known as the “piezoelectric coupling constant”, denoted $K^2 = e^2/c\epsilon$, which represents the ratio of coupled piezoelectric energy to total stored energy. “Total stored energy” includes energy stored both in the D-fields (scaling with ϵ) and in mechanical deformation (scaling with c).

K^2 varies widely between materials, ranging from 6.4×10^{-4} in GaAs [1] to 0.05 in LiNbO₃ [48]. Stronger piezoelectric interactions (increasing e) stiffen the material; conversely, a stronger dielectric (increasing ϵ) softens the material. This effective increase in elastic constant from piezoelectric interactions is known as “piezoelectric stiffening” and has important consequences for interactions between SAWs and charge carriers in thin films, as will be seen shortly.

Next, we tackle the case of intermediate σ — acoustic waves in a piezoelectric semiconductor. In this dissertation, acoustic waves in a piezoelectric semiconductor are particularly interesting because the physics is similar whether σ is contained in the bulk piezoelectric or a thin film (like graphene) on an insulating piezoelectric. The current density J in a

semiconductor is the sum of the drift and diffusion currents

$$J = qn\mu E + \frac{\mu}{\beta} \frac{\partial n}{\partial x}, \quad (2.20)$$

where q is the electron charge, β is the inverse of Boltzmann's constant times temperature, and n is the carrier density (assumed here to be populated only by electrons). Here, I assume the limiting case where drift current is much larger than diffusion current, so diffusion can be neglected. Differentiating Eq. 2.20 (neglecting diffusion), we have

$$\frac{\partial J}{\partial x} = \mu q \frac{\partial E}{\partial x}. \quad (2.21)$$

Using Poisson's equation $\partial D/\partial x = -qn$ and the continuity equation $\partial J/\partial x = q \partial n/\partial t$, Eq. 2.21 becomes

$$\frac{\partial^2 D}{\partial x \partial t} = -\mu q n \frac{\partial E}{\partial x}. \quad (2.22)$$

Assuming the E and D fields generated by our SAW take the form of plane waves $E = E_0 \exp(i(kx - \omega t))$ and $D = D_0 \exp(i(kx - \omega t))$, Eq. 2.22 becomes

$$D = -i \frac{\sigma}{\omega} E, \quad (2.23)$$

where $\sigma = \mu n q$ is the conductivity of the piezoelectric semiconductor. Now we can plug Eq. 2.23 into Eq. 2.14 to relate E to strain S , giving

$$E = -\frac{e}{\epsilon} \frac{(1 - i(\sigma/\epsilon\omega))}{1 + (\sigma/\epsilon\omega)^2} S. \quad (2.24)$$

Finally, the wave equation for a piezoelectric semiconductor can be found by substituting 2.24 into Eq. 2.15, giving

$$T = c \left(1 + \frac{e^2}{c\epsilon} \frac{(1 - i(\sigma/\epsilon\omega))}{1 + (\sigma/\epsilon\omega)^2} \right) S. \quad (2.25)$$

Clearly we have a similar equation to Eq. 2.19, in which our elastic constant is modified by piezoelectric interactions. Here, the value of our elastic constant varies with the ratio $\sigma/\epsilon\omega$. What is this ratio?

One might recognize σ/ϵ as the dielectric relaxation time. If this is not familiar, the derivation is as follows: Assume a free charge distribution qn in our semiconductor. Then, remember that from Poisson's equation and Eq. 2.21 we have

$$q \frac{\partial n}{\partial t} = \sigma \frac{\partial E}{\partial x} = \frac{\sigma q}{\epsilon} n, \quad (2.26)$$

where ϵ is the dielectric permittivity of our piezoelectric semiconductor. This differential equation describes an exponential relaxation of carrier density $n \propto \exp\{-t/\tau_c\}$ with characteristic time $\tau_c = \epsilon/\sigma$. τ_c is known as the “dielectric relaxation time”. For us, it’s helpful to think of the dielectric relaxation frequency $\omega_c = \tau_c^{-1} = \sigma/\epsilon$ (sometimes called the “characteristic frequency”), as it appears in 2.25.

Substituting $\omega_c = \sigma/\epsilon$, 2.25 becomes

$$T = c \left(1 + K^2 \frac{(1 - i(\omega_c/\omega))}{1 + (\omega_c/\omega)^2} \right) S \quad (2.27)$$

(recalling that $K^2 = e^2/c\epsilon$). Therefore, Eq. 2.27 describes a piezoelectric wave travelling at velocity $v = \sqrt{c'/\rho}$, where the modified elastic constant is $c' = c(1 + K^2(1 - i(\omega_c/\omega)))/(1 +$

$(\omega_c/\omega)^2)$.

Most notable in Eq. 2.27 is that the effective elastic constant c' depends on the ratio ω_c/ω . Modulating the ratio between the SAW frequency and the conductivity controls the piezoelectric stiffening. However, c' is complex. What does that mean? To understand the complex elastic constant in Eq. 2.27, consider its differential form,

$$\frac{\partial^2 u}{\partial t^2} = \frac{c'}{\rho} \frac{\partial^2 u}{\partial x^2}. \quad (2.28)$$

We can break c' into its real and complex parts. Assume $\sqrt{c'} = \beta + i\gamma$. Then, our plane wave solution becomes

$$u = u_0 e^{(i(kx - k\sqrt{c'/\rho}t))} = u_0 e^{\gamma kt/\sqrt{\rho}} e^{i(kx - \beta kt/\sqrt{\rho})}. \quad (2.29)$$

Examining Eq. 2.29, we can readily see that it describes a plane wave with phase velocity

$$v = \beta/\sqrt{\rho} = R\epsilon\sqrt{c'}/\sqrt{\rho} \quad (2.30)$$

and exponential loss (also known as attenuation) per unit length of

$$\Gamma = k \operatorname{Im}(\sqrt{c'})/\sqrt{\rho}. \quad (2.31)$$

This use of a complex wave propagation constant, where the real and complex parts describe dispersion and attenuation, has been used to describe lossy wave propagation in mechanical, electromagnetic, and piezoelectric materials [49] [50, p. 18] [46, 51].

Using Eqs. 2.30 and 2.31, we find the velocity and attenuation of our SAW in a bulk

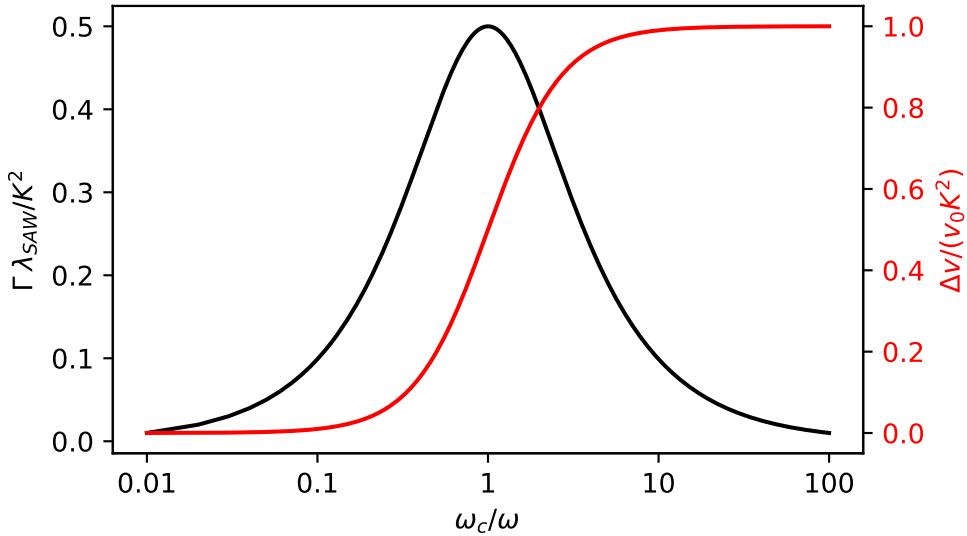


Figure 2.7: Eq. 2.33 (left axis) and Eq. 2.32 (right axis) plotted as dimensionless quantities against the ratio ω_c/ω .

piezoelectric semiconductor to be

$$\frac{\Delta v}{v_0} = \frac{K^2}{2} \frac{1}{1 + (\omega_c/\omega)^2} \quad (2.32)$$

and

$$\Gamma = K^2 \frac{\pi}{\lambda} \left(\frac{(\omega_c/\omega)}{1 + (\omega_c/\omega)^2} \right). \quad (2.33)$$

Figure 2.7 shows Eqs. 2.32 and 2.33 plotted with respect to ω_c/ω . From this, we can see that the SAW is maximally attenuated at $\omega = \omega_c$ and maximal velocity shift is achieved at $\omega \gg \omega_c$.

Equations 2.32 and 2.33 are known as the “classical relaxation model” for the acoustoelectric effect. Equation 2.32 describes relaxation dispersion, which is common in other

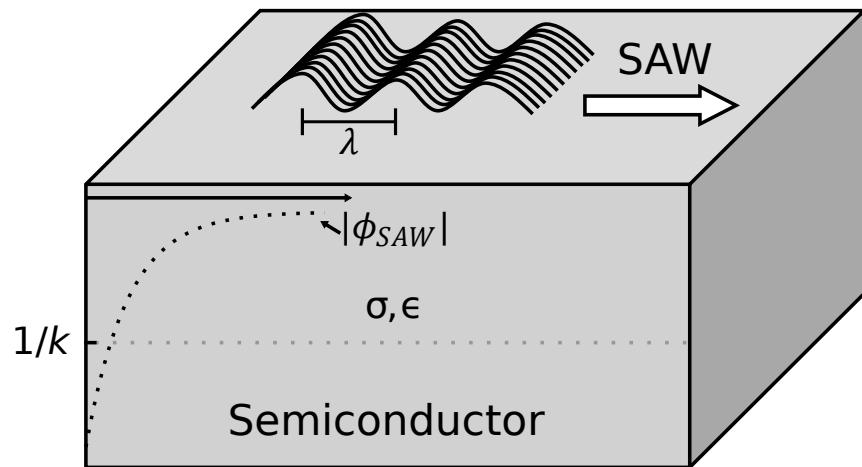
acoustic systems [47, 52] and can be understood as follows: First, the SAW strains the piezoelectric, perturbing the material from its equilibrium state. Then, the piezoelectric relaxes to equilibrium, returning energy to the SAW after a time $1/\omega_c$. However, depending on the time delay between stimulus ($1/\omega$) and response ($1/\omega_c$), this energy returns to the SAW with a phase delay, leading to dispersion and attenuation. In our case, the relaxation time (and thus, ω_c) depends on the conductivity of the piezoelectric semiconductor.

2.2.3 SAWs propagating in 2D materials

Equation 2.28 is fundamental to our investigations into acoustoelectric charge pumping (Ch. 4). However, Eqs. 2.32 and 2.33 describe a bulk piezoelectric material. How do these relations change when the conductivity is located in a thin film on an insulating piezoelectric material? Figure 2.8 (a) shows the bulk case described by Eqs. 2.33 and 2.32, in which the SAW's energy and the induced current is contained within a depth $1/k$ of the surface. Therefore, the conductance of the region of the bulk material in which the SAW is propagating is $\sigma' = \sigma/k$. Fig. 2.8 (b) illustrates a SAW propagating in a material with permittivity ϵ which is capped by a 2D material of thickness d .

This can be imagined as compressing the current-carrying region from thickness $1/k$ into a thin layer of thickness d and sheet conductivity $\sigma_{2D} = \sigma d$, where $d \ll 1/k$. Reducing the thickness of the current-carrying region from $1/k$ to d reduces its conductance by a factor of $1/kd$. Hence, in the 2D case, the dielectric relaxation frequency is also reduced by a factor of $1/kd$, giving $\omega_c = \sigma_{2D}k/\epsilon$. Then, we have

(a)



(b)

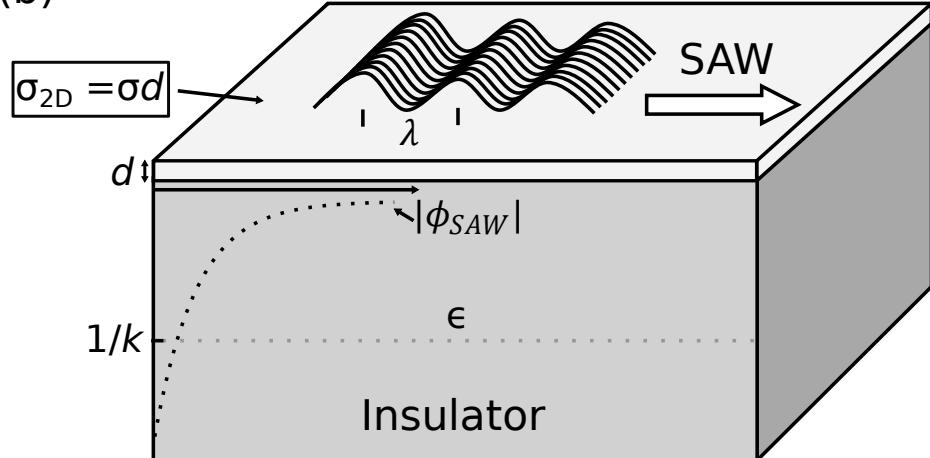


Figure 2.8: (a) A SAW propagating in a bulk material with conductivity σ and permittivity ϵ . (b) A SAW propagating in a piezoelectric material with permittivity ϵ that has been capped by a conductive material of thickness d and sheet conductivity $\sigma_{2D} = \sigma d$.

$$\frac{\omega_c}{\omega} = \frac{k\sigma_{2D}}{\epsilon} \frac{1}{\omega} = \sigma_{2D} \frac{k}{\omega\epsilon} = \frac{\sigma_{2D}}{\sigma_M}, \quad (2.34)$$

where $\sigma_M = v\epsilon$ is defined as the “characteristic conductivity” of the dielectric environment around the 2D material. Finally, Eqs. 2.32 and 2.33 become

$$\frac{\Delta v}{v_0} = \frac{K^2}{2} \frac{1}{1 + (\sigma_{2D}/\sigma_M)^2} \quad (2.35)$$

and

$$\Gamma = K^2 \frac{\pi}{\lambda} \left(\frac{(\sigma_{2D}/\sigma_M)}{1 + (\sigma_{2D}/\sigma_M)^2} \right). \quad (2.36)$$

Similarly to the bulk case (Eqs. 2.32 and 2.33), the SAW is dispersing and losing energy as it interacts with this conductive 2D material. However, the attenuation and dispersion is frequency-independent, and depends only on the ratio σ_{2D}/σ_M . This leads to an important question: Where does the lost SAW energy go?

2.2.4 The 2D acoustoelectric charge pumping effect

Fal’ko and Iordanskii found that the oscillating electric field that co-propagates with the SAW imparts an effective force on charge carriers. When this electric field passes through a thin film, it drives a DC sheet current that is proportional to the attenuation Γ [53]. In this section, I present the sketch of Fal’ko and Iordanskii’s model given in Ref. [15], which is more accessible than the original derivation in Ref. [53]. As previously discussed, a SAW

is accompanied by a co-propagating piezoelectric field of the form ²

$$E_p(x, t) = E_0 e^{i(kx - \omega t)}. \quad (2.37)$$

The mobile carriers in the thin film screen this field based on the local conductivity σ , resulting in an effective field

$$E_{eff}(x, t) = E_p(x, t) + E_{ind}(x, t) = \frac{E_p(x, t)}{1 + i(\sigma_{2D}/\sigma_M)}, \quad (2.38)$$

where E_{ind} is the induced screening field, and E_{ind} is phase-shifted with respect to $E_p(x, t)$ by $\phi = \arctan(\sigma_{2D}/\sigma_M)$.

This effective electric field creates a local oscillating current density

$$j(x, t) = \sigma_{2D} E(x, t), \quad (2.39)$$

where σ_{2D} is the sheet conductivity of the thin film, and $j(x, t)$ is a sheet current with dimensions of current/length. Assuming that the amplitude of the perturbation in carrier density caused by the SAW (denoted by Δn) is much smaller than the average carrier density in the thin film (denoted by n_0), the periodic carrier density in the SAW takes the form ³

$$n(x, t) = n_0 + \Delta n(x, t). \quad (2.40)$$

Using the continuity equation $\partial J/\partial x = q \partial n/\partial t$, Δn can be written in terms of $E(x, t)$,

²Note that when a quantity such as $E(x, t)$ or $j(x, t)$ is complex, the physical observable is given by the real part.

³If $\Delta n \geq n_0$, the perturbation in n can not be approximated as local, leading to the nonlinear acousto-electric effect. I discuss this further in Sec. 4.9.

giving

$$\Delta n(x, t) = -\frac{\sigma_{2D}}{q} \frac{k}{\omega} E_{eff}(x, t) = -\frac{\sigma_{2D}}{q} \frac{1}{v} E(x, t). \quad (2.41)$$

At this point, from Eqs. 2.41 and 2.38, we can predict how the pumped acoustoelectric current will depend on the ratio σ_{2D}/σ_M . Figure 2.9 shows $n(x, 0)$, $E_p(x, 0)$ for different values of σ_{2D}/σ_M . If $\sigma_{2D} \gg \sigma_M$ (the film is a perfect conductor), $E_{ind}(x, t) = -E_p(x, t)$, giving $E_{eff}(x, t) = 0$. This makes sense, as a perfect conductor can completely screen out the piezoelectric fields $E_p(x, t)$. If $\sigma_{2D} \ll \sigma_M$

This oscillating local carrier density will modulate the sheet conductivity. With $\Delta n \ll n_0$, and remembering that $\sigma_{2D} = qn\mu$, we can find the time-varying sheet conductivity $\sigma(x, t)$ in terms of Δ_n , which takes the form

$$\begin{aligned} \sigma(x, t) &= \sigma_0 + \frac{\partial \sigma_{2D}}{\partial n} \Delta n(x, t) = \sigma_0 + (q\mu) \left(\frac{-\sigma_{2D}}{q} \frac{1}{v} E(x, t) \right) \\ &= \sigma_0 - \frac{\mu \sigma_{2D}}{v} E(x, t). \end{aligned} \quad (2.42)$$

Now, we can find the DC acoustoelectric current by plugging Eqs. 2.42 and 2.41 into 2.39 and taking the time average, giving

$$\begin{aligned} j(x) &= \langle j(x, t) \rangle = \langle \sigma(x, t) E_{eff}(x, t) \rangle \\ &= \left\langle \left(\sigma_0 - \frac{\mu \sigma_{2D}}{v} E_{eff}(x, t) \right) E_{eff}(x, t) \right\rangle \\ &= -\frac{\mu}{v} \langle \sigma_{2D} E(x, t)^2 \rangle. \end{aligned} \quad (2.43)$$

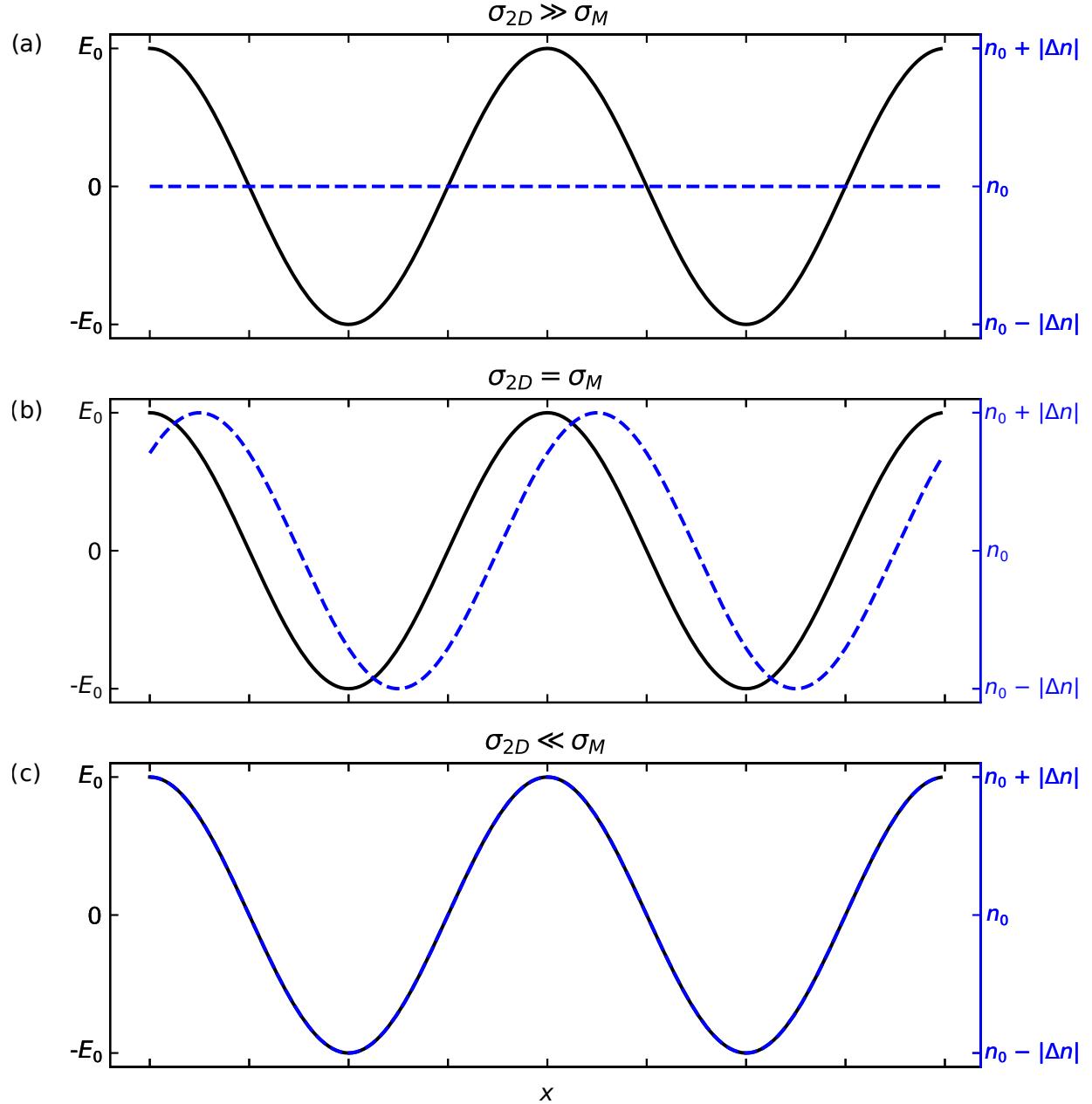


Figure 2.9: E_p (left axis) and Δn (right axis) plotted for the case of (a) $\sigma_{2D} \gg \sigma_M$ (very high sheet conductivity), (b) $\sigma_{2D} = \sigma_M$, and (c) $\sigma_{2D} \ll \sigma_M$ (very low sheet conductivity).

One might initially consider the notion of an oscillating E -field creating a DC current to be counter-intuitive. However, we can now see that, though $\langle E_{eff}(x, t) \rangle = 0$, a DC current arises from the cross-term $\langle \sigma E_{eff}(x, t)^2 \rangle$, which corresponds to the time-averaged Ohmic power dissipated by the charge carriers in the thin film. So far, this model considers a local perturbation in n from the SAW; therefore, this cross-term can be thought of as the local dissipation of SAW power by charge carriers in response to the co-propagating electric field. Finally, we need to relate Eq. 2.43 to Γ . Remembering that Γ describes the loss in SAW intensity per unit length, the SAW intensity I can be written in the form

$$I(x) = I_0 e^{(-\Gamma x)}. \quad (2.44)$$

Rearranging and differentiating I with respect to x , Γ takes the form

$$\Gamma = \frac{1}{I} \frac{\partial I}{\partial x} = \frac{1}{I} \langle \sigma E(x, t)^2 \rangle. \quad (2.45)$$

Then, combining Eqs. 2.43 and 2.45, the DC acoustoelectric current density becomes

$$j = -\frac{\mu}{v} \langle \sigma E(x, t)^2 \rangle = -\frac{\mu}{v} I \Gamma = -\frac{\mu I}{v} \frac{K^2}{2\lambda} \left(\frac{(\sigma_{2D}/\sigma_M)}{1 + (\sigma_{2D}/\sigma_M)} \right). \quad (2.46)$$

If the charge carrier is a hole instead of an electron, the continuity equation is instead $\partial J/\partial x = -q \partial n/\partial t$. Thus, the sign of Eq. 2.41 is reversed, giving

$$\Delta p(x, t) = \frac{\sigma_{2D}}{q} \frac{1}{v} E(x, t) \quad (2.47)$$

for the local oscillating hole density. The conductivity is still given by $\sigma_{2D} = qp\mu$ (does not flip sign), resulting in

$$\sigma(x, t) = \sigma_0 + \frac{\mu\sigma_{2D}}{v} E(x, t) \quad (2.48)$$

for the time-varying sheet conductivity in the hole-transport case. Finally, the DC acousto-electric current density for hole transport becomes

$$j = \frac{\mu I}{v} \frac{K^2}{2\lambda} \left(\frac{(\sigma_{2D}/\sigma_M)}{1 + (\sigma_{2D}/\sigma_M)} \right). \quad (2.49)$$

Comparing Eqs. 2.46 and 2.49, they are identical, but have opposite sign. Therefore, the SAW pushes both electrons and holes in the same direction. This is in stark contrast to ordinary DC current, where electrons and holes move in opposite directions under a DC electric field, resulting in the same sign of conventional current for electron and hole transport.

Equations 2.35, 2.36, and 2.49 are central to interactions between SAWs and quantum materials. In Sec. 4.6, we modify this classical relaxation model, which assumes charge carriers of a single type, to describe mixed-carrier transport in graphene.

2.3 Surface acoustic wave device design rules

So far, I have described the propagation of surface acoustic waves, and how they interact with charge carriers in thin films; however, I have not discussed how they are generated. In this section, I discuss the electrical response of interdigitated transducers (IDTs). The electrical response of IDTs inform the design of IDTs.

The discussion in this section follows that of Chapters 3 and 4 of Ref. [54].

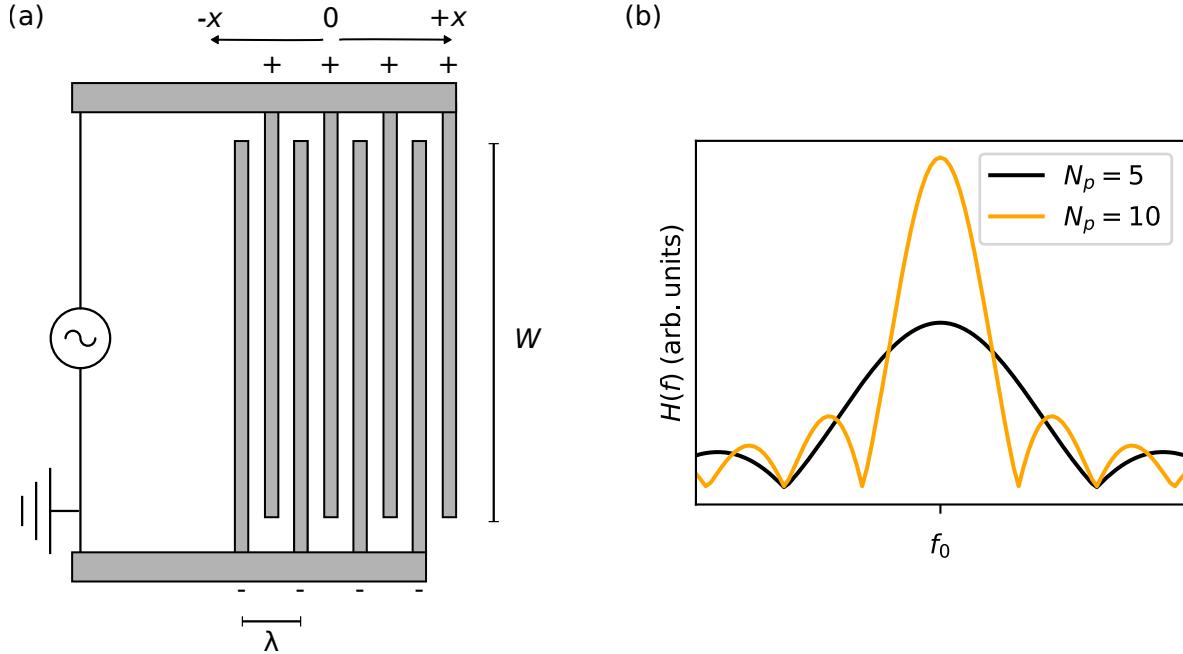
IDTs convert an RF signal into surface acoustic waves, or surface acoustic waves into RF signal. Figure 2.3 shows a schematic of an IDT. The wavelength *lambda* of the generated SAW spans two fingers of the IDT. Because of this, one of the defining parameters of an IDT is the number of finger pairs N_p .

The electrical response of an IDT can be approximated by assuming that each IDT finger is an infinitely thin point source, spaced by $\lambda/2$. This is known as the “delta function model”. The frequency response, or transfer function, of a single IDT in the delta function model can be approximated as

$$H(f) = \frac{V_{in}}{V_{out}} = N_p \left| \frac{\sin(N_p\pi(f - f_0)/f_0)}{N_p\pi(f - f_0)/f_0} \right|, \quad (2.50)$$

where $V_{in} = \sqrt{P_{RF}}$ is the amplitude of the input RF signal, $V_{out} = \sqrt{P_{SAW}}$ is the amplitude of the output SAW and $f_0 = v/\lambda$ (where v is the SAW velocity) is the center frequency of the IDT. Figure 2.3 (b) shows Eq. 2.50 for various values of N_p . From this, we can glean some important features of IDT response: The maximum conversion of input power to SAW power will be at the center frequency f_0 , and as N_p increases, a higher proportion of input RF power is converted to SAW power, but the central bandwidth of the IDT decreases.

When powering our IDT, we want to minimize the loss between applied RF power and output SAW power. For example, in the experiments described in Ch. 4, a higher resultant SAW power results in a larger acoustoelectric signal. Most RF signal generators are designed with 50Ω input impedance. Therefore, if we power our IDT of impedance Z_{IDT} , the ratio



of input RF power P_{RF} to resultant SAW power P_{SAW} (or, transmission coefficient) is

$$\frac{P_{RF}}{P_{SAW}} = \frac{2Z_{IDT}}{Z_{IDT} + 50\Omega} \quad (2.51)$$

The impedance of an IDT depends on its geometry, and must be evaluated numerically. This problem has been considered by numerous other authors (for example, Ref. [55]), and is beyond the scope of this dissertation. The relevant results are as follows: An IDT can be modelled as an equivalent circuit with capacitance C_{IDT} , real conductance G , and complex conductance B . The total IDT admittance $Y = 1/Z_{IDT}$ is given by

$$\begin{aligned} Y(f) &= G(f) + i(B(f) + 2\pi C_{IDT}) \\ &= G_0 \left(\frac{\sin X}{X} \right) + i \left(\frac{\sin(2X) - 2X}{2X^2} \right) + i2\pi f C_{IDT}, \end{aligned} \quad (2.52)$$

where X is given by

$$X = N_p \pi \frac{f - f_0}{f_0}, \quad (2.53)$$

and G_0 is the admittance at the center frequency, given by

$$G_0 \approx 8K^2 N_p^2 f_0 W C_s, \quad (2.54)$$

where C_s is the capacitance per unit length per finger pair, and K^2 is the piezoelectric coupling coefficient (see Sec. 2.2.2).

This model does not consider reflections. In real IDTs, each finger not only absorbs SAWs, but also reflects them. The reflection coefficient of a single IDT finger is around 1%, so Eq. 2.52 is still useful for estimating the impedance of an IDT design. For a more accurate model that considers reflections from each IDT finger, coupling of modes analysis must be used (see Refs. [56, p. 140-149] and [54, Ch. 4]). I use Eq. 2.52 to estimate the impedance of my IDTs in Sec.

Chapter 3: Methods

3.1 Fabricating 2D devices

In 2010, the 2D materials revolution was launched when Geim and Novoselov won the Nobel Prize for their experiments on exfoliated graphene [5]. From the humble beginnings of the ‘scotch tape technique’, the field of has matured to an immense parameter space of layered materials for us to explore. In this lies the greatest strength of 2D materials — we can combine the strengths of different materials to create designer heterostructures. These stacks of 2D materials are called “van der Waals heterostructures”, from the van der Waals force that holds them together. In this chapter, I describe methods for fabricating 2D devices. I begin by describing the best practices that I have found for exfoliation. Then, I discuss my implementation of the dry transfer method for stacking 2D materials to create designer heterostructures. Lastly, I show two methods for making electrical contact to 2D materials — photolithography and electron-beam lithography (EBL) — and compare the strengths and weaknesses of each.

3.1.1 Exfoliation of 2D crystals

While some groups are investigating large-area 2D growth for use in the next generation of electronics [57], the best devices with the lowest electrostatic disorder are still made using mechanical exfoliation [45]. Using sticky tape, layered crystals are cleaved 5-10 times, then

transferred onto clean SiO₂. Exfoliation is a simple process, but getting consistent results can be challenging due to the vast array of variables that affect the process. Different research groups, and even different members in the same group, can have vastly differing opinions on the best methods for exfoliation. Furthermore, every 2D material has different mechanical properties, so the best recipe varies widely between materials. I gained substantial knowledge on 2D material exfoliation from my visit to the Xu group at University of Washington in 2017. Since then, I have developed my best practices through trial and error. In this section, I briefly describe my best practices for exfoliating graphene and h-BN using sticky tape. At the end of this section, I collect some tips and tricks that I have learned from performing many exfoliations. For a review of exfoliation techniques and a model of the complex physics behind mechanical exfoliation, see Ref. [58].

Exfoliation begins with selecting the tape. The two most widely used tapes are Scotch® Magic™ Tape (“Scotch Tape”) and Nitto Denko SWT20+ wafer tape, (“blue tape”). The main differences between the two are as follows: Scotch tape is stickier and leaves more residue, and blue tape is less sticky and leaves less residue. While blue tape might seem like the obvious choice for the cleanest samples, in a discussion with members of the Yankowitz group at University of Washington, I learned that they still prefer Scotch tape for graphene, as they feel it gives the largest monolayer flakes. In my experience, I find that Scotch tape does work best for graphene, giving larger-area flakes than blue tape. For h-BN, I prefer to use blue tape, as the residue left by scotch tape is similar in color to the h-BN flakes.

Figure 3.1 shows a general overview of the exfoliation process. The details are as follows: First, I place a bulk layered crystal (such as graphite or boron nitride) onto sticky tape. Then, the tape is folded over and peeled back, cleaving the bulk crystal 8-10 times for

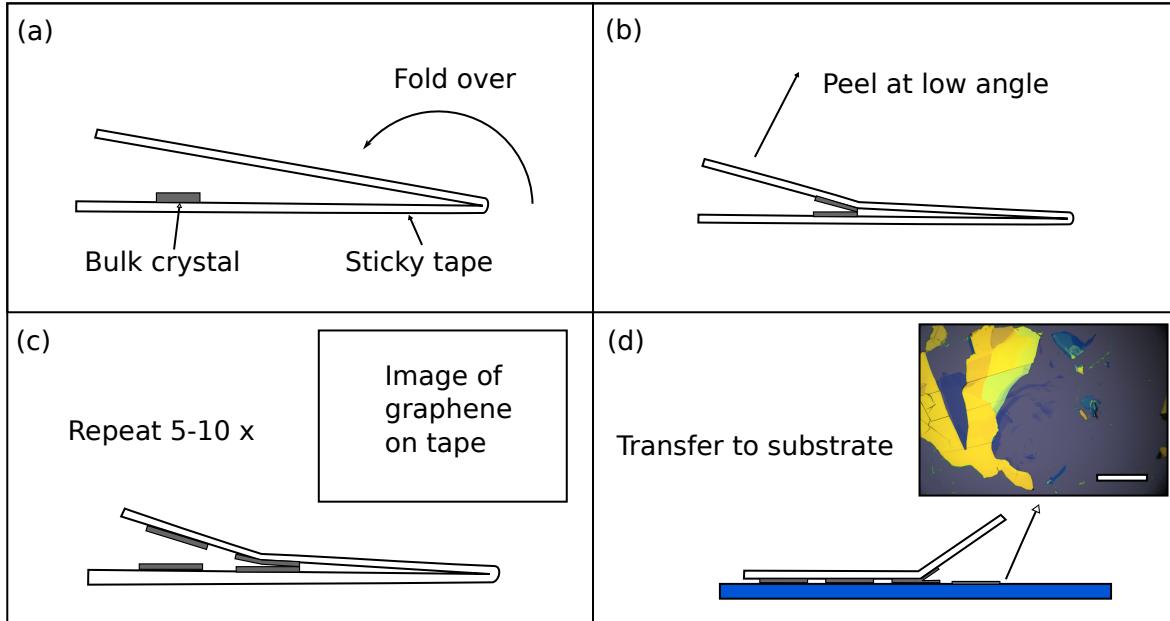


Figure 3.1:

graphene and 3-5 times for h-BN. While cleaving the bulk crystal, I plasma-clean a 300 nm SiO₂/Si substrate¹ using a PE-50 plasma etcher with O₂ plasma at 50 W for 1 minute. Then, I place the tape with cleaved crystals onto the plasma-cleaned SiO₂ substrate and rub the top of the tape with a semi-hard instrument, such as the back of a pen or an eraser, to ensure that the tape is in good contact with the substrate. Next, I heat the substrate with tape at 90 °C for 5 minutes, which helps adhere the 2D flakes to the SiO₂ (see Fig. 3 D of [58]). Finally, I peel the tape from the SiO₂ slowly at a low angle, cleaving flakes from the tape onto the SiO₂.

This exfoliation process results in flakes of a variety of sizes and thicknesses, from single-layer to thousands of layers (see inset of Fig. 3.1 (d)). The number of layers can be de-

¹Different SiO₂ thicknesses provide better optical contrast for different materials. 300 nm works well for graphene and h-BN.

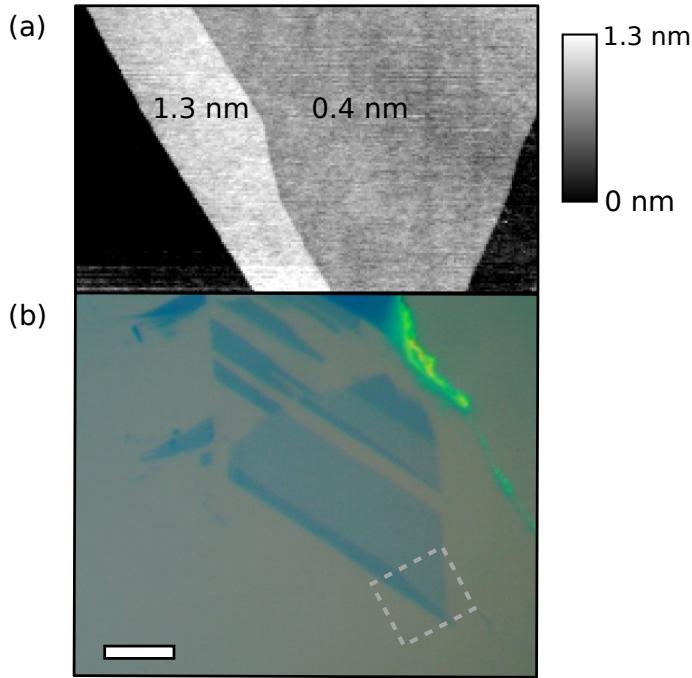


Figure 3.2: (a) AFM scan and (b) optical image of exfoliated graphene on SiO_2 . The AFM scan region is indicated by a gray dotted box. Scale bar = 10 μm .

terminated by examining the optical contrast between the 2D flakes and the surface, and confirmed with AFM. Figure 3.2 shows a tapping-mode AFM image (a) and optical image (b) of an exfoliated graphene flake.

Accurately measuring the number of layers of a graphene sample with AFM is difficult due to interactions between the AFM tip and graphene and water layers on substrates prepared in atmospheric conditions [59]. These difficulties can be reduced by using tapping-mode AFM; however, if monolayer graphene is necessary for an experiment, it is better to use Raman microscopy, which can distinguish between monolayer and multilayer graphene. In the graphene devices described in this dissertation, having monolayer graphene is not imperative, so I used AFM to determine the layer number of my graphene samples.

Here is a summary of my tips and tricks for exfoliation:

- Use scotch tape for graphene, and blue tape for h-BN
- Cleave 6-8 times on tape for graphene
- Cleave 3-5 times on tape for h-BN
- When peeling tape, peel at a low angle. The conventional wisdom is that this results in larger-area flakes.
- When placing h-BN bulk crystals onto tape, use tweezers to “smear” them flat onto the tape. h-BN crystals are thick, and need to be pressed flat to ensure good contact with the tape.
- In the final step, anneal tape on SiO_2 at 90°C for 5 minutes for all materials, then cool completely (2 minutes) before peeling tape from SiO_2 .
- Clean SiO_2 with O_2 plasma for 1 minute immediately before transferring crystals from tape onto SiO_2 .

3.1.2 Stacking 2D materials to create heterostructure devices

The ability to isolate single layers of 2D crystals with mechanical exfoliation opened wide the possibility of stacking different atomic layers to create designer heterostructures. In 2010, Dean et al. demonstrated that the mobility and electronic disorder of graphene can be vastly improved by encapsulating the graphene in insulating hexagonal boron nitride (h-BN) [44]. Since then, techniques for assembling stacks of 2D materials have improved, allowing for sub-micron lateral precision and sub-degree rotational alignment between layers [60]. Heterostructure fabrication techniques fall into two main categories: wet-transfer methods, which use sacrificial polymer layers to place down each 2D crystal, and dry-transfer methods, which only require dissolving the polymer stamp once the entire structure is completed. In

general, dry transfer methods are preferred as they reduce contamination between layers, and it is the method I use to create the devices discussed in this dissertation. Therefore, I will only describe the dry transfer method here. Similarly to exfoliation techniques, many researchers have different opinions on the best tricks for 2D transfer. For an overview of different 2D transfer methods, see the review by Castellanos-Gomez et al. [60]. The methods I present in the subsequent sections were initially learned through discussions with researchers at the University of Washington, then modified based on my own trial and error.

Figure 3.4 shows a generalized version of the dry transfer process that I use to build the devices in this dissertation. A sticky polymer stamp is mounted onto a micromanipulator stage underneath a long-focal length microscope. The stamp is brought into contact with a chip containing exfoliated 2D flakes. The temperature of the stage is increased to make the polymer stamp stickier. Then, the contact area of the stamp on the chip is increased by lowering the stamp. Once the entire 2D flake is covered with polymer, the stage is slowly retracted to pick up the 2D flake. This process is repeated to build the desired heterostructure top-down, using the previous layer to pick up the next. Finally, the stamp is melted at a high temperature and dissolved in a solvent. This method of heating up a polymer stamp to build 2D heterostructures is called the “hot pick up technique” [61].

3.1.2.1 Making the viscoelastic stamp

Figure 3.3 shows the viscoelastic stamp that I use, which is used to pick up and place 2D flakes. The stamp consists of a polydimethylsiloxane (PDMS) layer mounted on a glass slide, with a thin poly(bisphenol A carbonate) (PC) polymer layer on top (some groups use

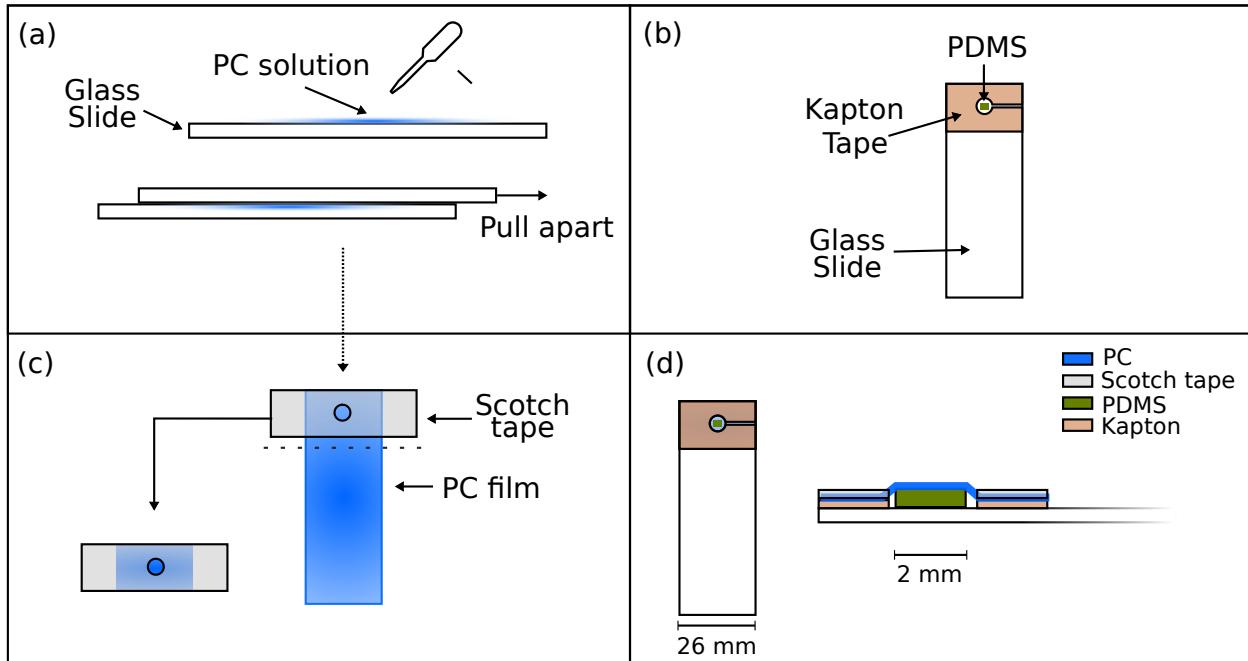


Figure 3.3: The viscoelastic stamp fabrication process.

polypropylene carbonate, referred to as PPC). The PDMS acts as a base for the stamp, while the PC layer becomes sticky at elevated temperatures.

I build the stamp as follows: First, I prepare the PC film (Fig. 3.3 (a)) I begin by making a solution of 6% PC in chloroform (mass percent). The PC takes 24-48 hours of stirring at medium speed to fully dissolve. Then, I clean two glass slides and place them next to each other in a fume hood. I pipette $\approx 2\text{ mL}$ of PC solution in a line on one glass slide, then flip the other slide on top. Using light pressure, I slide the two glass slides apart, leaving a film of PC on one side of each slide. Finally, I let the slides dry for at least 1 min before continuing².

To prepare the slide that composes the base of the stamp, I use a leather punch to punch a

²The chloroform evaporates very quickly, but I usually let it dry while preparing the rest of the stamp.

hole in a piece of double-sided polyimide tape (Kapton). Then, I place this piece of tape on a fresh glass slide, and cut a channel in one side of the tape (Fig. 3.3 (b)). This channel allows for air to escape when placing down the PC film in the next step. Without the channel, air gets trapped between the PDMS and PC layers. Next, I take pre-made PDMS sheets (Gel-Pak) that are 17 mil (0.432 mm) thick. These Gel-Pak sheets have a hard backing on one side, and a soft backing on the other side. I place a strip of double-sided polyimide tape (Kapton) into a plastic dish and place a $\approx 2 \times 2$ cm piece of Gel-Pak sheet onto the dish, hard backing-side down. The choice to put the hard backing side down makes picking up small pieces of PDMS easier. Then, I use a clean razor blade to cut the PDMS into 2×2 mm squares. Using tweezers, I grab one of these squares and place it into the hole in the center of the mounted Kapton tape (Fig. 3.3 (b), green square).

Next, I use a leather punch with diameter ≈ 4 mm to make a hole in a piece of scotch tape. Then, I put this scotch tape down onto the dried PC film, ensuring that the area in the tape hole is clean and uniform (Fig. 3.3 (c)). I cut the PC on the edge of the scotch tape using a razor blade and pick up the PC film. Lastly, I place the PC film onto the prepared slide base, aligning the hole in the scotch tape with the hole in the Kapton tape, and press the edges of the hole to ensure good adhesion between the scotch and Kapton tapes. Figure 3.3 (d) shows a completed viscoelastic stamp. Before using a stamp to transfer 2D flakes, I inspect it in an optical microscope to ensure that no dust came between the PC and PDMS layers. If there is dust trapped between the layers, it can cause the two layers to de-laminate from each other. Also, 2D flakes can not be picked up near dust, as the large dust prohibits the stamp from making good contact to the 2D material. Then, I anneal the stamp at 90 C for 5 minutes to ensure good contact between the PC and PDMS. Finally, I put the stamp

in the transfer station and lower it onto a bare SiO₂ substrate to check the location in which it first touches the surface. This determines the initial touch-down point of the stamp in the next step.

3.1.2.2 The hot pickup process

Figure 3.4 outlines the hot pickup process that I use for building 2D heterostructures. First, I select 2D flakes of interest using optical microscopy. Ideal flakes have a large area of a single thickness, and are free of residue (see inset of Fig. 3.4 (a)). I also take AFM images of flakes before I use them in a heterostructure to confirm their thickness and check for residue.

I begin the transfer process by lowering the viscoelastic stamp until it touches the surface. Then, I heat up the stage to at least 40 °C. The conventional wisdom is that higher temperature makes the stamp more sticky. However, high temperature also increases the likelihood of the PC and PDMS layers de-laminating (peeling away from each other), so I prefer to start at a lower temperature. For the same reason, I don't heat the stage above 90 °C during the transfer process.

I then lower the z-stage until the entire 2D flake is covered by polymer. The inset of Fig. 3.4 (b) shows a 2D flake during the polymer expansion process. The interference fringes indicate the direction that the polymer is expanding, and the smooth surface of the portion of the flake that is covered by polymer indicates good contact between the polymer and 2D flake. It is imperative that the 2D flake is smoothly covered by polymer — if any dust or bubbles separate the flake and polymer, the flake will be difficult to pick up. After the entire flake is covered by polymer, I slowly raise the z-stage to peel the flake off of the substrate.

The inset of Fig. 3.4 (c) shows a flake on a polymer stamp after pick-up.

Then, I find the next layer of the heterostructure and align to the previous layer by looking through the transparent polymer stamp. I then repeat the pick-up process, using the previous flake to pick up the next layer. Finally, to release the heterostructure from the stamp, I first lower the stamp onto the final substrate: Either a marker chip, if the next step is EBL (Sec. 3.3.1), or pre-patterned electrodes (Sec. 3.2.1). Then, I heat the stage to 170 °C to melt the PC away from the stamp, waiting 5 minutes to ensure that the PC is fully melted. Next, I slowly raise the stamp, ensuring that the PC pulls away from the stamp. It is important to watch the PC during this step — if the stage is too cool, the polymer will not melt enough, and the heterostructure will be picked up from the surface. Finally, I place the chip in a bath of chloroform for 20 minutes to dissolve the PC. At this point, spraying with a wash bottle of solvent can release the heterostructure from the surface. If residue needs to be cleaned off, I gently spray the edge of the chip with acetone then isopropyl alcohol, letting solvent run over the heterostructure.

Here are some tips and tricks that I have learned about the transfer process:

- Slowly peeling the flake from the substrate increases the success rate of the pick-up step.
- Higher temperatures make pick-up easier, but also increase the likelihood of ruining the stamp.
- Picking up thick flakes directly with the polymer stamp is easier than picking up thin flakes.
- Picking up subsequent flakes with h-BN is much easier than picking them up directly with the polymer.

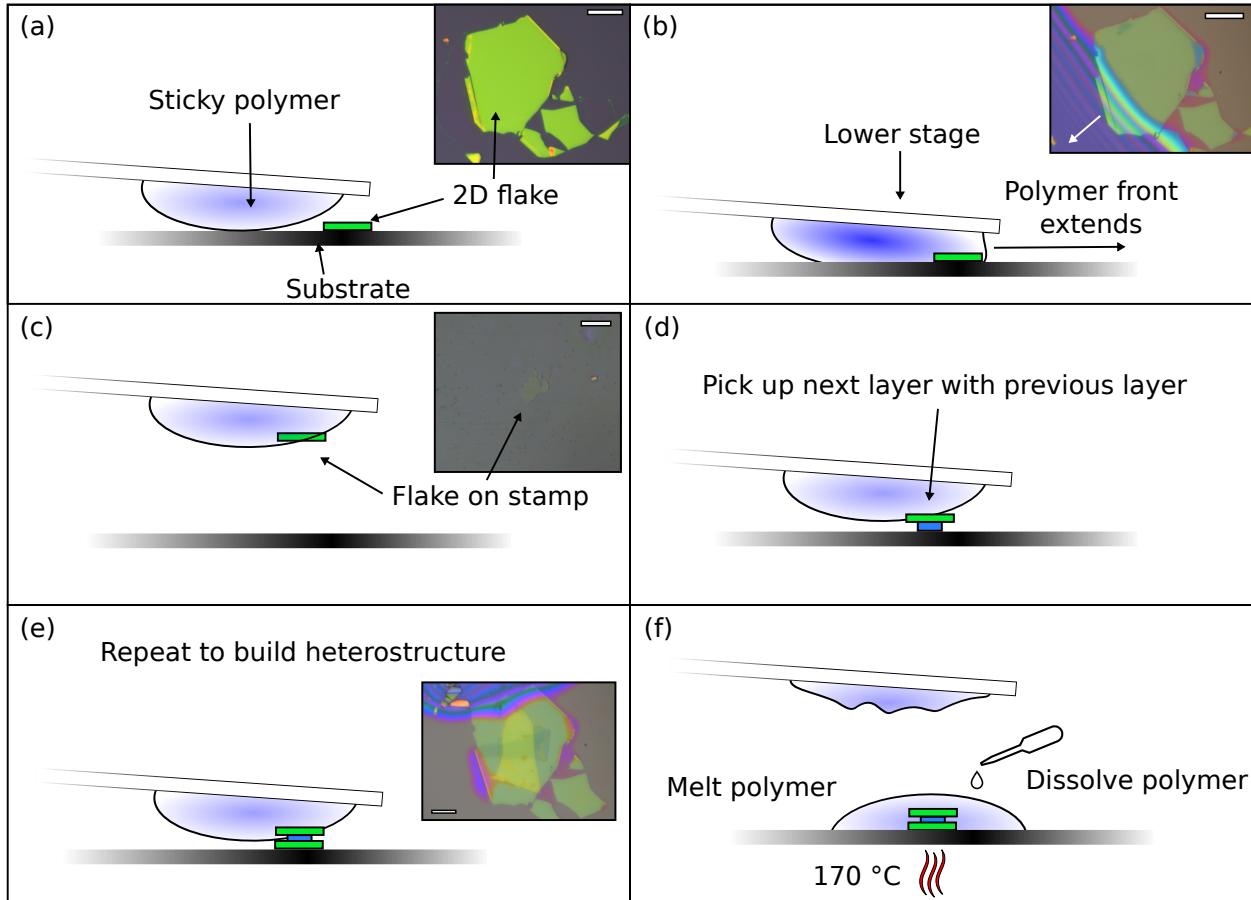


Figure 3.4: The hot-pickup process for constructing 2D heterostructures. (a) First, the polymer stamp is lowered close to a 2D flake. Inset: a ≈ 30 nm h-BN flake on SiO_2 . (b) The z-stage is slowly lowered and/or the stage is heated by 5°C at a time to slowly expand the polymer front over the 2D flake. Inset: a h-BN flake during the pickup process. (c) The z-stage is slowly raised, peeling the 2D flake from the substrate. Inset: A 2D flake which has been peeled from the substrate, barely visible on a polymer stamp. (d)-(e) Steps (a)-(c) are repeated, using the previous flake to pick up the next flake. (f) The completed heterostructure is placed down on the final substrate. The stage is heated to 170°C to melt the polymer. Finally, the polymer is dissolved in a solvent.

3.1.2.3 PCL cleaning

To be filled in

3.2 Contacts to 2D materials

3.2.1 Photolithography

In this section, I discuss methods for fabricating 2D devices on piezoelectric substrates using photolithography. One might ask: Why not use electron-beam lithography (EBL)? EBL can achieve higher lithographic resolution than photolithography and allows for custom circuit designs to match bespoke 2D heterostructures. For these reasons, EBL is an excellent choice for fabricating 2D devices on SiO₂ (Sec. 3.3.1). When performing EBL on a thin (< 0.5 μm) layer of insulating SiO₂ on conductive Si, the charge buildup from the electron beam can readily dissipate through the thin SiO₂. However, piezoelectric substrates like quartz or LiNbO₃ are insulating throughout, leading to charge buildup which deflects the incident electrons and distorts lithographic patterns. To dissipate the charge on insulating substrates, one can either deposit a thin charge dissipation layer on top of the EBL resist with thermal evaporation (often 10-20 nm of Al or Au), which is etched away after exposing the resist, or spin a conductive polymer on the EBL resist which is water-soluble [62]. These anti-charging layers complicate the fabrication process. Depositing a thin metal charge dissipation layer requires time-consuming thermal evaporation, and removing the metal requires a wet chemical etch. This needs to be repeated for every lithography step. Conductive polymers

solve these issues but are prohibitively expensive.³

At Oregon State, we can fabricate structures down to $3\text{ }\mu\text{m}$ with photolithography. Unless a device absolutely necessitates smaller feature sizes, it is in our best interest to simplify fabrication and reduce the number of processing steps. However, the motivation for reducing processing steps goes beyond just reducing cost and complexity. In my experience, 2D device fabrication is most likely to fail during liftoff. For example, Fig. 3.5 shows a 40 nm flake of h-BN transferred onto LiNbO_3 (top panel) which separated from the surface during liftoff (bottom panel), taking 50 nm of metal with it. For these reasons, I use photolithography to fabricate 2D devices on piezoelectric substrates. My process involves first creating pre-patterned metal contacts which are then cleaned using AFM (refer to Section 3.3) prior to transferring a 2D material onto them.

When transferring 2D flakes onto pre-patterned metal contacts, creating a smooth surface is of paramount importance. Therefore, clean liftoff with smooth edges is necessary. For this, I use a bilayer process with a tuned undercut, with S1813 photoresist on top of LOR 3A (“liftoff resist”). The full recipe can be found in App. B.1. Figure 3.6 shows a comparison between single-layer and bilayer liftoff processes in which I attempted to lift off $\approx 25\text{ nm}$ of Cr deposited on SiO_2 using electron-beam evaporation. In the single-layer process, metal which coated the resist walls did not lift off with the resist, creating wings that are much larger than the metal thickness. In a bilayer process, the bottom layer of resist develops faster than the top layer, creating an undercut profile that breaks the connection between the metal on the resist walls and the desired pattern. It’s clear that a bilayer process is

³The most common conductive polymer is ESpacer, which costs \$30,000 per 1 L bottle and expires after 6 months. Recently, an alternative conductive resist has been made available which is available in smaller quantities [63].

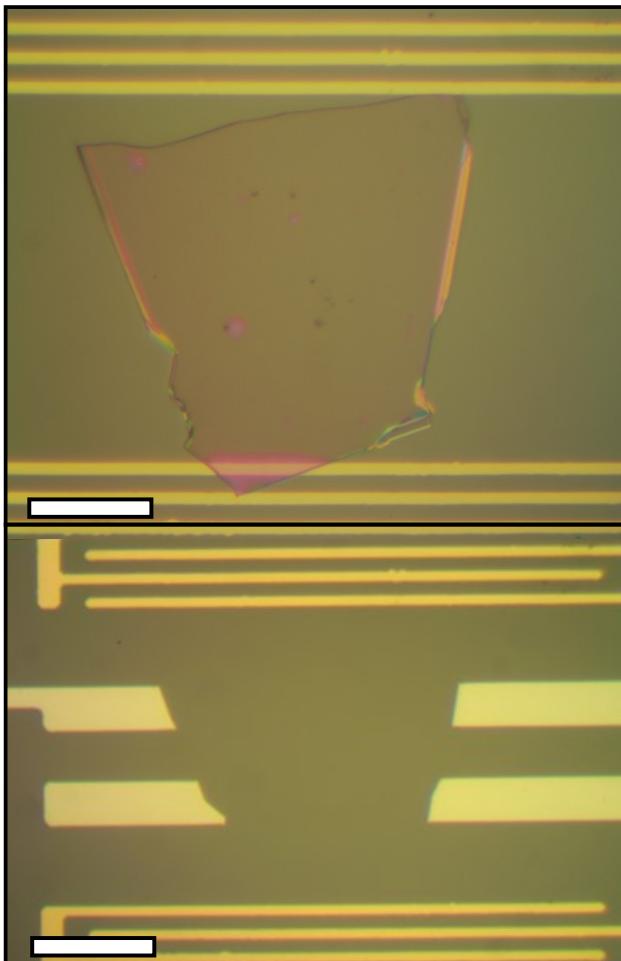


Figure 3.5: h-BN flake transferred onto LiNbO₃ before (top) and after (bottom) photolithography process to deposit metal electrodes on top of the h-BN. The h-BN lifted off with the deposited metal. Scale bar = 40 μm .

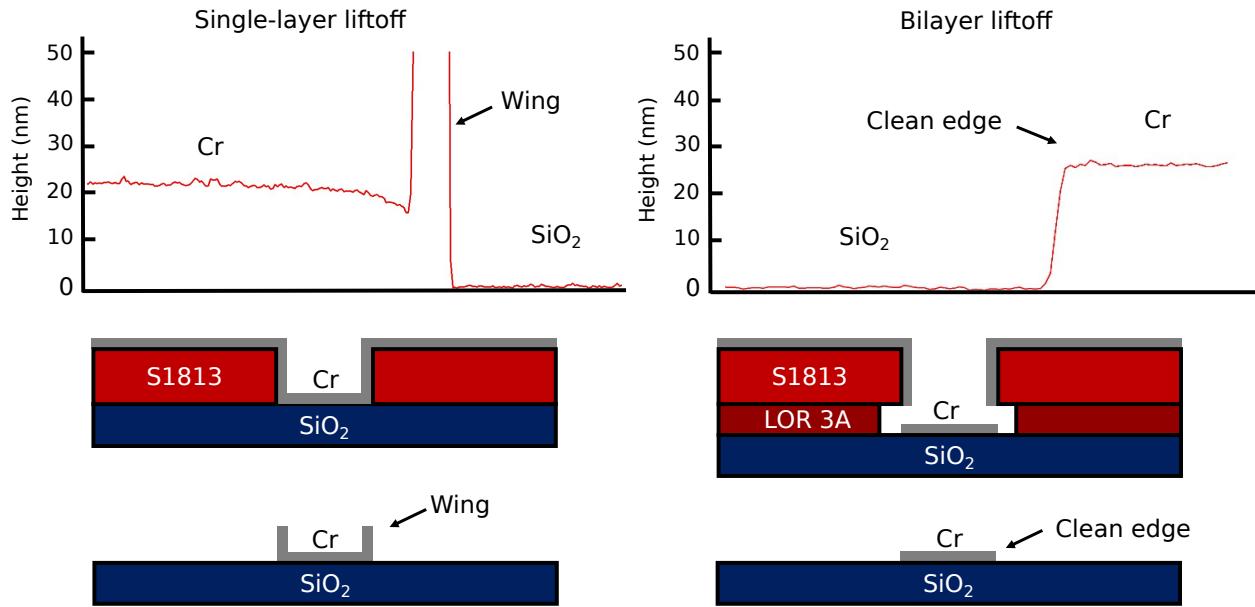


Figure 3.6: AFM trace (top) and schematic (bottom) for single-layer (left) and bilayer (right) liftoff processes of Cr on SiO₂

necessary for pre-patterned 2D material contacts.

The development rate of the LOR can be tuned by varying the bake temperature. A higher temperature bake results in a slower undercut rate, allowing us to optimize the undercut. If the undercut is too large, the top layer of resist will collapse. If the undercut is too small, the metal will not lift off cleanly. I first determined the optimal development time for S1813 as 100 seconds using the interdigitated finger pattern shown in Fig. 3.5. Then, I varied the LOR bake time from 170 C to 190 C and attempted liftoff of 3/20 nm Cr/Au. I found that 180 C was the lowest bake temperature at which liftoff was clean. Figure 2.4 shows a cross-sectional SEM image, in which I confirmed that a 180 C bake and 100 s development creates a \approx 3 μ m undercut.

The drawback of transferring metal onto pre-patterned contacts is that the contacts need

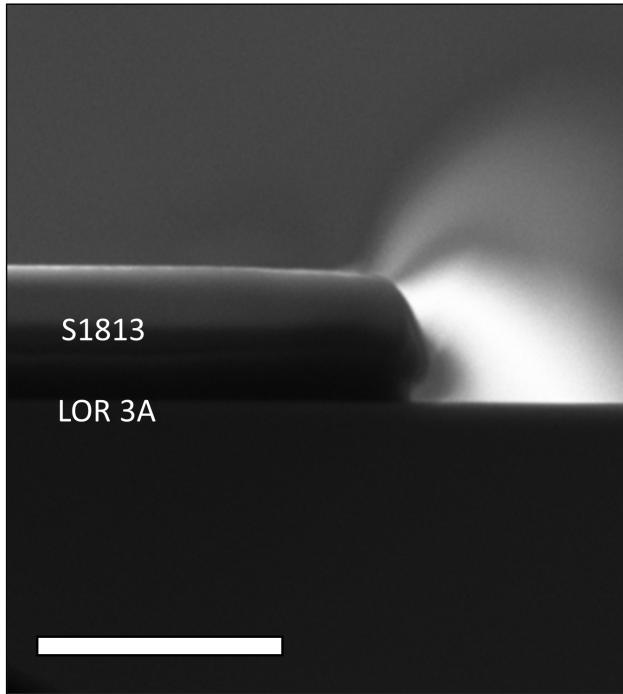


Figure 3.7: Cross-sectional SEM image showing bilayer resist process with undercut length $\approx 0.4 \mu\text{m}$. Scale bar = $3 \mu\text{m}$

to be cleaned to minimize contamination of the 2D material. In the next section, I detail a method for cleaning metal contacts with contact-mode AFM.

3.3 Cleaning electrodes with contact-mode AFM

Inevitably, as-deposited metal contacts will retain residues from the resist and solvents utilized during the photolithography process. Previously, contact-mode AFM has been used to remove contaminants from beneath 2D materials [38, 39]. However, I use contact-mode AFM to clean pre-patterned metal electrodes prior to transferring graphene onto them. I learned this technique from the Yankowitz group at the University of Washington.

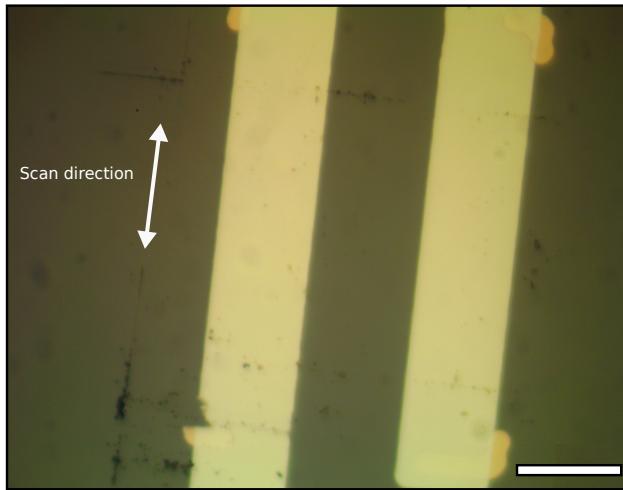


Figure 3.8: An optical microscope image of Pd electrodes on LiNbO₃ after AFM cleaning at a force of 150 N and a speed of 150 $\mu\text{m}/\text{s}$. Scale bar = 40 μm .

For this process, I use Tap150AL AFM probes (Budget Sensors) and an MFP-3D AFM. I first measure the exact spring constant of the AFM tip by taking a force curve. For the full force curve process and a sample force curve, see Appendix B.2. Then, I scan the AFM across the electrodes at a force of 150 N and a speed of 150 $\mu\text{m}/\text{s}$. The AFM scan size is 35 μm in the scan direction, and the Tap150AL tip has a minimum diameter of 10 nm. I chose 3584 lines for the scan (9.76 nm/line) to ensure that each line slightly overlaps the previous line. Figure 3.8 shows Pd electrodes after AFM cleaning. Although the metal appeared residue-free before cleaning, a significant amount of residue is now visible at the scan edges. For the devices described in Ch. 4, I use this process to clean pre-patterned Pd electrodes before transferring graphene onto them.

3.3.1 Electron-beam lithography

Electron-beam lithography uses the electron beam of a scanning electron microscope (SEM) to expose a polymer resist in a desired pattern. The electron beam breaks the bonds of the polymer, allowing it to be washed away with a chemical developer.

3.4 Interdigitated transducers

In this section, I discuss the fabrication and measurement of interdigitated transducers.

Before using an interdigitated transducer in an acoustoelectric device (Ch. 4), I need to verify its performance. In Sec. ??, I outline the expected frequency response and impedance of an IDT based on its geometry. Figure 3.9 shows an optical microscope image of an IDT that I fabricated on LiNbO₃ using photolithography (see App. B.1) and metallization of 5/25 nm Cr/Au.

A receiving IDT with identical geometry is located 200 μm away from the IDT pictured.

This IDT has $N_p = 20$ finger pairs and aperture width $W = 230 \mu\text{m}$. The SAW velocity on LiNbO₃ is 3488 m/s, giving a center frequency of $f_0 = 174.4 \text{ MHz}$. Using Eq. 2.52, the impedance of this IDT should be $Z_{IDT} \approx 170 \Omega$. In the rest of this section, when I refer to “the IDT pair”, I am referring to this specific pair of IDTs.

To benchmark the performance of the pair IDTs, I use an Agilent E5071C-280 vector network analyzer to measure their S-parameters. Figure 3.10 (a) shows the definition of the four S-parameters. S_{11} and S_{22} are the ratios of reflected RF power to input RF power for IDT 1 and IDT 2 respectively. S_{21} is the ratio of received RF power at IDT 2 to input RF power at IDT 1, and S_{12} is the ratio of received RF power at IDT 1 to input RF power at

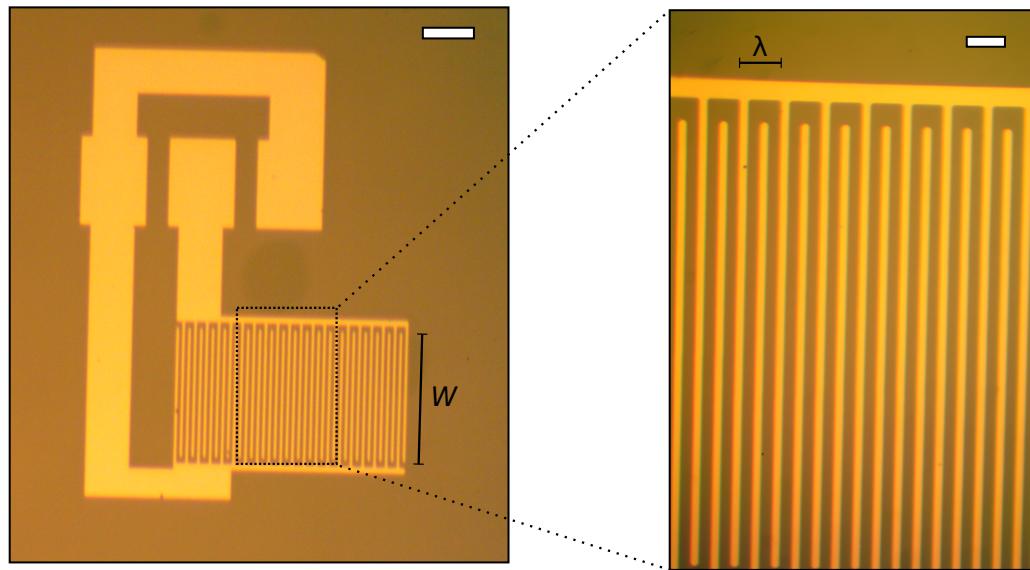


Figure 3.9:

IDT 2. Figure 3.10 (b) shows S11 and S22, and Fig. 3.10 (b) shows S21 and S12.

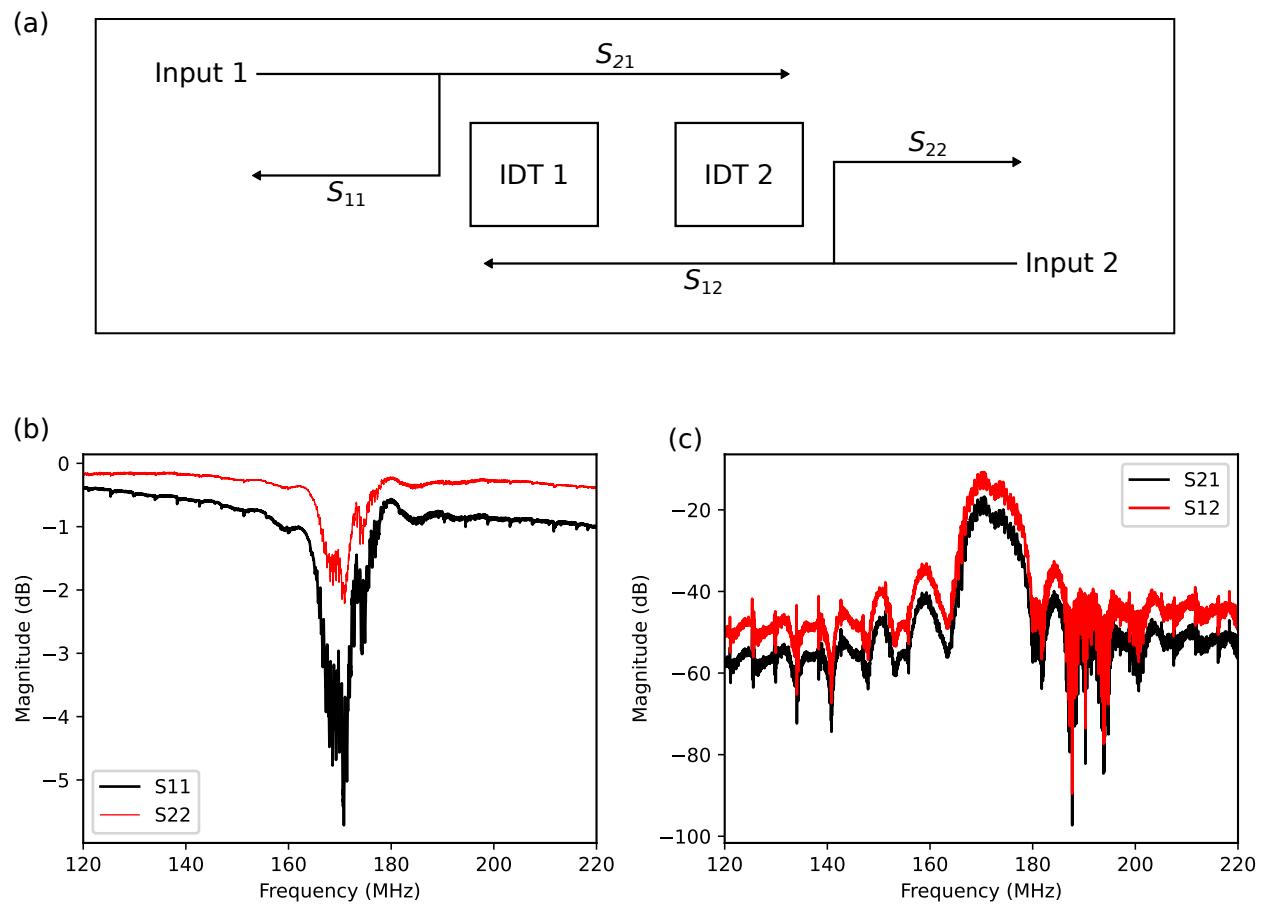


Figure 3.10:

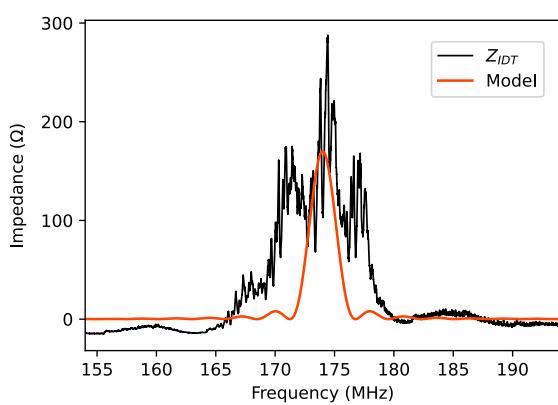


Figure 3.11:

Chapter 4: Acoustoelectric charge pumping in ultra-clean graphene using
surface acoustic waves

4.1 Abstract

4.2 Introduction

4.3 Background

4.4 Experiment design

4.5 Results

4.6 Discussion

4.7 Conclusion

4.8 Supplementary Material

4.9 Nonlinear acoustoelectric effect in graphene

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Chapter 5: Flip-chip design for coupling surface acoustic waves to quantum materials

5.1 Introduction

Lithographic patterning followed by metal deposition is the standard technique to define electrostatic gates; however, the methods of fabricating these devices often involve harsh processing. For example, taking a material to high temperatures — such as during thermal deposition of metals and chemical vapor deposition — can damage sensitive structures by thermal strain (See Appendix on EBL IDT damage from CNT growth processes). Similarly, harsh etching chemicals can introduce impurities and dopants to the surface, affecting electron mobility [2]. Electron-beam lithography can also damage pristine surfaces [64]. To fulfil this need for electrostatically gating a surface while leaving it pristine, the technique of “flip-chip gating” has emerged in recent years [2, 65]. Distinct from the similarly named “flip-chip packaging” technique in semiconductor device processing, flip-chip gating involves flipping the gate chip onto the chip to be gated, allowing a material to be field-effect gated without harsh processing (Fig. 1). This method of flip-chip construction has led to breakthroughs in hybrid quantum systems [66, 67].

The air gap between the gate chip and nanomaterial to be gated is of paramount importance for flip-chip devices. As the flip-chip spacing d increases, a capacitive electrostatic gate decreases in strength as $1/d$, and as mentioned in ??, most of the energy in a SAW’s

periodic potential is contained within one SAW wavelength of the surface. As we build higher-frequency SAW devices to interface with nanomaterials, such as for creating quantum pumps that output higher-magnitude quantized current, our flip-chip's spacing becomes increasingly important. However, most prior works don't ensure parallel mounting nor directly measure their flip-chip's spacing [66, 67, 68], with one work estimating their air gap using capacitance [2], and another roughly estimating their air gap by comparing to similar non-flip-chip devices [68]. In this chapter, I present a flip-chip platform that does not rely on external mounting pressure, and allows for characterization of the flip-chip air gap in multiple areas to determine parallel mounting. Instead of springs or tension arms, my design uses hard-cured varnish and etched Si spacers to hold a precise air gap. I benchmark this platform by building a flip-chip capacitor using photolithography, deep reactive ion etching (RIE), and a homebuilt flip-chip assembly station. I verify the spacing between the two chips with two independent methods — capacitance, and reflectance spectroscopy — and evaluate the feasibility of a flip-chip without external mounting pressure.

5.2 Measuring flip-chip spacing using interference spectroscopy

The first method I use to measure the air gap between two chips is interference spectroscopy. Using a laser with a spot size $< 1 \text{ mm}$, I can not only measure the central air gap, but probe various spots on the flip-chip to determine if the two chips are parallel. Figure 5.2 shows the optical setup used in the interference spectroscopy measurement.

To correct the reflectance spectrum for wavelength-dependent power fluctuations and substrate effects, I measure a reference spectrum using a bare Si substrate, then subtract

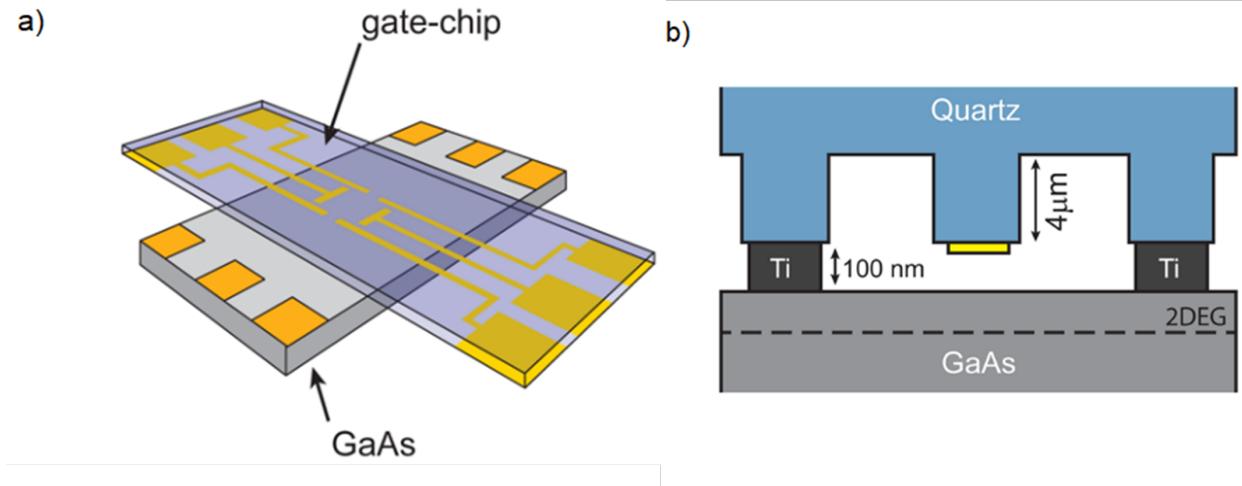


Figure 5.1: Flip-chip design from [2]. (a) The upper gate-chip is printed on quartz to allow alignment with the lower GaAs chip. The lower chip's gates are attached by micro soldering to preserve the pristine GaAs surface's ultrahigh electron mobility. (b) Side view of the stacked chips. The gate (yellow) and GaAs are separated by 100 nm using patterned Ti posts.

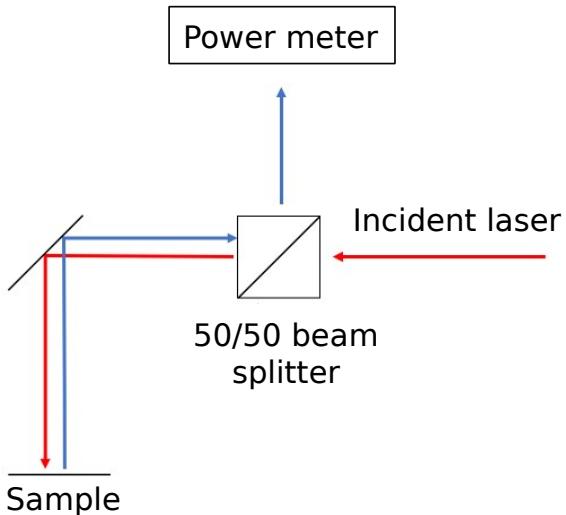


Figure 5.2: The interferometer setup used to measure the reflectance of a sample. Incident wavelength is scanned using a Labview-controlled monochromator and plotted against measured reflected power. The colors indicate incident light (red) and reflected light (blue).

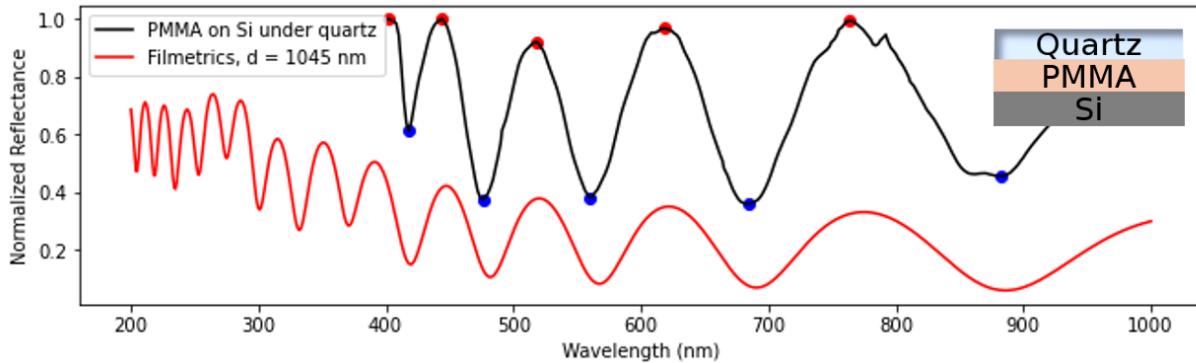


Figure 5.3: Corrected measured reflectance of a Si-PMMA-quartz stack compared to the Filmetrics reflectance calculation with 1045 nm-thick PMMA.

this reference spectrum from the measured interference spectrum. Then, I determine the flip-chip air gap by hand-fitting to a model spectrum calculated with Filmetrics's online thin-film modelling calculator.

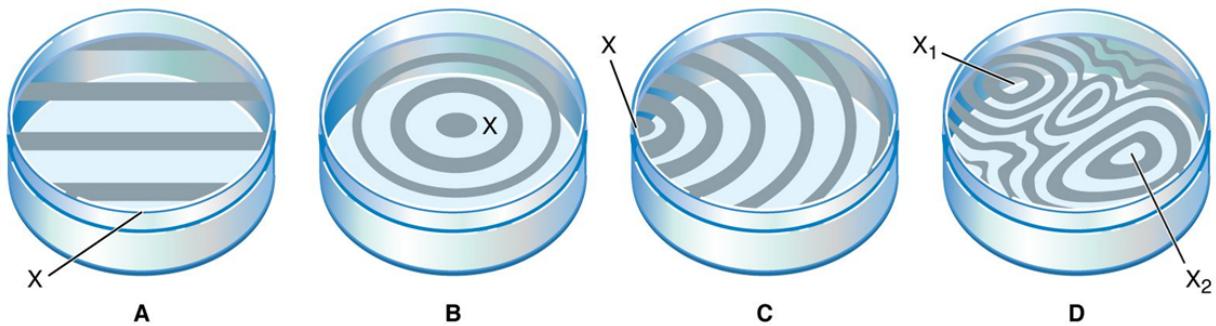
As a first test, I spun a PMMA 495 A11 solution on a Si chip at 2500 RPM for 60 seconds. According to the manufacturer's spin curves, the PMMA layer should be ≈ 1000 nm thick. Then, I used the process described in 5.3 to glue a quartz chip on top to create the Si-PMMA-quartz stack shown in the inset of Fig. 5.3. Figure 5.3 shows the corrected reflectance spectrum of this Si-PMMA-quartz stack versus the reflectance calculated with the Filmetrics model.

The peaks and troughs of the measured reflectance spectrum are consistent with a PMMA thickness of 1045 nm, close to the predicted spun PMMA thickness, verifying the validity of this method.

5.3 Flip-chips with no spacers

Figure *** shows a diagram of my home-built flip-chip assembly station. I designed the holder arm with a “tuning fork” structure (Fig. *** b) which allows me to look through the quartz chip to align structures on the top and bottom chips. For all the flip-chips described in this chapter, I used the following assembly process: To create the top and bottom chips, I coated fused quartz and bare p-doped Si wafers (University Wafer) with S1813 photoresist to protect them during the dicing process, then diced the Si into 7 mm × 12 mm rectangles and the quartz into 4.5 mm × 12 mm rectangles using a DISCO DAD 3220 wafer dicing SAW. Immediately prior to gluing the chips together, I removed the photoresist by soaking in a 60 °C Remover PG bath for 15 minutes, followed by spraying with acetone and isopropyl alcohol and drying with dry N2. Then, I cleaned both chips by submerging them in acetone and rubbing for 20 seconds with a Rubystick T-21 swab to remove any dust [?]. Next, using PDMS strips, (Gel-Pak), I mounted them to the homebuilt flip-chip mounting station as shown in Figure ****.

Figure ?? shows an optical image of a flip-chip during alignment. First, I align the edges of the top and bottom chip to ensure they are perpendicular. Then, I slowly lower the z-stage to bring the chips into contact, watching for interference fringes. As the flip-chip spacing becomes smaller, the interference fringes change. Once the top chip contacts the bottom chip, the spacing will not change as I lower the z-stage, so the interference fringes will remain static. This is how I determine that the two chips are in contact. Once the top and bottom chips are in contact, I glue the two chips together by putting two small beads of GE 7031 varnish at the edges. I hard-cure the varnish using a heat gun at 200 C for



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Figure 5.4: From [3]

5 minutes, holding the heat gun 20 cm from the chip. I also attempted to use photoresist to glue the chips together, as in Ref. [2], but it was difficult to avoid photoresist flowing between the sandwich due to the capillary effect (see Appendix C).

As a first check, a flip-chip's cleanliness can be assessed by viewing the interference fringes (Newton's rings) visible through its quartz top. Figure 5.4 illustrates the pattern of interference fringes expected from different surface topographies. If the two surfaces are parallel, the rings will be parallel (Fig. 5.4 (A)). Similarly, if a large piece of dust comes between the two surfaces, a point with many small concentric fringes will be visible, curving towards the point which the dust bridges the air gap (Fig. 5.4 (B)). This method was used in [68] to confirm that no large dust particles settled between the two sides of their flip-chip.

5.3.1 Smallest achievable air gap

Before attempting to control the air gap between two chips, I first need to determine the smallest air gap that I can achieve between two clean chips. Figure 5.5 (a) shows a flip-chip

constructed from pristine quartz and Si chips using the method described in Sec. 5.3. I performed three interference spectroscopy measurements on this chip — one in the center, and one on each edge — to determine if the chips are mounted parallel to each other.

The air gap measurement confirms that the air gap on one side of the flip-chip is $\approx 1 \mu\text{m}$ larger than the air gap on the other side. Note that the interference fringes curve towards the side with the smallest spacing, as expected. I constructed two other flip-chips with no spacers, and the smallest spacing I could achieve was the $2.4 \mu\text{m}$ side of the flip-chip shown in Figure 5.5. I was not able to determine the exact reason for this limit. When I observed visible dust between the chips, I uncoupled the flip-chip and cleaned the Si and quartz chips. No visible dust is present between the flip-chip shown in Fig. 5.5. However, unseen dust of size $\approx 2.4 \mu\text{m}$ could be present. The air gap limit could also arise from thickness variation over the surface of the quartz and Si wafers. Ref. [68] attributes their minimum achievable flip-chip spacing (fabricated in a class-100 clean room) of 50 to 200 nm to the top and bottom chips not being perfectly flat across the contact area. We did not buy special $< 1 \mu\text{m}$ total thickness variation Si wafers from University Wafer; furthermore, they do not quote the thickness variation of their fused quartz wafers. From these flip-chips with no spacers, I determine $2.4 \mu\text{m}$ to be the lower bound for the air gap that I can reasonably achieve with etched Si spacers, and use this to inform my flip-chip design in the next section.

5.4 Flip-chip capacitor with deep RIE-etched Si spacers

In the previous section, I determined that the smallest spacing that I can reasonably achieve between two pristine chips is $2.4 \mu\text{m}$. However, this does not exclude the possibility of

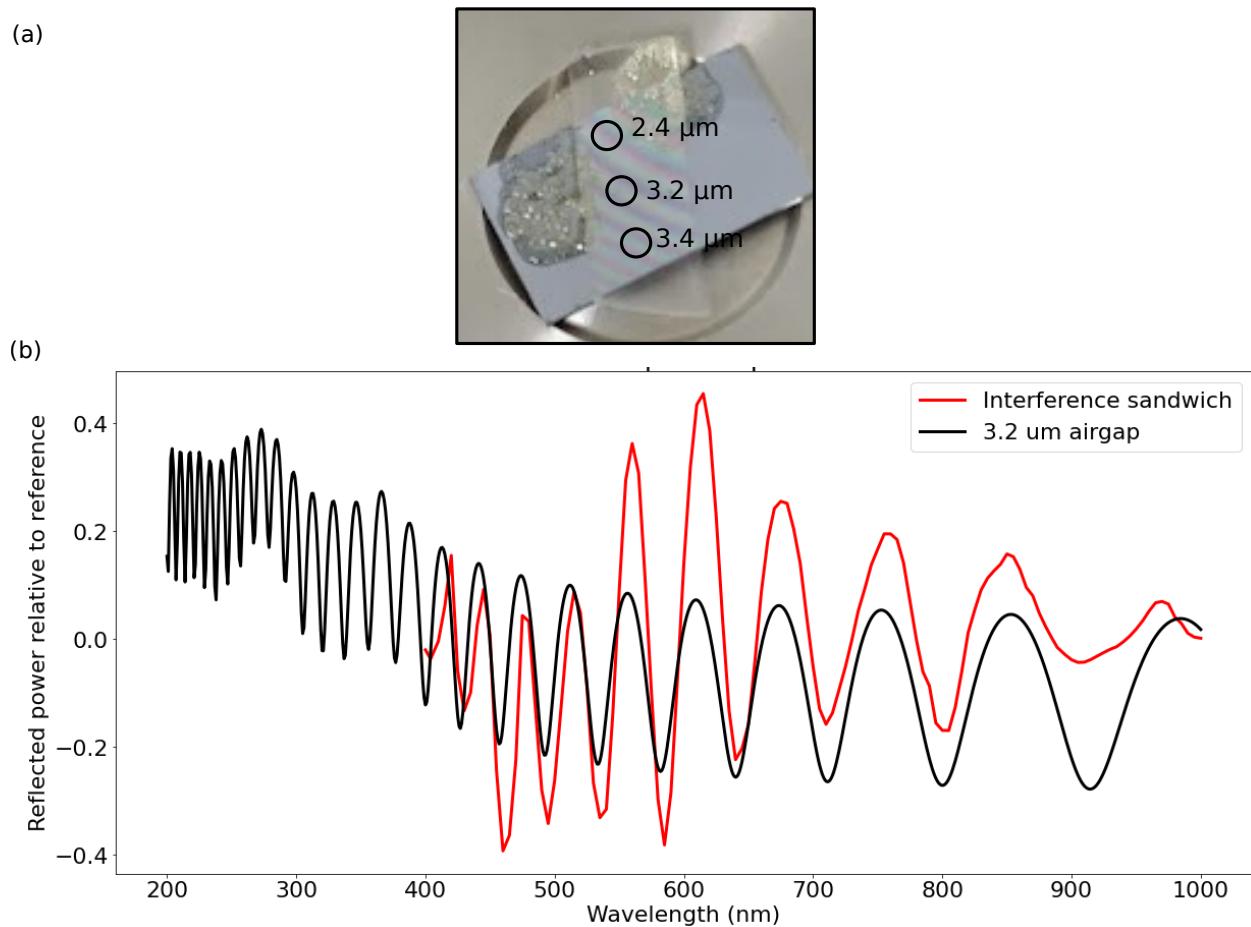


Figure 5.5: (a) A flip-chip with no spacers made from quartz and Si. The three circles indicate the spots at which I directed the laser for interference spectroscopy air gap measurement. (b) The reflectance spectrum from the central spot compared to the Filmetrics model with a $3.2 \mu\text{m}$ air gap.

bringing the gate chip closer to our nanomaterial in a small area while leaving most of the flip-chip spaced by $\geq 2.4 \mu\text{m}$. A two-tier etch has previously been used to achieve a narrow central spacing of $< 1 \mu\text{m}$ while leaving a larger air gap between most of the area of the flip-chip [2]. This reduces the likelihood of dust becoming sandwiched in-between the chips and preventing close spacing.

Figure 5.7 shows the two-tier deep reactive ion etch (RIE) process that I use to create pillars that define the flip-chip spacing. I first print $50 \times 50 \mu\text{m}$ Cr squares with center spacing $360 \mu\text{m}$ and thickness 150 nm on a p-doped Si substrate using photolithography (Figure 5.7 (1)). This Cr serves as an etch mask for the deep RIE. Then, I use the SI etch recipe described in B.4 and an Oxford Plasmalab 100 plasma etch system to etch 460 nm into the Si (Figure 5.7 (2)). This first etch defines the center spacing of the flip-chip. Next, I print the capacitor structure using photolithography and metallization of 150 nm Cr, consisting of a $750 \times 750 \mu\text{m}$ square center pad and $50 \mu\text{m}$ wires that extend to the edges of the chip (Figure 5.7 (3)). I fabricated this same capacitor structure on both the Si and quartz chips (Figure 5.7(b)). The long wires allow me to make electrical contact to the central pad of the capacitor when the two chips are sandwiched together. Then, I etched the final $5 \mu\text{m}$ into the Si (Figure 5.7 (4)). For both Si etches, I determined the exact etch depth using AFM. Figure 5.6 shows the flip-chip capacitor during alignment. I assembled the flip-chip capacitor using the process described in Sec. 5.3.

Figure 5.8 (a) shows the measured reflectance spectra for the left and right side of the flip-chip capacitor. The left side best-matches $(5.00 \pm 0.05) \mu\text{m}$, while the right side best-matches $(6.50 \pm 0.05) \mu\text{m}$. The error denotes the smallest step for which the best hand-fit was obvious. For example, during the fitting process, it was clear that, for the left side,

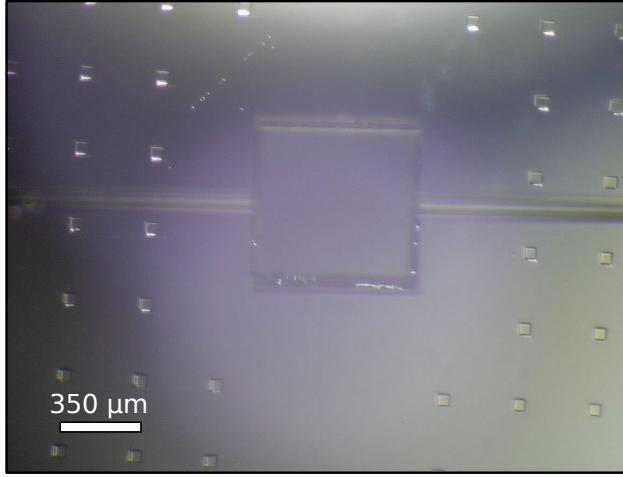


Figure 5.6: View through the microscope camera during initial alignment of the flip-chip capacitor (the top and bottom chips are still far from each other, so no Newton's rings are visible).

$5.00\text{ }\mu\text{m}$ was a better fit than $4.95\text{ }\mu\text{m}$ or $5.05\text{ }\mu\text{m}$. Figure 5.8 (b) shows the schematic of the completed flip-chip capacitor, with AFM measurements of the final structure indicated on the diagram.

Figure 5.8 illustrates that I did not achieve parallel mounting. The left air gap agrees precisely with the etched post height of $(4.950 \pm 0.005)\text{ }\mu\text{m}$; however, the right air gap sits $(1.50 \pm 0.05)\text{ }\mu\text{m}$ taller. The designed center gap is $(0.563 \pm 0.005)\text{ }\mu\text{m}$, from AFM measurements of the posts and central mesa. Therefore, I estimate my flip-chip capacitor spacing to be $(1.313 \pm 0.055)\text{ }\mu\text{m}$ $((0.563 \pm 0.005)\text{ }\mu\text{m} + (1.50 \pm 0.05)\text{ }\mu\text{m}/2)$. Though I did not achieve parallel mounting, this emphasizes the strength of determining the air gap with optical methods. Before mounting the chip, wire bonding, and taking electrical measurements, the air gap of a flip-chip can be estimated, and parallel mounting can be verified. If the estimated air gap is not suitable, or the top and bottom chips are not parallel, the flip-chip can be

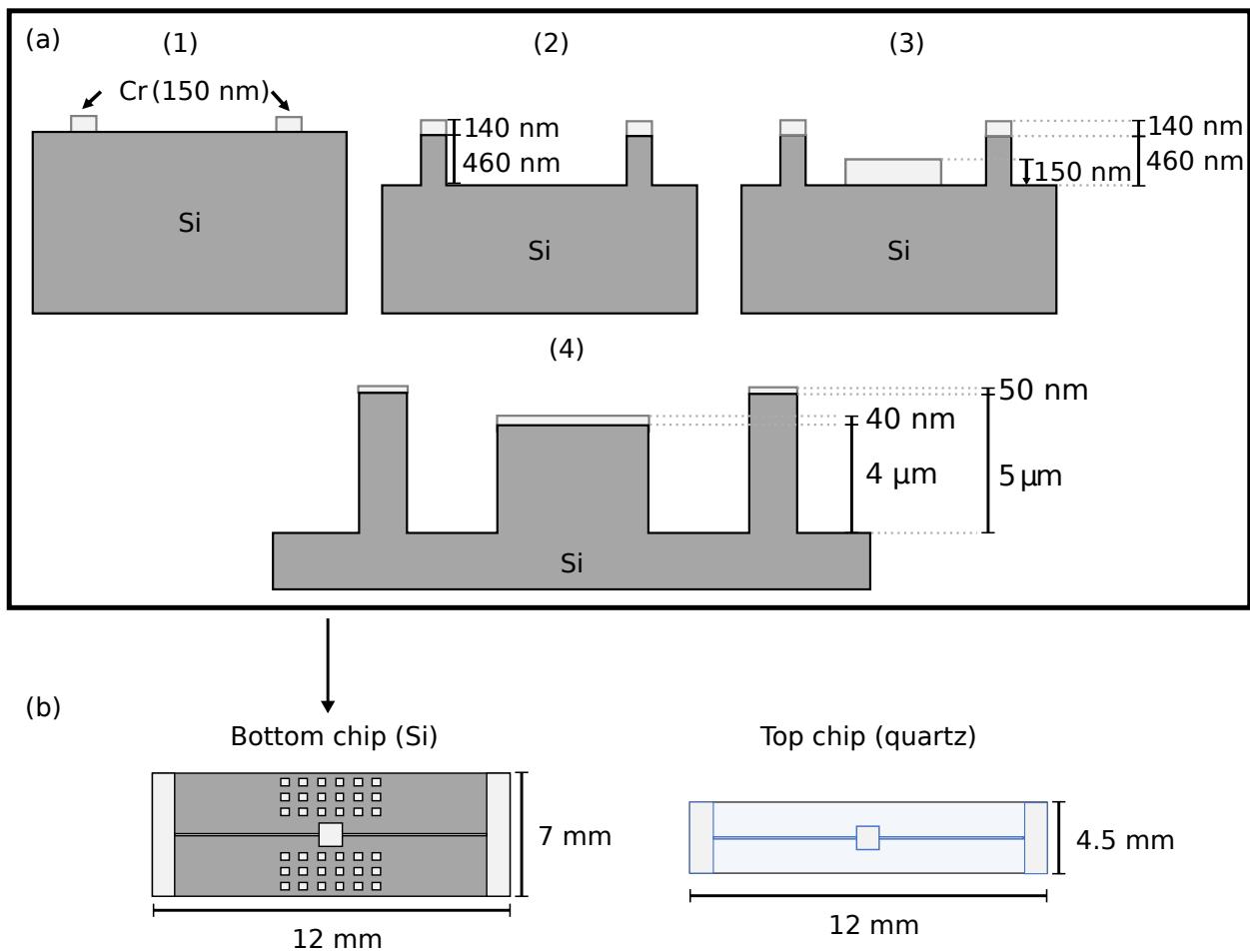


Figure 5.7: (a) Two-tier etch process for defining the center gap and post height of the flip-chip. The denoted measurements are estimated from known Cr deposition rates and known Cr and Si etch rates (see Appendix B.4). (b) The completed top and bottom sides of the flip-chip capacitor, before assembly.

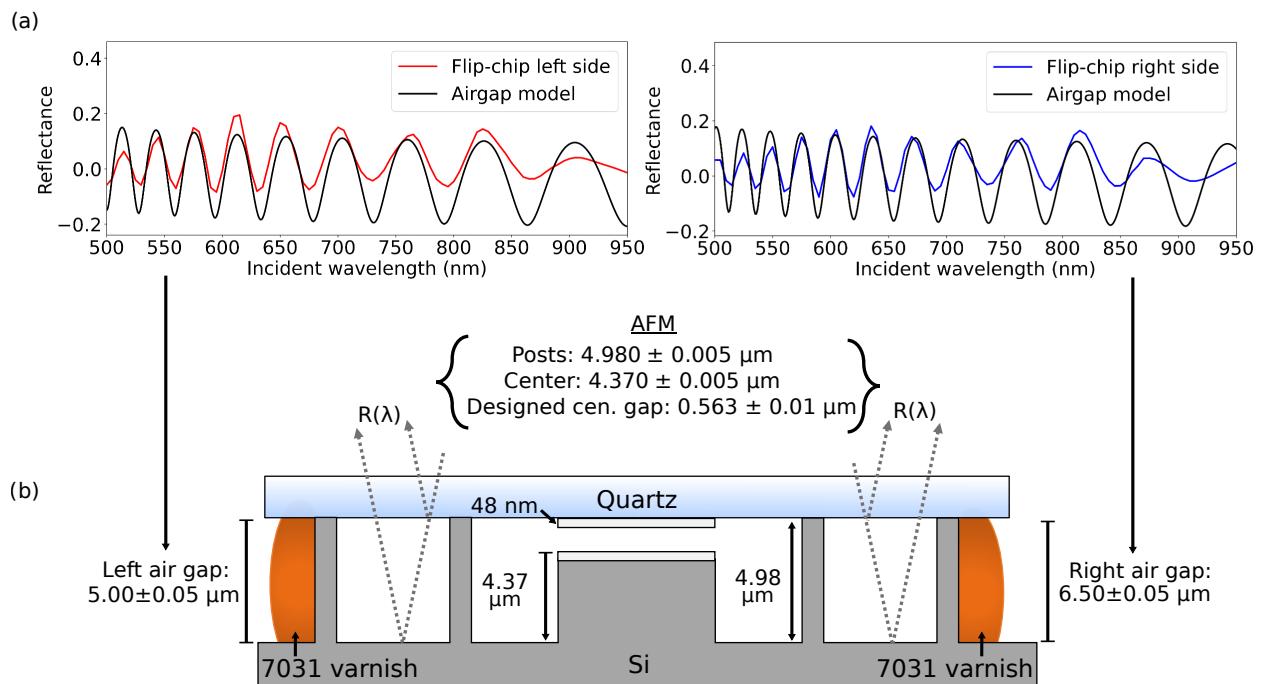


Figure 5.8:

deconstructed, cleaned, and re-mounted (7031 varnish readily dissolves in a solution of 99% ethanol). Then, once a suitable estimated air gap is achieved, a more precise measurement can be made using capacitance.

5.5 Flip-chip air gap measurement with capacitance

The total impedance of my flip-chip capacitor is the sum of the capacitor impedance and series resistance

$$Z = R_s + Z_C = R_s + \frac{1}{i\omega C}. \quad (5.1)$$

Assume an AC signal $V = V_0 \exp(i\omega t)$ is applied to the flip-chip. Then, the current is

$$I = \frac{V}{Z} = \frac{V}{R_s + 1/i\omega C} = V \frac{i\omega C}{1 + i\omega CR} \approx V i\omega C(1 - i\omega CR) = V(RC^2\omega^2 + i\omega C), \quad (5.2)$$

where $C = \epsilon_0 A/d$ is the capacitance of the flip-chip, and I assume that the resistance is small, so $\omega CR \ll 1$. The measured current is then the real part of Eq. 5.2,

$$I = V_0 \omega^2 R C \cos(\omega t) + V_0 C \omega \sin(\omega t). \quad (5.3)$$

Therefore, by applying an AC signal to the flip-chip capacitor and measuring the sine component of the resultant current, the distance between the flip-chip capacitor plates can be determined using $d = 2\pi f \epsilon_0 A V_0 / I$.

Figure 5.9 (a) shows the experimental setup that I use to measure the capacitance of my flip-chip. I use a Stanford SR58 lock-in amplifier to apply a signal of $V_0 = 100$ mV at

$f = 200$ Hz and measure the sine component of the resultant current. Figure 5.10 shows a schematic and photograph of the completed flip-chip capacitor.

Figure 5.9 shows the results of the capacitance central air gap measurement. To determine the effect of mounting pressure, I measured the capacitance in three scenarios: applying no force, applying force on either edge of the flip-chip, and applying force in the center of the flip-chip (directly on the capacitor plates). With no mounting pressure, I determined the central air gap to be (1.33 ± 0.01) μm , which is in very good agreement with the estimated central air gap from reflectance spectroscopy of (1.36 ± 0.06) μm determined in Sec. 5.4. When applying edge force to simulate mechanical mounting pressure, the air gap closed to (0.688 ± 0.010) μm , which is close to the designed air gap defined by the etched posts (measured with AFM to be (0.563 ± 0.010) μm). Applying a strong enough central force short-circuits the capacitor plates.

Figure 5.11 shows the geometry of the bent quartz chip when applying a central force to the flip-chip capacitor, short-circuiting the top and bottom chips. The bend is greatly exaggerated. Assuming that the quartz chip bends directly at the Si posts, it bends by (0.563 ± 0.010) μm over 1 mm, corresponding to a bending radius of 0.22 m (assuming the bend forms an arc). Therefore, the strain in the quartz is $0.85 \text{ nm} / 1 \text{ mm} = 8.5 \times 10^{-5}\%$.

5.6 Conclusions

In this section, I built a flip-chip capacitor by sandwiching patterned quartz and etched Si chips together with hard-cured varnish. I used two independent methods to characterize the gap between the two chips — interference spectroscopy (“the optical method”) and

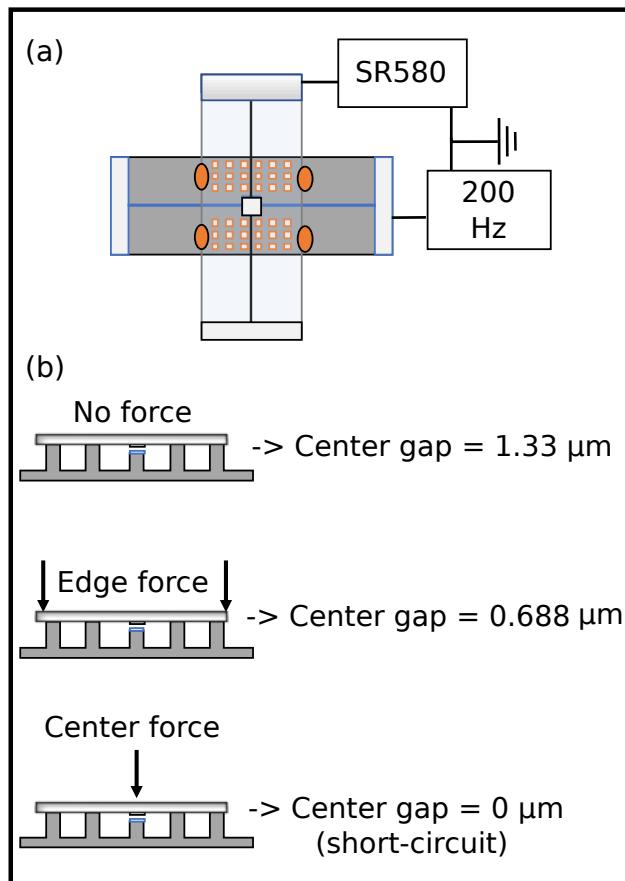


Figure 5.9: (a) schematic of the capacitance measurement. (b) Dependence of central air gap modulation with respect to location of applied mounting pressure. The edge force was applied onto the quartz chip, above the etched spacers closest to the edge of the Si chip. The central force was applied directly above the capacitor pads.

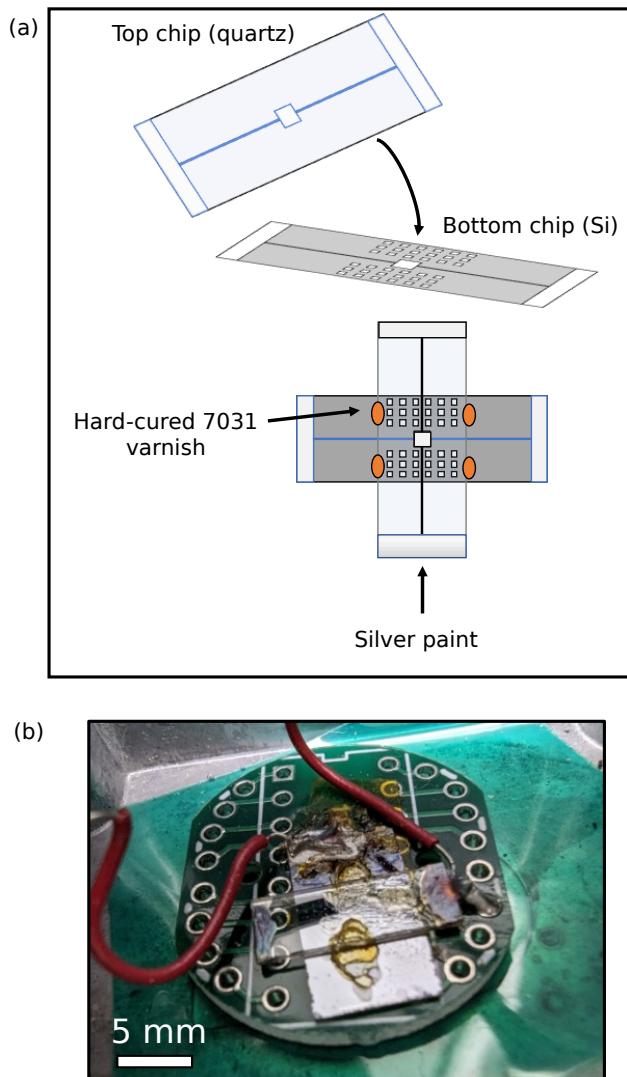


Figure 5.10: (a) Schematic of the completed flip-chip capacitor. (b) Optical image of the completed flip-chip capacitor. Wires are seen soldered to the silver paint, making electrical contact to the top and bottom chips.

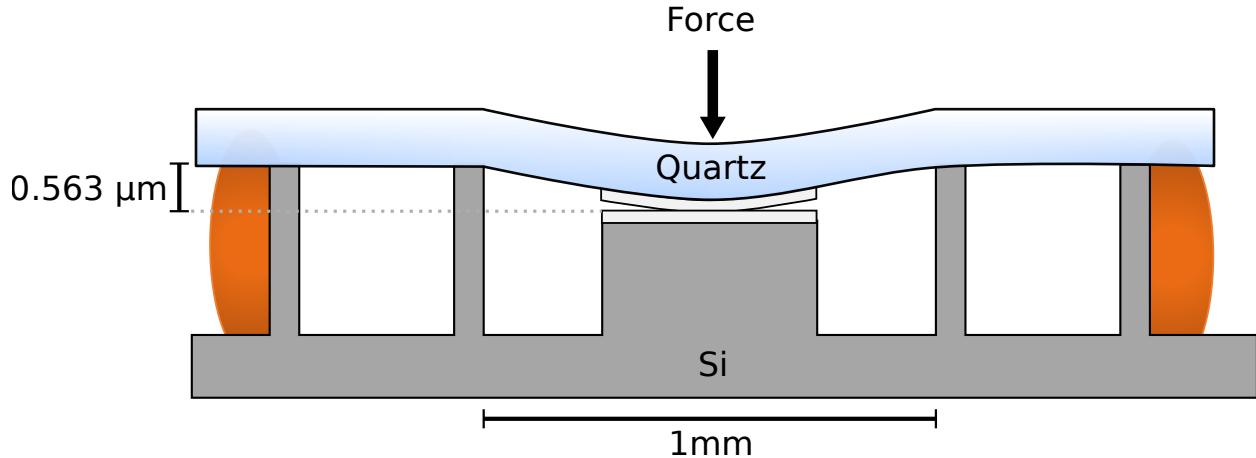


Figure 5.11: Geometry of the bent quartz chip with a centrally-applied force that short-circuits the top and bottom capacitor pads.

capacitance. Combining both methods allows for a complete characterization of the flip-chip air gap at multiple locations, and a precise measurement between the gate chip and quantum material to be gated. The optical air gap measurement is useful for quick determination of the air gap before spending time wire bonding the chip and mounting it in a cryostat. Prior reports of flip-chip devices did not use optical methods to measure their flip-chip spacing [2, 66, 67, 68]. Using this optical method, I found that I was not able to achieve parallel mounting without external mounting pressure, likely due to the arm of my homebuilt assembly station not being perfectly level, leading to uneven mounting pressure. This is in agreement with the Si-quartz sandwiches that I created without patterned spacers (Sec. 5.3.1), in which I noticed that one side was always $\approx 1 \mu\text{m}$ higher than the other, as measured using interference spectroscopy. Conversely, the capacitance measurement requires electrical contact to the chip, but can measure the air gap more precisely. The central spacing that I measured with capacitance (Fig. 5.9) in the cases of no mounting pressure and edge mounting

pressure are in good agreement with the flip-chip geometry determined by AFM and optical measurement (Fig. 5.8). When I applied mounting pressure to the central capacitor pads, I was able to bend the quartz chip by $(0.563 \pm 0.010) \mu\text{m}$ and short-circuit the capacitor pads. This suggests the possibility of measuring the air gap of a flip-chip inside a cryostat and tuning the air gap in-situ. Future flip-chip devices could be designed with a capacitive pad in multiple locations on top and bottom chips. Then, A motorized stage inside the cryostat, such as in [69], could be used to apply mounting pressure to the flip-chip while measuring the capacitor array to minimize the air gap and maximize the strength of coupling between the SAW gate and quantum material.

Chapter 6: Conclusion

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APPENDICES

Appendix A: Limitations of quantized charge pumps based on tunneling

Appendix B: Recipes

B.1 Photolithography recipe

1. Cleanly pipette enough LOR 3A photoresist to cover the substrate. Spin at 4000 RPM for 45 seconds.
2. Bake at 180 C for 4 minutes
3. Cleanly pipette enough S1813 photoresist to cover the substrate. Spin at 4000 RPM for 30 seconds.
4. Bake at 120 C for 2 minutes
5. Edge bead removal: The edges of the chip will have built-up photoresist that is many times thicker than the rest of the chip. Edge bead removal is particularly important for fine features on small substrates, as edge beads prevent the chip from fully contacting the mask. Try putting a tiny amount of Remover PG on the tip of a clean swab, such as a small square of cleanroom wipe, then swab your edges at a 45-degree angle to remove edge beads.
6. Expose chip for 12 seconds at 6 mJ/cm^2 .
7. Develop for 100 seconds in AZ-300 MIF developer
8. Rinse with DI water and blow dry with N_2 .

B.2 Force curve instructions

The following began as an excerpt from the Minot Lab wiki. I later updated it for the modern version of the MFP-3D software.

Static force curves allow you make graphs of deflection versus tip height for single pushes onto a sample. There is a calibration process that is necessary to make these measurements accurate.

Start with the tip far away from the surface to measure virtual deflection. If you don't, the tip will crash into the surface because the trigger channel is set to "none" by default.

Calibrating the measured deflection is a two part process: First, with the Trigger Channel left at "none" and all other options left at their default values, press the Single Force button near the bottom of the Master Panel. A new window should open with a noisy red and blue graph that looks linear. This line is the virtual deflection. In the "Cal" tab open the "Set Sens." dropdown list and click on "Virtual Defl Line". A black line will appear on the force vs displacement graph. The program automatically records these fit parameters in the virtual deflection box in the "Cal" tab. Virtual deflection is now calibrated.¹

Next, you will engage the surface with the tip. In this step, you will calibrate the Deflection InvOLS, or Inverse Optical Lever Sensitivity. It is the sensitivity of the detector-cantilever combination, which lets you relate deflection to an actual force value. (It's the inverse because the bigger the number, the less sensitive the detector is.)

¹'Virtual deflection' is a change in deflection as a function of height which is due to tiny changes in the optical path of the laser throughout the Z range. Virtual deflection should not be confused with 'squeeze-film damping', which is a reduction in free-air amplitude as the tip is lowered toward a surface. Squeeze-film damping arises due to air that becomes 'trapped' between the cantilever and the sample, thereby applying extra forces to the cantilever as it oscillates. Squeeze-film damping is observed only in the close vicinity of a sample, whereas virtual deflection can be observed in the absence of a sample.

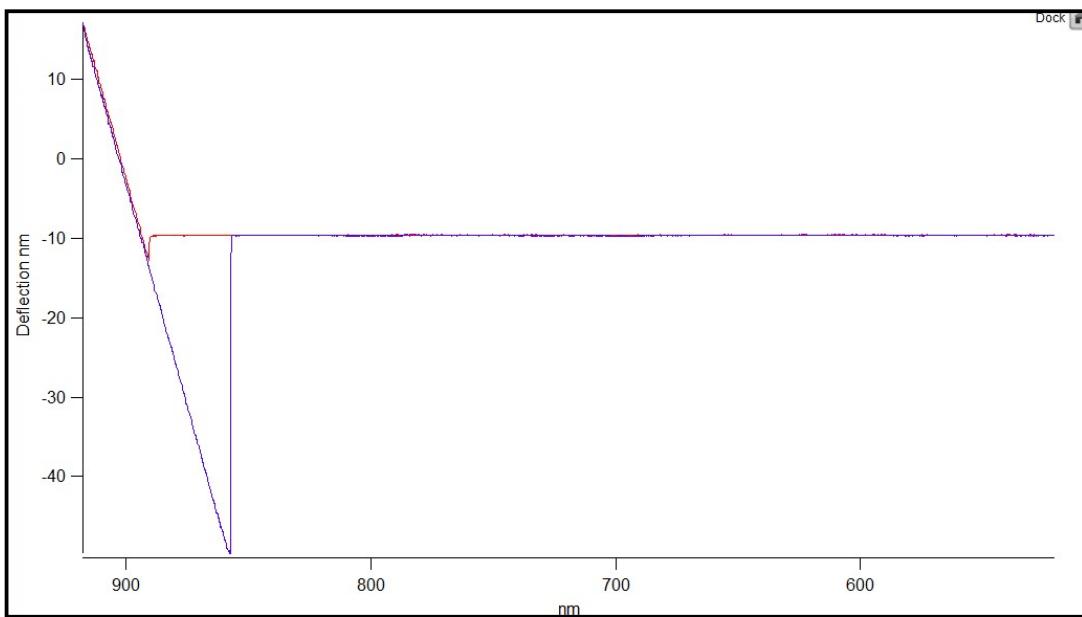


Figure B.1: A force curve for a dirty AFM tip. The colors indicate engaging (red) and retracting (blue) the AFM tip.

In the Trigger Channel dropdown list choose “Deflection” and set the trigger point to 20 nm. Press “Single Force”. The first graph you see will have a lot of extraneous data as the tip finds the surface. After the tip has reached the deflection trigger point, it will disengage and retract a small distance from the surface. A clean tip should produce a deflection curve that looks like a backwards checkmark. The red and blue (engage/retract) lines should lie very near to one another. Figure B.1 shows a force curve for a dirty tip, where the engage/retract lines do not overlap.

Next, with the graph window selected, press CTRL+I to bring up the cursors. Place the cursors (circle and square objects that pop up at the bottom of the window) on the left part of the graph where the tip is pressing against the surface, selecting a representative portion of the line. (The line of interest is the far left linear line with a negative slope) Make sure

the cursors are on the same line. Do this by pressing the left/right arrow keys. If the cursors are on the same line they will move in the same direction.

Select “Deflection InvOLS” from the “Set Sens.” dropdown list. The program automatically records the offset in the “Defl InvOLS” box. Click “Withdraw”. You are now done calibrating the Deflection.

To measure the AFM tip’s spring constant: First, set the deflection to zero using the left-side thumb wheel on the AFM head. Click the Thermal button on the right side of the Master Panel and click the Capture button at the top left of the Thermal Graph window. This will bring up the thermal graph. Allow it to collect at least 100 samples.

There should be a spike in the graph that corresponds to your driving frequency. Ensure that this makes sense from your tuning parameters — lower-frequency peaks can appear as well. Use the mouse to drag a box around this peak and expand it through the right click menu. When the peak is well-defined press “Stop Thermal”. Click the Fit button. A blue line will now fit to the peak. If the fit looks good, continue. The Spring Constant of the cantilever is now measured and updated in both the Thermal and Main tabs.

Now, you can use the measured spring constant to convert between your desired force and deflection in nm. You can use the Force Curve dialog box to convert between deflection in nm and deflection in volts. This deflection voltage is your desired set point.

B.3 Comparison between EBL and photolithography process on LiNbO₃

- **EBL process for encapsulated graphene FET on LiNbO₃ with edge contacts:**
 - Transfer encapsulated GR onto substrate

- Spin EBL resist
 - Deposit charge dissipation layer (thin Al)
 - Exposure (edge contact etch)
 - Etch Al
 - Develop resist
 - RIE etch for edge contacts
 - Spin EBL resist
 - Deposit Al
 - Exposure (contact metal)
 - Etch Al
 - Deposit S/D contacts
 - Spin EBL resist
 - Deposit Al
 - Exposure (gate contact)
 - Etch Al
 - Deposit gate contact
- **Photolithography process for graphene FET on LiNbO₃:**
 - Spin photoresist
 - Print S/D contacts

- Deposit S/D contacts
- Transfer encapsulated GR onto substrate
- Spin photoresist
- Print gate contact

B.4 Si RIE recipe

- SF₆: 14.0 sccm
- CHF₃: 35.0 sccm
- 100 W RF power
- Chamber pressure = 10 torr
- Si Etch rate: 40 nm/min
- Cr etch rate: 0.8 nm/min

Appendix C: Additional flip-chip tests

I initially tried to use photoresist as spacers for flip-chip construction, following the work of [68]. However, I found that the minimum spacing I could achieve was greater than a single layer of spun S1813 photoresist ($\approx 1500\text{ nm}$), so I transitioned to using etched Si spacers. Also, the photoresist tended to flow between the flip-chips due to capillary action, so I found that GE 7031 varnish worked much better as glue. Figure C.1 shows my attempts at photoresist-spaced and photoresist-glued flip-chips.

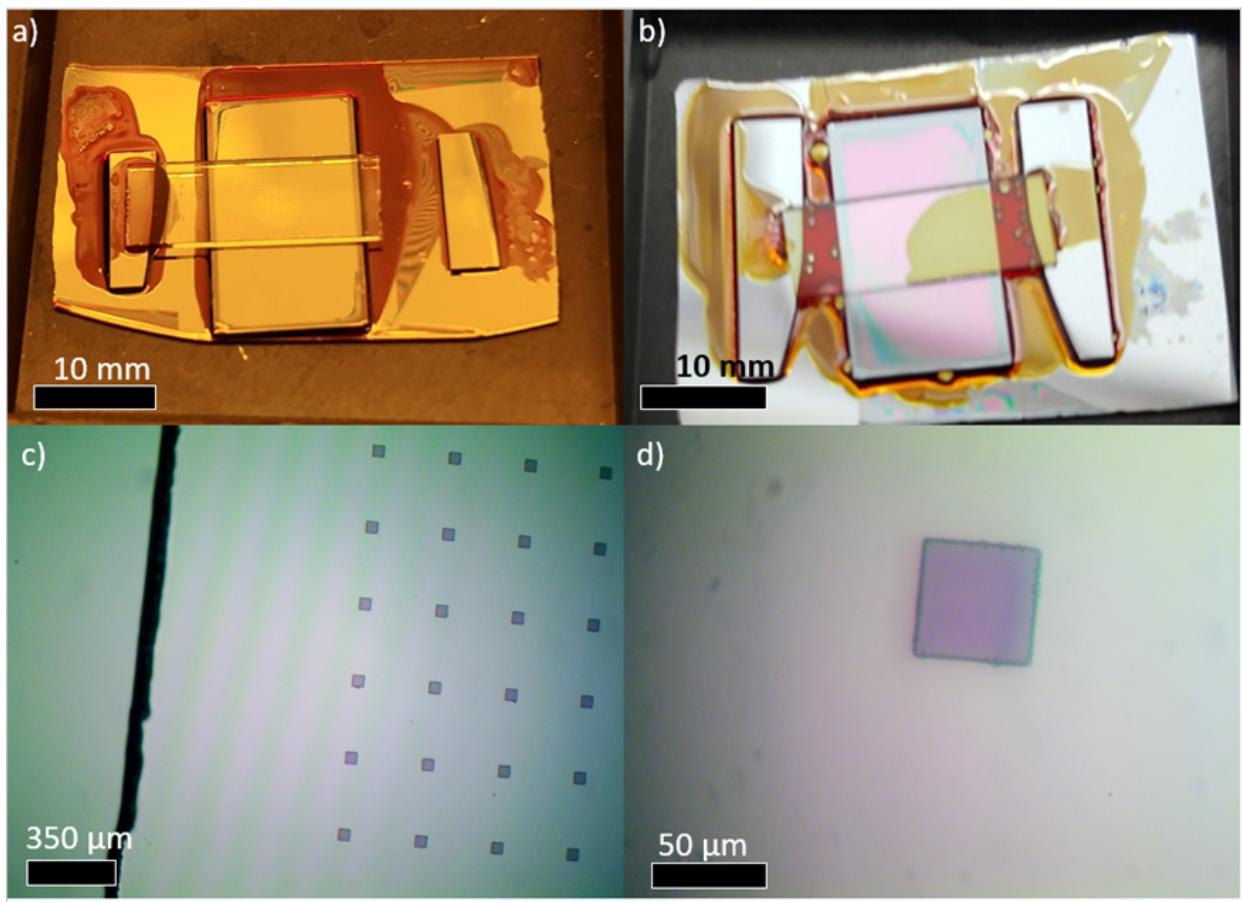


Figure C.1: (a) A flip-chip with sandwiched quartz and Si surfaces separated by a grid of $50\text{ }\mu\text{m}$ -wide squares spaced by $350\text{ }\mu\text{m}$. (b) A flip-chip where the quartz and silicon are separated by $\approx 1\text{ }\mu\text{m}$ micron of spin-coated PMMA. (c) The grid of photoresist squares under quartz during alignment. (d) A single $50\text{ }\mu\text{m}$ -wide square.

Appendix D: Transferred contacts for high-quality contact to 2D
semiconductors

Appendix E: Gate-tunable photoluminescence in h-BN-encapsulated MoS₂

100

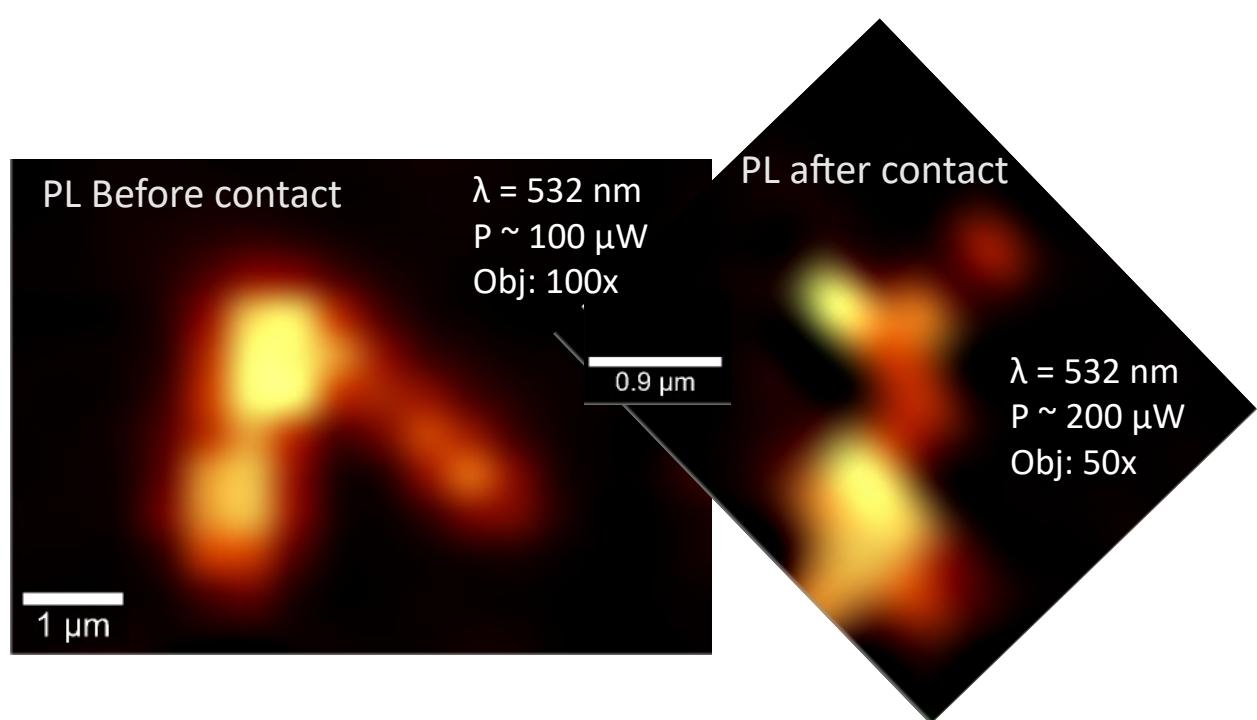


Figure E.1:

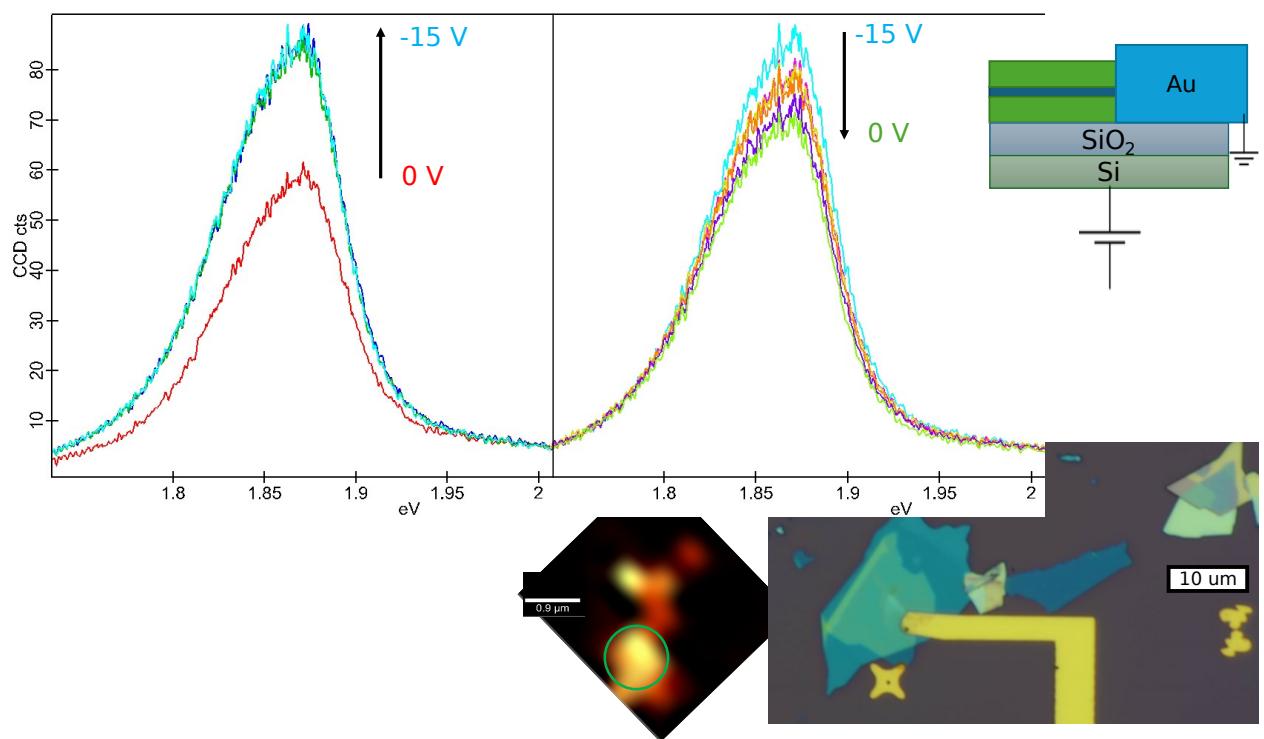


Figure E.2:

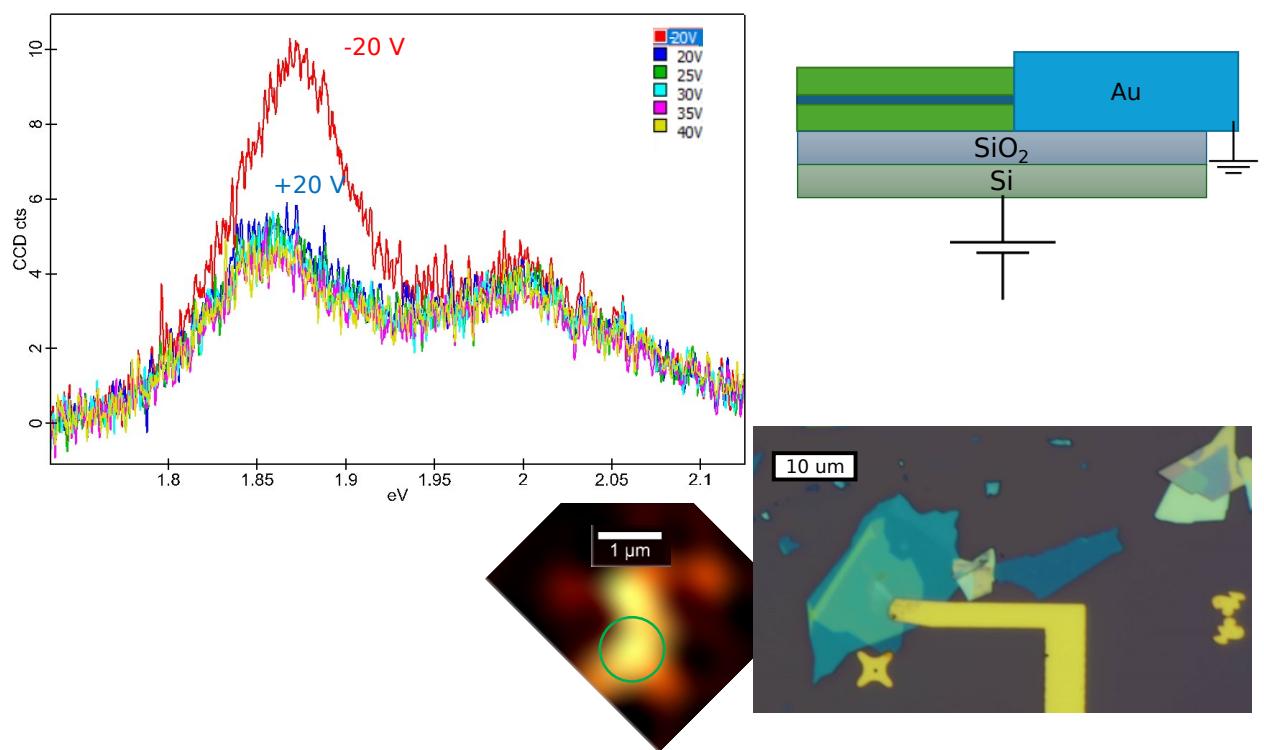


Figure E.3:

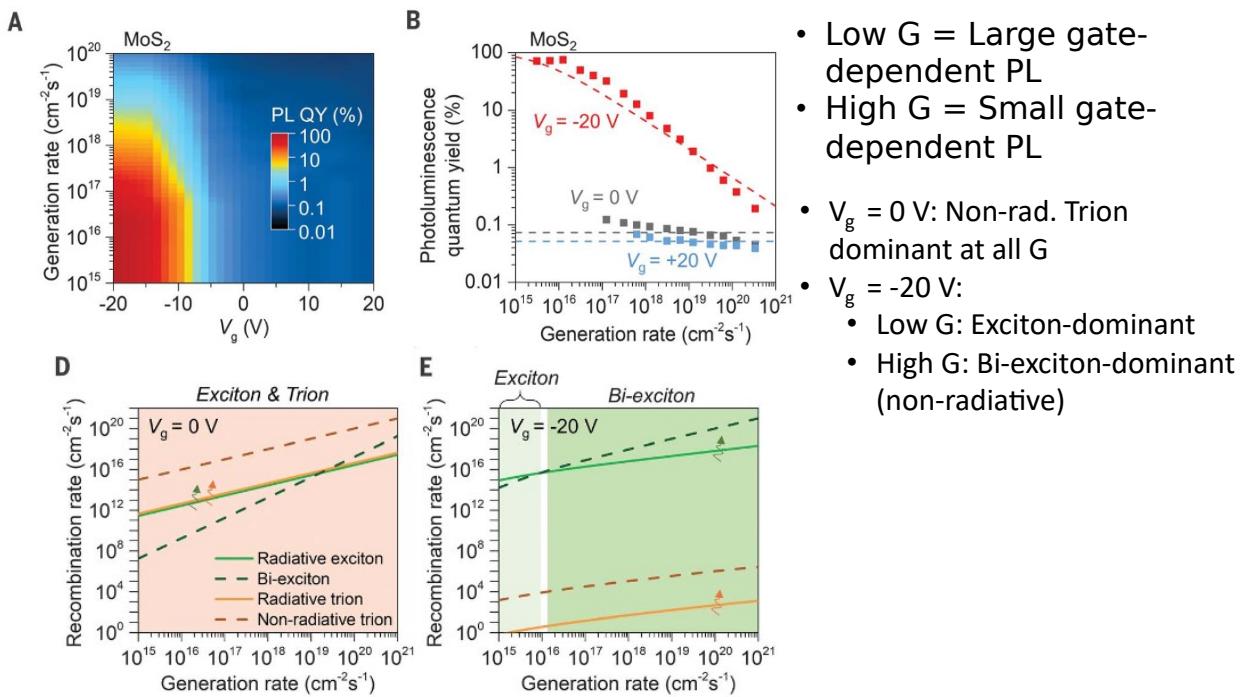


Figure E.4:

