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Dublin M. Nichols for the degree of Doctor of Philosophy in Physics presented on
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Title: Interactions between surface acoustic waves and charge carriers in quantum materials

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Abstract

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Interactions between surface acoustic waves and charge carriers in quantum
materials

by

Dublin M. Nichols

A DISSERTATION

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Dublin M. Nichols, Author

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Chapter 1: Introduction

1.1 Objective

1.2 Background and Motivation

1.2.1 Probing and controlling phenomena in quantum materials

Surface acoustic waves enable novel probes into quantum phenomena which are not accessible using conventional transport techniques. For example, SAWs were recently used to demonstrate that current-induced modifications of bubble and stripe phases in 2D electron systems (2DEs) are a local phenomenon [4]. In contrast to prior transport studies which indirectly probed the voltage drop on the edges of the 2DEs, the authors used SAWs to probe the entire sample at once, gaining new understanding into the effects of external current on highly-ordered electron phases. Another work used a combination of SAWs, microwave excitation, and optical detection to study quantum Hall stripes [5]. By employing SAWs with a wavelength of 60 nm, the authors were able to probe commensurability effects between the SAW superlattice and quantum Hall stripes. A plethora of earlier SAW-based studies provided new insight into the quantum Hall and fractional quantum Hall effect [6, 7, 8, 5, 9] and Wigner crystallization [10]. These works highlight the incredible strength of SAWs for probing phenomena in quantum systems. Building on these successes, researchers have begun to explore the potential of SAWs in the rapidly evolving field of 2D materials.

In 2018, interest in engineered 2D superlattices exploded with the discovery of unconventional superconductivity in twisted bilayer graphene [11]. The birth of the field of “twistronics” added a new knob to turn in the already massive parameter space available for creating bespoke 2D devices. By tuning the twist angle between two sheets of graphene (and thus the periodicity of the moiré superlattice), bilayer graphene can not only exhibit superconductivity, but also correlation-induced insulating states, magnetism, quantized anomalous

Hall states, and many more [12]. In 2D semiconductors, which exhibit exciton dynamics that are of great interest for next-generation electronics, tuning the moiré superlattice provides even more control over the spin and valley degrees of freedom [13]. While graphene has a lattice periodicity on the order of 0.15 nm, the moiré superlattices in twisted devices have much longer periods (tens to hundreds of nm) which are on the order of nominal SAW wavelengths. This congruence opens up the possibility of exploring commensurability effects between moiré superlattices and SAW potentials. Contactless probing using SAWs could also circumvent the challenges of making quality electrical contacts to 2D semiconductors for transport measurements [14]. Hence, SAWs are an ideal tool for contactlessly probing and controlling quantum phenomena in 2D materials. This potential has not gone unnoticed, as evidenced by recent works that have already employed SAWs to great effect, opening new avenues in the probing and manipulation of 2D quantum phenomena.

One phenomenon of interest is interlayer excitons in 2D semiconductor heterostructures. Interlayer excitons are composed of electrons and holes located in different layers in stacks of 2D semiconductors. Harnessing these excitons is exciting for nanophotonics and quantum information applications [15]; however, controlling them is difficult because they are charge-neutral and exhibit no net force under a uniform electric field. Prior works utilized diffusion to transport interlayer excitons, but the transport lengths achievable using diffusion are limited [16, 17]. In a recent work, the authors used SAWs to transport interlayer excitons over incredible distances in bilayer WSe₂ [18]. Given that SAWs transport both electrons and holes in the same direction (See Sec. ****), they can transport neutral excitons much further than the diffusion length. This approach also circumvents the challenges previously identified by other researchers when using local graphene gates [19]. In another work, SAWs

were used as a contactless probe of measuring wave-vector dependent conductivity in ultra-clean graphene, establishing the viability of SAW resonant cavities as a probe for quantum transport phenomena in 2D materials [20]. However, these studies have only scratched the surface of what is possible by interfacing SAWs with quantum materials. Many other SAW-induced phenomena in 2D materials have been theoretically predicted, but not yet achieved experimentally [21]. Therefore, it is imperative to further develop the methods of interfacing SAWs with 2D materials, and to further our understanding of interactions between SAWs and quantum phenomena in 2D materials.

1.2.2 Quantum pumps

1.2.3 Surface acoustic wave sensors

1.3 Outline

Chapter 2: Theory

2.1 Introduction to graphene

2.2 Surface acoustic waves

A surface acoustic wave (SAW) is an elastic wave that propagates along the surface of a material, with its energy confined to a depth of around one wavelength below the surface [22]. When a SAW propagates in a piezoelectric substrate, it mechanically stresses the piezoelectric, generating electric fields. In turn, these electric fields generate strain in the substrate. If we coat this piezoelectric surface with a thin film, the SAW feels and responds to electronic and mechanical properties of the film (in this dissertation the thin film of interest is graphene). This interplay between a SAW and its propagation environment make SAWs interesting for both probing phenomena in quantum materials, such as *insert stuff from intro*, and using quantum materials to probe the environment, such as in gas sensors, humidity sensors.

All of these applications utilize the velocity shift and/or attenuation of the SAW as their sensing tool, which vary depending on mechanical and electronic properties of the thin film coating the piezoelectric surface. Also, in this dissertation, I use SAWs to pump charge through encapsulated graphene. Therefore, I need to develop an understanding of SAW propagation in piezoelectric substrates and the interaction of SAWs with the environment in which they are generated. As we will see, a one-dimensional model of longitudinal SAWs

is sufficient to develop this understanding.

I begin this section with a discussion of elastic waves in bulk non-piezoelectric materials and derive the corresponding wave equation. Then, I discuss waves in bulk piezoelectric materials and explore how the effective stiffness of the piezoelectric substrate varies in cases of very low or very high bulk conductivity. Next, I consider the intermediate conductivity case and derive the bulk conductivity-dependent attenuation and velocity shift equations. Finally, I discuss how the velocity shift and attenuation change when the conductivity is located in a thin film on an insulating piezoelectric surface, and how the attenuation drives a DC acoustoelectric current in the thin film. This sets the stage for the later Sec. 4.6, where I modify these equations to consider mixed-carrier transport in graphene. The discussion in this section follows that of Refs. [23, 24, 1], except where noted by additional references.

2.2.1 Elastic waves in non-piezoelectric materials

To understand the propagation of SAWs in piezoelectric materials, we must first understand the constitutive equation of waves in bulk elastic materials. The constitutive equation relates the displacement of an internal element of this elastic material, known as “strain” (a dimensionless quantity), to the internal forces which caused the strain, known as “stress” (dimensions of force per unit area). The relationship between stress and strain determines how elastic waves propagate. Consider an infinitesimal element dx which is deformed to a length $du+dx$ (Fig. 2.1). Strain, denoted by S , is defined by the local change in displacement du relative to the original length dx ,

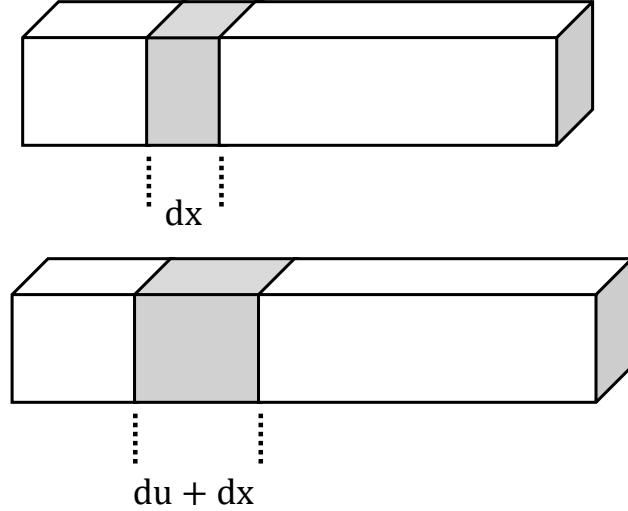


Figure 2.1: A one-dimensional illustration of an element which deforms from length dx to $du + dx$.

$$S = \frac{\partial u}{\partial x}. \quad (2.1)$$

This is a one-dimensional model, so we do not consider shear strains. Stress, denoted by T , is related to strain by the constitutive equation

$$T = cS, \quad (2.2)$$

where c is the stiffness coefficient, also known as Young's modulus. This is a generalization of Hooke's law, with a linear relationship between strain and stress. Stress T is related to du by

$$\frac{\partial T}{\partial x} = \rho \frac{\partial^2 u}{\partial t^2}, \quad (2.3)$$

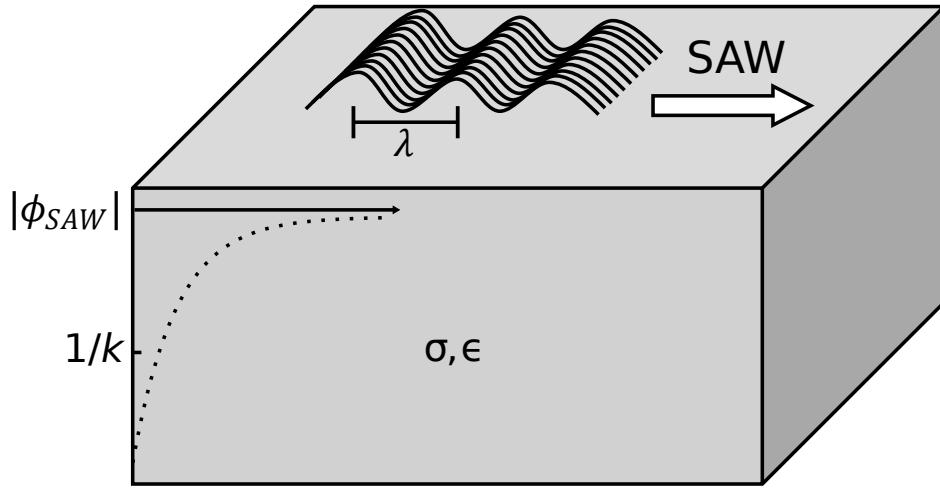


Figure 2.2: A surface acoustic wave travelling in a bulk piezoelectric material. The SAW amplitude $|\phi_{SAW}|$ is well-known to decay approximately exponentially into the surface, with most of its energy contained within a depth $1/k$ [1].

where ρ is the mass density of the material. From these relations, we get an equation for waves in elastic materials

$$\frac{\partial^2 u}{\partial t^2} = \frac{c}{\rho} \frac{\partial^2 u}{\partial x^2}, \quad (2.4)$$

from which we can readily see that plane waves propagate in this elastic material with a velocity $v_0 = \sqrt{\frac{c}{\rho}}$. This is familiar from travelling acoustic waves in a string: as stiffness increases, waves propagate more quickly, and as mass density increases, waves propagate more slowly. In piezoelectric materials, this intuition holds, with one caveat: the effective stiffness of a piezoelectric material depends on more than just its mechanical properties.

2.2.2 Waves in bulk piezoelectric materials

Consider a surface acoustic wave with wave vector k propagating in a bulk piezoelectric material with conductivity σ and dielectric permittivity ϵ , shown in Fig. 2.2. In a piezoelectric material, strain creates displacement fields (D -fields), and electric fields create stress. This translates to new constitutive equations for waves in piezoelectric materials. For small displacements u , these are

$$D = eS + \epsilon E \quad (2.5)$$

and

$$T = cS - eE, \quad (2.6)$$

where e is the piezoelectric constant (assumed here to cause electric fields only in the x -direction), c is the elastic constant at constant electric field, and ϵ is the dielectric permittivity at constant strain. Remembering the definition of displacement field $D = \epsilon E + P$, where P is polarization, we can see from Eq. 2.5 that the strength of polarization in piezoelectric materials scales with the piezoelectric constant e , and strain creates a polarization $P = eS$. Equation 2.6 can be thought of as the same generalized Hooke's law from Eq. 2.2, but with additional stress $-eE$ arising from the piezoelectric effect.

We are interested in the interaction of SAWs with conducting films, and Eqs. 2.5 and 2.6 do not include conductivity (denoted here by σ). To introduce the effect of conductivity on the constitutive equations, I first consider limiting cases of very high σ and very low σ . In a piezoelectric material with $\sigma = \infty$, $E = 0$ because the material can screen all internal

electric fields. The piezoelectric equations of state reduce to

$$T = cS \quad (2.7)$$

and

$$D = eS. \quad (2.8)$$

In this case, our wave velocity is $v_0 = \sqrt{c/\rho}$ (unchanged from before), and the elastic wave propagates in tandem with D -fields. This case of a material with very high conductivity is framed by Wixforth et al. as “a material that [to the elastic wave] appears to be non-piezoelectric” [1].

The next limiting case is that of very low conductivity ($\sigma = 0$). In this perfect piezoelectric insulator, there is no free charge, so Poisson’s equation requires that

$$\partial D / \partial x = 0. \quad (2.9)$$

Rearranging Eqs. 2.5 and 2.6, we find that the wave equation for our piezoelectric insulator is

$$\frac{\partial^2 u}{\partial t^2} = \frac{c}{\rho} \left(1 + \frac{e^2}{2c\epsilon}\right) \frac{\partial^2 u}{\partial x^2}. \quad (2.10)$$

Defining $c^* = c(1 + e^2/c\epsilon)$, this describes a wave travelling at a velocity $v^* = \sqrt{c^*/\rho}$. The piezoelectric interaction has caused our effective elastic constant to increase by a factor $e^2/2c\epsilon$! This quantity is known as the “piezoelectric coupling constant”, denoted $K^2 = e^2/c\epsilon$, which represents the ratio of coupled piezoelectric energy to total stored energy. “Total

stored energy” includes energy stored both in the D-fields (scaling with ϵ) and in mechanical deformation (scaling with c).

K^2 varies widely between materials, ranging from 6.4×10^{-4} in GaAs [1] to 0.05 in LiNbO₃ [25]. Stronger piezoelectric interactions (increasing e) stiffen the material; conversely, a stronger dielectric (increasing ϵ) softens the material. This effective increase in elastic constant from piezoelectric interactions is known as “piezoelectric stiffening” and has important consequences for interactions between SAWs and charge carriers in thin films, as will be seen shortly.

Next, we tackle the case of intermediate σ — acoustic waves in a piezoelectric semiconductor. In this dissertation, acoustic waves in a piezoelectric semiconductor are particularly interesting because the physics is similar whether σ is contained in the bulk piezoelectric or a thin film (like graphene) on an insulating piezoelectric. The current density J in a semiconductor is the sum of the drift and diffusion currents

$$J = qn\mu E + \frac{\mu}{\beta} \frac{\partial n}{\partial x}, \quad (2.11)$$

where q is the electron charge, β is the inverse of Boltzmann’s constant times temperature, and n is the carrier density (assumed here to be populated only by electrons). Here, I assume the limiting case where drift current is much larger than diffusion current, so diffusion can be neglected. Differentiating Eq. 2.11 (neglecting diffusion), we have

$$\frac{\partial J}{\partial x} = \mu q \frac{\partial E}{\partial x}. \quad (2.12)$$

Using Poisson’s equation $\partial D / \partial x = -qn$ and the continuity equation $\partial J / \partial x = q \partial n / \partial t$,

Eq. 2.12 becomes

$$\frac{\partial^2 D}{\partial x \partial t} = -\mu q n \frac{\partial E}{\partial x}. \quad (2.13)$$

Assuming the E and D fields generated by our SAW take the form of plane waves $E = E_0 \exp(i(kx - \omega t))$ and $D = D_0 \exp(i(kx - \omega t))$, Eq. 2.13 becomes

$$D = -i \frac{\sigma}{\omega} E, \quad (2.14)$$

where $\sigma = \mu n q$ is the conductivity of the piezoelectric semiconductor. Now we can plug Eq. 2.14 into Eq. 2.5 to relate E to strain S , giving

$$E = -\frac{e}{\epsilon} \frac{(1 - i(\sigma/\epsilon\omega))}{1 + (\sigma/\epsilon\omega)^2} S. \quad (2.15)$$

Finally, the wave equation for a piezoelectric semiconductor can be found by substituting 2.15 into Eq. 2.6, giving

$$T = c(1 + \frac{e^2}{c\epsilon} \frac{(1 - i(\sigma/\epsilon\omega))}{1 + (\sigma/\epsilon\omega)^2}) S. \quad (2.16)$$

Clearly we have a similar equation to Eq. 2.10, in which our elastic constant is modified by piezoelectric interactions. Here, the value of our elastic constant varies with the ratio $\sigma/\epsilon\omega$. What is this ratio?

One might recognize σ/ϵ as the dielectric relaxation time. If this is not familiar, the derivation is as follows: Assume a free charge distribution qn in our semiconductor. Then, remember that from Poisson's equation and Eq. 2.12 we have

$$q \frac{\partial n}{\partial t} = \sigma \frac{\partial E}{\partial x} = \frac{\sigma q}{\epsilon} n, \quad (2.17)$$

where ϵ is the dielectric permittivity of our piezoelectric semiconductor. This differential equation describes an exponential relaxation of carrier density $n \propto \exp\{-t/\tau_c\}$ with characteristic time $\tau_c = \epsilon/\sigma$. τ_c is known as the “dielectric relaxation time”. For us, it’s helpful to think of the dielectric relaxation frequency $\omega_c = \tau_c^{-1} = \sigma/\epsilon$ (sometimes called the “characteristic frequency”), as it appears in 2.16.

Substituting $\omega_c = \sigma/\epsilon$, 2.16 becomes

$$T = c(1 + K^2 \frac{(1 - i(\omega_c/\omega))}{1 + (\omega_c/\omega)^2})S \quad (2.18)$$

(recalling that $K^2 = e^2/c\epsilon$). Therefore, Eq. 2.18 describes a piezoelectric wave travelling at velocity $v = \sqrt{c'/\rho}$, where the modified elastic constant is $c' = c(1 + K^2(1 - i(\omega_c/\omega)))/(1 + (\omega_c/\omega)^2)$.

Most notable in Eq. 2.18 is that the effective elastic constant c' depends on the ratio ω_c/ω . Modulating the ratio between the SAW frequency and the conductivity controls the piezoelectric stiffening. However, c' is complex. What does that mean? To understand the complex elastic constant in Eq. 2.18, consider its differential form,

$$\frac{\partial^2 u}{\partial t^2} = \frac{c'}{\rho} \frac{\partial^2 u}{\partial x^2}. \quad (2.19)$$

We can break c' into its real and complex parts. Assume $\sqrt{c'} = \beta + i\gamma$. Then, our plane wave solution becomes

$$u = u_0 e^{(i(kx - k\sqrt{c'/\rho}t))} = u_0 e^{\gamma kt/\sqrt{\rho}} e^{i(kx - \beta kt/\sqrt{\rho})}. \quad (2.20)$$

Examining Eq. 2.20, we can readily see that it describes a plane wave with phase velocity

$$v = \beta/\sqrt{\rho} = Re\sqrt{c'}/\sqrt{\rho} \quad (2.21)$$

and exponential loss (also known as attenuation) per unit length of

$$\Gamma = k \operatorname{Im}(\sqrt{c'})/\sqrt{\rho}. \quad (2.22)$$

This use of a complex wave propagation constant, where the real and complex parts describe dispersion and attenuation, has been used to describe lossy wave propagation in mechanical, electromagnetic, and piezoelectric materials [26] [27, p. 18] [23, 28].

Using Eqs. 2.21 and 2.22, we find the velocity and attenuation of our SAW in a bulk piezoelectric semiconductor to be

$$\frac{\Delta v}{v_0} = \frac{K^2}{2} \frac{1}{1 + (\omega_c/\omega)^2} \quad (2.23)$$

and

$$\Gamma = K^2 \frac{\pi}{\lambda} \left(\frac{(\omega_c/\omega)}{1 + (\omega_c/\omega)^2} \right). \quad (2.24)$$

Figure 2.3 shows Eqs. 2.23 and 2.24 plotted with respect to ω_c/ω . From this, we can see that the SAW is maximally attenuated at $\omega = \omega_c$ and maximal velocity shift is achieved at $\omega \gg \omega_c$.

Equations 2.23 and 2.24 are known as the “classical relaxation model” for the acous-

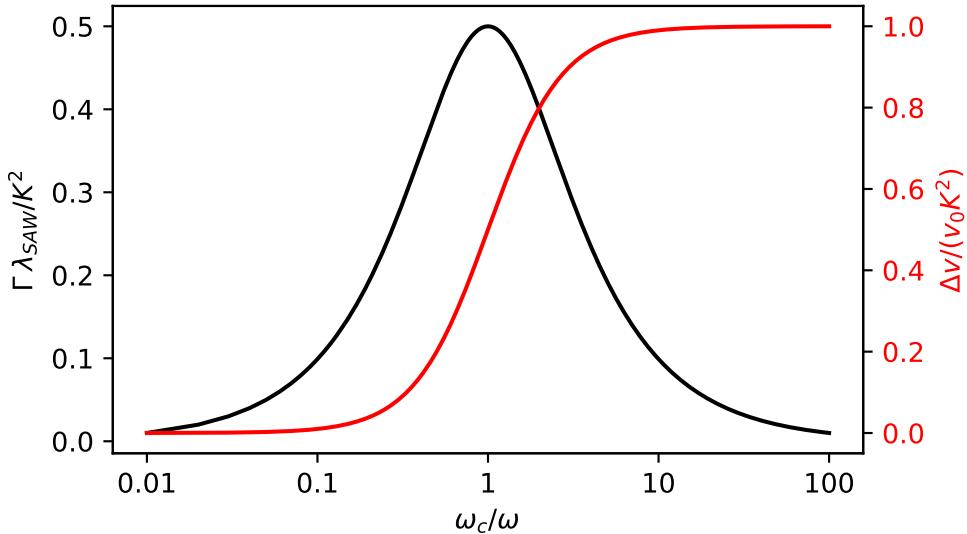


Figure 2.3: Eq. 2.24 (left axis) and Eq. 2.23 (right axis) plotted as dimensionless quantities against the ratio ω_c/ω .

toelectric effect. Equation 2.23 describes relaxation dispersion, which is common in other acoustic systems [24, 29] and can be understood as follows: First, the SAW strains the piezoelectric, perturbing the material from its equilibrium state. Then, the piezoelectric relaxes to equilibrium, returning energy to the SAW after a time $1/\omega_c$. However, depending on the time delay between stimulus ($1/\omega$) and response ($1/\omega_c$), this energy returns to the SAW with a phase delay, leading to dispersion and attenuation. In our case, the relaxation time (and thus, ω_c) depends on the conductivity of the piezoelectric semiconductor.

Equation ?? is fundamental to our investigations into acoustoelectric charge pumping (Sec. 4). However, Eqs. 2.23 and 2.24 describe a bulk material. How do these relations change in the 2D limit?

2.2.3 SAWs propagating in 2D materials

Equation 2.28 is fundamental to our investigations into acoustoelectric charge pumping (Ch. 4). However, Eqs. 2.23 and 2.24 describe a bulk piezoelectric material. How do these relations change when the conductivity is located in a thin film on an insulating piezoelectric material? Figure 2.4 (a) shows the bulk case described by Eqs. 2.24 and 2.23, in which the SAW's energy and the induced current is contained within a depth $1/k$ of the surface. Therefore, the conductance of the region of the bulk material in which the SAW is propagating is $\sigma' = \sigma/k$. Fig. 2.4 (b) illustrates a SAW propagating in a material with permittivity ϵ which is capped by a 2D material of thickness d .

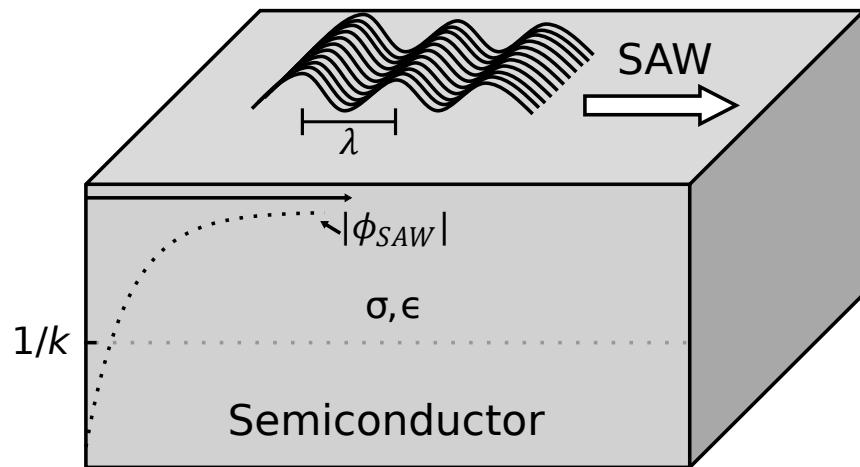
This can be imagined as compressing the current-carrying region from thickness $1/k$ into a thin layer of thickness d and sheet conductivity $\sigma_{2D} = \sigma d$, where $d \ll 1/k$. Reducing the thickness of the current-carrying region from $1/k$ to d reduces its conductance by a factor of $1/kd$. Hence, in the 2D case, the dielectric relaxation frequency is also reduced by a factor of $1/kd$, giving $\omega_c = \sigma_{2D}k/\epsilon$. Then, we have

$$\frac{\omega_c}{\omega} = \frac{k\sigma_{2D}}{\epsilon} \frac{1}{\omega} = \sigma_{2D} \frac{k}{\omega\epsilon} = \frac{\sigma_{2D}}{\sigma_M}, \quad (2.25)$$

where $\sigma_M = v\epsilon$ is defined as the “characteristic conductivity” of the dielectric environment around the 2D material. Finally, Eqs. 2.23 and 2.24 become

$$\frac{\Delta v}{v_0} = \frac{K^2}{2} \frac{1}{1 + (\sigma_{2D}/\sigma_M)^2} \quad (2.26)$$

(a)



(b)

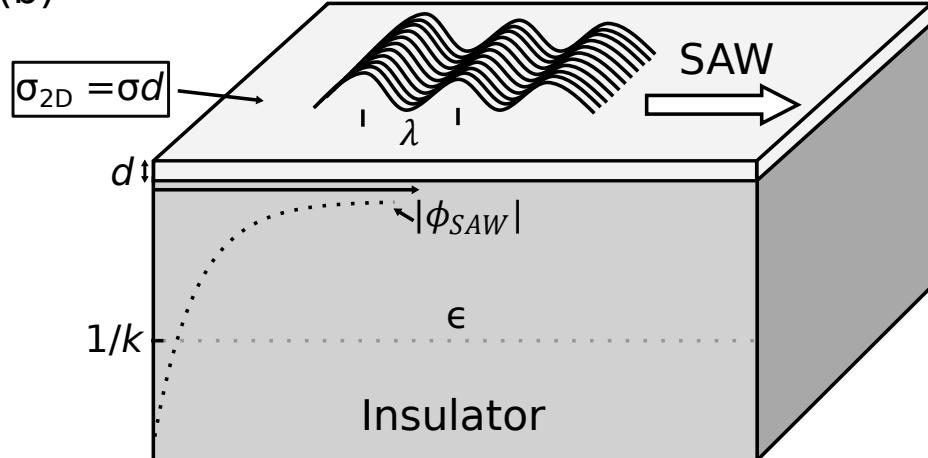


Figure 2.4: (a) A SAW propagating in a bulk material with conductivity σ and permittivity ϵ . (b) A SAW propagating in a piezoelectric material with permittivity ϵ that has been capped by a conductive material of thickness d and sheet conductivity $\sigma_{2D} = \sigma d$.

and

$$\Gamma = K^2 \frac{\pi}{\lambda} \left(\frac{(\sigma_{2D}/\sigma_M)}{1 + (\sigma_{2D}/\sigma_M)^2} \right). \quad (2.27)$$

Similarly to the bulk case (Eqs. 2.23 and 2.24), the SAW is dispersing and losing energy as it propagates through this conductive 2D material. However, the attenuation and dispersion is frequency-independent, and depends only on the ratio σ_{2D}/σ_M . This leads to an important question: Where does the lost SAW energy go?

2.2.4 The 2D acoustoelectric effect

Fal'ko and Iordanskii found that the oscillating electric field that co-propagates with the SAW imparts an effective force on charge carriers, driving a DC current that is proportional to the attenuation Γ [30]. In this section, I present the sketch of Fal'ko and Iordanskii's model given in Ref. [8], as I found their presentation easier to follow. Figure ?? shows a simplified illustration of a SAW propagating through a thin film. As previously discussed, a SAW is accompanied by a co-propagating electric field of the form

$$E(x, t) = E_0 e^{i(kx - \omega t)}. \quad (2.28)$$

From Ohm's law, $E(x, t)$ creates a local oscillating current density

$$j(x, t) = \sigma E(x, t), \quad (2.29)$$

where σ is the conductivity of the thin film. This local current density causes electrons to coalesce in the wells of the SAW potential, as shown in Fig. ???. Assuming that the amplitude

of the perturbation in carrier density caused by the SAW (denoted by Δn) is much smaller than the average carrier density in the thin film (denoted by n_0), the periodic carrier density in the SAW takes the form ¹

$$n(x, t) = n_0 + \Delta n e^{i(kx - \omega t)}. \quad (2.30)$$

Using the continuity equation $\partial J / \partial x = q \partial n / \partial t$, Δn can be written in terms of $E(x, t)$, giving

$$\Delta n(x, t) = -\frac{\sigma k}{q \omega} E(x, t) = -\frac{\sigma 1}{q v} E(x, t) \quad (2.31)$$

Next, with $\Delta n \ll n_0$, and remembering that $\sigma = qn\mu$, σ can be expanded in terms of Δ_n , taking the form

$$\sigma(x, t) = \sigma_0 + \frac{\partial \sigma}{\partial n} \Delta n e^{i(kx - \omega t)}. \quad (2.32)$$

Now, we can find the DC acoustoelectric current by plugging Eqs. 2.32 and 2.31 into 2.29 and taking the time average, giving

¹If $\Delta n \geq n_0$, the perturbation in n can not be approximated as local, leading to the nonlinear acoustoelectric effect. I discuss this further in Sec. 4.9.

$$\begin{aligned}
j(x) = \langle j(x, t) \rangle &= \left\langle \left(\sigma_0 + \frac{\partial \sigma}{\partial n} \Delta n e^{i(kx - \omega t)} \right) E(x, t) \right\rangle \\
&= \left\langle \left(\sigma_0 - \frac{\partial \sigma}{\partial n} \frac{\sigma}{q} \frac{1}{v} E(x, t) e^{i(kx - \omega t)} \right) E(x, t) \right\rangle \\
&= \left\langle \sigma_0 E(x, t) - \mu \frac{\sigma}{v} e^{i(kx - \omega t)} E(x, t)^2 \right\rangle \\
&= -\frac{\mu}{v} \langle \sigma E(x, t)^2 \rangle.
\end{aligned} \tag{2.33}$$

One might initially consider the notion of an oscillating E -field creating a DC current to be counter-intuitive. However, we can now see that, though $\langle E(x, t) \rangle = 0$, a DC current arises from the cross-term $\langle \sigma E(x, t)^2 \rangle$, which corresponds to the time-averaged Ohmic power dissipated by the charge carriers in the thin film. So far, this model considers a local perturbation in n from the SAW; therefore, this cross-term can be thought of as the local dissipation of SAW power by charge carriers in response to the co-propagating electric field.

Finally, we need to relate Eq. 2.33 to Γ . Remembering that Γ describes the loss in SAW intensity per unit length, the SAW intensity can be written in the form

$$I(x) = I_0 e^{(-\Gamma x)}. \tag{2.34}$$

Rearranging and differentiating I with respect to x , Γ takes the form

$$\Gamma = \frac{1}{I} \frac{\partial I}{\partial x} = \frac{1}{I} \langle \sigma E(x, t)^2 \rangle. \tag{2.35}$$

Then, combining Eqs. 2.33 and 2.35, the DC acoustoelectric current density becomes

$$j = -\frac{\mu}{v} \langle \sigma E(x, t)^2 \rangle = -\frac{\mu}{v} I\Gamma = -\frac{\mu I}{v} \frac{K^2}{2\lambda} \left(\frac{(\sigma_{2D}/\sigma_M)}{1 + (\sigma_{2D}/\sigma_M)} \right). \quad (2.36)$$

Equations 2.26, 2.27, and 2.36 are central to interactions between SAWs and quantum materials. In Sec. 4.6, we modify this classical relaxation model, which assumes charge carriers of a single type, to describe mixed-carrier transport in graphene.

2.3 Surface acoustic wave generation

Chapter 3: Methods for fabricating 2D devices

In 2010, the 2D materials revolution was launched when Geim and Novoselov won the Nobel Prize for their experiments on exfoliated graphene [31]. From the humble beginnings of the ‘scotch tape technique’, the field of has matured to an immense parameter space of layered materials for us to explore. In this lies the greatest strength of 2D materials — we can combine the strengths of different materials to create designer heterostructures. These stacks of 2D materials are called “van der Waals heterostructures”, from the van der Waals force that holds them together. In this chapter, I describe methods for fabricating 2D devices. I begin by describing the best practices that I have found for exfoliation. Then, I discuss my implementation of the dry transfer method for stacking 2D materials to create designer heterostructures. Lastly, I show two methods for making electrical contact to 2D materials — photolithography and electron-beam lithography (EBL) — and compare the strengths and weaknesses of each.

3.1 Exfoliation of 2D crystals

While some groups are investigating large-area 2D growth for use in the next generation of electronics [32], the best devices with the lowest electrostatic disorder are still made using mechanical exfoliation [33]. Using sticky tape, layered crystals are cleaved 5-10 times, then transferred onto clean SiO₂. Flake thicknesses can be determined using optical contrast and

verified using atomic-force microscopy (AFM), as shown in 3.1.

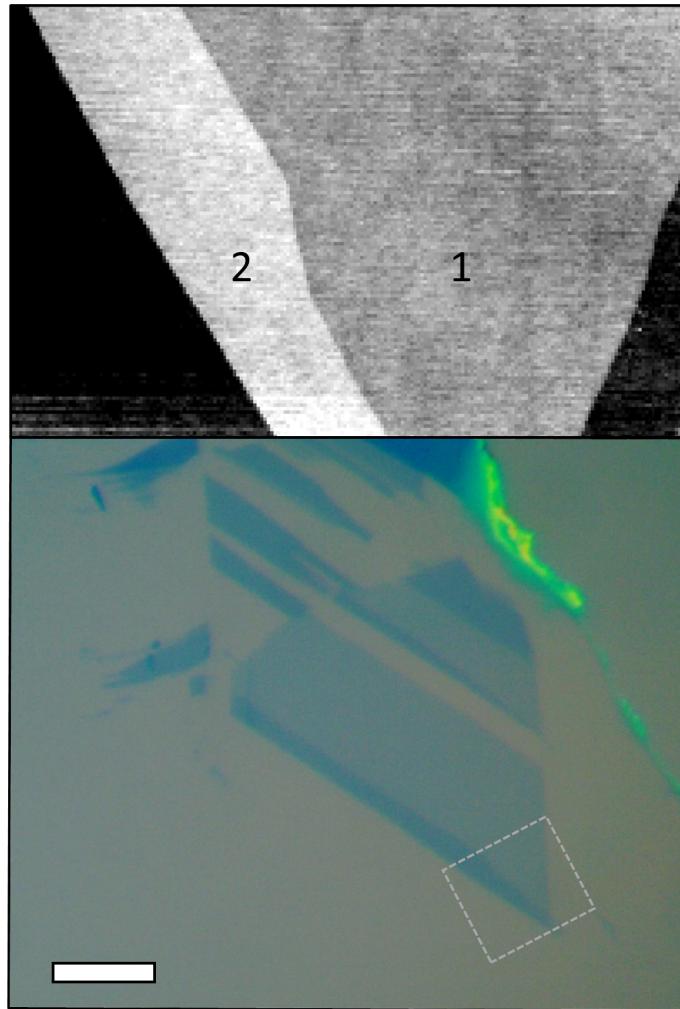


Figure 3.1: Scale bar = $10 \mu\text{m}$

Exfoliation is a simple process, but getting consistent results can be extremely challenging due to the vast array of variables that affect the process. Different research groups, and even different members in the same group, can have vastly differing opinions on the best methods for exfoliation. These often don't appear in literature, only being gleaned through personal

conversations. Furthermore, every 2D material has different mechanical properties, so the best recipe varies widely between materials. I gained substantial knowledge from my visits to the Xu group at University of Washington in 2017. Since then, I have developed my best practices through trial and error. In this section, I give my recommended practices for exfoliating graphene, hBN, and MoS₂.

Exfoliation begins with selecting the tape. The two most widely used tapes are Scotch® Magic™ Tape (“Scotch Tape”) and Nitto Denko SWT20+ wafer tape, (“blue tape”). The main differences between the two are as follows: Scotch tape is stickier and leaves more residue, and blue tape is less sticky and leaves less residue. While blue tape might seem like the obvious choice for the cleanest samples, in a discussion with members of the Yankowitz group at University of Washington, I learned that they still prefer Scotch tape for graphene, as they feel it gives the largest monolayer flakes. In my experience, I find that Scotch tape does work best for graphene, giving larger-area flakes than blue tape. For hBN, I prefer to use blue tape, as the residue left by scotch tape is similar in color to the hBN flakes, as shown in *this figure*.

3.2 Stacking 2D materials: The dry transfer method

The ability to isolate single layers of 2D crystals opened wide the possibility of stacking different atomic layers to create designer heterostructures. In 2010, Dean et al. demonstrated that the mobility and electronic disorder of graphene can be vastly improved by encapsulating the graphene in insulating hexagonal boron nitride (hBN) [34]. Since then, techniques for assembling stacks of 2D materials have improved, allowing for sub-micron

lateral precision and sub-degree rotational alignment between layers [35]. Heterostructure fabrication techniques fall into two main categories: wet-transfer methods, which use sacrificial polymer layers to place down each 2D crystal, and dry-transfer methods, which only require dissolving the polymer stamp once the entire structure is completed. In general, dry transfer methods are preferred as they reduce contamination between layers, and it is the method I use to create the devices discussed in this dissertation. Therefore, I will only describe the dry transfer method here. Similarly to exfoliation techniques, many researchers have different opinions on the best tricks for 2D transfer. For an overview of different 2D transfer methods, see the review by Castellanos-Gomez *et al.* [35]. The method I present in this section was initially learned through discussions with researchers at the University of Washington, then modified based on my own trial and error.

Figure 3.2 shows the viscoelastic stamp, which is mounted onto a micromanipulator stage and used to pick up and place the 2D crystals. The stamp consists of a polydimethylsiloxane (PDMS) layer mounted on a glass slide, with a thin poly(bisphenol A carbonate) (PC) polymer layer on top (some groups use polypropylene carbonate, referred to as PPC). The PDMS acts as a base for the stamp, while the PC layer becomes sticky at elevated temperatures. This method of heating up a polymer stamp to pick up 2D materials is called the “hot pick up technique” [36].

I build the stamp as follows: First, I prepare the PC film (Fig. 3.2 (a)). I begin by making a solution of 6% PC in chloroform (mass percent). The PC takes 24-48 hours of stirring at medium speed to fully dissolve. Then, I clean two glass slides and place them next to each other in a fume hood. I pipette $\approx 2\text{ mL}$ of PC solution in a line on one glass slide, then flip the other slide on top. Using light pressure, I slide the two glass slides apart, leaving

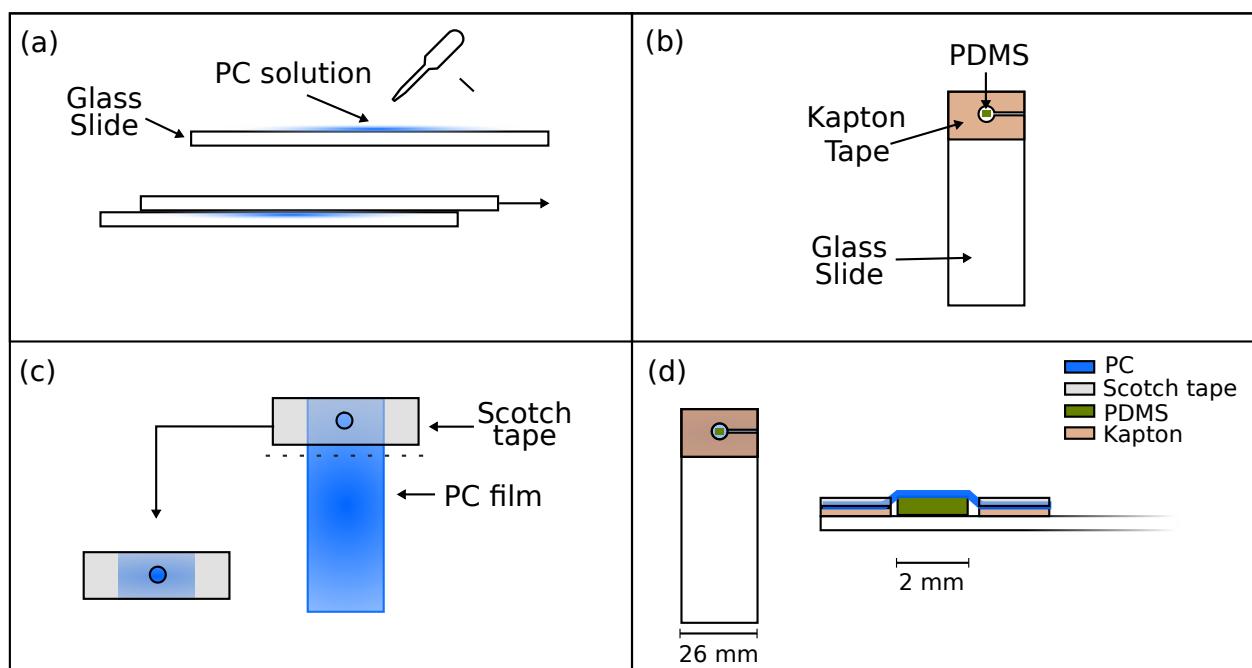


Figure 3.2: The viscoelastic stamp for deterministic transfer of 2D materials.

a film of PC on one side of each slide. Finally, I let the slides dry for at least 1 min before continuing¹.

To prepare the slide that composes the base of the stamp, I use a leather punch to punch a hole in a piece of double-sided polyimide tape (Kapton). Then, I place this piece of tape on a fresh glass slide, and cut a channel in one side of the tape (Fig. 3.2 (b)). This channel allows for air to escape when placing down the PC film in the next step. Without the channel, air gets trapped between the PDMS and PC layers. Next, I take pre-made PDMS sheets (Gel-Pak) that are 17 mil (0.4318 mm) thick. These Gel-Pak sheets have a hard backing on one side, and a soft backing on the other side. I place a strip of double-sided polyimide tape (Kapton) into a plastic dish and place a $\approx 2 \times 2$ cm piece of Gel-Pak sheet onto the dish, hard backing-side down. The choice to put the hard backing side down makes picking up small pieces of PDMS easier. Then, I use a clean razor blade to cut the PDMS into 2×2 mm squares. Using tweezers, I grab one of these squares and place it into the hole in the center of the mounted Kapton tape (Fig. 3.2 (b), green square).

Next, I use a leather punch to make a hole in a piece of scotch tape. Then, I put this scotch tape down onto the dried PC film, ensuring that the area in the tape hole is clean and uniform (Fig. 3.2 (c)). I cut a

¹The chloroform evaporates very quickly, but I usually let it dry while preparing the rest of the stamp, as the PC film isn't used until the final step

3.2.1 PCL cleaning

3.3 Contacts to 2D materials

3.3.1 Photolithography

In this section, I discuss methods for fabricating 2D devices on piezoelectric substrates using photolithography. One might ask: Why not use electron-beam lithography (EBL)? EBL can achieve higher lithographic resolution than photolithography and allows for bespoke circuit designs to match bespoke 2D heterostructures (see Section ***). For these reasons, EBL is an excellent choice for fabricating 2D devices on SiO₂. When performing EBL on a thin (\sim 0.5–3 μm) layer of insulating SiO₂ on conductive Si, the charge buildup from the electron beam can readily dissipate through the thin SiO₂. However, piezoelectric substrates like quartz or LiNbO₃ are insulating throughout, leading to charge buildup which deflects the incident electrons and distorts lithographic patterns. To dissipate the charge on insulating substrates, one can either deposit a thin charge dissipation layer on top of the EBL resist with thermal evaporation (often 10–20 nm of Al or Au), which is etched away after exposing the resist, or spin a conductive polymer on the EBL resist which is water-soluble [37]. These anti-charging layers complicate the fabrication process. Depositing a thin metal charge dissipation layer requires time-consuming thermal evaporation, and removing the metal requires a wet chemical etch. This needs to be repeated for every lithography step. Conductive polymers solve these issues but are prohibitively expensive.² At Oregon State, we can fabri-

²The most common conductive polymer is ESpacer, which costs \$30,000 per 1 L bottle and expires after 6 months. Recently, an alternative conductive resist has been made available, which is available in smaller quantities [38]

cate structures down to 3 μm with photolithography. Unless a device absolutely necessitates smaller feature sizes, it is in our best interest to simplify fabrication and reduce the number of processing steps. However, the motivation for reducing processing steps goes further than just reducing cost and complexity. In my experience, 2D device fabrication is most likely to fail during liftoff. For example, Fig. 3.3 shows a 40 nm flake of hBN transferred onto LiNbO₃ (top panel) which separated from the surface during liftoff (bottom panel), taking 50 nm of metal with it. For these reasons, I chose to use photolithography to fabricate 2D devices on piezoelectric substrates, creating pre-patterned metal contacts on which I transfer the 2DM.

When transferring 2DM onto pre-patterned metal contacts, creating a smooth surface is of paramount importance. Therefore, clean liftoff with smooth edges is necessary. For this, I use a bilayer process with a tuned undercut, with S1813 photoresist on top of LOR 3A (“liftoff resist”). The full recipe can be found in *APPENDIX*. Fig. 3.4 shows a comparison between single-layer and bilayer liftoff processes in which I attempted to lift off 25 nm of Cr deposited on SiO₂ using electron-beam evaporation. In the single-layer process, metal which coated the resist walls did not lift off with the resist, creating wings that are much larger than the metal thickness. In a bilayer process, the bottom layer of resist develops faster than the top layer, creating an undercut profile that breaks the connection between the metal on the resist walls and the desired pattern. It’s clear that a bilayer process is necessary for prepatterned 2D material contacts.

The development rate of the LOR can be tuned by varying the bake temperature. A higher temperature bake results in a slower undercut rate, allowing us to optimize the undercut. If the undercut is too large, the top layer of resist will collapse. If the undercut is too

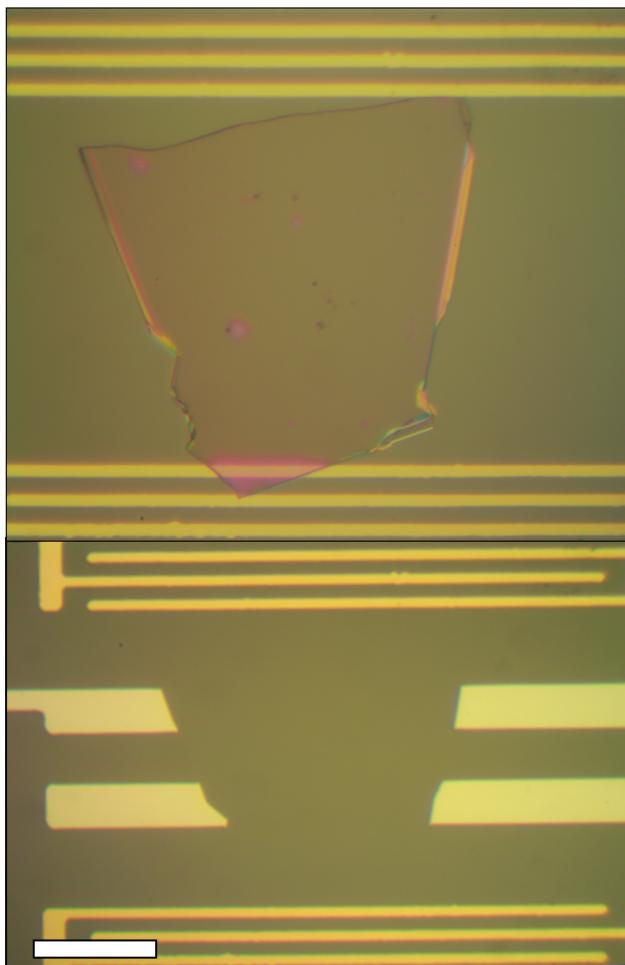


Figure 3.3: Scale bar = 40 μm

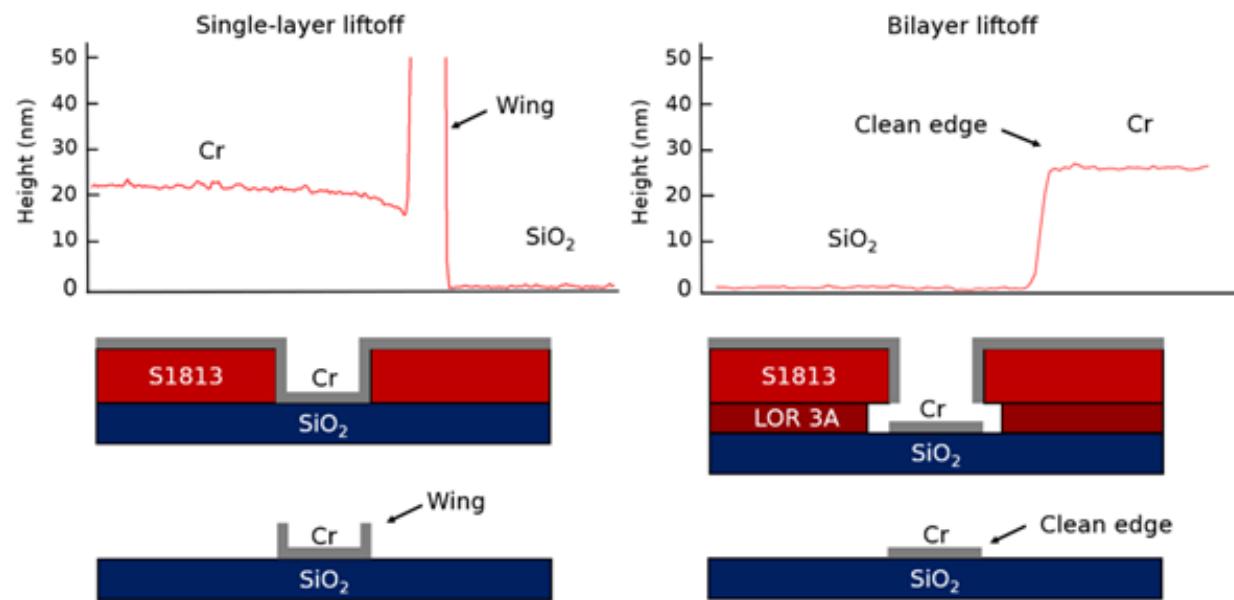


Figure 3.4: AFM trace (top) and schematic (bottom) for single-layer (left) and bilayer (right) liftoff processes of Cr on SiO₂/Si.

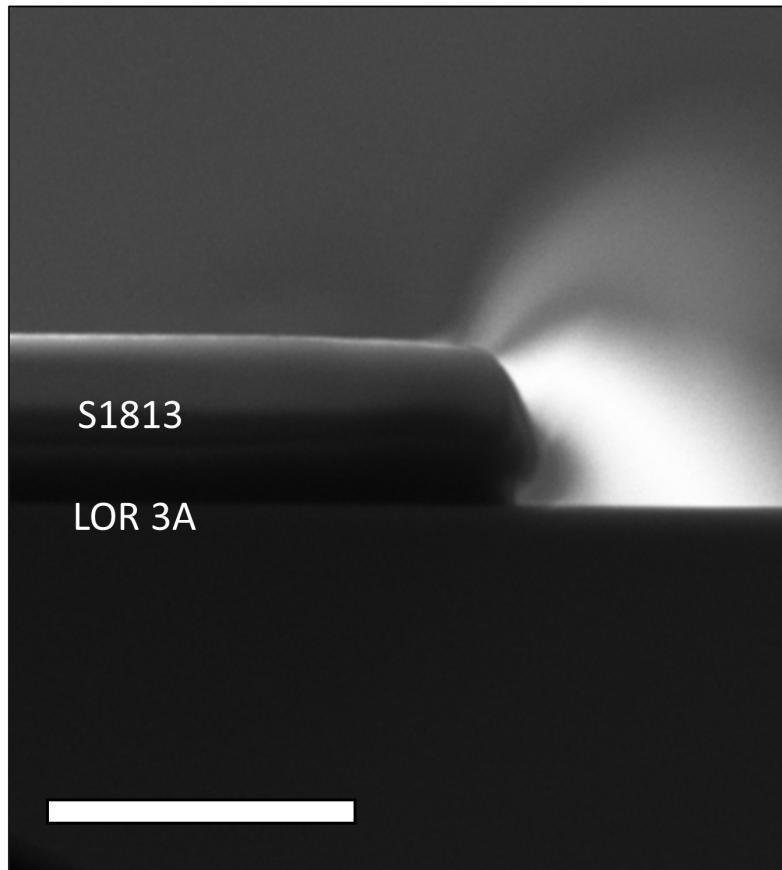


Figure 3.5: Cross-sectional SEM image showing bilayer resist process with undercut length $\approx 0.4 \mu\text{m}$. Scale bar = $3 \mu\text{m}$

small, the metal will not lift off cleanly. I first determined the optimal development time for S1813 as 100 seconds using the interdigitated finger pattern shown in Fig. 3.3 Then, I varied the LOR bake time from 170 C to 190 C and attempted liftoff of 3/20 nm Cr/Au. I found that 180 C was the lowest bake temperature at which liftoff was clean. Figure 2.4 shows a cross-sectional SEM image, in which I confirmed that a 180 C bake and 100 s development creates a $0.4 \mu\text{m}$ undercut.

3.4 Electron-beam lithography

Chapter 4: Acoustoelectric charge pumping in ultra-clean graphene using
surface acoustic waves

4.1 Abstract

4.2 Introduction

4.3 Background

4.4 Experiment design

4.5 Results

4.6 Discussion

4.7 Conclusion

4.8 Supplementary Material

4.9 Nonlinear acoustoelectric effect in graphene

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Chapter 5: Flip-chip design for non-invasive gating of pristine quantum materials

5.1 Introduction

Lithographic patterning followed by metal deposition is the standard technique to define electrostatic gates; however, the methods of fabricating these devices often involve harsh processing. For example, taking a material to high temperatures — such as during thermal deposition of metals and chemical vapor deposition — can damage sensitive structures by thermal strain (See Appendix on EBL IDT damage from CNT growth processes). Similarly, harsh etching chemicals can introduce impurities and dopants to the surface, affecting electron mobility [2]. Electron-beam lithography can also damage pristine surfaces [39]. To fulfil this need for electrostatically gating a surface while leaving it pristine, the technique of “flip-chip gating” has emerged in recent years [2, 40]. Distinct from the similarly named “flip-chip packaging” technique in semiconductor device processing, flip-chip gating involves flipping the gate chip onto the chip to be gated, allowing a material to be field-effect gated without harsh processing (Fig. 1). This method of flip-chip construction has led to breakthroughs in hybrid quantum systems [41, 42].

The air gap between the gate chip and nanomaterial to be gated is of paramount importance for flip-chip devices. As the flip-chip spacing d increases, a capacitive electrostatic gate decreases in strength as $1/d$, and as mentioned in ??, most of the energy in a SAW’s

periodic potential is contained within one SAW wavelength of the surface. As we build higher-frequency SAW devices to interface with nanomaterials, such as for creating quantum pumps that output higher-magnitude quantized current, our flip-chip's spacing becomes increasingly important. However, most prior works don't ensure parallel mounting nor directly measure their flip-chip's spacing [41, 42, 43], with one work estimating their air gap using capacitance [2], and another roughly estimating their air gap by comparing to similar non-flip-chip devices [43]. In this chapter, I present a flip-chip platform that does not rely on external mounting pressure, and allows for characterization of the flip-chip air gap in multiple areas to determine parallel mounting. Instead of springs or tension arms, my design uses hard-cured varnish and etched Si spacers to hold a precise air gap. I benchmark this platform by building a flip-chip capacitor using photolithography, deep reactive ion etching (RIE), and a homebuilt flip-chip assembly station. I verify the spacing between the two chips with two independent methods — capacitance, and reflectance spectroscopy — and evaluate the feasibility of a flip-chip without external mounting pressure.

5.2 Measuring flip-chip spacing using interference spectroscopy

The first method I use to measure the air gap between two chips is interference spectroscopy. Using a laser with a spot size $< 1 \text{ mm}$, I can not only measure the central air gap, but probe various spots on the flip-chip to determine if the two chips are parallel. Figure 5.2 shows the optical setup used in the interference spectroscopy measurement.

To correct the reflectance spectrum for wavelength-dependent power fluctuations and substrate effects, I measure a reference spectrum using a bare Si substrate, then subtract

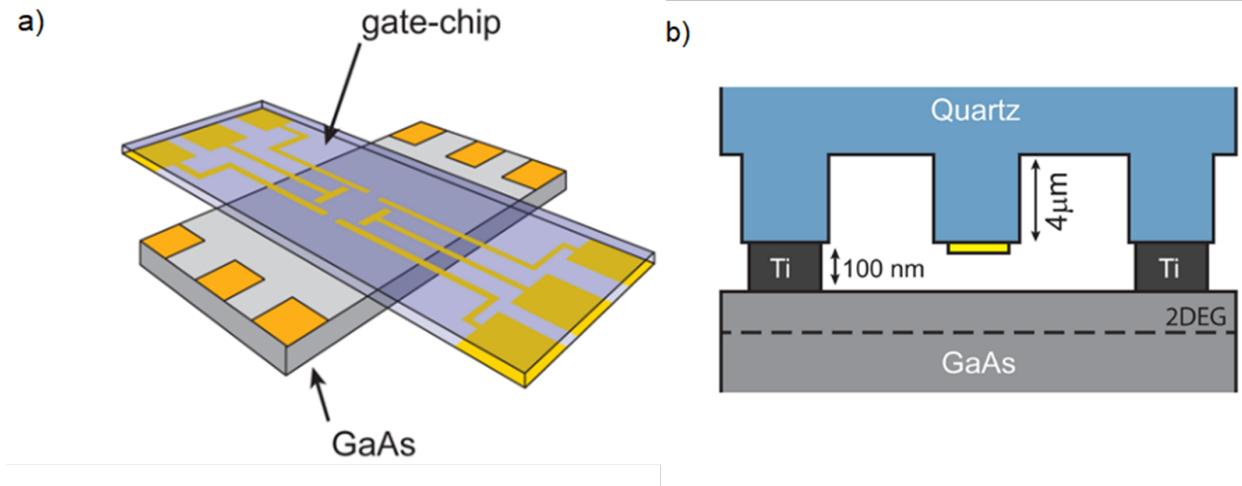


Figure 5.1: Flip-chip design from [2]. (a) The upper gate-chip is printed on quartz to allow alignment with the lower GaAs chip. The lower chip's gates are attached by micro soldering to preserve the pristine GaAs surface's ultrahigh electron mobility. (b) Side view of the stacked chips. The gate (yellow) and GaAs are separated by 100 nm using patterned Ti posts.

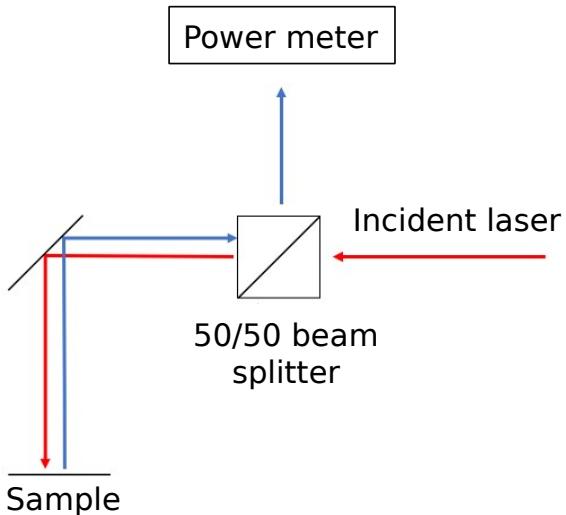


Figure 5.2: The interferometer setup used to measure the reflectance of a sample. Incident wavelength is scanned using a Labview-controlled monochromator and plotted against measured reflected power. The colors indicate incident light (red) and reflected light (blue).

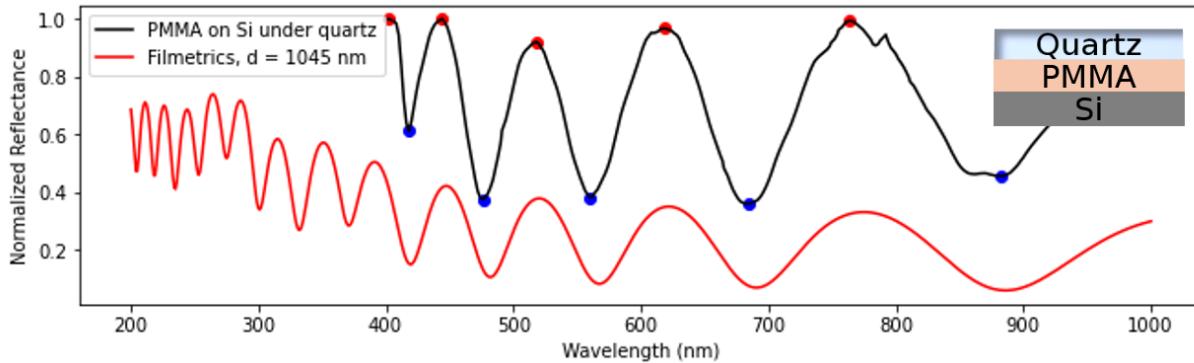


Figure 5.3: Corrected measured reflectance of a Si-PMMA-quartz stack compared to the Filmetrics reflectance calculation with 1045 nm-thick PMMA.

this reference spectrum from the measured interference spectrum. Then, I determine the flip-chip air gap by hand-fitting to a model spectrum calculated with Filmetrics's online thin-film modelling calculator.

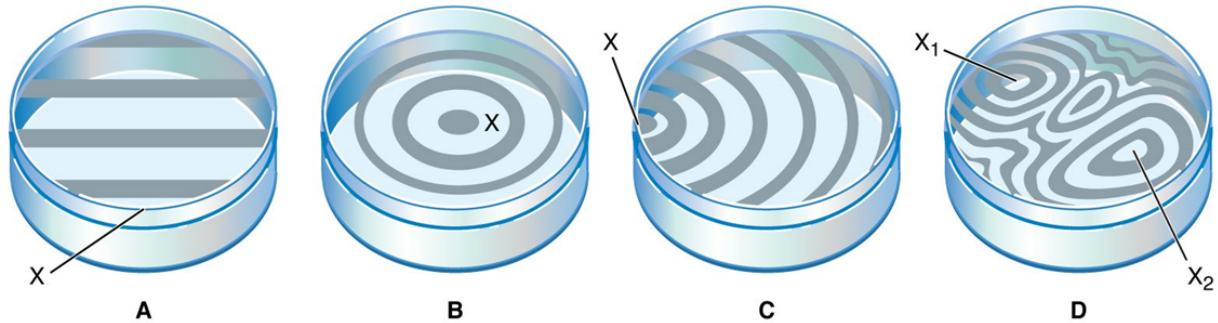
As a first test, I spun a PMMA 495 A11 solution on a Si chip at 2500 RPM for 60 seconds. According to the manufacturer's spin curves, the PMMA layer should be ≈ 1000 nm thick. Then, I used the process described in 5.3 to glue a quartz chip on top to create the Si-PMMA-quartz stack shown in the inset of Fig. 5.3. Figure 5.3 shows the corrected reflectance spectrum of this Si-PMMA-quartz stack versus the reflectance calculated with the Filmetrics model.

The peaks and troughs of the measured reflectance spectrum are consistent with a PMMA thickness of 1045 nm, close to the predicted spun PMMA thickness, verifying the validity of this method.

5.3 Flip-chips with no spacers

Figure *** shows a diagram of my home-built flip-chip assembly station. I designed the holder arm with a “tuning fork” structure (Fig. *** b) which allows me to look through the quartz chip to align structures on the top and bottom chips. For all the flip-chips described in this chapter, I used the following assembly process: To create the top and bottom chips, I coated fused quartz and bare p-doped Si wafers (University Wafer) with S1813 photoresist to protect them during the dicing process, then diced the Si into 7 mm × 12 mm rectangles and the quartz into 4.5 mm × 12 mm rectangles using a DISCO DAD 3220 wafer dicing SAW. Immediately prior to gluing the chips together, I removed the photoresist by soaking in a 60 °C Remover PG bath for 15 minutes, followed by spraying with acetone and isopropyl alcohol and drying with dry N2. Then, I cleaned both chips by submerging them in acetone and rubbing for 20 seconds with a Rubystick T-21 swab to remove any dust [44]. Next, using PDMS strips, (Gel-Pak), I mounted them to the homebuilt flip-chip mounting station as shown in Figure ****.

Figure ?? shows an optical image of a flip-chip during alignment. First, I align the edges of the top and bottom chip to ensure they are perpendicular. Then, I slowly lower the z-stage to bring the chips into contact, watching for interference fringes. As the flip-chip spacing becomes smaller, the interference fringes change. Once the top chip contacts the bottom chip, the spacing will not change as I lower the z-stage, so the interference fringes will remain static. This is how I determine that the two chips are in contact. Once the top and bottom chips are in contact, I glue the two chips together by putting two small beads of GE 7031 varnish at the edges. I hard-cure the varnish using a heat gun at 200 C for



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Figure 5.4: From [3]

5 minutes, holding the heat gun 20 cm from the chip. I also attempted to use photoresist to glue the chips together, as in Ref. [2], but it was difficult to avoid photoresist flowing between the sandwich due to the capillary effect (see Appendix B).

As a first check, a flip-chip's cleanliness can be assessed by viewing the interference fringes (Newton's rings) visible through its quartz top. Figure 5.4 illustrates the pattern of interference fringes expected from different surface topographies. If the two surfaces are parallel, the rings will be parallel (Fig. 5.4 (A)). Similarly, if a large piece of dust comes between the two surfaces, a point with many small concentric fringes will be visible, curving towards the point which the dust bridges the air gap (Fig. 5.4 (B)). This method was used in [43] to confirm that no large dust particles settled between the two sides of their flip-chip.

5.3.1 Smallest achievable air gap

Before attempting to control the air gap between two chips, I first need to determine the smallest air gap that I can achieve between two clean chips. Figure 5.5 (a) shows a flip-chip

constructed from pristine quartz and Si chips using the method described in Sec. 5.3. I performed three interference spectroscopy measurements on this chip — one in the center, and one on each edge — to determine if the chips are mounted parallel to each other.

The air gap measurement confirms that one side of the flip-chip is $\approx 1\text{ }\mu\text{m}$ closer than the other side. Note that the interference fringes curve towards the side with the smallest spacing, as expected. I constructed two other flip-chips with no spacers, and the smallest spacing I could achieve was the $2.4\text{ }\mu\text{m}$ side of the flip-chip shown in Figure 5.5. I was not able to determine the exact reason for this limit. When I observed visible dust between the chips, I uncoupled the flip-chip and cleaned the Si and quartz chips. No visible dust is present between the flip-chip shown in Fig. 5.5. However, unseen dust of size $\approx 2.4\text{ }\mu\text{m}$ could be present. The air gap limit could also arise from thickness variation over the surface of the quartz and Si wafers. Ref. [43] attributes their minimum achievable flip-chip spacing (fabricated in a class-100 clean room) of 50 to 200 nm to the top and bottom chips not being perfectly flat across the contact area. We did not buy special $< 1\text{ }\mu\text{m}$ total thickness variation Si wafers from University Wafer; furthermore, they do not quote the thickness variation of their fused quartz wafers. From these flip-chips with no spacers, I determine $2.4\text{ }\mu\text{m}$ to be the lower bound for the air gap that I can reasonably achieve with etched Si spacers, and use this to inform my flip-chip design in the next section.

5.4 Flip-chip capacitor with deep RIE-etched Si spacers

In the previous section, I determined that the smallest spacing that I can reasonably achieve between two pristine chips is $2.4\text{ }\mu\text{m}$. However, this does not exclude the possibility of

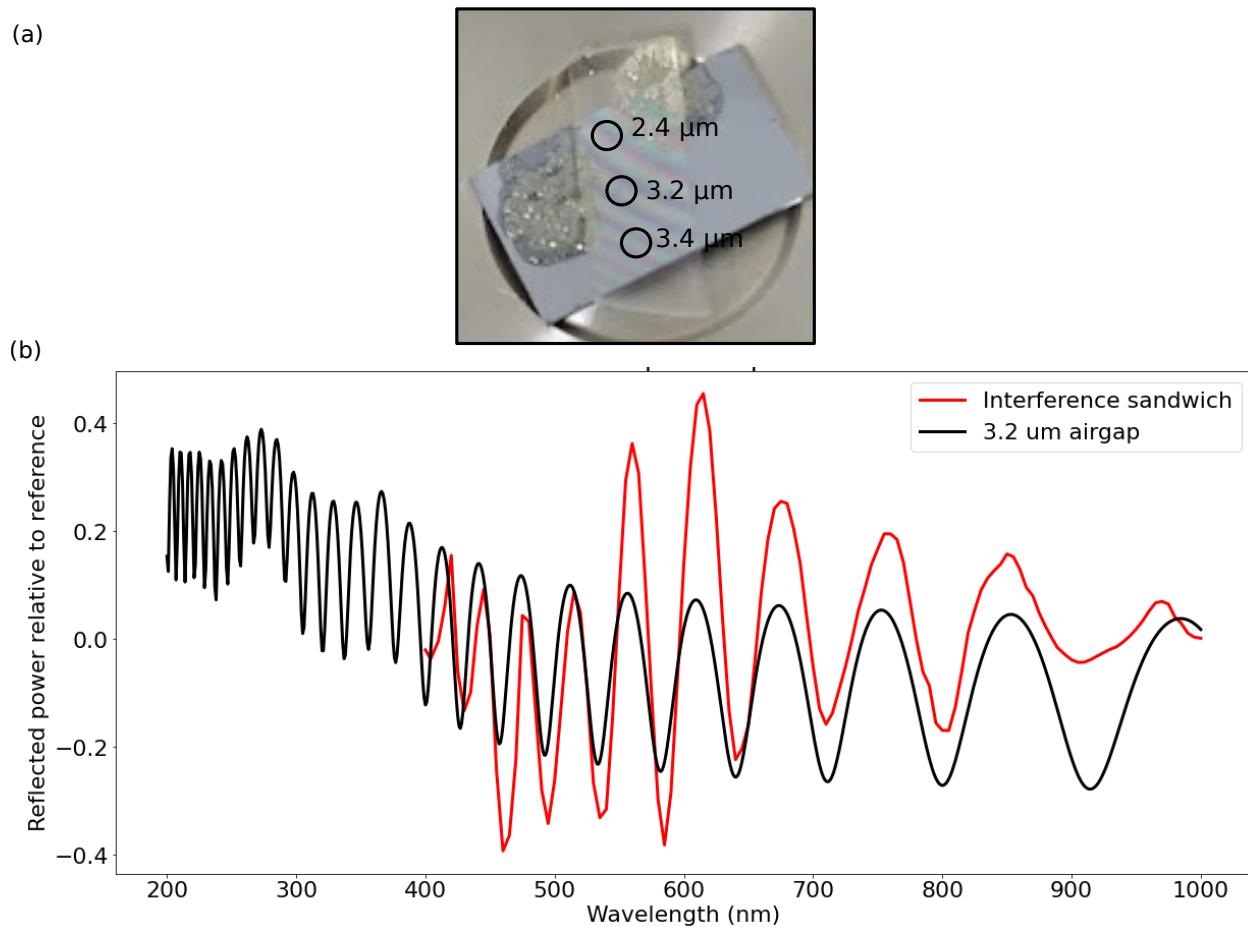


Figure 5.5: (a) A flip-chip with no spacers made from quartz and Si. The three circles indicate the spots at which I directed the laser for interference spectroscopy air gap measurement. (b) The reflectance spectrum from the central spot compared to the Filmetrics model with a $3.2 \mu\text{m}$ air gap.

bringing the gate chip closer to our nanomaterial in a small area while leaving most of the flip-chip spaced by $\geq 2.4 \mu\text{m}$. A two-tier etch has previously been used to achieve a narrow central spacing of $< 1 \mu\text{m}$ while leaving a larger air gap between most of the area of the flip-chip [2]. This reduces the likelihood of dust becoming sandwiched in-between the chips and preventing close spacing.

Figure 5.7 shows the two-tier deep reactive ion etch (RIE) process that I use to create pillars that define the flip-chip spacing. I first print $50 \times 50 \mu\text{m}$ Cr squares with center spacing $360 \mu\text{m}$ and thickness 150 nm on a p-doped Si substrate using photolithography (Figure 5.7 (1)). This Cr serves as an etch mask for the deep RIE. Then, I use the SI etch recipe described in A.2 and an Oxford Plasmalab 100 plasma etch system to etch 460 nm into the Si (Figure 5.7 (2)). This first etch defines the center spacing of the flip-chip. Next, I print the capacitor structure using photolithography and metallization of 150 nm Cr, consisting of a $750 \times 750 \mu\text{m}$ square center pad and $50 \mu\text{m}$ wires that extend to the edges of the chip (Figure 5.7 (3)). I fabricated this same capacitor structure on both the Si and quartz chips (Figure 5.7(b)). The long wires allow me to make electrical contact to the central pad of the capacitor when the two chips are sandwiched together. Then, I etched the final $5 \mu\text{m}$ into the Si (Figure 5.7 (4)). For both Si etches, I determined the exact etch depth using AFM. Figure 5.6 shows the flip-chip capacitor during alignment. I assembled the flip-chip capacitor using the process described in Sec. 5.3.

Figure 5.8 (a) shows the measured reflectance spectra for the left and right side of the flip-chip capacitor. The left side best-matches $(5.00 \pm 0.05) \mu\text{m}$, while the right side best-matches $(6.50 \pm 0.05) \mu\text{m}$. The error denotes the smallest step for which the best hand-fit was obvious. For example, during the fitting process, it was clear that, for the left side,

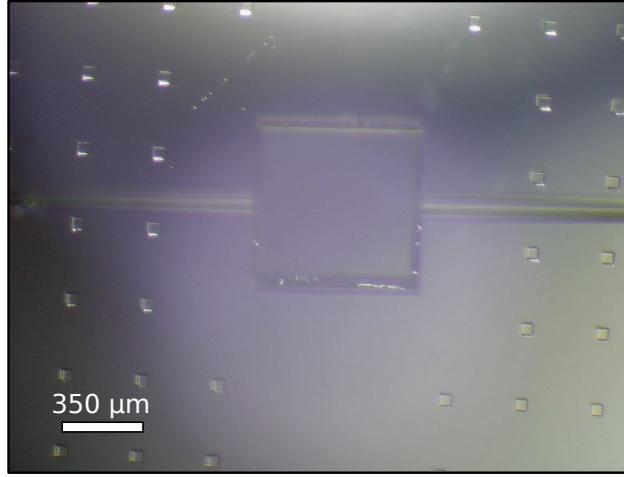


Figure 5.6: View through the microscope camera during initial alignment of the flip-chip capacitor (the top and bottom chips are still far from each other, so no Newton's rings are visible).

$5.00\text{ }\mu\text{m}$ was a better fit than $4.95\text{ }\mu\text{m}$ or $5.05\text{ }\mu\text{m}$. Figure 5.8 (b) shows the schematic of the completed flip-chip capacitor, with AFM measurements of the final structure indicated on the diagram.

Figure 5.8 illustrates that I did not achieve parallel mounting. The left air gap agrees precisely with the etched post height of $(4.950 \pm 0.005)\text{ }\mu\text{m}$; however, the right air gap sits $(1.50 \pm 0.05)\text{ }\mu\text{m}$ taller. The designed center gap is $(0.563 \pm 0.005)\text{ }\mu\text{m}$, from AFM measurements of the posts and central mesa. Therefore, I estimate my flip-chip capacitor spacing to be $(1.313 \pm 0.055)\text{ }\mu\text{m}$ $((0.563 \pm 0.005)\text{ }\mu\text{m} + (1.50 \pm 0.05)\text{ }\mu\text{m}/2)$. Though I did not achieve parallel mounting, this emphasizes the strength of determining the air gap with optical methods. Before mounting the chip, wire bonding, and taking electrical measurements, the air gap of a flip-chip can be estimated, and parallel mounting can be verified. If the estimated air gap is not suitable, or the top and bottom chips are not parallel, the flip-chip can be

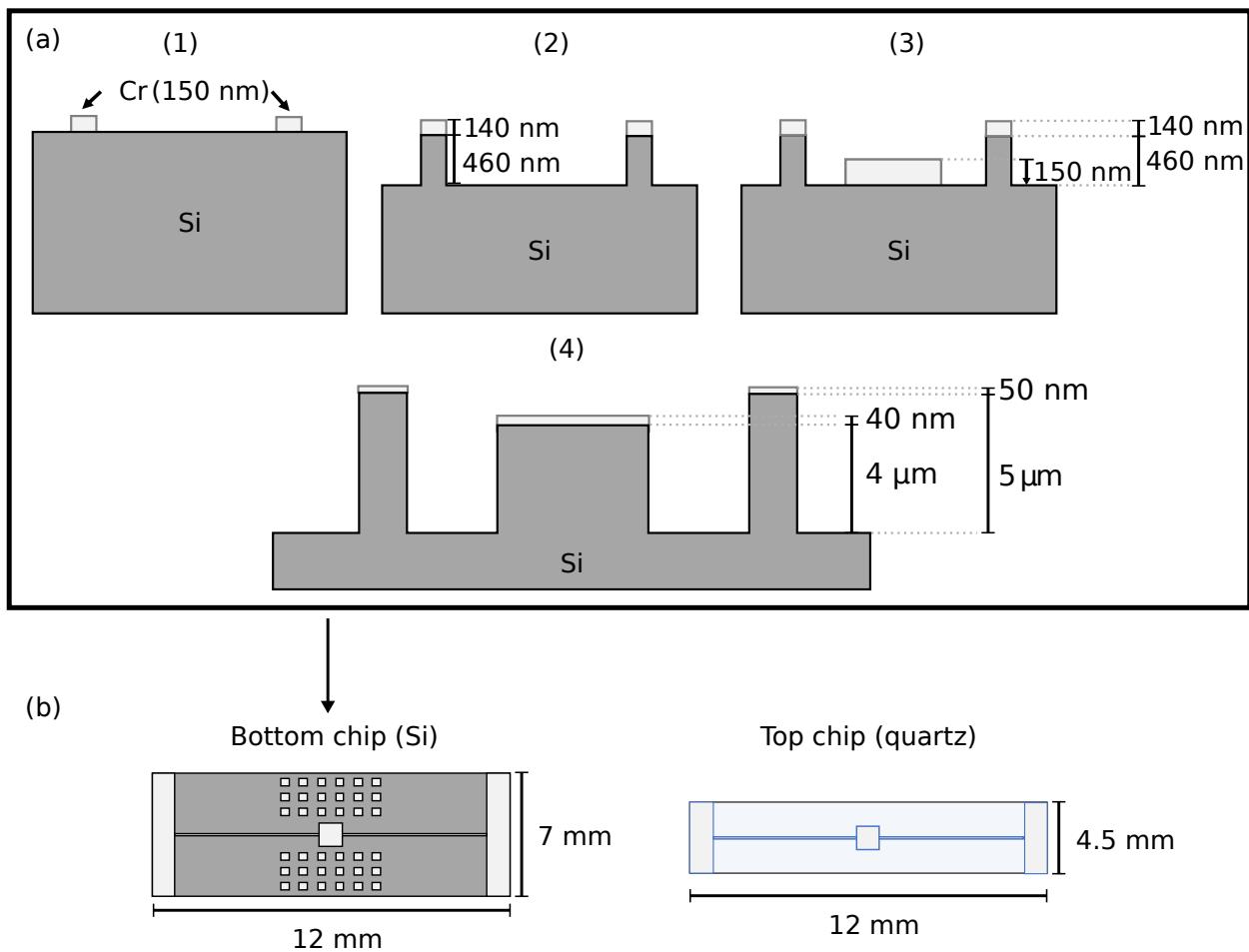


Figure 5.7: (a) Two-tier etch process for defining the center gap and post height of the flip-chip. The denoted measurements are estimated from known Cr deposition rates and known Cr and Si etch rates (see Appendix A.2). (b) The completed top and bottom sides of the flip-chip capacitor, before assembly.

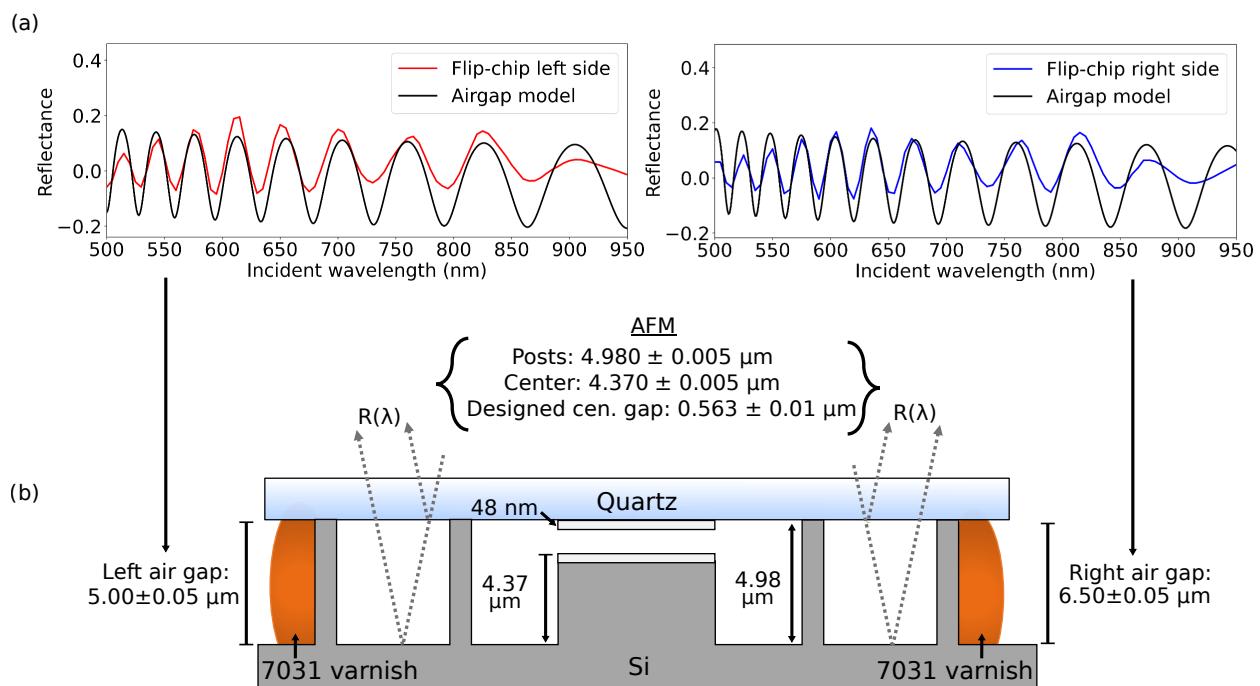


Figure 5.8:

deconstructed, cleaned, and re-mounted (7031 varnish readily dissolves in a solution of 99% ethanol). Then, once a suitable estimated air gap is achieved, a more precise measurement can be made using capacitance.

5.5 Flip-chip air gap measurement with capacitance

The total impedance of my flip-chip capacitor is the sum of the capacitor impedance and series resistance

$$Z = R_s + Z_C = R_s + \frac{1}{i\omega C}. \quad (5.1)$$

Assume an AC signal $V = V_0 \exp(i\omega t)$ is applied to the flip-chip. Then, the current is

$$I = \frac{V}{Z} = \frac{V}{R_s + 1/i\omega C} = V \frac{i\omega C}{1 + i\omega CR} \approx V i\omega C (1 - i\omega CR) = V (RC^2 \omega^2 + i\omega C), \quad (5.2)$$

where $C = \epsilon_0 A/d$ is the capacitance of the flip-chip, and I assume that the resistance is small, so $\omega CR \ll 1$. The measured current is then the real part of Eq. 5.2,

$$I = V_0 \omega^2 R C \cos(\omega t) + V_0 C \omega \sin(\omega t). \quad (5.3)$$

Therefore, by applying an AC signal to the flip-chip capacitor and measuring the sine component of the resultant current, the distance between the flip-chip capacitor plates can be determined using $d = 2\pi f \epsilon_0 A V_0 / I$.

Figure 5.9 (a) shows the experimental setup that I use to measure the capacitance of my flip-chip. I use a Stanford SR58 lock-in amplifier to apply a signal of $V_0 = 100$ mV at

$f = 200$ Hz and measure the sine component of the resultant current. Figure 5.10 shows a schematic and photograph of the completed flip-chip capacitor.

Figure 5.9 shows the results of the capacitance central air gap measurement. To determine the effect of mounting pressure, I measured the capacitance in three scenarios: applying no force, applying force on either edge of the flip-chip, and applying force in the center of the flip-chip (directly on the capacitor plates). With no mounting pressure, I determined the central air gap to be (1.33 ± 0.01) μm , which is in very good agreement with the estimated central air gap from reflectance spectroscopy of (1.36 ± 0.06) μm determined in Sec. 5.4. When applying edge force to simulate mechanical mounting pressure, the air gap closed to (0.688 ± 0.010) μm , which is close to the designed air gap defined by the etched posts (measured with AFM to be (0.563 ± 0.010) μm). Applying a strong enough central force short-circuits the capacitor plates.

Figure 5.11 shows the geometry of the bent quartz chip when applying a central force to the flip-chip capacitor, short-circuiting the top and bottom chips. The bend is greatly exaggerated. Assuming that the quartz chip bends directly at the Si posts, it bends by (0.563 ± 0.010) μm over 1 mm, corresponding to a bending radius of 0.22 m (assuming the bend forms an arc). Therefore, the strain in the quartz is $0.85 \text{ nm} / 1 \text{ mm} = 8.5 \times 10^{-5}\%$.

5.6 Conclusions

In this section, I built a flip-chip capacitor by sandwiching patterned quartz and etched Si chips together with hard-cured varnish. I used two independent methods to characterize the gap between the two chips — interference spectroscopy (“the optical method”) and

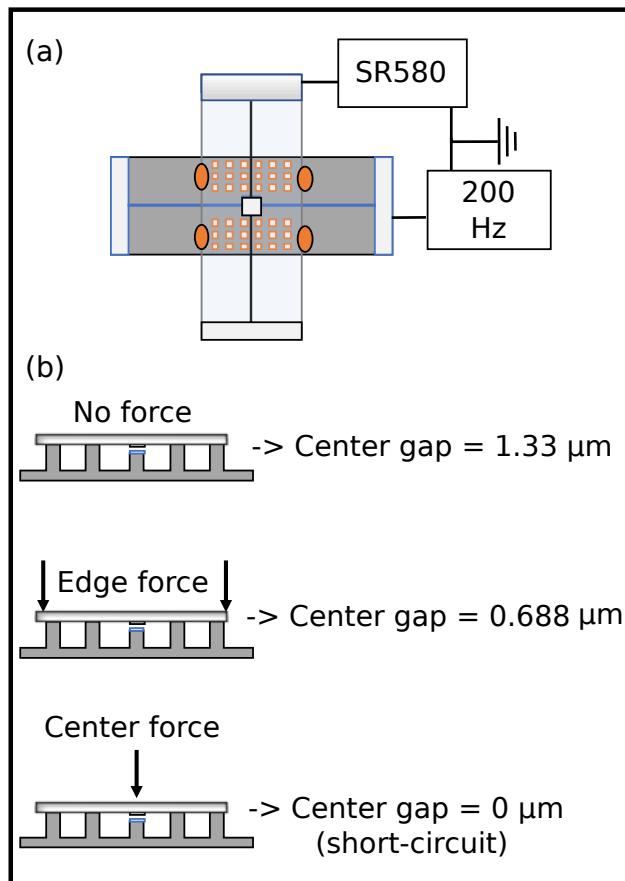


Figure 5.9: (a) schematic of the capacitance measurement. (b) Dependence of central air gap modulation with respect to location of applied mounting pressure. The edge force was applied onto the quartz chip, above the etched spacers closest to the edge of the Si chip. The central force was applied directly above the capacitor pads.

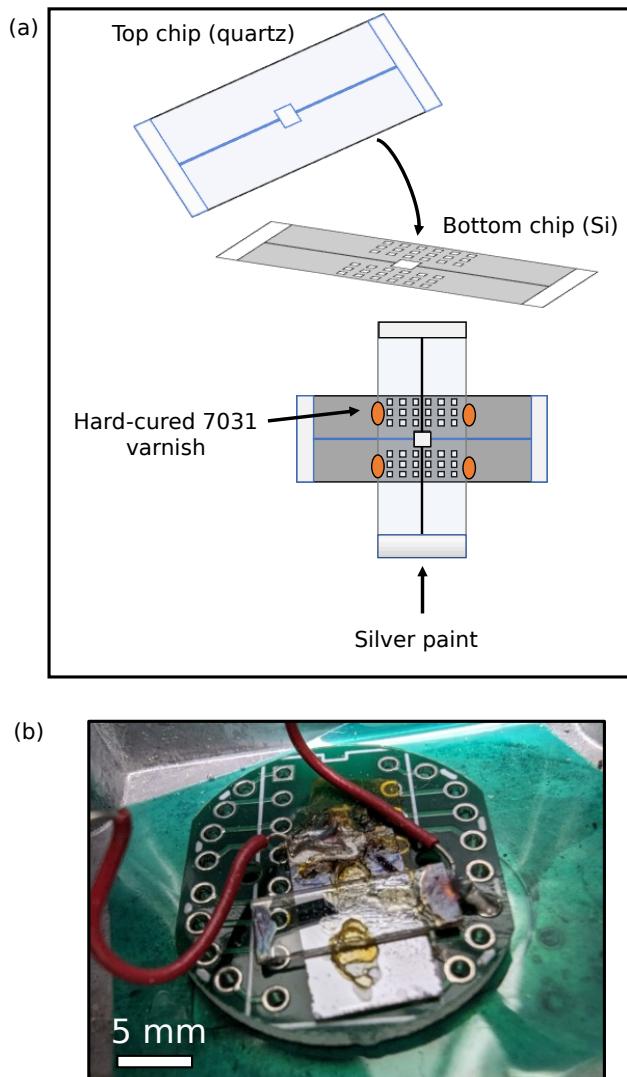


Figure 5.10: (a) Schematic of the completed flip-chip capacitor. (b) Optical image of the completed flip-chip capacitor. Wires are seen soldered to the silver paint, making electrical contact to the top and bottom chips.

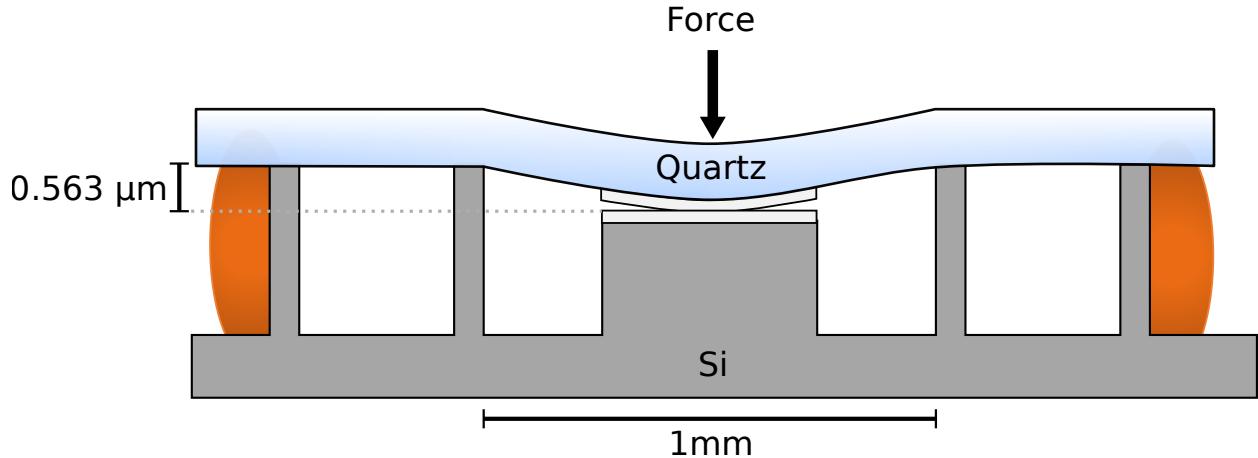


Figure 5.11: Geometry of the bent quartz chip with a centrally-applied force that short-circuits the top and bottom capacitor pads.

capacitance. Combining both methods allows for a complete characterization of the flip-chip air gap at multiple locations, and a precise measurement between the gate chip and quantum material to be gated. The optical air gap measurement is useful for quick determination of the air gap before spending time wire bonding the chip and mounting it in a cryostat. Prior reports of flip-chip devices did not use optical methods to measure their flip-chip spacing [2, 41, 42, 43]. Using this optical method, I found that I was not able to achieve parallel mounting without external mounting pressure, likely due to the arm of my homebuilt assembly station not being perfectly level, leading to uneven mounting pressure. This is in agreement with the Si-quartz sandwiches that I created without patterned spacers (Sec. 5.3.1), in which I noticed that one side was always $\approx 1 \mu\text{m}$ higher than the other, as measured using interference spectroscopy. Conversely, the capacitance measurement requires electrical contact to the chip, but can measure the air gap more precisely. The central spacing that I measured with capacitance (Fig. 5.9) in the cases of no mounting pressure and edge mounting

pressure are in good agreement with the flip-chip geometry determined by AFM and optical measurement (Fig. 5.8). When I applied mounting pressure to the central capacitor pads, I was able to bend the quartz chip by $(0.563 \pm 0.010) \mu\text{m}$ and short-circuit the capacitor pads. This suggests the possibility of measuring the air gap of a flip-chip inside a cryostat and tuning the air gap in-situ. Future flip-chip devices could be designed with a capacitive pad in multiple locations on top and bottom chips. Then, A motorized stage inside the cryostat, such as in [45], could be used to apply mounting pressure to the flip-chip while measuring the capacitor array to minimize the air gap and maximize the strength of coupling between the SAW gate and quantum material.

Chapter 6: Conclusion

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APPENDICES

Appendix A: Fabrication recipes

A.1 Comparison between EBL and photolithography process on LiNbO₃

- **EBL process for encapsulated graphene FET on LiNbO₃ with edge contacts:**
 - Transfer encapsulated GR onto substrate
 - Spin EBL resist
 - Deposit charge dissipation layer (thin Al)
 - Exposure (edge contact etch)
 - Etch Al
 - Develop resist
 - RIE etch for edge contacts
 - Spin EBL resist
 - Deposit Al
 - Exposure (contact metal)
 - Etch Al
 - Deposit S/D contacts
 - Spin EBL resist
 - Deposit Al

- Exposure (gate contact)
 - Etch Al
 - Deposit gate contact
- **Photolithography process for graphene FET on LiNbO₃:**
 - Spin photoresist
 - Print S/D contacts
 - Deposit S/D contacts
 - Transfer encapsulated GR onto substrate
 - Spin photoresist
 - Print gate contact

A.2 Si RIE recipe

- SF₆: 14.0 sccm
- CHF₃: 35.0 sccm
- 100 W RF power
- Chamber pressure = 10 torr
- Si Etch rate: 40 nm/min
- Cr etch rate: 0.8 nm/min

Appendix B: Additional flip-chip tests

I initially tried to use photoresist as spacers for flip-chip construction, following the work of [43]. However, I found that the minimum spacing I could achieve was greater than a single layer of spun S1813 photoresist ($\approx 1500\text{ nm}$), so I transitioned to using etched Si spacers. Also, the photoresist tended to flow between the flip-chips due to capillary action, so I found that GE 7031 varnish worked much better as glue. Figure B.1 shows my attempts at photoresist-spaced and photoresist-glued flip-chips.

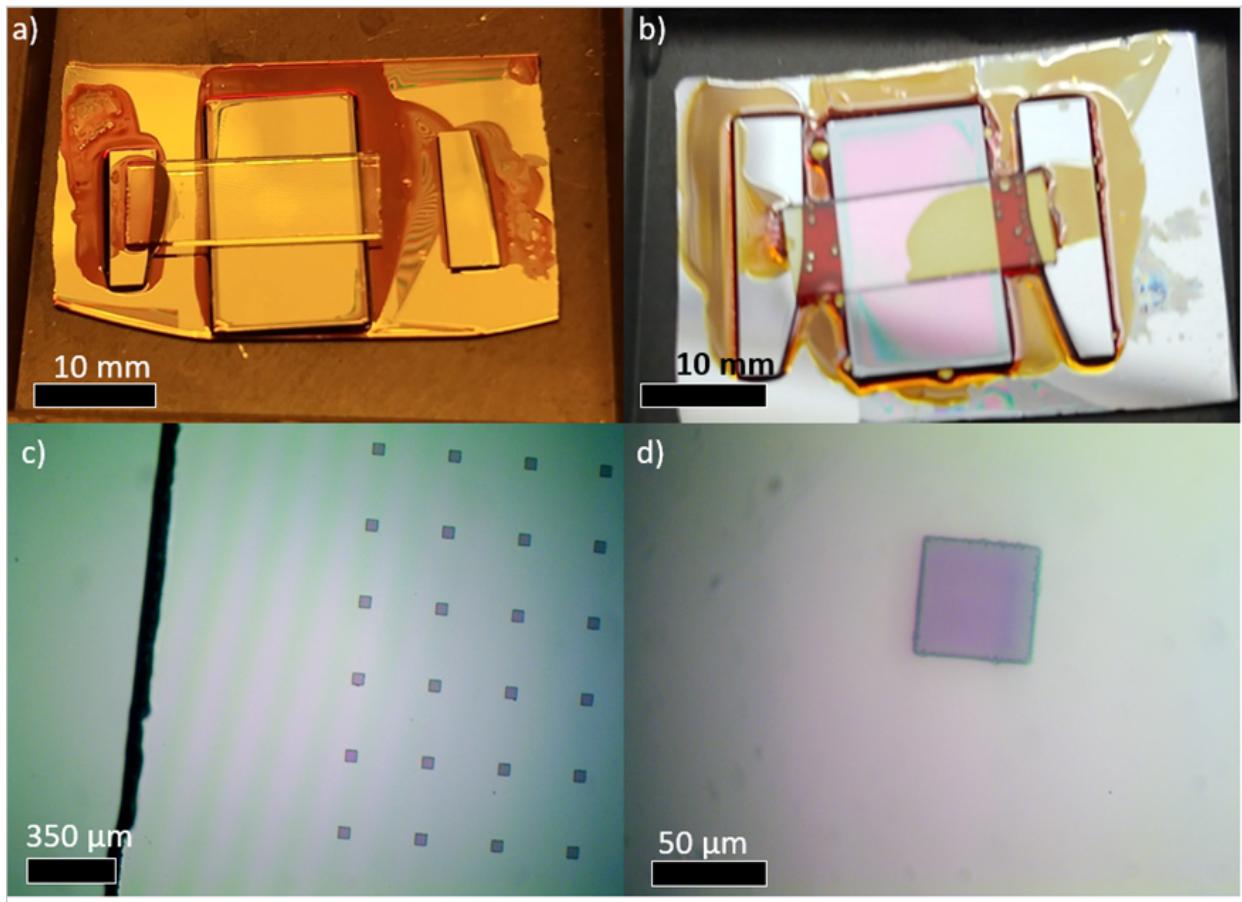


Figure B.1: (a) A flip-chip with sandwiched quartz and Si surfaces separated by a grid of $50\text{ }\mu\text{m}$ -wide squares spaced by $350\text{ }\mu\text{m}$. (b) A flip-chip where the quartz and silicon are separated by $\approx 1\text{ }\mu\text{m}$ micron of spin-coated PMMA. (c) The grid of photoresist squares under quartz during alignment. (d) A single $50\text{ }\mu\text{m}$ -wide square.

Appendix C: Transferred contacts for high-quality contact to 2D
semiconductors

Appendix D: Gate-tunable photoluminescence in hBN-encapsulated MoS₂

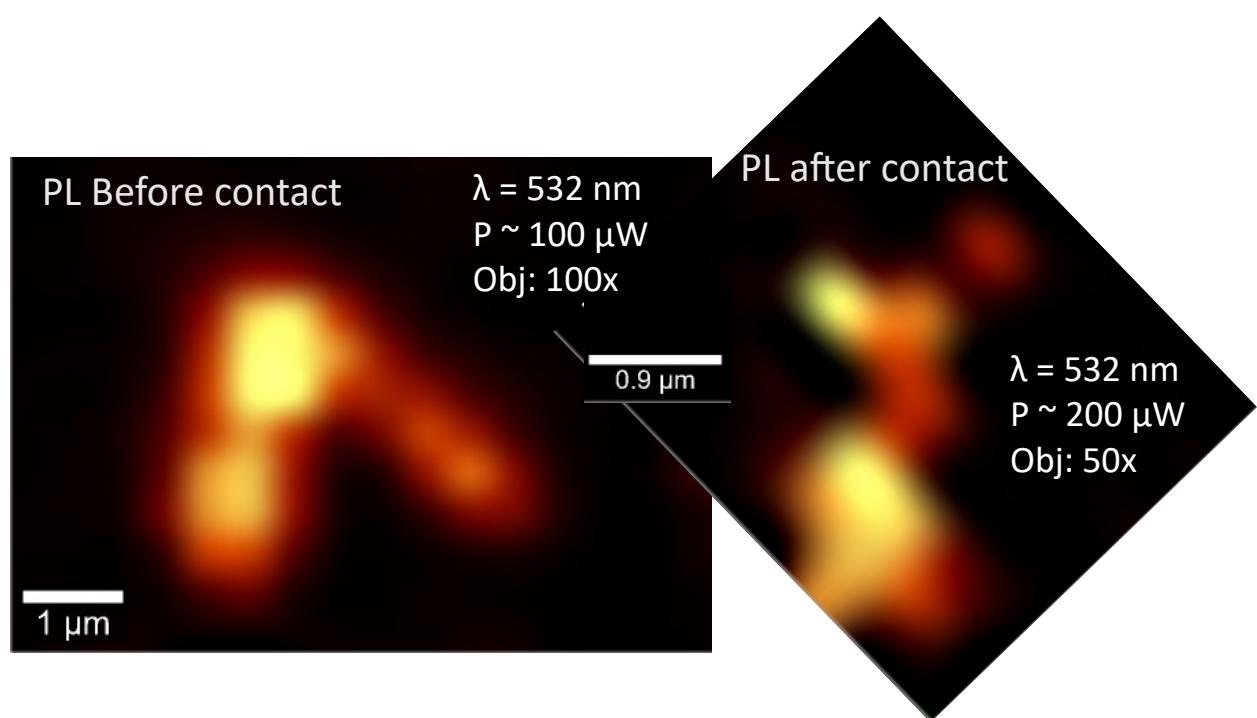


Figure D.1:

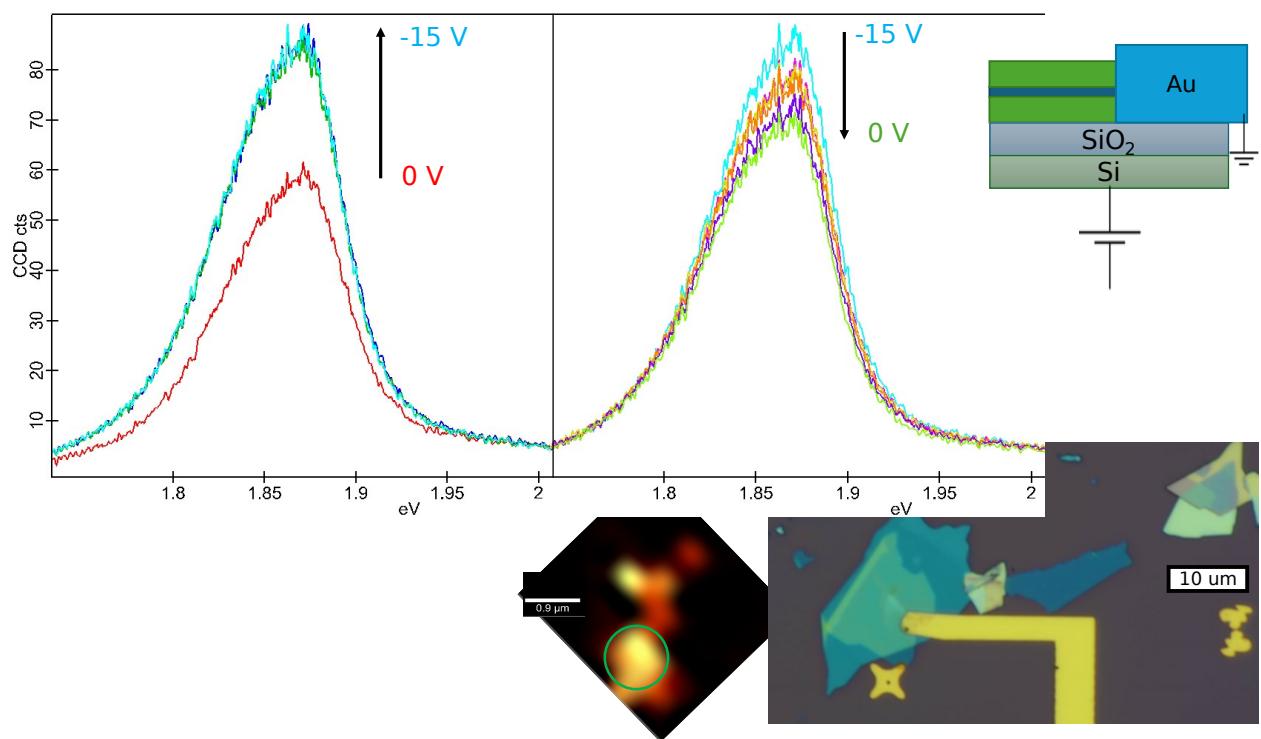


Figure D.2:

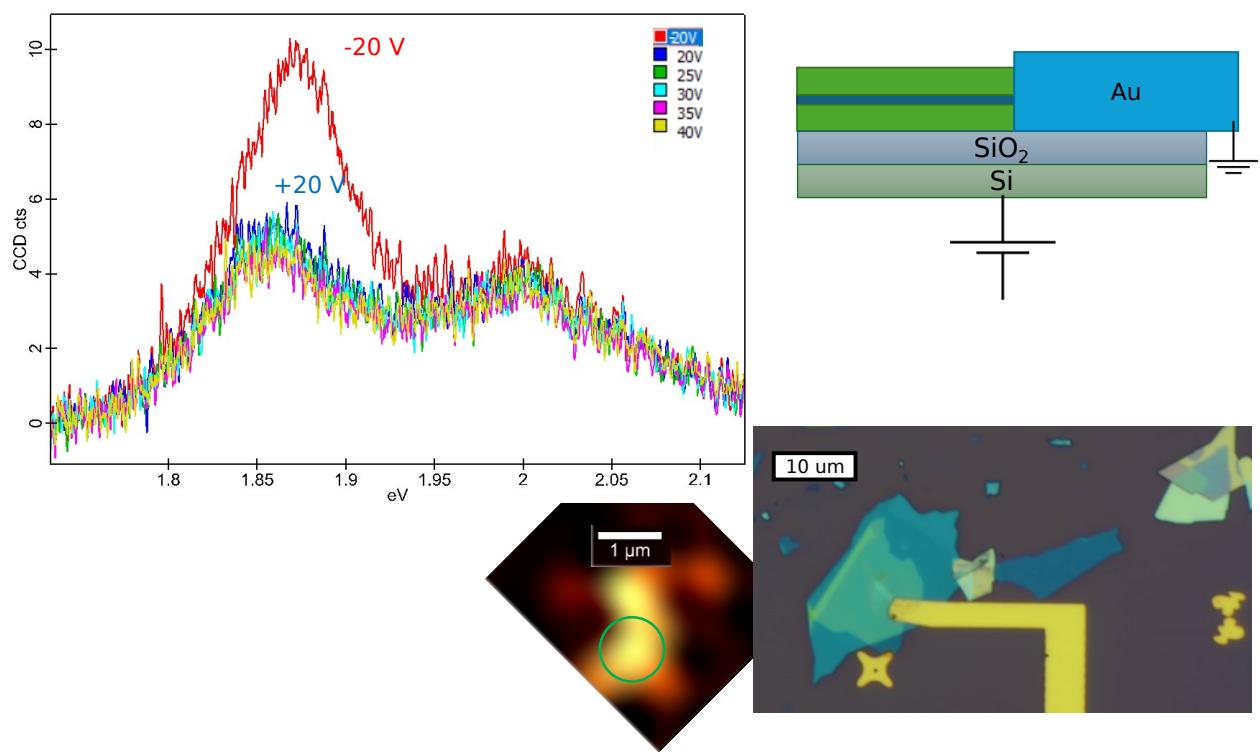


Figure D.3:

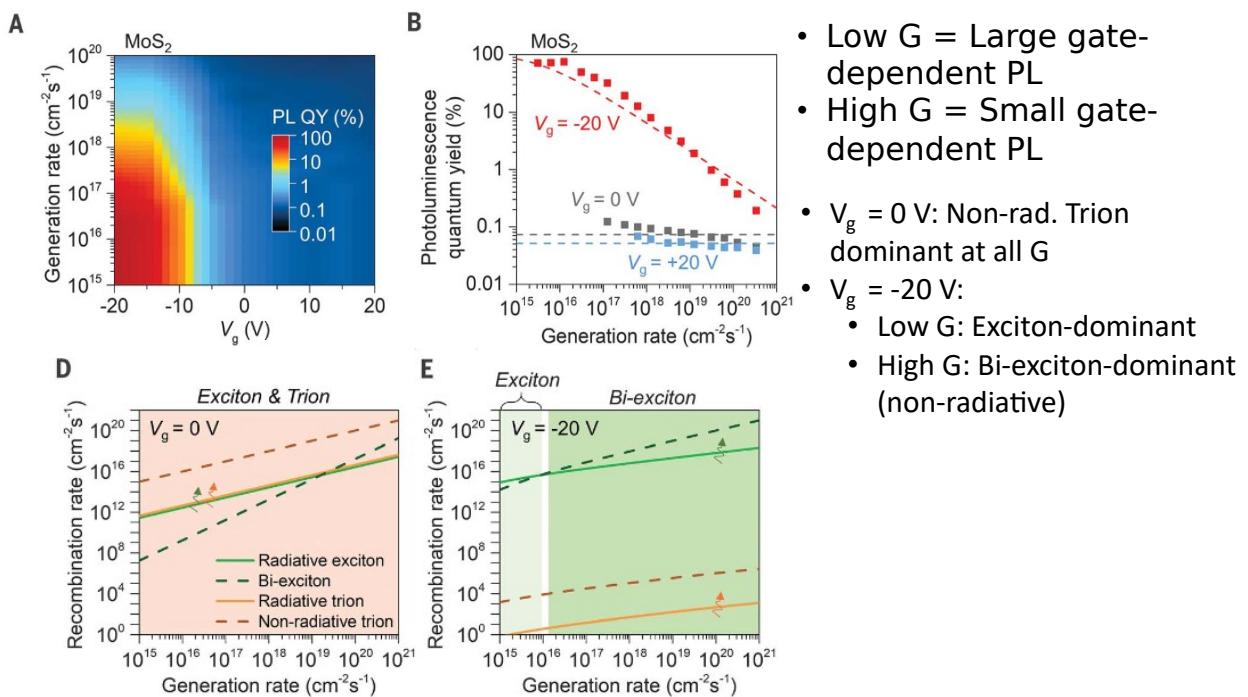


Figure D.4:

